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Everywhere you imagine. RENESAS

R0P7780LC0011RL

User's Manual

SH7780 CPU Board

User's Manual

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Renesas Technology
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• READ this user's manual before using this product.
• KEEP the user's manual handy for future reference.
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This Product:
In this manual, this product points out the following product which Renesas Solutions Corporation manufactured.
A user's user system and host machine are not included.

Purpose of the Product:

This product is a device to support the development of a system that uses the SuperH Risc engine Family SH7751R of Renesas 32-bit RISC MCUs. It provides support for system development in both software and hardware. Be sure to use this product correctly according to said purpose of use. Please avoid using this product for other than its intended purpose of use.

For those who use this product:
This product can only be used by those who have carefully read the user's manual and know how to use it. Use of this product requires the basic knowledge of electric circuits, logical circuits, and MCUs.

Precautions to be Taken when Using This Product:

(1) This product is a development supporting unit for use in your program development and evaluation stages. In mass-producing your program you have finished developing, be sure to make a judgment on your own risk that it can be put to practical use by performing integration test, evaluation, or some experiment else.
(2) In no event shall Renesas Solutions Corporation be liable for any consequence arising from the use of this product.
(3) Renesas Solutions Corporation strives to renovate or provide a workaround for product malfunction at some charge or without charge. However, this does not necessarily mean that Renesas Solutions Corporation guarantees the renovation or the provision under any circumstances.
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(7) This product is a product used for development of a program, and an evaluation stage. It cannot include in a user's product and cannot mass-produce.
(8) Even if it is the case where fault is in the device carried in this product, it does not exchange for the fault repair article of a device.
(9) Operation of all CF cards cannot be guaranteed.
(10) Connection with the apparatus of all LAN interfaces cannot be guaranteed.
(11) When you do not use it for a long time, please pull out and keep a power supply plug from a plug socket etc. for safety.
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Figures:

Some figures in this user's manual may show items different from your actual system.

* Compact Flash™ is the registered trademark of SanDisk Corporation

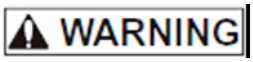
Precautions for Safety

Definitions of Signal Words

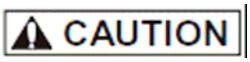
In both the General Information Manual and on the product itself, several icons are used to insure proper handling of this product and also to prevent injuries to you or other persons, or damage to your properties.
This chapter describes the precautions which should be taken in order to use this product safely and properly.
Be sure to read this chapter before using this product.

This symbol represents a warning about safety. It is used to arouse caution about a potential danger that will possibly inflict an injury on persons. To avoid a possible injury or death, please be sure to observe the safety message that follows this symbol.

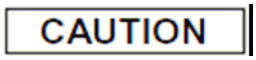
DANGER indicates an imminently dangerous situation that will cause death or heavy wound unless it is avoided. However, there are no instances of such danger for the product presented in this manual.



WARNING indicates a potentially dangerous situation that will cause death or heavy wound unless it is avoided.



CAUTION indicates a potentially dangerous situation that will cause a slight injury or a medium-degree injury unless it is avoided.



CAUTION with no safety warning symbols attached indicates a potentially dangerous situation that will cause property damage unless it is avoided.

NOTE emphasizes essential information.

In addition to the five above, the following are also used as appropriate.

△ means WARNING or CAUTION.
Example:

CAUTION AGAINST AN ELECTRIC SHOCK

⃠ means PROHIBITION.
Example:

DISASSEMBLY PROHIBITED

● means A FORCIBLE ACTION.
Example:

UNPLUG THE POWER CABLE FROM THE RECEPTACLE.

CAUTION

Warnings for AC Power Supply:

- If If the attached AC power cable does not fit the receptacle, do not alter the AC power cable and do not plug it forcibly. Failure to comply may cause electric shock and/or fire.
- Use an AC power cable which complies with the safety standard of the country.
- Do not touch the plug of the AC power cable when your hands are wet. This may cause electric shock.
- This product is connected signal ground with frame ground. If your developing product is transformless (not having isolation transformer of AC power), this may cause electric shock. Also, this may give an unrepairable damage to this product and your developing one.
- While developing, connect AC power of the product to commercial power through isolation transformer in order to avoid these dangers.
- If other equipment is connected to the same branch circuit, care should be taken not to overload the circuit.

- If you smell a strange odor, hear an unusual sound, or see smoke coming from this product, then disconnect power immediately by unplugging the AC power cable from the outlet.
- Do not use this as it is because of the danger of electric shock and/or fire. In this case, contact your local distributor.
- Before setting up this product and connecting it to other devices, turn off power or remove a power cable to prevent injury or product damage.

Warnings to Be Taken for This Product:

- Do not disassemble or modify this product. Personal injury due to electric shock may occur if this product is disassembled and modified.
- Make sure nothing falls into the cooling fan on the top panel, especially liquids, metal objects, or anything combustible.

Warning for Installation:

- Do not set this product in water or areas of high humidity. Make sure that the product does not get wet. Spilling water or some other liquid into the product may cause unrepairable damage.
- Please use this product indoors.

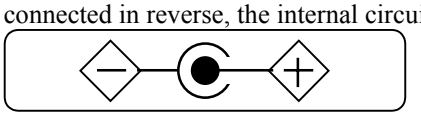
Warning for Use Environment:

- This equipment is to be used in an environment with a maximum ambient temperature of 35°C. Care should be taken that this temperature is not exceeded.

CAUTION

Note on Connecting the Power Supply:

- Do not use any power cable other than the one that is included with the product.
- At the time of connection with installation of this product or other equipments, please extract an AC/DC adaptor from a plug socket and prevent an injury and an accident.
- Pay attention to the polarities of the power supply. If its positive and negative poles are connected in reverse, the internal circuit may be broken.



Power supply injection :

- Once the power is turned off, wait for about 10 seconds before turning it back on again.

Cautions to Be Taken for Handling This Product:

- Handle the product with caution, taking care not to apply strong mechanical shock to the product by dropping or letting it fall down.
- Do not touch the communication interface connector pins or other connector pins directly with your hand. Static electricity from your body may break down the internal circuit of the product.
- Do not pull the product by the cable connecting to a board in it. Do not hold down a board while you pull the other end of it. The cable may break.

Contents

1. Outline

1.1. Package Components

This product is constituted by the following board and parts. When opened, please check whether it has gathered altogether.

Table 1.1.1 The contents list of packing

Item	Description	Quantity
R0P7780LC0011RL	SH7780 CPU board	1
FROM Board (Bus width is 32bit 64M Byte)	Within boot loader	1
Debug Interface board (DB board)	For R0P7780LC0011RL	1
CD-ROM	User's manual , Sample program etc.	1

* If there is any question or doubt about the packaged product, contact your local distributor.

1.2. System Configuration

1.2.1. System Configuration

Figure 1.2.1 shows the system configuration.

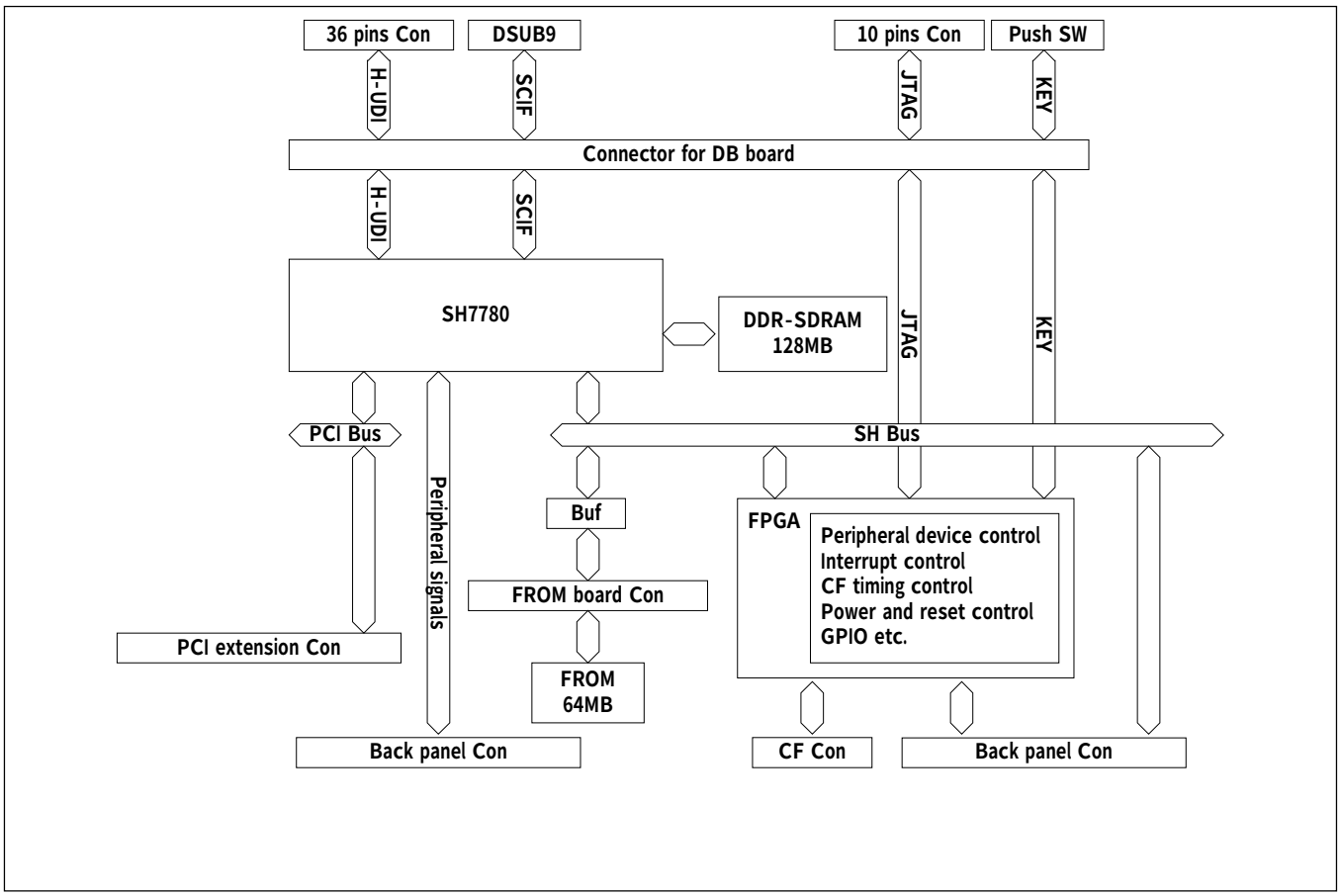


Figure 1.2.1 R0P7780LC0011RL system configuration

1.2.2. Names and Functions of each part of the System

Figure 1.2.2 shows the names of parts reference.

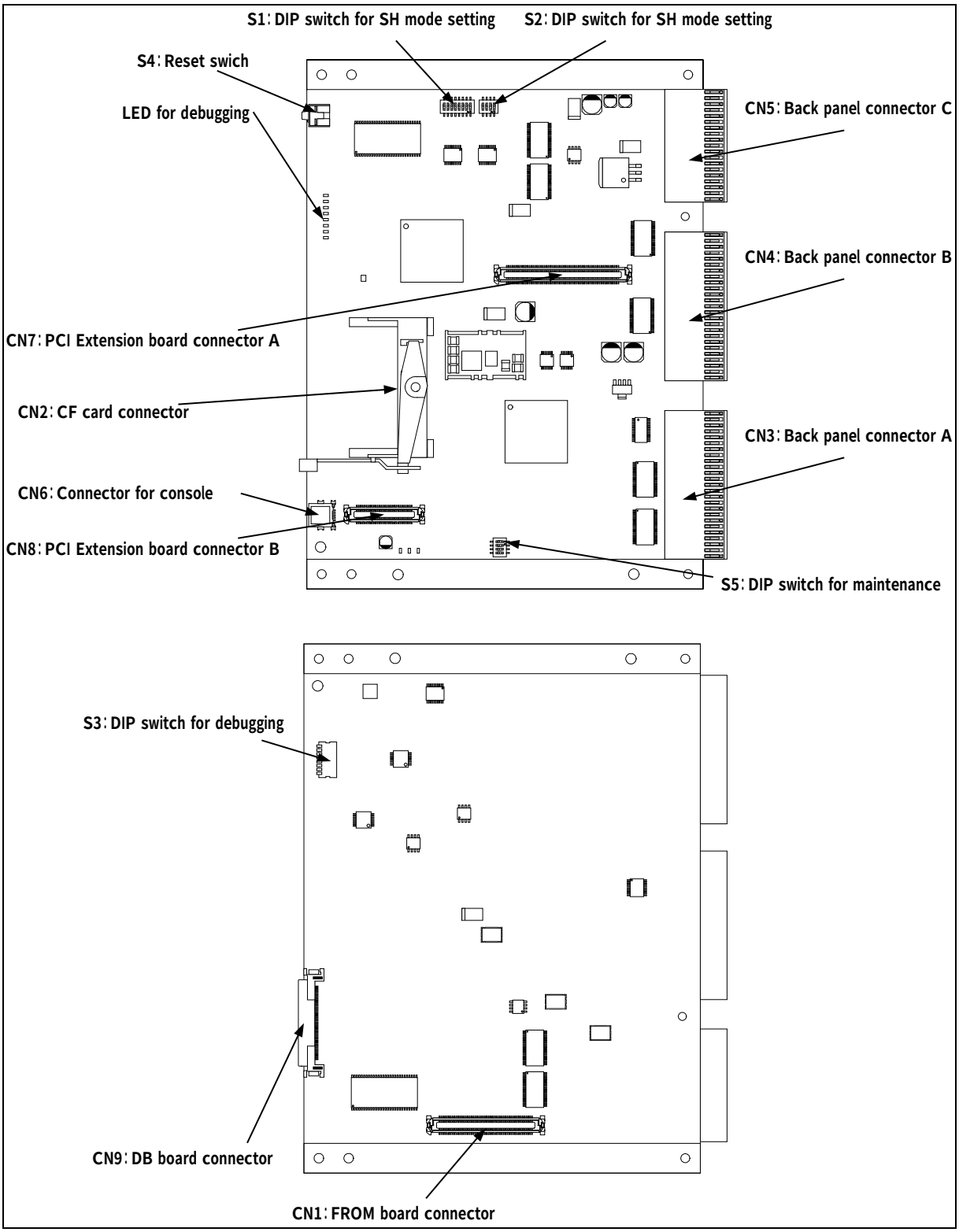


Figure 1.2.2 Name of R0P7780LC0011RL's parts reference

1.3. Setup Method (Up to Boot loader starting)

1.3.1. Connection method which used RS232C cable

The setup diagram of this product is shown in Fig. 1.3.1. The environment required for the setup of this product is as follows.

■R0P0400LP0011RL(Power supply board)

■Console Terminal (PC)

■RS232C cable(Cross)

Please prepare CF card, a CRT monitor, network environment, etc. of a user if needed.

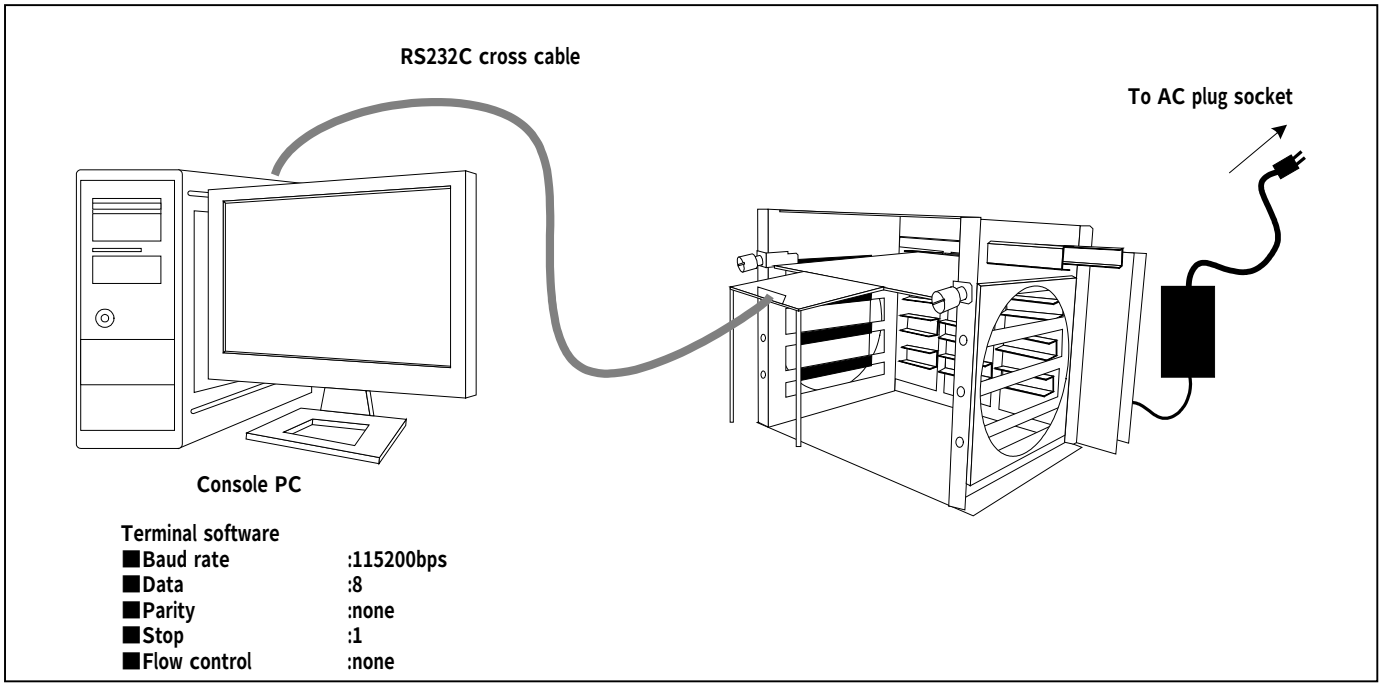


Figure 1.3.1 Set up method

(1) Please attach an attached FROM board in CN1 mounted in the solder side of R0P7780LC0011RL.

CAUTION
Where the power supply of this product is intercepted, please be sure to make connection of a FROM board. Moreover, be careful of poor contact of a FROM board. The mistaken usage leads to destruction of this product.

(2) Please attach DB board in R0P7780LC0011RL.

CAUTION
Where the power supply of this product is intercepted, please be sure to make connection of DB board. Moreover, be careful of poor contact of DB board. The mistaken usage leads to destruction of this product.

(3) Connect CN1 and the terminal for consoles of DB board with a RS232C cross cable.

(4) Start terminal software on the terminal for consoles.

(baudrate:115200bps, data:8bit, parity:none, stop bit:1bit, flow control:none)

(5) Insert an attached AC/DC adaptor in CN10 of R0P0400LP011RL, and connect with a plug socket.

(6) Push S1 of R0P0400LP011RL, and carry out a power supply injection.

CAUTION
If R0P0400LP0011RL's S1 is pushed again, power supply interception is possible. However, while using CF card, please carry out power supply interception processing in carried FPGA. When S1 is pushed during CF card operation and power supply interception is performed, there is possibility of destruction of CF card. Please refer to the clause of FPGA functional explanation about the specification of FPGA.

1.4. Specification List

Table 1.4.1 shows a list of specifications.

Table 1.4.1 R0P7780LC0011RL Specifications

Item	Description
CPU	R8A77800A (Renesas Technorogy) ・Input Clock: 33.33MHz ・CPU Clock(I): 400MHz (When Mode 0 set) ・Bus Clock(B): 100MHz (When Mode 0 set) ・Peripheral Clock(P): 50MHz (When Mode 0 set) ・DDR SDRAM clock: 160MHz (When Mode 0 set) ・PCI Bus: 33MHz (4ch) ・Package: 449pinBGA (1.27mm pitch)
Memory	FROM board:S29PL127J60TFI130 (Spansion) ・FROM:64M Byte・32bit Bus Access
	EDD5116ADTA -6B(x 2) (Elpida) ・DDR-SDAM:128MB・32 bit bus witdh
FPGA	EP1C20F400C8N (ALTERA) ROM for configration: EPCS4SI8N
LED	・LED for debugging (x 8) ・Status LED (x 6)
Switch	・RESET switch (x 1) ・DIP switch for debugging (8bit x 1) ・DIP switch for SH mode setting(8bit x 1、4bit x 1)
Compact Flash Card Connector	Header: ICM-MA50H-SS52-1151(LF)(SN) (JST) Ejector: ICM-MAE-R01 (JST)
Connector	FROM board connector:52837-1079 (Molex)
	Back panel connector: PCN21A-125SB-2PF-G(78) (HIROSE) PCN21A-95SB-2PF-G(78) (HIROSE)
	DB board connector : 87BFN-50R-3F (KEL)
	PCI Extnsion board connector: 52837-1279 (Molex) 52837-0679 (Molex)

Item	Description
Power IN	From R0P7780LC0011RL
Size	Size: 177.85mm × 133.00mm
Operating temperature	5 to 35°C (no dew)
Storage temperature	-10 to 60°C (no dew)

1.5. Address Map

Figure 1.5.1 shows Address Map. Please refer to the clause of FPGA functional explanation about the specification of FPGA.

H'0000_0000 H'03FF_FFFF	Area 0	32bit	FROM Area (64MB)
H'0400_0000 H'040F_FFFF	Area 1	16bit	FPGA Area (1MB)
H'0410_0000 H'041F_FFFF			AX88796 Area (1MB)
H'0420_0000 H'07FF_FFFF			External Area (62MB)
H'0800_0000 H'0BFF_FFFF	Area 2	32bit	DDR-SDRAM Area (64MB)
H'0C00_0000 H'0FFF_FFFF	Area 3	32bit	DDR-SDRAM Area (64MB)
H'1000_0000 H'13FF_FFFF	Area 4	8/16/32 bit	External Area (64MB)
H'1400_0000 H'17FF_FFFF	Area 5	16bit	Compact FLASH Area (64MB)
H'1800_0000 H'1BFF_FFFF	Area 6	8/16/32 bit	External Area (64MB)

Figure 1.5.1 SH7780 address map

＊The AX88796 mapped in area 1 is the LAN controller mounted in R0P0400LP0011RL.

2. Functional Specification

2.1. Switches Specification

2.1.1. DIP Switch for CPU Mode Setup 1

S1 is the Dip switch for a mode setup of operation of SH7780. The S1 specification is shown in Table 2.1.1 and the S1appearance figure is shown in Fig. 2.1.1. It is in a shading state at the time of shipment.

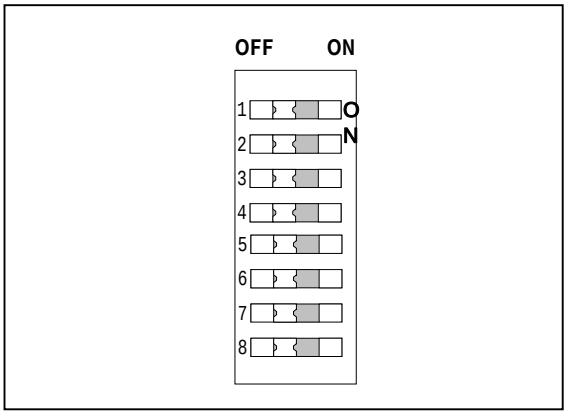


Figure 2.1.1 S1 appearance figure

Table 2.1.1 S1 specification

Switch	Connection terminal	ON	OFF	Function
S3-1	SH7780_MD3	H	L	MODE4 / MODE3 / Bus width: L / L / MPX IF; L / H / 8 bit; H / L / 16 bit; H / H / 32 bit
S3-2	SH7780_MD4	H	L	
S3-3	SH7780_MD5	H	L	A setup of an endian L:BIG Endian H:Little Endian
S3-4	SH7780_MD6	H	L	PCI mode L:PCI Target H:PCI Master
S3-5	SH7780_MD8	H	L	Clock Mode L:external clock H: crystal resonator
S3-6	NC	H	L	
S3-7	NC	H	L	
S3-8	NC	H	L	

2.1.2. DIP Switch for CPU Mode Setup 2

S2 is the Dip switch for a mode setup of operation of SH7780. The S1 specification is shown in Table 2.1.2.1 and the S2appearance figure is shown in Fig. 2.1.2. It is in a shading state at the time of shipment.

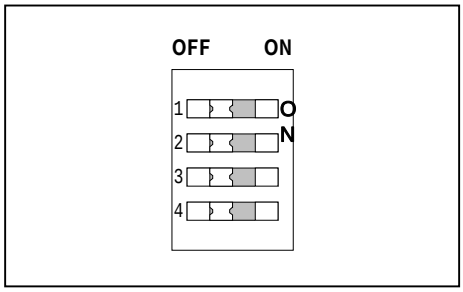


Figure 2.1.2 S2 appearance figure

Table 2.1.2.1 S2 specification

Switch	Connection terminal	ON	OFF	Function
S1-1	SH7780_MD0	H	L	Clock mode setting
S1-2	SH7780_MD1	H	L	
S1-3	SH7780_MD2	H	L	
S1-4	SH7780_MD7	H	L	

The clock operation mode of SH7780 is shown in Table 2.1.2.2.

Table 2.1.2.2 SH7780 clock mode matrix

Clock Mode	Mode control matrix				PLL 1、2	The rate of frequency multiplication (clock for an input)					FRQCR Initial value
	MODE7	MODE2	MODE1	MODE0		Ick	SHck	Pck	DDRck	Bck	
0	L	L	L	L	ON	x 12	x 6	x 3/2	x 24/5	x 3	H'1023_3335
1	L	L	L	H	ON	x 12	x 6	x 1	x 24/5	x 2	H'1024_4336
2	L	L	H	L	ON	x 12	x 6	x 3/2	x 24/5	x 3/2	H'1025_5335
3	L	L	H	H	ON	x 12	x 6	x 1	x 24/5	x 1	H'1026_6336
12	H	H	L	L	ON	x 12	x 4	x 1	x 4	x 2	H'1044_4346

CAUTION

Combination other than the above-mentioned setup of the clock operation mode of SH7780 is prohibition of a setup.

2.1.3. DIP Switch for Debugging

S3 is a DIP switch for debugging. It can connect with FPGA and can refer to by the dedicated register. It can be used of a user. Please refer to the clause of FPGA functional explanation about the specification of FPGA. The S3 appearance figure is shown in Table 2.1.3 and the S3 specification is shown in Fig. 2.1.3.

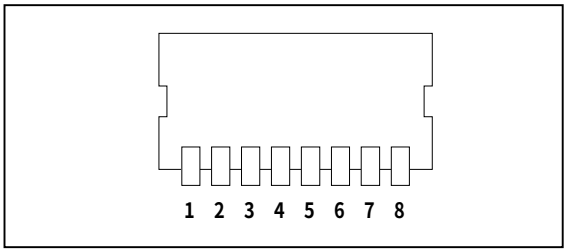


Figure 2.2.3 S3 appearance figure

Table 2.2.3 S3 specification

Switch	Connection terminal	ON	OFF	Function
S3-1	FPGA	H	L	Reference is possible at FPGA
S3-2	FPGA	H	L	
S3-3	FPGA	H	L	
S3-4	FPGA	H	L	
S3-5	FPGA	H	L	
S3-6	FPGA	H	L	
S3-7	FPGA	H	L	
S3-8	FPGA	H	L	

2.1.4. System Reset Switch

S4 is a system-reset switch. A reset pulse is generated to this timing in each device under S4 swich-pushing. The explanation about a reset signal is indicated to "2.10 Reset signal".

2.2. LED Specification

2.2.1. LED for the SH7780 Status

LED1 is LED for a status display of SH7780. It has connected with STATUS1, and STATUS0 of SH7780 ports. Functional assignment of LED is shown in Table 2.3.1.

Table 2.3.1 LED functional assignment.

LED	Function	Status
LED1	Reset	Lighting off
	Sleep	Green lighting
	Standby	Red lighting
	Nomal	Orange lighting

2.2.2. LED for the CF Card

LED9, LED10, and LED11 are LED for CF cards. It is automatically controlled by CF card insertion. LED functional assignment is shown in Table 2.3.2.

Table 2.3.2 LED functional assignment

LED	Function	Status
LED9	At the time of the power supply to CF card	Lighting
LED10	At the time of CF card insertion	Lighting
LED11	At the time of CF Device Active	Lighting

2.2.3. LED for Debugging

LED0 to LED7 are LED for debugging. It is controllable by FPGA. Please refer to the clause of FPGA functional explanation about the specification of FPGA.

2.3. Memories

The list of the memory carried in this product is shown in Table 2.3.1.

Table2.3.1.1 memory list

Classification	Start address	Size	Bus width	Note
External FROM	H'0000_0000	64MB	32bit	At the time of mounting of an enclosed FROM board
External DDR-SDRAM	H'0800_0000	128MB	32bit	

2.4. Back Panel Connector

2.4.1. Back Panel Connector A

CN3 is used for back board connection. It inserts in the front panel connector A of R0P0400LP0011RL. The general-view figure of the back panel connector A is shown in Fig. 2.4.1, and signal arrangement is shown in Table 2.4.1.

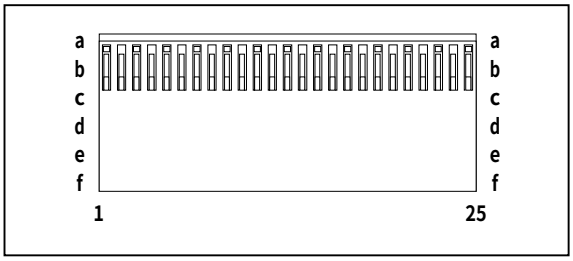


Figure 2.9.1 Back panel connector A

Table2.9.1 Signal arrangement of back panel connector A

Pin number	Signal name	Function	Note
1a	+5.0V	Power Supply	
2a	+5.0V	Power Supply	
3a	GND	Ground	
4a	D4	Data Bus 4	
5a	GND	Ground	
6a	D9	Data Bus 9	
7a	GND	Ground	
8a	D14	Data Bus 14	
9a	D19	Data Bus 19	
10a	GND	Ground	
11a	D24	Data Bus 24	
12a	D29	Data Bus 29	
13a	GND	Ground	
14a	EX_GPIO01	FPGA extension connector GPIO port 1	
15a	EX_GPIO03	FPGA extension connector GPIO port 3	
16a	EX_GPIO05	FPGA extension connector GPIO port 5	
17a	EX_GPIO07	FPGA extension connector GPIO port 7	
18a	HAC_RESET#	HAC Reset	
19a	GND	Ground	
20a	R.S.V11	Reserved 11	
21a	R.S.V12	Reserved 12	
22a	R.S.V17	Reserved 17	
23a	R.S.V22	Reserved 22	
24a	GND	Ground	
25a	GND	Ground	

Pin number	Signal name	Function	Note
1b	+5.0V	Power Supply	
2b	+5.0V	Power Supply	
3b	GND	Ground	
4b	D3	Data Bus 3	
5b	GND	Ground	
6b	D8	Data Bus 8	
7b	GND	Ground	
8b	D13	Data Bus 13	
9b	D18	Data Bus 18	
10b	GND	Ground	
11b	D23	Data Bus 23	
12b	D28	Data Bus 28	
13b	GND	Ground	
14b	EX_GPIO00	FPGA extension connector GPIO port 0	
15b	EX_GPIO02	FPGA extension connector GPIO port 2	
16b	EX_GPIO04	FPGA extension connector GPIO port 4	
17b	EX_GPIO06	FPGA extension connector GPIO port 6	
18b	GND	Ground	
19b	GND	Ground	
20b	HAC_BITCLK	HAC bit clock	
21b	SSI_CLK	SSI serial bit clock	
22b	R.S.V16	Reserved 16	
23b	R.S.V21	Reserved 21	
24b	R.S.V24	Reserved 24	
25b	GND	Ground	

Pin number	Signal name	Function	Note
1c	+5.0V	Power Supply	
2c	+5.0V	Power Supply	
3c	GND	Ground	
4c	D2	Data Bus 2	
5c	GND	Ground	
6c	D7	Data Bus 7	
7c	GND	Ground	
8c	D12	Data Bus 12	
9c	D17	Data Bus 17	
10c	GND	Ground	
11c	D22	Data Bus 22	
12c	D27	Data Bus 27	
13c	GND	Ground	
14c	EXT_CS0#	External Chip Select 0	
15c	EXT_CS1#	External Chip Select 1	
16c	EX_IRQn	External Interrupt	
17c	RDY#	Ready	
18c	IIC_SDA	IIC Data	
19c	GND	Ground	
20c	HAC_SYNC	HAC Frame Sync	
21c	SSI_SDATA	SSI Data	
22c	R.S.V15	Reserved 15	
23c	R.S.V20	Reserved 20	
24c	R.S.V23	Reserved 23	
25c	GND	Ground	

Pin number	Signal name	Function	Note
1d	+5.0V	Power Supply	
2d	+5.0V	Power Supply	
3d	GND	Ground	
4d	D1	Data Bus 1	
5d	GND	Ground	
6d	D6	Data Bus 6	
7d	GND	Ground	
8d	D11	Data Bus 11	
9d	D16	Data Bus 16	
10d	GND	Ground	
11d	D21	Data Bus 21	
12d	D26	Data Bus 26	
13d	D31	Data Bus 31	
14d	BREQ0#	Bus Request 0	
15d	GND	Ground	
16d	BACK0	Bus Acknowledge 0	
17d	GND	Ground	
18d	IIC_SCL	IIC clock	
19d	GND	Ground	
20d	HAC_SDATAI	HAC Data Input	
21d	SSI_WS	SSI Word Select	
22d	R.S.V14	Reserved 14	
23d	R.S.V19	Reserved 19	
24d	GND	Ground	
25d	+12V	Power Supply	

Pin number	Signal name	Function	Note
1e	+5.0V	Power Supply	
2e	+5.0V	Power Supply	
3e	GND	Ground	
4e	D0	Data Bus 0	
5e	GND	Ground	
6e	D5	Data Bus 5	
7e	GND	Ground	
8e	D10	Data Bus 10	
9e	D15	Data Bus 15	
10e	GND	Ground	
11e	D20	Data Bus 20	
12e	D25	Data Bus 25	
13e	D30	Data Bus 30	
14e	GND	Ground	
15e	CKIO	SH CKIO	
16e	GND	Ground	
17e	CLKIN	External Clock Input	
18e	GND	Ground	
19e	GND	Ground	
20e	HAC_SDATAO	HAC Data Output	
21e	SSI_SCK	SSI serial bit clock	
22e	R.S.V13	Reserved 13	
23e	R.S.V18	Reserved 18	
24e	GND	Ground	
25e	+12V	Power Supply	

2.4.2. Back Panel Connector B

CN4 is used for back board connection. It inserts in the front panel connector B of R0P0400LP0011RL. The general-view figure of the back panel connector B is shown in Fig. 2.4.2, and signal arrangement is shown in Table 2.4.2.

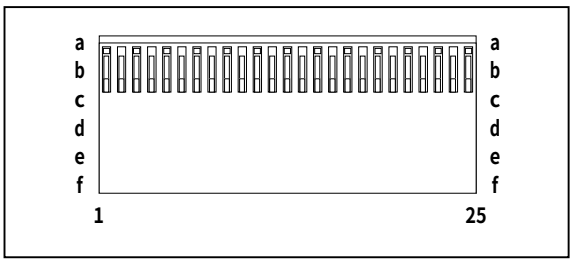


Figure 2.4.2 Back panel connector B

Table2.4.2 Signal arrangement of back panel connector B

Pin number	Signal name	Function	Note
1a	+3.3V	Power Supply	
2a	+3.3V	Power Supply	
3a	GND	Ground	
4a	A25	Address Bus 25	
5a	A20	Address Bus 20	
6a	A15	Address Bus 15	
7a	GND	Ground	
8a	A10	Address Bus 10	
9a	A5	Address Bus 5	
10a	R.S.V0	Reserved0	
11a	R.S.V3	Reserved3	
12a	R.S.V7	Reserved7	
13a	GND	Ground	
14a	CS3#	Chip Select 3	
15a	GND	Ground	
16a	GND	Ground	
17a	GND	Ground	
18a	DREQ0#	DMA Request 0	
19a	DACK0	DMA Acknowledge 0	
20a	WAIT0#	External wait 0	
21a	WAIT4#	External wait 4	
22a	GND	Ground	
23a	IRQ0#	External Interrupt 0	
24a	IRQ4#	External Interrupt 4	
25a	GND	Ground	

Pin number	Signal name	Function	Note
1b	+3.3V	Power Supply	
2b	+3.3V	Power Supply	
3b	GND	Ground	
4b	A24	Address Bus 24	
5b	A19	Address Bus 19	
6b	A14	Address Bus 14	
7b	GND	Ground	
8b	A9	Address Bus 9	
9b	A4	Address Bus 4	
10b	R.S.V1	Reserved1	
11b	R.S.V4	Reserved4	
12b	WE0#	Write Enable 0	
13b	GND	Ground	
14b	CS2#	Chip Select 2	
15b	CS6#	Chip Select 6	
16b	PRESET#	Power On Reset	
17b	GND	Ground	
18b	DREQ1#	DMA Request 1	
19b	DACK1	DMA Acknowledge 1	
20b	WAIT1#	External wait 1	
21b	WAIT5#	External wait 5	
22b	GND	Ground	
23b	IRQ1#	External Interrupt 1	
24b	IRQ5#	External Interrupt 5	
25b	GND	Ground	

Pin number	Signal name	Function	Note
1c	+3.3V	Power Supply	
2c	+3.3V	Power Supply	
3c	GND	Ground	
4c	A23	Address Bus 23	
5c	A18	Address Bus 18	
6c	A13	Address Bus 13	
7c	GND	Ground	
8c	A8	Address Bus 8	
9c	A3	Address Bus 3	
10c	R.S.V2	Reserved2	
11c	R.S.V5	Reserved5	
12c	WE1#	Write Enable 1	
13c	GND	Ground	
14c	CS1#	Chip Select 1	
15c	CS5#	Chip Select 5	
16c	GND	Ground	
17c	GND	Ground	
18c	DREQ2#	DMA Request 2	
19c	DACK2	DMA Acknowledge 2	
20c	WAIT2#	External wait 2	
21c	WAIT6#	External wait 6	
22c	GND	Ground	
23c	IRQ2#	External Interrupt 2	
24c	IRQ6#	External Interrupt 6	
25c	GND	Ground	

Pin number	Signal name	Function	Note
1d	+3.3V	Power Supply	
2d	+3.3V	Power Supply	
3d	GND	Ground	
4d	A22	Address Bus 22	
5d	A17	Address Bus 17	
6d	A12	Address Bus 12	
7d	GND	Ground	
8d	A7	Address Bus 7	
9d	A2	Address Bus 2	
10d	GND	Ground	
11d	R.S.V6	Reserved6	
12d	WE2#	Write Enable 2	
13d	GND	Ground	
14d	CS0#	Chip Select 0	
15d	CS4#	Chip Select 4	
16d	RD/WR#	Read/Write Enable	
17d	GND	Ground	
18d	DREQ3#	DMA Request 3	
19d	DACK3	DMA Acknowledge 3	
20d	WAIT3#	External wait 3	
21d	WAIT7#	External wait 7	
22d	GND	Ground	
23d	IRQ3#	External Interrupt 3	
24d	IRQ7#	External Interrupt 7	
25d	GND	Ground	

Pin number	Signal name	Function	Note
1e	+3.3V	Power Supply	
2e	+3.3V	Power Supply	
3e	GND	Ground	
4e	A21	Address Bus 21	
5e	A16	Address Bus 16	
6e	A11	Address Bus 11	
7e	GND	Ground	
8e	A6	Address Bus 6	
9e	A1	Address Bus 1	
10e	A0	Address Bus 0	
11e	GND	Ground	
12e	WE3#	Write Enable 3	
13e	GND	Ground	
14e	BS#	Bus Start	
15e	GND	Ground	
16e	RD#	Read Enable	
17e	GND	Ground	
18e	GND	Ground	
19e	DRAK0	DMAC0 Request Acknowledge	
20e	GND	Ground	
21e	POW_OFF#	System Power OFF	
22e	SYS_RESET#	System Reset	
23e	R.S.V8	Reserved 8	
24e	R.S.V9	Reserved 9	
25e	R.S.V10	Reserved 10	

2.4.3. Back Panel Connector C

CN5 is used for back board connection. It inserts in the front panel connector C of R0P0400LP0011RL. The general-view figure of the back panel connector C is shown in Fig. 2.4.3, and signal arrangement is shown in Table 2.4.3.

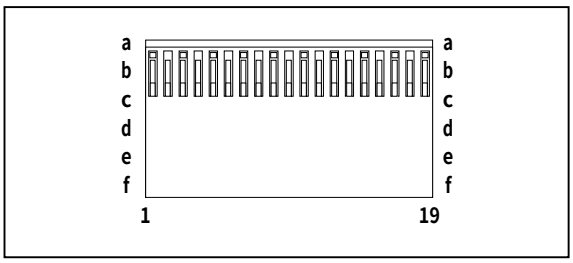


Figure 2.4.3 Back panel connector C

Table2.4.3 Signal arrangement of back panel connector C

Pin number	Signal name	Function	Note
1a	A_3.3V	Analog 3.3V Power Supply	
2a	AN0	Analog Input 0	
3a	AN2	Analog Input 2	
4a	AN3	Analog Input 3	
5a	GND	Ground	
6a	D_R4	LCD Data Bus Red 4	
7a	D_G2	LCD Data Bus Green 2	
8a	D_B0	LCD Data Bus Blue 0	
9a	D_B5	LCD Data Bus Blue 5	
10a	GND	Ground	
11a	RTC_32K	RTC Clock 32KHz	
12a	RTC_IRQA#	RTC Interrupt A	
13a	RTC_IRQB#	RTC Interrupt B	
14a	TP_DOUT	Touch Panel Data Output	
15a	CAN_ERR#	CAN Bus Error	
16a	POW_INT#	Interrupt for Amperometries	
17a	POW_D1	Data Bus 1 for Amperometries	
18a	GND	Ground	
19a	GND	Ground	

Pin number	Signal name	Function	Note
1b	A_3.3V	Analog 3.3V Power Supply	
2b	AN_GND	Analog Ground	
3b	AN1	Analog Input 1	
4b	D_CDE	Digital color detection	
5b	D_DOTCLK	LCD Dot Clock	
6b	D_R3	LCD Data Bus Red 3	
7b	D_G1	LCD Data Bus Green 1	
8b	GND	Ground	
9b	D_B4	LCD Data Bus Blue 4	
10b	RESET_LED	Reset Led Control	
11b	AX_RDY#	AX88796 Ready	
12b	GND	Ground	
13b	GND	Ground	
14b	TP_DIN	Touch Panel Data Input	
15b	CAN_RX	CAN Bus RXD	
16b	POW_CS#	Chip Select for Amperometries	
17b	POW_D0	Data Bus 0 for Amperometries	
18b	POW_D5	Data Bus 5 for Amperometries	
19b	POW_D9	Data Bus 9 for Amperometries	

Pin number	Signal name	Function	Note
1c	A_3.3V	Analog 3.3V Power Supply	
2c	A_B	Analog Blue（CRT）	
3c	AN_GND	Analog Ground	
4c	D_CLAMP	Digital CLAMP	
5c	D_DISP	Digital DISP	
6c	D_R2	LCD Data Bus Red 2	
7c	D_G0	LCD Data Bus Green 0	
8c	D_G5	LCD Data Bus Green 5	
9c	D_B3	LCD Data Bus Blue 3	
10c	DASP_LED	CF Sccess LED Control	
11c	AX_IRQ	AX88796 Interrupt	
12c	SCI0_SCK	SCIF0 Clock	
13c	SCI1_SCK	SCIF1 Clock	
14c	TP_CS#	Touch Panel Chip Select	
15c	CAN_TX	CAN Bus Transmit Data	
16c	GND	Ground	
17c	POW_S0	for Amperometries	
18c	POW_D4	Data Bus 4 for Amperometries	
19c	POW_D8	Data Bus 8 for Amperometries	

Pin number	Signal name	Function	Note
1d	AN_GND	Analog Ground	
2d	A_G	Analog Green (CRT)	
3d	AN_GND	Analog Ground	
4d	A_HSYNC	Analog HSYNC	
5d	D_HSYNC	Analog HSYNC	
6d	D_R1	LCD Data Bus Red 1	
7d	GND	Ground	
8d	D_G4	LCD Data Bus Green 4	
9d	D_B2	LCD Data Bus Blue 2	
10d	LCD_VDD_ENB	LCD Power Enable	
11d	AX_CSn	AX88796 Chip Select	
12d	SCI0_RXD	SCIF0 Receive Data	
13d	SCI1_RXD	SCIF1 Receive Data	
14d	TP_CLK	Touch Panel Clock	
15d	TP_IRQn	Touch Panel Interrupt	
16d	GPS_CLK	GPS Clock	
17d	POW_RDn	Read Enable for Amperometries	
18d	POW_D3	Data Bus 3 for Amperometries	
19d	POW_D7	Data Bus 7 for Amperometries	

Pin number	Signal name	Function	Note
1e	AN_GND	Analog Ground	
2e	A_R	Analog Red（CRT）	
3e	AN_GND	Analog Ground	
4e	A_VSYNC	Analog VSYNC	
5e	D_VSYNC	Analog VSYNC	
6e	D_R0	LCD Data Bus Red 0	
7e	D_R5	LCD Data Bus Red 5	
8e	D_G3	LCD Data Bus Green 3	
9e	D_B1	LCD Data Bus Blue 1	
10e	LCD_LIGHT_ENB	LCD Back Light Enable	
11e	AX_RESET	AS88796 Reset	
12e	SCI0_TXD	SCIF0 Transmit Data	
13e	SCI1_TXD	SCIF1 Transmit Data	
14e	GND	Ground	
15e	TP_BUSY	Touch Panel Busy	
16e	GPS_IN	GPS Data	
17e	GND	Ground	
18e	POW_D2	Data Bus 2 for Amperometries	
19e	POW_D6	Data Bus 6 for Amperometries	

2.5. CF Card Connector

CN2 is a connector for CF card interfaces. Timing control is performed in FPGA.

Access equivalent to the True-IDE interface timing based on CFA is possible. It corresponds to PIO mode 0-4.

Please refer to the clause of FPGA functional explanation about the specification of FPGA.

2.6. FROM Board Connector

CN1 is a connector for FROM board interfaces. The general-view figure of a FROM board interface connector is shown in Fig. 2.6.1, and signal arrangement is shown in Table 2.6.1. A use connector is the product 52837-1079 made from Molex.

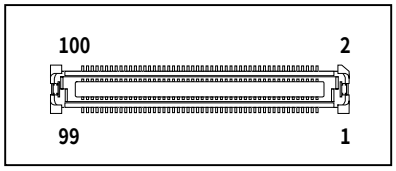


Figure 2.6.1 FROM board interface connector general view

Table 2.6.1 Signal arrangement of FROM board interface connector

Pin number	Signal name	IO	Note
1	5.0V		
2	3.3V		
3	GND		
4	GND		
5	D0	IO	
6	D16	IO	
7	D1	IO	
8	D17	IO	
9	D2	IO	
10	D18	IO	
11	D3	IO	
12	D19	IO	
13	D4	IO	
14	D20	IO	
15	D5	IO	
16	D21	IO	
17	D6	IO	
18	D22	IO	
19	D7	IO	
20	D23	IO	
21	D8	IO	
22	D24	IO	
23	D9	IO	
24	D25	IO	
25	5.0V		
26	3.3V		
27	GND		
28	GND		
29	D10	IO	
30	D26	IO	
31	D11	IO	
32	D27	IO	
33	D12	IO	
34	D28	IO	
35	D13	IO	

Pin number	Signal name	IO	Note
36	D29	IO	
37	D14	IO	
38	D30	IO	
39	D15	IO	
40	D31	IO	
41	A0	O	
42	A13	O	
43	A1	O	
44	A14	O	
45	A2	O	
46	A15	O	
47	A3	O	
48	A16	O	
49	5.0V		
50	3.3V		
51	GND		
52	GND		
53	A4	O	
54	A17	O	
55	A5	O	
56	A18	O	
57	A6	O	
58	A19	O	
59	A7	O	
60	A20	O	
61	A8	O	
62	A21	O	
63	A9	O	
64	A22	O	
65	A10	O	
66	A23	O	
67	A11	O	
68	A24	O	
69	A12	O	
70	A25	O	
71	5.0V		
72	3.3V		
73	GND		
74	GND		
75	WE0#	O	
76	CS0#	O	
77	WE1#	O	
78	NC		
79	WE2#	O	
80	NC		
81	WE3#	O	
82	NC		
83	GND		
84	GND		
85	RD#	O	

Pin number	Signal name	IO	Note
86	NC		
87	RD/WR#	O	
88	NC		
89	NC		10KΩpull-up
90	BS#	O	
91	RESET#	O	
92	NC		10KΩpull-up
93	GND		
94	CKIO	O	
95	5.0V		
96	5.0V		
97	3.3V		
98	3.3V		
99	GND		
100	GND		

2.7. Serial Interface

The SH7780 built-in SCIF is prepared by the connector pattern on this product. The silk of CN11 is printed. Signal arrangement is shown in Table 2.7.1. Please use it of a user if needed.

Table2.7.1 Signal arrangement of CN11

Pin number	Signal name	IO	Note
1	3.3V		
2	TxD1	O	Transmit data
3	RxD1	I	Receive data
4	CTS1	O	Ready for sending
5	RTS1	I	Request to Send
6	SCI_CLK1	IO	Serial clock
7	GND		Ground

2.8. DB Board Interface

CN9 is a connector for DB board interfaces. The general-view figure of DB board interface connector is shown in Fig. 2.8.1, and signal arrangement is shown in Table 2.8.1. It uses 87BFN-50R-3F made from KEL.

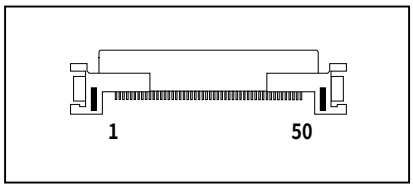


Figure 2.8.1 DB board connector

Table2.8.1 Signal arrangement of DB board connector

Pin number	Signal name	IO	Function
1	3.3V		Power supply
2	3.3V		Power supply
3	DB_PRST#	I	DB board Detect
4	GND		Ground
5	GND		Ground
6	GND		Ground
7	GND		Ground
8	DB_CTS0		Short to DB_RTS0
9	SH_TxD2	O	SH7780_TxD2
10	DB_RTS0		Short to DB_CTS0
11	SH_RxD2	I	SH7780_RxD2
12	GND		Ground
13	GND		Ground
14	SH_PRST#	I	Power on reset
15	JRST#	I	External Reset In
16	MPMD	I	Connect to SH7780'MPMD
17	TMS	O	H-UDI pin
18	ASEBRK#	IO	H-UDI pin
19	TDI	O	H-UDI pin
20	TDO	I	H-UDI pin
21	TCK	I	H-UDI pin
22	TRST#	O	H-UDI pin
23	GND		Ground
24	GND		Ground
25	AUDCK	I	H-UDI pin
26	AUDSYNC#	I	H-UDI pin
27	AUDATA3	I	H-UDI pin
28	AUDATA2	I	H-UDI pin
29	AUDATA1	I	H-UDI pin
30	AUDATA0	I	H-UDI pin
31	GND		Ground
32	GND		Ground
33	PSW2	I	Push switch 2 for debugging
34	PSW1	I	Push switch 1 for debugging
35	PSW0	I	Push switch 0 for debugging

Pin number	Signal name	IO	Function
36	SSW3	I	Dip switch 3 for debugging
37	SSW2	I	Dip switch 2 for debugging
38	SSW1	I	Dip switch 1 for debugging
39	SSW0	I	Dip switch 0 for debugging
40	GND		Ground
41	GND		Ground
42	DCLK	I	JTAG for FPGA
43	nCS	I	JTAG for FPGA
44	nCE	O	JTAG for FPGA
45	ASDO	I	JTAG for FPGA
46	CONFDONE	IO	JTAG for FPGA
47	nCONFIG	O	JTAG for FPGA
48	DATA	O	JTAG for FPGA
49	GND		Ground
50	GND		Ground

2.9. PCI Extension Board Interface

2.9.1. PCI Extension Board Interface A

CN7 is a connector for PCI extension board connection. The general-view figure of a PCI extension interface connector is shown in Fig. 2.91, and signal arrangement is shown in Table 2.9.1 A use connector is the product 52760-1279 made from Molex.

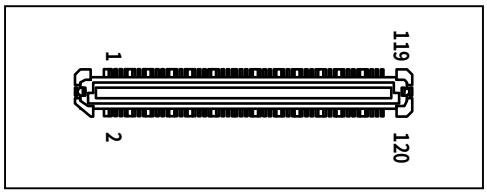


図2.9.1 PCI Extension connector A appearance figure

Table2.9.1 Signal arrangement of PCI extension connector A

Pin number	Signal name	IO	Note
1	GND		Ground
2	GND		Ground
3	PCI_CLK1	O	PCI clock
4	GND		Ground
5	NC		Not use
6	PCI_CLK2	O	PCI clock
7	PCI_CLK3	O	PCI clock
8	NC		Not use
9	GND		Ground
10	PCI_CLK4	O	PCI clock
11	GND		Ground
12	GND		Ground
13	PCI_RST#	O	Reset out
14	PCI_C/BE0#	O	Command/Byte enable 0
15	PCI_C/BE1#	O	Command/Byte enable 1
16	PCI_C/BE2#	O	Command/Byte enable 2
17	PCI_C/BE3#	O	Command/Byte enable 3
18	PCI_PAR	IO	Parity
19	GND		Ground
20	GND		Ground
21	NC		Not use
22	NC		Not use
23	GND		Ground
24	GND		Ground
25	PCI_FRAME#	O	Bus cycle
26	PCI_IRDY#	O	Initiator ready
27	PCI_TRDY#	I	Target ready
28	PCI_STOP#	I	Transaction stop
29	PCI_DEVSEL	I	Device select
30	PCI_LOCK#	O	Lock
31	PCI_PER#	IO	Parity error
32	PCI_SEER#	O	System error
33	GND		Ground
34	GND		Ground
35	PCI_REQ1#	I	Bus request 1

Pin number	Signal name	IO	Note
36	PCI_REQ2#	I	Bus request 2
37	PCI_REQ3#	I	Bus request 3
38	PCI_REQ4#	I	Bus request 4
39	PCI_GNT1#	O	Bus grant 1
40	PCI_GNT2#	O	Bus grant 2
41	PCI_GNT3#	O	Bus grant 3
42	PCI_GNT4#	O	Bus grant 4
43	GND		Ground
44	GND		Ground
45	PCI_AD0	IO	Address/Data 0
46	PCI_AD1	IO	Address/Data 1
47	PCI_AD2	IO	Address/Data 2
48	PCI_AD3	IO	Address/Data 3
49	PCI_AD4	IO	Address/Data 4
50	PCI_AD5	IO	Address/Data 5
51	PCI_AD6	IO	Address/Data 6
52	PCI_AD7	IO	Address/Data 7
53	GND		Ground
54	GND		Ground
55	PCI_AD8	IO	Address/Data 8
56	PCI_AD9	IO	Address/Data 9
57	PCI_AD10	IO	Address/Data 10
58	PCI_AD11	IO	Address/Data 11
59	PCI_AD12	IO	Address/Data 12
60	PCI_AD13	IO	Address/Data 13
61	PCI_AD14	IO	Address/Data 14
62	PCI_AD15	IO	Address/Data 15
63	GND		Ground
64	GND		Ground
65	3.3V		Power supply
66	3.3V		Power supply
67	GND		Ground
68	GND		Ground
69	PCI_AD16	IO	Address/Data 16
70	PCI_AD17	IO	Address/Data 17
71	PCI_AD18	IO	Address/Data 18
72	PCI_AD19	IO	Address/Data 19
73	PCI_AD20	IO	Address/Data 20
74	PCI_AD21	IO	Address/Data 21
75	PCI_AD22	IO	Address/Data 22
76	PCI_AD23	IO	Address/Data 23
77	GND		Ground
78	GND		Ground
79	PCI_AD24	IO	Address/Data 24
80	PCI_AD25	IO	Address/Data 25
81	PCI_AD26	IO	Address/Data 26
82	PCI_AD27	IO	Address/Data 27
83	PCI_AD28	IO	Address/Data 28
84	PCI_AD29	IO	Address/Data 29
85	PCI_AD30	IO	Address/Data 30

Pin number	Signal name	IO	Note
86	PCI_AD31	IO	Address/Data 31
87	GND		Ground
88	GND		Ground
89	IDSEL1	O	PCI_AD16
90	IDSEL2	O	PCI_AD17
91	IDSEL3	O	PCI_AD18
92	IDSEL4	O	PCI_AD19
93	NC		Not use
94	NC		Not use
95	NC		Not use
96	NC		Not use
97	GND		Ground
98	GND		Ground
99	5.0V		Power supply
100	5.0V		Power supply
101	GND		Ground
102	GND		Ground
103	NC		Not use
104	NC		Not use
105	NC		Not use
106	NC		Not use
107	NC		Not use
108	NC		Not use
109	NC		Not use
110	POW_RESET#	O	Power ON reset
111	GND		Ground
112	GND		Ground
113	GND		Ground
114	GND		Ground
115	GND		Ground
116	GND		Ground
117	GND		Ground
118	GND		Ground
119	GND		Ground
120	GND		Ground

2.9.2. PCI Extension Board Interface B

CN8 is a connector for PCI extension board connection. The general-view figure of a PCI extension interface connector is shown in Fig. 2.9.2, and signal arrangement is shown in Table 2.9.2. A use connector is the product 52760-0679 made from Molex.

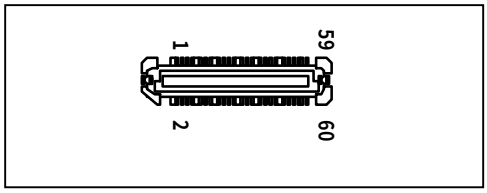


図2.9.2 PCI Extension connector B appearance figure

Table2.9.2 Signal arrangement of PCI extension connector B

Pin number	Signal name	IO	Note
1	GND		Ground
2	GND		Ground
3	PCI_INTA#	I	Interrupt
4	PCI_INTB#	I	Interrupt
5	PCI_INTC#	I	Interrupt
6	PCI_INTD#	I	Interrupt
7	GND		Ground
8	GND		Ground
9	PCI_PRST#	I	PCI Extension board detection
10	PCI_PRST_EXT#	I	PCI Edge card detection
11	GND		Ground
12	GND		Ground
13	TS_CLK		Not use
14	GND		Ground
15	GND		Ground
16	TS_VLDA		Not use
17	TS_SYNC		Not use
18	GND		Ground
19	GND		Ground
20	TS_DATA		Not use
21	TS_IOEN		Not use
22	GND		Ground
23	GND		Ground
24	TS_DIR		Not use
25	TS_ERR		Not use
26	GND		Ground
27	GND		Ground
28	GND		Ground
29	iVDR0	O	iVDR clock control
30	iVDR_POW_ON	O	iVDR power control
31	GND		Ground
32	GND		Ground
33	PW_ID0	I	iVDR PW ID0
34	PW_ID1	I	iVDR PW ID1
35	NC		Not use

Pin number	Signal name	IO	Note
36	NC		Not use
37	IF_ID0	I	iVDR IF ID0
38	IF_ID1	I	iVDR IF ID1
39	IF_ID2	I	iVDR IF ID2
40	IF_ID3	I	iVDR IF ID3
41	GND		Ground
42	GND		Ground
43	NC		Not use
44	NC		Not use
45	NC		Not use
46	NC		Not use
47	NC		Not use
48	NC		Not use
49	NC		Not use
50	NC		Not use
51	NC		Not use
52	NC		Not use
53	NC		Not use
54	NC		Not use
55	NC		Not use
56	NC		Not use
57	NC		Not use
58	NC		Not use
59	GND		Ground
60	GND		Ground

2.10. Reser Signal

2.10.1. Power On Reset

A power-on reset signal is published to each device at the time of a power supply. 3.3V generated from the voltage regulator are made into criteria voltage, and when criteria voltage is less than [2.93V], a reset signal is published from Reset IC.
With this board, since the configuration of FPGA is performed at the time of a power supply, the reset signal over SH7780 is inputted after the configuration end of FPGA. Power-on reset timing is shown in Fig. 2.10.1.

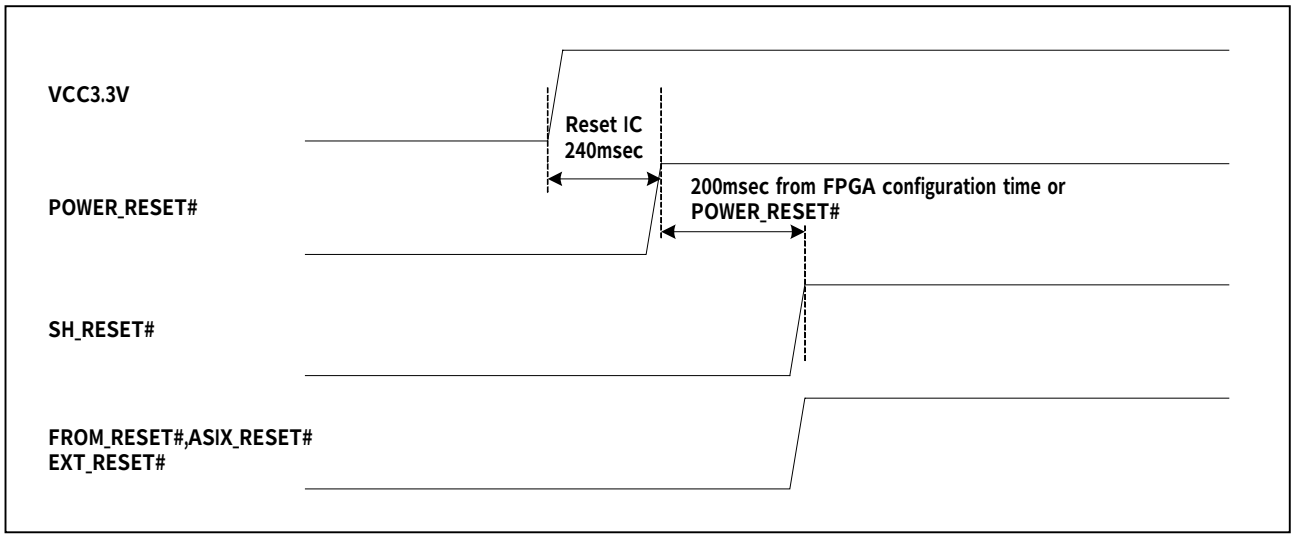


Figure 2.10.1 Power on reset timing

2.10.2. System Reset

This product publishes a system-reset signal under S4 swich-pushing. In a system reset, a reset pulse is published to this timing to each device. System-reset timing is shown in Fig. 2.10.2.

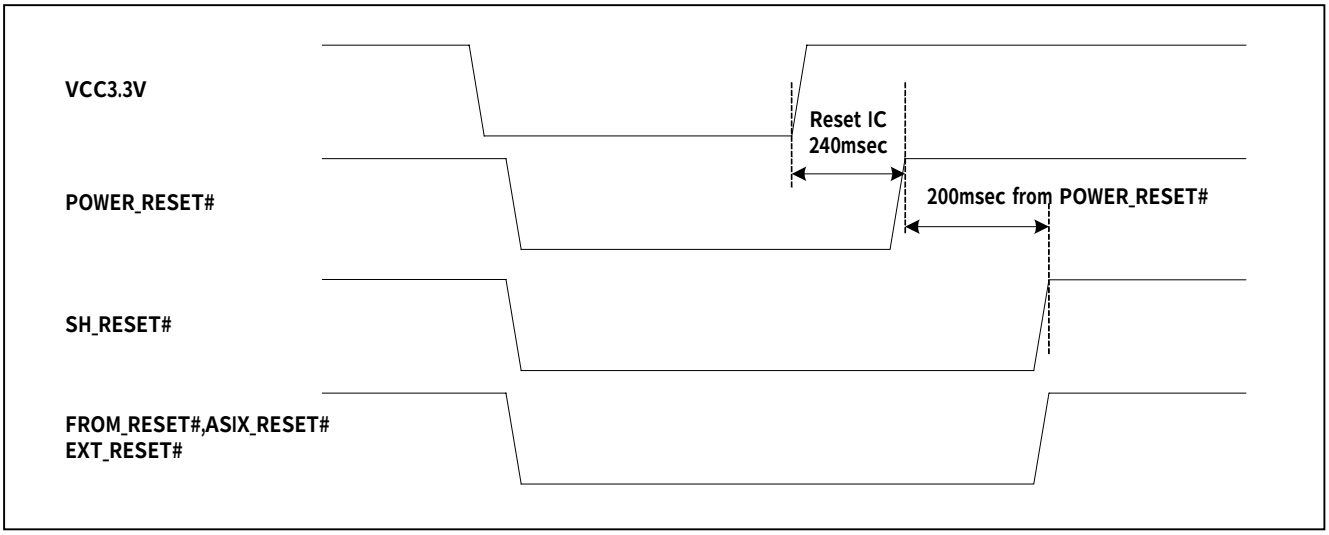


Figure 2.10.2 System reset timing

2.10.3. CF Card Reset

About the reset signal to CF card, after the power supply outputted from the power supply supply control IC(TPS2211) to CF card is stabilized, it is made the specification of which the reset to CF card is canceled. Moreover, in case the power supply from TPS2211 is intercepted, the reset signal to CF card is confirmed. CF card reset timing is shown in Fig. 2.10.3.

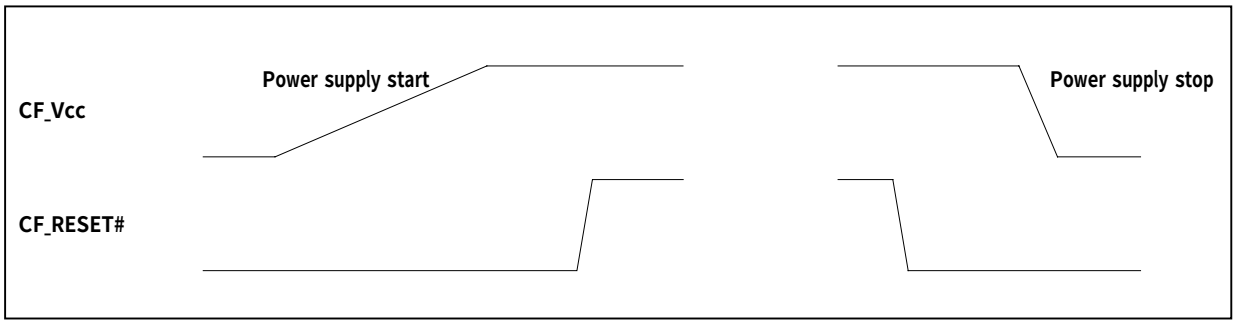


Figure 2.10.3 CF Card reset timing

3. FPGA Logic Function Specification

3.1. Pin Function

This product carries EP1C4F400C8N made from ALTERA. Terminal functional arrangement is shown in Table 3.1.1. The terminal only for JTAG(s) and a power supply related terminal are omitted. Refer to the EP1C4F400C8N data for each terminal function.

Table3.1.1 Terminal functional arrangement of EP1C4F400C8N

Signal Name	FPGA Pin	IO	Function	Active
SH_CS0#	A4	I	SH4A Chip Select 0	L
SH_CS1#	A6	I	SH4A Chip Select 1	L
SH_CS2#	A7	I	SH4A Chip Select 2	L
SH_CS4#	A9	I	SH4A Chip Select 4	L
SH_CS5#	A10	I	SH4A Chip Select 5	L
SH_CS6#	B4	I	SH4A Chip Select 6	L
SH_BS#	B5	I	SH4A Bus Start	L
SH_WE0#	B6	I	SH4A Write Enable 0	L
SH_WE1#	B7	I	SH4A Write Enable 1	L
SH_WE2#	B8	I	SH4A Write Enable 2	L
SH_WE3#	B9	I	SH4A Write Enable 3	L
SH_RD#	B10	I	SH4A Read Enable	L
SH_RDWE#	C2	I	SH4A Read / Write	R:H/W:L
SH_RDY#	C5	O	SH4A Ready	L
SH_CKIO	K5	I	SH4A Clock	—
SH_RESET#	T4	O	SH4A Reset	L
SH_IRL0#	C7	O	SH4A Interrupt 0	L
SH_IRL1#	C8	O	SH4A Interrupt 1	L
SH_IRL2#	C9	O	SH4A Interrupt 2	L
SH_IRL3#	C10	O	SH4A Interrupt 3	L
SH_A[1]	D6	I	SH4A Address 1	—
SH_A[2]	D7	I	SH4A Address 2	—
SH_A[3]	D8	I	SH4A Address 3	—
SH_A[4]	D9	I	SH4A Address 4	—
SH_A[5]	D10	I	SH4A Address 5	—
SH_A[6]	E2	I	SH4A Address 6	—
SH_A[7]	E3	I	SH4A Address 7	—
SH_A[8]	E4	I	SH4A Address 8	—
SH_A[9]	E5	I	SH4A Address 9	—
SH_A[10]	E6	I	SH4A Address 10	—
SH_A[11]	E7	I	SH4A Address 11	—
SH_A[12]	E8	I	SH4A Address 12	—
SH_A[13]	E9	I	SH4A Address 13	—
SH_A[14]	E10	I	SH4A Address 14	—
SH_A[15]	F1	I	SH4A Address 15	—
SH_A[16]	F2	I	SH4A Address 16	—
SH_A[17]	F4	I	SH4A Address 17	—
SH_A[18]	F5	I	SH4A Address 18	—
SH_A[19]	F6	I	SH4A Address 19	—
SH_A[20]	F7	I	SH4A Address 20	—
SH_A[21]	F8	I	SH4A Address 21	—
SH_A[22]	F10	I	SH4A Address 22	—

Signal Name	FPGA Pin	IO	Function	Active
SH_A[23]	G1	I	SH4A Address 23	—
SH_A[24]	G2	I	SH4A Address 24	—
SH_A[25]	G3	I	SH4A Address 25	—
SH_D[0]	G4	I/O	SH4A Data 0	—
SH_D[1]	G5	I/O	SH4A Data 1	—
SH_D[2]	G6	I/O	SH4A Data 2	—
SH_D[3]	G7	I/O	SH4A Data 3	—
SH_D[4]	H1	I/O	SH4A Data 4	—
SH_D[5]	H2	I/O	SH4A Data 5	—
SH_D[6]	H3	I/O	SH4A Data 6	—
SH_D[7]	H4	I/O	SH4A Data 7	—
SH_D[8]	H5	I/O	SH4A Data 8	—
SH_D[9]	H6	I/O	SH4A Data 9	—
SH_D[10]	H7	I/O	SH4A Data 10	—
SH_D[11]	J1	I/O	SH4A Data 11	—
SH_D[12]	J2	I/O	SH4A Data 12	—
SH_D[13]	J3	I/O	SH4A Data 13	—
SH_D[14]	J4	I/O	SH4A Data 14	—
SH_D[15]	J5	I/O	SH4A Data 15	—
SH_D[16]	J6	I/O	SH4A Data 16	—
SH_D[17]	J7	I/O	SH4A Data 17	—
SH_D[18]	J8	I/O	SH4A Data 18	—
SH_D[19]	M1	I/O	SH4A Data 19	—
SH_D[20]	M2	I/O	SH4A Data 20	—
SH_D[21]	M3	I/O	SH4A Data 21	—
SH_D[22]	M4	I/O	SH4A Data 22	—
SH_D[23]	M5	I/O	SH4A Data 23	—
SH_D[24]	M6	I/O	SH4A Data 24	—
SH_D[25]	M7	I/O	SH4A Data 25	—
SH_D[26]	N1	I/O	SH4A Data 26	—
SH_D[27]	N2	I/O	SH4A Data 27	—
SH_D[28]	N3	I/O	SH4A Data 28	—
SH_D[29]	N4	I/O	SH4A Data 29	—
SH_D[30]	N5	I/O	SH4A Data 30	—
SH_D[31]	N6	I/O	SH4A Data 31	—
FROM_CS#	R1	O	FROM Chip Select	L
FROM_RST#	R2	O	FROM Reset	L
CF_VCC5EN#	R4	O	CF 5V Power permission	L
CF_VCC3EN#	R5	O	CF 3.3V Power permission	L
CF_IORD#	R6	O	CF Read Strobe	L
CF_IOWR#	R7	O	CF Write Strobe	L
CF_CE0#	T2	O	CF Chip select 0	L
CF_CE1#	T3	O	CF Chip select 1	L
CF_CDINT1#	T5	I	CF Card detection 1	L
CF_CDINT2#	T7	I	CF Card detection 2	L
CF_INT	T8	I	CF Interrupt	H
CF_RDY#	T9	I	CF Ready	L
CF_RST#	T10	O	CF Reset	L
CF_DET_LED	R9	O	CF Detect LED	H
CF_A[0]	U1	O	CF Address 0	—
CF_A[1]	U2	O	CF Address 1	—
CF_A[2]	U3	O	CF Address 2	—

Signal Name	FPGA Pin	IO	Function	Active
CF_A[3]	U4	O	CF Address 3	—
CF_A[4]	U5	O	CF Address 4	—
CF_A[5]	U6	O	CF Address 5	—
CF_A[6]	U7	O	CF Address 6	—
CF_A[7]	U8	O	CF Address 7	—
CF_A[8]	U9	O	CF Address 8	—
CF_A[9]	U10	O	CF Address 9	—
CF_A[10]	U11	O	CF Address 10	—
CF_D[0]	V2	I/O	CF Data 0	—
CF_D[1]	V3	I/O	CF Data 1	—
CF_D[2]	V4	I/O	CF Data 2	—
CF_D[3]	V5	I/O	CF Data 3	—
CF_D[4]	V6	I/O	CF Data 4	—
CF_D[5]	V7	I/O	CF Data 5	—
CF_D[6]	V8	I/O	CF Data 6	—
CF_D[7]	V9	I/O	CF Data 7	—
CF_D[8]	V10	I/O	CF Data 8	—
CF_D[9]	W3	I/O	CF Data 9	—
CF_D[10]	W4	I/O	CF Data 10	—
CF_D[11]	W5	I/O	CF Data 11	—
CF_D[12]	W6	I/O	CF Data 12	—
CF_D[13]	W7	I/O	CF Data 13	—
CF_D[14]	W8	I/O	CF Data 14	—
CF_D[15]	W9	I/O	CF Data 15	—
PCI_PRSTN#	Y4	I	PCI Extension board present	L
PCI_PRSTN_EXT#	Y10	I	PCI Edge card present	L
FPGA_LED[0]	A11	O	LED control for debugging 0	H
FPGA_LED[1]	A12	O	LED control for debugging 1	H
FPGA_LED[2]	A13	O	LED control for debugging 2	H
FPGA_LED[3]	A14	O	LED control for debugging 3	H
FPGA_LED[4]	A15	O	LED control for debugging 4	H
FPGA_LED[5]	A17	O	LED control for debugging 5	H
FPGA_LED[6]	B11	O	LED control for debugging 6	H
FPGA_LED[7]	B12	O	LED control for debugging 7	H
FPGA_SW[0]	B13	I	Dip switch control for debuggong 0	—
FPGA_SW[1]	B14	I	Dip switch control for debuggong 1	—
FPGA_SW[2]	B15	I	Dip switch control for debuggong 2	—
FPGA_SW[3]	B16	I	Dip switch control for debuggong 3	—
FPGA_SW[4]	B17	I	Dip switch control for debuggong 4	—
FPGA_SW[5]	B18	I	Dip switch control for debuggong 5	—
FPGA_SW[6]	C11	I	Dip switch control for debuggong 6	—
FPGA_SW[7]	C12	I	Dip switch control for debuggong 7	—
POWER_RST#	F3	I	System reset	L
EXT_BUSEN#	E11	O	Bus enable for External connector	L
EXT_RESET#	D20	O	Reset signal for External connector	L
EXT_CS1#	C13	O	Chip select 1 for External connector	L
EXT_CS4#	C14	O	Chip select 4 for External connector	L
EXT_CS5#	C16	O	Chip select 5 for External connector	L
EXT_CS6#	C17	O	Chip select 6 for External connector	L
EXT_WAIT0	C18	I	Wait 0 for External connector	L
EXT_WAIT1	C19	I	Wait 1 for External connector	L
EXT_WAIT2	D11	I	Wait 2 for External connector	L

Signal Name	FPGA Pin	IO	Function	Active
EXT_WAIT4	D12	I	Wait 4 for External connector	L
EXT_WAIT5	D13	I	Wait 5 for External connector	L
EXT_WAIT6	D14	I	Wait 6 for External connector	L
EXT_INT1#	D15	I	Interrupt 1 for External connector	L
EXT_INT2#	D16	I	Interrupt 2 for External connector	L
EXT_INT4#	D17	I	Interrupt 4 for External connector	L
EXT_INT5#	D18	I	Interrupt 5 for External connector	L
EXT_INT6#	D19	I	Interrupt 6 for External connector	L
POW_CS#	E13	O	Chip select for ADC10062	L
POW_RD#	E14	O	Read enable for ADC10062	L
POW_S0	E15	O	ADC10062 select	—
POW_INT#	E16	I	ADC10062 wait	L
POW_D[0]	E17	I	ADC10062 data 0	—
POW_D[1]	E18	I	ADC10062 data 1	—
POW_D[2]	E19	I	ADC10062 data 2	—
POW_D[3]	F14	I	ADC10062 data 3	—
POW_D[4]	F15	I	ADC10062 data 4	—
POW_D[5]	F16	I	ADC10062 data 5	—
POW_D[6]	F17	I	ADC10062 data 6	—
POW_D[7]	F19	I	ADC10062 data 7	—
POW_D[8]	F20	I	ADC10062 data 8	—
POW_D[9]	G14	I	ADC10062 data 9	—
TP_DCLK	R11	O	Clock for ADS7846	—
TP_BUSY	F12	I	ADS7846 busy	H
TP_CS#	H18	O	Chip select for ADS7846	L
TP_DIN	H19	O	ADS7846 data input	—
TP_DOUT	H20	I	ADS7846 data output	—
TP_INT#	M19	I	Interrupt for ADS7846	L
TWS_CLK	V19	I/O	Clock for Two wired serial	—
TWS_DA	W18	I/O	Two wired serial data	—
IVDR_PW_ON	W16	O	iVDR power control	H
PW_ID0	Y11	I	iVDR status	—
PW_ID1	Y12	I	iVDR status	—
IF_ID0	Y13	I	iVDR status	—
IF_ID1	Y14	I	iVDR status	—
IF_ID2	Y15	I	iVDR status	—
IF_ID3	Y17	I	iVDR status	—
IVDR_CK_EN#	W10	O	SATA controller clock enable	L
SCI_CK0	C6	I/O	Serial clock 0	—
SCI_TXD0	N7	O	Serial transmit data 0	—
SCI_RXD0	N20	I	Serial receive data 0	—
SCI_CTS0#	R3	I/O	Ready for sending 0	L
SCI_RTS0#	U18	I/O	Request to Send 0	L
SCI_CK1	V16	I/O	Serial clock 1	—
SCI_TXD1	V12	O	Serial transmit data 1	—
SCI_RXD1	V13	I	Serial receive data 1	—
SCI_CTS1#	V14	I/O	Ready for sending 1	L
SCI_RTS1#	V15	I/O	Request to Send 1	L
AX_RST	H14	O	AX88796 reset (On the R0P0400LP0011RL)	H
AX_RDY	H15	I	AX88796 ready (On the R0P0400LP0011RL)	H
AX_IRQ	H16	I	AX88796 interrupt (On the R0P0400LP0011RL)	H
AX_CS#	H17	O	AX88796 chip select (On the R0P0400LP0011RL)	L

Signal Name	FPGA Pin	IO	Function	Active
DB_PSW0	M20	I	Push switch 0 (On the DB board)	H
DB_PSW1	N14	I	Push switch 1 (On the DB board)	H
DB_PSW2	N15	I	Push switch 2 (On the DB board)	H
DB_DSW0	N16	I	Dip switch 0 (On the DB board)	H
DB_DSW1	N17	I	Dip switch 1 (On the DB board)	H
DB_DSW2	N18	I	Dip switch 2 (On the DB board)	H
DB_DSW3	N19	I	Dip switch 3 (On the DB board)	H
CK1_8M	K6	I	Clock in for serial baudrate (1.8432MHz)	—
BKPRST	P17	O	Back up reset for DDR	—
S_SEL	P18	O	HAC/SSI select	—
CLK32K	L14	I	RTC32KHz clock	—
RTC_INTA#	R13	I	RTC interrupt A	L
RTC_INTB#	R14	I	RTC interrupt B	L
EXT_GPIO[0]	R15	I/O	External GPIO 0	—
EXT_GPIO[1]	R16	I/O	External GPIO 1	—
EXT_GPIO[2]	R17	I/O	External GPIO 2	—
EXT_GPIO[3]	R18	I/O	External GPIO 3	—
EXT_GPIO[4]	R19	I/O	External GPIO 4	—
EXT_GPIO[5]	R20	I/O	External GPIO 5	—
EXT_GPIO[6]	U12	I/O	External GPIO 6	—
EXT_GPIO[7]	U13	I/O	External GPIO 7	—
MDIPSW[0]	P4	I	Dip switch for maintenance 0	—
MDIPSW[1]	P5	I	Dip switch for maintenance 1	—
MDIPSW[2]	P6	I	Dip switch for maintenance 2	—
MDIPSW[3]	P7	I	Dip switch for maintenance 3	—
VCXO_CNT	P15	O	TS clock control	—
TS_CLK	P16	O	TS clock	—
TS_VLDA	P19	O	TS Valid	H
TS_SYNC	P20	O	TS Sync	H
TS_DATA	V11	O	TS data	—
TS_IOEN	V17	I	TS IO enable	H
TS_DIR	W11	I	TS data direction	—
TS_ERR	W12	O	TS error	H
GPIO0	P1	O		
POWER_OFF#	W13	O	Power off control	L
SH_MODESET#	W14	O	SH mode set valid	L
SSI_RST#	L14	O	SSI reset	L
FROM_REV0	K16	I/O	FROM_I/F_Reserve0	—
FROM_REV1	K15	I/O	FROM_I/F_Reserve1	—
FROM_REV2	E12	I/O	FROM_I/F_Reserve2	—
FROM_REV3	G15	I/O	FROM_I/F_Reserve3	—
FROM_REV4	G16	I/O	FROM_I/F_Reserve4	—
FROM_REV5	G17	I/O	FROM_I/F_Reserve5	—
R.S.V11	U15	I/O	Reserve11	—
R.S.V12	T11	I/O	Reserve12	—
R.S.V13	T12	I/O	Reserve13	—
R.S.V14	T13	I/O	Reserve14	—
R.S.V15	T14	I/O	Reserve15	—
R.S.V16	T15	I/O	Reserve16	—
R.S.V17	T16	I/O	Reserve17	—
R.S.V18	T17	I/O	Reserve18	—
R.S.V19	T18	I/O	Reserve19	—

Signal Name	FPGA Pin	IO	Function	Active
R.S.V20	U16	I/O	Reserve20	—
R.S.V21	U17	I/O	Reserve21	—

3.2. Register Map

The FPGA register address map is shown in Table 3.2.1.

Table3.2.1 FPGA Regiater Map

No	Register Name	Abbreviation	Bit	Initial Value	R/W	Address
1	Interrupt mask control register	IRLMSK	16	H'0000	R/W	H'04000000
2	Interrupt status monitor register	IRLMON	16	H'0000	R	H'04000002
3	Interrupt priority control 1 register	IRLPRI1	16	H'4361	R/W	H'04000004
4	Interrupt priority control 2 register	IRLPRI2	16	H'2578	R/W	H'04000006
5	Interrupt priority control 3 register	IRLPRI3	16	H'9ABE	R/W	H'04000008
6	Interrupt priority control 4 register	IRLPRI4	16	H'000D	R/W	H'0400000A
7	Reset control register	RSTCTL	16	H'0000	W	H'0400000C
8	PCI extension board detection control register	PCIBD	16	H'0000	R	H'0400000E
9	PCI expansion slot card detection control register	PCICD	16	H'0000	R	H'04000010
10	External GPIO direction control register	EXTGIO	16	H'00xx	R/W	H'04000016
11	iVDR pins monitor register	IVDRMON	16	H'0000	R/W	H'04000018
12	iVDR control register	IVDRCTL	16	H'0000	R/W	H'0400001A
13	On Board LED control register	OBLED	16	H'0000	R/W	H'0400001C
14	On Board Switch control register	OBSW	16	H'0000	R	H'0400001E
15	Sound Interface Select register	AUDIOSEL	16	H'0000	R/W	H'04000020
16	3.3V Power moniter register	W3VMON	16	H'0xxx	R	H'04000022
17	5.0V Power moniter register	W5VMON	16	H'0xxx	R	H'04000024
18	Touch panel controller access control register	TPCTL	16	H'0000	R/W	H'04000100
19	Touch panel controller access data clock control register	TPTXCLK	16	H'0000	R/W	H'04000102
20	Touch panel controller access reset control register	TPRST	16	H'0000	W	H'04000104
21	Touch panel X position data register	TPXRD	16	H'0000	R	H'04000106
22	Touch panel Y position data register	TPYRD	16	H'0000	R	H'04000108
23	DB board switch control register	DBSW	16	H'000x	R	H'04000200
24	CF card timing control register	CFCTL	16	H'0000	R/W	H'04000300
25	CF card power control register	CFPOW	16	H'0000	R/W	H'04000302
26	CF card detection clear control register	CFCDINTCLR	16	H'0000	W	H'04000304
27	SCIF serial mode register 0	SCSMR0	16	H'0000	R/W	H'04000400
28	SCIF baudrate register 0	SCBRR0	8	H'FF	R/W	H'04000404
29	SCIF serial control register 0	SCSCR0	16	H'0000	R/W	H'04000408
30	SCIF transmit FIFO data register 0	SCFTDR0	8	H'00	W	H'0400040C
31	SCIF serial status register 0	SCFSR0	16	H'0060	R/W	H'04000410
32	SCIF receive FIFO data register 0	SCFRDR0	8	H'00	R	H'04000414
32	SCIF FIFO control register 0	SCFCR0	16	H'0000	R/W	H'04000418
33	SCIF transmit FIFO data count register 0	SCTFDR0	16	H'0000	R	H'0400041C
34	SCIF receive FIFO data count register 0	SCRFDR0	16	H'0000	R	H'04000420
35	SCIF serial port register 0	SCSPTR0	16	H'0000	R/W	H'04000424
36	SCIF line status register 0	SCLSR0	16	H'0000	R/W	H'04000428
37	SCIF serial error register 0	SCRER0	16	H'0000	R	H'0400042C
38	SCIF serial mode register 1	SCSMR1	16	H'0000	R/W	H'04000500
39	SCIF baudrate register 1	SCBRR1	8	H'FF	R/W	H'04000504
40	SCIF rerial control register 1	SCSCR1	16	H'0000	R/W	H'04000508
41	SCIF transmit FIFO data register 1	SCFTD1	8	H'00	W	H'0400050C
42	SCIF serial status register 1	SCFSR1	16	H'0060	R/W	H'04000510
43	SCIF receive FIFO data register 1	SCFRDR1	8	H'00	R	H'04000514
44	SCIF FIFO control register 1	SCFCR1	16	H'0000	R/W	H'04000518

No	Register Name	Abbreviation	Bit	Initial Value	R/W	Address
45	SCIF transmit FIFO data count register 1	SCTFDR1	16	H'0000	R	H'0400051C
46	SCIF receive FIFO data count register 1	SCRFDR1	16	H'0000	R	H'04000520
47	SCIF serial port register 1	SCSPTR1	16	H'0000	R/W	H'04000524
48	SCIF line status register 1	SCLSR1	16	H'0000	R/W	H'04000528
49	SCIF serial error register 1	SCRER1	16	H'0000	R	H'0400052C
50	Two wired serial control register	ICCR	16	H'0000	R/W	H'04000600
51	Two wired serial slave address register	SAR	16	H'0000	R/W	H'04000602
52	Two wired serial mode control register	MDR	16	H'0000	R/W	H'04000604
53	Two wired serial address control register 1	ADR1	16	H'0000	R/W	H'04000606
:	:	:	:	:	:	:
84	Two wired serial address control register 32	ADR32	16	H'0000	R/W	H'04000644
85	Two wired serial data control register 1	DAR1	16	H'0000	R/W	H'04000646
:	:	:	:	:	:	:
100	Two wired serial data control register 16	DAR16	16	H'0000	R/W	H'04000664
101	Version management register	VERREG	16	H'2020	R/W	H'04000700
102	Power OFF Control Register	POFF	16	H'0000	W	H'04000800
103	Maintenance Dip switch control register	PMR	16	H'000x	R	H'04000900

3.3. FPGA Register Specification

3.3.1. Interrupt mask control register (IRLMSK)

This register controls the SH7780 interrupt mask.

■Interrupt mask control register (IRLMSK) <Address: H'0400_0000>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCI0_ INT_ MSK	SCI1_ INT_ MSK	RTC_ INT_ MSK	-	CF_ INT_ MSK	-	TP_ INT_ MSK	TWS_ INT_ MSK	-	EXT_ INT6_ MSK	EXT_ INT5_ MSK	EXT_ INT4_ MSK	EXT_ INT2_ MSK	EXT_ INT1_ MSK	DBPSW _INT_ MSK	AX_ IRQ_ MSK
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

b	Bit Name	Function	R	W
15	SCI0_INT_MSK SH7780 SCIF0 Interrupt MASK bit	0:SH7780 SCIF0 Interrupt MASK 1:SH7780 SCIF0 Interruput enabled	R	W
14	SCI1_INT_MSK SH7780 SCIF1 Interrupt MASK bit	0:SH7780 SCIF1 Interrupt MASK 1:SH7780 SCIF1 Interruput enabled	R	W
13	RTC_INT_MSK RTC Interrupt MASK bit	0:RTC Interrupt MASK 1:RTC Interruput enabled	R	W
12	Reserved		0	-
11	CF_INT_MSK CF Interrupt MASK bit	0:CF Interrupt MASK 1:CF Interruput enabled	R	W
10	Reserved		0	-
9	TP_INT_MSK Touch panel controller Interrupt MASK bit	0:Touch panel controller Interrupt MASK 1:Touch panel controller Interruput enabled	R	W
8	TWS_INT_MSK Two wired serial Interrupt MASK bit	0:Two wired serial Interrupt MASK 1:Two wired serial Interrupt enabled	R	W
7	Reserved		0	-
6	EXT_INT6_MSK External Area 6 Interrupt MASK bit	0: External Area 6 Interrupt MASK 1: External Area 6 Interruput enabled	R	W
5	EXT_INT5_MSK External Area 5 Interrupt MASK bit	0: External Area 5 Interrupt MASK 1: External Area 5 Interruput enabled	R	W
4	EXT_INT4_MSK External Area 4 Interrupt MASK bit	0: External Area 4 Interrupt MASK 1: External Area 4 Interruput enabled	R	W
3	EXT_INT2_MSK External Area 2 Interrupt MASK bit	0: External Area 2 Interrupt MASK 1: External Area 2 Interruput enabled	R	W
2	EXT_INT1_MSK External Area 1 Interrupt MASK bit	0: External Area 1 Interrupt MASK 1: External Area 1 Interruput enabled	R	W
1	DBPSW_INT_MSK Push switch on the DB board Interrupt MASK bit	0:Push switch Interrupt MASK 1:Push switch Interruput enabled	R	W
0	AX_IRQ_MSK AX88796 on the R0P0400LP0011RL Interrupt MASK bit	0:AX88796 Interrupt MASK 1:AX88796 Interruput enabled	R	W

3.3.2. Interrupt status monitor register (IRLMON)

This register indicates interrupts from peripheral devices.

■Interrupt status monitor register (IRLMON) <Address: H'0400_0002>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCI0_ INT_ MON	SCI1_ INT_ MON	RTC_ INTA_ MON	RTC_ INTB_ MON -	CF_ INT_ MON	CF_ CDINT _MON	TP_ INT_ MON	TWS_ INT_ MON	-	EXT_ INT6_ MON	EXT_ INT5_ MON	EXT_ INT4_ MON	EXT_ INT2_ MON	EXT_ INT1_ MON	DBPSW _INT_ MON	AX_ IRQ_ MON
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

b	Bit Name	Function	R	W
15	SCI0_INT_MON SH7780 SCIF0 Interrupt Moniter bit	0:No Interrupt 1:With INterrupt	R	-
14	SCI1_INT_MON SH7780 SCIF1 Interrupt Moniter bit	0:No Interrupt 1:With Interrupt	R	-
13	RTC_INTA_MON RTC Timer/Alarm Interrupt Moniter bit	0:No Interrupt 1:With Interrupt	R	-
12	RTC_INTB_MON RTC Alarm Interrupt Moniter bit	0:No Interrupt 1:With Interrupt	R	-
11	CF_INT_MON CF Interrupt Moniter bit	0:No Interrupt 1:With Interrupt	R	-
10	CF_CDINT_MON CF card insert Interrupt Moniter bit	0:No Interrupt 1:With Interrupt	R	-
9	TP_INT_MON Touch panel controller Interrupt Moniter bit	0:No Interrupt 1:With Interrupt	R	-
8	TWS_INT_MON Two wired serial Interrupt Moniter bit	0:No Interrupt 1:With Interrupt	R	-
7	Reserved		0	-
6	EXT_INT6_MON External Area 6 Interrupt Moniter bit	0:No Interrupt 1:With Interrupt	R	-
5	EXT_INT5_MON External Area 5 Interrupt Moniter bit	0:No Interrupt 1:With Interrupt	R	-
4	EXT_INT4_MON External Area 4 Interrupt Moniter bit	0:No Interrupt 1:With Interrupt	R	-
3	EXT_INT2_MON External Area 2 Interrupt Moniter bit	0:No Interrupt 1:With Interrupt	R	-
2	EXT_INT1_MON External Area 1 Interrupt Moniter bit	0:No Interrupt 1:With Interrupt	R	-
1	DBPSW_INT_MON Push switch on the DB board Interrupt Moniter bit	0:No Interrupt 1:With Interrupt	R	-
0	AX_IRQ_MON AX88796 on the R0P0400LP0011RL Interrupt Moniter bit	0:No Interrupt 1:With INterrupt	R	-

3.3.3. Interrupt priority control

This register sets up the priority of the various interruption to SH7780. The set point is determined by a setup 4 bits each, H'0 - H'E. Interruption is not generated when it is set as H'F. (Perfect masked state) H'0 is the highest and H'E of priority is the lowest.

3.3.3.1. Interrupt priority control 1 register (IRLPRI1)

This register sets up the priority of SCI, RTC, and CF interruption.

■Interrupt priority control 1 register (IRLPRI1) <Address: H'0400_0004>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCI0_ INT_ PRI3	SCI0_ INT_ PRI2	SCI0_ INT_ PRI1	SCI0_ INT_ PRI0	SCI1_ INT_ PRI3	SCI1_ INT_ PRI2	SCI1_ INT_ PRI1	SCI1_ INT_ PRI0	RTC_ INT_ PRI3	RTC_ INT_ PRI2	RTC_ INT_ PRI1	RTC_ INT_ PRI0	CF_ INT_ PRI3	CF_ INT_ PRI2	CF_ INT_ PRI1	CF_ INT_ PRI0
0	1	0	0	0	0	1	1	0	1	1	0	0	0	0	1

b	Bit Name	Function	R	W
15～12	SCI0_INT_PRI3-0 SCI0 Interruption priority setting bit 3-0	A setup of the priority of the SCIF0 interruption（Default H'4）	R	W
11～8	SCI1_INT_PRI3-0 SCI1 Interruption priority setting bit 3-0	A setup of the priority of the SCIF1 interruption（Default H'3）	R	W
7～4	RTC_INT_PRI3-0 RTC Interruption priority setting bit 3-0	A setup of the priority of the RTC interruption（Default H'6）	R	W
3～0	CF_INT_PRI3-0 CF Interruption priority setting bit 3-0	A setup of the priority of the CF interruption（Default H'1）	R	W

3.3.3.2. Interrupt priority control 2 register (IRLPRI2)

This register sets up the priority of touch panel, tow wired serial, external area 6 and external area 5 interruption.

■Interrupt priority control 2 register (IRLPRI2) <Address:H'0400_0006>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TP_ INT_ PRI3	TP_ INT_ PRI2	TP_ INT_ PRI1	TP_ INT_ PRI0	TWS_ INT_ PRI3	TWS_ INT_ PRI2	TWS_ INT_ PRI1	TWS_ INT_ PRI0	EXT6_ INT_ PRI3	EXT6_ INT_ PRI2	EXT6_ INT_ PRI1	EXT6_ INT_ PRI0	EXT5_ INT_ PRI3	EXT5_ INT_ PRI2	EXT5_ INT_ PRI1	EXT5_ INT_ PRI0
0	0	1	0	0	1	0	1	0	1	1	1	1	0	0	0

b	Bit Name	Function	R	W
15～12	TP_INT_PRI3-0 Touch panel controller Interruption priority setting bit 3-0	A setup of the priority of the touch panel controller interruption（Default H'2）	R	W
11～8	TWS_INT_PRI3-0 Two wired serial Interruption priority setting bit 3-0	A setup of the priority of the two wired serial interruption（Default H'5）	R	W
7～4	EXT6_INT_PRI3-0 External Area 6 Interruption priority setting bit 3-0	A setup of the priority of the external area 6 interruption（Default H'7）	R	W
3～0	EXT5_INT_PRI3-0 External Area 5 Interruption priority setting bit 3-0	A setup of the priority of the external area 5 interruption（Default H'8）	R	W

3.3.3.3. Interrupt priority control 3 register (IRLPRI3)

This register sets up the priority of external area 4, external area 2, external area 1 and push switch on the DB board interruption.

■Interrupt priority control 3 register (IRLPRI3) <Address:H'0400_0008>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXT4_INT_PRI3	EXT4_INT_PRI2	EXT4_INT_PRI2	EXT4_INT_PRI0	EXT2_INT_PRI3	EXT2_INT_PRI2	EXT2_INT_PRI1	EXT2_INT_PRI0	EXT1_INT_PRI3	EXT1_INT_PRI2	EXT1_INT_PRI1	EXT1_INT_PRI0	DBPSW_INT_PRI3	DBPSW_INT_PRI2	DBPSW_INT_PRI1	DBPSW_INT_PRI0
1	0	0	1	1	0	1	0	1	0	1	1	1	1	1	0

b	Bit Name	Function	R	W
15～12	EXT4_INT_PRI3-0 External Area 4 Interruption priority setting bit 3-0	A setup of the priority of the external area 4 interruption（Default H'9）	R	W
11～8	EXT2_INT_PRI3-0 External Area 2 Interruption priority setting bit 3-0	A setup of the priority of the external area 2 interruption（Default H'A）	R	W
7～4	EXT1_INT_PRI3-0 External Area 1 Interruption priority setting bit 3-0	A setup of the priority of the external area 1 interruption（Default H'B）	R	W
3～0	DBPSW_INT_PRI3-0 Push switch on the DB board Interruption priority setting bit 3-0	A setup of the priority of the push switch on the DB board interruption（Default H'E）	R	W

3.3.3.4. Interrupt priority control 4 register (IRLPRI4)

This register sets up the priority of AX88796 on the R0P0400LP0011RL interruption.

■Interrupt priority control 4 register (IRLPRI4) <Address:H'0400_000A>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	AX_IRQ_PRI3	AX_IRQ_PRI2	AX_IRQ_PRI1	AX_IRQ_PRI0
0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1

b	Bit Name	Function	R	W
15～4	Reserved		0	-
3～0	AX_IRQ_PRI3-0 AX88796 on the R0P0400LP0011RL Interruption priority setting bit 3-0	A setup of the priority of the AX88796 on the R0P0400LP0011RLinterruption（Default H'D）	R	W

3.3.3.5. Interrupt Priority at Default

The interruption priority at the time of power on is shown in Table 3.3.4.

Table3.3.4 Interruption priority at the time of power on

No.	Interruption	Priority level		Note
1	-	15	Highest	
2	CF card	14	↑	"H"Level
3	Touch panel	13		"L" Level
4	SCIF1	12		"L" Level
5	SCIF0	11		"L" Level
6	Two wired serial	10		"H" Level
7	RTC	9		"L" Level
8	External Area 6	8		"L" Level
9	External Area 5	7		"L" Level
10	External Area 4	6		"L" Level
11	External Area 2	5		"L" Level
12	External Area 1	4		"L" Level
13	-	3		
14	AX88796	2	↓	"H" Level
15	Push switch (On the DB board)	1	Lowest	"L"Edge

3.3.4. Reset control register (RSTCTL)

This register controls reset for peripheral devices.

■Reset control register (RSTCTL) <Address:H'0400_000C>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	CF_RST	-	-	-	-	-	-	EXT_RST	-	FROM_RST	-	AX_RST
0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1

b	Bit Name	Function	R	W
15～12	Reserved		0	-
11	CF_RST CF reset control bit	0:Invalid 1:Reset out (10usec pulse width)	0	W
10～5	Reserved		0	-
4	EXT_RST External Area reset control bit	0:Invalid 1:Reset out (10usec pulse width)	0	W
3	Reserved		0	-
2	FROM_RST FROM board reset control bit	0:Invalid 1:Reset out (10usec pulse width)	0	W
1	Reserved		0	-
0	AX_RST AX88796 reset control bit	0:Invalid 1:Reset out (10usec pulse width)	0	W

3.3.5. PCI expansion slot card detection control register (PCICD)

This register detects the PCI edge card connecting to the PCI extension board.

■P CI expansion slot card detection control register (PCICD) <Address:H'0400_000E>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	PCI_PRST
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

b	Bit Name	Function	R	W
15～1	Reserved		0	-
0	PCI_PRST PCI card insertion detection bit	0:PCI card un-inserting 1:PCI card insertion	R	-

3.3.6. PCI extension board detection control register (PCIBD)

This register detects the PCI extension board connecting to the CN7 and CN8.

■P CI extension board detection control register (PCIBD) <Address:H'0400_00010>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	PCI_PRST_EXT
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

b	Bit Name	Function	R	W
15～1	Reserved		0	-
0	PCI_PRST_EXT PCI extension board insertion detection bit	0: Not connected 1: PCI extension board connected	R	-

3.3.7. External GPIO direction control register (EXTGIO)

This register controls external GPIO into the FPGA.

■External GPIO direction control register (EXTGIO) <Address:H'0400_00016>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXT_ DIR7	EXT_ DIR6	EXT_ DIR5	EXT_ DIR4	EXT_ DIR3	EXT_ DIR2	EXT_ DIR1	EXT_ DIR0	EXT_ DATA 7	EXT_ DATA 6	EXT_ DATA 5	EXT_ DATA 4	EXT_ DATA 3	EXT_ DATA 2	EXT_ DATA 1	EXT_ DATA 0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

b	Bit Name	Function	R	W
15	EXT_DIR7 EXT_GPIO 7 IO mode setting bit	0:Input mode 1:Output mode	R	W
14	EXT_DIR6 EXT_GPIO 6 IO mode setting bit	0:Input mode 1:Output mode	R	W
13	EXT_DIR5 EXT_GPIO 5 IO mode setting bit	0:Input mode 1:Output mode	R	W
12	EXT_DIR4 EXT_GPIO 4 IO mode setting bit	0:Input mode 1:Output mode	R	W
11	EXT_DIR3 EXT_GPIO 3 IO mode setting bit	0:Input mode 1:Output mode	R	W
10	EXT_DIR2 EXT_GPIO 2 IO mode setting bit	0:Input mode 1:Output mode	R	W
9	EXT_DIR1 EXT_GPIO 1 IO mode setting bit	0:Input mode 1:Output mode	R	W
8	EXT_DIR0 EXT_GPIO 0 IO mode setting bit	0:Input mode 1:Output mode	R	W
7	EXT_DATA7 EXT_GPIO 7 control bit	An input/output changes by setup of this register of b15. Output:0: "L"output from FPGA_GPIO7 1: "H"output from FPGA_GPIO7 Input : Status of FPGA_GPIO7	R	W
6	EXT_DATA6 EXT_GPIO 6 control bit	An input/output changes by setup of this register of b14. Output:0: "L"output from FPGA_GPIO6 1: "H"output from FPGA_GPIO6 Input : Status of FPGA_GPIO6	R	W
5	EXT_DATA5 EXT_GPIO 5 control bit	An input/output changes by setup of this register of b13. Output:0: "L"output from FPGA_GPIO5 1: "H"output from FPGA_GPIO5 Input : Status of FPGA_GPIO5	R	W
4	EXT_DATA4 EXT_GPIO 4 control bit	An input/output changes by setup of this register of b12. Output:0: "L"output from FPGA_GPIO4 1: "H"output from FPGA_GPIO4 Input : Status of FPGA_GPIO4	R	W
3	EXT_DATA3 EXT_GPIO 3 control bit	An input/output changes by setup of this register of b11. Output:0: "L"output from FPGA_GPIO3 1: "H"output from FPGA_GPIO3 Input : Status of FPGA_GPIO3	R	W

2	EXT_DATA2 EXT_GPIO 2 control bit	An input/output changes by setup of this register of b10. Output:0: "L"output from FPGA_GPIO2 1: "H"output from FPGA_GPIO2 Input : Status of FPGA_GPIO2	R	W
1	EXT_DATA1 EXT_GPIO 1 control bit	An input/output changes by setup of this register of b9. Output:0: "L"output from FPGA_GPIO1 1: "H"output from FPGA_GPIO1 Input : Status of FPGA_GPIO1	R	W
0	EXT_DATA0 EXT_GPIO 0 control bit	An input/output changes by setup of this register of b8. Output:0: "L"output from FPGA_GPIO0 1: "H"output from FPGA_GPIO0 Input : Status of FPGA_GPIO0	R	W

3.3.8. iVDR pins monitor register (IVDRMON)

This register detects iVDR pins on the connecting PCI extension board.

■iVDR pins monitor register (IVDRMON) <Address:H'0400_00018>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	PW_ ID1	PW_ ID0	IF_ ID3	IF_ ID2	IF_ ID1	IF_ ID0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

b	Bit Name	Function	R	W
15～6	Reserved		0	-
5,4	PW_ID1,0 iVDR Power IDmoniter bit 1,0	The combination of PW ID is the following PW_ID1 / PW_ID0 / : 1 / 0 / Operate by 5V and 3.3V 1 / 1 / Operate by 5V Other values are reservation	R	-
3～0	IF_ID3-0 iVDR IF ID moniter bit 3-0	The combination of IF ID is the following IF_ID3 / IF_ID2 / IF_ID1 / IF_ID0 / : 1 / 1 / 1 / 0 / Port A only Device 0 / 0 / 0 / 1 / Port B only Device 1 / 0 / 0 / 1 0 / 1 / 0 / 1 1 / 1 / 0 / 1 1 / 1 / 1 / 1 / No Device Other values are reservation	R	-

3.3.9. iVDR control register (IVDRCTL)

This register controls clock and power supply for the iVDR controller on the PCI extension board.

■iVDR control register (IVDRCTL) <Address:H'0400_0001A>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	IVDR_CK_ON	-	-	-	-	-	-	-	IVDR_PW_ON
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

b	Bit Name	Function	R	W
15～9	Reserved		0	-
8	IVDR_CK_ON Clock supply control to the iVDR controller	0:No clock supply 1:With clock supply	R	W
7～1	Reserved		0	-
0	IVDR_PW_ON Power supply control to the iVDR	0:No power supply 1:With power supply	R	W

3.3.10. On Board LED control register (OBLED)

This register controls LEDs connected to FPGA.

■On Board LED control register (OBLED) <Address:H'0400_0001C>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	OB LED_7	OB LED_6	OB LED_5	OB LED_4	OB LED_3	OB LED_2	OB LED_1	OB LED_0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

b	Bit Name	Function	R	W
15～8	Reserved		0	-
7	OB_LED7 LED7 lighting control bit	0:OFF 1:ON	0	W
6	OB_LED6 LED6 lighting control bit	0:OFF 1:ON	0	W
5	OB_LED5 LED5 lighting control bit	0:OFF 1:ON	0	W
4	OB_LED4 LED4 lighting control bit	0:OFF 1:ON	0	W
3	OB_LED3 LED3 lighting control bit	0:OFF 1:ON	0	W
2	OB_LED2 LED2 lighting control bit	0:OFF 1:ON	0	W
1	OB_LED1 LED1 lighting control bit	0:OFF 1:ON	0	W
0	OB_LED0 LED0 lighting control bit	0:OFF 1:ON	0	W

3.3.11. On Board Switch control register (OBSW)

This register stores the state of the switch connected to FPGA.

■On Board Switch control register (OBSW) <Address:H'0400_001E>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	OB SW_7	OB SW_6	OB SW_5	OB SW_4	OB SW_3	OB SW_2	OB SW_1	OB SW_0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

b	Bit Name	Function	R	W
15～8	Reserved		0	-
7	OBSW_7 Dip switch (S3) bit 8 status bit	0:OFF 1:ON	0/1	
6	OBSW_6 Dip switch (S3) bit 7 status bit	0:OFF 1:ON	0/1	
5	OBSW_5 Dip switch (S3) bit 6 status bit	0:OFF 1:ON	0/1	
4	OBSW_4 Dip switch (S3) bit 5 status bit	0:OFF 1:ON	0/1	
3	OBSW_3 Dip switch (S3) bit 4 status bit	0:OFF 1:ON	0/1	
2	OBSW_2 Dip switch (S3) bit 3 status bit	0:OFF 1:ON	0/1	
1	OBSW_1 Dip switch (S3) bit 2 status bit	0:OFF 1:ON	0/1	
0	OBSW_0 Dip switch (S3) bit 1 status bit	0:OFF 1:ON	0/1	

3.3.12. Sound Interface Select register (AUDIOSEL)

This register chooses SSI or HAC, when connecting the sound interface of SH7780 to an external extension connector.

■Sound Interface Select register (AUDIOSEL) <Address:H'0400_0020>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	S_SEL
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

b	Bit Name	Function	R	W
15～1	Reserved		0	-
0	S_SEL Sound interface select bit	0:HAC 1:SSI	R	W

3.3.13. 3.3V Power moniter register (W3VMON)

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	W3V MON_ 9	W3V MON_ 8	W3V MON_ 7	W3V MON_ 6	W3V MON_ 5	W3V MON_ 4	W3V MON_ 3	W3V MON_ 2	W3V MON_ 1	W3V MON_ 0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

b	Bit Name	Function	R	W
15～10	Reserved		0	-
9～0			R	

3.3.14. 5.0V Power moniter register (W5VMON)

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	W5V MON_ 9	W5V MON_ 8	W5V MON_ 7	W5V MON_ 6	W5V MON_ 5	W5V MON_ 4	W5V MON_ 3	W5V MON_ 2	W5V MON_ 1	W5V MON_ 0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

b	Bit Name	Function	R	W
15～10	Reserved		0	-
9～0			R	

3.3.15. Touch panel controller access control register (TPCTL)

This register chooses effective/invalid of a touch panel controller.

■Touch panel controller access control register(TPCTL) <Address:H'0400_0100>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	TEN
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

b	Bit Name	Function	R	W
15～1	Reserved		0	-
0	TEN Touch panel controller access enable bit	0:touch panel controller desable 1:touch panel controller enable	R	W

3.3.16. Touch panel controller access data clock control register (TPTXCLK)

This register sets up the base clock inputted into a touch panel controller.

■Touch panel controller access data clock control register (TPTXCLK) <Address:H'0400_0102>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	TC3	TC2	TC1	TC0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

b	Bit Name	Function	R	W
15～4	Reserved		0	-
3	TC3 Base clock for touch panel controller setting bit 3	Base clock set up	R	W
2	TC2 Base clock for touch panel controller setting bit 2		R	W
1	TC1 Base clock for touch panel controller setting bit 1		R	W
0	TC0 Base clock for touch panel controller setting bit 0		R	W

b3	b2	b1	b0	Base clock
TC3	TC2	TC1	TC0	
0	0	0	0	60KHz
0	0	0	1	65KHz
0	0	1	0	70KHz
0	0	1	1	75KHz
0	1	0	0	80KHz
0	1	0	1	85KHz
0	1	1	0	90KHz
0	1	1	1	95KHz
1	0	0	0	100KHz
1	0	0	1	105KHz
1	0	1	0	110KHz

Setup other than the above is set to about 60kHz.

3.3.17. Touch panel controller access reset control register (TPRST)

This register resets touch-panel controller.

■Touch panel controller access reset control register (TPRST) <Address:H'0400_0104>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	TPRST
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

b	Bit Name	Function	R	W
15～1	Reserved		0	-
0	TPRST Touch panel control block reset bit	0:Invalid 1:Reset	0	W

3.3.18. Touch panel X position data register (TPXRD)

This register stores X position data from a touch panel controller. It is automatically cleared after read out.

■Touch panel X position data register (TPXRD) <Address:H'0400_0106>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	XD11	XD10	XD9	XD8	XD7	XD6	XD5	XD4	XD3	XD2	XD1	XD0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

b	Bit Name	Function	R	W
15～12	Reserved		0	-
11	XD11 X position data 11	X position data from a touch panel controller are stored. It is automatically cleared after read out.	R	-
10	XD10 X position data 10		R	-
9	XD9 X position data 9		R	-
8	XD8 X position data 8		R	-
7	XD7 X position data 7		R	-
6	XD6 X position data 6		R	-
5	XD5 X position data 5		R	-
4	XD4 X position data 4		R	-
3	XD3 X position data 3		R	-
2	XD2 X position data 2		R	-
1	XD1 X position data 1		R	-
0	XD0 X position data 0		R	-

3.3.19. Touch panel Y position data register(TPYRD)

This register stores Y position data from a touch panel controller. It is automatically cleared after read out.

■Touch panel Y position data register (TPYRD) <Address:H'0400_0108>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	YD11	YD10	YD9	YD8	YD7	YD6	YD5	YD4	YD3	YD2	YD1	YD0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

b	Bit Name	Function	R	W
15～12	Reserved		0	-
11	YD11 Y position data 11	Y position data from a touch panel controller are stored. It is automatically cleared after read out.	R	-
10	YD10 Y position data 10		R	-
9	YD9 Y position data 9		R	-
8	YD8 Y position data 8		R	-
7	YD7 Y position data 7		R	-
6	YD6 Y position data 6		R	-
5	YD5 Y position data 5		R	-
4	YD4 Y position data 4		R	-
3	YD3 Y position data 3		R	-
2	YD2 Y position data 2		R	-
1	YD1 Y position data 1		R	-
0	YD0 Y position data 0		R	-

3.3.20. DB board switch control register (DBSW)

This register controls the interrupt detection and status moniter on the DB board.

■DB board switch control register (DBSW) <Address:H'0400_0200>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	DB_ PSW_2 CLR	DB_ PSW_1 CLR	DB_ PSW_0 CLR	-	-	-	-	-	DBSW _6	DBSW _5	DBSW _4	DBSW _3	DBSW _2	DBSW _1	DBSW _0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

b	Bit Name	Function	R	W
15	Reserved		0	-
14	DB_PSW_2CLR Interruption clear bit to push switch 1 on the DB board	1:Clear 0:Invalid		W
13	DB_PSW_1CLR Interruption clear bit to push switch 2 on the DB board	1:Clear 0:Invalid		W
12	DB_PSW_0CLR Interruption clear bit to push switch 3 on the DB board	1:Clear 0:Invalid		W
11～7	Reserved		0	-
6	DBSW_6 Push switch 1 status moniter bit	0:OFF 1:ON	R	
5	DBSW_5 Push switch 2 status moniter bit	0:OFF 1:ON	R	
4	DBSW_4 Push switch 3 status moniter bit	0:OFF 1:ON	R	
3	DBSW_3 Dip switch 4 bit 1 (on the DB board) status moniter bit	0:OFF 1:ON	R	
2	DBSW_2 Dip switch 4 bit 2 (on the DB board) status moniter bit	0:OFF 1:ON	R	
1	DBSW_1 Dip switch 4 bit 3 (on the DB board) status moniter bit	0:OFF 1:ON	R	
0	DBSW_0 Dip switch 4 bit 4 (on the DB board) status moniter bit	0:OFF 1:ON	R	

3.3.21. CF card timing control register (CFCTL)

This register controls CF card access timing. An access setup from SH7780 is in SRAM mode.

■CF card timing control register (CFCTL) <Address:H'0400_0300>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	TCLK1	TCLK0	-	TED2	TED1	TED0	-	THE2	THE1	THE0	-	-	PCW1	PCW0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

b	Bit Name	Function	R	W
15,14	Reserved		0	-
13	TCLK1 Timing clock divide setting bit 1	Timing clock Divide b13 TCLK1 / b12 TCLK0 / clock 0 0 Φ 0 1 Φ/2 1 0 Φ/4 1 1 Φ/8	R	W
12	TCLK0 Timing clock divide setting bit 0		R	W
11	Reserved		0	-
10	TED2 Address to IORD#/IOWR# assertion delay time selection bit 2	Address to IORD#/IOWR# assertion delay time selection b10 TED2 / b9 TED1 / b8 TED0 / Wait cycle 0 0 0 1 0 0 1 2 0 1 0 3 0 1 1 6 1 0 0 9 1 0 1 12 1 1 0 15 1 1 1 Prohibition	R	W
9	TED1 Address to IORD#/IOWR# assertion delay time selection bit 1		R	W
8	TED0 Address to IORD#/IOWR# assertion delay time selection bit 0		R	W
7	Reserved		0	-
6	THE2 IORD#/IOWR# negation to address delay time selection bit 2	IORD#/IOWR# negation to address delay time selection b6 THE2 / b5 THE1 / b4 THE0 / Wait cycle 0 0 0 1 0 0 1 2 0 1 0 3 0 1 1 6 1 0 0 9 1 0 1 12 1 1 0 15 1 1 1 Prohibition	R	W
5	THE1 IORD#/IOWR# negation to address delay time selection bit 1		R	W
4	THE0 IORD#/IOWR# negation to address delay time selection bit 0		R	W
3,2	Reserved		0	-
1	PCW1 PCMCIA wait cycle selection bit 1	PCMCIA wait cycle selection b1 PCW1 / b0 PCW0 / Wait cycle 0 0 1 0 1 15 1 0 20 1 1 30	R	W
0	PCW0 PCMCIA wait cycle selection bit 0		R	W

3.3.22. CF card power control register (CFPOW)

This register determines the supply voltage supplied to CF card.

■CF card power control register (CFPOW) <Address:H'0400_0302>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	VCC5 EN	VCC3 EN
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

b	Bit Name	Function	R	W
15～2	Reserved		0	-
1	VCC5EN Power supply 5V control bit	CF card power supply valtage	R	W
0	VCC3EN Power supply 3.3V control bit		R	W

b1 VCC5EN	b0 VCC3EN	Power supply
0	0	0V
0	1	3.3V
1	0	5.0V
1	1	Prohibition

3.3.23. CF card detection clear control register (CFCDINTCLR)

This register clears insertion detection interruption of CF card.

■CF card detection clear control register (CFCDINTCLR) <Address:H'0400_0304>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CF CLR
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

b	Bit Name	Function	R	W
15～1	Reserved		0	-
0	CFCLR CF	0:Invalid 1:CFCDINT Clear		W

3.3.24. SCIF serial mode register 0,1(SCSMR0,1)

This register carries out mode control of the SCIF block built in FPGA. This SCIF operates only by the asynchronous mode.

■SCIF serial mode register 0 (SCSMR0) <Address:H'0400_0400>

■SCIF serial mode register 1 (SCSMR1) <Address:H'0400_0500>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	CHR	PE	O_En	STOP	-	CKS1	CKS0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

b	Bit Name	Function	R	W
15～7	Reserved		0	-
6	CHR Data length	0:8 bit 1:7 bit	R	W
5	PE Parity bit control bit	0:none 1:valid	R	W
4	O_En Parity bit	0:even 1:odd	R	W
3	STOP Stop bit	0:1bit 1:2bit	R	W
2	Reserved		0	-
1	CKS1 Clock divide setting bit 1	Clock dividion	R	W
0	CKS0 Clock divide setting bit 0		R	W

Clock dividion

b1	b0	clock
CKS1	CKS0	
0	0	Φ
0	1	Φ/4
1	0	Φ/16
1	1	Φ/64

3.3.25. SCIF baudrate register 0,1(SCBRR0,1)

This register controls the transceiver bit rate of the SCIF block with built in FPGA.

■SCIF baudrate register 0(SCBRR0) <Address:H'0400_0404>

■SCIF baudrate register 1(SCBRR1) <Address:H'0400_0504>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	N7	N6	N5	N4	N3	N2	N1	N0
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

b	Bit Name	Function	R	W
15～8	Reserved		0	-
7	N7 baud rate set bit 7	Refer The SCBRR setting is found from the following equation	R	W
6	N6 baud rate set bit 6		R	W
5	N5 baud rate set bit 5		R	W
4	N4 baud rate set bit 4		R	W
3	N3 baud rate set bit 3		R	W
2	N2 baud rate set bit 2		R	W
1	N1 baud rate set bit 1		R	W
0	N0 baud rate set bit 0		R	W

The SCBRR setting is found from the following equation.

$$N = \frac{Pck}{64 \times 2^{2n-1} \times B} \times 10^6 - 1$$

B : Bit rate (bits/s)

N : SCBRR setting for baud rate generator (0 < N <255)

Pck : operating frequency (MHz)

n : Baud rate generator input clock (n = 0 to 3)

(The relation between n and a clock should look at the following table.)

n	clock	SCSMR setting	
		CKS1	CKS0
0	Pck	0	0
1	Pck/4	0	1
2	Pck/16	1	0
3	Pck/64	1	1

The bit rate error in asynchronous mode is found from the following equation:

$$\text{Error (\%)} = \left\{ \frac{Pck \times 10^6}{(N+1) \times B \times 64 \times 2^{2n-1}} - 1 \right\} \times 100$$

3.3.26. SCIF serial control register 0, 1(SCSCR0, 1)

This register carries out transceiver control of the SCIF block with built in FPGA.

■SCIF serial control register 0(SCSCR0) <Address:H'0400_0408>

■SCIF serial control register 1(SCSCR1) <Address:H'0400_0508>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	TIE	RIE	TE	RE	REIE	-	CKE1	CKE0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

b	Bit Name	Function	R	W
15～8	Reserved		0	-
7	TIE Transmission FIFO data empty interrupt enable bit	0: Interrupt disabled 1: Interruput enabled	R	W
6	RIE Receive (Data (RXI),Error (ERI),Break (BRI)) interrupt enable bit	0: Interrupt disabled 1: Interruput enabled	R	W
5	TE Transmission Enable bit	0: Disabled 1: Enabled	R	W
4	RE Receive Enable bit	0: Disabled 1: Enabled	R	W
3	REIE Receive Error Interrupt Enable *(RIE bit (b6) = effective in the case of 0)	0: Interrupt disabled 1: Interruput enabled	R	W
2	Reserved		0	-
1	CKE1 Base clock select bit 1	Base clock selection b1 (CKE1) / b0 (CKE0) / SCK pin function 0 / 0 / Input port 0 / 1 / Clock out 1 / 0 / 1.8432MHz 1 / 1 / External input clock	R	W
0	CKE0 Base clock select bit 0		R	W

3.3.27. SCIF transmit FIFO data register 0,1 (SCFTDR0,1)

This register stores the transmit data of the SCIF block with built in FPGA.

■SCIF transmit FIFO data register 0(SCFTDR0) <Address:H'0400_040C>

■SCIF transmit FIFO data register 1(SCFTDR1) <Address:H'0400_050C>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	TD7	TD6	TD5	TD4	TD3	TD2	TD1	TD0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

b	Bit Name	Function	R	W
15～8	Reserved		0	-
7	TD7 Transmission data bit 7	Transmission data	0	-
6	TD6 Transmission data bit 6		-	W
5	TD5 Transmission data bit 5		-	W
4	TD4 Transmission data bit 4		-	W
3	TD3 Transmission data bit 3		-	W
2	TD2 Transmission data bit 2		-	W
1	TD1 Transmission data bit 1		-	W
0	TD0 Transmission data bit 0		-	W

3.3.28. SCIF serial status register 0,1(SCFSR0,1)

This register carries out the monitor of the status of the serial block with built in FPGA. Only "0" lights of (W) are effective.

■SCIF serial status register 0(SCFSR0) <Address:H'0400_0410>

■SCIF serial status register 1(SCFSR1) <Address:H'0400_0510>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	ER	TEND	TDFE	BRK	FER	PER	RDF	DR
0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0

b	Bit Name	Function	R	W
15～8	Reserved		0	-
7	ER Receive Error bit	0:No erroe 1:Parity or framing error existence	R	(W)
6	TEND Transmission end bit	0:Under transmission 1:Transmission end	R	(W)
5	TDFE Transmit FIFO Data Empty bit	0: A number of transmit data bytes exceeding the transmit trigger set number have been written to SCFTDR 1: The number of transmit data bytes in SCFTDR does not exceed the transmit trigger set number (Initial value)	R	(W)
4	BRK Break Detect bit	0: A break signal has not been received 1: A break signal has been received	R	(W)
3	FER Framing Error detect bit	0:No framing error 1:Framing error existemnce	R	-
2	PER Pariry Error detect bit	0:No parity error 1:Parity error existence	R	-
1	RDF Receive FIFO Data Full	0: The number of receive data bytes in SCFRDR is less than the receive trigger set number 1: The number of receive data bytes in SCFRDR is equal to or greater than the receive trigger set number	R	(W)
0	DR Receive Data Ready bit	0: Reception is in progress or has ended normally and there is no receive data left in SCFRDR 1: No further receive data has arrived [Setting condition] • When SCFRDR contains fewer than the receive trigger set number of receive data bytes, and no further data has arrived for at least 15 etu after the stop bit of the last data received	R	(W)

3.3.29. SCIF receive FIFO data count register 0,1(SCFRDR0,1)

This register stores the received data of the SCIF block with built in FPGA.

■SCIF receive FIFO data count register 0(SCFRDR0) <Address:H'0400_0414>

■SCIF receive FIFO data count register 1(SCFRDR1) <Address:H'0400_0514>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

b	Bit Name	Function	R	W
15～8	Reserved		0	-
7	RD7 Receive data bit 7	Receive data	R	-
6	RD6 Receive data bit 6		R	-
5	RD5 Receive data bit 5		R	-
4	RD4 Receive data bit 4		R	-
3	RD3 Receive data bit 3		R	-
2	RD2 Receive data bit 2		R	-
1	RD1 Receive data bit 1		R	-
0	RD0 Receive data bit 0		R	-

3.3.30. SCIF FIFO control register 0,1(SCFCR0,1)

This register performs FIFO control of the serial block with built in FPGA.

■SCIF FIFO control register 0(SCFC0) <Address:H'0400_0418>

■SCIF FIFO control register 1(SCFC1) <Address:H'0400_0518>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	RS TRG2	RS TRG1	RS TRG0	R TRG1	R TRG0	T TRG1	T TRG0	MCE	TFRST	RFRST	LOOP
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

b	Bit Name	Function	R	W
15	Reserved		0	-
10	RSTRG2 RTS output trigger bit 2	The SCIF_RTS signal becomes high when the number of receive data stored in SCFRDR exceeds the trigger number shown below.	R	W
9	RSTRG1 RTS output trigger bit 1		R	W
8	RSTRG0 RTS output trigger bit 0		R	W
7	RTRG1 Receive FIFO data count trigger bit 1	These bits are used to set the number of receive data bytes that sets the RDF flag in SCFSR.	R	W
6	RTRG0 Receive FIFO data count trigger bit 0		R	W
5	TTRG1 Transmit FIFO data count trigger bit 1	These bits are used to set the number of remaining transmit data bytes that sets the TDFE flag in SCFSR.	R	W
4	TTRG0 Transmit FIFO data count trigger bit 0		R	W
3	MCE MODEM control enable bit	Enables the SCIF_CTS and SCIF_RTS modem control signals. 0: Modem signals disabled 1: Modem signals enabled	R	W
2	TFRST Transmit FIFO data register reset bit	0: Reset operation disabled 1: Reset operation enabled	R	W
1	RFRST Receive FIFO data register reset bit	0: Reset operation disabled 1: Reset operation enabled	R	W

b10	b9	b8	RTS output trigger
RSTRG2	RSTRG1	RSTRG0	
0	0	0	15
0	0	1	1
0	1	0	4
0	1	1	6
1	0	0	8
1	0	1	10
1	1	0	12
1	1	1	14

b7	b6	The number of receive triggers
RTRG1	RTRG0	
0	0	1
0	1	4
1	0	8
1	1	14

b5	b4	The number of transmit triggers
TTRG1	TTRG0	
0	0	8
0	1	4
1	0	2
1	1	1

b	Bit Name	Function	R	W
0	LOOP Loop back bit	Loopback Test Internally connects the transmit output pin (TXD) and receive input pin (RXD), and the RTS pin and CTS pin, enabling loopback testing. 0: Loopback test disabled 1: Loopback test enabled	R	W

3.3.31. SCIF transmit FIFO data count register 0,1(SCTFDR0,1)

SCTFDR is a register that indicates the number of transmit data bytes stored in SCTFDRn.

■SCIF transmit FIFO data count register 0(SCTFDR0) <Address:H'0400_041C>

■SCIF transmit FIFO data count register 1(SCTFDR1) <Address:H'0400_051C>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	T6	T5	T4	T3	T2	T1	T0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

b	Bit Name	Function	R	W
15～7	Reserved		0	-
6	T6 Transmit FIFO data count bit 6	These bits show the number of untransmitted data bytes in SCTFDR. A value of H'00 indicates that there is no transmit data, and a value of H'40 indicates that SCTFDR is full of transmit data.	R	-
5	T5 Transmit FIFO data count bit 5		R	-
4	T4 Transmit FIFO data count bit 4		R	-
3	T3 Transmit FIFO data count bit 3		R	-
2	T2 Transmit FIFO data count bit 2		R	-
1	T1 Transmit FIFO data count bit 1		R	-
0	T0 Transmit FIFO data count bit 0		R	-

3.3.32. SCIF receive FIFO data count register 0,1(SCRFDR0,1)

SCRFDR is a register that indicates the number of receive data bytes stored in SCRFDRn.

■SCIF receive FIFO data count register 0(SCRFDR0) <Address:H'0400_0420>

■SCIF receive FIFO data count register 1(SCRFDR1) <Address:H'0400_0520>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	R6	R5	R4	R3	R2	R1	R0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

b	Bit Name	Function	R	W
15～7	Reserved		0	-
6	R6 Receive FIFO data count bit 6	These bits show the number of receive data bytes in SCRFDR. A value of H'00 indicates that there is no receive data, and a value of H'40 indicates that SCRFDR is full of receive data.	R	-
5	R5 Receive FIFO data count bit 5		R	-
4	R4 Receive FIFO data count bit 4		R	-
3	R3 Receive FIFO data count bit 3		R	-
2	R2 Receive FIFO data count bit 2		R	-
1	R1 Receive FIFO data count bit 1		R	-
0	R0 Receive FIFO data count bit 0		R	-

3.3.33. SCIF serial port register 0,1(SCSPTR0,1)

SCSPTR is a readable/writable register that controls input/output and data for the port pins multiplexed with the serial communication interface (SCIF) pins at all times. Input data can be read from the RXD pin, output data written to the TXD pin, and breaks in serial transmission/reception controlled, by means of bits 1 and 0.

- The RTS and CTS pin becomes effective when the MCE bit of SCFCR is "0".
- The SCK pin becomes effective when the CKE1 and CKE0 bit of SCSCR are "00".
- The TxD pin becomes effective when the TE bit of SCSCR is "0".

■SCIF serial port register 0(SCSPTR0) <Address:H'0400_0420>

■SCIF serial port register 1(SCSPTR1) <Address:H'0400_0520>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	RTSIO	RTSDT	CTSIO	CTSDT	SCKIO	SCKDT	SPB2IO	SPB2DT
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

b	Bit Name	Function	R	W
15～8	Reserved		0	-
7	RTSIO Serial Port RTS Port Input/Output	0: RTSDT bit value is not output to RTS pin 1: RTSDT bit value is output to RTS pin	R	W
6	RTSDT Serial Port RTS Port Data	0: Input/output data is low-level 1: Input/output data is high-level	R	W
5	CTSIO Serial Port CTS Port Input/Output	0: CTSDT bit value is not output to CTS pin 1: CTSDT bit value is output to CTS pin	R	W
4	CTSDT Serial Port CTS Port Data	0: Input/output data is low-level 1: Input/output data is high-level	R	W
3	SCKIO Serial Port Clock Port Input/Output	0: SCKDT bit value is not output to SCK pin 1: SCKDT bit value is output to SCK pin	R	W
2	SCKDT Serial Port Clock Port Data	0: Input/output data is low-level 1: Input/output data is high-level	R	W
1	SPB2IO Serial Port Break Input/Output	0: SPB2DT bit value is not output to the TXD pin 1: SPB2DT bit value is output to the TXD pin	R	W
0	SPB2DT Serial Port Break Data	0: Input/output data is low-level 1: Input/output data is high-level	R	W

3.3.34. SCIF line status register 0,1(SCLSR0,1)

This register shows that the overrun error occurred and terminated abnormally at the time of reception.Only "0" lights of (W) are effective.

■SCIF line status register 0(SCLSR0) <Address:H'0400_0428>

■SCIF line status register 1(SCLSR1) <Address:H'0400_0528>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	ORER
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

b	Bit Name	Function	R	W
15～1	Reserved		0	-
0	ORER Overrun error detection bit	0: Reception in progress, or reception has ended normally 1: An overrun error occurred during reception	R	(W)

3.3.35. SCIF serial error register 0,1(SCRER0,1)

■SCIF serial error register 0(SCRER0) <Address:H'0400_042C>

■SCIF serial error register 1(SCRER1) <Address:H'0400_052C>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	PER_5	PER_4	PER_3	PER_2	PER_1	PER_0	-	-	FER_5	FER_4	FER_3	FER_2	FER_1	FER_0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

b	Bit Name	Function	R	W
15,14	Reserved		0	-
13～8	PER5-0 Number of Parity Errors bits 5-0	These bits indicate the number of data bytes in which a parity error occurred in the receive data stored in SCFRDR. After the ER bit in SCFSR is set, the value indicated by bits PER5 to PER0 is the number of data bytes in which a parity error occurred. If all 64 bytes of receive data in SCFRDR have parity errors, the value indicated by bits PER5 to PER0 will be 0.	R	-
7,6	Reserved		0	-
5～0	FER5-0 Number of framnig error bits 5-0	These bits indicate the number of data bytes in which a framing error occurred in the receive data stored in SCFRDR. After the ER bit in SCFSR is set, the value indicated by bits FER5 to FER0 is the number of data bytes in which a framing error occurred. If all 64 bytes of receive data in SCFRDR have framing errors, the value indicated by bits FER5 to FER0 will be 0.	R	-

3.3.36. Two wired serial control register(ICCR)

This register performs the two wired serial interruption, start, and status control.

■Two wired serial control register(ICCR) <Address:H'0400_0600>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	IEIC	-	RST	ACKE	BBSY	IRIC	START
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

b	Bit Name	Function	R	W
15～7	Reserved		0	-
6	IEIC Interrupt control bit	0: Interrupt Desable 1: Interruput enabled	R	W
5	Reserved		0	-
4	RST Module reset bit	0:Invalid 1:Reset	-	W
3	ACK Operation status (ACK judgment) bit	0:Normal 1:Abnormal	R	-
2	BBSY Bus busy detection bit	0:Not Busy 1:Busy	R	-
1	IRIC Module operation status bit	0:Active 1:Finish	R	
0	START Module operation control bit	0:Invalid 1:Start	R	W

3.3.37. Two wired serial slave address (SAR)

This register sets up the slave address of the target device connected the two wired serial, and sets up transmission/reception.

■Two wired serial slave address (SAR) <Address:H'0400_0602>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	SA6	SA5	SA4	SA3	SA2	SA1	SA0	R_W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

b	Bit Name	Function	R	W
15～6	Reserved		0	-
7	SA6 Slave address setting bit 6	Slave address setting	R	W
6	SA5 Slave address setting bit 5		R	W
5	SA4 Slave address setting bit 4		R	W
4	SA3 Slave address setting bit 3		R	W
3	SA2 Slave address setting bit 2		R	W
2	SA1 Slave address setting bit 1		R	W
1	SA0 Slave address setting bit 0		R	W
0	R_W Transmit/receive mode setting bit	0:Transmit 1:Receive	R	W

3.3.38. Two wired serial mode control register(MDR)

This register controls a two wired serial transmission rate and a transmission byte count.

■Two wired serial mode control register(MDR) <Address:H'0400_0604>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	SP	-	-	TM MD	CAP	-	MODE 1	MODE 0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

b	Bit Name	Function	R	W
15～8	Reserved		0	-
7	SP Transmission baud rate setting bit	0:100KHz 1:400KHz	R	W
6,5	Reserved		0	-
4	TMMD Transmission Mode setting bit	0:FPGA custam mode (The mode which specifies all the addresses and publishes stop-condition for every frame when carrying out continuation access.) 1:original mode (At the time of continuation access by which stop-condition is not published for every frame, a target is automatic, and when there is a function which carries out an internal address increment, it is effective.)	R	W
3	CAP Connection device capacity setting bit (It is effective when a connection device is memory.)	0: Less than 32K bytes 1:32K bytes or more	R	W
2	Reserved		0	-
1	MODE1 Number of transmission data bytes setting bit 1		R	W
0	MODE0 Number of transmission data bytes setting bit 0		R	W

MODE1	MODE0	Number of transmission data bytes
0	0	1 byte
0	1	8 bytes
1	0	16 bytes
1	1	32 bytes

3.3.39. Two wired serial address control register 1～32(ADR1～ADR32)

This register controls a setup of the internal address of the target device connected two wired serial.

■Two wired serial address control register 1～32(ADR1～ADR32) <Address:H'0400_0606～H'0400_0644>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADn7	ADn6	ADn5	ADn4	ADn3	ADn2	ADn1	ADn0	ADn+1 7	ADn+1 6	ADn+1 5	ADn+1 4	ADn+1 3	ADn+1 2	ADn+1 1	ADn+1 0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

b	Bit Name	Function	R	W
15	ADn7 Transmission address [n] setting bit 7	The transmission address [n] is set up.	R	W
14	ADn6 Transmission address [n] setting bit 6		R	W
13	ADn5 Transmission address [n] setting bit 5		R	W
12	ADn4 Transmission address [n] setting bit 4		R	W
11	ADn3 Transmission address [n] setting bit 3		R	W
10	ADn2 Transmission address [n] setting bit 2		R	W
9	ADn1 Transmission address [n] setting bit 1		R	W
8	ADn0 Transmission address [n] setting bit 0		R	W
7	ADn+1 7 Transmission address [n+1] setting bit 7	The transmission address [n+1] is set up.	R	W
6	ADn+1 6 Transmission address [n+1] setting bit 6		R	W
5	ADn+1 5 Transmission address [n+1] setting bit 5		R	W
4	ADn+1 4 Transmission address [n+1] setting bit 4		R	W
3	ADn+1 3 Transmission address [n+1] setting bit 3		R	W
2	ADn+1 2 Transmission address [n+1] setting bit 2		R	W
1	ADn+1 1 Transmission address [n+1] setting bit 1		R	W
0	ADn+1 0 Transmission address [n+1] setting bit 0		R	W

*The number of n is odd. It is from 1 to 63.

3.3.40. Two wired serial data control register 1～16(DAR1～DAR16)

This register stores a transmit data setup to the target device connected two wired serial, or received data.

■Two wired serial data control register 1～16(DAR1～DAR16) <Address:H'0400_0646～H'0400_0664>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAn7	DAn6	DAn5	DAn4	DAn3	DAn2	DAn1	DAn0	DAn+1 7	DAn+1 6	DAn+1 5	DAn+1 4	DAn+1 3	DAn+1 2	DAn+1 1	DAn+1 0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

b	Bit Name	Function	R	W
15	DAn7 Transmission data [n] bit 7	Setup of transmit data [n], or receiveddata [n]	R	W
14	DAn6 Transmission data [n] bit 6		R	W
13	DAn5 Transmission data [n] bit 5		R	W
12	DAn4 Transmission data [n] bit 4		R	W
11	DAn3 Transmission data [n] bit 3		R	W
10	DAn2 Transmission data [n] bit 2		R	W
9	DAn1 Transmission data [n] bit 1		R	W
8	DAn0 Transmission data [n] bit 0		R	W
7	DAn+1 7 Transmission data [n+1] bit 7	Setup of transmit data [n+1], or receiveddata [n+1]	R	W
6	DAn+1 6 Transmission data [n+1] bit 6		R	W
5	DAn+1 5 Transmission data [n+1] bit 5		R	W
4	DAn+1 4 Transmission data [n+1] bit 4		R	W
3	DAn+1 3 Transmission data [n+1] bit 3		R	W
2	DAn+1 2 Transmission data [n+1] bit 2		R	W
1	DAn+1 1 Transmission data [n+1] bit 1		R	W
0	DAn+1 0 Transmission data [n+1] bit 0		R	W

*The number of n is odd. It is from 1 to 31.

3.3.41. Two wired serial control module operation note

3.3.41.1. Transmit operation

Please set up a register before executing a start condition issue command.

Operation of a transmitting procedure is shown below.

（1）MDR-SP bit、MDR-CAP bit、MDR-MODE1-MODE0 bits、ICCR-IEIC bit set up operation mode.

（2）The value of ADRn and DARn is set up according to the value set up by (1).

The setting list is shown below.

Table 3.3.41.1 List of MDR set up data

MDR(CAP bit)	MDR(MODE1-0 bits)	ADR and DAR
0	00	ADR1: Bit15-8, DAR1: Bit15-8
0	01	ADR1-4, DAR1-4
0	10	ADR1-8, DAR1-8
0	11	ADR1-16, DAR1-16
1	00	ADR1: Bit15-0, DAR1: Bit15-8
1	01	ADR1-8, DAR1-4
1	10	ADR1-16, DAR1-8
1	11	ADR1-32, DAR1-16

（3）0-6 bits of SAs of SAR are set up according to the target device, and the R_W bit of SAR is set as '0'.

（4）The BBSY bit of ICCR is read and it checks that a bus is in a free state.

（5）'1' is written in the START bit of ICCR and transmitting operation is started.

（6）If IRIC is "1", transmission is end. When IRIC = "0" and BBSY = "1" are under operation.

If IRIC = "0" and ACKE = "1" are error status, please reset Two wired serial module. (Writing to 1 ICCR's RST bit)

3.3.41.2. Receive operation

（1）MDR-SP bit、MDR-CAP bit、MDR-MODE1-MODE0 bits、ICCR-IEIC bit set up operation mode.

（2）The value of ADRn and DARn is set up according to the value set up by (1).

（3）0-6 bits of SAs of SAR are set up according to the target device, and the R_W bit of SAR is set as '1'.

（4）The BBSY bit of ICCR is read and it checks that a bus is in a free state.

（5）'1' is written in the START bit of ICCR and receiving operation is started.

（6）If IRIC is "1", receiving is end. When IRIC = "0" and BBSY = "1" are under operation.

If IRIC = "0" and ACKE = "1" are error status, please reset Two wired serial module. (Writing to 1 ICCR's RST bit)

3.3.42. Version management register (VERREG)

This register controls the Version management.

■Version management register (VERREG) <Address:H'0400_0700>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BVER 3	BVER 2	BVER 1	BVER 0	BREV 3	BREV 2	BREV 1	BREV 0	FVER 3	FVER 2	FVER 1	FVER 0	FREV 3	FREV 2	FREV 1	FREV 0
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1

b	Bit Name	Function	R	W
15	BVER3 Board Version management bit 3	Board Version	0	-
14	BVER2 Board Version management bit 2		0	-
13	BVER1 Board Version management bit 1		1	-
12	BVER0 Board Version management bit 0		0	-
11	BREV3 Board Revision management bit 3	Board Revision	0	-
10	BREV2 Board Revision management bit 2		0	-
9	BREV1 Board Revision management bit 1		0	-
8	BREV0 Board Revision management bit 0		0	-
7	FVER3 FPGA Version management bit 3	FPGA Version	0	-
6	FVER2 FPGA Version management bit 2		0	-
5	FVER1 FPGA Version management bit 1		1	-
4	FVER0 FPGA Version management bit 0		0	-
3	FREV3 FPGA Revision management bit 3	FPGA Revision	0	-
2	FREV2 FPGA Revision management bit 2		0	-
1	FREV1 FPGA Revision management bit 1		0	-
0	FREV0 FPGA Revision management bit 0		0	-

3.3.43. Power OFF Control Register (POWOFF)

This register turns off R0P0400LP0011RL.

■Power OFF Control Register (POWOFF) <Address:H'0400_0800>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	POW_OFF
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

b	Bit Name	Function	R	W
15～1	Reserved		0	-
0	POW_OFF Borad power OFF control bit	0:Invalid 1:Power OFF (Turns off R0P0400LP0011RL)	0	W

3.3.44. Maintenance Dip switch control register (PMR)

This register stores the state of the Dip switch for maintenance. Initial value is unfixed in order to be dependent on the state of the Dip switch at the time of a power ON.

■Maintenance Dip switch control register (PMR) <Address:H'0400_0900>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	MD SW3	MD SW2	MD SW1	MD SW0
0	0	0	0	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1

b	Bit Name	Function	R	W
15～3	Reserved		0	-
3	DIPSW3 Dip switch bit 4 status	S5 bit 4 status 0:OFF 1:ON	0/1	-
2	DIPSW2 Dip switch bit 3 status	S5 bit 3 status 0:OFF 1:ON	0/1	-
1	DIPSW1 Dip switch bit 2 status	S5 bit 2 status 0:OFF 1:ON	0/1	-
0	DIPSW0 Dip switch bit 1 status	S5 bit 1 status 0:OFF 1:ON	0/1	-

4. Extension Board Specification

4.1. About Extension Board Size

4.1.1. R0P0400LP0011RL Add-in Board

Please observe the following matters, in case the add-in board for these products is created of a user.

An add-in board size figure is shown in Fig. 3.1.1, and a terminal accommodation figure is shown in Fig. 3.1.2.

■Board size is 117.85mm x 133mm fixation. Moreover, the board both ends each 10mm x 133mm is pattern prohibition and the ban on part mounting.

■A part side and a solder side set height restrictions of mounting parts to a maximum of 15mm.

Connector A, B: PCN21A-125SB-2PF-G (HIROSE)

Connector C: PCN21A-95SB-2PF-G(HIROSE)

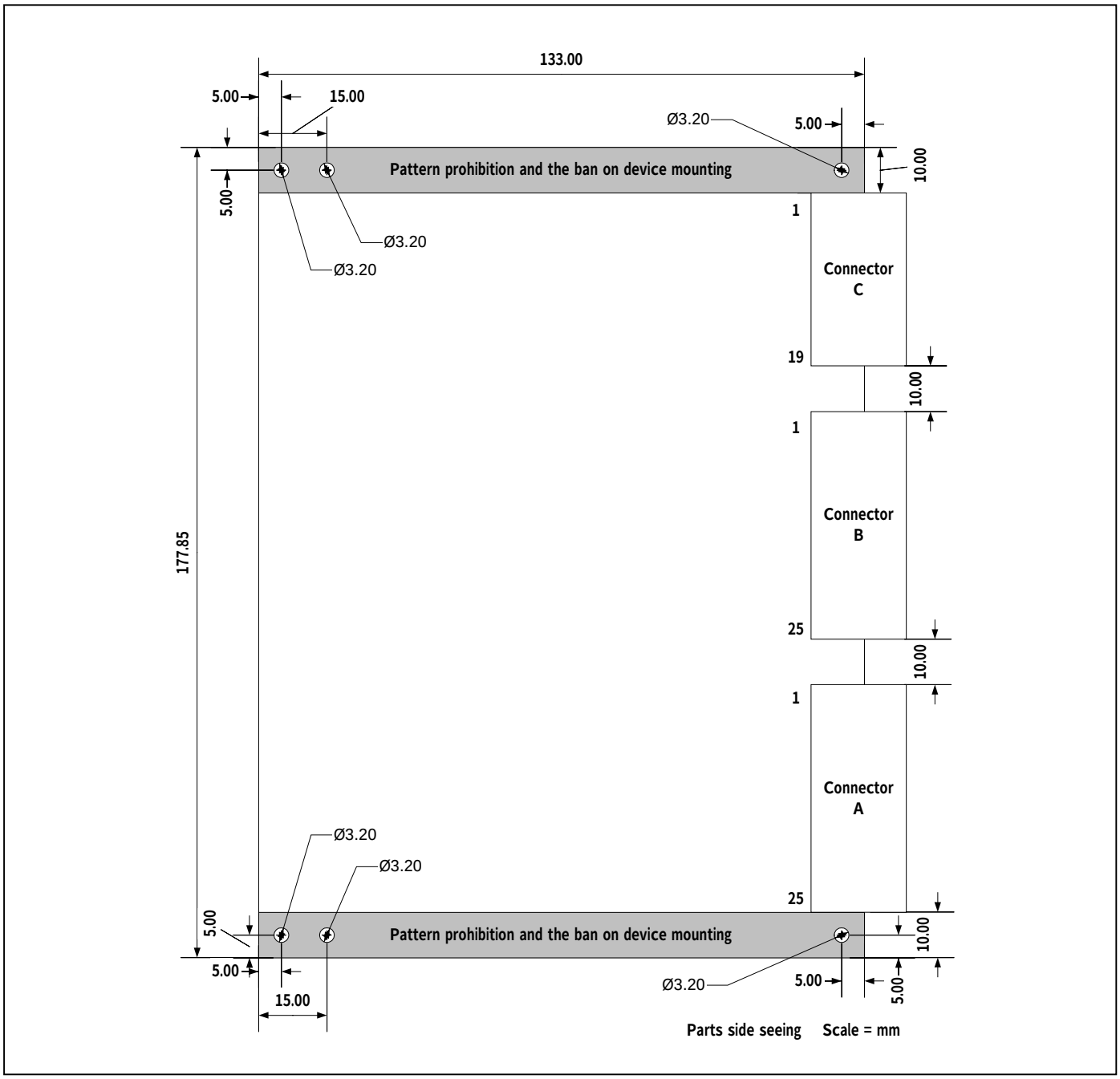


Figure 4.1.1 Add-in board size

4.1.2. PCI Extension Board

Please observe the following matters, in case a PCI extension board is created like this product of a user. A PCI extension board size figure is shown in Fig. 3.1.2.

■Board size is 133.00mm × 150.00mm fixation.

■Be careful of arrangement of the connector for board connection. (A figure is part side perspective drawing.)

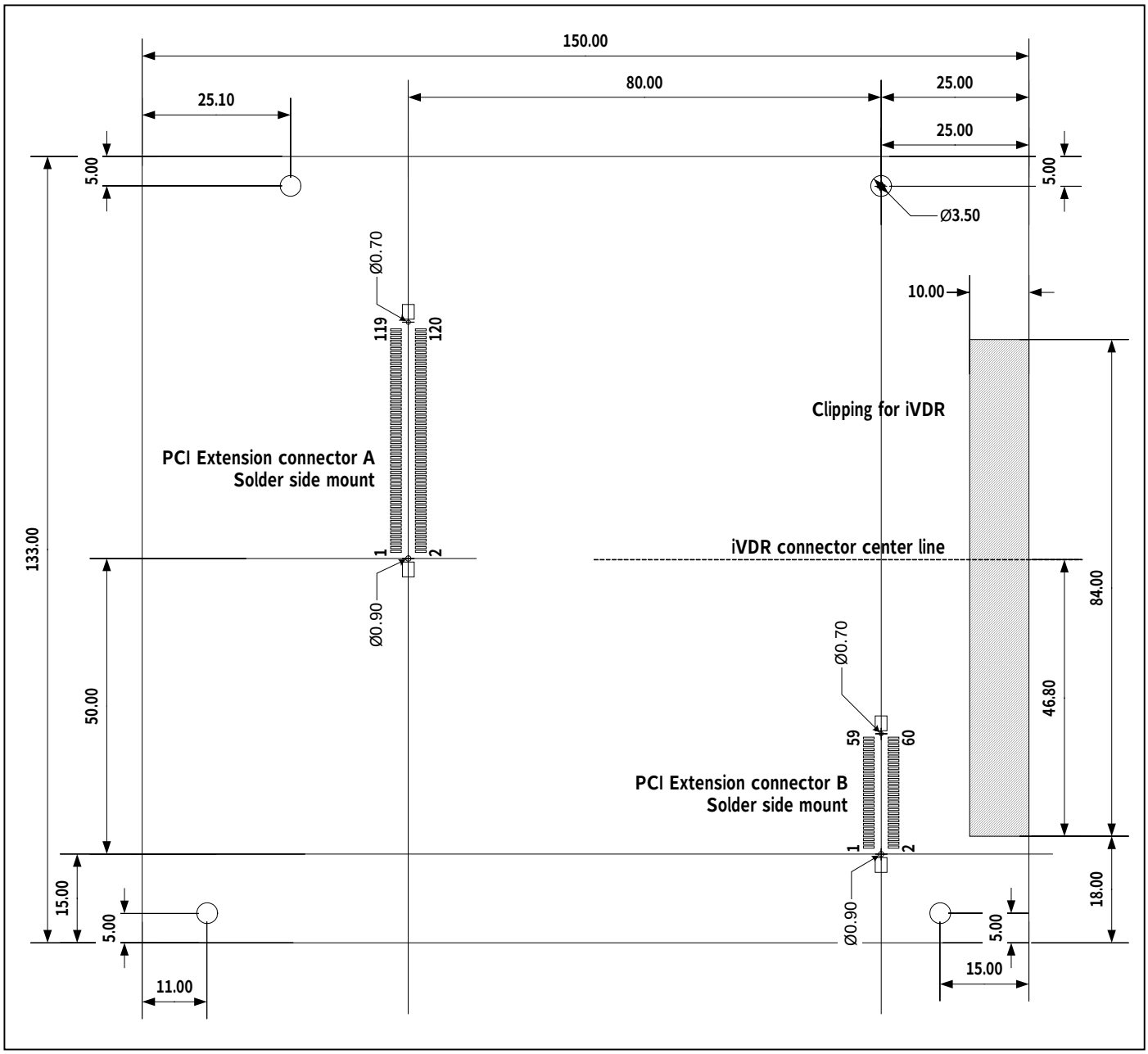


Figure 4.1.2 PCI Extension board size (A connector is part-side-seen through)

4.2. The allowable current of add-in board and PCI Extension board

The maximum consumed electric power of this product is about 11W. When you carry out use of an add-in board or the PCI card of a user, be careful of the following points.

4.2.1. The allowable current of Add-in board

When an add-in board is prepared of a user, please use the thing of the specification which does not exceed 3.3V/2A.

4.2.2. The allowable current of PCI Extension board

When a extension board is prepared of a user, please use the thing of the specification which does not exceed 3.3V/2A.

5. DB Board Specification

DB board is an add-in board for supporting the interface function for debugging of R0P7780LC0011RL.

5.1. Names of Functions of each parts of the System

The name of each part of DB board is shown in Fig. 5.1.1.

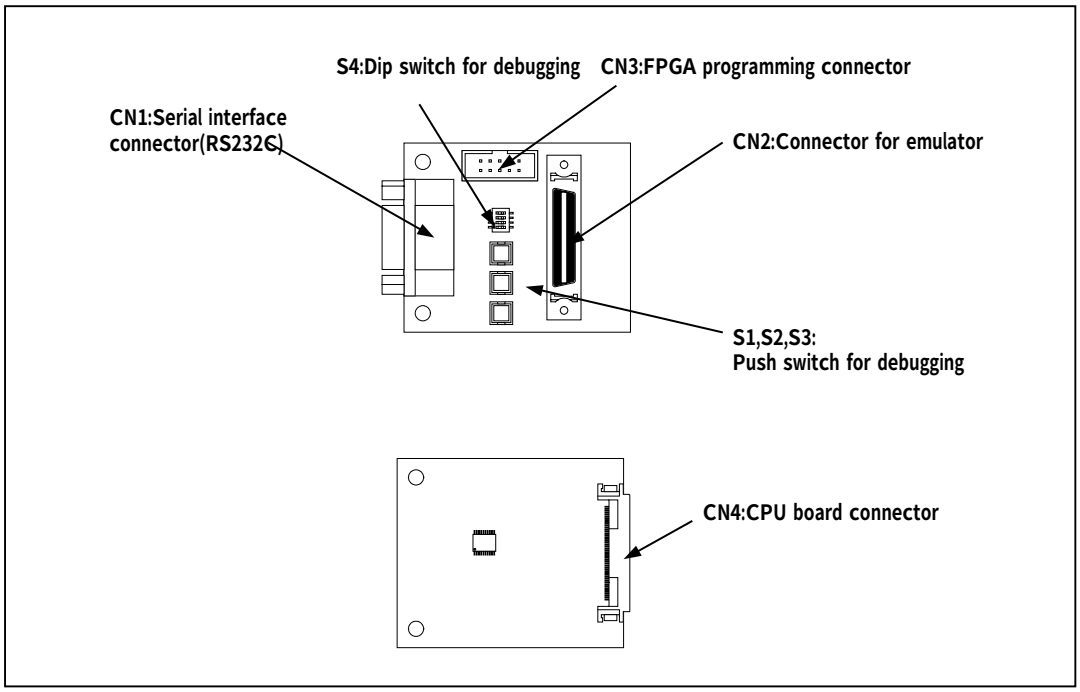


Figure 5.1.1 The name of each part of DB board

5.2. Serial Interface

CN1 is mainly used by the object for serial interface cable splicing, connecting with a console. SCIF of SH7780 is connected to Dsub9 pin connector via a RS232C driver receiver. As an exclusive clock for SCIF, a communication baud rate inputs 1.8432MHz into SH7780, and is considering it as fixation at 115200bps. It connects with a DSUB9 pin cross cable.
Signal arrangement of a serial interface connector is shown in Table 5.2.1.

Table5.2.1 Signal arrangement of a serial interface connector

Pin number	Signal name	IO	Note
1	NC		
2	RD	I	Data transmission
3	TD	O	Data reception
4	NC		
5	GND		
6	NC		
7	NC		
8	NC		
9	NC		

5.3. Connector for Emulator

CN2 is a connector for the Emulator. Signal arrangement is shown in Table 5.3.1.

Table5.3.1 Signal arrangement of Emulator interface connector

Pin number	Signal name	IO	Note
1	AUDCK	O	
2	GND	-	
3	AUDATA0	O	
4	GND	-	
5	AUDDATA1	O	
6	GND	-	
7	AUDATA2	O	
8	GND	-	
9	AUDATA3	O	
10	GND	-	
11	AUDSYNCn	O	
12	GND	-	
13	N.C.	O	
14	GND	-	
15	N.C.	O	
16	GND	-	
17	TCK	O	
18	GND	-	
19	TMS	O	
20	GND	-	
21	TRSTn	O	
22	GND	-	
23	TDI	O	
24	GND	-	
25	TDO	O	
26	GND	-	
27	ASEBRKn	O	
28	GND	-	
29	N.C.	O	
30	GND	-	
31	RESETn	O	
32	GND	-	
33	GND	-	
34	GND	-	
35	N.C.	O	
36	GND	-	

5.4. FPGA Programming Connector

CN3 is a connector for the FPGA on the R0P7780RLC0011RL. Signal arrangement is shown in Table 5.4.1.

Table5.4.1 Signal arrangement of FPGA programming connector

Pin No.	Signal Name	IO	Note
1	DB_DCLK	I	Config clock
2	GND	-	Ground
3	DB_CONFDONE	I/O	Config finish flag
4	3.3V	-	Power supply
5	DB_nCONFIG	I	Config control
6	DB_nCE	I	Chip enable
7	DB_DATA	I	Config data
8	DB_nCS	I	Control signal
9	DB_ASDO	I	Config data resad enable

5.5. DB Board Connector

CN4 is a connector for connecting with CN9 of R0P7780LC0011RL. Terminal arrangement is the same of R0P7780LC0011RL's CN9. Various debugging functions are realizable by connecting this board.

6. Linux Kernel Download

About Linux software, it is downloadable from the following URL etc.

http://www.kernel.org/

http://www.linux-sh.org/cgi-bin/moin.cgi

http://mirror.sh-linux.org/rpm-index/index.html

http://www.m17n.org/linux-sh/

http://www.superh-linux.org/

⚠ CAUTION
Downloadable software is an open source and is not contained in the range of a guarantee. **The information about GPL refers to http://www.gnu.org/copyleft/gpl.html, and please uses it in the range of a user's responsibility.**

7. Appendix

SH7780 Evaluation Platform
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R0P7780LC0011RL

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