REJ10J1322-0100

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# R0P751RLC0011RL

## User's Manual

SH7751R Evaluation Platform

User's Manual

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Renesas Technology
www.renesas.com

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# IMPORTANT INFORMATION

## READ FIRST

• READ this user's manual before using this product.
• KEEP the user's manual handy for future reference.
Do not attempt to use the product until you fully understand its mechanism.

### This Product:

In this manual, this product points out the following product which Renesas Solutions Corporation manufactured.
A user's user system and host machine are not included.

### Purpose of the Product:

This product is a device to support the development of a system that uses the SuperH Risc engine Family SH7751R of Renesas 32-bit RISC MCUs. It provides support for system development in both software and hardware. Be sure to use this product correctly according to said purpose of use. Please avoid using this product for other than its intended purpose of use.

### For those who use this product:

This product can only be used by those who have carefully read the user's manual and know how to use it. Use of this product requires the basic knowledge of electric circuits, logical circuits, and MCUs.

### Precautions to be Taken when Using This Product:

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(9) Operation of all CF cards cannot be guaranteed.
(10) Connection with the apparatus of all LAN interfaces cannot be guaranteed.
(11) When you do not use it for a long time, please pull out and keep a power supply plug from a plug socket etc. for safety.
(12) This product is a lead free mounting product.
(13) Generally each brand name carried in these data is each maker's trademark or registered trademark.
(14) Near DC jack of this product becomes high temperature. Be careful of a burn.

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* Compact Flash™ is the registered trademark of SanDisk Corporation.

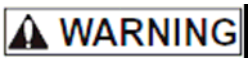
# Precautions for Safety

## Definitions of Signal Words

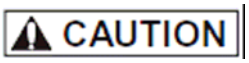
In both the General Information Manual and on the product itself, several icons are used to insure proper handling of this product and also to prevent injuries to you or other persons, or damage to your properties.
This chapter describes the precautions which should be taken in order to use this product safely and properly.
Be sure to read this chapter before using this product.

This symbol represents a warning about safety. It is used to arouse caution about a potential danger that will possibly inflict an injury on persons. To avoid a possible injury or death, please be sure to observe the safety message that follows this symbol.

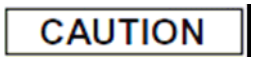

**DANGER** indicates an imminently dangerous situation that will cause death or heavy wound unless it is avoided. However, there are no instances of such danger for the product presented in this manual.




**WARNING** indicates a potentially dangerous situation that will cause death or heavy wound unless it is avoided.




**CAUTION** indicates a potentially dangerous situation that will cause a slight injury or a medium-degree injury unless it is avoided.




**CAUTION** with no safety warning symbols attached indicates a potentially dangerous situation that will cause property damage unless it is avoided.

**NOTE** emphasizes essential information.

In addition to the five above, the following are also used as appropriate.

△ means WARNING or CAUTION.
Example:

**CAUTION AGAINST AN ELECTRIC SHOCK**

⃠ means PROHIBITION.
Example:

**DISASSEMBLY PROHIBITED**

● means A FORCIBLE ACTION.
Example:

**UNPLUG THE POWER CABLE FROM THE RECEPTACLE.**

## CAUTION

Warnings for AC Power Supply:

- If If the attached AC power cable does not fit the receptacle, do not alter the AC power cable and do not plug it forcibly. Failure to comply may cause electric shock and/or fire.
- Use an AC power cable which complies with the safety standard of the country.
- Do not touch the plug of the AC power cable when your hands are wet. This may cause electric shock.
- This product is connected signal ground with frame ground. If your developing product is transformless (not having isolation transformer of AC power), this may cause electric shock. Also, this may give an unrepairable damage to this product and your developing one.
  While developing, connect AC power of the product to commercial power through isolation transformer in order to avoid these dangers.
- If other equipment is connected to the same branch circuit, care should be taken not to overload the circuit.

- If you smell a strange odor, hear an unusual sound, or see smoke coming from this product, then disconnect power immediately by unplugging the AC power cable from the outlet.
  Do not use this as it is because of the danger of electric shock and/or fire. In this case, contact your local distributor.
- Before setting up this product and connecting it to other devices, turn off power or remove a power cable to prevent injury or product damage.

Warnings to Be Taken for This Product:

- Do not disassemble or modify this product. Personal injury due to electric shock may occur if this product is disassembled and modified.
- Make sure nothing falls into the cooling fan on the top panel, especially liquids, metal objects, or anything combustible.

Warning for Installation:

- Do not set this product in water or areas of high humidity. Make sure that the product does not get wet. Spilling water or some other liquid into the product may cause unrepairable damage.
- Please use this product indoors.

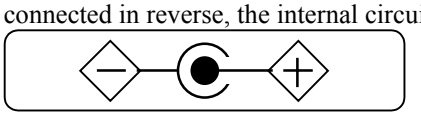
Warning for Use Environment:

- This equipment is to be used in an environment with a maximum ambient temperature of 35°C. Care should be taken that this temperature is not exceeded.

## CAUTION

Note on Connecting the Power Supply:

- Do not use any power cable other than the one that is included with the product.
- At the time of connection with installation of this product or other equipments, please extract an AC/DC adaptor from a plug socket and prevent an injury and an accident.
- Pay attention to the polarities of the power supply. If its positive and negative poles are connected in reverse, the internal circuit may be broken.



Power supply injection :

- Once the power is turned off, wait for about 10 seconds before turning it back on again.

Cautions to Be Taken for Handling This Product:

- Handle the product with caution, taking care not to apply strong mechanical shock to the product by dropping or letting it fall down.
- Do not touch the communication interface connector pins or other connector pins directly with your hand. Static electricity from your body may break down the internal circuit of the product.
- Do not pull the product by the cable connecting to a board in it. Do not hold down a board while you pull the other end of it. The cable may break.

Contents

# 1. Outline

## 1.1. Package Components

This product is constituted by the following board and parts. When opened, please check whether it has gathered altogether.

Table 1.1.1 The contents list of packing

| Item | Description | Quantity |
|---|---|---|
| R0P751RLC0011RL | SH7751R Platform | 1 |
| FROM Board (Bus width is 32bit 64M Byte) | Within boot loader | 1 |
| AC Adapter | DC12.0V 5.0A | 1 |
| CD-ROM | User's manual , Sample program etc. | 1 |

* If there is any question or doubt about the packaged product, contact your local distributor.

## 1.2. System Configuration

### 1.2.1. System Configuration

Figure 1.2.1 shows the system configuration.

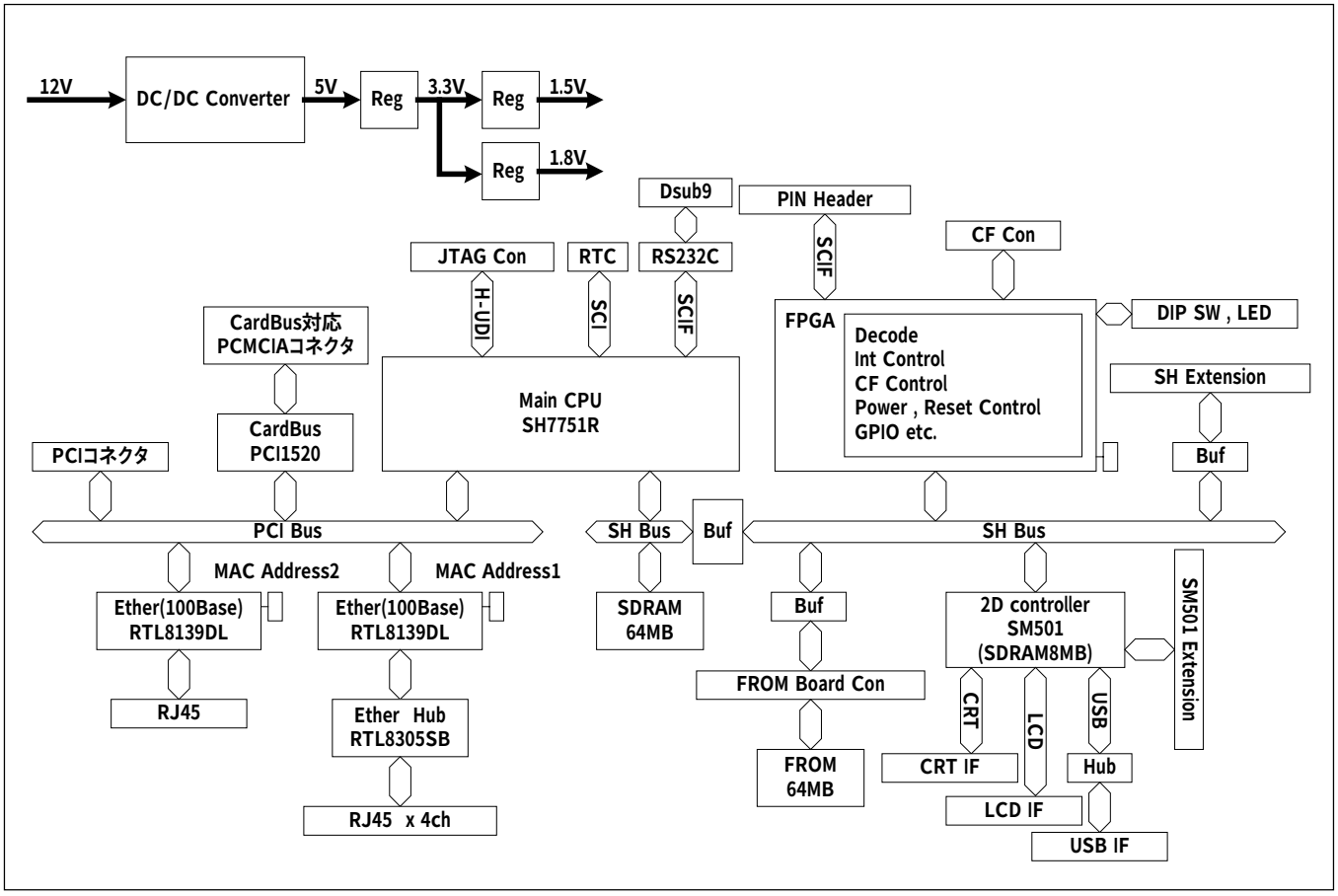



Figure 1.2.1 R0P751RLC0011RL system configuration

### 1.2.2. Names and Functions of each part of the System

Figure 1.2.2 shows the names of parts reference.

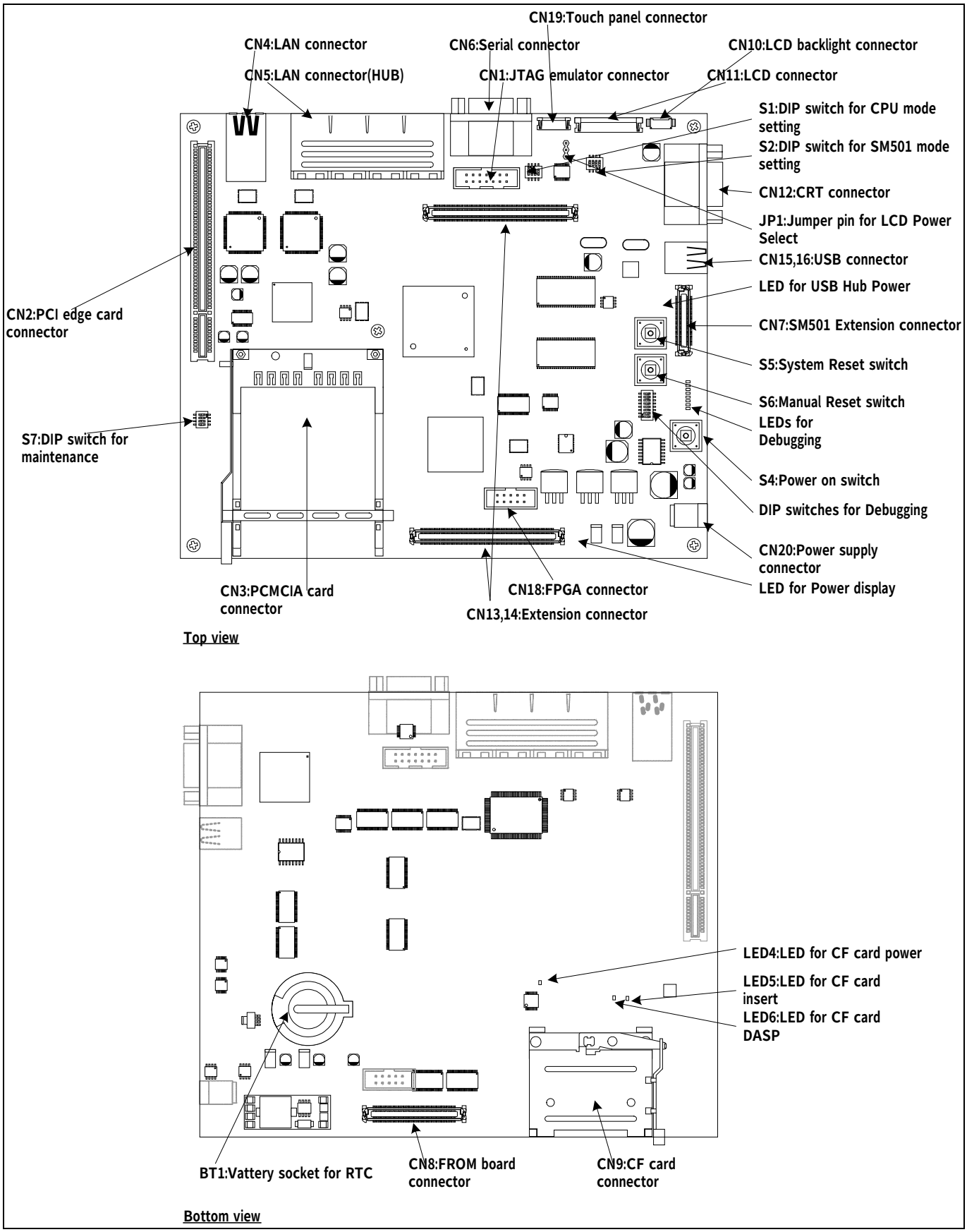



Figure 1.2.2 Name of R0P751RLC0011RL's parts reference

## 1.3. Setup Method (Up to Boot loader starting)

Figure 1.3.1 shows the setting up this system. Please prepare the follows:

■Console PC

■RS232C cross cable

Please prepare CF card, a CRT monitor, network environment, etc. if needed.

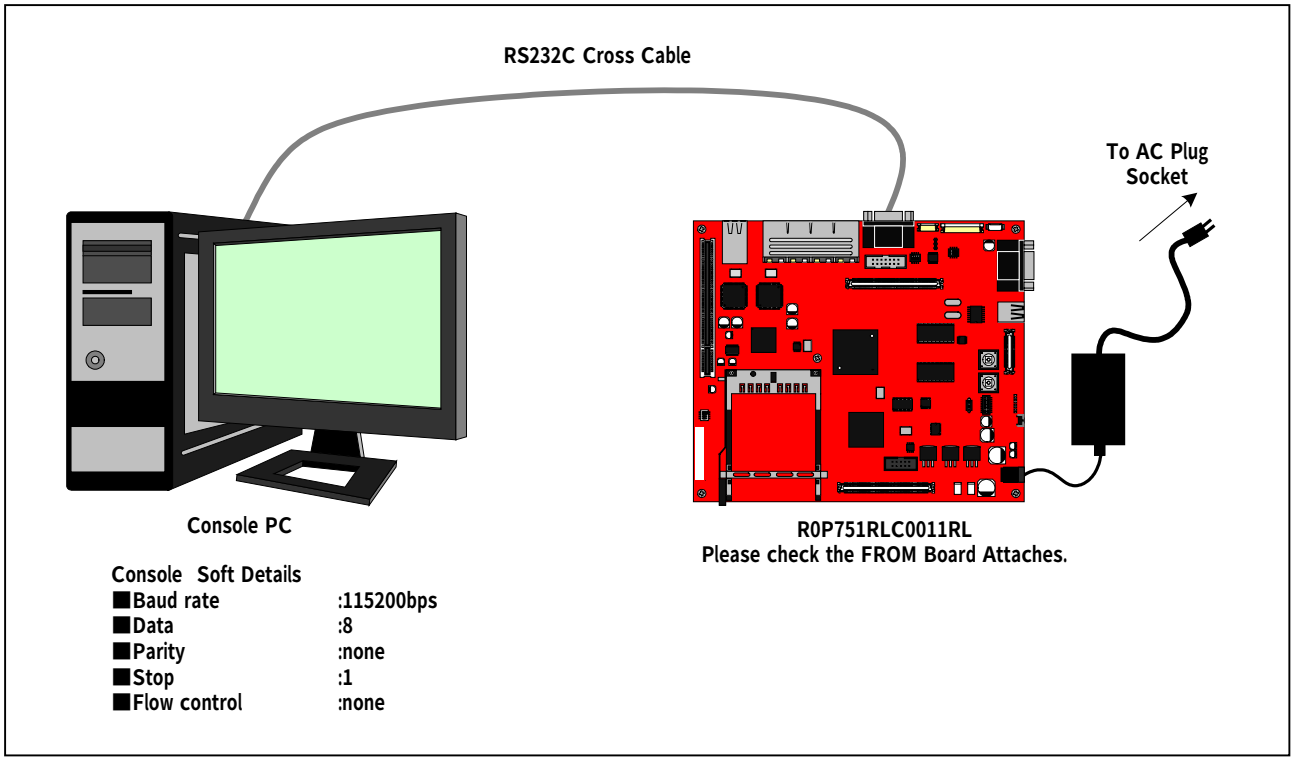



Figure 1.3.1 Set Up this system

(1) Please attach the FROM board in CN8 mounted in the solder side of R0P751RLC0011RL. (Be careful of poor contact.)

| CAUTION |
|---|
| Where the power supply of this product is intercepted, please be sure to make connection of a FROM board.<br>Moreover, be careful of poor contact of a FROM board. The mistaken usage leads to destruction of this product. |

(2) Connect the terminal for consoles with this board with a RS232C cross cable.

(3) Start terminal software on the terminal for consoles.

(baudrate:115200bps, data:8bit, parity:none, stop bit:1bit, flow control:none)

(4) Insert an attached AC/DC adaptor in CN20, and connect with a plug socket.

(5) If S4 of R0P751RLC0011RL is pushed, a power supply injection will be carried out. (Red button)

| CAUTION |
|---|
| If S4 is pushed again, power supply interception is possible. However, while using CF card, please carry out power supply interception processing in carried FPGA. When S4 is pushed during CF card operation and power supply interception is performed, there is possibility of destruction of CF card. Please refer to the clause of FPGA functional explanation about the specification of FPGA. |

## 1.4. Specification List

Table 1.4.1 shows a list of specifications.

Table 1.4.1 R0P751RLC0011RL Specifications

| Item | Description |
|---|---|
| CPU | HD6417751RBP240 (Renesas Technorogy)<br>・Input Clock: 20MHz<br>・CPU Clock(I): 240MHz (Mode 5)<br>・Bus Clock(B): 120MHz (Mode 5)<br>・Peripheral Clock(P): 60MHz (Mode 5)<br>・PCI Bus: 33MHz (4ch)<br>・Package: 256pins BGA (1.27mm pitch) |
| Memory | FROM board:S29PL127J60TFI130 (Spansion)<br>・FROM:64M Byte、32bit Bus Access |
| | EDS2516ADTA-75E (Elpida memory)<br>・SDRAM:64MB<br>・32bit Bus Access |
| FPGA | EP1C4F400C8N (ALTERA)<br>・Address Decode ,Interrupt control ,CF control etc.<br>Configuration ROM: EPCS4SI8N |
| 2D Graphic Controller | SM501GX08LF00-AB (Silicon Motion) |
| LAN Controller | RTL8139DL-LF (Realtek)<br>LAN Connector: LU1S041C-43-LF(BOTHHAND) |
| LAN Hub Controller | RTL8305SB-VD-LF (Realtek)<br>LAN Connector:0810-1X4T-36-F(BelFuse) |
| CardBus Controller | PCI1520ZHK (Texas Instruments) |
| Real Time Clock | RTC-9701JE(Epson Toyocom)<br>・Uses SH7751R'SCI |
| LED | ・for Debugging (8):Control FPGA register<br>・for Status (6) |
| Switch | ・for Power ON (x 1)<br>・for RESET (x 2)<br>・for Debugging (8bit x 1)<br>・for Mode setting (4bit x 2) |
| Compact Flash Card Connector | Header: ICM-MA2H-SS52-N11B(LF)(SN) (JST)<br>Ejector: ICME-CB68L5-302N (JST) |
| PCMCIA Card Connector | Header: ICM-CB68H-S112-502N(LF)(SN) (JST)<br>Ejector:ICM-MAE-R32 (JST) |
| Serial Connector | RS232C Connector:JEY- 9P-1A2B (JST)<br>SH7751R's SCIF |
| Connectors | SH Bus Extension connector: 52837-1679 (Molex) |
| | FROM board connector:52837-1079 (Molex) |
| | SM501 Extension connector:52837-0679 (Molex) |
| | USB connector:XM7A-0442-A (Omron) |
| | CRT connector:XM4L-1542-132 (Omron) |
| | LCD connector:40FLH-SM1-TB(LF)(SN) (JST) |
| | LCD backlight connector:53261-0590 (Molex) |
| | Touchpanel interface connector:<br>14FLH-SM1-TB (LF)(SN) (JST) |
| | SH7751R JTAG Emulator connector (14pins)<br>XG4C-1031 (Omron) |
| | EPCS4SI8N connector (10pins)<br>XG4C-1431 (Omron) |

| Item | Description |
|---|---|
| Power IN | 2.1mmSocket Center Plus<br>・From AC/DC Adapter |
| Size | ・Size: 170mm × 200mm |
| Operating temperature | 5 to 35°C (no dew) |
| Storage temperature | -10 to 60°C (no dew) |

## 1.5. Address Map

Figure 1.5.1 shows Address Map. Please refer to the clause of FPGA functional explanation about the specification of FPGA.

| | | | |
|---|---|---|---|
| H'0000_0000<br><br>H'03FF_FFFF | Area 0 | 32bit | FROM Area (64MB) |
| H'0400_0000<br>H'0400_004F<br>H'0400_0050<br><br>H'07FF_FFFF | Area 1 | 16bit | FPGA Area (80B)<br>Disable Area (FPGA Shadow) |
| H'0800_0000<br><br>H'0BFF_FFFF | Area 2 | 8/16/32 bit | Extension Area (64MB) |
| H'0C00_0000<br><br>H'0FFF_FFFF | Area 3 | 32bit | SDRAM Area (64MB) |
| H'1000_0000<br><br>H'13FF_FFFF | Area 4 | 32bit | SM501GX08LF00 Area |
| H'1400_0000<br><br>H'17FF_FFFF | Area 5 | 16bit | Compact FLASH Area (64MB) |
| H'1800_0000<br><br>H'1BFF_FFFF | Area 6 | 8/16/32 bit | Extension Area (64MB) |

Figure 1.5.1 SH7751R Address Map

# 2. Functional Specification

## 2.1. Power Supply Specification

This board operates by supply of 12V from an attached AC/DC adaptor.

A power supply system figure is shown in Fig. 2.1.1

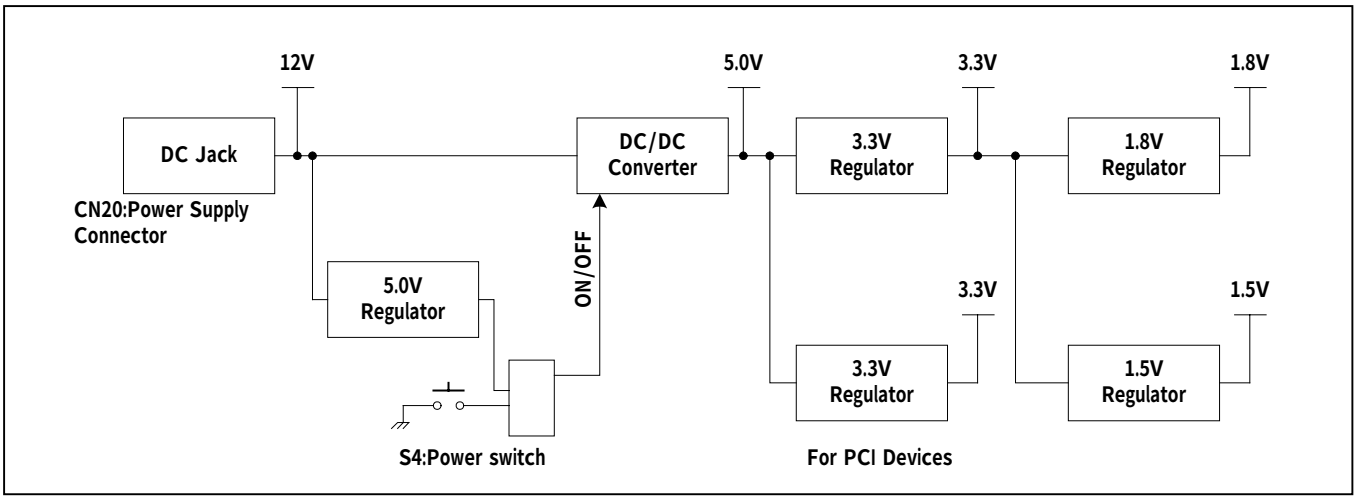



Figure 2.1.1 power-supply system figure

Each voltage is used by the following blocks. The main power supply use blocks are shown in Table 2.1.1.

Table 2.1.1 The main power supply use blocks

| Voltage | Use place | Note |
|---|---|---|
| 12V | PCI connector | |
| | PCMCIA connector | |
| | Inverter for LCD | |
| | The connector for extension | |
| 5.0V | Standby power | |
| | PCI connector | |
| | PCMCIA connector | |
| | LAN controller | RTL8139DL |
| | USB Hub controller | |
| | 拡張connector | |
| 3.3V | PCI connector | |
| | PCMCIA connector | |
| | SH7751R | HD6417751RBP240 |
| | FROM | S29PL127J60TFI130 |
| | SDRAM | EDS2516ADTA |
| | FPGA | EP1C4F400C8N |
| | SM501 | SM501GX08LF00 |
| | CF card connector | |
| | CardBus card controller | PCI1520ZHK |
| | LAN controller | RTL8139DL |
| | LAN Hub controller | RTL8305SB |
| | The connector for extension | |
| 1.8V | SM501 core power | SM501GX08LF00 |
| 1.5V | SH7751R core power | HD6417751RBP240 |
| | FPGA core power | EP1C4F400C8N |

### 2.1.1. DC Jack Input Power Supply

The input power supply specification from DC jack of this board is shown.
Please choose the power supply which suits the specification shown in Table 2.1.2 in the case of use of except for an attached AC/DC adaptor.

Table 2.1.2 DC jack input specification.

| Item | Specification |
|---|---|
| Plug | Φ2.5mm |
| Plug Polarity | Outside: Minus, inner side:Plus.   |
| Input voltage | 12.0V |
| Supply current | More than 5.0A |

**CAUTION**

Keep in mind that near DC jack becomes high temperature very much at the time of this product operation.

**WARNING**

When an AC/DC adaptor with the reverse polarity of a plug is used, it leads to destruction of this product.
Moreover, keep in mind that there is possibility of emitting smoke and ignition.

## 2.2. Switches Specification

Three push switches and three DIP switches are mounted in this board.

### 2.2.1. DIP Switch for CPU Mode Setup

S1 is the DIP switch for a mode setup of operation of SH7751R. The clock mode and the endian of SH7751R are specified. The S1 specification is shown in Table 2.2.1 and the S1appearance figure is shown in Fig. 2.2.1. It is in a shading state at the time of shipment, it was made into the clock mode 5 (internal:240MHz, external bus:120MHz, circumference module:60MHz), and is set as a little endian.

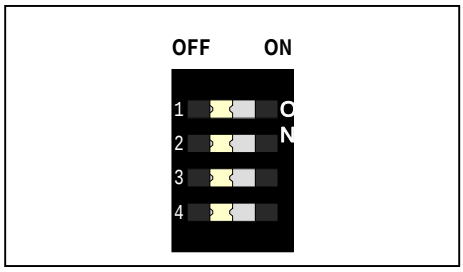



Figure 2.2.1 S1 appearance figure

Table 2.2.1 S1 specification.

| Switch | Connection terminal | ON | OFF | Function |
|---|---|---|---|---|
| S1-1 | SH7751R_MD0 | H | L | A setup of an clock mode |
| S1-2 | SH7751R_MD1 | H | L | |
| S1-3 | SH7751R_MD2 | H | L | |
| S1-4 | SH7751R_MD5 | H | L | A setup of an endian<br>L:Big endian<br>H:Little endian |

### 2.2.2. DIP Switch for Debugging

S3 is a DIP switch for debugging. It can connect with FPGA and can refer to by the dedicated register. It can be used of a user. Please refer to the clause of FPGA functional explanation about the specification of FPGA. The S3 appearance figure is shown in Table 2.2.2 and the S3 specification is shown in Fig. 2.2.2.

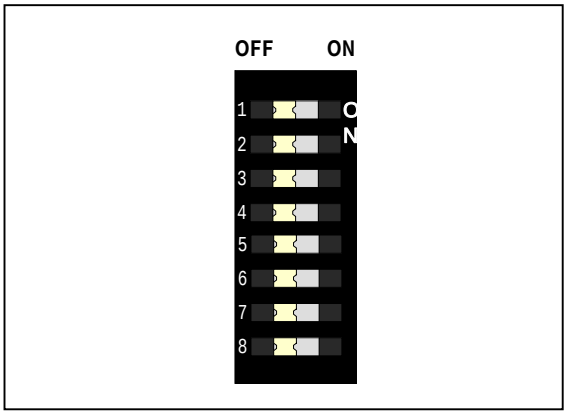



Figure 2.2.2 S3 appearance figure.

Table 2.2.2 S3 specification.

| Switch | Connection terminal | ON | OFF | Function |
|---|---|---|---|---|
| S3-1 | FPGA | H | L | Reference is possible at FPGA |
| S3-2 | FPGA | H | L | |
| S3-3 | FPGA | H | L | |
| S3-4 | FPGA | H | L | |
| S3-5 | FPGA | H | L | |
| S3-6 | FPGA | H | L | |
| S3-7 | FPGA | H | L | |
| S3-8 | FPGA | H | L | |

### 2.2.3. Power On Switch

S4 is a power supply switch. Key-top is "red". After inserting an attached AC/DC adaptor in CN20, a power supply is supplied to this board under switch-pushing. A power supply is again intercepted under S4 swich-pushing at the time of this board operation.

**CAUTION**

The method of power supply interception is controllable by "S4 switch-pushing" or the control from FPGA. When you perform sudden power supply interception by S4, since the data of CF card etc. may be destroyed, please perform power supply interception by the control from FPGA.
Please refer to the clause of FPGA functional explanation about the specification of FPGA.

### 2.2.4. Switch for System Reset

S5 is a system-reset switch. A key-top is "white". A reset pulse is generated to this timing in each device under S5 swich-pushing. The explanation about a reset signal is indicated to "2.15 Reset signal".

### 2.2.5. Switch for Manual Reset

S6 is a manual reset switch. A key-top is "blue". Manual reset is inputted into SH7751R under S6 swich-pushing. There is no input to other devices. The explanation about a reset signal is indicated to "2.15 Reset signal" .

### 2.2.6. DIP Switch for Maintenance

S7 is a DIP switch for a maintenance setup. Moreover, the bus width of FROM at the time of starting is also set up by ON/OFF of bit4.

It can connect with FPGA and can refer to by the dedicated register. Please refer to the clause of FPGA functional explanation about the specification of FPGA. An attached FROM board is connected, and if bit1 is set as "ON" and started, it will start in maintenance mode.

By starting in maintenance mode, use of boot loader update and test mode is attained.

Please refer to the clause of boot loader functional explanation about the specification in boot loader update and test mode.

The S7 specification is shown in Table 2.2.6 and the S7 appearance figure is shown in Fig. 2.2.6. It is in a shading state at the time of shipment, and it is set as normal mode starting and a bus width of 32 bits.

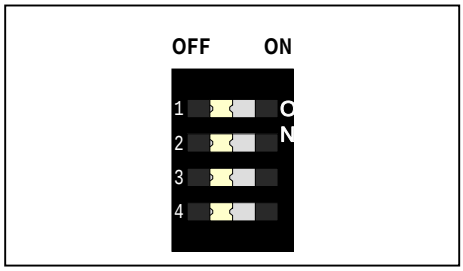



Figure 2.2.6 S7 appearance figure

Table 2.2.6 S7 specification

| Switch | Connection terminal | ON | OFF | Function |
|---|---|---|---|---|
| S7-1 | FPGA | H | L | Boot loader mode |
| S7-2 | FPGA | H | L | Reservation |
| S7-3 | FPGA | H | L | Reservation |
| S7-4 | SH7751R_MD3 | H | L | Area 0 bus width is specified<br>0：16bit / 1：32bit |

## 2.3. LED Specification

### 2.3.1. LED for the SH7751R status

LED1 is LED for a status display of SH7751R. It has connected with STATUS1, and STATUS0 of SH7751R ports. Functional assignment of LED is shown in Table 2.3.1.

Table 2.3.1 LED functional assignment.

| LED | Function | Status |
|---|---|---|
| LED1 | Reset | Lighting off |
| | Sleep | Green lighting |
| | Standby | Red lighting |
| | Nomal | Orange lighting |

### 2.3.2. LED for the Ethernet Hub

LED2 and LED3 are connected to LED_ACT4, and LED_SPD4 of RTL8305SB. A function changes with setup of RTL8305SB. Please refer to the data of RTL8305SB about the details of the usage.

### 2.3.3. LED for the CF Card

LED4, LED5, and LED 6 are LED for CF cards. It is automatically controlled by CF card insertion.
LED functional assignment is shown in Table 2.3.2.

Table 2.3.2 LED functional assignment

| LED | Function | Status |
|---|---|---|
| LED4 | At the time of the power supply to CF card | Lighting |
| LED5 | At the time of CF card insertion | Lighting |
| LED6 | At the time of CF_DASP mode | Lighting |

### 2.3.4. LED for the USB Hub

LED7 and LED8 are connected to a USB Hub controller. If a power supply is supplied to each USB connector, it will light up.LED functional assignment is shown in Table 2.3.3.

Table 2.3.3 LED functional assignment

| LED | Function | Status |
|---|---|---|
| LED7 | It is power supply supply to USB Hub No.1 | Lighting |
| LED8 | It is power supply supply to USB Hub No.2 | Lighting |

### 2.3.5. LED for Power Supply

LED17 is LED for a power supply display. If a power supply is supplied to this board, it will light up.

### 2.3.6. LED for Debugging

LED9 to LED16 are LED for debugging. It is controllable by FPGA. Please refer to the clause of FPGA functional explanation about the specification of FPGA.

## 2.4. JTAG Emurator Interface

CN1 is a connector for JTAG emulator. The emulator which used the H-UDI interface of SH7751R is connected. Please use it, connecting the emulator corresponding to H-UDI made from Renesas Technology Corp.

The general-view figure of a JTAG emulator connector is shown in Fig. 2.4.1, and signal arrangement is shown in Table 2.4.1.

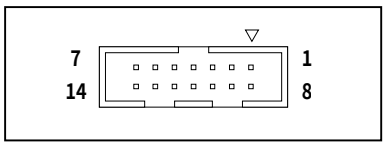



Figure 2.4.1 Appearance figure of JTAG emulator connector

Table 2.4.1 Signal arrangement of JTAG emulator connector

| Pin number | Signal name |
|---|---|
| 1 | TCK |
| 2 | TRST# |
| 3 | TDO |
| 4 | ASEBRK# |
| 5 | TMS |
| 6 | TDI |
| 7 | RESET# |
| 8 | GND |
| 9 | GND |
| 10 | GND |
| 11 | NC |
| 12 | GND |
| 13 | GND |
| 14 | GND |

## 2.5. Memories

The list of the memory carried in this product is shown in Table 2.5.1.

Table 2.5.1 memory list

| Classification | Start address | Size | Bus width | Note |
|---|---|---|---|---|
| External FROM | H'0000_0000 | 64MB | 32bit | At the time of mounting of an enclosed FROM board |
| External SDRAM | H'0C00_0000 | 64MB | 32bit | |

### 2.5.1. An Access Timing Setup to Each Device Connected to SH Bus

The timing specification of each device linked to the SH7751R local bus of this board is shown in Table 2.5.2.

(STATUS: Input clock is 20MHz and CPU modeis mode5)

Table 2.5.2 The timing specification of each device

| Area | Classification | Product name | Bus width | Timing specifications |
|---|---|---|---|---|
| 0 | FROM Board | S29PL127J60TFI130 | 32 | The number of soft waits: 9 |
| 1 | FPGA | EP1C4F400C8N | 16 | The number of soft waits: 3 |
| 3 | SDRAM | EDS2516ADTA-75-E | 32 | CAS latency: 3 |
| 4 | 2DGraphic controller | SM501GX08LF00-AB | 32 | The number of soft waits: 9 |
| 5 | CF card | CF card | 16 | The number of SH7751R soft waits: 12<br>The CFCTL register of FPGA also needs to be set up. |

## 2.6. PCI Devices

With this board, one PCI connector, one CardBus card controller, and two LAN controllers are connected to the PCI bus of SH7751R. One of two LAN controllers connects a Hub controller, and it has 4 ports.

Each device number (DEVNO) is shown in Table 2.6.1. A device number is a number of a device set as the object of configuration access.

Table 2.6.1 device number list

| DEVNO | Device | Function | Interruption |
|---|---|---|---|
| H'0 | PCI card connector | all-purpose PCI card | PCI_INTA |
| H'1 | RTL8139DL<br>(with RTL8305SB) | Ethernet 10/100Base<br>(with Ethernet Hub) | PCI_INTB |
| H'2 | PCI1520ZHK | PCI – CardBus bridge | PCI_INTC |
| H'3 | RTL8139DL | Ethernet 10/100Base | PCI_INTD |

### 2.6.1. CI Card Slot

CN2 is a PCI card connector. It has connected with the PCI bus of SH7751R.

**CAUTION**

Although the connector based on PCI 5V card specification is mounted, a PCI bus signal should use the card of 3.3V signal specification for the specification of SH7751R. If 5V signal is supplied to SH7751R, there is a possibility of destroying SH7751R.

### 2.6.2. CardBus Card Connector

CN3 is a CardBus card controller, PCI1520ZHK (made from Texas Instruments) is connected to the PCI bus of SH7751R.

This controller supports the PC card and 3.3V CardBus card of 5V/3.3V mixture.

Please refer to the data of PCI1520ZHK about the details of the usage.

### 2.6.3. LAN Connector

This board -- as an Ethernet controller -- the product made from REALTEK -- two RTL8139DL(s) are mounted .

Please refer to the data of RTL8139DL about the details of the usage.

Moreover, RTL8139DL arranged for the device number 1 is connected to Hub controller RTL8305SB.

A Hub-controller (RTL8305SB) supports 4 ports.

#### 2.6.3.1. MAC Address Assignment

The MAC Address is written in external EEPROM of RTL8139DL. Please refer to MAC1 and MAC2 on the solder side of this product.

MAC1 is supported the device number 1and MAC2 is supported the device number 3.

## 2.7. 2D Graphic Controller Interface

This board -- as 2D graphic controller -- Silicon Motion Inc. make -- SM501GX08LF00-AB is mounted.
It has connected with SH bus. About the "RDY" signal to SH7751R, timing adjustment is carried out in FPGA.
Please refer to the data of SM501GX08LF00-AB about the details of the usage.

| **CAUTION** |
|---|
| HCLK supplied to SM501GX about this product is use limitation in a laboratory, and Silicon Motion Inc. consents to operation by a maximum of 120MHz. In the adoption to a user's product, please perform a sufficient examination and sufficient evaluation. |

### 2.7.1. CRT Connector

CN12 is a connector for CRT connection. It has connected with the CRT output terminal of SM501.
Signal arrangement of the connector for CRT interfaces is shown in Table 2.7.1.

Table 2.7.1 Signal arrangement of connector for CRT interfaces

| Pin number | Signal name |
|---|---|
| 1 | R |
| 2 | G |
| 3 | B |
| 4 | NC |
| 5 | GND |
| 6 | GND |
| 7 | GND |
| 8 | GND |
| 9 | NC |
| 10 | GND |
| 11 | NC |
| 12 | NC |
| 13 | CRTHS |
| 14 | CRTVS |
| 15 | NC |

### 2.7.2. LCD Connector

CN11 is a connector for LCD interfaces. It has connected with the LCD output terminal of SM501.
Please use it according to the specification of LCD which the user adopted. The supply voltage of LCD can be chosen in JP1.
The connectors currently used are 40 FLH-SM1-TB (LF), and (SN) (made from the J.S.T. Mfg Co.,Ltd) The appearance figure of the connector for LCD interfaces is shown in Fig. 2.7.2, and signal arrangement is shown in Table 2.7.2.

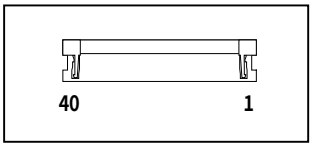



Figure 2.7.2 Connector appearance figure for LCD interfaces

Table 2.7.2 Signal arrangement of connector for LCD interfaces

| Pin number | Signal name | Note |
|---|---|---|
| 1 | GND | |
| 2 | CK | Clock signal |
| 3 | GND | |
| 4 | HSYNC | Horizontal Synchronizing signal |
| 5 | GND | |
| 6 | VSYNC | Vertical Synchronizing signal |
| 7 | GND | |
| 8 | R0 | Red data |
| 9 | R1 | |
| 10 | R2 | |
| 11 | R3 | |
| 12 | R4 | |
| 13 | R5 | |
| 14 | GND | |
| 15 | G0 | Green data |
| 16 | G1 | |
| 17 | G2 | |
| 18 | G3 | |
| 19 | G4 | |
| 20 | G5 | |
| 21 | GND | |
| 22 | B0 | Blue data |
| 23 | B1 | |
| 24 | B2 | |
| 25 | B3 | |
| 26 | B4 | |
| 27 | B5 | |
| 28 | GND | |
| 29 | FPEN | LCD enable |
| 30 | GND | |
| 31 | GND | |
| 32 | NC | |
| 33 | NC | |
| 34 | VCC | 3.3V/5.0V change is possible at J1.<br>1-2 short-circuit: 3.3V<br>2-3 short-circuit: 5.0V<br>It is 3.3V setup at the time of shipment. |
| 35 | VCC | |
| 36 | VCC | |
| 37 | VCC | |
| 38 | VCC | |
| 39 | VCC | |
| 40 | VCC | |

### 2.7.3. LCD Back Light Connector

CN10 is a connector for LCD inverter connection. The appearance figure of the connector for LCD inverter connection is shown in Fig. 2.7.3, and signal arrangement of the connector for LCD inverter connection is shown in Table 2.7.3.
The connector currently used is the product 53261-0571 made from Molex. Conformity housing is 51021-0500.

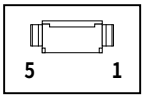



Figure 2.7.3 Connector appearance figure for LCD inverter connection

Table 2.7.2 Signal arrangement of connector for LCD inverter connection

| Pin number | Signal name | Note |
|---|---|---|
| 1 | VCC | 12.0V |
| 2 | GND | |
| 3 | VRMT | Inverter ON/OFF |
| 4 | VR0 | Brightness (however, short at 20Kohm). |
| 5 | VR1 | |

### 2.7.4. USB Connector

CN15 and CN16 are the connectors for USB connection. The USB terminal of SM501 is connected to LSI for USB Hub, and 2ch mounting is carried out. It is based on USB1.1.

### 2.7.5. SM501 Extention Connector

CN17 has connected the signal of I2C of SM501 and a ZV port, and AC97 and UART. The connector has not mounted. Please prepare of a user if needed. An assumption connector is the product 52837-0679 made from Molex.
Signal arrangement is shown in Table 2.7.5.

Table 2.7.5 Signal arrangement of SM501 extension interface connector

| Pin number | Signal name | Note | Pin number | Signal name | Note |
|---|---|---|---|---|---|
| 1 | 5.0V | | 31 | GPIO59 | ZV port |
| 2 | 5.0V | | 32 | GPIO29 | |
| 3 | 5.0V | | 33 | GPIO60 | ZV port |
| 4 | 5.0V | | 34 | GPIO37 | UART |
| 5 | GND | | 35 | GPIO61 | ZV port |
| 6 | GND | | 36 | GND | |
| 7 | GPIO16 | ZV port | 37 | GPIO62 | ZV port |
| 8 | GND | | 38 | GND | |
| 9 | GPIO17 | ZV port | 39 | GPIO63 | ZV port |
| 10 | GND | | 40 | GND | |
| 11 | GPIO18 | ZV port | 41 | GND | |
| 12 | GPIO24 | AC97 | 42 | GPIO38 | UART |
| 13 | GPIO19 | ZV port | 43 | VP_HREF | ZV port |
| 14 | GPIO25 | AC97 | 44 | GND | |
| 15 | GPIO20 | ZV port | 45 | VP_VSYNC | ZV port |
| 16 | GPIO26 | AC97 | 46 | GND | |
| 17 | GPIO21 | ZV port | 47 | VP_CLK | ZV port |
| 18 | GND | | 48 | GND | |
| 19 | GPIO22 | ZV port | 49 | GND | |
| 20 | GND | | 50 | GPIO39 | UART |
| 21 | GPIO23 | ZV port | 51 | I2CCK | I2C |
| 22 | GND | | 52 | GND | |
| 23 | GND | | 53 | GND | |
| 24 | GPIO27 | AC97 | 54 | GPIO40 | UART |
| 25 | GPIO56 | ZV port | 55 | I2CDA | I2CD |
| 26 | GND | | 56 | GND | |
| 27 | GPIO57 | ZV port | 57 | GND | |
| 28 | GND | | 58 | GND | |
| 29 | GPIO58 | ZV port | 59 | 12V | |
| 30 | GPIO28 | AC97 | 60 | 12V | |

## 2.8. Touch Panel Connector

CN19 is a connector for interfaces for receiving the signal from LSI for touch-panel control. The inputted signal can be referred to in FPGA. Please prepare of a user about a touch-panel interface circuitry. Please refer to the clause of FPGA functional explanation about the specification of FPGA.

The appearance figure of the connector for touch-panel interfaces is shown in Fig. 2.8.1, and signal arrangement is shown in Table 2.8.1.

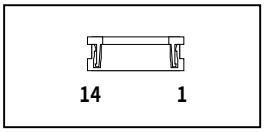



Figure 2.8.1 The connector appearance figure

Table 2.8.1 Signal arrangement of the connector (CN19)

| Pin number | Signal name | IO | Note |
|---|---|---|---|
| 1 | 3.3V | | |
| 2 | 3.3V | | |
| 3 | DCLK | O | Clock output (it can change on FPGA to 60kHz - 110kHz). |
| 4 | GND | | |
| 5 | CS# | O | Chip selection signal |
| 6 | GND | | |
| 7 | DIN | O | Write Data |
| 8 | GND | | |
| 9 | BUSY | I | Busy signal |
| 10 | GND | | |
| 11 | DOUT | I | Read Data |
| 12 | GND | | |
| 13 | IRQ# | I | Interruption |
| 14 | GND | | |

## 2.9. SH Bus Extention Connector

CN13 and CN14 are SH bus extension interface connectors. General-purpose from SH bus and FPGA for extension I/O is connected. The general-view figure of SH bus extension interface connector is shown in Fig. 2.9.1, and signal arrangement is shown in Table 2.9.1 and Table 2.9.2. A use connector is the product 52837-1679 made from Molex. Please refer to the clause of FPGA functional explanation about the specification of FPGA.

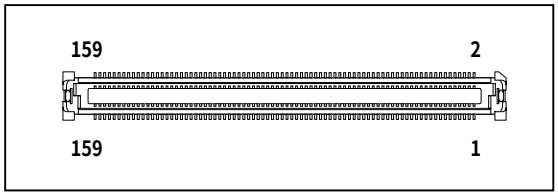



Figure 2.9.1 SH bus extension interface connector general-view figure

Table 2.9.1 Signal arrangement of SH bus extension interface connector (CN13)

| Pin number | Signal name | IO | Note |
|---|---|---|---|
| 1 | 3.3V | | |
| 2 | 3.3V | | |
| 3 | 3.3V | | |
| 4 | 3.3V | | |
| 5 | 5.0V | | |
| 6 | 5.0V | | |
| 7 | 5.0V | | |
| 8 | 5.0V | | |
| 9 | GND | | |
| 10 | GND | | |
| 11 | CKIO | O | |
| 12 | GND | | |
| 13 | GND | | |
| 14 | EXT_D0 | IO | |
| 15 | EXT_D1 | IO | |
| 16 | GND | | |
| 17 | GND | | |
| 18 | EXT_D2 | IO | |
| 19 | EXT_D3 | IO | |
| 20 | GND | | |
| 21 | GND | | |
| 22 | EXT_D4 | IO | |
| 23 | EXT_D5 | IO | |
| 24 | GND | | |
| 25 | GND | | |
| 26 | EXT_D6 | IO | |
| 27 | EXT_D7 | IO | |
| 28 | GND | | |
| 29 | GND | | |
| 30 | EXT_D8 | IO | |
| 31 | EXT_D9 | IO | |
| 32 | GND | | |
| 33 | GND | | |
| 34 | EXT_D10 | IO | |
| 35 | EXT_D11 | IO | |

| Pin number | Signal name | IO | Note |
|---|---|---|---|
| 36 | GND | | |
| 37 | GND | | |
| 38 | EXT_D12 | IO | |
| 39 | EXT_D13 | IO | |
| 40 | GND | | |
| 41 | GND | | |
| 42 | EXT_D14 | IO | |
| 43 | EXT_D15 | IO | |
| 44 | GND | | |
| 45 | GND | | |
| 46 | EXT_D16 | IO | |
| 47 | EXT_D17 | IO | |
| 48 | GND | | |
| 49 | GND | | |
| 50 | EXT_D18 | IO | |
| 51 | EXT_D19 | IO | |
| 52 | GND | | |
| 53 | GND | | |
| 54 | EXT_D20 | IO | |
| 55 | EXT_D21 | IO | |
| 56 | GND | | |
| 57 | GND | | |
| 58 | EXT_D22 | IO | |
| 59 | EXT_D23 | IO | |
| 60 | GND | | |
| 61 | GND | | |
| 62 | EXT_D24 | IO | |
| 63 | EXT_D25 | IO | |
| 64 | GND | | |
| 65 | GND | | |
| 66 | EXT_D26 | IO | |
| 67 | EXT_D27 | IO | |
| 68 | GND | | |
| 69 | GND | | |
| 70 | EXT_D28 | IO | |
| 71 | EXT_D29 | IO | |
| 72 | GND | | |
| 73 | GND | | |
| 74 | EXT_D30 | IO | |
| 75 | EXT_D31 | IO | |
| 76 | GND | | |
| 77 | GND | | |
| 78 | EXT_RST_OUT | O | The reset output to an expansive board |
| 79 | EXT_RST_IN | I | Reset input from an expansive board |
| 80 | GND | | |
| 81 | GND | | |
| 82 | GND | | |
| 83 | GND | | |
| 84 | FPGA_GPIO21 | IO | It is controlled by FPGA |
| 85 | FPGA_GPIO22 | IO | It is controlled by FPGA |

| Pin number | Signal name | IO | Note |
|---|---|---|---|
| 86 | GND | | |
| 87 | GND | | |
| 88 | FPGA_GPIO23 | IO | It is controlled by FPGA |
| 89 | FPGA_GPIO24 | IO | It is controlled by FPGA |
| 90 | GND | | |
| 91 | GND | | |
| 92 | FPGA_GPIO25 | IO | It is controlled by FPGA |
| 93 | FPGA_GPIO26 | IO | It is controlled by FPGA |
| 94 | GND | | |
| 95 | GND | | |
| 96 | FPGA_GPIO27 | IO | It is controlled by FPGA |
| 97 | FPGA_GPIO28 | IO | It is controlled by FPGA |
| 98 | GND | | |
| 99 | GND | | |
| 100 | FPGA_GPIO29 | IO | It is controlled by FPGA |
| 101 | FPGA_GPIO30 | IO | It is controlled by FPGA |
| 102 | GND | | |
| 103 | GND | | |
| 104 | FPGA_GPIO31 | IO | It is controlled by FPGA |
| 105 | FPGA_GPIO32 | IO | It is controlled by FPGA |
| 106 | GND | | |
| 107 | GND | | |
| 108 | FPGA_GPIO33 | IO | It is controlled by FPGA |
| 109 | FPGA_GPIO34 | IO | It is controlled by FPGA |
| 110 | GND | | |
| 111 | GND | | |
| 112 | FPGA_GPIO35 | IO | It is controlled by FPGA |
| 113 | FPGA_GPIO36 | IO | It is controlled by FPGA |
| 114 | GND | | |
| 115 | GND | | |
| 116 | FPGA_GPIO37 | IO | It is controlled by FPGA |
| 117 | FPGA_GPIO38 | IO | It is controlled by FPGA |
| 118 | GND | | |
| 119 | GND | | |
| 120 | FPGA_GPIO39 | IO | It is controlled by FPGA |
| 121 | FPGA_GPIO40 | IO | It is controlled by FPGA |
| 122 | GND | | |
| 123 | GND | | |
| 124 | FPGA_GPIO41 | IO | It is controlled by FPGA |
| 125 | FPGA_GPIO42 | IO | It is controlled by FPGA |
| 126 | GND | | |
| 127 | GND | | |
| 128 | FPGA_GPIO43 | IO | It is controlled by FPGA |
| 129 | FPGA_GPIO44 | IO | It is controlled by FPGA |
| 130 | GND | | |
| 131 | GND | | |
| 132 | FPGA_GPIO45 | IO | It is controlled by FPGA |
| 133 | FPGA_GPIO46 | IO | It is controlled by FPGA |
| 134 | GND | | |
| 135 | GND | | |

| Pin number | Signal name | IO | Note |
|---|---|---|---|
| 136 | FPGA_GPIO47 | IO | It is controlled by FPGA |
| 137 | FPGA_GPIO48 | IO | It is controlled by FPGA |
| 138 | GND | | |
| 139 | GND | | |
| 140 | FPGA_GPIO49 | IO | It is controlled by FPGA |
| 141 | FPGA_GPIO50 | IO | It is controlled by FPGA |
| 142 | GND | | |
| 143 | GND | | |
| 144 | FPGA_GPIO51 | IO | It is controlled by FPGA |
| 145 | FPGA_GPIO52 | IO | It is controlled by FPGA |
| 146 | GND | | |
| 147 | GND | | |
| 148 | FPGA_GPIO53 | IO | It is controlled by FPGA |
| 149 | GND | | |
| 150 | GND | | |
| 151 | GND | | |
| 152 | GND | | |
| 153 | 3.3V | | |
| 154 | 3.3V | | |
| 155 | 3.3V | | |
| 156 | 3.3V | | |
| 157 | 12V | | |
| 158 | 12V | | |
| 159 | 12V | | |
| 160 | 12V | | |

Table 2.9.2 Signal arrangement of SH bus extension interface connector (CN14)

| Pin number | Signal name | IO | Note |
|---|---|---|---|
| 1 | 3.3V | | |
| 2 | 3.3V | | |
| 3 | 3.3V | | |
| 4 | 3.3V | | |
| 5 | 5.0V | | |
| 6 | 5.0V | | |
| 7 | 5.0V | | |
| 8 | 5.0V | | |
| 9 | GND | | |
| 10 | GND | | |
| 11 | EXT_A0 | O | |
| 12 | GND | | |
| 13 | GND | | |
| 14 | EXT_A1 | O | |
| 15 | EXT_A2 | O | |
| 16 | GND | | |
| 17 | GND | | |
| 18 | EXT_A3 | O | |
| 19 | EXT_A4 | O | |
| 20 | GND | | |
| 21 | GND | | |
| 22 | EXT_A5 | O | |
| 23 | EXT_A6 | O | |
| 24 | GND | | |
| 25 | GND | | |

| Pin number | Signal name | IO | Note |
|---|---|---|---|
| 26 | EXT_A7 | O | |
| 27 | EXT_A8 | O | |
| 28 | GND | | |
| 29 | GND | | |
| 30 | EXT_A9 | O | |
| 31 | EXT_A10 | O | |
| 32 | GND | | |
| 33 | GND | | |
| 34 | EXT_A11 | O | |
| 35 | EXT_A12 | O | |
| 36 | GND | | |
| 37 | GND | | |
| 38 | EXT_A13 | O | |
| 39 | EXT_A14 | O | |
| 40 | GND | | |
| 41 | GND | | |
| 42 | EXT_A15 | O | |
| 43 | EXT_A16 | O | |
| 44 | GND | | |
| 45 | GND | | |
| 46 | EXT_A17 | O | |
| 47 | EXT_A18 | O | |
| 48 | GND | | |
| 49 | GND | | |
| 50 | EXT_A19 | O | |
| 51 | EXT_A20 | O | |
| 52 | GND | | |
| 53 | GND | | |
| 54 | EXT_A21 | O | |
| 55 | EXT_A22 | O | |
| 56 | GND | | |
| 57 | GND | | |
| 58 | EXT_A23 | O | |
| 59 | EXT_A24 | O | |
| 60 | GND | | |
| 61 | GND | | |
| 62 | EXT_A25 | O | |
| 63 | EXT_CS0# | O | |
| 64 | GND | | |
| 65 | GND | | |
| 66 | EXT_CS1# | O | |
| 67 | EXT_BS# | O | |
| 68 | GND | | |
| 69 | GND | | |
| 70 | EXT_RD# | O | |
| 71 | EXT_RD/WR# | O | |
| 72 | GND | | |
| 73 | GND | | |
| 74 | EXT_WE0# | O | |
| 75 | EXT_WE1# | O | |

| Pin number | Signal name | IO | Note |
|---|---|---|---|
| 76 | GND | | |
| 77 | GND | | |
| 78 | EXT_WE2# | O | |
| 79 | EXT_WE3# | O | |
| 80 | GND | | |
| 81 | GND | | |
| 82 | EXT_INT0 | I | Interruption from an expansive board |
| 83 | EXT_INT1 | I | Interruption from an expansive board |
| 84 | GND | | |
| 85 | GND | | |
| 86 | EXT_INT2 | I | Interruption from an expansive board |
| 87 | EXT_INT3 | I | Interruption from an expansive board |
| 88 | GND | | |
| 89 | GND | | |
| 90 | EXT_DREQ0# | I | |
| 91 | EXT_DREQ1# | I | |
| 92 | GND | | |
| 93 | GND | | |
| 94 | EXT_DRAK0 | O | |
| 95 | EXT_DRAK1 | O | |
| 96 | GND | | |
| 97 | GND | | |
| 98 | EXT_DACK0 | O | |
| 99 | EXT_DACK1 | O | |
| 100 | GND | | |
| 101 | GND | | |
| 102 | EXT_CE2A# | O | |
| 103 | EXT_CE2B# | O | |
| 104 | GND | | |
| 105 | GND | | |
| 106 | EXT_RDY# | I | |
| 107 | EXT_IOIS16 | IO | |
| 108 | GND | | |
| 109 | GND | | |
| 110 | GND | | |
| 111 | GND | | |
| 112 | FPGA_GPIO0 | IO | It is controlled by FPGA |
| 113 | FPGA_GPIO1 | IO | It is controlled by FPGA |
| 114 | GND | | |
| 115 | GND | | |
| 116 | FPGA_GPIO2 | IO | It is controlled by FPGA |
| 117 | FPGA_GPIO3 | IO | It is controlled by FPGA |
| 118 | GND | | |
| 119 | GND | | |
| 120 | FPGA_GPIO4 | IO | It is controlled by FPGA |
| 121 | FPGA_GPIO5 | IO | It is controlled by FPGA |
| 122 | GND | | |
| 123 | GND | | |
| 124 | FPGA_GPIO6 | IO | It is controlled by FPGA |
| 125 | FPGA_GPIO7 | IO | It is controlled by FPGA |

| Pin number | Signal name | IO | Note |
|---|---|---|---|
| 126 | GND | | |
| 127 | GND | | |
| 128 | FPGA_GPIO8 | IO | It is controlled by FPGA |
| 129 | FPGA_GPIO9 | IO | It is controlled by FPGA |
| 130 | GND | | |
| 131 | GND | | |
| 132 | FPGA_GPIO10 | IO | It is controlled by FPGA |
| 133 | FPGA_GPIO11 | IO | It is controlled by FPGA |
| 134 | GND | | |
| 135 | GND | | |
| 136 | FPGA_GPIO12 | IO | It is controlled by FPGA |
| 137 | FPGA_GPIO13 | IO | It is controlled by FPGA |
| 138 | GND | | |
| 139 | GND | | |
| 140 | FPGA_GPIO14 | IO | It is controlled by FPGA |
| 141 | FPGA_GPIO15 | IO | It is controlled by FPGA |
| 142 | GND | | |
| 143 | GND | | |
| 144 | FPGA_GPIO16 | IO | It is controlled by FPGA |
| 145 | FPGA_GPIO17 | IO | It is controlled by FPGA |
| 146 | GND | | |
| 147 | GND | | |
| 148 | FPGA_GPIO18 | IO | It is controlled by FPGA |
| 149 | FPGA_GPIO19 | IO | It is controlled by FPGA |
| 150 | GND | | |
| 151 | GND | | |
| 152 | FPGA_GPIO20 | IO | It is controlled by FPGA |
| 153 | 3.3V | | |
| 154 | 3.3V | | |
| 155 | 3.3V | | |
| 156 | 3.3V | | |
| 157 | 5.0V | | |
| 158 | 5.0V | | |
| 159 | 5.0V | | |
| 160 | 5.0V | | |

## 2.10. Serial Connector

CN6 is mainly used by the object for serial interface cable splicing, connecting with a console. SCIF of SH7751R is connected to Dsub9 pin connector via a RS232C driver receiver. As an exclusive clock for SCIF, a communication baud rate inputs 1.8432MHz into SH7751R, and is considering it as fixation at 115200bps. It connects with a DSUB9 pin cross cable.
Signal arrangement of a serial interface connector is shown in Table 2.10.1.

Table 2.10.1 Signal arrangement of serial-interface connector (CN6)

| Pin number | Signal name | IO | Note |
|---|---|---|---|
| 1 | NC | | |
| 2 | RD | I | Data transmission |
| 3 | TD | O | Data reception |
| 4 | DTR | | It is connection on 6 pins and a board |
| 5 | GND | | |
| 6 | DSR | | It is connection on 4 pins and a board |
| 7 | RTS | I | Request to Send |
| 8 | CTS | O | Ready for sending |
| 9 | NC | | |

## 2.11. CF Card Connector

CN9 is a connector for CF card interfaces. Timing control is performed in FPGA.
Access equivalent to the True-IDE interface timing based on CFA is possible. It corresponds to PIO mode 0-4.
Please refer to the clause of FPGA functional explanation about the specification of FPGA.

## 2.12. FROM Board Connector

CN8 is a connector for FROM board interfaces. The general-view figure of a FROM board interface connector is shown in Fig. 2.12.1, and signal arrangement is shown in Table 2.12.1. A use connector is the product 52837-1079 made from Molex.

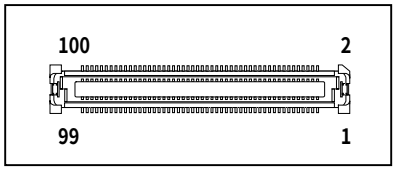



Figure 2.12.1 FROM board interface connector general view

Table 2.12.1 Signal arrangement of FROM board interface connector (CN8)

| Pin number | Signal name | IO | Note |
|---|---|---|---|
| 1 | 5.0V | | |
| 2 | 3.3V | | |
| 3 | GND | | |
| 4 | GND | | |
| 5 | D0 | IO | |
| 6 | D16 | IO | |
| 7 | D1 | IO | |
| 8 | D17 | IO | |
| 9 | D2 | IO | |
| 10 | D18 | IO | |
| 11 | D3 | IO | |
| 12 | D19 | IO | |
| 13 | D4 | IO | |
| 14 | D20 | IO | |
| 15 | D5 | IO | |
| 16 | D21 | IO | |
| 17 | D6 | IO | |
| 18 | D22 | IO | |
| 19 | D7 | IO | |
| 20 | D23 | IO | |
| 21 | D8 | IO | |
| 22 | D24 | IO | |
| 23 | D9 | IO | |
| 24 | D25 | IO | |
| 25 | 5.0V | | |
| 26 | 3.3V | | |
| 27 | GND | | |
| 28 | GND | | |
| 29 | D10 | IO | |
| 30 | D26 | IO | |
| 31 | D11 | IO | |
| 32 | D27 | IO | |
| 33 | D12 | IO | |
| 34 | D28 | IO | |
| 35 | D13 | IO | |

| Pin number | Signal name | IO | Note |
|---|---|---|---|
| 36 | D29 | IO | |
| 37 | D14 | IO | |
| 38 | D30 | IO | |
| 39 | D15 | IO | |
| 40 | D31 | IO | |
| 41 | A0 | O | |
| 42 | A13 | O | |
| 43 | A1 | O | |
| 44 | A14 | O | |
| 45 | A2 | O | |
| 46 | A15 | O | |
| 47 | A3 | O | |
| 48 | A16 | O | |
| 49 | 5.0V | | |
| 50 | 3.3V | | |
| 51 | GND | | |
| 52 | GND | | |
| 53 | A4 | O | |
| 54 | A17 | O | |
| 55 | A5 | O | |
| 56 | A18 | O | |
| 57 | A6 | O | |
| 58 | A19 | O | |
| 59 | A7 | O | |
| 60 | A20 | O | |
| 61 | A8 | O | |
| 62 | A21 | O | |
| 63 | A9 | O | |
| 64 | A22 | O | |
| 65 | A10 | O | |
| 66 | A23 | O | |
| 67 | A11 | O | |
| 68 | A24 | O | |
| 69 | A12 | O | |
| 70 | A25 | O | |
| 71 | 5.0V | | |
| 72 | 3.3V | | |
| 73 | GND | | |
| 74 | GND | | |
| 75 | WE0# | O | |
| 76 | CS0# | O | |
| 77 | WE1# | O | |
| 78 | NC | | |
| 79 | WE2# | O | |
| 80 | NC | | |
| 81 | WE3# | O | |
| 82 | NC | | |
| 83 | GND | | |
| 84 | GND | | |
| 85 | RD# | O | |

| Pin number | Signal name | IO | Note |
|---|---|---|---|
| 86 | NC | | |
| 87 | RD/WR# | O | |
| 88 | NC | | |
| 89 | NC | | 10KΩpull-up |
| 90 | BS# | O | |
| 91 | RESET# | O | |
| 92 | NC | | 10KΩpull-up |
| 93 | GND | | |
| 94 | CKIO | O | |
| 95 | 5.0V | | |
| 96 | 5.0V | | |
| 97 | 3.3V | | |
| 98 | 3.3V | | |
| 99 | GND | | |
| 100 | GND | | |

## 2.13. Real Time Clock

The real time clock module "RTC-9701JE" (made from the EPSON TOYOCOM CORPORATION) are mounted in this board as an object for time management. It has connected with the SCI interface of SH7751R. Please refer to the data of RTC-9701JE about the details of the usage.

About the battery back-up, it has realized by inserting a button battery in BT1.

When a button battery is exchanged, a diameter should use a 20mm product.

## 2.14. Serial Interface (Internal FPGA)

SCIF is mounted in FPGAof this board. The SCIF terminal is prepared by the through hole on this board. The silk of CN17 is printed. Signal arrangement is shown in Table 2.14.1. Please refer to the clause of FPGA functional explanation about the specification of FPGA.

Table 2.14.1 Signal arrangement of connector for SCIF interfaces with built-in FPGA

| Pin number | Signal name | IO | Note |
|---|---|---|---|
| 1 | 3.3V | | |
| 2 | TxD | O | Data transmission |
| 3 | RxD | I | Data reception |
| 4 | CTS | O | Ready for sending |
| 5 | RTS | I | Request to Send |
| 6 | NC | | |
| 7 | GND | | |
| 8 | GND | | |

## 2.15. Reset Signal

The reset signal connection diagram of this product is shown in Fig. 2.15.1.

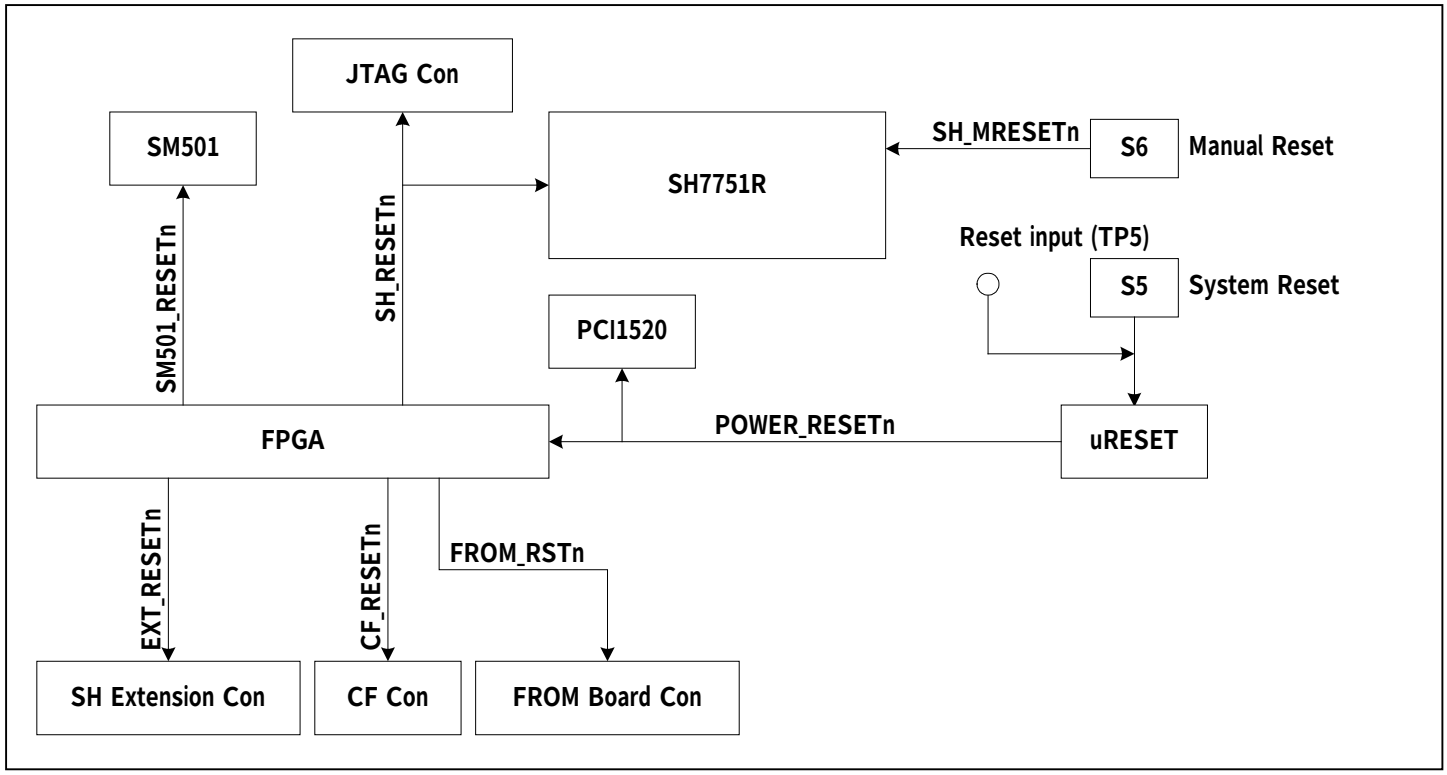



Figure 2.15.1 reset signal connection diagram

### 2.15.1. Power On Reset

A power-on reset signal is published to each device at the time of a power supply. 3.3V generated from the voltage regulator are made into criteria voltage, and when criteria voltage is less than [2.93V], a reset signal is published from Reset IC.
With this board, since the configuration of FPGA is performed at the time of a power supply, the reset signal over SH7751R is inputted after the configuration end of FPGA. Power-on reset timing is shown in Fig. 2.15.2.

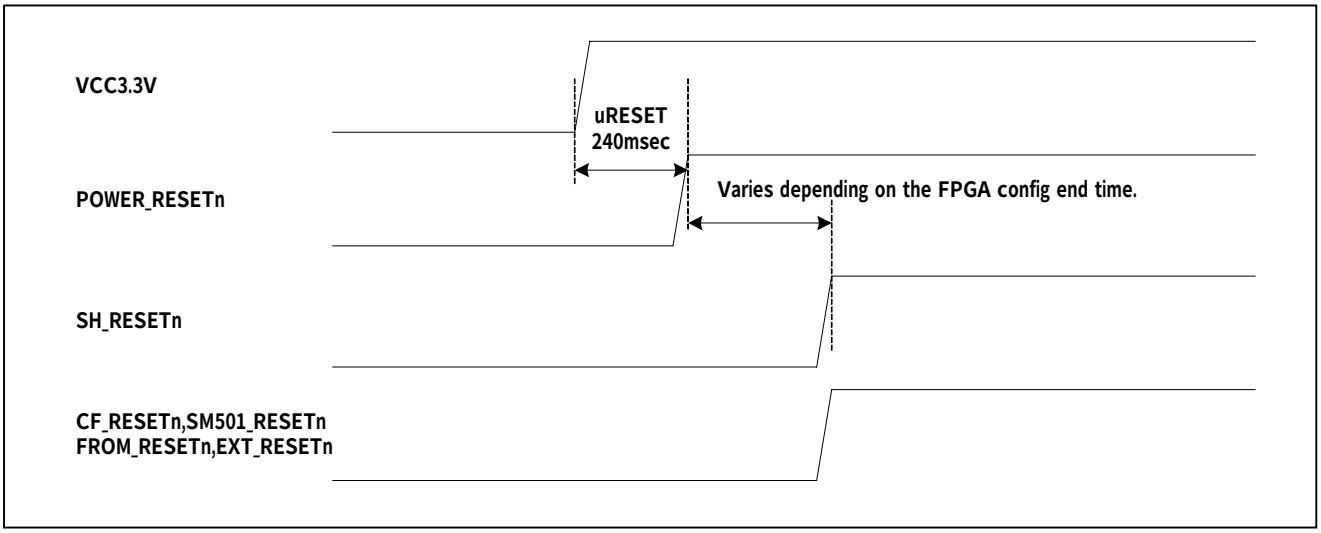



Figure 2.15.2 power-on reset timing

### 2.15.2. System Reset

This product publishes a system-reset signal under S5 swich-pushing. In a system reset, a reset pulse is published to this timing to each device. System-reset timing is shown in Fig. 2.15.3.

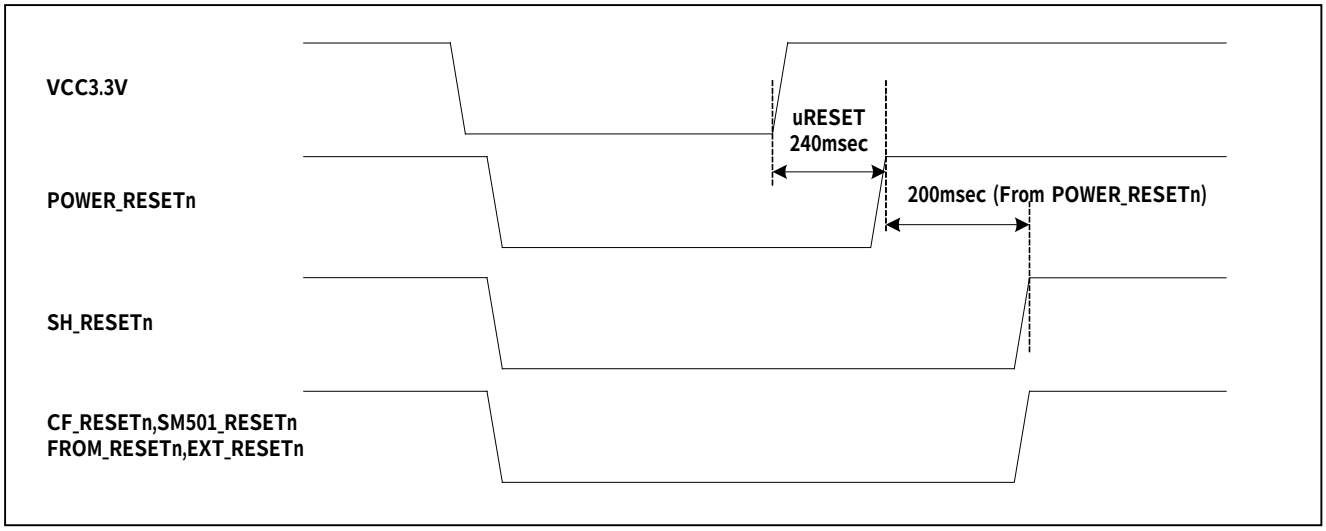



Figure 2.15.3 system-reset timing

### 2.15.3. Manual Reset

This product publishes a manual reset signal to SH7751R under S6 swich-pushing. The reset signal to other devices is not published. Manual reset timing is shown in Fig. 2.15.4.


Figure 2.15.4 system-reset timing

### 2.15.4. CF Card Reset

About the reset signal to CF card, after the power supply outputted from the power supply supply control IC(TPS2211) to CF card is stabilized, it is made the specification of which the reset to CF card is canceled. Moreover, in case the power supply from TPS2211 is intercepted, the reset signal to CF card is confirmed. CF card reset timing is shown in Fig. 2.15.5.

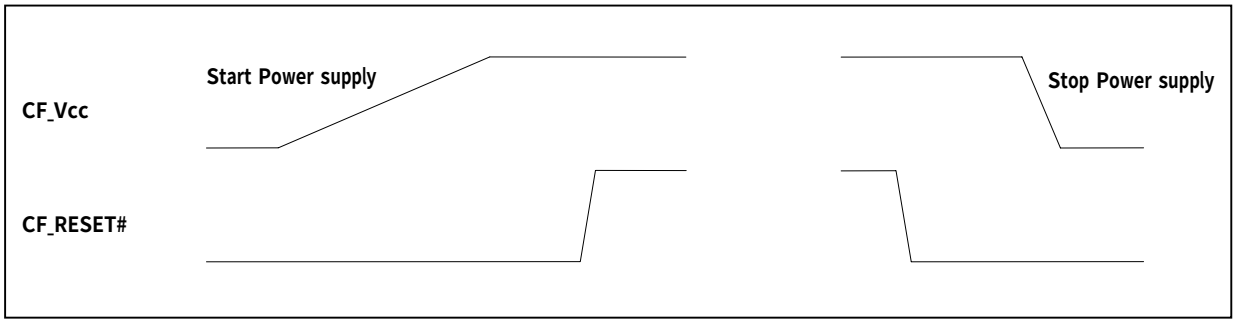



Figure 2.15.5 CF card reset timing

# 3. FPGA Logic Function Specification

## 3.1. Pin Function

For the FPGA, the EP1C4F400C8N manufactured by Altera is used. Table 3-1-1 is a list of the pin assignments. Pins dedicated to JTAG and power supply pins are omitted. The EP1C4F400C8N manual is referred to for details.

Table 3-1-1 EP1C4F400C8N Pin assignments

| Signal Name | FPGA Pin | IO | Function | Active |
|---|---|---|---|---|
| SH_CS0# | A4 | I | SH7751R Chip Select Signal 0 | L |
| SH_CS1# | A6 | I | SH7751R Chip Select Signal 1 | L |
| SH_CS2# | A7 | I | SH7751R Chip Select Signal 2 | L |
| SH_CS4# | A9 | I | SH7751R Chip Select Signal 4 | L |
| SH_CS5# | A10 | I | SH7751R Chip Select Signal 5 | L |
| SH_CS6# | B4 | I | SH7751R Chip Select Signal 6 | L |
| SH_BS# | B5 | I | SH7751R Bus Start Signal | L |
| SH_WE0# | B6 | I | SH7751R Write Enable Signal 0 | L |
| SH_WE1# | B7 | I | SH7751R Write Enable Signal 1 | L |
| SH_WE2# | B8 | I | SH7751R Write Enable Signal 2 | L |
| SH_WE3# | B9 | I | SH7751R Write Enable Signal 3 | L |
| SH_RD# | B10 | I | SH7751R Read Enable Signal | L |
| SH_RDWE# | C2 | I | SH7751R Read/Write Strobe Signal | R:H/W:L |
| SH_RDY# | C5 | O | SH7751R Ready Signal | L |
| SH_CKIO | K5 | I | SH7751R Clock Signal | - |
| SH_RESET# | T4 | O | SH7751R Power ON Reset Signal | L |
| SH_IRL0# | C7 | O | SH7751R Interrupt Signal 0 | L |
| SH_IRL1# | C8 | O | SH7751R Interrupt Signal 1 | L |
| SH_IRL2# | C9 | O | SH7751R Interrupt Signal 2 | L |
| SH_IRL3# | C10 | O | SH7751R Interrupt Signal 3 | L |
| SH_DREQ0 | D1 | O | SH7751R DMA Request Signal 0 | L |
| SH_DREQ1 | D2 | O | SH7751R DMA Request Signal 1 | L |
| SH_DACK0 | D4 | I | SH7751R DMA Acknowledge Signal 0 | H |
| SH_DACK1 | D5 | I | SH7751R DMA Acknowledge Signal 1 | H |
| SH_A[1] | D6 | I | SH7751R Address Bus | - |
| SH_A[2] | D7 | I | SH7751R Address Bus | - |
| SH_A[3] | D8 | I | SH7751R Address Bus | - |
| SH_A[4] | D9 | I | SH7751R Address Bus | - |
| SH_A[5] | D10 | I | SH7751R Address Bus | - |
| SH_A[6] | E2 | I | SH7751R Address Bus | - |
| SH_A[7] | E3 | I | SH7751R Address Bus | - |
| SH_A[8] | E4 | I | SH7751R Address Bus | - |
| SH_A[9] | E5 | I | SH7751R Address Bus | - |
| SH_A[10] | E6 | I | SH7751R Address Bus | - |
| SH_A[11] | E7 | I | SH7751R Address Bus | - |
| SH_A[12] | E8 | I | SH7751R Address Bus | - |
| SH_A[13] | E9 | I | SH7751R Address Bus | - |
| SH_A[14] | E10 | I | SH7751R Address Bus | - |
| SH_A[15] | F1 | I | SH7751R Address Bus | - |
| SH_A[16] | F2 | I | SH7751R Address Bus | - |
| SH_A[17] | F4 | I | SH7751R Address Bus | - |
| SH_A[18] | F5 | I | SH7751R Address Bus | - |
| SH_A[19] | F6 | I | SH7751R Address Bus | - |

| Signal Name | FPGA Pin | IO | Function | Active |
|---|---|---|---|---|
| SH_A[20] | F7 | I | SH7751R Address Bus | - |
| SH_A[21] | F8 | I | SH7751R Address Bus | - |
| SH_A[22] | F10 | I | SH7751R Address Bus | - |
| SH_A[23] | G1 | I | SH7751R Address Bus | - |
| SH_A[24] | G2 | I | SH7751R Address Bus | - |
| SH_A[25] | G3 | I | SH7751R Address Bus | - |
| SH_D[0] | G4 | IO | SH7751R Data Bus | - |
| SH_D[1] | G5 | IO | SH7751R Data Bus | - |
| SH_D[2] | G6 | IO | SH7751R Data Bus | - |
| SH_D[3] | G7 | IO | SH7751R Data Bus | - |
| SH_D[4] | H1 | IO | SH7751R Data Bus | - |
| SH_D[5] | H2 | IO | SH7751R Data Bus | - |
| SH_D[6] | H3 | IO | SH7751R Data Bus | - |
| SH_D[7] | H4 | IO | SH7751R Data Bus | - |
| SH_D[8] | H5 | IO | SH7751R Data Bus | - |
| SH_D[9] | H6 | IO | SH7751R Data Bus | - |
| SH_D[10] | H7 | IO | SH7751R Data Bus | - |
| SH_D[11] | J1 | IO | SH7751R Data Bus | - |
| SH_D[12] | J2 | IO | SH7751R Data Bus | - |
| SH_D[13] | J3 | IO | SH7751R Data Bus | - |
| SH_D[14] | J4 | IO | SH7751R Data Bus | - |
| SH_D[15] | J5 | IO | SH7751R Data Bus | - |
| SH_D[16] | J6 | IO | SH7751R Data Bus | - |
| SH_D[17] | J7 | IO | SH7751R Data Bus | - |
| SH_D[18] | J8 | IO | SH7751R Data Bus | - |
| SH_D[19] | M1 | IO | SH7751R Data Bus | - |
| SH_D[20] | M2 | IO | SH7751R Data Bus | - |
| SH_D[21] | M3 | IO | SH7751R Data Bus | - |
| SH_D[22] | M4 | IO | SH7751R Data Bus | - |
| SH_D[23] | M5 | IO | SH7751R Data Bus | - |
| SH_D[24] | M6 | IO | SH7751R Data Bus | - |
| SH_D[25] | M7 | IO | SH7751R Data Bus | - |
| SH_D[26] | N1 | IO | SH7751R Data Bus | - |
| SH_D[27] | N2 | IO | SH7751R Data Bus | - |
| SH_D[28] | N3 | IO | SH7751R Data Bus | - |
| SH_D[29] | N4 | IO | SH7751R Data Bus | - |
| SH_D[30] | N5 | IO | SH7751R Data Bus | - |
| SH_D[31] | N6 | IO | SH7751R Data Bus | - |
| CF_VCC5EN# | R4 | O | CF Card 5.0V Power control Signal | L |
| CF_VCC3EN# | R5 | O | CF Card 3.3V Power control Signal | L |
| CF_IORD# | R6 | O | CF Card I/O Write strobe Signal | L |
| CF_IOWR# | R7 | O | CF Card I/O Read strobe Signal | L |
| CF_CE0# | T2 | O | CF Card Chip Select Signal | L |
| CF_CE1# | T3 | O | CF Card Chip Select Signal | L |
| CF_CDINT1# | T5 | I | CF Card Card Detect Signal 1 | L |
| CF_CDINT2# | T7 | I | CF Card Card Detect Signal 2 | L |
| CF_INT | T8 | I | CF Card Interrupt Signal | L |
| CF_RDY# | T9 | I | CF Card Ready Signal | H |
| CF_RST# | T10 | O | CF Card Reset Signal | L |
| CF_DET_LED | R9 | O | CF Card Card Detect LED Signal | H |
| CF_A[0] | U1 | O | CF Card Address Bus | - |
| CF_A[1] | U2 | O | CF Card Address Bus | - |

| Signal Name | FPGA pin | IO | Function | Active |
|---|---|---|---|---|
| CF_A[2] | U3 | OO | CF Card Address Bus | - |
| CF_D[0] | V2 | IO | CF Data Bus | - |
| CF_D[1] | V3 | IO | CF Data Bus | - |
| CF_D[2] | V4 | IO | CF Data Bus | - |
| CF_D[3] | V5 | IO | CF Data Bus | - |
| CF_D[4] | V6 | IO | CF Data Bus | - |
| CF_D[5] | V7 | IO | CF Data Bus | - |
| CF_D[6] | V8 | IO | CF Data Bus | - |
| CF_D[7] | V9 | IO | CF Data Bus | - |
| CF_D[8] | V10 | IO | CF Data Bus | - |
| CF_D[9] | W3 | IO | CF Data Bus | - |
| CF_D[10] | W4 | IO | CF Data Bus | - |
| CF_D[11] | W5 | IO | CF Data Bus | - |
| CF_D[12] | W6 | IO | CF Data Bus | - |
| CF_D[13] | W7 | IO | CF Data Bus | - |
| CF_D[14] | W8 | IO | CF Data Bus | - |
| CF_D[15] | W9 | IO | CF Data Bus | - |
| PCI_INTA# | Y6 | I | PCI Interrupt Signal A | L |
| PCI_INTB# | Y7 | I | PCI Interrupt Signal B | L |
| PCI_INTC# | Y8 | I | PCI Interrupt Signal C | L |
| PCI_INTD# | Y9 | I | PCI Interrupt Signal D | L |
| PCI_PRST# | Y4 | O | PCI Reset Signal | L |
| FROM_CS#_FPGA | R1 | O | FlashROM Board Chip Select Signal | L |
| FROM_RST# | R2 | O | FlashROM Board Reset Signal | L |
| EXT_RD/WE# | C14 | O | External extension connector Read/Write Strobe Signal | R:H/W:L |
| EXT_DB_OE# | C16 | O | External extension connector Read Signal | L |
| EXT_INT0# | C17 | I | External extension connector Interrupt Signal 0 | L |
| EXT_INT1# | C18 | I | External extension connector Interrupt Signal 1 | L |
| EXT_INT2# | C19 | I | External extension connector Interrupt Signal 2 | L |
| EXT_INT3# | K15 | I | External extension connector Interrupt Signal 3 | L |
| EXT_RESET#_OUT | D11 | O | External extension connector Reset Signal | L |
| EXT_RESET#_IN | D12 | I | External extension connector Reset input Signal | L |
| SM501_RESET# | D15 | O | SM501 Reset Signal | L |
| SM501_INT# | D16 | I | SM501 Interrupt Signal | L |
| SM501_BS# | D17 | O | SM501 Bus Start Signal | L |
| SM501_CS# | D18 | O | SM501 Chip Select Signal | L |
| SM501_RDY# | E17 | I | SM501 Ready Signal | L |
| RTC_AIRQ# | F16 | I | RealTime Clock Alarm Interrupt Signal | L |
| RTC_TIRQ# | F17 | I | RealTime Clock Timer Interrupt Signal | L |
| RTC_CE | F19 | O | RealTime Clock Chip Select Signal | H |
| LOCAL_BUS_EN# | G15 | O | External extension connector Bus enable signal | L |
| EXT_DACK0 | G16 | O | External extension connector DMA Request Signal 0 | H |
| EXT_DACK1 | G17 | O | External extension connector DMA Request Signal 1 | H |
| EXT_DREQ0# | G18 | I | External extension connector DMA Acknowledge Signal 0 | L |
| EXT_DREQ1# | G19 | I | External extension connector DMA Acknowledge Signal 1 | L |
| POWER_OFF# | G20 | O | Power supply Shutdown Signal | L |
| SH_MODESET# | W14 | O | SH7751R Mode setting Signal | L |
| POWER_RESET# | F3 | I | PoweON Reset Signal | L |
| SCI_TXD | W10 | O | TXD data signal of FPGA's SCIF | - |
| SCI_RXD | W16 | I | RXD data signal of FPGA's SCIF | - |
| TP_BUSY | F12 | I | Touch-panel controller Busy Signal | H |
| TP_CS# | H18 | O | Touch-panel controller Chip Select Signal | L |

| Signal Name | FPGA pin | IO | Function | Active |
|---|---|---|---|---|
| TP_DIN | H19 | O | Touch-panel controller Data Output Signal | - |
| TP_DOUT | H20 | I | Touch-panel controller Data Input Signal | - |
| TP_DCLK | R11 | O | Touch-panel controller Clock Signal | - |
| TP_INT# | M19 | I | Touch-panel controller Interrupt Signal | H |
| LCD_BKL_OFF# | C6 | O | The back light control signal for LCD panel | L |
| SCI_RTS | V12 | | RTS signal of FPGA's SCIF for Modems | - |
| SCI_CTS | V13 | | CTS signal of FPGA's SCIF for Modems | - |
| Reserved [1] | V14 | | Reserve Signal 1 (Connected to Resistor) | - |
| Reserved [2] | V15 | | Reserve Signal 2 (Connected to Resistor) | - |
| Reserved [3] | V16 | | Reserve Signal 3 (Connected to Resistor) | - |
| Reserved [4] | V17 | | Reserve Signal 4 (Connected to Resistor) | - |
| Reserved [5] | W11 | | Reserve Signal 5 (Connected to Resistor) | - |
| Reserved [6] | W13 | | Reserve Signal 6 (Connected to Resistor) | - |
| USB_RESET# | W12 | | USB Hub controller Reset Signal | - |
| FPGA_GPIO00 | H14 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO01 | H15 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO02 | H16 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO03 | H17 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO04 | J13 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO05 | J14 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO06 | J15 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO07 | J16 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO08 | M14 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO09 | M15 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO10 | M16 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO11 | M17 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO12 | M18 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO13 | M20 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO14 | N14 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO15 | N15 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO16 | N16 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO17 | N17 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO18 | N18 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO19 | N19 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO20 | P1 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO21 | P2 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO22 | P3 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO23 | R13 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO24 | R14 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO25 | R15 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO26 | R16 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO27 | R17 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO28 | R18 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO29 | R19 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO30 | R20 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO31 | U12 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO32 | U13 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO33 | U14 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO34 | U15 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO35 | T11 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO36 | T12 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO37 | T13 | IO | FPGA General Input/Output Port | - |

| Signal Name | FPGA pin | IO | Function | Active |
|---|---|---|---|---|
| FPGA_GPIO38 | T14 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO39 | T15 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO40 | T16 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO41 | T17 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO42 | T18 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO43 | U16 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO44 | U17 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO45 | J17 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO46 | J18 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO47 | J19 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO48 | J20 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO49 | K19 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO50 | V19 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO51 | W18 | IO | FPGA General Input/Output Port | - |
| FPGA_GPIO52 | U20 | IO | FPGA General Input/Output Port | - |
| EXT_PRST# | N7 | IO | External extension Board Ditect Signal | L |
| FPGA_LED0 | A11 | O | LED control signal for debugging | H |
| FPGA_LED1 | A12 | O | LED control signal for debugging | H |
| FPGA_LED2 | A13 | O | LED control signal for debugging | H |
| FPGA_LED3 | A14 | O | LED control signal for debugging | H |
| FPGA_LED4 | A15 | O | LED control signal for debugging | H |
| FPGA_LED5 | A17 | O | LED control signal for debugging | H |
| FPGA_LED6 | B11 | O | LED control signal for debugging | H |
| FPGA_LED7 | B12 | O | LED control signal for debugging | H |
| FPGA_SW0 | B13 | I | DIP switch signal for debugging | - |
| FPGA_SW1 | B14 | I | DIP switch signal for debugging | - |
| FPGA_SW2 | B15 | I | DIP switch signal for debugging | - |
| FPGA_SW3 | B16 | I | DIP switch signal for debugging | - |
| FPGA_SW4 | B17 | I | DIP switch signal for debugging | - |
| FPGA_SW5 | B18 | I | DIP switch signal for debugging | - |
| FPGA_SW6 | C11 | I | DIP switch signal for debugging | - |
| FPGA_SW7 | C12 | I | DIP switch signal for debugging | - |
| B_SW1 | P4 | I | DIP switch signal for boot loader selection | - |
| B_SW2 | P5 | I | DIP switch signal for boot loader selection | - |
| B_SW3 | P6 | I | DIP switch signal for boot loader selection | - |

## 3.2. Register Map

A register map is shown in Table 3.2.1.

Table3-2-1 FPGA Internal Register List

| No | Register Name | Abbreviation | Bit | Initial Value | R/W | Address |
|---|---|---|---|---|---|---|
| 1 | Interrupt mask control Register | IRLMSK | 16 | H'0000 | R/W | H'0400_0000 |
| 2 | Interrupt status control Register | IRLMON | 16 | H'0000 | R/W | H'0400_0002 |
| 3 | CompactFlash timing control Register | CFCTL | 16 | H'0000 | R/W | H'0400_0004 |
| 4 | CompactFlash power-supply control Register | CFPOW | 16 | H'0000 | R/W | H'0400_0006 |
| 5 | RealTime Clock chip enable control Register | RTCCE | 16 | H'0000 | R/W | H'0400_000C |
| 6 | PCI expansion slot card detection control Register | PCICD | 16 | H'0000 | R | H'0400_000E |
| 7 | Touch-panel control Register | TP_CTL | 16 | H'0000 | R/W | H'0400_0010 |
| 8 | Touch-panel TXCLK variable control Register | TP_TXCLK | 16 | H'0000 | R/W | H'0400_0012 |
| 9 | Touch-panel control reset control Register | TP_RST | 16 | H'0000 | W | H'0400_0014 |
| 10 | Touch-panel X position data Register | TP_XRD | 16 | H'0000 | R | H'0400_0016 |
| 11 | Touch-panel Y position data Register | TP_YRD | 16 | H'0000 | R | H'0400_0018 |
| 12 | SM501 reset control Register | SM501RST | 16 | H'0000 | W | H'0400_0020 |
| 13 | CompactFlash reset control Register | CFRST | 16 | H'0000 | W | H'0400_0024 |
| 14 | Expansion Connector reset control Register | EXTRST | 16 | H'0000 | R/W | H'0400_0028 |
| 15 | CompactFlash insertion detection interrupt clear control Register | CFCDINTCLR | 16 | H'0000 | W | H'0400_002A |
| 16 | Board power OFF control Register | POWOFF | 16 | H'0000 | W | H'0400_0030 |
| 17 | FPGA version management control Register | VERREG | 16 | H'0010 | R | H'0400_0032 |
| 18 | General input port control Register | INPORT | 16 | H'00xx | R | H'0400_0034 |
| 19 | General output port control Register | OUTPORT | 16 | H'0000 | W | H'0400_0036 |
| 20 | Board version Register | BVERREG | 16 | H'0011 | R | H'0400_0038 |
| 21 | GPIO Port 0 Data Register | GPIO_DATA_0G | 16 | H'0000 | R/W | H'0400_0040 |
| 22 | GPIO Port 1 Data Register | GPIO_DATA_1G | 16 | H'0000 | R/W | H'0400_0042 |
| 23 | GPIO Port 2 Data Register | GPIO_DATA_2G | 16 | H'0000 | R/W | H'0400_0044 |
| 24 | GPIO Port 3 Data Register | GPIO_DATA_3G | 16 | H'0011 | R/W | H'0400_0046 |
| 25 | General IO Pin function Register 0 | GPIO_DIR_0G | 16 | H'0000 | R/W | H'0400_0048 |
| 26 | General IO Pin function Register 1 | GPIO_DIR_1G | 16 | H'0000 | R/W | H'0400_004A |
| 27 | General IO Pin function Register 2 | GPIO_DIR_2G | 16 | H'0000 | R/W | H'0400_004C |
| 28 | General IO Pin function Register 3 | GPIO_DIR_3G | 16 | H'0000 | R/W | H'0400_004E |
| 29 | External extension Board Status Register | EXT_PRST | 16 | H'0000 | R | H'0400_0050 |
| 30 | FlashROM board Reset control Register | FROMRST | 16 | H'0000 | W | H'0400_0052 |
| 31 | Back light control Register (for LCD Panel) | LCDPOW | 18 | H'0000 | W | H'0400_0054 |
| 32 | SCIF Serial mode control Register | SCSMR | 16 | H'0000 | R/W | H'0400_0100 |
| 33 | SCIF Bit rate Register | SCBRR | 16 | H'00FF | R/W | H'0400_0104 |
| 34 | SCIF Serial Control Register | SCSCR | 16 | H'0000 | R/W | H'0400_0108 |
| 35 | SCIF Transmit FIFO Data Register | SCFTDR | 16 | H'0000 | W | H'0400_010C |
| 36 | SCIF Status Register | SCFSR | 16 | H'0060 | R/(W) | H'0400_0110 |
| 37 | SCIF Receive FIFO Register | SCFRDR | 16 | H'0000 | R | H'0400_0114 |
| 38 | SCIF FIFO control Register | SCFCR | 16 | H'0000 | R/W | H'0400_0118 |
| 39 | SCIF FIFO Data count Register | SCFDR | 16 | H'0000 | R | H'0400_011C |
| 40 | SCIF Serial port Register | SCSPTR | 16 | H'0000 | R/W | H'0400_0120 |
| 41 | SCIF line Status Register | SCLSR | 16 | H'0000 | R/(W) | H'0400_0124 |

## 3.3. FPGA Register Specification

### 3.3.1. Interrupt mask control (IRLMSK)

This register controls the SH4 interrupt mask.

| Address: H'0400_0000, Register name: Interrupt mask control Register(IRLMSK), Initial Value: H'0000 | | | |
|---|---|---|---|
| Bit | Bit Name | R/W | Function |
| 15 | TPRDIRQ_MSK | R/W | Touch-panel interruput mask;<br>0: Interruput masked, 1: Interruput enabled |
| 14 | PCI_INTA_MSK | R/W | PCI interuput A(INTA) mask;<br>0: Interruput masked, 1: Interruput enabled |
| 13 | PCI_INTB_MSK | R/W | PCI interuput B(INTB) mask;<br>0: Interruput masked, 1: Interruput enabled |
| 12 | PCI_INTC_MSK | R/W | PCI interuput C(INTC) mask;<br>0: Interruput masked, 1: Interruput enabled |
| 11 | PCI_INTD_MSK | R/W | PCI interuput D(INTD) mask;<br>0: Interruput masked, 1: Interruput enabled |
| 10 | SM501_INT_MSK | R/W | SM501 interruput mask;<br>0: Interruput masked, 1: Interruput enabled |
| 9 | CF_INT_MSK | R/W | CF Card interruput mask;<br>0: Interruput masked, 1: Interruput enabled |
| 8 | CF_CDINT_MSK | R/W | CF Card detection interruput mask;<br>0: Interruput masked, 1: Interruput enabled |
| 7 | SCI_INT_MSK | R/W | FPGA's SCIF interruput mask;<br>0: Interruput masked, 1: Interruput enabled |
| 6 | Reserved | R | Not use |
| 5 | RTC_AIRQ_MSK | R/W | RealTime Clock alarm interrupt mask;<br>0: Interruput masked, 1: Interruput enabled |
| 4 | RTC_TIRQ_MSK | R/W | RealTime Clock timer interrupt mask;<br>0: Interruput masked, 1: Interruput enabled |
| 3 | Reserved | R | Not use |
| 2 | Reserved | R | Not use |
| 1 | Reserved | R | Not use |
| 0 | EXT_INT_MSK | R/W | External extension connector interrupt mask;<br>0: Interruput masked, 1: Interruput enabled |

### 3.3.2. Interrupt status control Register(IRLMON)

This register monitors interrupts from external devices.

| Address: H'0400_0002, Register name: Interrupt monitor register(IRLMON), Initial Value: H'0000 | | | |
|---|---|---|---|
| Bit | Bit Name | R/W | Function |
| 15 | TPRDIRQ_MON | R | Touch-panel interruput monitor;<br>0: No interrupt, 1: With interrupt |
| 14 | PCI_INTA_MON | R | PCI interuput A(INTA) monitor;<br>0: No interrupt, 1: With interrupt |
| 13 | PCI_INTB_MON | R | PCI interuput B(INTB) monitor;<br>0: No interrupt, 1: With interrupt |
| 12 | PCI_INTC_MON | R | PCI interuput C(INTC) monitor;<br>0: No interrupt, 1: With interrupt |
| 11 | PCI_INTD_MON | R | PCI interuput D(INTD) monitor;<br>0: No interrupt, 1: With interrupt |
| 10 | SM501_INT_MON | R | SM501 interruput monitor;<br>0: No interrupt, 1: With interrupt |
| 9 | CF_INT_MON | R | CF Card interruput monitor;<br>0: No interrupt, 1: With interrupt |
| 8 | CF_CDINT_MON | R | CF Card detection interruput monitor;<br>0: No interrupt, 1: With interrupt |
| 7 | SCI_INT_MON | R | FPGA's SCIF interruput monitor;<br>0: No interrupt, 1: With interrupt |
| 6 | Reserved | R | Not used |
| 5 | RTC_AIRQ_MON | R | RealTime Clock alarm interrupt monitor;<br>0: No interrupt, 1: With interrupt |
| 4 | RTC_TIRQ_MON | R | RealTime Clock timer interrupt monitor;<br>0: No interrupt, 1: With interrupt |
| 3 | EXT_INT0_MON | R | External extension connector interrupt 0 monitor;<br>0: No interrupt, 1: With interrupt |
| 2 | EXT_INT1_MON | R | External extension connector interrupt 1 monitor;<br>0: No interrupt, 1: With interrupt |
| 1 | EXT_INT2_MON | R | External extension connector interrupt 2 monitor;<br>0: No interrupt, 1: With interrupt |
| 0 | EXT_INT3_MON | R | External extension connector interrupt 3 monitor;<br>0: No interrupt, 1: With interrupt |

#### 3.3.2.1. About the kind and priority of interruption

The following interrupts are generated in the FPGA on R0P751RLC0011RL Board, with the priorities given below.

Table 3-3-1

| No. | Interrupt Type | Priority Level | | Remarks |
|---|---|---|---|---|
| 1 | PCI_INTD(Ethernet) interrupt | 15 | High | "L" level |
| 2 | CF Card interrupt | 14 | ↑ | "H" level |
| 3 | CF Card detection interruput | 13 | | "L" level |
| 4 | PCI_INEC(CardBus or PCMCIA) interruput | 12 | | "L" level |
| 5 | SM501 interruput | 11 | | "L" level |
| 6 | FPGA's SCIF interruput | 10 | | "L" level |
| 7 | RealTime Clock alarm interrupt | 9 | | "L" level |
| 8 | RealTime Clock timer interrupt | 8 | | "L" level |
| 9 | - | 7 | | - |
| 10 | PCI_INTA(other PCI Card) interrupt | 6 | | "L" level |
| 11 | PCI_INTB(Ethernet Hub) interrupt | 5 | | "L" level |
| 12 | External extension connector interrupt 0 | 4 | | "L" level |
| 13 | External extension connector interrupt 1 | | | |
| 14 | External extension connector interrupt 2 | | | |
| 15 | External extension connector interrupt 3 | | ↓ | |
| 16 | Touch-panel read request interrupt | 3 | Low | "L" level |

### 3.3.3. Compact Flash timing control Register(CFCTL)

This register controls the CompactFlash timing.

Address: H'0400_0004, Register name: Compact Flash timing control register(CFCTL), Initial Value: H'0000

| Bit | Bit Name | R/W | Function |
|---|---|---|---|
| 15 | Reserved | R | Not used |
| 14 | Reserved | R | Not used |
| 13-12 | TCLK[1:0] | R/W | Timing clock division selection;<br>b13 (TCLK1) / b12 (TCLK0) / clock<br>0 / 0 / f<br>0 / 1 / f/2<br>1 / 0 / f/4<br>1 / 1 / f/8 |
| 11 | Reserved | R | Not used |
| 10-8 | TED[2:0] | R/W | Address to IORDn/IOWRn assertion delay time selection;<br>b10 (TED2) / b9 (TED1) / b8 (TED0) / Insert wait cycles<br>0 / 0 / 0 / 1<br>0 / 0 / 1 / 2<br>0 / 1 / 0 / 3<br>0 / 1 / 1 / 6<br>1 / 0 / 0 / 9<br>1 / 0 / 1 / 12<br>1 / 1 / 0 / 15<br>1 / 1 / 1 / Don't setteing |
| 7 | Reserved | R | Not used |
| 6-4 | THE[2:0] | R/W | IORDn/IOWRn negation to address delay time selection;<br>b6 (THE2) / b5 (THE1) / b4 (THE0) / Insert wait cycles<br>0 / 0 / 0 / 1<br>0 / 0 / 1 / 2<br>0 / 1 / 0 / 3<br>0 / 1 / 1 / 6<br>1 / 0 / 0 / 9<br>1 / 0 / 1 / 12<br>1 / 1 / 0 / 15<br>1 / 1 / 1 / Don't setteing |
| 3 | Reserved | R | Not used |
| 2 | Reserved | R | Not used |
| 1 | PCW[1:0] | R/W | PCMCIA wait cycle selection;<br>b1 (PCW1) / b0 (PCW0) / Insert wait cycles<br>0 / 0 / 1<br>0 / 1 / 15<br>1 / 0 / 20<br>1 / 1 / 30 |

### 3.3.3.1. About Compact Flash card timing control

The access timing of a Compact Flash card is generated by this FPGA of R0P751RLC0011RL. The CompactFlash card is mapped in Area 5 of SH7751R.

WCR2 register bit [25:23] of the Bus State Controller (BSC) of SH7751R should be set to "1, 0, 0". In addition, please set up the Bus State Controller (BSC) of SH7751R about Area 5 with "16-bit bus width" and a "SRAM interface".

See Compact Flash card access read timing of Fig. 3-3-3-1, and the write timing of Fig. 3-3-3-2.

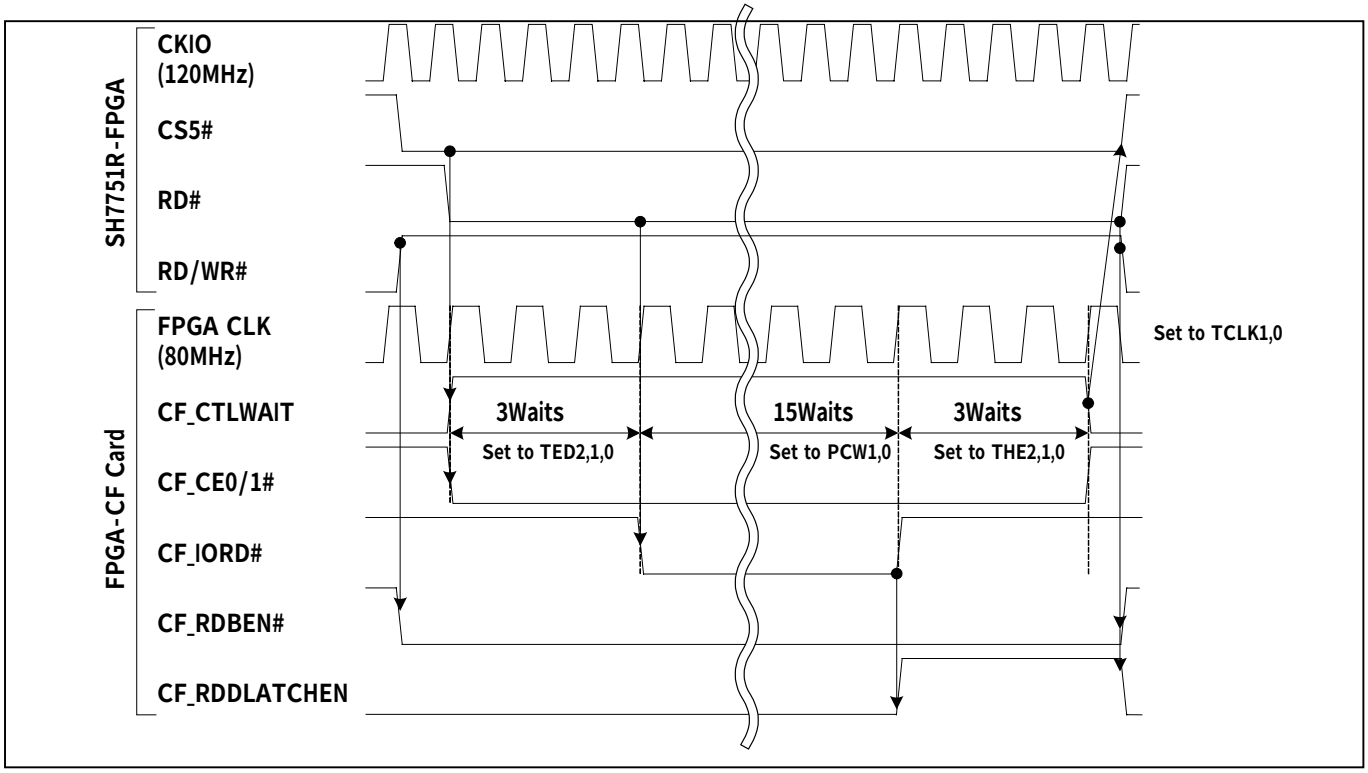



Figure 3-3-3-1 Compact Flash card Read Timing(CFCTL=H'0221：TCLK:Φ/TED:3cycles/THE:3cycles/PCW:15waits)

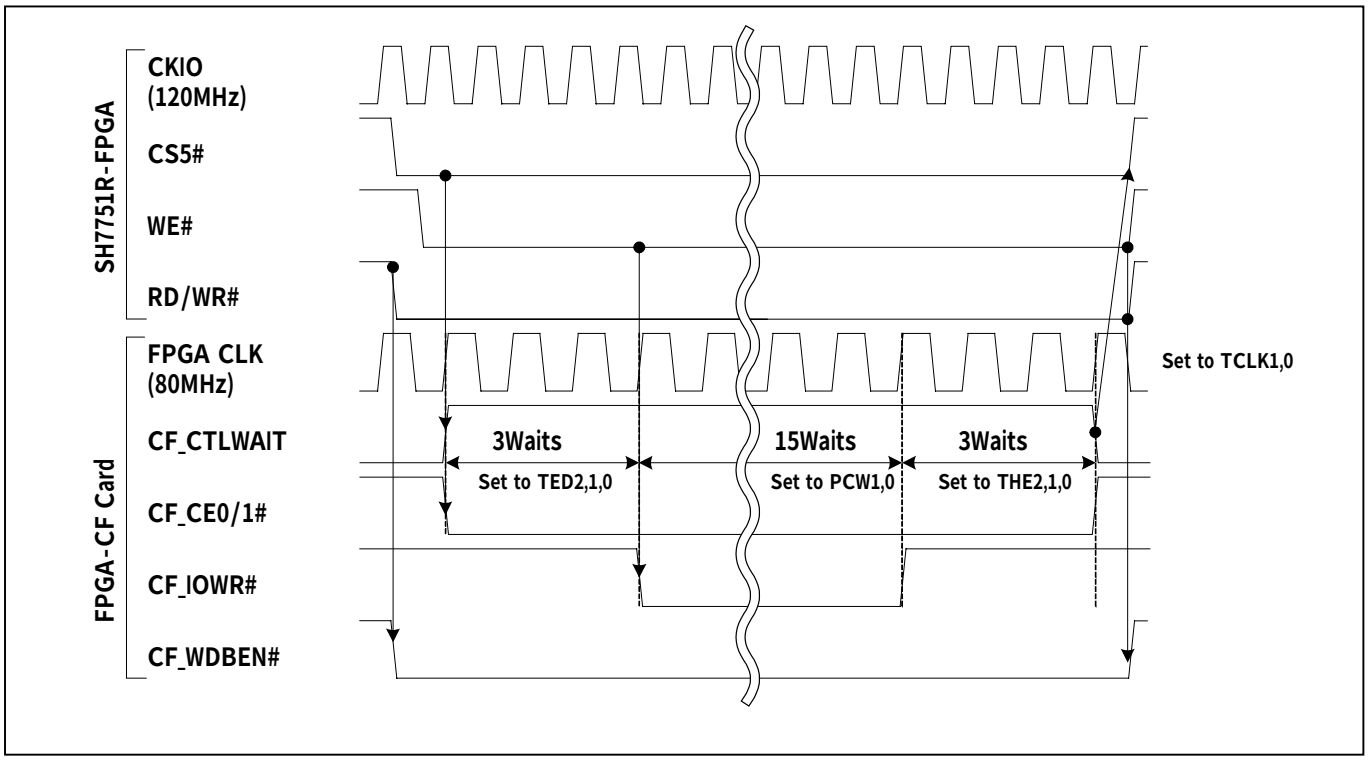



Figure 3-3-3-2 Compact Flash card Write timing(CFCTL=H'0221：TCLK:Φ/TED:3cycles/THE:3cycles/PCW:15waits)

### 3.3.4. CompactFlash card power supply control Register (CFPOW)

This register controls the power supply to the CompactFlash card.

Address: H'0400_0006, Register name: CompactFlash power supply control register(CFPOW), Initial Value: H'0000

| Bit | Bit Name | R/W | Function |
|---|---|---|---|
| 15-2 | Reserved | R | Not used |
| 1-0 | VCCEN[1:0] | R/W | Compact Flash Card power supply selection; |

| b1 | b0 | Supplied power |
|---|---|---|
| VCCEN1 | VCCEN0 | |
| 0 | 0 | 0V |
| 0 | 1 | 3.3V |
| 1 | 0 | 5.0V |
| 1 | 1 | Don't setteing |

### 3.3.5. RealTime Clock chip enable control Register (RTCCE)

This register controls the RTC-9701 chip enable.

Address: H'0400_000C, Register name: RealTime Clock chip enable control Register(RTCCE), Initial Value: H'0000

| Bit | Bit Name | R/W | Function |
|---|---|---|---|
| 15-1 | Reserved | R | Not used |
| 0 | CEEN | R/W | RealTime Clock chip enable control;<br>0: disable, 1: enable |

### 3.3.6. PCI expansion slot card detection control (PCICD)

This register detects the PCI expansion slot (CN2) card insertion.

Address: H'0400_000E, Register name: PCI expansion slot card detection control Register(PCICD), Initial Value: H'0000

| Bit | Bit Name | R/W | Function |
|---|---|---|---|
| 15-1 | Reserved | R | Not used |
| 0 | PCI_PRST1 | R | PCI expansion slot card detection;<br>0: Card not inserted, 1: Card inserted |

### 3.3.7. Touch panel control Register (TP_CTL)

This register controls the touch-panel I/F.

Address: H'0400_0010, Register name: Touch panel control Register(TP_CTL), Initial Value: H'0000

| Bit | Bit Name | R/W | Function |
|---|---|---|---|
| 15-1 | Reserved | R | Not used |
| 0 | TEN | R/W | Touch panel control block enable;<br>0: disable, 1: enable |

### 3.3.8. Touch panel TXCLK variable control Register (TP_TXCLK)

This register controls the variable transmission clock.

Address: H'0400_0012, Register name: Touch panel TXCLK variable control Register(TP_TXCLK), Initial Value: H'0000

| Bit | Bit Name | R/W | Function |
|---|---|---|---|
| 15-4 | Reserved | R | Not used |
| 3-0 | TC[3:0] | R/W | Touch panel control clock selection;<br>Variable in 5-kHz units from about 60 kHz to 110 kHz |

| b3 | b2 | b1 | b0 | TX clock |
|---|---|---|---|---|
| TC3 | TC2 | TC1 | TC0 | |
| 0 | 0 | 0 | 0 | 60KHz |
| 0 | 0 | 0 | 1 | 65KHz |
| 0 | 0 | 1 | 0 | 70KHz |
| 0 | 0 | 1 | 1 | 75KHz |
| 0 | 1 | 0 | 0 | 80KHz |
| 0 | 1 | 0 | 1 | 85KHz |
| 0 | 1 | 1 | 0 | 90KHz |
| 0 | 1 | 1 | 1 | 95KHz |
| 1 | 0 | 0 | 0 | 100KHz |
| 1 | 0 | 0 | 1 | 105KHz |
| 1 | 0 | 1 | 0 | 110KHz |

Other than above 60 kHz

### 3.3.9. Touch panel reset control Register (T_RST)

This register resets the touch-panel control register.

Address: H'0400_0014, Register name: Touch panel reset control register (T_RST), Initial Value: H'0000

| Bit | Bit Name | R/W | Function |
|---|---|---|---|
| 15-1 | Reserved | R | Not used |
| 0 | TPRST | R/W | Touch panel control block reset;<br>0: usual operation, 1: reset<br>When this bit is set to 1, a reset occurs, writing 0 to this bit is invalid |

### 3.3.10. Touch-panel X position data Register (TP_XRD)

This register controls the X position data.

| Address: H'0400_0016, Register name: Touch-panel X position data Register (T_XRD), Initial Value: H'0000 | | | |
|---|---|---|---|
| Bit | Bit Name | R/W | Function |
| 15-12 | Reserved | R | Not used |
| 11-0 | XD[11:0] | R | Touch-panel X position read data<br>Automatically cleared after reading once |

### 3.3.11. Touch-panel Y position data Register (T_YRD)

This register controls the Y position data.

| Address: H'0400_0018, Register name: Touch-panel Y position data Register (T_YRD), Initial Value: H'0000 | | | |
|---|---|---|---|
| Bit | Bit Name | R/W | Function |
| 15-12 | Reserved | R | Not used |
| 11-0 | YD[11:0] | R | Touch-panel Y position read data<br>Automatically cleared after reading once |

### 3.3.12. SM501 reset control Register (SM501RST)

This register controls reset output to the SM501.

| Address: H'0400_0020, Register name: SM501 reset control Register(SM501RST), Initial Value: H'0000 | | | |
|---|---|---|---|
| Bit | Bit Name | R/W | Function |
| 15-1 | Reserved | R | Not used |
| 0 | SM501_RST | W | Writing 1 to this bit outputs a 10-µs pulse width reset.<br>Writing 0 to this bit is invalid. |

### 3.3.13. Compact Flash card reset control Register (CFRST)

This register controls reset output to the Compact Flash card.

| Address: H'0400_0024, Register name: Compact Flash card reset control Register (CFRST), Initial Value: H'0000 | | | |
|---|---|---|---|
| Bit | Bit Name | R/W | Function |
| 15-1 | Reserved | R | Not used |
| 0 | CF_RST | W | Writing 1 to this bit outputs a 10-µs pulse width reset.<br>Writing 0 to this bit is invalid. |

### 3.3.14. Expansion connector reset control Register (EXTRST)

This register controls reset output to any external extension board.

| Address: H'0400_0028, Register name:Expansion connector reset control Register(EXTRST), Initial Value: H'0000 | | | |
|---|---|---|---|
| Bit | Bit Name | R/W | Function |
| 15-9 | Reserved | R | Not used |
| 8 | EXT_IN_ACTIVE | R/W | The Reset signal input selection bit from external extension board;<br>0: Active "Low" input, 1: Active"High" input |
| 7-5 | Reserved | R | Not used |
| 4 | EXT_OUT_ACTIVE | R/W | The Reset signal output selection bit to external extension board.<br>0: Active "Low" output, 1: Active"High" output |
| 3-1 | Reserved | R | Not used |
| 0 | EXT_OUT_RST | W | Reset signal output control to external extension board.<br>Writing 1 to this bit outputs a 10-µs pulse width reset.<br>Writing 0 to this bit is invalid. |

### 3.3.15. Compact Flash card insertion detection intrrupt clear control Register (CFCDINTCLR)

This register clears insertion detection interruption of Compact Flash card.

| Address: H'0400_002A, Register name: Compact Flash card insertion detection intrrupt clear control Register(CFCDINTCLR), Initial Value: H'0000 | | | |
|---|---|---|---|
| Bit | Bit Name | R/W | Function |
| 15-1 | Reserved | R | Not used |
| 0 | CFCLR | W | Writing 1 to this bit clears the CFCDINT interrupt, writing 0 to this bit is invalid. |

### 3.3.16. Board power off control Register (POWOFF)

This register turns off the board power supply.

| Address: H'0400_0030, Register name: Board power off control Register(POWOFF), Initial Value: H'0000 | | | |
|---|---|---|---|
| Bit | Bit Name | R/W | Function |
| 15-1 | Reserved | R | Not used |
| 0 | POW_OFF | W | Writing 1 to this bit turns off the board power supply, writing 0 to this bit is invalid. |

### 3.3.17. General input port control Register (INPORT)

This register can see the state of a Dip switch (S3).

| Address: H'0400_0034, Register name: General input port control Register(INPORT), Initial Value: H'00xx | | | |
|---|---|---|---|
| Bit | Bit Name | R/W | Function |
| 15-8 | Reserved | R | Not used |
| 7 | DIPSW7 | R | S3 Switch 8 recognition;<br>0: Off, 1: On |
| 6 | DIPSW6 | R | S3 Switch 7 recognition;<br>0: Off, 1: On |
| 5 | DIPSW5 | R | S3 Switch 6 recognition;<br>0: Off, 1: On |
| 4 | DIPSW4 | R | S3 Switch 5 recognition;<br>0: Off, 1: On |
| 3 | DIPSW3 | R | S3 Switch 4 recognition;<br>0: Off, 1: On |
| 2 | DIPSW2 | R | S3 Switch 3 recognition;<br>0: Off, 1: On |
| 1 | DIPSW1 | R | S3 Switch 2 recognition;<br>0: Off, 1: On |
| 0 | DIPSW0 | R | S3 Switch 1 recognition;<br>0: Off, 1: On |

### 3.3.18. General output port control Register (OUTPORT)

This register controls LED (LED9-LED16).

| Address: H'0400_0036, Register name: General output port control Register(OUTPORT), Initial Value: H'0000 | | | |
|---|---|---|---|
| Bit | Bit Name | R/W | Function |
| 15-8 | Reserved | R | Not used |
| 7 | LED7 | R/W | LED16 lighting control;<br>0: Off, 1: On |
| 6 | LED6 | R/W | LED15 lighting control;<br>0: Off, 1: On |
| 5 | LED5 | R/W | LED14 lighting control;<br>0: Off, 1: On |
| 4 | LED4 | R/W | LED13 lighting control;<br>0: Off, 1: On |
| 3 | LED3 | R/W | LED12 lighting control;<br>0: Off, 1: On |
| 2 | LED2 | R/W | LED11 lighting control;<br>0: Off, 1: On |
| 1 | LED1 | R/W | LED10 lighting control;<br>0: Off, 1: On |
| 0 | LED0 | R/W | LED9 lighting control;<br>0: Off, 1: On |

### 3.3.19. FPGA version Register (VERREG)

This register can see the logic version of FPGA.

| Address: H'0400_0032, Register name: Board version Register (VERREG) , Initial Value: H'0010 | | | |
|---|---|---|---|
| Bit | Bit Name | R/W | Function |
| 15-8 | Reserved | R | Not used |
| 7-4 | VER[3:0] | R | Version information |
| 3-0 | REV[3:0] | R | Revision information |

### 3.3.20. Board version Register (BVERREG)

This register can see the logic version of Board.

| Address: H'0400_0038, Register name: Board version Register (BVERREG) , Initial Value: H'0011 | | | |
|---|---|---|---|
| Bit | Bit Name | R/W | Function |
| 15-8 | Reserved | R | Not used |
| 7-4 | BVER[3:0] | R | Version information |
| 3-0 | BREV[3:0] | R | Revision information |

### 3.3.21. General Purpose I/O (GPIO)

This FPGA has three general ports (1 to 3), which provide 54 input/output pins in total. Each port pin can be inputted or outputted to an external extension connector.

Each port has a data register that stores data for the pins.

#### 3.3.21.1. GPIO Port 0 Data Register (GPIO_DATA_0G)

This register controls the general-purpose IO port linked to SH bus extension interface connector. In addition, this register is used after setting up GPIO_DIR_0G.

Address: H'0400_0040, Register name: GPIO Port 0 Data Register(GPIO_DATA_0G), Initial Value: H'0000

| Bit | Bit Name | R/W | Function |
|---|---|---|---|
| 15 | GPIO_DATA15 | R/W | These bits store output data of a pin which is used as a general output port. When the pin functions as a general output port, if the port is read, the value of this corresponding register will be read out. When the pin functions as a general input port, if the port is read, the status of the corresponding pin will be read out.<br><br>GPIO_DATA15 bit = FPGA_GPIO15 Port<br>GPIO_DATA14 bit = FPGA_GPIO14 Port<br>.<br>.<br>.<br>.<br>GPIO_DATA1 bit = FPGA_GPIO1 Port<br>GPIO_DATA0 bit = FPGA_GPIO0 Port |
| 14 | GPIO_DATA14 | R/W | |
| 13 | GPIO_DATA13 | R/W | |
| 12 | GPIO_DATA12 | R/W | |
| 11 | GPIO_DATA11 | R/W | |
| 10 | GPIO_DATA10 | R/W | |
| 9 | GPIO_DATA9 | R/W | |
| 8 | GPIO_DATA8 | R/W | |
| 7 | GPIO_DATA7 | R/W | |
| 6 | GPIO_DATA6 | R/W | |
| 5 | GPIO_DATA5 | R/W | |
| 4 | GPIO_DATA4 | R/W | |
| 3 | GPIO_DATA3 | R/W | |
| 2 | GPIO_DATA2 | R/W | |
| 1 | GPIO_DATA1 | R/W | |
| 0 | GPIO_DATA0 | R/W | |

#### 3.3.21.2. GPIO Port 1 Data Register (GPIO_DATA_1G)

This register controls the general-purpose IO port linked to SH bus extension interface connector. In addition, this register is used after setting up GPIO_DIR_1G.

Address: H'0400_0042, Register name: GPIO Port 1 Data Register(GPIO_DATA_1G), Initial Value: H'0000

| Bit | Bit Name | R/W | Function |
|---|---|---|---|
| 15 | GPIO_DATA31 | R/W | These bits store output data of a pin which is used as a general output port. When the pin functions as a general output port, if the port is read, the value of this corresponding register will be read out. When the pin functions as a general input port, if the port is read, the status of the corresponding pin will be read out.<br><br>GPIO_DATA31 bit = FPGA_GPIO31 Port<br>GPIO_DATA30 bit = FPGA_GPIO30 Port<br>.<br>.<br>.<br>.<br>GPIO_DATA17 bit = FPGA_GPIO17 Port<br>GPIO_DATA16 bit = FPGA_GPIO16 Port |
| 14 | GPIO_DATA30 | R/W | |
| 13 | GPIO_DATA29 | R/W | |
| 12 | GPIO_DATA28 | R/W | |
| 11 | GPIO_DATA27 | R/W | |
| 10 | GPIO_DATA26 | R/W | |
| 9 | GPIO_DATA25 | R/W | |
| 8 | GPIO_DATA24 | R/W | |
| 7 | GPIO_DATA23 | R/W | |
| 6 | GPIO_DATA22 | R/W | |
| 5 | GPIO_DATA21 | R/W | |
| 4 | GPIO_DATA20 | R/W | |
| 3 | GPIO_DATA19 | R/W | |
| 2 | GPIO_DATA18 | R/W | |
| 1 | GPIO_DATA17 | R/W | |
| 0 | GPIO_DATA16 | R/W | |

### 3.3.21.3. GPIO Port 2 Data Register (GPIO_DATA_2G)

This register controls the general-purpose IO port linked to SH bus extension interface connector. In addition, this register is used after setting up GPIO_DIR_2G.

| Address: H'0400_0044, Register name: GPIO Port 2 Data Register(GPIO_DATA_2G), Initial Value: H'0000 | | | |
|---|---|---|---|
| Bit | Bit Name | R/W | Function |
| 15 | GPIO_DATA47 | R/W | These bits store output data of a pin which is used as a general output port. When the pin functions as a general output port, if the port is read, the value of this corresponding register will be read out. When the pin functions as a general input port, if the port is read, the status of the corresponding pin will be read out.<br><br>GPIO_DATA47 bit = FPGA_GPIO47 Port<br>GPIO_DATA46 bit = FPGA_GPIO46 Port<br>.<br>.<br>.<br>.<br>GPIO_DATA33 bit = FPGA_GPIO33 Port<br>GPIO_DATA32 bit = FPGA_GPIO32 Port |
| 14 | GPIO_DATA46 | R/W | |
| 13 | GPIO_DATA45 | R/W | |
| 12 | GPIO_DATA44 | R/W | |
| 11 | GPIO_DATA43 | R/W | |
| 10 | GPIO_DATA42 | R/W | |
| 9 | GPIO_DATA41 | R/W | |
| 8 | GPIO_DATA40 | R/W | |
| 7 | GPIO_DATA39 | R/W | |
| 6 | GPIO_DATA38 | R/W | |
| 5 | GPIO_DATA37 | R/W | |
| 4 | GPIO_DATA36 | R/W | |
| 3 | GPIO_DATA35 | R/W | |
| 2 | GPIO_DATA34 | R/W | |
| 1 | GPIO_DATA33 | R/W | |
| 0 | GPIO_DATA32 | R/W | |

### 3.3.21.4. GPIO Port 3 Data Register (GPIO_DATA_3G)

This register controls the general-purpose IO port linked to SH bus extension interface connector. In addition, this register is used after setting up GPIO_DIR_3G.

| Address: H'0400_0046, Register name: GPIO Port 3 Data Register(GPIO_DATA_3G), Initial Value: H'0000 | | | |
|---|---|---|---|
| Bit | Bit Name | R/W | Function |
| 15-6 | Reserved | R | Not used |
| 5 | GPIO_DATA53 | R/W | These bits store output data of a pin which is used as a general output port. When the pin functions as a general output port, if the port is read, the value of this corresponding register will be read out. When the pin functions as a general input port, if the port is read, the status of the corresponding pin will be read out.<br><br>GPIO_DATA53 bit = FPGA_GPIO53 Port<br>GPIO_DATA52 bit = FPGA_GPIO52 Port<br>.<br>.<br>GPIO_DATA49 bit = FPGA_GPIO49 Port<br>GPIO_DATA48 bit = FPGA_GPIO48 Port |
| 4 | GPIO_DATA52 | R/W | |
| 3 | GPIO_DATA51 | R/W | |
| 2 | GPIO_DATA50 | R/W | |
| 1 | GPIO_DATA49 | R/W | |
| 0 | GPIO_DATA48 | R/W | |

### 3.3.21.5. GPIO Port 0 control Register (GPIO_DIR_0G)

This register controls the general-purpose IO port linked to SH bus extension interface connector.

| Address: H'0400_0048, Register name: GPIO Port 0 control Register(GPIO_DIR_0G), Initial Value: H'0000 | | | |
|---|---|---|---|
| Bit | Bit Name | R/W | Function |
| 15 | GPIO_DIR15 | R/W | A setup of FPGA_GPIO15 Port is = ;<br>0: Output, 1: Input |
| 14 | GPIO_DIR14 | R/W | A setup of FPGA_GPIO14 Port is = ;<br>0: Output, 1: Input |
| 13 | GPIO_DIR13 | R/W | A setup of FPGA_GPIO13 Port is = ;<br>0: Output, 1: Input |
| 12 | GPIO_DIR12 | R/W | A setup of FPGA_GPIO12 Port is = ;<br>0: Output, 1: Input |
| 11 | GPIO_DIR11 | R/W | A setup of FPGA_GPIO11 Port is = ;<br>0: Output, 1: Input |
| 10 | GPIO_DIR10 | R/W | A setup of FPGA_GPIO10 Port is = ;<br>0: Output, 1: Input |
| 9 | GPIO_DIR9 | R/W | A setup of FPGA_GPIO9 Port is = ;<br>0: Output, 1: Input |
| 8 | GPIO_DIR8 | R/W | A setup of FPGA_GPIO8 Port is = ;<br>0: Output, 1: Input |
| 7 | GPIO_DIR7 | R/W | A setup of FPGA_GPIO7 Port is = ;<br>0: Output, 1: Input |
| 6 | GPIO_DIR6 | R/W | A setup of FPGA_GPIO6 Port is = ;<br>0: Output, 1: Input |
| 5 | GPIO_DIR5 | R/W | A setup of FPGA_GPIO5 Port is = ;<br>0: Output, 1: Input |
| 4 | GPIO_DIR4 | R/W | A setup of FPGA_GPIO4 Port is = ;<br>0: Output, 1: Input |
| 3 | GPIO_DIR3 | R/W | A setup of FPGA_GPIO3 Port is = ;<br>0: Output, 1: Input |
| 2 | GPIO_DIR2 | R/W | A setup of FPGA_GPIO2 Port is = ;<br>0: Output, 1: Input |
| 1 | GPIO_DIR1 | R/W | A setup of FPGA_GPIO1 Port is = ;<br>0: Output, 1: Input |
| 0 | GPIO_DIR0 | R/W | A setup of FPGA_GPIO0 Port is = ;<br>0: Output, 1: Input |

### 3.3.21.6. GPIO Port 1 control Register (GPIO_DIR_1G)

This register controls the general-purpose IO port linked to SH bus extension interface connector.

| Address: H'0400_004A, Register name: GPIO Port 1 control Register(GPIO_DIR_1G), Initial Value: H'0000 | | | |
|---|---|---|---|
| Bit | Bit Name | R/W | Function |
| 15 | GPIO_DIR31 | R/W | A setup of FPGA_GPIO31 Port is = ;<br>0: Output, 1: Input |
| 14 | GPIO_DIR30 | R/W | A setup of FPGA_GPIO30 Port is = ;<br>0: Output, 1: Input |
| 13 | GPIO_DIR29 | R/W | A setup of FPGA_GPIO29 Port is = ;<br>0: Output, 1: Input |
| 12 | GPIO_DIR28 | R/W | A setup of FPGA_GPIO28 Port is = ;<br>0: Output, 1: Input |
| 11 | GPIO_DIR27 | R/W | A setup of FPGA_GPIO27 Port is = ;<br>0: Output, 1: Input |
| 10 | GPIO_DIR26 | R/W | A setup of FPGA_GPIO26 Port is = ;<br>0: Output, 1: Input |
| 9 | GPIO_DIR25 | R/W | A setup of FPGA_GPIO25 Port is = ;<br>0: Output, 1: Input |
| 8 | GPIO_DIR24 | R/W | A setup of FPGA_GPIO24 Port is = ;<br>0: Output, 1: Input |
| 7 | GPIO_DIR23 | R/W | A setup of FPGA_GPIO23 Port is = ;<br>0: Output, 1: Input |
| 6 | GPIO_DIR22 | R/W | A setup of FPGA_GPIO22 Port is = ;<br>0: Output, 1: Input |
| 5 | GPIO_DIR21 | R/W | A setup of FPGA_GPIO21 Port is = ;<br>0: Output, 1: Input |
| 4 | GPIO_DIR20 | R/W | A setup of FPGA_GPIO20 Port is = ;<br>0: Output, 1: Input |
| 3 | GPIO_DIR19 | R/W | A setup of FPGA_GPIO19 Port is = ;<br>0: Output, 1: Input |
| 2 | GPIO_DIR18 | R/W | A setup of FPGA_GPIO18 Port is = ;<br>0: Output, 1: Input |
| 1 | GPIO_DIR17 | R/W | A setup of FPGA_GPIO17 Port is = ;<br>0: Output, 1: Input |
| 0 | GPIO_DIR16 | R/W | A setup of FPGA_GPIO16 Port is = ;<br>0: Output, 1: Input |

### 3.3.21.7. GPIO Port 2 control Register (GPIO_DIR_2G)

This register controls the general-purpose IO port linked to SH bus extension interface connector.

| Address: H'0400_004C, Register name: GPIO Port 2 control Register(GPIO_DIR_2G), Initial Value: H'0000 | | | |
|---|---|---|---|
| Bit | Bit Name | R/W | Function |
| 15 | GPIO_DIR47 | R/W | A setup of FPGA_GPIO47 Port is = ;<br>0: Output, 1: Input |
| 14 | GPIO_DIR46 | R/W | A setup of FPGA_GPIO46 Port is = ;<br>0: Output, 1: Input |
| 13 | GPIO_DIR45 | R/W | A setup of FPGA_GPIO45 Port is = ;<br>0: Output, 1: Input |
| 12 | GPIO_DIR44 | R/W | A setup of FPGA_GPIO44 Port is = ;<br>0: Output, 1: Input |
| 11 | GPIO_DIR43 | R/W | A setup of FPGA_GPIO43 Port is = ;<br>0: Output, 1: Input |
| 10 | GPIO_DIR42 | R/W | A setup of FPGA_GPIO42 Port is = ;<br>0: Output, 1: Input |
| 9 | GPIO_DIR41 | R/W | A setup of FPGA_GPIO41 Port is = ;<br>0: Output, 1: Input |
| 8 | GPIO_DIR40 | R/W | A setup of FPGA_GPIO40 Port is = ;<br>0: Output, 1: Input |
| 7 | GPIO_DIR39 | R/W | A setup of FPGA_GPIO39 Port is = ;<br>0: Output, 1: Input |
| 6 | GPIO_DIR38 | R/W | A setup of FPGA_GPIO38 Port is = ;<br>0: Output, 1: Input |
| 5 | GPIO_DIR37 | R/W | A setup of FPGA_GPIO37 Port is = ;<br>0: Output, 1: Input |
| 4 | GPIO_DIR36 | R/W | A setup of FPGA_GPIO36 Port is = ;<br>0: Output, 1: Input |
| 3 | GPIO_DIR35 | R/W | A setup of FPGA_GPIO35 Port is = ;<br>0: Output, 1: Input |
| 2 | GPIO_DIR34 | R/W | A setup of FPGA_GPIO34 Port is = ;<br>0: Output, 1: Input |
| 1 | GPIO_DIR33 | R/W | A setup of FPGA_GPIO33 Port is = ;<br>0: Output, 1: Input |
| 0 | GPIO_DIR32 | R/W | A setup of FPGA_GPIO32 Port is = ;<br>0: Output, 1: Input |

### 3.3.21.8. GPIO Port 3 control Register (GPIO_DIR_3G )

This register controls the general-purpose IO port linked to SH bus extension interface connector.

| Address: H'0400_004E, Register name: GPIO Port 3 control Register(GPIO_DIR_3G), Initial Value: H'0000 | | | |
|---|---|---|---|
| Bit | Bit Name | R/W | Function |
| 15-6 | Reserved | R | Not used |
| 5 | GPIO_DIR53 | R/W | A setup of FPGA_GPIO53 Port is = ;<br>0: Output, 1: Input |
| 4 | GPIO_DIR52 | R/W | A setup of FPGA_GPIO52 Port is = ;<br>0: Output, 1: Input |
| 3 | GPIO_DIR51 | R/W | A setup of FPGA_GPIO51 Port is = ;<br>0: Output, 1: Input |
| 2 | GPIO_DIR50 | R/W | A setup of FPGA_GPIO50 Port is = ;<br>0: Output, 1: Input |
| 1 | GPIO_DIR49 | R/W | A setup of FPGA_GPIO49 Port is = ;<br>0: Output, 1: Input |
| 0 | GPIO_DIR48 | R/W | A setup of FPGA_GPIO48 Port is = ;<br>0: Output, 1: Input |

### 3.3.22. External extension Board status Register (EXT_PRST)

This register can see the state of an external extension board. Low level of the EXT_PRST port of FPGA is detected.

| Address: H'0400_0050, Register name: External extension Board status Register(EXT_PRST), Initial Value: H'000x | | | |
|---|---|---|---|
| Bit | Bit Name | R/W | Function |
| 15-1 | Reserved | R | Not used |
| 0 | EXT_PRSTN | R | 0: No board detection , 1: Board detection |

### 3.3.23. FlashROM Board Reset control Register (FROMRST)

This register controls reset to a FlashROM board.

| Address: H'0400_0052, Register name: FlashROM Board reset control Register(FROMRST), Initial Value: H'0000 | | | |
|---|---|---|---|
| Bit | Bit Name | R/W | Function |
| 15-1 | Reserved | R | Not used |
| 0 | FROM_RST | W | Writing 1 to this bit outputs a 10-µs pulse width reset. Writing 0 to this bit is invalid. |

### 3.3.24. Back light control Register for LCD (LCDPOW)

This register controls the power supply supply to the back light for LCD.

| Address: H'0400_0054, Register name: control Register,<br>Initial Value: H'0000 | | | |
|---|---|---|---|
| Bit | Bit Name | R/W | Function |
| 15-1 | Reserved | R | Not used |
| 0 | LCD_EN | R/W | 0: LCD Power on, 1: LCD Power off |

### 3.3.25. Serial communication interface with FIFO (SCIF)

This FPGA is equipped with a 1-channel serial communication interface with built-in FIFO buffers (Serial Communication Interface with FIFO: SCIF). The SCIF can perform both asynchronous serial communications.

16-stage FIFO buffers are provided for both transmission and reception, enabling fast, efficient, and continuous communication.

The SCIF has modem control functions (RTS, CTS).

#### 3.3.25.1. SCIF Serial mode control Register (SCSMR)

SCSMR is a 16-bit register used to set the SCIF's serial transfer format and select the baud rate generator clock source.

Address: H'0400_0100, Register name: Serial mode control Register(SCSMR), Initial Value: H'0000

| Bit | Bit Name | R/W | Function |
|---|---|---|---|
| 15-7 | Reserved | R | Not used |
| 6 | CHR | R/W | Character Length<br>0: 8-bit data, 1: 7-bit data |
| 5 | PE | R/W | Parity Enable<br>0: Parity bit addition and checking disabled<br>1: Parity bit addition and checking enabled |
| 4 | O_En | R/W | Parity Mode<br>0: Even parity, 1: Odd parity |
| 3 | STOP | R/W | Stop Bit Length<br>0: 1 stop bit, 1: 2 stop bits |
| 2 | Reserved | R | Not used |
| 1-0 | CKS[1:0] | R/W | Clock Select 1 and 0 |

| b1 | b0 | clock |
|---|---|---|
| CKS1 | CKS0 | |
| 0 | 0 | Pck |
| 0 | 1 | Pck/4 |
| 1 | 0 | Pck/16 |
| 1 | 1 | Pck/64 |

### 3.3.25.2. SCIF Bit Rate Register (SCBRR)

SCBRR is a register that set the serial transmission/reception bit rate in accordance with the baud rate generator operating clock selected by bits CKS1 and CKS0 in SCSMR.

| Address: H'0400_0104, Register name: SCIF Bit Rate Register(SCBRR), Initial Value: H'00FF | | | |
|---|---|---|---|
| Bit | Bit Name | R/W | Function |
| 15-8 | Reserved | R | Not used |
| 7-0 | N[7:0] | R/W | Please see the calculation method of following SCBRR. |

The SCBRR setting is found from the following equation.

$$N = \frac{Pck}{64 \times 2^{2n-1} \times B} \times 10^6 - 1$$

B : Bit rate (bits/s)
N : SCBRR setting for baud rate generator (0 < N <255)
Pck : operating frequency (MHz)
n : Baud rate generator input clock (n = 0 to 3)
(The relation between n and a clock should look at the following table.)

| n | clock | SCSMR setting | |
|---|---|---|---|
| | | CKS1 | CKS0 |
| 0 | Pck | 0 | 0 |
| 1 | Pck/4 | 0 | 1 |
| 2 | Pck/16 | 1 | 0 |
| 3 | Pck/64 | 1 | 1 |

The bit rate error in asynchronous mode is found from the following equation:

$$\text{Error (\%)} = \left\{ \frac{Pck \times 10^6}{(N+1) \times B \times 64 \times 2^{2n-1}} - 1 \right\} \times 100$$

### 3.3.25.3. SCIF Serial Control Register (SCSCR)

SCSCR is a register used to enable/disable transmission/reception by SCIF, serial clock output, interrupt requests, and to select transmission/reception clock source for the SCIF.

Address: H'0400_0108, Register name: SCIF Serial Control Register (SCSCR),
Initial Value: H'0000

| Bit | Bit Name | R/W | Function |
|---|---|---|---|
| 15-6 | Reserved | R | Not used |
| 7 | TIE | R/W | Transmit Interrupt Enable<br>0: Transmit-FIFO-data-empty interrupt (TXI) request disabled<br>1: Transmit-FIFO-data-empty interrupt (TXI) request enabled |
| 6 | RIE | R/W | Receive Interrupt Enable<br>0: Receive-data-full interrupt (RXI) request, receiveerror interrupt (ERI) request, and break interrupt (BRI) request disabled<br>1: Receive-data-full interrupt (RXI) request, receiveerror interrupt (ERI) request, and break interrupt (BRI) request enabled |
| 5 | TE | R/W | Transmit Enable<br>0: Transmission disabled<br>1: Transmission enabled |
| 4 | RE | R/W | Receive Error Interrupt Enable<br>0: Receive-error interrupt (ERI) and break interrupt (BRI) requests disabled<br>1: Receive-error interrupt (ERI) and break interrupt (BRI) requests enabled |
| 3 | REIE | R/W | Receive Error Interrupt Enable<br>0: Receive-error interrupt (ERI) and break interrupt (BRI) requests disabled<br>1: Receive-error interrupt (ERI) and break interrupt (BRI) requests enabled<br>(RIE bit (b6) = effective in the case of 0) |
| 2 | Reserved | R | Not used |
| 1-0 | CKE[1:0] | R/W | Clock Enable 1, 0 select |

| b1 | b0 | Function of SCK pin |
|---|---|---|
| CKE1 | CKE0 | |
| 0 | 0 | input port |
| 0 | 1 | clock output |
| 1 | 0 | 1.8432MHz |
| 1 | 1 | external clock |

### 3.3.25.4. SCIF Transmit FIFO Data Register (SCFTDR)

SCFTDR is an FIFO register of 16 stages that stores data for serial transmission.

If SCTSR is empty when transmit data has been written to SCFTDR, the SCIF transfers the transmit data written in SCFTDR to SCTSR and starts serial transmission.

The next data cannot be written when SCFTDR is filled with 16 bytes of transmit data. Data written in this case is ignored.

Address: H'0400_010C, Register name: SCIF Transmit FIFO Data Register (SCFTDR),
Initial Value: H'0000

| Bit | Bit Name | R/W | Function |
|---|---|---|---|
| 15-8 | Reserved | R | Not used |
| 7-0 | TD[7:0] | W | Transmit data |

### 3.3.25.5. SCIF Status Register (SCFSR)

SCFSR is a register that consists of status flags that indicate the operating status of the SCIF

| Address: H'0400_0110, Register name: SCIF Status Register (SCFSR), Initial Value: H'0060 | | | |
|---|---|---|---|
| Bit | Bit Name | R/W | Function |
| 15-12 | PER[3:0] | R | Number of Parity Errors<br>These bits indicate the number of data bytes in which a parity error occurred in the receive data stored in SCFRDR.<br>After the ER bit in SCFSR is set, the value indicated by bits PER3 to PER0 is the number of data bytes in which a parity error occurred.<br>If all 16 bytes of receive data in SCFRDR have parity errors, the value indicated by bits PER3 to PER0 will be 0. |
| 11-8 | FER[3:0] | R | Number of Framing Errors<br>These bits indicate the number of data bytes in which a framing error occurred in the receive data stored in SCFRDR.<br>After the ER bit in SCFSR is set, the value indicated by bits FER3 to FER0 is the number of data bytes in which a framing error occurred.<br>If all 16 bytes of receive data in SCFRDR have framing errors, the value indicated by bits FER3 to FER0 will be 0. |
| 7 | ER | R/(W) | Receive Error<br>0: No framing error or parity error occurred during reception<br>[Clearing conditions]<br>• When 0 is written to ER after reading ER = 1<br>1: A framing error or parity error occurred during reception |
| 6 | TEND | R/(W) | Transmit End<br>0: Transmission is in progress<br>[Clearing conditions]<br>• When transmit data is written to SCFTDR, and 0 is written to TEND after reading TEND = 1<br>1: Transmission has been ended |
| 5 | TDFE | R/(W) | Transmit FIFO Data Empty<br>0: A number of transmit data bytes exceeding the transmit trigger set number have been written to SCFTDR<br>[Clearing conditions]<br>• When transmit data exceeding the transmit trigger set number is written to SCFTDR after reading TDFE = 1, and 0 is written to TDFE<br>• When transmit data exceeding the transmit trigger set number is written to SCFTDR by the DMAC<br>1: The number of transmit data bytes in SCFTDR does not exceed the transmit trigger set number (Initial value) |
| 4 | BRK | R/(W) | Break Detect<br>0: A break signal has not been received<br>[Clearing conditions]<br>• When 0 is written to BRK after reading BRK = 1<br>1: A break signal has been received |

| | | | |
|---|---|---|---|
| 3 | FER | R | Framing Error<br>0: There is no framing error that is to be read from SCFRDR<br>[Clearing conditions]<br>• When there is no framing error in the data that is to be read next from SCFRDR<br>1: There is a framing error that is to be read from SCFRDR |
| 2 | PER | R | Parity Error<br>0: There is no parity error that is to be read from SCFRDR<br>[Clearing conditions]<br>• When there is no parity error in the data that is to be read next from SCFRDR<br>1: There is a parity error in the receive data that is to be read from SCFRDR |
| 1 | RDF | R/(W) | Receive FIFO Data Full<br>0: The number of receive data bytes in SCFRDR is less than the receive trigger set number<br>[Clearing conditions]<br>• When SCFRDR is read until the number of receive data bytes in SCFRDR falls below the receive trigger set number after reading RDF = 1, and 0 is written to RDF<br>1: The number of receive data bytes in SCFRDR is equal to or greater than the receive trigger set number<br>[Setting condition]<br>• When SCFRDR contains at least the receive trigger set number of receive data bytes |
| 0 | DR | R/(W) | Receive Data Ready<br>0: Reception is in progress or has ended normally and there is no receive data left in SCFRDR<br>[Clearing conditions]<br>• When all the receive data in SCFRDR has been read after reading DR = 1, and 0 is written to DR<br>1: No further receive data has arrived<br>[Setting condition]<br>• When SCFRDR contains fewer than the receive trigger set number of receive data bytes, and no further data has arrived for at least 15 etu after the stop bit of the last data received |

### 3.3.25.6. About interruption of the SCIF block with built-in FPGA

The interruption logic diagram of the SCIF block with built-in FPGA is shown in Fig. 3-3-36-1. The register bit of SCIF block interruption origin with built-in FPGA is shown in Table 3-3-36-1.

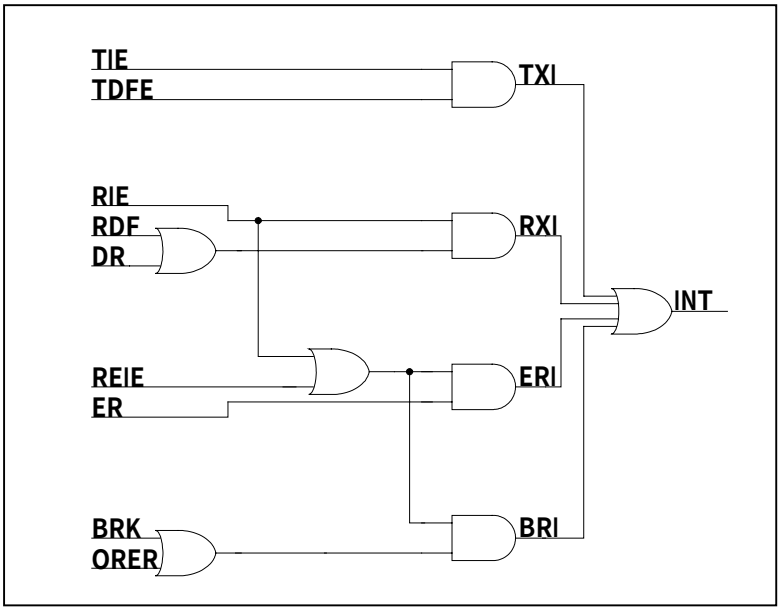



Fig. 3-3-36-1 The interruption logic diagram of the SCIF block with built-in FPGA

Table 3-3-36-1 The register bit of SCIF block interruption origin with built-in FPGA

| Signal (Bit) name | Contents |
|---|---|
| TIE | Transmit FIFO Data Empty interrupt |
| RIE | Receive-data-full interrupt (RXI), Receive-error interrupt (ERI), Break interrupt (BRI) |
| REIE | Receive-error interrupt (ERI), Break interrupt (BRI) |
| TDFE | Transmit FIFO data status |
| RDF | Receive FIFO data status |
| DR | Receive data ready |
| ER | Receive-data error |
| BRK | Receive-data break |
| ORER | Overrun error |

### 3.3.25.7. SCIF Receive FIFO Data Register (SCFRDR)

SCFRDR is a FIFO register of 16 stages that stores received serial data.

When the SCIF has received one byte of serial data, it transfers the received data from SCRSR to SCFRDR where it is stored, and completes the receive operation. SCRSR is then enabled for reception, and consecutive receive operations can be erformed until SCFRDR is full (16 databytes).

| Address: H'0400_0114, Register name: SCIF Receive FIFO Data Register (SCFRDR), Initial Value: H'0000 | | | |
|---|---|---|---|
| Bit | Bit Name | R/W | Function |
| 15-8 | Reserved | R | Not used |
| 7-0 | RD[7:0] | R | Receive data |

### 3.3.25.8. SCIF FIFO Control Register (SCFCR)

SCFCR performs data count resetting and trigger data number setting for transmit and receive FIFO registers, and also contains a loopback test enable bit.

<table>
<tr><td colspan="4">Address: H'0400_0118, Register name: SCIF FIFO Control Register (SCFCR), Initial Value: H'0060</td></tr>
<tr><td>Bit</td><td>Bit Name</td><td>R/W</td><td>Function</td></tr>
<tr><td>15-11</td><td>Reserved</td><td>R</td><td>Not used</td></tr>
<tr><td>10-8</td><td>RSTRG[2:0]</td><td>R/W</td><td>SCIF_RTS Output Active Trigger<br>The SCIF_RTS signal becomes high when the number of receive data stored in SCFRDR exceeds the trigger number shown below.
<table>
<tr><td>b10</td><td>b9</td><td>b8</td><td rowspan="2">RTS output trigger</td></tr>
<tr><td>RSTRG2</td><td>RSTRG1</td><td>RSTRG0</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>15</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>4</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>6</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>8</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>10</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>12</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>14</td></tr>
</table></td></tr>
<tr><td>7-6</td><td>RTRG[1:0]</td><td>R/W</td><td>Receive FIFO Data Number Trigger<br>These bits are used to set the number of receive data bytes that sets the RDF flag in SCFSR.
<table>
<tr><td>b7</td><td>b6</td><td rowspan="2">The number of receive triggers</td></tr>
<tr><td>RTRG1</td><td>RTRG0</td></tr>
<tr><td>0</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>4</td></tr>
<tr><td>1</td><td>0</td><td>8</td></tr>
<tr><td>1</td><td>1</td><td>14</td></tr>
</table></td></tr>
</table>

<table>
<tr><td>5-4</td><td>TTRG[1:0]</td><td>R/W</td><td>Transmit FIFO Data Number Trigger<br>These bits are used to set the number of remaining transmit data bytes that sets the TDFE flag in SCFSR.<br><table><tr><td>b5<br>TTRG1</td><td>b4<br>TTRG0</td><td>The number of transmit triggers</td></tr><tr><td>0</td><td>0</td><td>8</td></tr><tr><td>0</td><td>1</td><td>4</td></tr><tr><td>1</td><td>0</td><td>2</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table></td></tr>
<tr><td>3</td><td>MCE</td><td>R/W</td><td>Modem Control Enable<br>Enables the SCIF_CTS and SCIF_RTS modem control signals.<br>0: Modem signals disabled<br>1: Modem signals enabled</td></tr>
<tr><td>2</td><td>TFRST</td><td>R/W</td><td>Transmit FIFO Data Register Reset<br>0: Reset operation disabled<br>1: Reset operation enabled</td></tr>
<tr><td>1</td><td>RFRST</td><td>R/W</td><td>Receive FIFO Data Register Reset<br>0: Reset operation disabled<br>1: Reset operation enabled</td></tr>
<tr><td>0</td><td>LOOP</td><td>R/W</td><td>Loopback Test<br>Internally connects the transmit output pin (TXD) and receive input pin (RXD), and the RTS pin and CTS pin, enabling loopback testing.<br>0: Loopback test disabled<br>1: Loopback test enabled</td></tr>
</table>

### 3.3.25.9. SCIF FIFO Data Count Register (SCFDR)

SCFDR is a register that indicates the number of transmit/ receive data bytes stored in SCFTDR.

| Address: H'0400_011C, Register name: SCIF FIFO Data Count Register (SCFDR), Initial Value: H'0000 | | | |
|---|---|---|---|
| Bit | Bit Name | R/W | Function |
| 15-13 | Reserved | R | Not used |
| 12-8 | T[4:0] | R | These bits show the number of untransmitted data bytes in SCFDR.<br>A value of H'00 indicates that there is no transmit data, and a value of H'10 indicates that SCFDR is full of transmit data. |
| 7-5 | Reserved | R | Not used |
| 4-0 | R[4:0] | R | These bits show the number of receive data bytes in SCFDR.<br>A value of H'00 indicates that there is no receive data, and a value of H'10 indicates that SCFDR is full of receive data. |

### 3.3.25.10. SCIF Serial Port Register (SCSPTR)

SCSPTR is a readable/writable register that controls input/output and data for the port pins multiplexed with the serial communication interface (SCIF) pins at all times. Input data can be read from the RXD pin, output data written to the TXD pin, and breaks in serial transmission/reception controlled, by means of bits 1 and 0.

- The RTS and CTS pin becomes effective when the MCE bit of SCFCR is "0".
- The SCK pin becomes effective when the CKE1 and CKE0 bit of SCSCR are "00".
- The TxD pin becomes effective when the TE bit of SCSCR is "0".

| Address: H'0400_0120, Register name: SCIF Serial Port Register (SCSPTR), Initial Value: H'0060 | | | |
|---|---|---|---|
| Bit | Bit Name | R/W | Function |
| 15-8 | Reserved | R | Not used |
| 7 | RTSIO | R/W | Serial Port RTS Port Input/Output<br>0: RTSDT bit value is not output to RTS pin<br>1: RTSDT bit value is output to RTS pin |
| 6 | RTSDT | R/W | Serial Port RTS Port Data<br>0: Input/output data is low-level<br>1: Input/output data is high-level |
| 5 | CTSIO | R/W | Serial Port CTS Port Input/Output<br>0: CTSDT bit value is not output to CTS pin<br>1: CTSDT bit value is output to CTS pin |
| 4 | CTSDT | R/W | Serial Port CTS Port Data<br>0: Input/output data is low-level<br>1: Input/output data is high-level |
| 3 | SCKIO | R/W | Serial Port Clock Port Input/Output<br>0: SCKDT bit value is not output to SCK pin<br>1: SCKDT bit value is output to SCK pin |
| 2 | SCKDT | R/W | Serial Port Clock Port Data<br>0: Input/output data is low-level<br>1: Input/output data is high-level |
| 1 | SPB2IO | R/W | Serial Port Break Input/Output<br>0: SPB2DT bit value is not output to the TXD pin<br>1: SPB2DT bit value is output to the TXD pin |
| 0 | SPB2DT | R/W | Serial Port Break Data<br>0: Input/output data is low-level<br>1: Input/output data is high-level |

### 3.3.25.11. SCIF Line Status Register (SCLSR)

| Address: H'0400_0124, Register name: SCIF Line Status Register (SCLSR), Initial Value: H'0000 | | | |
|---|---|---|---|
| Bit | Bit Name | R/W | Function |
| 15-1 | Reserved | R | Not used |
| 4-0 | ORER | R | Overrun Error<br>Indicates that an overrun error occurred during reception, causing abnormal termination.<br>0: Reception in progress, or reception has ended normally<br>[Clearing conditions]<br>• When 0 is written to ORER after reading ORER = 1<br>1: An overrun error occurred during reception<br>[Setting condition]<br>• When the next serial reception is completed while SCFDR receives 16-byte data (SCFDR is full) |

# 4. Extension Board Specification

Please observe the following matters when the extension board for this product is made by the customer.

Figure 4.1.1 shows the extension board dimensional drawing.

■In the substrate size, the vertical direction is 138.00mm fixation. Please give horizontal direction to me longest the shorts by 147.00mm as 100.00mm.

■CN13 and 14 are the insect eyeviews on the part side. The terminal number is also similar.

| CAUTION |
|---|
| Please do not mount parts other than CN13 and CN14 on the solder side of the extension board. |

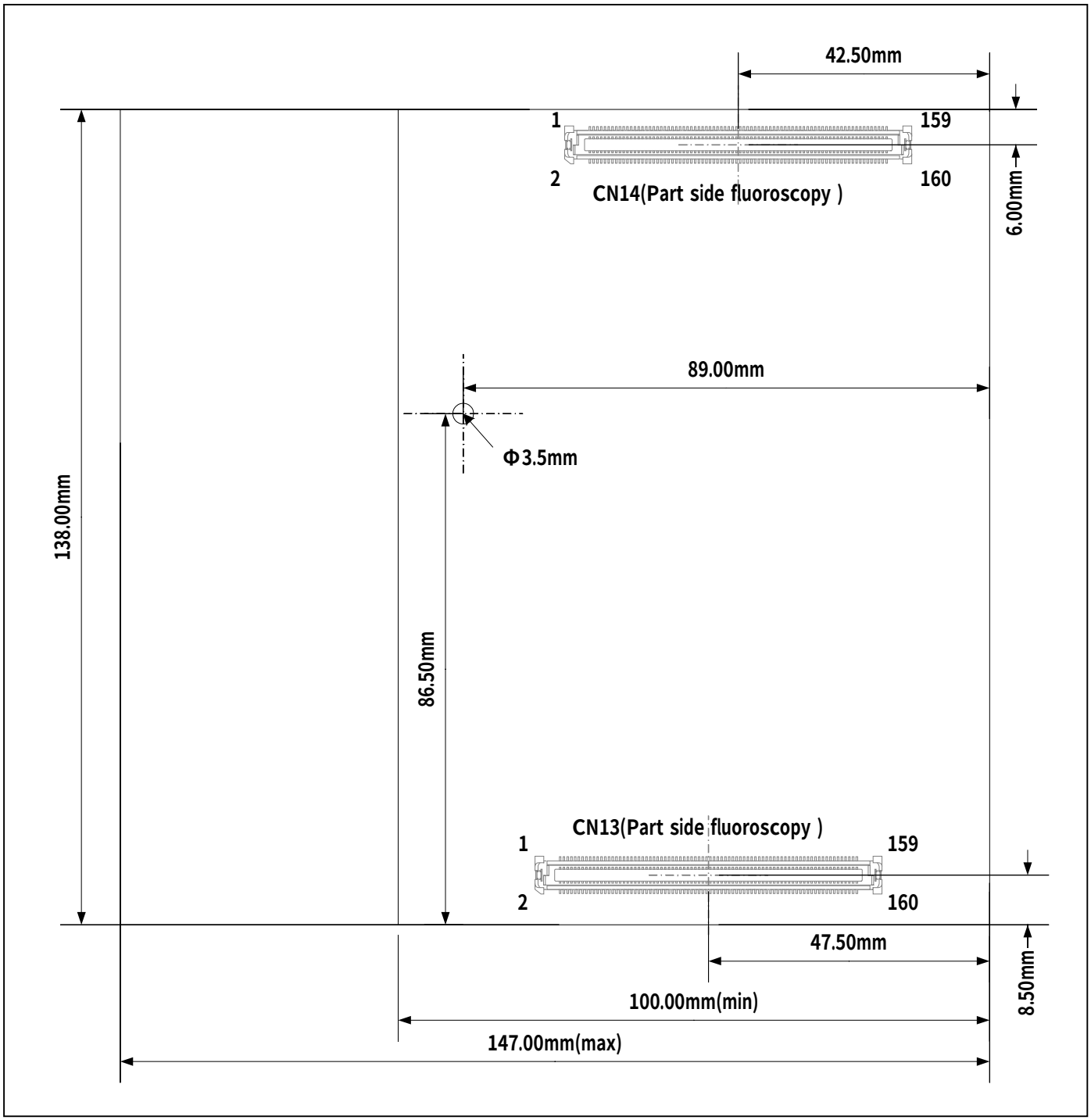



Figure 4.1.1 The extention board dimension

## 4.1. The allowable current of add-in board and PCI card

The maximum consumed electric power of this product is about 11W. When you carry out use of an add-in board or the PCI card of a user, be careful of the following points.

### 4.1.1. The allowable current of add-in board

When an add-in board is prepared of a user, please use the thing of the specification which does not exceed 3.3V/2A.

### 4.1.2. The allowable current of PCI board

When a PCI card is used of a user, please use the thing of the specification which does not exceed 3.3V/3A.

|  **CAUTION** |
|---|
| Although the connector based on PCI 5V card specification is mounted, the specification top PCI bus signal of SH7751R should use the card of 3.3V signal specification. If 5V signal is supplied to SH7751R, there is a possibility of destroying SH7751R. Moreover, it leads to destruction of this product. |

# 5. Boot Loader Specification

## 5.1. Boot Loader Functional List

The Boot Loader to start Linux is written on the FROM board bundled to this product. Table 5.1.1 shows the function to support by the boot loader. zImage used in this chapter indicates the Linux kernel image.

Table 5.1.1 Boot Loader Functional list

| No | Command | Function | Note |
|---|---|---|---|
| 1 | h or ? | Command list display | |
| 2 | b | Program loading from CF card | |
| 3 | l | The message display about license | |
| 4 | w | The message display about Warranty(None) | |
| 5 | n | Lord zImage from Ethernet | Channel:eth0 |
| 6 | z | Program counter movement and execution zImage development ahead | |
| 7 | i | Board information display | |
| 8 | v | Boot loader version information display | |

## 5.2. Command List Display

The command list supported by this boot loader in “h" or "?" input is displayed.

## 5.3. Load from CF Card

Stored zImage is downloaded from the CF card has been inserted in CN9 by “b” input and it starts.
It is necessary to prepare host PC in whom LinuxOS was installed by the customer for writing zImage. Moreover, please do the following when you write zImage on the CF card.

(1) The CF card is prepared, and EXT2 is formatted.
(2) The root file system is copied onto the CF card.
(3) A zImage is copied under "/boot" in the CF card.
(4) Please update the kernel by the lilo-command execution.

## 5.4. The Message Display about License

The message of the license of this boot loader is displayed by “1” input.
This boot loader is made based on free software SH IPL+g as shown in this message.

SH IPL+g is free software; you can redistribute it and/or modify it under the terms of the GNU Lesser General Public License as published by the Free Software Foundation; either version 2.1 of the License, or (at your option) any later version.

## 5.5. The Message Display about Warranty

The message of the guarantee of this boot loader is displayed by “w” input.
This boot loader is not wrranted as being in this message.

SH IPL+g is distributed in the hope that it will be useful, but WITHOUT ANY WARRANTY; without even the implied warranty of MERCHANTABILITY or FITNESS FOR A PARTICULAR PURPOSE.
See the GNU Lesser General Public License for more details.

## 5.6. Load zImage File from Ethernet

A zImage on host PC is downloaded by way of Ethernet in “n” input and it starts. Ethernet used becomes eth0 and uses RTL8139DL of device number 1. There is no problem wherever it uses it. The corresponding MAC address becomes an address on the MAC1 side.
However, it is necessary to construct the NFS (Network File System) environment to use this command.

## 5.7. Program counter movement and execution zImage development ahead

The program counter is moved and executed by "z" input development zImage ahead.

## 5.8. Board Information

Information on this product is displayed by "i" input.

<A setting example is as follows>

| | |
|---|---|
| CPU family | : SH4 |
| CPU name | : SH7751R |
| cache size | : 8K-byte/16K-byte |
| CPU clock | : 240.00MHz |
| Bus clock | : 120.00MHz |
| Module clock | : 60.00MHz |
| FPGA Version | : 1.1 |

## 5.9. Boot loader version information display

Version information on this boot loader is displayed by "v" input.

## 5.10. Boot Loader update

When this product is started in maintenance mode, rewriting of a boot loader is possible in the "u" input.
The specification of a maintenance mode boot loader is shown in Table 5.10.1.

Table 5.10.1 Maintenance mode boot loader specification list

| Item | Specification | Note |
|---|---|---|
| FROM board memory map | Refer to Figure 5.10.1 | |
| The communication method | RS232C | 115200bps/8bit/none parity/none control flow |
| Correspondence format | S-Type format. | File size is below a 512K byte.<br>ROM size is 64 K bytes or less. |
| Support FROM | Spansion | The program code for rewriting is copied to SDRAM, and is performed on SDRAM. |
| Operation mode | maintenance mode | It is rewritable only at the time of maintenance mode. |

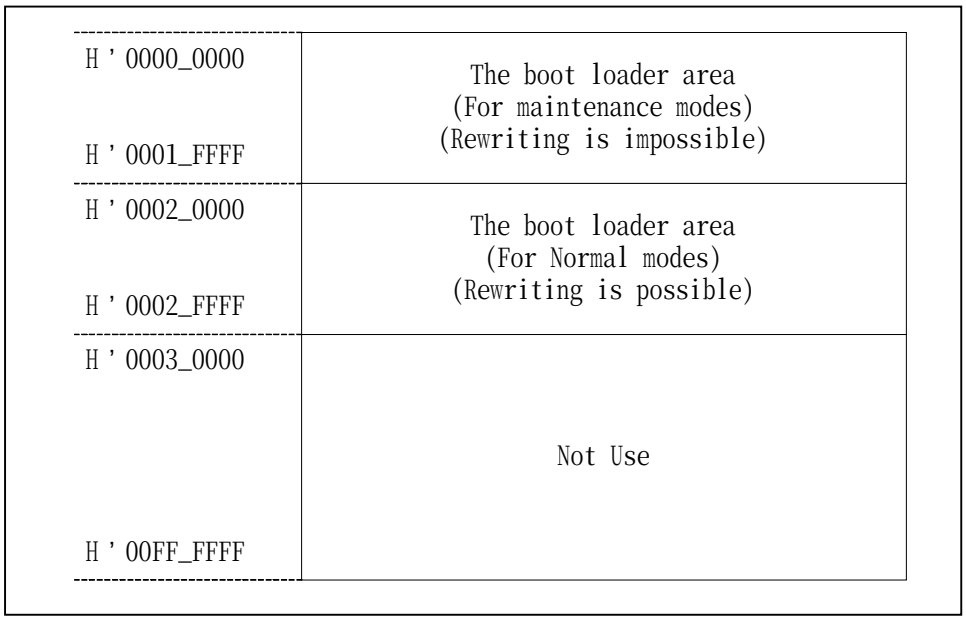



Figure 5.10.1 FROM board memory map

The boot loader rewriting procedure is as follows.

(1) It starts in maintenance mode.
(2) It rewrites by the “u” command and the mode is started.
(3) It is displayed on "please send S-Type format data" and a console.
(4) Transmission of a text file is chosen within 30 seconds, and a file to write an S-Type format is transmitted.
(*When a transmitting start is not carried out within 30 seconds, it becomes a time-out error.)
(5) If file transmission is completed. It is displayed one by one.
“decode start” → “decode finish” → “flash erase & program start” → “all finish”
(6) After rewriting is completed normally, it reboots in maintenance mode again.
(7) A power supply is once intercepted, a DIP switch is changed to the normal mode, and a power supply injection is carried out again.

* When rewriting goes wrong, please perform the above-mentioned procedure again.

## 5.11. Test Mode

When this product is started in maintenance mode, failure diagnosis of a board is possible in the "t" input. The contents which can be checked in this test mode are in the connection state of SH bus, SH PCI bus, and other devices. It cannot check about the connection state between each device-connector.

A test mode specification list is shown in Table 5.11.1.

Table 5.11.1 Test mode specification list

| command | Item | Specification |
|---|---|---|
| 1 | RAM Check | Area3 SDRAM Write/Read Check |
| 2 | FPGA Version Check | Area1 FPGA Version Register Check |
| 3 | SM501 Device ID Check | Are14 SM501 Device IDRegister Check |
| 4 | LED & Dip Switch Check | Debugging LED、DIP Switches Check |
| 5 | eth0 Device ID Vender ID Check | DEVNO H'1 RTL8139DL Access Check |
| 6 | eth1 Device ID Vender ID Check | DEVNO H'3 RTL8139DL Access Check |
| 7 | CardBus controller Device ID Vender ID Check | DEVNO H'2 PCII1520ZHK Access Check |
| 8 | PCI Slot Check | DEVNOH'0 PCI Card Connecter Access Check |
| 9 | All Check (1 to 8) | No.1 to 8 is performed one by one. |
| a | Mac Address Write | MAC Address writing |
| b | Mac Address Read | MAC Address read-out |

At the time of test mode starting, the input command of Table 5.11.1 and an item list are displayed. When performing each test, the corresponding command number is inputted. If it is normal operation and is "ok" and unusual operation, "no good" and the contents of an error will be displayed.

### 5.11.1. RAM Check

The access check of SDRAM (M1, M2) arranged in area 3 in "1" input is performed. Data are written in shifting 1 bit of address buses at a time, and it compares with expected value.

### 5.11.2. FPGA Version Check

"2" inputs are the access checks of FPGA (U34) arranged in area 1. The 0x04000032nd values (VERREG) are read and it compares with expected value 0x0011.

### 5.11.3. SM501 Device ID Check

"3" inputs are the access checks of SM501GX (U33) arranged in area 4. The 0x0x13E00060th values (Devicd Id) are read, and it compares with expected value 0x050100A0.

### 5.11.4. LED & Dip Switch Check

"4" inputs are the access checks of LED for debugging, and a DIP switch. The following operations are performed.

(1) It is displayed as 'please input S3"01010101"' on a console.

(2) S3 is set up as a specification bit and a return key is inputted.

The setup of a switch is as follows.

| Switch No. | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| set value | OFF | ON | OFF | ON | OFF | ON | OFF | ON |

(3) When the input of "0xAA" is able to be checked, it is displayed on a console as "ok" and the correspondence bit of LED is turned on. In the case of NG, it is displayed as "no good".

(4) In “ok”, it is displayed as ‘please input S3"10101010"’ on a console by the test of (1) to (3).
(5) S3 is set up as a specification bit and a return key is inputted.
The setup of a switch is as follows.

| Switch No. | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| set value | ON | OFF | ON | OFF | ON | OFF | ON | OFF |

(6) When the input of “0x55” is able to be checked, it is displayed on a console as “ok” and the correspondence bit of LED is turned on. In the case of NG, it is displayed as “no good”.

### 5.11.5. eth0 Device ID Vender ID Check

“5” inputs perform the access check of RTL8139DL (U13) arranged to the PCI bus.
0x80000800 is written in the 0xFE2001C0th of SH7751R, 0xFE200220th is read, and it compares with expected-value 0x813910EC.

### 5.11.6. eth1 Device ID Vender ID Check

“6” inputs perform the access check of RTL8139DL (U12) arranged to the PCI bus.
0x80001800 is written in the 0xFE2001C0th of SH7751R, 0xFE200220th data is read, and it compares with expected-value 0x813910EC.

### 5.11.7. CardBus controller Device ID Vender ID Check

“7” inputs perform the access check of PCI1520ZHK (U10) arranged to the PCI bus.
0x80001000 is written in the 0xFE2001C0th of SH7751R, 0xFE200220th data is read, and it compares with expected-value 0xAC55104C.

### 5.11.8. PCI Slot Check

“8” inputs perform the access check to the PCI card connector arranged to the PCI bus.
0x80001000 is written in the 0xFE2001C0th of SH7751R, and the 0xFE200220th data are read and displayed.
By this test, there is no display of “ok” and “no good”.

### 5.11.9. All Check (1 to 8)

“9” inputs execute commands 1-8 one by one.

### 5.11.10. Mac Address Write

This command is used before this product shipment. Use of a user is forbidden. When this command is executed accidentally, please push S5 and return to an initial state.

### 5.11.11. Mac Address Read

This command is used before this product shipment. Use of a user is forbidden. When this command is executed accidentally, please push S5 and return to an initial state.

# 6. Linux Kernel Download

About Linux software, it is downloadable from the following URL etc.

http://www.kernel.org/

http://www.linux-sh.org/cgi-bin/moin.cgi

http://mirror.sh-linux.org/rpm-index/index.html

http://www.m17n.org/linux-sh/

http://www.superh-linux.org/

|  **CAUTION** |
|---|
| Downloadable software is an open source and is not contained in the range of a guarantee.<br>The information about GPL refers to http://www.gnu.org/copyleft/gpl.html, and please uses it in the range of a user's responsibility. |

# 7. Appendix

## 7.1. R0P751RLC0011RL Circuit

## 7.2. FROM Board Circuit

SH7751R Evaluation Platform
User's Manual
R0P751RLC0011RL

Publication Date: Jun. 2006 Rev.1.00

Published by: Renesas Solutions Corp.
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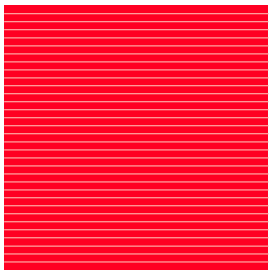
# R0P751RLC0011RL
# User's Manual



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