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Sparrow Hawk-V4H

- Hardware User's Manual

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Revision History

Description	Revision	Date
Initial Release	V0.0.5	2025/06/18
Revise Section 1 : Add hardware version info	V0.0.6	2025/06/26
Add Section 1.4 Environment Specification Revise Section 1.1 : Correct Description Section 2.3.1 : Add support type Section 2.5.1 : Add CTIA & OMTP configuration setting Section 2.6.2 : Correct VBUS description Section 2.12.2 : Clarify the description Section 2.12.3 : Correct VBUS description. Change Figure 1, Table 2 and 4.	V0.0.7	2025/07/09
Revise Section 2.6.3 : Correct VBUS description Section 2.12.3 : Add the requirement of USB PD charger	V0.0.8	2025/07/10
Add Legal Notice and Disclaimer	V0.0.9	2025/07/18
Revise Table of Contents Section 2.7 : Index No. Add Figure 4 : ACC power on/off illustration	V0.1.0	2025/07/21
Revise Header & Footer Add Figure 4 : PCIE M.2 Form factor illustration Change Figure 2 : Swap J1 & J2 illustration	V0.1.1	2025/07/23
Add Section 2.10 : Supported memory card types	V0.1.2	2025/08/06
Revise Header Change Figure 2 : Highlight SoC marking	V0.1.3	2025/08/06
Revise Section 1.1 : Debugger interface Typo Add Section 1.4 : Mechanical Dimension	V0.1.4	2025/08/12
Revise Figure 1 :	V0.1.5	2025/08/20

1. Overview

This document provides a comprehensive guide to the Sparrow Hawk hardware, including connectors, switches, and system configurations. Using the Sparrow Hawk board allows the developers to efficiently conduct required tasks such as evaluation of the Renesas R-Car V4H system performance and thus greatly to reduce the turn-around time in their product development.

This manual applies to hardware version Sparrow Hawk Rev. 1.1. Please ensure the board revision matches this manual to avoid configuration or compatibility issues.

Hardware Version: Sparrow Hawk Rev. 1.1
Date: July 2025

1.1 Features

The following table lists the features of the Sparrow Hawk board. For the features of the Renesas R-Car V4H, see the ***Renesas R-Car V4H Series User's Manual: Hardware.***

Item	Description
SoC	Renesas R-Car V4H
NOR flash memory	Serial NOR flash memory device for QSPI0
SDRAM	LPDDR5 device for DBSC5
Display interfaces	1 x Display port connector for DSI1 1 x Output connector for DSI0
Video input interfaces	2 x Input connectors for CSI0 and CSI1
Memory interfaces	1 x MicroSD slot for SD card
Network interfaces	1 x 6-pin connector for CANFD3 and CANFD4 1 x RJ45 connector for EtherAVB0
Peripheral interfaces	1 x M.2 Key-M connector 2 x USB TYPE A connector for USB3.0 2 x USB TYPE C connector for USB3.0 1 x Headset connector for I2S(MSIOF) 1 x AUX_IN connector for I2S(MSIOF) 1 x 40-pin connector for GPIO, I2C and UART
Debugger interface	1 x 20-pin JTAG connector for JTAG 1 x USB Micro-B connector for HSCIF0 and HSCIF1

1.2 System Block Diagram
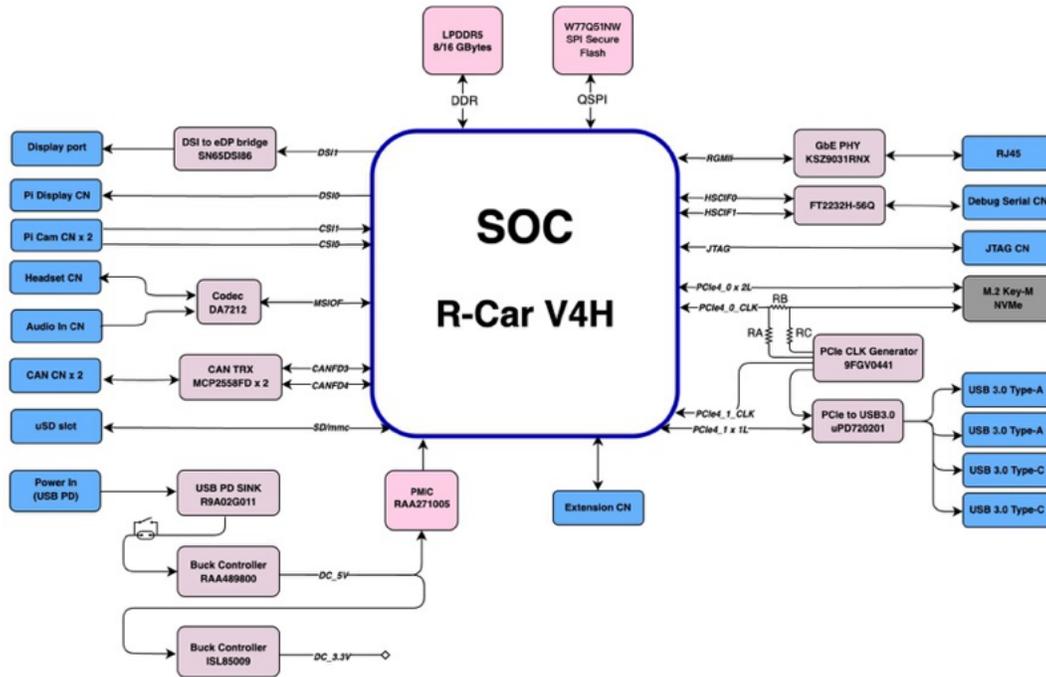
Figure 1. System Block Diagram

1.3 PCBA Overview

This section provides an overview of the main hardware components visible on the Sparrow Hawk printed circuit board assembly (PCBA), including the DIP switch, control buttons, and I/O connectors.

1.3.1. PCBA Layout Top View
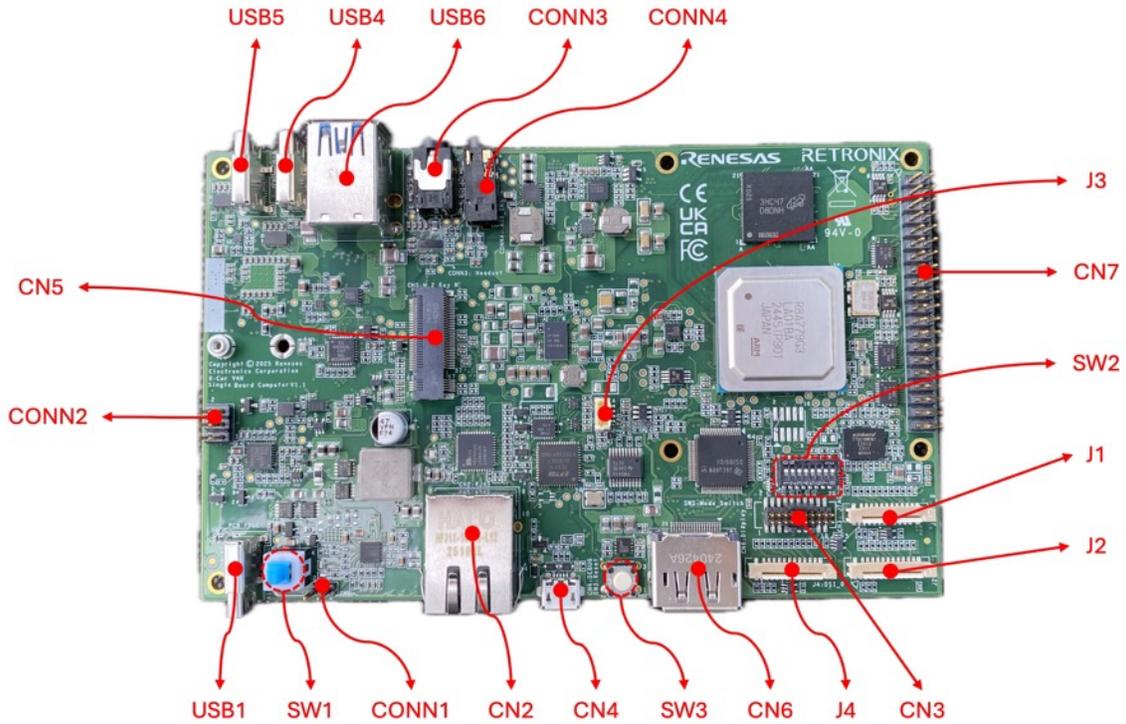
Figure 2. PCBA Layout Top View

1.3.2. PCBA Layout Bottom View
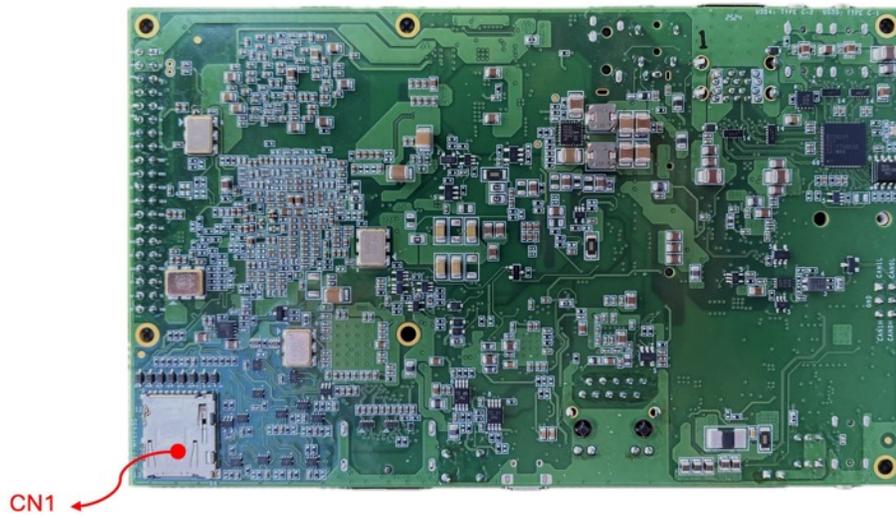
Figure 3. PCBA Layout Bottom View

1.4   Mechanical Dimensions

This section provides the dimensional characteristics of the Sparrow Hawk board to assist in mechanical integration, enclosure design, and system assembly. All dimensions are provided in millimeters unless otherwise specified. Tolerances should be observed as indicated in the accompanying mechanical drawing.
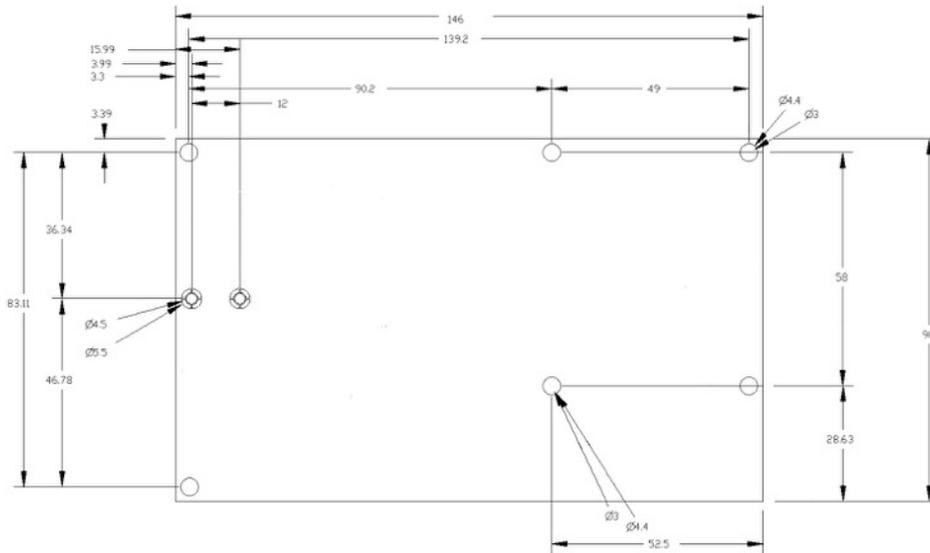
Figure 4. PCBA Mechanical Dimensions

1.5   Environment Specifications

The Sparrow Hawk board is intended for use in controlled indoor environments. The recommended environmental operating conditions are:

Table 1. Environment Specifications

Environment Specification	
Parameter	**Specification**
Operating Temperature	0°C to 40°C
Operating Humidity	5% to 95% RH (non-condensing)

2. Connectors and Switches Assignment

This section describes the configuration and assignment of DIP switch, connectors, and related settings on the Sparrow Hawk board.

2.1 Initial Switch Setting

The following table shows the default configuration of the DIP switch (**SW2**) used during system initialization.

Table 2. Initial Configuration of Mode Switch

DIP Switch	SW2
Settings	1110(1)111
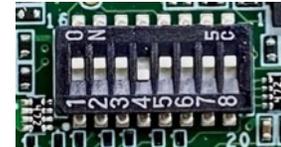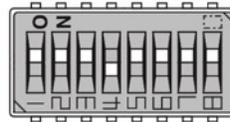
*Note: 1=ON, 0=OFF

2.2 Mode Switch (SW2)

The DIP switch (**SW2**) controls various boot and configuration settings via multiple mode pins (MD). The table below outlines the function of each pin on SW2.

SW2								
Pin	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
Signal	MD1	MD2	MD4	MD6	-	MD20	MD21	MD10
Electrical Condition								
ON	Pull-down to GND							
OFF	Pull-up to 3.3V							

These pins(**MD1**,**MD2**,**MD4**) are used to select the boot device of Sparrow Hawk board.

Table 3. Selection of Boot Device

SW2				
Pin	**1**	**2**	**3**	**Selection of Boot Device**
Signal	MD1	MD2	MD4	
Status	ON	ON	ON	Serial flash ROM with single reading at 40 MHz with the use of DMA (Default)
	OFF	OFF	OFF	HSCIF downloading mode, 921,600 bps
	Other than the above			Not Supported

MD6 is used to select the master boot processor of Sparrow Hawk board.

Table 4. Selection of Master Boot Processor

SW2		
Pin	**4**	**Selection of Master Boot Processor**
Signal	MD6	
Status	OFF	Booted through Cortex-R52(Default)
	ON	Booted through ICUMXA

The JTAG functions are determined by the combination of **MD20**, **MD21**, and **MD10** pin states. The table below outlines the supported configurations:

Table 5. Selection of JTAG Debugging functions

SW2			
Pin	**6**	**7**	**8**
Signal	MD20	MD21	MD10
Status	ON	ON	ON
	OFF	ON	ON
	ON	OFF	ON
	OFF	ON	OFF
	Other than the above		

JTAG(CN3)
-(Initial Default)
ICUMX JTAG
CoreSight
ICUMX LPD
Settings Reserved

2.3   PCIe Interface

The Sparrow Hawk board provides a PCI Express interface via a standard M.2 Type M connector. This interface enables high-speed communication with expansion modules such as SSDs, wireless adapters, or other PCIe-based devices.

2.3.1.   PCIE M.2 Connector (SSD) (CN5)

The PCIe M.2 connector supports:

● Up to two PCIe lanes (x2 configuration)

● Module form factors 2230 and 2242
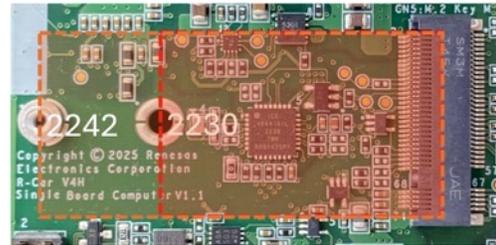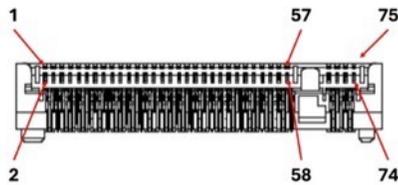
Figure 5. PCIE M.2 Form factor illustration

● **CN5**: JAE SM3ZS067U410AMR1000, PCI-SIG standard M.2 compatible card edge connector, 67 contacts, **TYPE M**, SMD/SMT, Right Angle.

Table 6. PCIE M.2 Type M Connector (CN5) Pin Assignment

CN5			
Pin	Signal	Description	Type
1	CONFIG3	Module type configuration	-
2	D3.3V1_M2	+3.3V power supply	Power
3	GND	Ground	Power
4	D3.3V1_M2	+3.3V power supply	Power
5	NC	-	-
6	NC	-	-
7	NC	-	-
8	NC	-	-
9	GND	Ground	Power
10	NC	-	-
11	NC	-	-
12	D3.3V1_M2	+3.3V power supply	Power
13	NC	-	-
14	D3.3V1_M2	+3.3V power supply	Power
15	GND	Ground	Power
16	D3.3V1_M2	+3.3V power supply	Power
17	NC	-	-
18	D3.3V1_M2	+3.3V power supply	Power

19	NC	-	-
20	NC	CP55	-
21	CONFIG0	Module type configuration (Floating)	-
22	NC	-	-
23	NC	-	-
24	NC	CP56	-
25	NC	-	-
26	NC	CP57	-
27	GND	Ground	Power
28	NC	CP58	-
29	PCIE0_RX1_M	PCIe Port 0 Lane 1 receive differential pair (negative) of (U1) V4H	I
30	NC	-	-
31	PCIE0_RX1_P	PCIe Port 0 Lane 1 receive differential pair (positive) of (U1) V4H	I
32	GND	Ground	Power
33	GND	Ground	Power
34	NC	-	-
35	PCIE0_TX1_M	PCIe Port 0 Lane 1 transmit differential pair (negative) of (U1) V4H	O
36	NC	-	-
37	PCIE0_TX1_P	PCIe Port 0 Lane 1 transmit differential pair (positive) of (U1) V4H	O
38	NC	-	-
39	GND	Ground	Power
40	NC	-	-
41	PCIE0_RX0_M	PCIe Port 0 Lane 0 receive differential pair (negative) of (U1) V4H	I
42	NC	-	-
43	PCIE0_RX0_P	PCIe Port 0 Lane 0 receive differential pair (positive) of (U1) V4H	I
44	NC	-	-
45	GND	Ground	Power
46	NC	-	-
47	PCIE0_TX0_M	PCIe Port 0 Lane 0 transmit differential pair (negative) of (U1) V4H	O
48	NC	-	-
49	PCIE0_TX0_P	PCIe Port 0 Lane 0 transmit differential pair (positive) of (U1) V4H	O
50	GP2_02/M2_RESET	PCIe Reset (Active Low)	O
51	GND	Ground	Power
52	NC	-	-
53	PCIE0_CLK_M2_M	PCIe Port 0 reference Clock differential pair (negative) of (U1) V4H	O
54	NC	-	-
55	PCIE0_CLK_M2_P	PCIe Port 0 reference Clock differential pair (positive) of (U1) V4H	O
56	NC	-	-
57	GND	Ground	Power
58	NC	-	
59-66	Key Notch	Mechanical Key for M	-
67	NC	CP59	-

68	D3.3V1_M2	+3.3V power supply	Power
69	CONFIG1	Module type configuration	-
70	D3.3V1_M2	+3.3V power supply	Power
71	GND	Ground	Power
72	D3.3V1_M2	+3.3V power supply	Power
73	GND	Ground	Power
74	D3.3V1_M2	+3.3V power supply	Power
75	CONFIG2	Module type configuration	-

2.4 GPIO, I2C and UART Interface

The Sparrow Hawk board provides a 40-pin GPIO connector that also supports I²C and UART communication. This interface enables flexible integration with sensors, actuators, and peripheral devices.

2.4.1. GPIO, I2C and UART Connector (CN7)
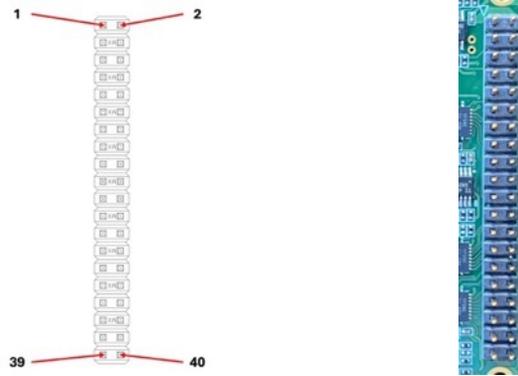
- **CN7**: Molex 10897400, 2.54mm Pitch C-Grid Breakaway Header, Dual Row, Vertical, High Temperature, 40 Circuits, 0.76µm Gold (Au) Selective Plating, Tin (Sn) PC Tail Plating, 2.72mm PC Tail.

Table 7. GPIO, I2C and UART Connector (CN7) Pin Assignment

CN7			
Pin	Signal	Description	Type
1	D3.3V1	+3.3V Power Supply	Power
2	D5.0V1	+5.0V Power Supply	Power
3	SDA	I2C3 serial data input/output pin of (U1) V4H	I/O
4	D5.0V1	+5.0V Power Supply	Power
5	SCL	I2C3 serial clock input/output pin of (U1) V4H	I/O
6	GND	Ground	Power
7	GPIO 4	IO/Interrupt input Port GP1_06 of (U1) V4H	I/O
8	GPIO 14/TXD	IO/Interrupt input Port GP1_28 or HSCIF3 Transmit data output pin of (U1) V4H	I/O
9	GND	Ground	Power
10	GPIO 15/RXD	IO/Interrupt input Port GP1_24 or HSCIF3 Receive data input pin of (U1) V4H	I/O
11	GPIO 17	IO/Interrupt input Port GP2_12 of (U1) V4H	I/O
12	GPIO 18	IO/Interrupt input Port GP2_13 of (U1) V4H	I/O
13	GPIO 27	IO/Interrupt input Port GP2_05 of (U1) V4H	I/O
14	GND	Ground	Power
15	GPIO 22	IO/Interrupt input Port GP2_06 of (U1) V4H	I/O
16	GPIO 23	IO/Interrupt input Port GP2_04 of (U1) V4H	I/O
17	D3.3V1	+3.3V Power Supply	Power
18	GPIO 24	IO/Interrupt input Port GP1_25 of (U1) V4H	I/O

19	GPIO 10/MOSI	IO/Interrupt input Port GP1_09 or MSIOF0 Transmit data output pin of (U1) V4H	I/O
20	GND	Ground	Power
21	GPIO 9/MISO	IO/Interrupt input Port GP1_11 or MSIOF0 Receive data input pin of (U1) V4H	I/O
22	GPIO 25	IO/Interrupt input Port GP1_26 of (U1) V4H	I/O
23	GPIO 11/SCLK	IO/Interrupt input Port GP1_10 or MSIOF0 serial clock for transmission pin of (U1) V4H	I/O
24	GPIO 8	IO/Interrupt input Port GP1_08 of (U1) V4H	I/O
25	GND	Ground	Power
26	GPIO 7	IO/Interrupt input Port GP1_09 of (U1) V4H	I/O
27	GPIO 0/ID_SD	IO/Interrupt input Port GP8_09 or I2C4 serial data input/output pin of (U1) V4H	I/O
28	GPIO 1/ID_SC	IO/Interrupt input Port GP8_08 or I2C4 serial clock input/output pin of (U1) V4H	I/O
29	GPIO 5	IO/Interrupt input Port GP0_04 of (U1) V4H	I/O
30	GND	Ground	Power
31	GPIO 6	IO/Interrupt input Port GP0_07 of (U1) V4H	I/O
32	GPIO 12	IO/Interrupt input Port GP2_18 of (U1) V4H	I/O
33	GPIO 13	IO/Interrupt input Port GP2_19 of (U1) V4H	I/O
34	GND	Ground	Power
35	GPIO 19/PCM_FS	IO/Interrupt input Port GP0_09 or MSIOF5 frame synchronization signal for transmission of (U1) V4H	I/O
36	GPIO 16	IO/Interrupt input Port GP2_13 of (U1) V4H	I/O
37	GPIO 26	IO/Interrupt input Port GP1_27 of (U1) V4H	I/O
38	GPIO 20/PCM_DIN	IO/Interrupt input Port GP0_12 or MSIOF5 Receive data input pin of (U1) V4H	I/O
39	GND	Ground	Power
40	GPIO 21/PCM_DOUT	IO/Interrupt input Port GP0_10 or MSIOF5 Transmit data output pin of (U1) V4H	I/O

2.5 Audio Interfaces

The Sparrow Hawk board provides audio input and output through two 3.5 mm stereo connectors: one for headsets and one for auxiliary input.

2.5.1. Headset Connector (CONN3)
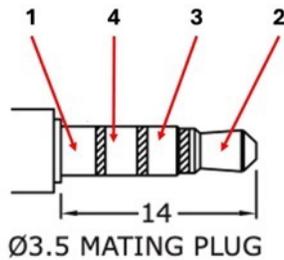
- **CONN3** : SAME KEY SJ3-350114B, 3.5 mm Stereo Jack, Through Hole, 4 Conductors, 1 Internal Switches

- **CTIA/OMTP Configuration** : The board supports both CTIA (**C**ellular **T**elecommunications **I**ndustry **A**ssociation) and OMTP (**O**pen **M**obile **T**erminal **P**latform) headset Pin Assignment standards. To configure the correct standard, adjust the resistor population as follows:

CTIA/OMTP Configuration	
Standard	**Resistor Settings**
CTIA	Mount R630 and R633, unmount R631 and R632 (Default)
OMTP	Mount R631 and R632, unmount R630 and R633

Table 8. Headset Connector (CONN3) Pin Assignment-(CTIA)

CONN3-CTIA			
Pin	**Signal**	**Description**	**Type**
1	MIC/ MIC1_P	Differential mic. input 1 (pos) / Single-ended mic. input 1 (left) of (U67)DA7212	I
2	HPL/HP_L	True-ground headphone output left of (U67)DA7212	O
3	HPR/HP_R	True-ground headphone output right of (U67)DA7212	O
4	GND/ GND_SENSE	Ground reference for headphone output of (U67)DA7212	-
5	DET	Tip Switch detection signal	-

Table 9. Headset Connector (CONN3) Pin Assignment-(OMTP)

CONN3-OMTP			
Pin	**Signal**	**Description**	**Type**
1	GND/ GND_SENSE	Ground reference for headphone output of (U67)DA7212	-
2	HPL/HP_L	True-ground headphone output left of (U67)DA7212	O
3	HPR/HP_R	True-ground headphone output right of (U67)DA7212	O
4	MIC/ MIC1_P	Differential mic. input 1 (pos) / Single-ended mic. input 1 (left) of (U67)DA7212	I
5	DET	Tip Switch detection signal	-

2.5.2. AUX-IN Connector (CONN4)
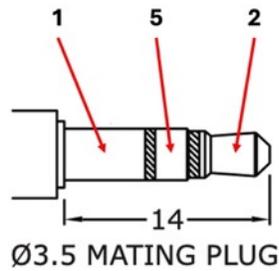
- **CONN4** : SAME KEY SJ3-35083C-TR, 3.5 mm Stereo Jack, Through Hole, 3 Conductors, 0 Internal Switches

Table 10. AUX-IN Connector (CONN4) Pin Assignment

CONN4			
Pin	Signal	Description	Type
1	GND	Ground	-
2	LEFT/AUX_L	Single-ended auxiliary input right of (U67)DA7212	I
3	NC	No Connection	-
4	DET	Tip Switch	-
5	RIGHT/AUX_R	Single-ended auxiliary input left of (U67)DA7212	I

2.6 USB interfaces

The Sparrow Hawk board includes three USB interfaces:

● One USB 3.0 Type-A dual port (**USB6**)

● Two USB 3.0 Type-C ports (**USB4, USB5**)

● One Micro USB Type-B debug port (**CN4**)

2.6.1. USB3.0 Type A Connector (USB6)
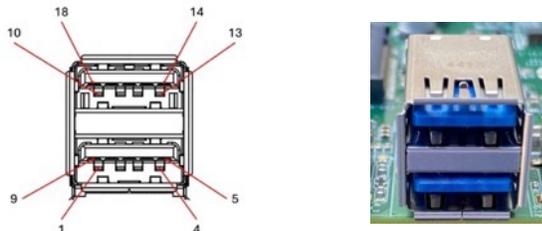
● **USB6** : Amphenol GSB3112311HR, USB 3.0, Type A, Receptacle, Right Angle Stacked, 18 Pins, Shell Kink with Nickel Plating, 30µin Gold, Dip 3.0mm, Blue High Temperature Housing.

Table 11. USB3.0 Type A Connector (USB6) Pin Assignment

	USB6		
Pin	Signal	Description	Type
1	VBUS/VCCCH4	+5V Power Supply	Power
2	D-/DM4_CN	USB2.0 D– signal for Hi-/Full-/Low-Speed of (U46) uPD720201	I/O
3	D+/DP4_CN	USB2.0 D+ signal for Hi-/Full-/Low-Speed of (U46) uPD720201	I/O
4	GND	Ground	Power
5	SSRX-/RXDN4_CN	USB3.0 Receive data D- signal for SuperSpeed of (U46) uPD720201	I
6	SSRX+/RXDP4_CN	USB3.0 Receive data D+ signal for SuperSpeed of (U46) uPD720201	I
7	GND	Ground	Power
8	SSTX-/TXDN4_CN	USB3.0 Transmit data D- signal for SuperSpeed of (U46) uPD720201	O
9	SSTX+/TXDP4_CN	USB3.0 Transmit data D+ signal for SuperSpeed of (U46) uPD720201	O
10	VBUS/VCCCH3	+5V Power Supply	Power
11	D-/DM3_CN	USB2.0 D– signal for Hi-/Full-/Low-Speed of (U46) uPD720201	I/O
12	D+/DP3_CN	USB2.0 D+ signal for Hi-/Full-/Low-Speed of (U46) uPD720201	I/O
13	GND	Ground	Power
14	SSRX-/RXDN3_CN	USB3.0 Receive data D- signal for SuperSpeed of (U46) uPD720201	I
15	SSRX+/RXDP3_CN	USB3.0 Receive data D+ signal for SuperSpeed of (U46) uPD720201	I
16	GND	Ground	Power
17	SSTX-/TXDN3_CN	USB3.0 Transmit data D- signal for SuperSpeed of (U46) uPD720201	O
18	SSTX+/TXDP3_CN	USB3.0 Transmit data D+ signal for SuperSpeed of (U46) uPD720201	O

2.6.2. USB Type C Connector (USB4, USB5)
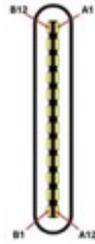
- **USB4, USB5** : TECHBEST USB3.1_24_Type-C, USB3.1 Type C, Female, 24 pins, upright. SMT

Table 12. USB3.0 Type C Connector (USB4, USB5) Pin Assignment

USB4, USB5			
Pin	Signal	Description	Type
A1	GND	Ground	Power
A2	SSTX1+	USB3.0 Transmit data D+ signal for SuperSpeed of (U46) uPD720201	O
A3	SSTX1-	USB3.0 Transmit data D- signal for SuperSpeed of (U46) uPD720201	O
A4	VBUS	+5.0V Power Supply	Power
A5	NC	No Connection.	-
A6	D+	USB2.0 D+ signal for Hi-/Full-/Low-Speed of (U46) uPD720201	I/O
A7	D-	USB2.0 D− signal for Hi-/Full-/Low-Speed of (U46) uPD720201	I/O
A8	NC	No Connection	-
A9	VBUS	+5.0V Power Supply	Power
A10	SSRX2-	USB3.0 Receive data D+ signal for SuperSpeed of (U46) uPD720201	I
A11	SSRX2+	USB3.0 Receive data D- signal for SuperSpeed of (U46) uPD720201	I
A12	GND	Ground	Power
B1	GND	Ground	Power
B2	SSTX2+	USB3.0 Transmit data D+ signal for SuperSpeed of (U46) uPD720201	O
B3	SSTX2-	USB3.0 Transmit data D- signal for SuperSpeed of (U46) uPD720201	O
B4	VBUS	+5.0V Power Supply	Power
B5	NC	No Connection.	-
B6	D+	USB2.0 D+ signal for Hi-/Full-/Low-Speed of (U46) uPD720201	I/O
B7	D-	USB2.0 D− signal for Hi-/Full-/Low-Speed of (U46) uPD720201	I/O
B8	NC	No Connection.	-
B9	VBUS	+5.0V Power Supply	Power
B10	SSRX1-	USB3.0 Receive data D+ signal for SuperSpeed of (U46) uPD720201	I
B11	SSRX1+	USB3.0 Receive data D- signal for SuperSpeed of (U46) uPD720201	I
B12	GND	Ground	Power

2.6.3. Debug Serial Micro USB Type B Connector (CN4)
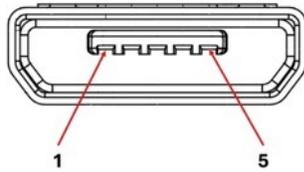
- **CN4** : Hirose ZX62D-B-5PA8, Micro USB Type B Connector, Female, USB2.0, SMT, 5 contact

Table 13. Debug Serial Micro USB Type B Connector (CN4) Pin Assignment

Pin	Signal	Description	Type
**CN4**			

Pin	Signal	Description	Type
1	USB_VBUS	+5.0V Power Supply	Power
2	D-/USB_DM	USB2.0 D– signal for Hi-/Full-/Low-Speed of (U28) FT2232H	I/O
3	D+/USB_DP	USB2.0 D+ signal for Hi-/Full-/Low-Speed of (U28) FT2232H	I/O
4	ID	Connect to GND	-
5	GND	Ground	Power

2.7 Ethernet Interface

The Sparrow Hawk board provides a high-speed Ethernet connection via a standard RJ45 connector, which supports AVB (Audio Video Bridging) through the Renesas R-Car V4H SoC's EtherAVB0 port.

2.7.1. Ethernet AVB Interface (CN2)
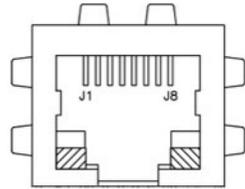
- **CN2** : Halo HFJ11-1G41E-L12RL, Modular Connectors / Ethernet Connectors GIGABIT 1x1 Tab Down RJ45 w/mag G/Y LED.

Table 14. Ethernet AVB Interface (CN2) Pin Assignment

| CN2			
Pin	Signal	Description	Type
J1	TXRXP_A	Media Dependent Interface[0] of (U26)KSZ9031RNXVB, positive signal of differential pair, (U1) V4H EtherAVB0 port	I/O
J2	TXRXM_A	Media Dependent Interface[0] of (U26)KSZ9031RNXVB, negative signal of differential pair, (U1) V4H EtherAVB0 port	
J3	TXRXP_B	Media Dependent Interface[1] of (U26)KSZ9031RNXVB, positive signal of differential pair, (U1) V4H EtherAVB0 port	
J4	TXRXP_C	Media Dependent Interface[2] of (U26)KSZ9031RNXVB, positive signal of differential pair, (U1) V4H EtherAVB0 port	
J5	TXRXM_C	Media Dependent Interface[2] of (U26)KSZ9031RNXVB, negative signal of differential pair, (U1) V4H EtherAVB0 port	
J6	TXRXM_B	Media Dependent Interface[1] of (U26)KSZ9031RNXVB, negative signal of differential pair, (U1) V4H EtherAVB0 port	
J7	TXRXP_D	Media Dependent Interface[3] of (U26)KSZ9031RNXVB, positive signal of differential pair, (U1) V4H EtherAVB0 port	
J8	TXRXM_D	Media Dependent Interface[3] of (U26)KSZ9031RNXVB, negative signal of differential pair, (U1) V4H EtherAVB0 port	

2.8   Display Interfaces

The Sparrow Hawk board supports two display output options:

● A standard DisplayPort (DP) connector (**CN6**)

● A 22-pin MIPI DSI (Display Serial Interface) connector for flat-panel displays (**J4**)

2.8.1. Display Port Connector (CN6)
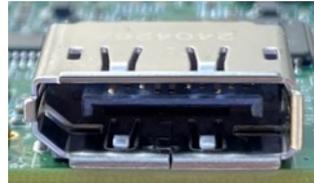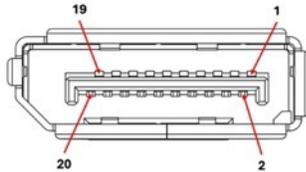
● **CN6** : Molex SD-47272-001, 0.50mm Pitch DisplayPort Receptacle, Right-Angle, Surface Mount, 0.76μm Gold (Au) Plating, 20 Circuits, without Cover, Mylar or Flange; with Latch Holes, Peg and Solder Tab of Shell, Lead-Free

Table 15. DP Connector (CN6) Pin Assignment

CN6			
Pin	Signal	Description	Type
1	MainLane0+	DisplayPort lane 0 transmit differential pair, Positive Signal, Connect to (U54) SN65DSI86	O
2	GND	Ground	Power
3	MainLane0-	DisplayPort lane 0 transmit differential pair, Negative Signal, Connect to (U54) SN65DSI86	O
4	MainLane1+	DisplayPort lane 1 transmit differential pair, Positive Signal, Connect to (U54) SN65DSI86	O
5	GND	Ground	Power
6	MainLane1-	DisplayPort lane 1 transmit differential pair, Negative Signal, Connect to (U54) SN65DSI86	O
7	MainLane2+	DisplayPort lane 2 transmit differential pair, Positive Signal, Connect to (U54) SN65DSI86	O
8	GND	Ground	Power
9	MainLane2-	DisplayPort lane 2 transmit differential pair, Negative Signal, Connect to (U54) SN65DSI86	O
10	MainLane3+	DisplayPort lane 3 transmit differential pair, Positive Signal, Connect to (U54) SN65DSI86	O
11	GND	Ground	Power
12	MainLane3-	DisplayPort lane 3 transmit differential pair, Negative Signal, Connect to (U54) SN65DSI86	O
13	CONFIG1	Configuration (Connected to ground)	-
14	CONFIG2	Configuration (Connected to ground)	-
15	AUX+	Auxiliary Channel Positive	I/O
16	GND	Ground	Power
17	AUX-	Auxiliary Channel Negative	I/O
18	HPD	Hot Plug Detect. Detects connection to a display	I
19	Return	Return for Power	Power
20	DP_PWR	+3.3V Power for connector	Power

2.8.2. MIPI DSI Interface Connector (J4)
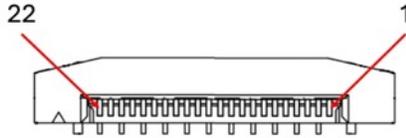
- **J4** : Molex 525592253, **FFC/FPC Connector**. 0.50mm Pitch, Slider Series, Vertical, 3.90mm Height, 22 Circuits, Gold Plating.

Table 16. MIPI DSI IF Connector (J4) Pin Assignment

J4			
Pin	**Signal**	**Description**	**Type**
1	D3.3V1_CSI	+3.3V Power Supply	Power
2	I2C0_SDA_M2	I2C serial interface data, connect to (U1) V4H I2C0	I/O
3	I2C0_SCL_M2	I2C serial interface clock output, connect to (U1) V4H I2C0	O
4	GND	Ground	Power
5	NC		-
6	MSIOF2_RXD	MSIOF2 receive data pin of (U1) V4H	I
7	GND	Ground	Power
8	DSI0_DATAP3	Positive D-PHY Differential Data Line3 of (U1) V4H	O
9	DSI0_DATAN3	Negative D-PHY Differential Data Line3 of (U1) V4H	O
10	GND	Ground	Power
11	DSI0_DATAP2	Positive D-PHY Differential Data Line2 of (U1) V4H	O
12	DSI0_DATAN2	Negative D-PHY Differential Data Line2 of (U1) V4H	O
13	GND	Ground	Power
14	DSI0_CLKP	Positive D-PHY Differential Clock Line of (U1) V4H	O
15	DSI0_CLKN	Negative D-PHY Differential Clock Line of (U1) V4H	O
16	GND	Ground	Power
17	DSI0_DATAP1	Positive D-PHY Differential Data Line1 of (U1) V4H	O
18	DSI0_DATAN1	Negative D-PHY Differential Data Line1 of (U1) V4H	O
19	GND	Ground	Power
20	DSI0_DATAP0	Positive D-PHY Differential Data Line0 of (U1) V4H	O
21	DSI0_DATAN0	Negative D-PHY Differential Data Line0 of (U1) V4H	I/O
22	GND	Ground	Power

2.9 Video Input Interfaces

The Sparrow Hawk board includes two FPC connectors for camera input, compatible with MIPI CSI-2 (Camera Serial Interface 2) interface signals. These connectors support dual camera modules for advanced image processing applications.

2.9.1. MIPI CSI Interface Connector (J1, J2)
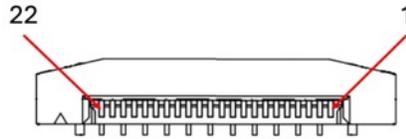
- **J1,J2** : Molex 525592253, **FFC/FPC Connector**. 0.50mm Pitch, Slider Series, Vertical, 3.90mm Height, 22 Circuits, Gold Plating.

Table 17. MIPI CSI0 Connector (J1) Pin Assignment

J1			
Pin	**Signal**	**Description**	**Type**
1	CAM_GND/GND	Ground	Power
2	CAM_D0_N/CSI0_DATAN0	Pixel Data Lane0 Negative, connect to (U1) V4H CSI0 D-PHY data lane 0 negative terminal.	I
3	CAM_D0_P/CSI0_DATAP0	Pixel Data Lane0 Positive, connect to (U1) V4H CSI0 D-PHY data lane 0 positive terminal.	I
4	CAM_GND/GND	Ground	Power
5	CAM_D1_N/CSI0_DATAN1	Pixel Data Lane1 Negative, connect to (U1) V4H CSI0 D-PHY data lane 1 negative terminal.	I
6	CAM_D1_P/CSI0_DATAP1	Pixel Data Lane1 Positive, connect to (U1) V4H CSI0 D-PHY data lane 1 positive terminal.	I
7	CAM_GND/GND	Ground	Power
8	CAM_CK_N/CSI0_CLKN	Pixel Clock Output from Sensor Negative, connect to (U1) V4H CSI0 D-PHY clock lane negative terminal.	I
9	CAM_CK_P/CSI0_CLKP	Pixel Clock Output from Sensor Positive, connect to (U1) V4H CSI0 D-PHY clock lane positive terminal.	I
10	CAM_GND/GND	Ground	Power
11	CAM_D2_N/CSI0_DATAN2	Pixel Data Lane2 Negative, connect to (U1) V4H CSI0 D-PHY data lane 2 negative terminal.	I
12	CAM_D2_P/CSI0_DATAP2	Pixel Data Lane2 Positive, connect to (U1) V4H CSI0 D-PHY data lane 2 positive terminal.	I
13	CAM_GND/GND	Ground	Power
14	CAM_D3_N/CSI0_DATAN3	Pixel Data Lane3 Negative, connect to (U1) V4H CSI0 D-PHY data lane 3 negative terminal.	I

| 15	CAM_D3_P/CSI0_DATAP3	Pixel Data Lane3 Positive, connect to (U1) V4H CSI0 D-PHY data lane 3 positive terminal.	I
16	CAM_GND/GND	Ground	Power
17	CAM_IO0/GP0_01	Power Enable	O
18	NC	-	-
19	CAM_GND/GND	Ground	Power
20	CAM_SCL/I2C1_SCL_CAM_CN0	I2C serial interface clock output, connect to (U1) V4H I2C1	O
21	CAM_SDA/I2C1_SDA_CAM_CN0	I2C serial interface data I/O, connect to (U1) V4H I2C1	I/O
22	CAM_3V3/D3.3V1_CSI	+3.3V Power Supply	Power

Table 18. MIPI CSI1 Connector (J2) Pin Assignment

J2			
Pin	Signal	Description	Type
1	CAM_GND/GND	Ground	Power
2	CAM_D0_N/CSI1_DATAN0	Pixel Data Lane0 Negative, connect to (U1) V4H CSI1 D-PHY data lane 0 negative terminal.	I
3	CAM_D0_P/CSI1_DATAP0	Pixel Data Lane0 Positive, connect to (U1) V4H CSI1 D-PHY data lane 0 positive terminal.	I
4	CAM_GND/GND	Ground	Power
5	CAM_D1_N/CSI1_DATAN1	Pixel Data Lane1 Negative, connect to (U1) V4H CSI1 D-PHY data lane 1 negative terminal.	I
6	CAM_D1_P/CSI1_DATAP1	Pixel Data Lane1 Positive, connect to (U1) V4H CSI1 D-PHY data lane 1 positive terminal.	I
7	CAM_GND/GND	Ground	Power
8	CAM_CK_N/CSI1_CLKN	Pixel Clock Output from Sensor Negative, connect to (U1) V4H CSI1 D-PHY clock lane negative terminal.	I
9	CAM_CK_P/CSI1_CLKP	Pixel Clock Output from Sensor Positive, connect to (U1) V4H CSI1 D-PHY clock lane positive terminal.	I
10	CAM_GND/GND	Ground	Power
11	CAM_D2_N/CSI1_DATAN2	Pixel Data Lane2 Negative, connect to (U1) V4H CSI1 D-PHY data lane 2 negative terminal.	I
12	CAM_D2_P/CSI1_DATAP2	Pixel Data Lane2 Positive, connect to (U1) V4H CSI1 D-PHY data lane 2 positive terminal.	I
13	CAM_GND/GND	Ground	Power
14	CAM_D3_N/CSI1_DATAN3	Pixel Data Lane3 Negative, connect to (U1) V4H CSI1 D-PHY data lane 3 negative terminal.	I
15	CAM_D3_P/CSI1_DATAP3	Pixel Data Lane3 Positive, connect to (U1) V4H CSI1 D-PHY data lane 3 positive terminal.	I
16	CAM_GND/GND	Ground	Power
17	CAM_IO0/GP0_02	Power Enable, connect to (U1) V4H GP0_02	O
18	NC		-

19	CAM_GND/GND	Ground	Power
20	CAM_SCL/I2C2_SCL_CAM_CN1	I2C serial interface clock output, connect to (U1) V4H I2C2	O
21	CAM_SDA/I2C2_SDA_CAM_CN1	I2C serial interface data I/O, connect to (U1) V4H I2C2	I/O
22	CAM_3V3/D3.3V1_CSI	+3.3V Power Supply	Power

2.10 Storage Interface

The Sparrow Hawk board features a MicroSD card slot for external storage, supporting SD, SDHC, and SDXC SD memory card types.

2.10.1. MicroSD Card Connector (CN1)
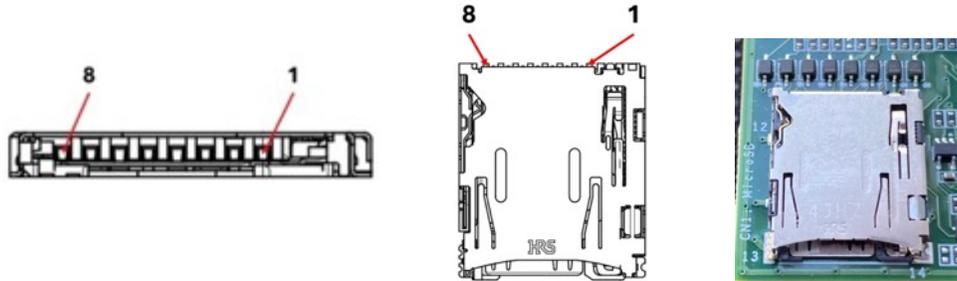
- **CN1** : Hirose DM3AT-SF-PEJM5, MICROSD Card Connectors, 8 Contact, 1 Row, 1.1 mm Pitch, SMD/SMT , PUSH-PUSH

Table 19. MicroSD Card Connector (CN1) Pin Assignment

CN1			
Pin	Signal	Description	Type
1	DATA2	Data line 2. Used for 4-bit SD bus. Connect to (U1) V4H MMC_SD_D2	I/O
2	CD/DATA3	Card Detect / Data line 3. Chip select in SPI / Data in SD. Connect to (U1) V4H MMC_SD_D3	I/O
3	CMD	Command/Response. Command line / SPI data input. Connect to (U1) V4H MMC_SD_CMD	I/O
4	VDD	+3.3V Power Supply	Power
5	CLK	Clock signal. Connect to (U1) V4H MMC_SD_CLK	I/O
6	GND	Ground	Power
7	DATA0	Data line 0. Main data line. Connect to (U1) V4H MMC_SD_D0	I/O
8	DATA1	Data line 1. Used for 4-bit SD bus. Connect to (U1) V4H MMC_SD_D1	I/O

2.11 CAN Interface

The Sparrow Hawk board includes a CAN (Controller Area Network) interface, supporting two CAN-FD channels via a 6-pin header. This allows connection to automotive and industrial networks using differential signaling.

2.11.1. CAN Bus Connector (CONN2)
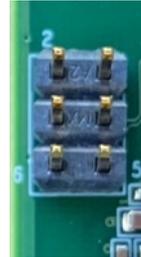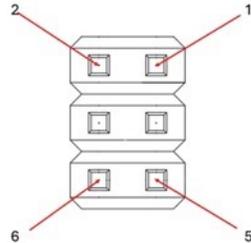
- **CONN2** :   Molex 10897060, 2.54mm Pitch C-Grid Breakaway Header, Dual Row, Vertical, High Temperature, 6 Circuits, 0.76µm Gold (Au) Selective Plating, Tin (Sn) PC Tail Plating, 2.72mm PC Tail

Table 20. CAN Bus Connector (CONN2) Pin Assignment

CONN2			
Pin	Signal	Description	Type
1	CAN1L	CAN-FD Low-Level Voltage I/O, differential signals for (U1) V4H CANFD4	I/O
2	CAN0L	CAN-FD Low-Level Voltage I/O, differential signals for (U1) V4H CANFD3	I/O
3	GND	Ground	Power
4	GND	Ground	Power
5	CAN1H	CAN-FD High-Level Voltage I/O, differential signals for (U1) V4H CANFD4	I/O
6	CAN0H	CAN-FD High-Level Voltage I/O, differential signals for (U1) V4H CANFD3	I/O

2.12 Power, JTAG, and other interfaces

This section describes the power control options and JTAG debugging interface for the Sparrow Hawk board. It includes the ACC power switch, power jumper, USB power input, JTAG header, and fan power control.

2.12.1. ACC Power Switch (SW1)

The ACC power switch controls system power-on/off behavior.

Table 21. ACC Power Switch Mode (SW1)

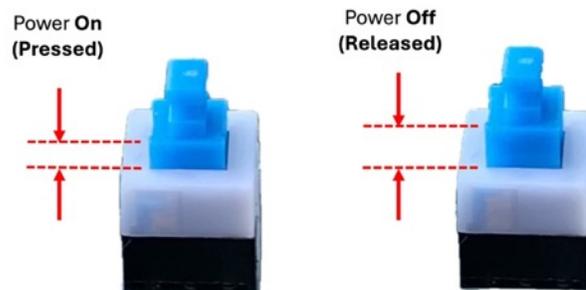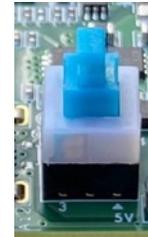| SW1		
Signal	**Mode of Operation**	
Status	ON	Initial power on
	OFF	Power off

Figure 6. ACC Power ON/OFF illustration

*Notes:

● Always ensure the ACC power switch **(SW1)** is OFF before plugging in or unplugging the AC adapter.

● Never connect the power adapter while **SW1** is in the ON position.

2.12.2. Power ON/OFF Jumper (CONN1)

The **CONN1** jumper selects the power-on control method for the board. It determines whether system startup is controlled by the ACC power switch (**SW1**) or automatically triggered upon USB power connection.

Table 22. Power ON/OFF Jumper (CONN1)

CONN1		
Jumper		**Power Control Behavior**
Status	OPEN	Power is controlled manually via the ACC power switch (**SW1**). The system powers on only when **SW1** is switched ON.
	SHORT	Power-on is automatically triggered when a USB PD charger is connected to the **USB1**. The ACC power switch (**SW1**) is bypassed.

2.12.3. USB Power Delivery Connector (USB1)

The Sparrow Hawk board receives power via a USB Type-C connector (USB1) that supports USB Power Delivery (PD) negotiation. This connector enables flexible power management and efficient system startup without external switches when configured appropriately (see Section 2.12.2).

Power Specification

● **Voltage**: 20 V (via USB PD)

● **Current**: 3A to 5A

● **Power Range**: 60W to 100W
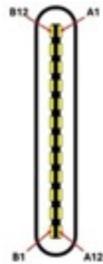
● **USB1** : TECHBEST USB3.1_24_Type-C, USB3.1 Type C, Female, 24 pins, upright. SMT

Table 23. USB3.0 Type C Connector (USB1) Pin Assignment

USB1			
Pin	Signal	Description	Type
A1	GND	Ground	Power
A2	NC	No Connection	-
A3	NC	No Connection	-
A4	VBUS	+5.0~20V Power Supply	Power
A5	CC1	Configuration Channel 1, Analog pin from CC-PHY of (U20) R9A02G011	I/O
A6	NC	No Connection	-
A7	NC	No Connection	-
A8	NC	No Connection	-
A9	VBUS	+5.0~20V Power Supply	Power
A10	NC	No Connection	-
A11	NC	No Connection	-
A12	GND	Ground	Power
B1	GND	Ground	Power
B2	NC	No Connection	-
B3	NC	No Connection	-
B4	VBUS	+5.0~20V Power Supply	Power

B5	CC2	Configuration Channel 2, Analog pin from CC-PHY of (U20) R9A02G011	I/O
B6	NC	No Connection	-
B7	NC	No Connection	-
B8	NC	No Connection.	-
B9	VBUS	+5.0~20V Power Supply	Power
B10	NC	No Connection	-
B11	NC	No Connection	-
B12	GND	Ground	Power

2.12.4. JTAG Connector (CN3)

The Sparrow Hawk board includes a 20-pin JTAG connector for debugging, boundary scan, and low-level firmware development.
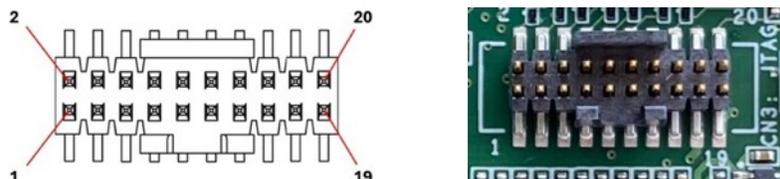

- **CN3** : SAMTEC FTSH-110-01-L-DV-K, 20 Pins, 1.27mm Pitch, 10 u" Gold on post, Matte Tin on tail, Double Row, Vertical, Keying Shroud for mating with FFSD.

Table 24. JTAG Connector (CN3) Pin Assignment

CN3			
Pin	**Signal**	**Description**	**Type**
1	D1.8V	+1.8V Power Supply	Power
2	TMS_18	DCUTMS. Debug mode selection, connect to (U1) V4H	I
3	GND	Ground.	Power
4	TCK_18	DCUTCK_LPDCLK. Debug clock, connect to (U1) V4H	I
5	GND	Ground.	Power
6	TDO_18	DCUTDO_LPDO. Debug data output, connect to (U1) V4H	O
7	NC	-	-
8	TDI_18	DCUTDI_LPDI. Debug data input, connect to (U1) V4H	I
9	GND	Ground.	Power
10	PRESETN_18	PRESET. Power-on-reset The low-level input on this pin places the V4H in the power-on-reset state.	I
11	NC	-	-
12	RDYn_18	DCURDY. Debug ready, connect to (U1) V4H	O
13	NC	-	-
14	NC	-	-
15	GND	Ground.	Power
16	TRSTn_18	DCUTRST. Debug reset, connect to (U1) V4H	I
17	GND	Ground.	Power
18	NC	-	-
19	GND	Ground.	Power
20	GND	Ground.	Power

2.12.5. FAN Control Connector (J3)

The Sparrow Hawk board includes a 4-pin fan connector to provide cooling for the SoC and other heat-generating components. This connector supplies regulated 5V power and supports PWM (Pulse Width Modulation) fan speed control as well as tachometer feedback for real-time RPM monitoring.
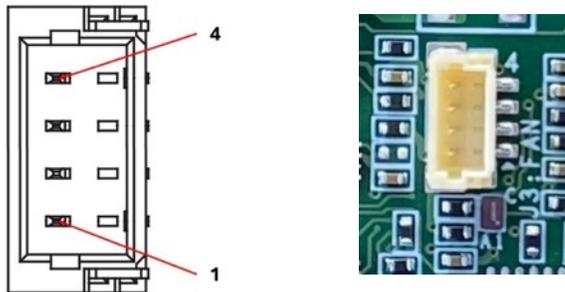
- **J3** : JST BM04B-SRSS-TB, Headers & Wire Housings, 4 Pins, 1.0 mm Pitch, Single Row, SMT,

Table 25. FAN Power Connector (J3) Pin Assignment

J3			
Pin	**Signal**	**Description**	**Type**
1	5V/VSYS	+5V Power Supply	Power
2	PWM/ HSCIF0_HSCK0	PWM Signal, connected to (U1)V4H GP1_15	O
3	GND	Ground	Power
4	TACH/ FAN_SENSE	FAN_SENSE, connected to (U1)V4H GP2_03	I

2.13 Reset Button (SW3)

The Sparrow Hawk board includes a manual reset button for the SoC, allowing developers to trigger a system reset without removing power.

The reset button **(SW3)** is connected to the MR_N input of the RESET IC (U12), which drives the PRESET# signal of the Renesas R-Car V4H SoC. Pressing this button triggers a hardware reset of the SoC, returning it to its default startup state.

*Note: This reset does not affect external devices or board power — only the SoC is reset.