Highlander 80 Hardware Specification

[Notes regarding this document]

1. Please use this product in temperature environment of 0 degrees - 45 degrees.

2. This board is not designed to prevent influence by radioactive rays.

3. Products and the specifications contained in this document are subject to change without notice.

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7. Some parts of the diagrams used in this document may differ from the actual substance.

8. This board is made for evaluation before product development. Please ensure that the board will not be installed on any product. Renesas Solutions Corporation cannot predict all potential conditions or misuse which may cause danger. Therefore, the cautions and warnings contained in this document do not cover every conceivable danger. Please use this board correctly and safely in a responsible manner.

[Revision record]

[Contents]

【Introduction】

This board applies to the Highlander80 from Renesas Solutions Corporation which uses the RISC SH7780 microcomputer from Renesas Technology Corp.

The basic composition of this platform serves as the main board in which SH7780 was carried, SH bus add-in board, a PCI bus add-in board, a board for debugging, and a back-plane board.

The model name of each board is as follows.

SH7780 main board: R7780RP-1

PCI bus add-in board: RPCIRP-1

SH bus add-in board: RSOUNDRP-1(Option)

Debugging board: RDBRP-1

Back-plane board: RMAIN_BWBRP-1+ RSUB_BWBRP-1

This manual indicates the hardware composition, the main function, and its usage of each board.

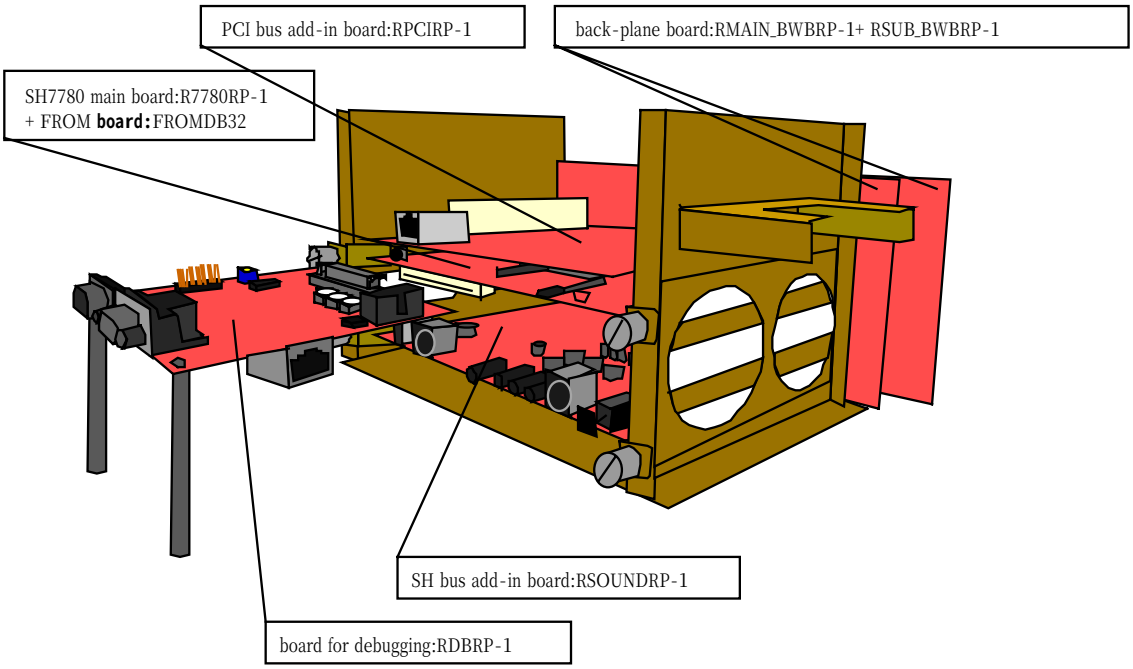


Figure1 - 1 The example of Highlander80 composition

【R7780RP-1】

1. Scope

This board applies to the R7780RP-1 from Renesas Solutions Corporation which uses the RISC SH7780 microcomputer from Renesas Technology Corp.

2. System Configuration

Figure 2-1 shows the system configuration.

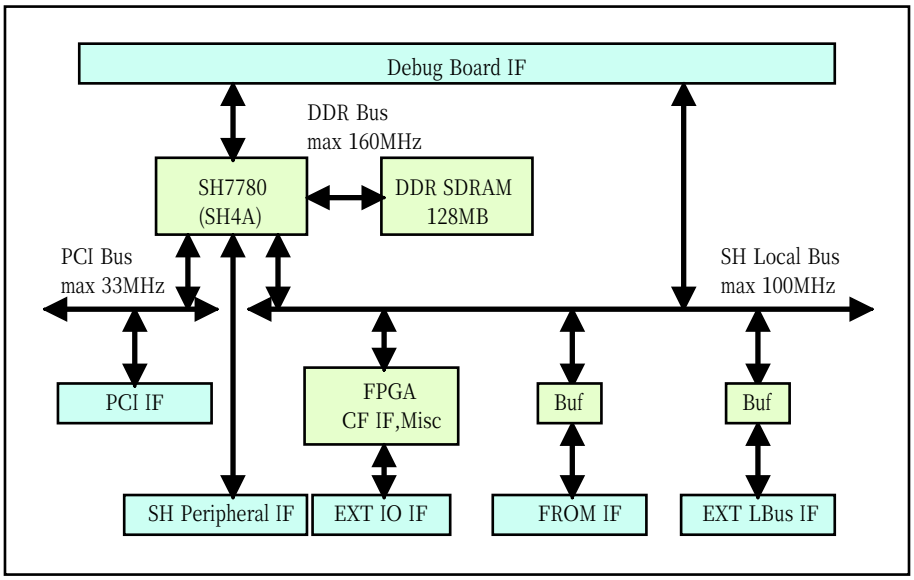


Figure2-1 R7780RP-1System Configuration

3. Connector Specification

Figure 3-1 shows the allocation of parts. Table 3-1 shows a list of connectors. The specifications are described below.

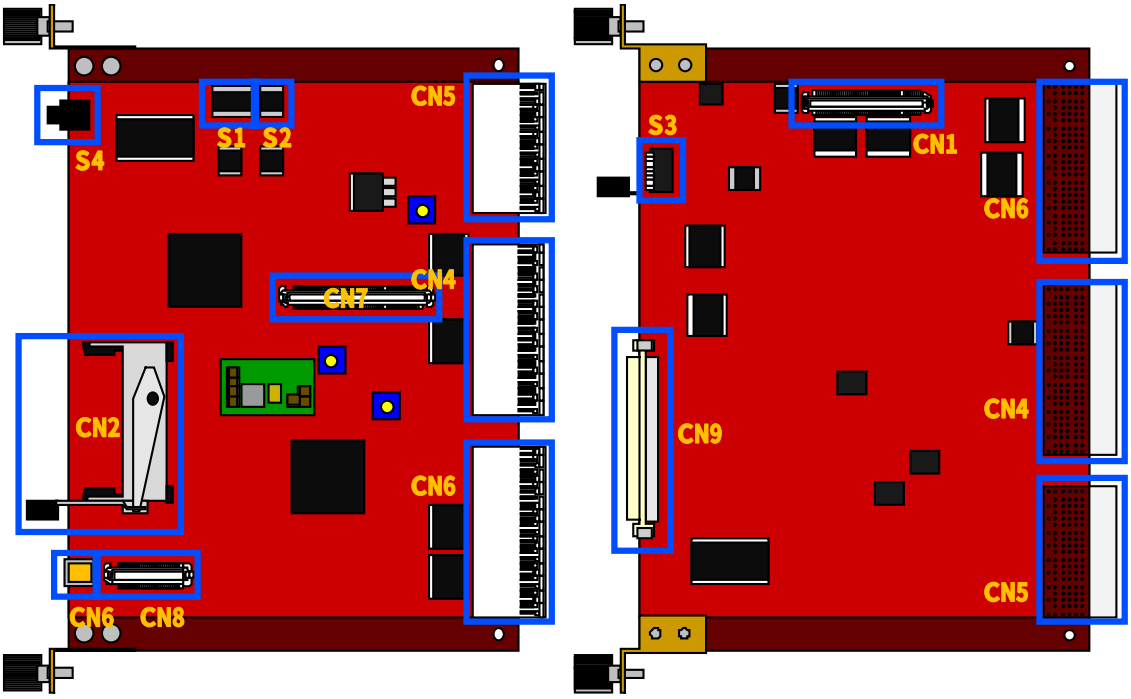


Figure 3-1 Parts Allocation

Table3-1 List of Connectors

Ref No.	Function	Note	Ref No.	Function	Note
CN1	FROM Board IF		CN6	USB	Serial
CN2	CF Card IF		CN7	PCI Board IF A	PCI BUS
CN3	External Expansion IF A	CPU_BUS	CN8	PCI Board IF B	PCI BUS
CN4	External Expansion IF B	CPU_BUS	CN9	Debug Board IF	
CN5	External Expansion IF C	Peripheral			

3.1 FROM Board Connection

CN1 is a connector to FROM board. The pin assignment specifications are as follows:

Connector type:52760-1009 Manufacturer: Molex					
Pin No.	Signal	Function	Pin No.	Signal	Function
1	+5V	Supply +5.0V	2	+3.3V	Supply +3.3V
3	GND	Ground	4	GND	Ground
5	D0	Data	6	D16	Data
7	D1	Data	8	D17	Data
9	D2	Data	10	D18	Data
11	D3	Data	12	D19	Data
13	D4	Data	14	D20	Data
15	D5	Data	16	D21	Data
17	D6	Data	18	D22	Data
19	D7	Data	20	D23	Data
21	D8	Data	22	D24	Data
23	D9	Data	24	D25	Data
25	+5V	Supply +5.0V	26	+3.3V	Supply +3.3V
27	GND	Ground	28	GND	Ground
29	D10	Data	30	D26	Data
31	D11	Data	32	D27	Data
33	D12	Data	34	D28	Data
35	D13	Data	36	D29	Data
37	D14	Data	38	D30	Data
39	D15	Data	40	D31	Data
41	A0	Address	42	A13	Address
43	A1	Address	44	A14	Address
45	A2	Address	46	A15	Address
47	A3	Address	48	A16	Address
49	+5V	Supply +5.0V	50	+3.3V	Supply +3.3V
51	GND	Ground	52	GND	Ground
53	A4	Address	54	A17	Address

55	A5	Address	56	A18	Address
57	A6	Address	58	A19	Address
59	A7	Address	60	A20	Address
61	A8	Address	62	A21	Address
63	A9	Address	64	A22	Address
65	A10	Address	66	A23	Address
67	A11	Address	68	A24	Address
69	A12	Address	70	A25	Address
71	+5V	Supply	72	+3.3V	Supply
73	GND	Ground	74	GND	Ground
75	WE0N	Write enable	76	CS0N	Chip select
77	WE1N	Write enable	78	NC	Not connected
79	WE2N	Write enable	80	CS2N	Chip select
81	WE3N	Write enable	82	CS3N	Chip select
83	GND	Ground	84	GND	Ground
85	RDN	Read	86	CS4N	Chip select
87	RD/WRN	Read/write	88	CS5N	Chip select
89	FLRDY	Ready	90	BSN	Bus start
91	RESETN	Reset	92	RDYN	Device ready
93	GND	Ground	94	CKIO	Clock
95	+5V	Supply +5.0V	96	+5V	Supply +5.0V
97	+3.3V	Supply +3.3V	98	+3.3V	Supply +3.3V
99	GND	Ground	100	GND	Ground

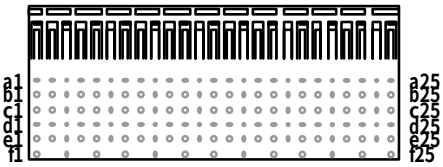
3.2 Connector for Compact Flash Card

CN2 is a Compact Flash Connector. The pin assignment specifications are as follows:

Connector type:ICM-MA50H-SS52-1151 Manufacturer: JST					
Pin No.	Signal	Function	Pin No.	Signal	Function
1	GND	Ground	26	-CD2	Card Detection
2	D3	Data	27	D11	Data
3	D4	Data	28	D12	Data
4	D5	Data	29	D13	Data
5	D6	Data	30	D14	Data
6	D7	Data	31	D15	Data
7	-CE1	Card Enable	32	-CE2	Card Enable
8	A10	Address	33	-VS1	Voltage detection
9	-OE	Output Enable	34	-IORD	I/O Read
10	A9	Address	35	-IOWR	I/O Write
11	A8	Address	36	-WE	Write Enable
12	A7	Address	37	IREQ	Interrupt
13	Vcc	Supply Vcc	38	Vcc	Supply Vcc
14	A6	Address	39	-CSEL	Cable Select
15	A5	Address	40	-VS2	Voltage detection
16	A4	Address	41	RESET	Reset
17	A3	Address	42	-WAIT	Wait
18	A2	Address	43	-INPACK	IN Port Acknowledge
19	A1	Address	44	-REG	Register Select
20	A0	Address	45	-SPKR	Audio Output
21	D0	Data	46	-STSCHG	Status Change
22	D1	Data	47	D8	Data
23	D2	Data	48	D9	Data
24	-IOIS16	16bit I/O	49	D10	Data
25	-CD1	Card Detection	50	GND	Ground

3.3 Connector for External Expansion

CN3 is connector to RMAIN_BWBRP-1. It connects with other board via RMAIN_BWBRP-1. The pin assignment specifications are as follows:



Connector type:PCN21A-125SB-2PF-G Manufacturer: HIROSE					
Pin No.	Signal	Function	Pin No.	Signal	Function
1a	+5V	Supply +5.0V	1b	+5V	Supply +5.0V
2a	GND	Ground	2b	GND	Ground
3a	EXT_INTBN	Interrupt B	3b	EXT_INTAN	Interrupt A
4a	VI_DATA0	Not connected	4b	VI_DATA1	Not connected
5a	VI_DATA5	Not connected	5b	VI_DATA6	Not connected
6a	GND	Ground	6b	GND	Ground
7a	HAC_SDATA_OUT	Tx Frame Serial Data	7b	HAC_SDATA_IN	Rx Frame Serial Data
8a	PCIBO_INT0N	Not connected	8b	PCIBO_INT1N	Not connected
9a	PCIB_CSSDN	Not connected	9b	PCIBCSPCN	Not connected
10a	GND	Ground	10b	SSI_RSTN	Module Reset
11a	SH_CKIO	Clock	11b	GND	Ground
12a	GND	Ground	12b	SH_D2	Data
13a	SH_D4	Data	13b	GND	Ground
14a	GND	Ground	14b	SH_D7	Data
15a	SH_D9	Data	15b	GND	Ground
16a	GND	Ground	16b	SH_D12	Data
17a	SH_D14	Data	17b	GND	Ground
18a	GND	Ground	18b	SH_D17	Data
19a	SH_D19	Data	19b	GND	Ground
20a	GND	Ground	20b	SH_D22	Data
21a	SH_D24	Data	21b	GND	Ground
22a	GND	Ground	22b	SH_D27	Data
23a	SH_D29	Data	23b	GND	Ground
24a	GND	Ground	24b	GND	Ground
25a	+5V	Supply	25b	+5V	Supply

Connector type:PCN21A-125SB-2PF-G Manufacturer: HIROSE					
Pin No.	Signal	Function	Pin No.	Signal	Function
1c	+5V	Supply +5.0V	1d	+5V	Supply +5.0V
2c	GDN	Ground	2d	GDN	Ground
3c	EX_RSTN	Reset Out	3d	VI_HSYNC	Not connected
4c	VI_DATA2	Not connected	4d	VI_DATA3	Not connected
5c	VI_DATA7	Not connected	5d	VI_CLK	Not connected
6c	GND	Ground	6d	GND	Ground
7c	HAC_SYNC	HAC Sync Signal	7d	HAC_BITCLK	HAC Clock
8c	PCIBO_INT2N	Not connected	8d	PCIBO_INT3N	Not connected
9c	PCIB_CSREGN	Not connected	9d	PCIB_RSTN	Not connected
10c	GND	Ground	10d	SSI_SCK0	SSI Clock
11c	SH_D0	Data	11d	GND	Ground
12c	GND	Ground	12d	SH_D3	Data
13c	SH_D5	Data	13d	GND	Ground
14c	GND	Ground	14d	SH_D8	Data
15c	SH_D10	Data	15d	GND	Ground
16c	GND	Ground	16d	SH_D13	Data
17c	SH_D15	Data	17d	GND	Ground
18c	GND	Ground	18d	SH_D18	Data
19c	SH_D20	Data	19d	GND	Ground
20c	GND	Ground	20d	SH_D23	Data
21c	SH_D25	Data	21d	GND	Ground
22c	GND	Ground	22d	SH_DF28	Data
23c	SH_D30	Data	23d	GND	Ground
24c	GND	Ground	24d	GND	Ground
25c	+5V	Supply +5.0V	25d	+5V	Supply +5.0V

Connector type:PCN21A-125SB-2PF-G Manufacturer: HIROSE					
Pin No.	Signal	Function	Pin No.	Signal	Function
1e	+5V	Supply +5.0V	1f	FDGND	Ground
2a	GND	Ground	2f	FDGND	Ground
3e	VI_VSYNC	Not connected	3f	FDGND	Ground
4e	VI_DATA4	Not connected	4f	FDGND	Ground
5e	VI_EN	Not connected	5f	FDGND	Ground
6e	GND	Ground	6f	FDGND	Ground
7e	HAC_RESN	Module Reset	7f	FDGND	Ground
8e	SSI_WS0	SSI Ward Select	8f	FDGND	Ground
9e	SSI_SDATA0	SSI Data	9f	FDGND	Ground
10e	GND	Ground	10f	FDGND	Ground
11e	SH_D1	Data	11f	FDGND	Ground
12e	GND	Ground	12f	FDGND	Ground
13e	SH_D6	Data	13f	FDGND	Ground
14e	GND	Ground	14f	FDGND	Ground
15e	SH_D11	Data	15f	FDGND	Ground
16e	GND	Ground	16f	FDGND	Ground
17e	SH_D16	Data	17f	FDGND	Ground
18e	GND	Ground	18f	FDGND	Ground
19e	SH_D21	Data	19f	FDGND	Ground
20e	GND	Ground	20f	FDGND	Ground
21e	SH_D26	Data	21f	FDGND	Ground
22e	GND	Ground	22f	FDGND	Ground
23e	SH_D31	Data	23f	FDGND	Ground
24e	GND	Ground	24f	FDGND	Ground
25e	+5V	Supply +5.0V	25f	FDGND	Ground

＊ HAC＝Audio Codec Interface (Audio Codec 97 (AC'97) Version 2.1)

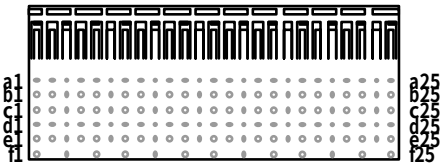
＊ SSI＝Serial Sound Interface

＊ VI＝Video Interface

＊ PCIB＝PCI Bus Bridge

3.4 Connector for External Expansion

CN4 is connector to RMAIN_BWBRP-1. It connects with other board via RMAIN_BWBRP-1. The pin assignment specifications are as follows:



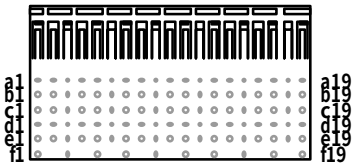
Connector type:PCN21A-125SB-2PF-G Manufacturer: HIROSE					
Pin No.	Signal	Function	Pin No.	Signal	Function
1a	+3.3V	Supply +3.3V	1b	+3.3V	Supply +3.3V
2a	GND	Ground	2b	GND	Ground
3a	SH_A21	Address	3b	SH_A22	Address
4a	SH_A16	Address	4b	SH_A17	Address
5a	GND	Ground	5b	GND	Ground
6a	SH_A11	Address	6b	SH_A12	Address
7a	SH_A6	Address	7b	SH_A7	Address
8a	GND	Ground	8b	GND	Ground
9a	SH_A1	Address	9b	SH_A2	Address
10a	GND	Ground	10b	GND	Ground
11a	GDN	Ground	11b	SH_WE3N	Write Enable
12a	SH_WE0N	Write Enable	12b	GND	Ground
13a	GND	Ground	13b	SH_RDWEN	Read Write
14a	EXT_WAITB	External Wait	14b	GND	Ground
15a	EX_WAITA	External Wait	15b	EX_CSB	External Chip Select
16a	SH_DACK0	DMA Acknowledge	16b	SH_DACK1	DMA Acknowledge
17a	USB20_RSTN	USB_IC Reset	17b	SH_DREQ0	DMA Request
18a	GND	Ground	18b	GND	Ground
19a	USB20_CSN	USB Chip Select	19b	USB20_INTN	USB Interrupt
20a	USB20_SD5	USB Data	20b	USB20_SD6	USB Data
21a	USB20_SD0	USB Data	21b	USB20_SD1	USB Data
22a	GND	Ground	22b	IF_ID0	Not connected
23a	IF_ID2	Not connected	23b	IF_ID3	Not connected
24a	SD_CS1N	SD Chip Select	24b	SD_CS2N	SD Chip Select
25a	+3.3V	Supply +3.3V	25b	+3.3V	Supply +3.3V

Connector type:PCN21A-125SB-2PF-G Manufacturer: HIROSE					
Pin No.	Signal	Function	Pin No.	Signal	Function
1c	+3.3V	Supply +3.3V	1d	+3.3V	Supply +3.3V
2c	GND	Ground	2d	GND	Ground
3c	SH_A23	Address	3d	SH_A24	Address
4c	SH_A18	Address	4d	SH_A19	Address
5c	GND	Ground	5d	GND	Ground
6c	SH_A13	Address	6d	SH_A14	Address
7c	SH_A8	Address	7d	SH_A9	Address
8c	GND	Ground	8d	GND	Ground
9c	SH_A3	Address	9d	SH_A4	Address
10c	GND	Ground	10d	GND	Ground
11c	GND	Ground	11d	SH_BSN	Bus Start
12c	SH_WE1N	Write	12d	GND	Ground
13c	GND	Ground	13d	SH_RDN	Read
14c	I2C_SDA	IIC Data	14d	GND	Ground
15c	GND	Ground	15d	EX_CSA	External Chip Select
16c	SH_DACK2	DMA Acknowledge	16d	SH_DACK3	DMA Acknowledge
17c	SH_DREQ1	DMA Request	17d	SH_DREQ2	DMA Request
18c	USB20_SOEN	Not connected	18d	GND	Ground
19c	SH_BREQN	Bus Request	19d	SH_BACKN	Bus Acknowledge
20c	USB20_SD7	USB Data	20d	USB20_DEND1N	USB Data Enable
21c	USB20_SD2	USB Data	21d	USB20_SD3	USB Data
22c	IVDR0	Not connected	22d	IF_ID1	Not connected
23c	PW_ID0	Not connected	23d	PW_ID1	Not connected
24c	SD_INTN	SD Card Interrupt	24d	SD_RSTN	SD Card Reset
25c	+3.3V	Supply +3.3V	25d	+3.3V	Supply +3.3V

Connector type:PCN21A-125SB-2PF-G Manufacturer: HIROSE					
Pin No.	Signal	Function	Pin No.	Signal	Function
1e	+3.3V	Supply +3.3V	1f	FDGND	Ground
2a	GND	Ground	2f	FDGND	Ground
3e	SH_A25	Address	3f	FDGND	Ground
4e	SH_A20	Address	4f	FDGND	Ground
5e	GND	Ground	5f	FDGND	Ground
6e	SH_A15	Address	6f	FDGND	Ground
7e	SH_A10	Address	7f	FDGND	Ground
8e	GND	Ground	8f	FDGND	Ground
9e	SH_A5	Address	9f	FDGND	Ground
10e	SH_A0	Address	10f	FDGND	Ground
11e	GND	Ground	11f	FDGND	Ground
12e	SH_WE2N	Write Enable	12f	FDGND	Ground
13e	GND	Ground	13f	FDGND	Ground
14e	I2C_SCL	IIC Clock	14f	FDGND	Ground
15e	GND	Ground	15f	FDGND	Ground
16e	SH_EXCPUCS0N	Not connected	16f	FDGND	Ground
17e	SH_DREQ3	DMA Request	17f	FDGND	Ground
18e	GND	Ground	18f	FDGND	Ground
19e	SH_DACK0	DMA Acknowledge	19f	FDGND	Ground
20e	USB20_DEN0N	USB Data Enable	20f	FDGND	Ground
21e	USB20_SD4	USB Data	21f	FDGND	Ground
22e	GND	Ground	22f	FDGND	Ground
23e	IVDR_PWR_ON	Not connected	23f	FDGND	Ground
24e	SD_PE	SD Power Control	24f	FDGND	Ground
25e	+3.3V	Supply +3.3V	25f	FDGND	Ground

3.5 Connector for External Expansion

CN5 is connector to RMAIN_BWBRP-1. It connects with other board via RMAIN_BWBRP-1. The pin assignment specifications are as follows:



Connector type:PCN21A-95SB-2PF-G Manufacturer: HIROSE					
Pin No.	Signal	Function	Pin No.	Signal	Function
1a	AN_GND	Not connected	1b	SH_HSYNC	Not connected
2a	SH_VSYNC	Not connected	2b	AN_GND	Not connected
3a	GND	Ground	3b	TP_CSN	Touch Panel Select
4a	IDENT0	Extension ID	4b	TP_IRQN	Touch Panel Interrupt
5a	IDENT1	Extension ID	5b	EXT_GPIO3	Extension GPIO
6a	IDENT2	Extension ID	6b	EXT_GPIO7	Extension GPIO
7a	SSI_SCK	Not connected	7b	GND	Ground
8a	GND	Ground	8b	SSI_CLK	Not connected
9a	TFT_R3	Not connected	9b	GND	Ground
10a	TFT_G2	Not connected	10b	TFT_G1	Not connected
11a	TFT_B1	Not connected	11b	TFT_B0	Not connected
12a	GND	Ground	12b	TFT_B5	Not connected
13a	TFT_DOTCLK	Not connected	13b	GND	Ground
14a	TFT_VDD	Not connected	14b	TFT_VDD	Not connected
15a	GND	Ground	15b	RESET_LED	POW_ON Reset
16a	CAN_ERRN	Not connected	16b	GND	Ground
17a	GND	Ground	17b	SCI_SCK9	Not connected
18a	SH_GPIO28	Not connected	18b	SH_GPIO27	Not connected
19a	GND	Ground	19b	GPS_IN	Not connected

Connector type:PCN21A-95SB-2PF=G Manufacturer: HIROSE					
Pin No.	Signal	Function	Pin No.	Signal	Function
1c	AN_GND	Not connected	1d	SH_R	Not connected
2c	SH_B	Not connected	2d	AN_GND	Not connected
3c	GND	Ground	3d	TP_CLK	Touch Panel Clock
4c	TP_DOUT	Touch Panel Data Out	4d	TP_BUSY	Touch Panel Busy
5c	EXT_GPIO2	Extension GPIO	5d	EXT_GPIO1	Extension GPIO
6c	EXT_GPIO6	Extension GPIO	6d	EXT_GPIO2	Extension GPIO
7c	SCI_SCK0	Serial Clock	7d	SCI_TX0	Serial Data Out
8c	GND	Ground	8d	SSI_WS	Not connected
9c	TFT_R2	Not connected	9d	TFT_R1	Not connected
10c	TFT_G0	Not connected	10d	TFT_R5	Not connected
11c	TFT_G5	Not connected	11d	TFT_G4	Not connected
12c	TFT_B4	Not connected	12d	TFT_B3	Not connected
13c	TFT_ENB	Not connected	13d	TFT_VSYNC	Not connected
14c	TFT_VDD	Not connected	14d	TFT_BKLED_EN	Not connected
15c	CF/HDD_LED	CF_DASP	15d	TFT_CDE	Not connected
16c	CAN_RX	Not connected	16d	GND	Ground
17c	SCI_RX9	Not connected	17d	SCI_TX9	Not connected
18c	SH_GPIO26	Not connected	18d	SH_GPIO25	Not connected
19c	GPS_CLK	Not connected	19d	GND	Ground

Connector type:PCN21A-95SB-2PF=G Manufacturer: HIROSE					
Pin No.	Signal	Function	Pin No.	Signal	Function
1e	AN_GND	Not connected	1f	FDGND	Ground
2e	SH_G	Not connected	2f	FDGND	Ground
3e	GND	Ground	3f	FDGND	Ground
4e	TP_DIN	Touch Panel Data In	4f	FDGND	Ground
5e	EXT_GPIO0	Extension GPIO	5f	FDGND	Ground
6e	EXT _GPIO4	Extension GPIO	6f	FDGND	Ground
7e	SCI_RX0	Serial Data In	7f	FDGND	Ground
8e	SSI_DATA	Not connected	8f	FDGND	Ground
9e	TFT_R0	Not connected	9f	FDGND	Ground
10e	TFT_R4	Not connected	10f	FDGND	Ground
11e	TFT_G3	Not connected	11f	FDGND	Ground
12e	TFT_B2	Not connected	12f	FDGND	Ground
13e	GND	Ground	13f	FDGND	Ground
14e	TFT_HSYNC	Not connected	14f	FDGND	Ground
15e	TFT_CLAMP	Not connected	15f	FDGND	Ground
16e	CAN_TX	Not connected	16f	FDGND	Ground
17e	GND	Ground	17f	FDGND	Ground
18e	SH_GPIO24	Not connected	18f	FDGND	Ground
19e	SH_GPIO29	Not connected	19f	FDGND	Ground

3.6 Connector for USB

CN6 is USB mini B type connector. It has connected with CP2101EK via FPGA. The pin assignment specifications are as follows:

Connector type:54366-0418 Manufacturer: Molex					
Pin No.	Signal	Function	Pin No.	Signal	Function
1	VBUS	USB VBus	2	DM	D-
3	DP	D+	4	IP	Not connected
5	VSS	Ground	6	FG	Frame Ground

3.7 Connector for PCI bus add-in board

CN7 connects with a RPCIRP-1. The pin assignment specifications are as follows:

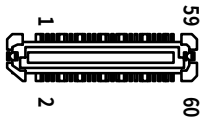
Connector type:52760-1209 Manufacturer: Molex					
Pin No.	Signal	Function	Pin No.	Signal	Function
1	GND	Ground	2	GND	Ground
3	PCI_CLK1	PCI Clock	4	GND	Ground
5	NC	Not connected	6	PCI_CLK2	PCI Clock
7	PCI_CLK3	PCI Clock	8	NC	Not connected
9	GND	Ground	10	PCI_CLK4	PCI Clock
11	GND	Ground	12	GND	Ground
13	PCI_RSTN	PCI Reset	14	PCI_C/BE0N	PCI C/BE
15	PCI_C/BE1N	PCI C/BE	16	PCI_C/BE2N	PCI C/BE
17	PCI_C/BE3N	PCI C/BE	18	PCI_PAR	PCI Parity
19	GND	Ground	20	GND	Ground
21	NC	Not connected	22	NC	Not connected
23	GND	Ground	24	GND	Ground
25	PCI_FRAMEN	PCI Cycle Frame	26	PCI_IRDYN	PCI initiator ready
27	PCI_TRDYN	PCI Target Ready	28	PCI_STOPN	PCI Cycle Stop
29	PCI_DEVSEL	PCI Device Select	30	PCI_LOCKN	PCI Lock
31	PCI_PERN	PCI Parity Error	32	PCI_SERRN	PCI System Error
33	GND	Ground	34	GND	Ground
35	PCI_REQ1N	PCI Bus Request	36	PCI_REQ2N	PCI Bus Request

37	PCI_REQ3N	PCI Bus Request	38	PCI_REQ4N	PCI Bus Request
39	PCI_GNT1N	PCI Bus Grant	40	PCI_GNT2N	PCI Bus Grant
41	PCI_GNT3N	PCI Bus Grant	42	PCI_GNT4N	PCI Bus Grant
43	GND	Ground	44	GND	Ground
45	PCI_AD0	PCI Address/Data	46	PCI_AD1	PCI Address/Data
47	PCI_AD2	PCI Address/Data	48	PCI_AD3	PCI Address/Data
49	PCI_AD4	PCI Address/Data	50	PCI_AD5	PCI Address/Data
51	PCI_AD6	PCI Address/Data	52	PCI_AD7	PCI Address/Data
53	GND	Ground	54	GND	Ground
55	PCI_AD8	PCI Address/Data	56	PCI_AD9	PCI Address/Data
57	PCI_AD10	PCI Address/Data	58	PCI_AD11	PCI Address/Data
59	PCI_AD12	PCI Address/Data	60	PCI_AD13	PCI Address/Data
61	PCI_AD14	PCI Address/Data	62	PCI_AD15	PCI Address/Data
63	GND	Ground	64	GND	Ground
65	+3.3V	Not connected	66	+3.3V	Not connected
67	GND	Ground	68	GND	Ground
69	PCI_AD16	PCI Address/Data	70	PCI_AD17	PCI Address/Data
71	PCI_AD18	PCI Address/Data	72	PCI_AD19	PCI Address/Data
73	PCI_AD20	PCI Address/Data	74	PCI_AD21	PCI Address/Data
75	PCI_AD22	PCI Address/Data	76	PCI_AD23	PCI Address/Data
77	GND	Ground	78	GND	Ground
79	PCI_AD24	PCI Address/Data	80	PCI_AD25	PCI Address/Data
81	PCI_AD26	PCI Address/Data	82	PCI_AD27	PCI Address/Data
83	PCI_AD28	PCI Address/Data	84	PCI_AD29	PCI Address/Data
85	PCI_AD30	PCI Address/Data	86	PCI_AD31	PCI Address/Data
87	GND	Ground	88	GND	Ground
89	IDSEL1	Initialization Device Select	90	IDSEL2	Initialization Device Select
91	IDSEL3	Initialization Device Select	92	IDSEL4	Initialization Device Select
93	NC	Not connected	94	NC	Not connected
95	NC	Not connected	96	NC	Not connected
97	GND	Ground	98	GND	Ground
99	+5V	Not connected	100	+5V	Not connected
101	GND	Ground	102	GND	Ground
103	NC	Not connected	104	NC	Not connected

105	NC	Not connected	106	NC	Not connected
107	NC	Not connected	108	NC	Not connected
109	NC	Not connected	110	POW_RESETN	Not connected
111	GND	Ground	112	GND	Ground
113	GND	Ground	114	GND	Ground
115	GND	Ground	116	GND	Ground
117	GND	Ground	118	GND	Ground
119	GND	Ground	120	GND	Ground

3.8 Connector for PCI bus add-in board

CN8 connects with RPCIRP-1. The pin assignment specifications are as follows:



Connector type:52760-0609 Manufacturer: Molex					
Pin No.	Signal	Function	Pin No.	Signal	Function
1	GND	Ground	2	GND	Ground
3	PCI_INTAN	PCI Interrupt A	4	PCI_INTBN	PCI Interrupt B
5	PCI_INTCN	PCI Interrupt C	6	PCI_INTDN	PCI Interrupt D
7	GND	Ground	8	GND	Ground
9	PCI_RSTN	PCI Reset	10	PCI_PRST_EXTN	PCI Board Information
11	GND	Ground	12	GND	Ground
13	TS_CLK	Not connected	14	GND	Ground
15	GND	Ground	16	TS_VLDA	Not connected
17	TS_SYNC	Not connected	18	GND	Ground
19	GND	Ground	20	TS_DATA	Not connected
21	TS_IOEN	Not connected	22	GND	Ground
23	GND	Ground	24	TS_DIR	Not connected
25	TS_ERR	Not connected	26	GND	Ground
27	GND	Ground	28	GND	Ground
29	IVDR0	IVDR Control	30	IVDR_PER_ON	IVDR Power Control
31	GND	Ground	32	GND	Ground
33	PW_ID0	IVDR Power ID	34	PW_ID1	IVDR Power ID
35	GND	Ground	36	GND	Ground
37	IF_ID0	IVDR Function ID	38	IF_ID1	IVDR Function ID

39	IF_ID2	IVDR Function ID	40	IF_ID3	IVDR Function ID
41	GND	Ground	42	GND	Ground
43	NC	Not connected	44	NC	Not connected
45	NC	Not connected	46	NC	Not connected
47	NC	Not connected	48	NC	Not connected
49	NC	Not connected	50	NC	Not connected
51	NC	Not connected	52	NC	Not connected
53	NC	Not connected	54	NC	Not connected
55	NC	Not connected	56	NC	Not connected
57	NC	Not connected	58	NC	Not connected
59	GND	Ground	60	GND	Ground

3.9 Debugging board connection

CN9 connects with RDBRP-1. The pin assignment specifications are as follows:

Connector type：BMF-100R Manufacturer：KEL					
Pin No.	Signal	Function	Pin No.	Signal	Function
1	+5V	Supply +5.0V	51	AX_WEN	ETHER IC Write
2	+5V	Supply +5.0V	52	AX_RDN	ETHER IC Read
3	GND	Ground	53	GND	Ground
4	GND	Ground	54	GND	Ground
5	DB_A12	Address	55	DB_DOTWEN	Dot LCD Write
6	DB_A10	Address	56	DB_MPMD	SH MODE9 Control
7	GND	Ground	57	DB_DOTCSN	Dot LCD Select
8	GND	Ground	58	DB_DOTRDN	Dot LCD Read/Write
9	DB_A9	Address	59	DB_CTS0	Modem Control
10	DB_A8	Address	60	DB_TX0	Serial Data Out
11	DB_A7	Address	61	DB_RTS0	Modem Control
12	DB_A6	Address	62	DB_RX0	Serial Data In
13	GND	Ground	63	GND	Ground
14	GND	Ground	64	GND	Ground
15	DB_A5	Address	65	DB_CRTHS	CRT Hsync
16	DB_A4	Address	66	DB_CRTVS	CRT Vsync
17	DB_A3	Address	67	DB_RED	CRT RED
18	DB_A2	Address	68	DB_GREEN	CRT GREEN
19	DB_A1	Address	69	DB_BLUE	CRT BLUE

20	GND	Ground	70	GND	Ground
21	GND	Ground	71	GND	Ground
22	GND	Ground	72	GND	Ground
23	DB_D15	Data	73	SH_PRSTN	Reset Out
24	DB_D14	Data	74	DB_JRSTN	Reset In
25	DB_D13	Data	75	DB_TMS	Mode Select
26	DB_D12	Data	76	DB_ASEBRKN	Break
27	GND	Ground	77	DB_TDI	Data In
28	GND	Ground	78	DB_TDO	Data Out
29	DB_D11	Data	79	DB_TCK	Clock
30	DB_D10	Data	80	DB_TRSTN	Reset
31	DB_D10	Data	81	DB_AUDCK	AUD Clock
32	DB_D9	Data	82	DB_AUDSYNCN	AUD Sync
33	GND	Ground	83	DB_AUDATA3	AUD Data
34	GND	Ground	84	DB_AUDATA2	AUD Data
35	DB_D7	Data	85	DB_AUDATA1	AUD Data
36	DB_D6	Data	86	DB_AUDATA0	AUD Data
37	DB_D5	Data	87	DB_PSW2	Push Switch
38	DB_D4	Data	88	DB_PSW1	Push Switch
39	GND	Ground	89	DB_PSW0	Push Switch
40	GND	Ground	90	DB_DSW3	Dip Switch
41	DB_D3	Data	91	DB_DSW2	Dip Switch
42	DB_D2	Data	92	DB_DSW1	Dip Switch
43	DB_D1	Data	93	DB_DSW0	Dip Switch
44	DB_D0	Data	94	DB_DCLK	FPGA JTAG Signal
45	GND	Ground	95	DB_NCS	FPGA JTAG Signal
46	GND	Ground	96	DB_NCE	FPGA JTAG Signal
47	AX_RSTN	ETHER IC Reset	97	DB_ASDO	FPGA JTAG Signal
48	AX_RDYN	ETHER IC Ready	98	DB_CONF_DONE	FPGA JTAG Signal
49	AX_IRQ	ETHER IC Interrupt	99	DB_NCONFIG	FPGA JTAG Signal
50	AX_CSN	ETHER IC Select	100	DB_DATA	FPGA JTAG Signal

4. Switch Specification

Table 4-1 shows the list of switches. The specifications are described below

Table4-1 List of Switches

Ref No.	Function	Note	Ref No.	Function	Note
S1	CPU Mode Set		S4	Reset SW	
S2	CPU Mode Set				
S3	Debug SW	Dip SW			

4.1 Switch for the CPU Mode Setting A

S1 is the switch for the operating mode setting of the SH7780. The allocation of each switch is listed below.

At shipment, MD3, MD4, MD5, MD6 and MD8 are set to High, High, High, High, Low, respectively: Area 0 is SRAM Interface / 32bit Bus width / Little Endian / PCI Host / Oscillator use

Switch No.	Connected pin	ON	OFF
S1-1	MODE3	H	L
S1-2	MODE4	H	L
S1-3	MODE5	H	L
S1-4	MODE6	H	L
S1-5	MODE8	H	L
S1-6	Not connected		
S1-7	Not connected		
S1-8	Not connected		

4.2 Switch for the CPU Mode Setting B

S2 is the switch for the operating mode setting of the SH7780. The allocation of each switch is listed below.

At shipment, MD0, MD1, MD2 and MD7 are set to low, low, low, low, respectively: Clock mode 0.

(CPU CLK=400MHz/DDR CLK=160MHz/CPU BUS CLK=100MHz)

Switch No.	Connected pin	ON	OFF
S2-1	MODE0	H	L
S2-2	MODE1	H	L
S2-3	MODE2	H	L
S2-4	MODE7	H	L

4.3 DIP Switch for Debugging

S4 is switch for debugging. The allocation of each switch is listed below. Switch status get in the register of FPGA.

Please refer to the FPGA section for the specifications.

Address:0500 0018 h supporting bits:Bit0-7

Switch No.	Connected pin	ON	OFF
S3-1	FPGA_SW0	H	L
S3-2	FPGA_SW1	H	L
S3-3	FPGA_SW2	H	L
S3-4	FPGA_SW3	H	L
S3-5	FPGA_SW4	H	L
S3-6	FPGA_SW5	H	L
S3-7	FPGA_SW6	H	L
S3-8	FPGA_SW7	H	L

5. LED Specification

Each LED function is shown below.

5.1 LED for the SH7780 Status

LED No.	Status
LED1	Off: Reset
	GREEN: Sleep
	RED: Standby
	YELLOW: Normal

5.2 LED for the Compact Flash

LED No.	Status
LED2	CF Power Supply
LED3	CF Insert
LED4	CF_DASP Mode

5.3 LEDs for Debugging

LEDs5-12 are for debugging. They are controllable through the general-purpose output ports of the FPGA.

Address:0500 0018 h supporting bits:Bit0-7

LED	Bit	0	1
LED5	0	OFF	ON
LED 6	1	OFF	ON
LED 7	2	OFF	ON
LED 8	3	OFF	ON
LED 9	4	OFF	ON
LED 10	5	OFF	ON
LED 11	6	OFF	ON
LED 12	7	OFF	ON

6. Reset Signal

The reset pins on the board are described in the following. Figure 6-1 shows the reset signal connections.

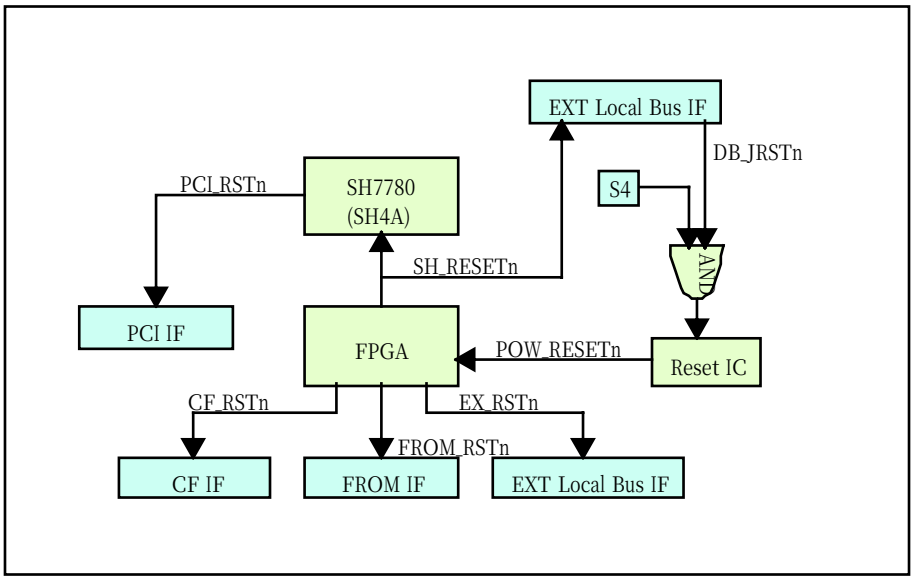


Figure 6-1 Connections to Reset Pins

6.1 Power-On Reset

Power-on reset inputs a reset signal on the device connected to the SuperH bus. The reference voltage is 3.3 V and is generated from the regulator. If the voltage falls below 2.93 V, a reset pulse will be generated.

The FPGA configuration starts on this board when the power is turned on. The reset pulse, which is input to the SH7780, will be input after the configuration of the FPGA. Figure 6-2 shows the power-on reset sequence.

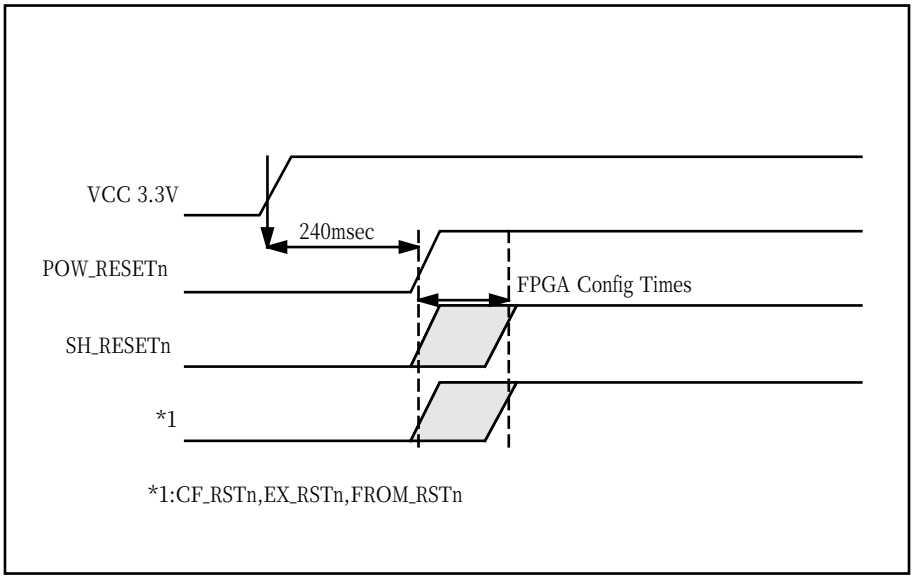


Figure6-2 Power-On Reset Sequence

6.2 System Reset

The system is reset by pressing the reset switch (S4). The reset pulse will occur for each device with the same timing as the system reset. Figure 6-3 shows the system reset sequence.

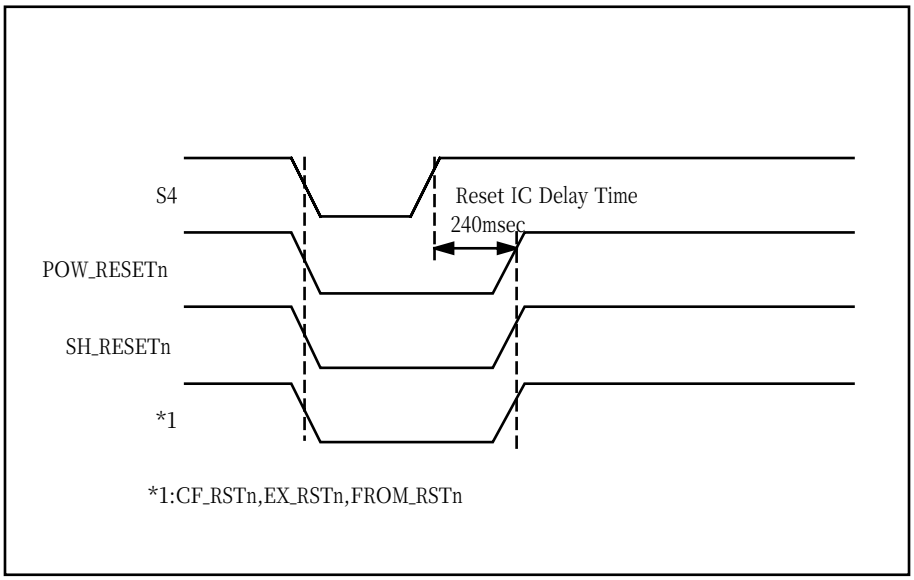


Figure6-3 System Reset Sequence

7. Memory Map

Table 7-1 shows the memory map of this board.

Table7-1 Memory Map

Area	Function	Bus Width(bit)	Address	Device	Note
0	FROM Area	32	0000 0000 - 01FF FFFF	M5M29KB/T641AVP M5M29KE131BVP	M5M29KB/T641AVP Use 32MB
			0200 0000 - 03FF FFFF	M5M29KB/T641AVP shadow M5M29KE131BVP	
1	FPGA , RSOUNDRP-1 Area	16	0400 0000 - 047F FFFF	TE4300	SD Card Controller
			0480 0000 - 04FF FFFF	M66596	USB2.0 Controller(Host)
			0500 0000 - 057F FFFF	FPGA	
			0580 0000 - 05FF FFFF	AX88796L	Ethernet Controller
			0600 0000 - 067F FFFF	SC1602BSLB	Character Dot LCD
			0680 0000 - 07FF FFFF	shadow	
2	DDR SDRAM Area	32	0800 0000 - 0BFF FFFF	EDD5116ADTA	

Area	Function	Bus Width(bit)	Address	Device	Note
3	DDR SDRAM Area	32	0C00 0000 - 0FFF FFFF	EDD5116ADTA	
4	External SH Bus Area A	8/16/32	1000 0000 - 13FF FFFF		
5	Compact Flash Area	16	1400 0000 - 1400 1FFF	CF CARD	
			1400 2000 - 17FF FFFF	CF shadow	
6	External SH Bus Area B	8/16/32	1800 0000 - 1BFF FFFF		

7.1 Area Overview

7.1.1 SH Bus area

The SH bus area is described below.

7.1.2 Area0

Area 0 is an FROM area, which is allocated to the expansion connector.

The bus width is 32 bits.

7.1.3 Area1

Area 1 is FPGA internal register, SD card Controller, USB Controller, Debug Board area. The bus width is 16 bits.

(For RSOUNDRP-1 area)

7.1.4 Area2

Area 2 is for the DDR SDRAM. 64 Mbytes are used. The bus width is 32 bits.

7.1.5 Area3

Area 3 is for the DDR SDRAM. 64 Mbytes are used. The bus width is 32 bits.

7.1.6 Area4

Area 4 is External SH Bus area. The bus width is 8 or 16 or 32 bits.

7.1.7 Area5

Area 5 is Compact Flash area. The bus width is 16 bits.

7.1.8 Area6

Area 6 is External SH Bus area. The bus width is 8 or 16 or 32 bits.

8. FPGA Specification

8.1 FPGA Functional Specifications

For the FPGA, the EP1C20 manufactured by Altera is used.

The FPGA performs the following functions.

1) Address decoding

2) SH7780 interrupts control

3) Peripheral device reset control

4) Compact Flash timing control

5) Compact Flash power-supply control

6) SD card power-supply control

7) FPGA version management

8) General input ports

9) General output ports

8.2 FPGA Internal Register Specifications

Table 8-1 FPGA Internal Register List. Internal registers are all 16bits registers.

Table8-1 List of FPGA Internal Registers

Address	Register name	Abbreviation	R/W	Initial value
H'0500 0000	Interrupt mask control	IRLMSK	R/W	H'0000
H'0500 0002	Interrupt status monitor	IRLMON	R	H'0000
H'0500 0004	SD Card Power-Supply control	SDPOW	R/W	H'0000
H'0500 0006	Reset control	RSTCTL	W	H'0000
H'0500 0008	PCI expansion slot card detection control	PCIBD	R	H'0000
H'0500 000A	PCI add-in board detection control	PCICD	R	H'0000
H'0500 000C	External GPIO board Control 1	EXTIO1	R/W	H'0000
H'0500 000E	External GPIO board Control 2	EXTIO2	R/W	H'0000
H'0500 0010	External GPIO board Control 3	EXTIO3	R/W	H'0000
H'0500 0012	External GPIO board Control 4	EXTIO4	R	H'000x
H'0500 0014	iVDR pins monitor	IVDRMON	R/W	H'0000
H'0500 0016	iVDR control	IVDRCTL	R/W	H'0000
H'0500 0018	On Board LED control	OBLED	R/W	H'0000
H'0500 001A	On Board Switch control	OBSW	R/W	H'0000
H'0500 001C	Sound Interface Select	AUDIOSEL	R/W	H'0000
H'0500 001E	External extension pin polar select	EXTPLR	R/W	H'0000
H'0500 0100	Touch panel controller access control	TPCTL	R/W	H'0000
H'0500 0102	Touch panel controller access clock select	TPDCKCTL	R/W	H'0000
H'0500 0104	Touch panel controller access clear	TPCTLCLR	W	H'0000
H'0500 0106	Touch panel X position data	TPXPOS	R	H'0000
H'0500 0108	Touch panel Y position data	TPYPOS	R	H'0000
H'0500 0200	Debug board detection control	DBDET	R	H'000x
H'0500 0202	Character dot LCD control	DBDISPCTL	R/W	H'0000
H'0500 0204	Debug switch control	DBSW	R/W	H'0000
H'0500 0300	Compact flash timing control	CFCTL	R/W	H'0000
H'0500 0302	Compact flash power supply control	CFPOW	R/W	H'0000
H'0500 0304	Compact flash insert interrupt clear	CFCDINTCLR	W	H'0000
H'0500 0400	SCIF mode register	SCSMR	R/W	H'0000
H'0500 0402	SCIF bit rate control	SCBRR	R/W	H'00FF
H'0500 0404	SCIF control	SCSCR	R/W	H'0000

H’0500 0406	SCIF transmit FIFO data	SCFTDR	W	H’0000
H’0500 0408	SCIF status register	SCFSR	R/W	H’0060
H’0500 040A	SCIF receive FIFO data	SCFRDR	R	H’0000
H’0500 040C	SCIF FIFO control	SCFCR	R/W	H’0000
H’0500 040E	SCIF FIFO data count	SCFDR	R	H’0000
H’0500 0412	SCIF line status	SCLSR	R/W	H’0000
H’0500 0500	Two wired serial control	ICCR	R/W	H’0000
H’0500 0502	Two wired serial slave address control	SAR	R/W	H’0000
H’0500 0504	Two wired serial mode control	MDR	R/W	H’0000
H’0500 0506	Two wired serial address control 1	ADR1	R/W	H’0000
:	:	:	:	H’0000
H’0500 0544	Two wired serial address control 32	ADR32	R/W	H’0000
H’0500 0546	Two wired serial data control 1	DAR1	R/W	H’0000
:	:	:	:	H’0000
H’0500 0564	Two wired serial data control 16	DAR16	R/W	H’0000
H’0500 0600	Version management	VERREG	R/W	H’1010

8.2.1 Interrupt mask Control

This register controls the SH4A interrupt mask.

Address:H'0500 0000 Resister name: Interrupt mask Control (IRLMSK) Initial value:H'0000			
Bit	Bit Name	R/W	Function
15	PCI_INTA_MSK	R/W	PCI device 0 interrupt mask, 0: Interrupt masked, 1: Interrupt enabled
14	PCI_INTB_MSK	R/W	PCI device 1 interrupt mask, 0: Interrupt masked, 1: Interrupt enabled
13	PCI_INTC_MSK	R/W	PCI device 2 interrupt mask, 0: Interrupt masked, 1: Interrupt enabled
12	PCI_INTD_MSK	R/W	PCI device 3 interrupt mask, 0: Interrupt masked, 1: Interrupt enabled
11	CF_INT_MSK	R/W	Compact flash interrupt mask, 0: Interrupt masked, 1: Interrupt enabled
10	CF_CDINT_MSK	R/W	Compact flash insert interrupt mask, 0: Interrupt masked, 1: Interrupt enabled
9	M66596_INT_MSK	R/W	M66596 interrupt mask, 0: Interrupt masked, 1: Interrupt enabled
8	TE4300_INT_MSK	R/W	TE4300 interrupt mask, 0: Interrupt masked, 1: Interrupt enabled
7	TP_INT_MSK	R/W	Touch panel interrupt mask, 0: Interrupt masked, 1: Interrupt enabled
6	TWS_INT_MSK	R/W	Two wired serial interrupt mask, 0: Interrupt masked, 1: Interrupt enabled
5	SCI_INT_MSK	R/W	SCIF (FPGA Function) interrupt mask, 0: Interrupt masked, 1: Interrupt enabled
4	EXT_INTA_MSK	R/W	External board interrupt A mask, 0: Interrupt masked, 1: Interrupt enabled
3	EXT_INTB_MSK	R/W	External board interrupt B mask, 0: Interrupt masked, 1: Interrupt enabled
2	EXTIO_IRQ_MSK	R/W	External GPIO interrupt mask, 0: Interrupt masked, 1: Interrupt enabled
1	DB_PSWINT_MSK	R/W	Debug push switch interrupt mask, 0: Interrupt masked, 1: Interrupt enabled
0	AX_IRQ_MSK	R/W	AX88796L interrupt mask, 0: Interrupt masked, 1: Interrupt enabled

8.2.2 Interrupt status Monitor

This register indicates interrupts from peripheral devices.

Address:H'0500 0002 Resister name: Interrupt status Monitor (IRLMON) Initial value:H'0000			
Bit	Bit Name	R/W	Function
15	PCI_INTA_MON	R	PCI_INT0 interrupt, 0: No interrupt, 1: With interrupt
14	PCI_INTB_MON	R	PCI_INT1 interrupt, 0: No interrupt, 1: With interrupt
13	PCI_INTC_MON	R	PCI_INT2 interrupt, 0: No interrupt, 1: With interrupt
12	PCI_INTD_MON	R	PCI_INT3 interrupt, 0: No interrupt, 1: With interrupt
11	CF_INT_MON	R	Compact flash interrupt, 0: No interrupt, 1: With interrupt
10	CF_CDINT_MON	R	Compact flash insert interrupt, 0: No interrupt, 1: With interrupt
9	M66596_MON	R	M66596 interrupt 0: No interrupt, 1: With interrupt
8	TE4300_MON	R	TE4300 interrupt 0: No interrupt, 1: With interrupt
7	TP_INT_MON	R	Touch panel interrupt, 0: No interrupt, 1: With interrupt

6	TWS_INT_MON	R	Two wired serial interrupt , 0: No interrupt, 1: With interrupt
5	SCI_INT_MON	R	SCIF (FPGA Function) interrupt , 0: No interrupt, 1: With interrupt
4	EXT_INTA_MON	R	External board interrupt A, 0: No interrupt, 1: With interrupt
3	EXT_INT_MON	R	External board interrupt B, 0: No interrupt, 1: With interrupt
2	EXTIO_IRQ_MON	R	External GPIO interrupt, 0: No interrupt, 1: With interrupt
1	DBPWS_INT_MON	R	Debug push switch interrupt, 0: No interrupt, 1: With interrupt
0	AX_IRQ_MON	R	AX88796L interrupt, 0: No interrupt, 1: With interrupt

The following interrupts are generated in the Highlander80, with the priorities given below.

No.	Interrupt Type	Priority Level		Remarks
1	PCI_INT0 interrupt	15	High	“L”Level
2	PCI_INT1 interrupt	14	↑	“H”Level
3	PCI_INT2 interrupt	13		“L”Level
4	PCI_INT03 interrupt	12		“L”Level
5	Compact flash interrupt	11		“L”Level
6	Compact flash insert interrupt	10		“L”Level
7	M66596 interrupt	9		“L”Level
8	TE4300 interrupt	8		“L”Level
9	Touch panel interrupt	7		“L”Level
10	SCIF (FPGA Function) interrupt	6		“L”Level
11	Two wired serial interrupt	5		“L”Level
12	External board interrupt A	4		*selectable
13	External board interrupt B			
14	AX88796L interrupt	3		“L”Level
15	Debug push switch interrupt	2	↓	“L”Level
16	External GPIO interrupt	1	Low	*selectable

*selectable: “Level” or “Edge” and “High” or “Low” is selectable at FPGA register.

8.2.3 SD Card Power-Supply control

This register controls power supply to SD card.

Address:H'0500 0004 Resister name: SD Card Power-Supply control (SDPOW) Initial value:H'0000			
Bit	Bit Name	R/W	Function
15:1	—	R	Not Used
0	VCCEN	R/W	0:Not power supply 1:With power supply

8.2.4 Reset Control

This register controls reset output to the peripheral devices.

Writing 1 to this bit outputs a 10-us pulse width reset. Writing 0 to this bit is invalid.

Address:H'0500 0006 Resister name: Reset Control (RSTCTL) Initial value:H'0000			
Bit	Bit Name	R/W	Function
15:12	—	R	Not Used
11	CF_RST	W	To CF, 1: outputs a 10-us pulse width reset 0: invalid.
10	—	R	Not Used
9	M66596_RST	W	To M66896, 1: outputs a 10-us pulse width reset 0: invalid.
8	TE4300_RST	W	To TE4300, 1: outputs a 10-us pulse width reset 0: invalid.
7:6	—	R	Not Used
5	—	R	Not Used
4	EXT_RST	W	To External, 1: outputs a 10-us pulse width reset 0: invalid.
3	—	R	Not Used
2	FROM_RST	W	To FROM board, 1: outputs a 10-us pulse width reset 0: invalid.
1	SSI_RST	W	To SSI Device, 1: outputs a 10-us pulse width reset 0: invalid.
0	AX_RST	W	To AX88796L, 1: outputs a 10-us pulse width reset 0: invalid.

8.2.5 PCI expansion slot card detection control

This register is detection which PCI card connectivity.

Address:H'0500 0008 Resister name: PCI expansion slot card detection control (PCIBD) Initial value:H'000x			
Bit	Bit Name	R/W	Function
15:1	—	R	Not Used
0	PCI_PRST	R	0:Not connected 1:PCI card connected

8.2.6 PCI add-in board detection control

This register is detection which add-in PCI board connectivity.

Address:H'0500 000A Resister name: PCI add-in board detection control (PCICD) Initial value:H'000x			
Bit	Bit Name	R/W	Function
15:1	—	R	Not Used
0	PCI_PRST_EXIT	R	0:Not connected 1:add-in PCI board connected

8.2.7 External GPIO board Control 1

This register controls External GPIO.

Address:H'0500 000C Resister name: External GPIO board Control 1 (EXTIO1) Initial value:H'0000			
Bit	Bit Name	R/W	Function
15	EXT7_DIR	R/W	EXT7_IO input/output select, 0:Input 1:Output
14	EXT6_DIR	R/W	EXT6_IO input/output select, 0:Input 1:Output
13	EXT5_DIR	R/W	EXT5_IO input/output select, 0:Input 1:Output
12	EXT4_DIR	R/W	EXT4_IO input/output select, 0:Input 1:Output
11	EXT3_DIR	R/W	EXT3_IO input/output select, 0:Input 1:Output
10	EXT2_DIR	R/W	EXT2_IO input/output select, 0:Input 1:Output
9	EXT1_DIR	R/W	EXT1_IO input/output select, 0:Input 1:Output
8	EXT0_DIR	R/W	EXT0_IO input/output select, 0:Input 1:Output
7	EXT7_IO	R/W	EXT7_IO Data
6	EXT6_IO	R/W	EXT6_IO Data
5	EXT5_IO	R/W	EXT5_IO Data
4	EXT4_IO	R/W	EXT4_IO Data
3	EXT3_IO	R/W	EXT3_IO Data
2	EXT2_IO	R	EXT2_IO Data
1	EXT1_IO	R/W	EXT1_IO Data
0	EXT0_IO	R/W	EXT0_IO Data

EXTn_IOs are selected EXTn_DIR value. If it is output mode, the register bit output setting data. (0: output "L", 1: output"H")

If it is input mode, the register bit reads port status. And Input mode is selected by EXTn_IRQ, input data read or interrupt mode.

(EXTn_IRQ = 0: GPIO, 1: Interrupt)

8.2.8 External GPIO board Control 2

This register controls External GPIO. (Only EXTn_IOs are Input mode)

Address:H'0500 000E Resister name: External GPIO board Control 2 (EXTIO2) Initial value:H'0000			
Bit	Bit Name	R/W	Function
15	EXT7_IRQ_CLR	R/W	When EXT7_IO is interrupt mode (edge). Writing 1 to clear.
14	EXT6_IRQ_CLR	R/W	When EXT6_IO is interrupt mode (edge). Writing 1 to clear.
13	EXT5_IRQ_CLR	R/W	When EXT5_IO is interrupt mode (edge). Writing 1 to clear.
12	EXT4_IRQ_CLR	R/W	When EXT4_IO is interrupt mode (edge). Writing 1 to clear.
11	EXT3_IRQ_CLR	R/W	When EXT3_IO is interrupt mode (edge). Writing 1 to clear.
10	EXT2_IRQ_CLR	R/W	When EXT2_IO is interrupt mode (edge). Writing 1 to clear.
9	EXT1_IRQ_CLR	R/W	When EXT1_IO is interrupt mode (edge). Writing 1 to clear.
8	EXT0_IRQ_CLR	R/W	When EXT0_IO is interrupt mode (edge). Writing 1 to clear.
7	EXT7_IRQ	R/W	EXT7_IO mode select, 0:GPIO 1:Interrupt
6	EXT6_IRQ	R/W	EXT6_IO mode select, 0:GPIO 1:Interrupt
5	EXT5_IRQ	R/W	EXT5_IO mode select, 0:GPIO 1:Interrupt
4	EXT4_IRQ	R/W	EXT4_IO mode select, 0:GPIO 1:Interrupt
3	EXT3_IRQ	R/W	EXT3_IO mode select, 0:GPIO 1:Interrupt
2	EXT2_IRQ	R/W	EXT2_IO mode select, 0:GPIO 1:Interrupt
1	EXT1_IRQ	R/W	EXT1_IO mode select, 0:GPIO 1:Interrupt
0	EXT0_IRQ	R/W	EXT0_IO mode select, 0:GPIO 1:Interrupt

Writing 0 to bits 8 - 15 are invalid.

8.2.9 External GPIO board Control 3

This register controls External GPIO. (This register is valid at EXTn_IOs are input mode or interrupt mode)

Address:H'0500 000E Resister name: External GPIO board Control 3 (EXTIO3) Initial value:H'0000			
Bit	Bit Name	R/W	Function
15	EXT7_EL1	R/W	EXT7_IO interrupt mode select 1
14	EXT7_EL0	R/W	EXT7_IO interrupt mode select 0
13	EXT6_EL1	R/W	EXT6_IO interrupt mode select 1
12	EXT6_EL0	R/W	EXT6_IO interrupt mode select 0
11	EXT5_EL1	R/W	EXT5_IO interrupt mode select 1
10	EXT5_EL0	R/W	EXT5_IO interrupt mode select 0
9	EXT4_EL1	R/W	EXT4_IO interrupt mode select 1
8	EXT4_EL0	R/W	EXT4_IO interrupt mode select 0

7	EXT3_EL1	R/W	EXT3_IO interrupt mode select 1
6	EXT3_EL0	R/W	EXT3_IO interrupt mode select 0
5	EXT2_EL1	R/W	EXT2_IO interrupt mode select 1
4	EXT2_EL0	R/W	EXT2_IO interrupt mode select 0
3	EXT1_EL0	R/W	EXT1_IO interrupt mode select 1
2	EXT1_EL0	R/W	EXT1_IO interrupt mode select 0
1	EXT0_EL0	R/W	EXT0_IO interrupt mode select 1
0	EXT0_EL0	R/W	EXT0_IO interrupt mode select 0

Mode selection details

MODE	EXTn_EL1	EXTn_EL0	Function
1	L	L	rising edge interrupt mode
2	L	H	falling edge interrupt mode
3	H	L	“L” Level interrupt mode
4	H	H	“H” Level interrupt mode

8.2.10 External GPIO board Control 4

This register carries out functional detection of the connected External GPIO board.

Address:H’0500 0012 Resister name: External GPIO board Control 4 (EXTIO4) Initial value:H’000x			
Bit	Bit Name	R/W	Function
15:3	—	R	Not Used
2	EXT_IDENT2	R	External GPIO board distinction 2
1	EXT_IDENT1	R	External GPIO board distinction 1
0	EXT_IDENT0	R	External GPIO board distinction 0

Mode selection details

MODE	EXT_IDENT2	EXT_IDENT1	EXT_IDENT0	Function
1	L	H	H	EXT_SW
2	H	L	H	Console
3	H	H	H	ZigBee
4				It reserves except 1-3

8.2.11 iVDR pins monitor

This register indicates the iVDR pin status.

Address:H'0500 0014 Resister name: iVDR pins monitor (IVDRMON) Initial value:H'00xx			
Bit	Bit Name	R/W	Function
15:6	—	R	Not Used
5	PW_ID1	R	iVDR pin 21 status
4	PW_ID0	R	iVDR pin 22 status
3	IF_ID3	R	iVDR pin 26 status
2	IF_ID2	R	iVDR pin 25 status
1	IF_ID1	R	iVDR pin 24 status
0	IF_ID0	R	iVDR pin 23 status

8.2.12 iVDR control

This register is iVDR pin monitor.

Address:H'0500 0014 Resister name: iVDR control (IVDRCTL) Initial value:H'00xx			
Bit	Bit Name	R/W	Function
15:9	—	R	Not Used
8	IVDR_CK_EN	R/W	To Si13112 clock supply, 0:not supply 1:clock supply
7:1	—	R	Not Used
0	IVDR_PW_ON	R/W	To iVDR power supply, 0:not supply 1:With power supply

8.2.13 On Board LED control

This register controls On board LEDs.

Address:H'0500 0018 Resister name: On Board LED control (OBLED) Initial value:H'0000			
Bit	Bit Name	R/W	Function
15:8	—	R	Not Used
7	OBLED7	W	LED12 control, 0:Off 1:On
6	OBLED6	W	LED11 control, 0:Off 1:On
5	OBLED5	W	LED10 control, 0:Off 1:On
4	OBLED4	W	LED9 control, 0:Off 1:On
3	OBLED3	W	LED8 control, 0:Off 1:On
2	OBLED2	W	LED7 control, 0:Off 1:On
1	OBLED1	W	LED6 control, 0:Off 1:On
0	OBLED0	W	LED5 control, 0:Off 1:On

8.2.14 On Board Switch control

This register indicates On board Dip switches status.

Address:H'0500001A Resister name: On Board Switch control (OBSW) Initial value:H'00xx(State of switches)			
Bit	Bit Name	R/W	Function
15:8	—	R	Not Used
7	OBSW7	R	S3-8 status, 0:OFF 1:ON
6	OBSW6	R	S3-7 status, 0:OFF 1:ON
5	OBSW5	R	S3-6 status, 0:OFF 1:ON
4	OBSW4	R	S3-5 status, 0:OFF 1:ON
3	OBSW3	R	S3-4 status, 0:OFF 1:ON
2	OBSW2	R	S3-3 status, 0:OFF 1:ON
1	OBSW1	R	S3-2 status, 0:OFF 1:ON
0	OBSW0	R	S3-1 status, 0:OFF 1:ON

8.2.15 Sound Interface Select

This register controls SH7780's audio interface.

Address:H'0500 001C Resister name: Sound Interface Select (AUDIOSEL) Initial value:H'0000			
Bit	Bit Name	R/W	Function
15:1	—	R	Not Used
0	S_SEL	R/W	Sound / SSI Interface select, 0:HAC (Sound) 1:SSI

8.2.16 External extension pin's polarity select

This register controls extension pin's polarity.

Address:H'0500 001E Resister name: External extension pin's polarity select (EXTPLR) Initial value:H'0000			
Bit	Bit Name	R/W	Function
15:5	—	R	Not Used
9	INTA_CLR	W	When INTA is interrupt mode (edge). Writing 1 to clear.
8	INTB_CLR	W	When INTB is interrupt mode (edge). Writing 1 to clear.
7	—	R	Not Used
6	INTA_ELSEL	R/W	INTA interrupt detection mode, 0: Edge 1: Level
5	INTB_ELSEL	R/W	INTB interrupt detection mode, 0: Edge 1: Level
4	INTA_PNSEL	R/W	INTA active polarity select, 0:L 1:H
3	INTB_PNSEL	R/W	INTB active polarity select, 0:L 1:H
2	WAITA_PNSEL	R/W	WAITA active polarity select, 0:L 1:H

1	WAITB_PNSEL	R/W	WAITB active polarity select, 0:L 1:H
0	RST_PNSEL	R/W	RST active polarity select, 0:L 1:H

8.2.17 Touch panel controller access control

This register controls touch panel controller board control.

Address:H'0500 0100 Resister name: Touch panel controller access control(TPCTL) Initial value:H'0000			
Bit	Bit Name	R/W	Function
15:1	—	R	Not Used
0	TP_EN	R/W	Touch panel controller board access control, 0:Disable 1:Enable

8.2.18 Touch panel controller access clock select

This register selects clock mode for touch panel controller.

Address:H'0500 0102 Resister name: Touch panel controller access clock select (TPTCKCTL) Initial value:H'0000			
Bit	Bit Name	R/W	Function
15:4	—	R	Not Used
3	TC3	R/W	Clock Select Mode 3
2	TC2	R/W	Clock Select Mode 2
1	TC1	R/W	Clock Select Mode 1
0	TC0	R/W	Clock Select Mode 0

Clock select (A setup of those other than the following is set to 60 KHz.)

TC3	TC2	TC1	TC0	TXCLK
L	L	L	L	60 KHz
L	L	L	H	65 KHz
L	L	H	L	70 KHz
L	L	H	H	75 KHz
L	H	L	L	80 KHz
L	H	L	H	85 KHz
L	H	H	L	90 KHz
L	H	H	H	95 KHz
H	L	L	L	100 KHz
H	L	L	H	105 KHz
H	L	H	L	110 KHz

8.2.19 Touch panel controller access clear

This register resets the touch panel control module.

Address:H'0500 0104 Resister name: Touch panel controller access clear (TPCTLCLR) Initial value:H'0000			
Bit	Bit Name	R/W	Function
15:1	—	R	Not Used
0	TRST	W	Touch panel controller access control module reset, Writing 1 to this bit output reset pulse. Writing 0 to this bit is invalid.

8.2.20 Touch panel X position data

This register is X position read data.

Address:H'0500 0106 Resister name: Touch panel X position data (TPXPOS) Initial value:H'0000			
Bit	Bit Name	R/W	Function
15:12	—	R	Not Used
11:0	XD11:0	R	Touch panel X position read data

Data storing of a touch panel is performed three consecutive times by one sampling.

So, access this register three consecutive times.

8.2.21 Touch panel Y position data

This register is Y position read data.

Address:H'0500 0108 Resister name: Touch panel Y position data (TPYPOS) Initial value:H'0000			
Bit	Bit Name	R/W	Function
15:12	—	R	Not Used
11:0	YD11:0	R	Touch panel Y position read data

Data storing of a touch panel is performed three consecutive times by one sampling.

So, access this register three consecutive times.

8.2.22 Debug board detection control

This register detects that Debug board connectivity.

Address:H'0500 0200 Resister name: Debug board detection control (DBDET) Initial value:H'0000			
Bit	Bit Name	R/W	Function
15:1	—	R	Not Used
0	DB_DET	R	0:Not connected 1:Debug board connected

8.2.23 Character dot LCD control

This register controls a character dot LCD.

Address:H'0500 0202 Resister name: Character dot LCD control (DBDISPCTL) Initial value:H'0000			
Bit	Bit Name	R/W	Function
15:14	—	R	Not Used
13	DCLK1	R/W	clock operating mode DCLK1 DCLK0 clock 0 0 φ 0 1 φ/2 1 0 φ/3 1 1 φ/8
12	DCLK0	R/W	
11	—	R	Not Used
10	TAS2	R/W	Address - DISP_CS Assertion delay TAS2 TAS1 TAS0 number of wait states 0 0 0 2 0 0 1 3 0 1 0 4 0 1 1 6 1 0 0 9 1 0 1 12 1 1 0 15
9	TAS1	R/W	
8	TAS0	R/W	
7	—	R	Not Used
6	TAH2	R/W	DISP_CS negation – Address delay TAH2 TAH1 TAH0 number of wait states 0 0 0 2 0 0 1 3 0 1 0 4 0 1 1 6 1 0 0 9 1 0 1 12 1 1 0 15
5	TAH1	R/W	
4	TAH0	R/W	
3:2	—	R	Not Used

1	PWEH1	R/W	DISP_CE Assertion cycle PWENH1 PWENH0 number of wait states 0 0 1 0 1 15 1 0 20 1 1 30
0	PWEH0	R/W	

8.2.24 Debug switch control

This register indicates debugging switches status.

Address:H'0500 0204 Resister name: Debug switch control (DBSW) Initial value:H'00xx			
Bit	Bit Name	R/W	Function
15	—	R	Not Used
14	DB_PSW_2_CLR	W	PSW S2 interrupt clear Writing 1 to clear. Writing 1 is invalid.
13	DB_PSW_1_CLR	W	PSW S3 interrupt clear Writing 1 to clear. Writing 1 is invalid.
12	DB_PSW_0_CLR	W	PSW S4 interrupt clear Writing 1 to clear. Writing 1 is invalid.
11:7	—	R	Not Used
6	DBSW_6	R	Push SW (On the RDBRP-1) S2 0:OFF 1:ON
5	DBSW_5	R	Push SW (On the RDBRP-1) S3 0:OFF 1:ON
4	DBSW_4	R	Push SW (On the RDBRP-1) S4 0:OFF 1:ON
3	DBSW_3	R	Dip SW (On the RDBRP-1) S5-1 0:OFF 1:ON
2	DBSW_2	R	Dip SW (On the RDBRP-1) S5-2 0:OFF 1:ON
1	DBSW_1	R	Dip SW (On the RDBRP-1) S5-3 0:OFF 1:ON
0	DBSW_0	R	Dip SW (On the RDBRP-1) S5-4 0:OFF 1:ON

8.2.25 Compact flash timing control

This register controls the compact flash card.

Address:H'0500 0300 Resister name: Compact flash timing control (CFCTL) Initial value:H'0000			
Bit	Bit Name	R/W	Function
15:14	—	R	Not Used
13	TCLK1	R/W	clock operating mode TCLK1 TCLK0 clock 0 0 φ 0 1 φ/2 1 0 φ/3 1 1 φ/8
12	TCLK0	R/W	
11	—	R	Not Used
10	TED2	R/W	Address – IORDn/IOWRn Assertion delay TED2 TED1 TED0 number of wait states 0 0 0 1 0 0 1 2 0 1 0 3 0 1 1 6 1 0 0 9 1 0 1 12 1 1 0 15
9	TED1	R/W	
8	TED0	R/W	
7	—	R	Not Used
6	THE2	R/W	IORDn/IOWRn Negation – Address delay THE2 THE1 THE0 number of wait states 0 0 0 1 0 0 1 2 0 1 0 3 0 1 1 6 1 0 0 9 1 0 1 12 1 1 0 15
5	THE1	R/W	
4	THE0	R/W	
3	—	R	Not Used
2	—	R	Not Used

1	PCW1	R/W	PCMCIA wait state TED1 TED0 number of wait states 0 0 1 0 1 15 1 0 20 1 1 30
0	PCW0	R/W	

8.2.26 Compact flash power supply control

This register controls power supply to the compact flash card.

Address:H'0500 0302 Resister name: Compact flash power supply control (CFPOW) Initial value:H'0000			
Bit	Bit Name	R/W	Function
15:2	—	R	Not Used
1	VCC5EN	R/W	VCC5EN VCC3EN Supply Voltage 0 0 0V 0 1 3V 1 0 5V 1 1 Prohibition of a setup
0	VCC3EN	R/W	

8.2.27 Compact flash insert interrupt clear

Address:H'0500 0304 Resister name: Compact flash insert interrupt clear (CFCDINTCLR) Initial value:H'0000			
Bit	Bit Name	R/W	Function
15:1	—	R	Not Used
0	CFCLR	W	CFCDINT interrupt clear, Writing 1 is clear. Writing 0 is invalid.

8.2.28 SCIF mode register (FPGA Function)

This register controls SCIF mode.

Address:H'0500 0400 Resister name: SCIF mode register (SCSMR) Initial value:H'0000			
Bit	Bit Name	R/W	Function
15:7	—	R	Not Used
6	CHR	R/W	Asynchronous mode, data length 0:8bits 1:7bits
5	PE	R/W	parity, 0:none 1:support
4	O_En	R/W	Parity, 0:Even 1:odd
3	STOP	R/W	stop bit, 0:1bit 1:2bits
2	—	R	Not Used
1	CKS1	R/W	clock mode CKS1 CKS0 mode 0 0 CLK 0 1 CLK/4 1 0 CLK/16 1 1 CLK/64
0	CKS0	R/W	

8.2.29 SCIF bit rate control (FPGA Function)

This register sets the SCIF bit rate.

Address:H'0500 0402 Resister name: SCIF bit rate control (SCBRP) Initial value:H'00FF			
Bit	Bit Name	R/W	Function
15:8	—	R	Not Used
7:0	N7-0	R/W	

The SCBRR setting is found from the following equation.

Asynchronous mode:

$$N = \frac{P\Phi}{64 \times 2^{2n-1} \times B} \times 10^{6} - 1$$

Where B: Bit rate (bits/s)

N: SCBRR setting for baud rate generator (0 ≤ N ≤ 255)

P□: Peripheral module operating frequency (MHz)

n: Baud rate generator input clock (n = 0 to 3) (SCSMR CKS0,CKS1 value)

The bit rate error in asynchronous mode is found from the following equation:

$$Error(\%) = \left\{ \frac{P\Phi \times 10^{6}}{(N+1) \times B \times 64 \times 2^{2n-1}} - 1 \right\} \times 100$$

8.2.30 SCIF control (FPGA Function)

This register controls SCIF communication mode.

Address:H'0500 0404 Resister name: SCIF control (SCSCR) Initial value:H'0000			
Bit	Bit Name	R/W	Function
15:8	—	R	Not Used
7	TIE	R/W	Transmission FIFO data empty (TXI) interrupt, 0:Disabled 1:Enabled
6	RIE	R/W	Receive (data(RXI), error(ERI), break(BRI)) interrupt, 0:Disabled 1:Enabled
5	TE	R/W	Transmit control 0:Disabled 1:Enabled
4	RE	R/W	Receive control 0:Disabled 1:Enabled
3	REIE	R/W	Receive (error(ERI), break (BRI))interrupt (When Bit6 (RIE) =0), 0:Disabled 1:Enabled
2	—	R	Not Used
1	CKE1	R/W	Clock mode CKE1 CKE0 SCK pin mode 0 0 port 0 1 output clock 1 0 Input clock(1.8432MHz) 1 1 Input clock(Outside)
0	CKE0	R/W	

8.2.31 SCIF transmit FIFO data (FPGA Function)

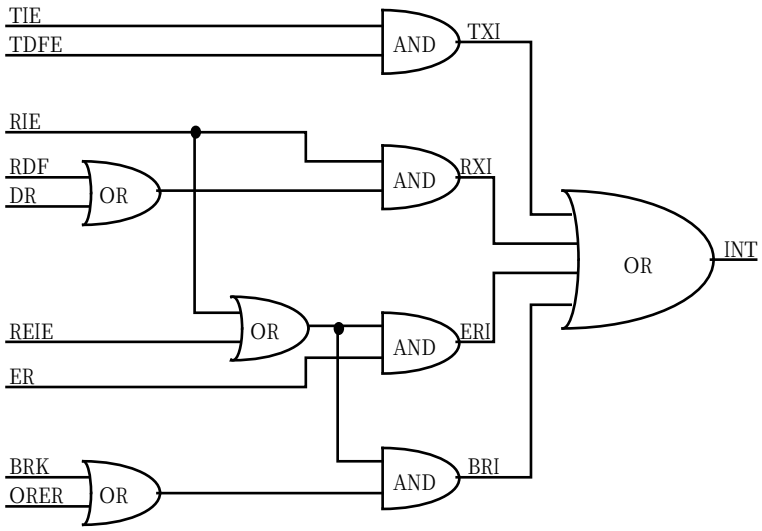
This register controls Transmission data.

Address:H'0500 0406 Resister name: CIF transmit FIFO data (SCFTDR) Initial value:H'0000			
Bit	Bit Name	R/W	Function
15:8	—	R	Not Used
7:0	TD7-0	W	Transmission data

8.2.32 SCIF status register (FPGA Function)

This register indicates the SCIF module status.

SCIF module interrupt block



Signal Name		Register Name	Bit
TIE	:	SCSCR	7
RIE	:	SCSCR	6
REIE	:	SCSCR	3
TDFE	:	SCFSR	5
RDF	:	SCFSR	1
DR	:	SCFSR	0
ER	:	SCFSR	7
BRK	:	SCFSR	4
RER	:	SCLSR	0

Address:H'0500 0408Resister name: SCIF status register (SCFSR) Initial value:H'0000		
Bit	Bit Name	Function
15:12	PER3-0	The number of data which has generated the parity error in the received data stored in SCFRDR is shown. When 16 bytes of all received data of SCFRDR are accompanied by the parity error, PER 3-0 shows 0.
11-8	FER3-0	The number of data which has generated the framing error in the received data stored in SCFRDR is shown. When 16 bytes of all received data of SCFRDR are accompanied by the framing error, PER 3-0 shows 0.
7	ER	It is shown that the framing error or the parity error occurred, 0: none 1: error
6	TEND	Transmission end, 0: Under transmission . 1: Transmission end
5	TDFE	Transmission FIFO shows below the number of setting data, 0: More transmit data than the number of setup. 1: Transmit data is below the number of setup.
4	BRK	The break signal of received data is detected, 0:none 1:break
3	FER	Detection of the framing error of SCFRDR, 0: none 1: error
2	PER	Detection of the parity error of SCFRDR, 0: none 1: error
1	RDF	Receive FIFO shows below the number of setting data, 0: Few received data than the number of setup. 1: Received data are more than the number of setup.
0	DR	0: The following received data do not come more than 1.5-frame time from the stop bit of data which the data of under the number of setup are in SCFRDR, and received at the end. 1: The completion of reception is carried out more than 1.5-frame time at receiving Naka or normalcy from the stop bit of data which the data of under the number of setup are in SCFRDR, and received at the end, and received data do not remain in SCFRDR.

8.2.33 SCIF receive FIFO data (FPGA Function)

This register controls Receive data.

Address:H'0500 040A Resister name: SCIF receive FIFO data (SCFRDR) Initial value:H'0000			
Bit	Bit Name	R/W	Function
15:8	—	R	Not Used
7:0	RD7-0	W	Receive data

8.2.34 SCIF FIFO control (FPGA Function)

This register controls SCI FIFO.

Address:H'0500 040C Resister name: SCIF FIFO control (SCFCR) Initial value:H'0000		
Bit	Bit Name	Function
15:11	−	Not Used
10-8	RSTRG2-0	When the number of received data becomes more than the number of setup, High is outputted to an RTS signal. 3'b000: 15 3'b001: 1 3'b010: 4 3'b011: 6 3'b100: 8 3'b101: 10 3'b110: 12 3'b111: 14
7-6	RTRG1-0	The number of received data which sets a RDF flag is set up. 2'b00: 1 2'b01: 4 2'b10: 8 2'b11: 14
5-4	TTRG1-0	The remaining numbers of transmit data which set a TDFE flag is set up. 2'b00:8 (8) 2'b01:4 (12) 2'b10:2 (14) 2'b11:1 (15) The value in () shows the number of openings of SCFTDR at the time of flag generating.
3	MCE	Enable/Disable is controlled for the modem control signals CTSn and RTSn, 0: Disable 1: Enable
2	TFRST	The data of SCFTDR are reset, 0:not reset 1: reset
1	RFRST	The data of SCFRDR are reset, 0:not reset 1: reset
0	LOOP	Internal connection mode. (TXD to RXD,CTSn to RTSn)

8.2.35 SCIF FIFO data count (FPGA Function)

This register indicates the number of data bytes stored in SCFTDR.

Address:H'0500 040E Resister name: SCIF FIFO data count (SCFDR) Initial value:H'0000		
Bit	Bit Name	Function
15:13	−	Not Used
12-8	T4-0	The number of data which is not transmitted in SCFTDR is shown. H'00 is none data. H'10 is full data.
7-5	−	Not Used
4-0	R4-0	The number of data which is not received in SCFRDR is shown. H'00 is none data. H'10 is full data.

8.2.36 SCIF line status (FPGA Function)

This register indicates that an overrun error occurred during reception, causing abnormal termination.

Address:H'0500 0410 Resister name: SCIF line status (SCLSR) Initial value:H'0000		
Bit	Bit Name	Function
15:1	—	Not Used
0	ORER	0:Normally complete or Under operation 1: Overrun error

8.2.37 Two wired serial control

This register controls the Two wired serial module.

Address:H'0500 0500 Resister name: Two wired serial control (ICCR) Initial value:H'0000			
Bit	Bit Name	R/W	Function
15:7	—	R	Not Used
6	IEIC	R/W	Interrupt, 0: Disable 1: Enable
5	—	R	Not Used
4	RST	W	Two wired serial module reset (With FIFO), 1: Reset 0: Invalid.
3	ACKE	R	Result of operation.(Judgement by ACK) 0: Normal 1: Abnormal
2	BBSY	R	Two wired serial module bus status, 0: Bus Open 1: Bus Occupancy
1	IRIC	R	Two wired serial module status, 0: Under operation 1:End of operation
0	START	R/W	Two wired serial module communication control 1: Start 0: Invalid (0clear is end of communication.)

8.2.38 Two wired serial slave address control

This register controls slave address and communication mode.

Address:H'0500 0502 Resister name: Two wired serial slave address control (SAR) Initial value:H'0000			
Bit	Bit Name	R/W	Function
15:8	—	R	Not Used
7:1	SA6:0	R/W	Slave address set up
0	R_W	R/W	Transmission mode select, 0:transmit 1:receive

8.2.39 Two wired serial mode control

This register controls the Two wired serial control module.

Address:H'0500 0504 Resister name: Two wired serial mode control (MDR) Initial value:H'0000			
Bit	Bit Name	R/W	Function
15:8	—	R	Not Used
7	IEIC	R/W	transmission data rate, 0:100KHz 1:400KHz
6:4	—	R	Not Used
3	CAP	R/W	Device Capacity 0:0-32Kbyte 1:32Kbyte or more
2	—	R	Not Used
1	MODE1	R/W	Transmission data Byte count
0	MODE0	R/W	MODE1 MODE0 Byte count 0 0 1Byte 0 1 8Byte 1 0 16Byte 1 1 32Byte

8.2.40 Two wired serial address control 1-32

This registers set up the Two wired serial module addresses.

Address:H'0500 0506 Resister name: Two wired serial address control (ADR1) Initial value:H'0000			
Bit	Bit Name	R/W	Function
15:8	AD1[7:0]	R/W	Transmission address 1 set up
7:0	AD2[7:0]	R/W	Transmission address 2 set up

Table 6-1 shows a list of ADR2 – 32.

8.2.41 Two wired serial data control 1

This registers set up the Two wired serial module data.

Address:H'0500 0546 Resister name: Two wired serial data control 1 (DAR1) Initial value:H'0000			
Bit	Bit Name	R/W	Function
15:8	DA1[7:0]	R/W	Transmission data 1 set up
7:0	DA2[7:0]	R/W	Transmission data 2 set up

Table 6-2 shows a list of ADR2 – 16.

Table6-1 ADR2-32

Register Name	Address	15:8	Setting Address	7:0	Setting Address
ADR2	H'0500 0508	AD3[7:0]	transmission address 3	AD4[7:0]	transmission address 4
ADR3	H'0500 050A	AD5[7:0]	transmission address 5	AD6[7:0]	transmission address 6
ADR4	H'0500 050C	AD7[7:0]	transmission address 7	AD8[7:0]	transmission address 8
ADR5	H'0500 050E	AD9[7:0]	transmission address 9	AD10[7:0]	transmission address 10
ADR6	H'0500 0510	AD11[7:0]	transmission address 11	AD12[7:0]	transmission address 12
ADR7	H'0500 0512	AD13[7:0]	transmission address 13	AD14[7:0]	transmission address 14
ADR8	H'0500 0514	AD15[7:0]	transmission address 15	AD16[7:0]	transmission address 16
ADR9	H'0500 0516	AD17[7:0]	transmission address 17	AD18[7:0]	transmission address 18
ADR10	H'0500 0518	AD19[7:0]	transmission address 19	AD20[7:0]	transmission address 20
ADR11	H'0500 051A	AD21[7:0]	transmission address 21	AD22[7:0]	transmission address 22
ADR12	H'0500 051C	AD23[7:0]	transmission address 23	AD24[7:0]	transmission address 24
ADR13	H'0500 051E	AD25[7:0]	transmission address 25	AD26[7:0]	transmission address 26
ADR14	H'0500 0520	AD27[7:0]	transmission address 27	AD28[7:0]	transmission address 28
ADR15	H'0500 0522	AD29[7:0]	transmission address 29	AD30[7:0]	transmission address 30
ADR16	H'0500 0524	AD31[7:0]	transmission address 31	AD32[7:0]	transmission address 32
ADR17	H'0500 0526	AD33[7:0]	transmission address 33	AD34[7:0]	transmission address 34
ADR18	H'0500 0528	AD35[7:0]	transmission address 35	AD36[7:0]	transmission address 36
ADR19	H'0500 052A	AD37[7:0]	transmission address 37	AD38[7:0]	transmission address 38
ADR20	H'0500 052C	AD39[7:0]	transmission address 39	AD40[7:0]	transmission address 40
ADR21	H'0500 052E	AD41[7:0]	transmission address 41	AD42[7:0]	transmission address 42
ADR22	H'0500 0530	AD43[7:0]	transmission address 43	AD44[7:0]	transmission address 44
ADR23	H'0500 0532	AD45[7:0]	transmission address 45	AD46[7:0]	transmission address 46
ADR24	H'0500 0534	AD47[7:0]	transmission address 47	AD48[7:0]	transmission address 48
ADR25	H'0500 0536	AD49[7:0]	transmission address 49	AD50[7:0]	transmission address 50
ADR26	H'0500 0538	AD51[7:0]	transmission address 51	AD52[7:0]	transmission address 52
ADR27	H'0500 053A	AD53[7:0]	transmission address 53	AD54[7:0]	transmission address 54
ADR28	H'0500 053C	AD55[7:0]	transmission address 55	AD56[7:0]	transmission address 56
ADR29	H'0500 053E	AD57[7:0]	transmission address 57	AD58[7:0]	transmission address 58
ADR30	H'0500 0540	AD59[7:0]	transmission address 59	AD60[7:0]	transmission address 60
ADR31	H'0500 0542	AD61[7:0]	transmission address 61	AD62[7:0]	transmission address 62
ADR32	H'0500 0544	AD63[7:0]	transmission address 63	AD64[7:0]	transmission address 64

Table6-2 DAR2-16

Register Name	Address	15:8	Setting Data	7:0	Setting Data
DAR2	H'0500 0548	DA3[7:0]	transmission data 3	DA4[7:0]	transmission data 4
DAR3	H'0500 054A	DA5[7:0]	transmission data 5	DA6[7:0]	transmission data 6
DAR4	H'0500 054C	DA7[7:0]	transmission data 7	DA8[7:0]	transmission data 8
DAR5	H'0500 054E	DA9[7:0]	transmission data 9	DA10[7:0]	transmission data 10
DAR6	H'0500 0550	DA11[7:0]	transmission data 11	DA12[7:0]	transmission data 12
DAR7	H'0500 0552	DA13[7:0]	transmission data 13	DA14[7:0]	transmission data 14
DAR8	H'0500 0554	DA15[7:0]	transmission data 15	DA16[7:0]	transmission data 16
DAR9	H'0500 0556	DA17[7:0]	transmission data 17	DA18[7:0]	transmission data 18
DAR10	H'0500 0558	DA19[7:0]	transmission data 19	DA20[7:0]	transmission data 20
DAR11	H'0500 055A	DA21[7:0]	transmission data 21	DA22[7:0]	transmission data 22
DAR12	H'0500 055C	DA23[7:0]	transmission data 23	DA24[7:0]	transmission data 24
DAR13	H'0500 055E	DA25[7:0]	transmission data 25	DA26[7:0]	transmission data 26
DAR14	H'0500 0560	DA27[7:0]	transmission data 27	DA28[7:0]	transmission data 28
DAR15	H'0500 0562	DA29[7:0]	transmission data 29	DA30[7:0]	transmission data 30
DAR16	H'0500 0564	DA31[7:0]	transmission data 31	DA32[7:0]	transmission data 32

8.2.42 Two wired serial control module operation note

8.2.42.1 Transmit operation

Please set up a register before executing a start condition issue command.

Operation of a transmitting procedure is shown below.

⑴ MDR-SP bit、MDR-CAP bit、MDR-MODE1-MODE0 bits、ICCR-IEIC bit set up operation mode.

⑵ The value of ADRn and DARn is set up according to the value set up by (1).

The setting list is shown below.

Table6 -3 List of MDR set up data

MDR(CAP bit)	MDR(MODE1-0 bits)	ADR and DAR
0	00	ADR1: Bit15-8, DAR1: Bit15-8
0	01	ADR1-4, DAR1-4
0	10	ADR1-8, DAR1-8
0	11	ADR1-16, DAR1-16
1	00	ADR1: Bit15-0, DAR1: Bit15-8
1	01	ADR1-8, DAR1-4
1	10	ADR1-16, DAR1-8
1	11	ADR1-32, DAR1-16

⑶ 0-6 bits of SAs of SAR are set up according to the target device, and the R_W bit of SAR is set as '0'.

⑷ The BBSY bit of ICCR is read and it checks that a bus is in a free state.

⑸ '1' is written in the START bit of ICCR and transmitting operation is started.

⑹ If IRIC is “1”, transmission is end. When IRIC = “0” and BBSY = “1” are under operation.

If IRIC = “0” and ACKE = “1” are error status, please reset Two wired serial module. (Writing to 1 ICCR’s RST bit)

8.2.42.2 Receive operation

⑴ MDR-SP bit、MDR-CAP bit、MDR-MODE1-MODE0 bits、ICCR-IEIC bit set up operation mode.

⑵ The value of ADRn and DARn is set up according to the value set up by (1).

⑶ 0-6 bits of SAs of SAR are set up according to the target device, and the R_W bit of SAR is set as '1'.

⑷ The BBSY bit of ICCR is read and it checks that a bus is in a free state.

⑸ '1' is written in the START bit of ICCR and receiving operation is started.

⑹ If IRIC is “1”, receiving is end. When IRIC = “0” and BBSY = “1” are under operation.

If IRIC = “0” and ACKE = “1” are error status, please reset Two wired serial module. (Writing to 1 ICCR’s RST bit)

8.2.43 Version management

This register controls the Version management.

Address:H'0500 0600 Resister name: Version management (VERREG) Initial value:H'1010			
Bit	Bit Name	R/W	Function
15	BVER3	R	Board Version management
14	BVER2	R	
13	BVER1	R	
12	BVER0	R	
11	BREV3	R	Board Revision management
10	BREV2	R	
9	BREV1	R	
8	BREV0	R	
7	VER3	R	FPGA Version management
6	VER2	R	
5	VER1	R	
4	VER0	R	
3	REV3	R	FPGA Revision management
2	REV2	R	
1	REV1	R	
0	REV0	R	

【RPCIRP-1】

1. Scope

This board is applied to RPCIRP-1 aiming at PCI bus extension.

This board is equivalent to a PC card (Cardbus too), Gigabit Ether, Serial-ATA, iVDR, and the PCI edge card (one slot).

2. System Configuration

Figure 2-1 shows the system configuration.

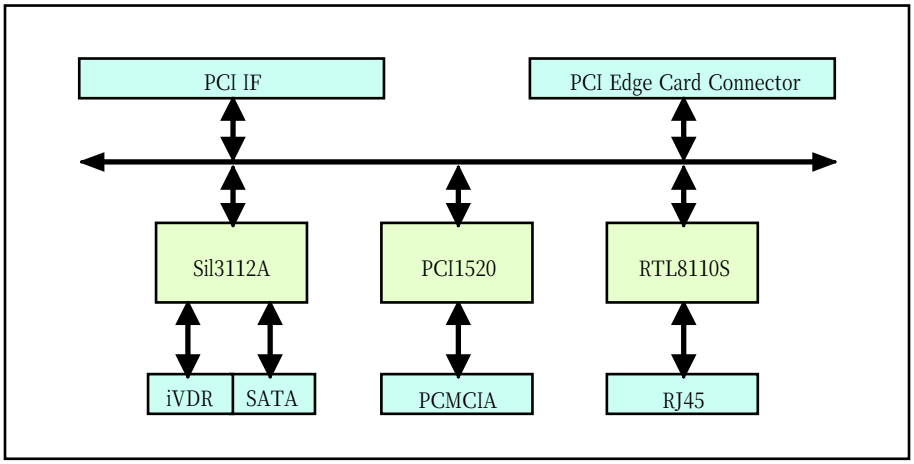


Figure2-1 System Configuration

Each device number (DEVNO) is shown below.

DEV NO	Device	Function	Note
H'0	RTL8110S	Gigabit Ethernet Controller	
H'1	Sil3112A	SATA Controller	
H'2	PCI Slot		
H'3	PCI1520	Card Bus Controller	

3. Connector Specification

Figure 3-1 shows the allocation of parts. Table 3-1 shows a list of connectors. The specifications are described below.

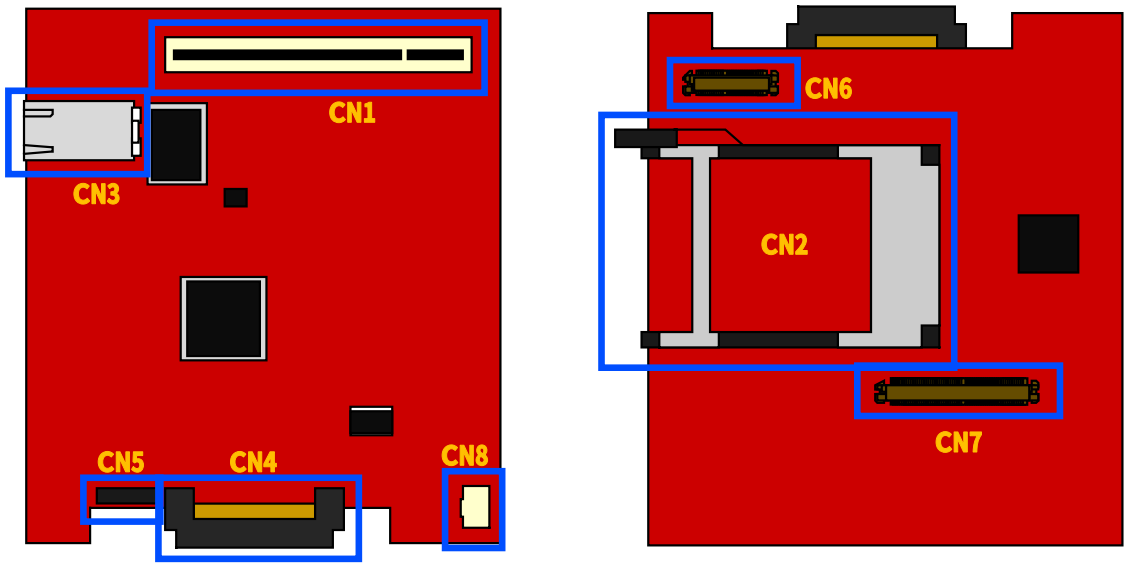


Figure3-1 Parts Allocation

Table3-1 List of Connectors

Ref No.	Function	Note	Ref No.	Function	Note
CN1	PCI Edge Card Connector		CN5	SATA Connector	
CN2	PCMCIA Connector	Type II	CN6	PCI Board IF B	PCI BUS
CN3	LAN Connector	RJ45	CN7	PCI Board IF A	PCI BUS
CN4	iVDR Connector		CN8	POWER	

3.1 Connector for the PCI Card

CN1 is PCI Card connector.

3.2 Connector for the PCMCIA Card

CN2 is PCMCIA connector. It has connected with Card Bus Bridge Controller PCI1520. Card Bus Card is also supported.

3.3 Connector for the Ethernet

CN3 is LAN connector. It has connected with Gigabit Ether Controller RTL8110.

3.4 Connector for the iVDR

CN4 is iVDR connector. The pin assignment specifications are as follows:

Connector type:52837-0609 Manufacturer: Molex					
Pin No.	Signal	Function	Pin No.	Signal	Function
1	GND	Ground	2	A+	Port A+
3	A-	Port A-	4	GND	Ground
5	B+	Port B+	6	B-	Port B-
7	GND	Ground	8	GND	Ground
9	C+	Port C+	10	C-	Port C-
11	GND	Ground	12	NC	Not Connected
13	NC	Not Connected	14	NC	Not Connected
15	GND	Ground	16	GND	Ground
17	GND	Ground	18	PWR	5Vor3.3V
19	PWR	5Vor3.3V	20	PWR	5Vor3.3V
21	PW-ID0	Power ID0	22	PW-ID1	Power ID1
23	IF-ID0	IF-ID0	24	IF-ID1	IF-ID1
25	IF-ID2	IF-ID2	26	IF-ID3	IF-ID3

3.5 Connector for the SATA HDD

CN5 is SATA HDD Connector.

3.6 Connector for the Main board B

CN6 is connected with R7780RP-1's CN8. The pin assignment specifications are as follows:

Connector type:52837-0609 Manufacturer: Molex					
Pin No.	Signal	Function	Pin No.	Signal	Function
1	GND	Ground	2	GND	Ground
3	PCI_INTAN	PCI Interrupt A	4	PCI_INTBN	PCI Interrupt B
5	PCI_INTCN	PCI Interrupt C	6	PCI_INTDN	PCI Interrupt D
7	GND	Ground	8	GND	Ground
9	PCI_RSTN	PCI Reset	10	PCI_PRST_EXTN	PCI Board Information
11	GND	Ground	12	GND	Ground
13	TS_CLK	Not connected	14	GND	Ground
15	GND	Ground	16	TS_VLDA	Not connected
17	TS_SYNC	Not connected	18	GND	Ground
19	GND	Ground	20	TS_DATA	Not connected

21	TS_IOEN	Not connected	22	GND	Ground
23	GND	Ground	24	TS_DIR	Not connected
25	TS_ERR	Not connected	26	GND	Ground
27	GND	Ground	28	GND	Ground
29	IVDR0	IVDR Control	30	IVDR_PER_ON	IVDR Power Control
31	GND	Ground	32	GND	Ground
33	PW_ID0	IVDR Power ID	34	PW_ID1	IVDR Power ID
35	GND	Ground	36	GND	Ground
37	IF_ID0	IVDR Function ID	38	IF_ID1	IVDR Function ID
39	IF_ID2	IVDR Function ID	40	IF_ID3	IVDR Function ID
41	GND	Ground	42	GND	Ground
43	NC	Not connected	44	NC	Not connected
45	NC	Not connected	46	NC	Not connected
47	NC	Not connected	48	NC	Not connected
49	NC	Not connected	50	NC	Not connected
51	NC	Not connected	52	NC	Not connected
53	NC	Not connected	54	NC	Not connected
55	NC	Not connected	56	NC	Not connected
57	NC	Not connected	58	NC	Not connected
59	GND	Ground	60	GND	Ground

3.7 Connector for the Main board A

CN7 is connected with R7780RP-1's CN7. The pin assignment specifications are as follows:

Connector type:52837-1209 Manufacturer: Molex					
Pin No.	Signal	Function	Pin No.	Signal	Function
1	GND	Ground	2	GND	Ground
3	PCI_CLK1	PCI Clock	4	GND	Ground
5	NC	Not connected	6	PCI_CLK2	PCI Clock
7	PCI_CLK3	PCI Clock	8	NC	Not connected
9	GND	Ground	10	PCI_CLK4	PCI Clock
11	GND	Ground	12	GND	Ground
13	PCI_RSTN	PCI Reset	14	PCI_C/BE0N	PCI C/BE
15	PCI_C/BE1N	PCI C/BE	16	PCI_C/BE2N	PCI C/BE
17	PCI_C/BE3N	PCI C/BE	18	PCI_PAR	PCI Parity
19	GND	Ground	20	GND	Ground

21	NC	Not connected	22	NC	Not connected
23	GND	Ground	24	GND	Ground
25	PCI_FRAMEN	PCI Cycle Frame	26	PCI_IRDYN	PCI initiator ready
27	PCI_TRDYN	PCI Target Ready	28	PCI_STOPN	PCI Cycle Stop
29	PCI_DEVSEL	PCI Device Select	30	PCI_LOCKN	PCI Lock
31	PCI_PERN	PCI Parity Error	32	PCI_SERRN	PCI System Error
33	GND	Ground	34	GND	Ground
35	PCI_REQ1N	PCI Bus Request	36	PCI_REQ2N	PCI Bus Request
37	PCI_REQ3N	PCI Bus Request	38	PCI_REQ4N	PCI Bus Request
39	PCI_GNT1N	PCI Bus Grant	40	PCI_GNT2N	PCI Bus Grant
41	PCI_GNT3N	PCI Bus Grant	42	PCI_GNT4N	PCI Bus Grant
43	GND	Ground	44	GND	Ground
45	PCI_AD0	PCI Address/Data	46	PCI_AD1	PCI Address/Data
47	PCI_AD2	PCI Address/Data	48	PCI_AD3	PCI Address/Data
49	PCI_AD4	PCI Address/Data	50	PCI_AD5	PCI Address/Data
51	PCI_AD6	PCI Address/Data	52	PCI_AD7	PCI Address/Data
53	GND	Ground	54	GND	Ground
55	PCI_AD8	PCI Address/Data	56	PCI_AD9	PCI Address/Data
57	PCI_AD10	PCI Address/Data	58	PCI_AD11	PCI Address/Data
59	PCI_AD12	PCI Address/Data	60	PCI_AD13	PCI Address/Data
61	PCI_AD14	PCI Address/Data	62	PCI_AD15	PCI Address/Data
63	GND	Ground	64	GND	Ground
65	+3.3V	Not connected	66	+3.3V	Not connected
67	GND	Ground	68	GND	Ground
69	PCI_AD16	PCI Address/Data	70	PCI_AD17	PCI Address/Data
71	PCI_AD18	PCI Address/Data	72	PCI_AD19	PCI Address/Data
73	PCI_AD20	PCI Address/Data	74	PCI_AD21	PCI Address/Data
75	PCI_AD22	PCI Address/Data	76	PCI_AD23	PCI Address/Data
77	GND	Ground	78	GND	Ground
79	PCI_AD24	PCI Address/Data	80	PCI_AD25	PCI Address/Data
81	PCI_AD26	PCI Address/Data	82	PCI_AD27	PCI Address/Data
83	PCI_AD28	PCI Address/Data	84	PCI_AD29	PCI Address/Data
85	PCI_AD30	PCI Address/Data	86	PCI_AD31	PCI Address/Data
87	GND	Ground	88	GND	Ground

89	IDSEL1	Initialization Device Select	90	IDSEL2	Initialization Device Select
91	IDSEL3	Initialization Device Select	92	IDSEL4	Initialization Device Select
93	NC	Not connected	94	NC	Not connected
95	NC	Not connected	96	NC	Not connected
97	GND	Ground	98	GND	Ground
99	+5V	Not connected	100	+5V	Not connected
101	GND	Ground	102	GND	Ground
103	NC	Not connected	104	NC	Not connected
105	NC	Not connected	106	NC	Not connected
107	NC	Not connected	108	NC	Not connected
109	NC	Not connected	110	POW_RESETN	Not connected
111	GND	Ground	112	GND	Ground
113	GND	Ground	114	GND	Ground
115	GND	Ground	116	GND	Ground
117	GND	Ground	118	GND	Ground
119	GND	Ground	120	GND	Ground

3.8 Connector for External Power-Supply

CN8 is Power-Supply connector. A power is supplied from a back board. The pin assignment specifications are as follows:

Connector type:DF1E-4P-2.54DS Manufacturer: HIROSE					
Pin No.	Signal	Function	Pin No.	Signal	Function
1	+5V	Supply +5.0V	3	+3.3V	Supply +3.3V
2	GND	Ground	4	GND	Ground

【RDBRP-1】

1. Scope

This board is used connecting with main board R7780RP-1.

2. System Configuration

Figure 2-1 shows the system configuration.

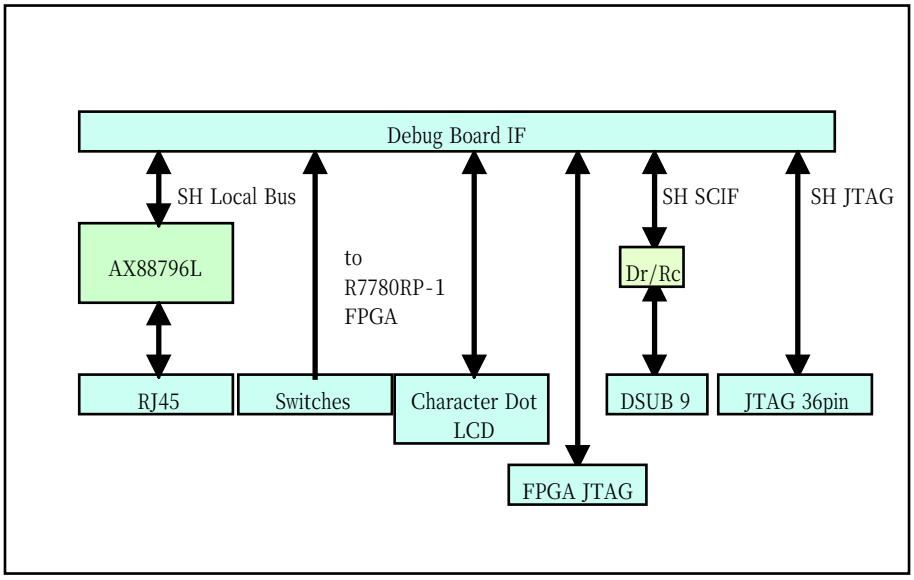


Figure2-1 System Configuration

3. Connector Specification

Figure 3-1 shows the allocation of parts. Table 3-1 shows a list of connectors. The specifications are described below.

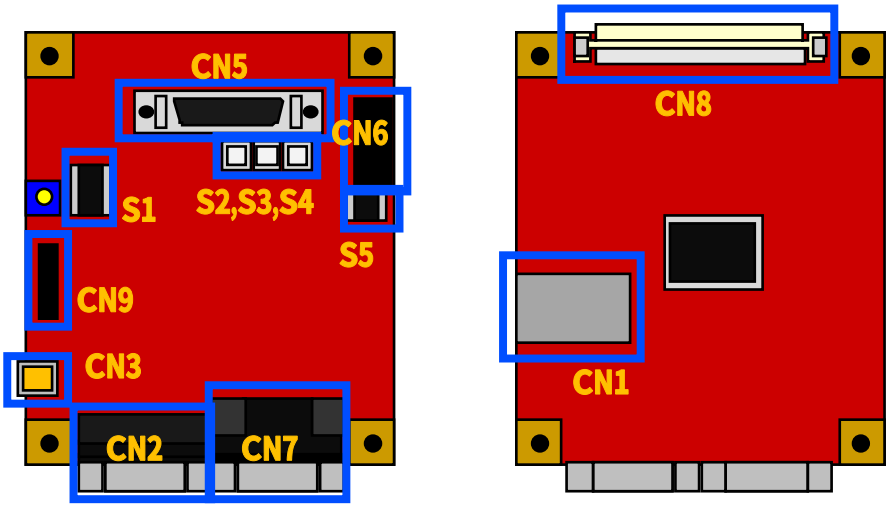


Figure3-1 Parts Allocation

Table3-1 List of Connectors

Ref No.	Function	Note	Ref No.	Function	Note
CN1	LAN Connector	RJ45	CN6	FPGA Programming	
CN2	Serial Connector	DSUB9	CN7	CRT Connector	Option
CN3	USB Connector	miniB	CN8	CPU Board IF	
CN5	SH JTAG Connector		CN9	Character Dot LCD	Option

3.1 Ethernet connector

CN1 is LAN connector. It has connected with Ether Controller AX88796L.

3.2 Connector for he Serial Interface

CN2 is Serial connector. The pin assignment specifications are as follows:

Connector type:JEY-9P-1A1B Manufacturer: JST					
Pin No.	Signal	Function	Pin No.	Signal	Function
1	NC	Not connected	6	DSR	Connected Pin 4
2	RD	Receive Data	7	RTS	Request to send
3	TD	Transmit Data	8	CTS	Clear to Send
4	DTR	Connected Pin 6	9	NC	Not connected
5	GND	Ground			

3.3 Connector for the USB

CN3 is mini USB B connector.

3.4 Connector for the JTAG Emulator

CN5 is JTAG connector. It has connected with JTAG Emulator. The pin assignment specifications are as follows:

Connector type: DX20M-36S Manufacturer: HIROSE					
Pin No.	Signal	Function	Pin No.	Signal	Function
1	AUDCK	AUD Clock	19	TMS	Mode Select
2	GND	Ground	20	GND	Ground
3	AUDATA0	AUD Data	21	TRSTn	Reset
4	GND	Ground	22	GND	Ground
5	AUDDATA1	AUD Data	23	TDI	Data Input
6	GND	Ground	24	GND	Ground
7	AUDATA2	AUD Data	25	TDO	Data Output
8	GND	Ground	26	GND	Ground

9	AUDATA3	AUD Data	27	ASEBRKn	Break
10	GND	Ground	28	GND	Ground
11	AUDSYNCn	AUD Sync	29	NC	Not connected
12	GND	Ground	30	GND	Ground
13	NC	Not connected	31	RESETn	Reset
14	GND	Ground	32	GND	Ground
15	NC	Not connected	33	GND	Ground
16	GND	Ground	34	GND	Ground
17	TCK	Clock	35	NC	Not connected
18	GND	Ground	36	GND	Ground

3.5 Connector for the FPGA Programming

CN6 is FPGA Programming connector. Rewriting of FPGA carried on a Main board from this connector. The pin assignment specifications are as follows:

Connector type:FAP-10-08#4-0BS Manufacturer: YAMAICHI					
Pin No.	Signal	Function	Pin No.	Signal	Function
1	DB_CLK		6	DB_nCE	
2	GND	Ground	7	DB_DATA	
3	DB_CONFDONE		8	DB_nCS	
4	V33	Supply +3.3V	9	DB_ASDO	
5	DB_nCONFIG		10	GND	Ground

3.6 Connector for the CRT Monitor

CN7 is CRT Monitor connector. The pin assignment specifications are as follows:

Connector type:KEY-15S-2A2B Manufacturer: JST					
Pin No.	Signal	Function	Pin No.	Signal	Function
1	RED	RED	9	NC	Not connected
2	GREEN	GREEN	10	GND	Ground
3	BLUE	BLUE	11	NC	Not connected
4	NC	Not connected	12	NC	Not connected
5	GND	Ground	13	CRTHS	H Sync
6	GND	Ground	14	CRTVS	V Sync
7	GND	Ground	15	NC	Not connected
8	GND	Ground			

3.7 Main board connection

CN8 is Main board connector. The pin assignment specifications are as follows:

Connector type：BMN80-100R Manufacturer：KEL					
Pin No.	Signal	Function	Pin No.	Signal	Function
1	+5V	Supply +5.0V	51	AX_WEN	ETHER IC Write
2	+5V	Supply +5.0V	52	AX_RDN	ETHER IC Read
3	GND	Ground	53	GND	Ground
4	GND	Ground	54	GND	Ground
5	DB_A12	Address	55	DB_DOTWEN	Dot LCD Write
6	DB_A10	Address	56	DB_MPMD	SH MODE9 Control
7	GND	Ground	57	DB_DOTCSN	Dot LCD Select
8	GND	Ground	58	DB_DOTRDN	Dot LCD Read/Write
9	DB_A9	Address	59	DB_CTS0	Modem Control
10	DB_A8	Address	60	DB_TX0	Serial Data Out
11	DB_A7	Address	61	DB_RTS0	Modem Control
12	DB_A6	Address	62	DB_RX0	Serial Data In
13	GND	Ground	63	GND	Ground
14	GND	Ground	64	GND	Ground
15	DB_A5	Address	65	DB_CRTHS	CRT Hsync
16	DB_A4	Address	66	DB_CRTVS	CRT Vsync
17	DB_A3	Address	67	DB_RED	CRT RED
18	DB_A2	Address	68	DB_GREEN	CRT GREEN
19	DB_A1	Address	69	DB_BLUE	CRT BLUE
20	GND	Ground	70	GND	Ground
21	GND	Ground	71	GND	Ground
22	GND	Ground	72	GND	Ground
23	DB_D15	Data	73	SH_PRSTN	Reset Out
24	DB_D14	Data	74	DB_JRSTN	Reset In
25	DB_D13	Data	75	DB_TMS	Mode Select
26	DB_D12	Data	76	DB_ASEBRKN	Break
27	GND	Ground	77	DB_TDI	Data In
28	GND	Ground	78	DB_TDO	Data Out
29	DB_D11	Data	79	DB_TCK	Clock
30	DB_D10	Data	80	DB_TRSTN	Reset

31	DB_D10	Data	81	DB_AUDCK	AUD Clock
32	DB_D9	Data	82	DB_AUDSYNCN	AUD Sync
33	GND	Ground	83	DB_AUDATA3	AUD Data
34	GND	Ground	84	DB_AUDATA2	AUD Data
35	DB_D7	Data	85	DB_AUDATA1	AUD Data
36	DB_D6	Data	86	DB_AUDATA0	AUD Data
37	DB_D5	Data	87	DB_PSW2	Push Switch
38	DB_D4	Data	88	DB_PSW1	Push Switch
39	GND	Ground	89	DB_PSW0	Push Switch
40	GND	Ground	90	DB_DSW3	Dip Switch
41	DB_D3	Data	91	DB_DSW2	Dip Switch
42	DB_D2	Data	92	DB_DSW1	Dip Switch
43	DB_D1	Data	93	DB_DSW0	Dip Switch
44	DB_D0	Data	94	DB_DCLK	FPGA JTAG Signal
45	GND	Ground	95	DB_NCS	FPGA JTAG Signal
46	GND	Ground	96	DB_NCE	FPGA JTAG Signal
47	AX_RSTN	ETHER IC Reset	97	DB_ASDO	FPGA JTAG Signal
48	AX_RDYN	ETHER IC Ready	98	DB_CONF_DONE	FPGA JTAG Signal
49	AX_IRQ	ETHER IC Interrupt	99	DB_NCONFIG	FPGA JTAG Signal
50	AX_CSN	ETHER IC Select	100	DB_DATA	FPGA JTAG Signal

3.8 Connector for the character LCD (Option)

CN9 is Character dot LCD connector. The pin assignment specifications are as follows:。

Connector type:FAP-14-08#4-0BS Manufacturer: YAMAICHI					
Pin No.	Signal	Function	Pin No.	Signal	Function
1	D7	Data	8	D0	Data
2	D6	Data	9	E	Enable
3	D5	Data	10	R/W	Read/Write
4	D4	Data	11	RS	Register Select
5	D3	Data	12	VLC	Contrast ADJ.
6	D2	Data	13	VSS	Ground
7	D1	Data	14	V5	Supply +5.0V

4. Switch Specification

Table 4-1 shows the list of switches. The specifications are described below.

Table4-1 List of Switches

Ref No.	Function	Note	Ref No.	Function	Note
S1	AX88796L Mode Set		S4	Debug SW	Push SW
S2	Debug SW	Push SW	S5	Debug SW	Dip
S3	Debug SW	Push SW			

4.1 Switch for the AX88796L Mode Setting

S1 is the switch for the operating mode setting of the AX88796. The allocation of each switch is listed below.

At shipment, the CPU type is the ISA bus mode (CPU0 = low and CPU1 = low offset = 200h).

S1-8 uses the in/output of SCI for selection of DSUB9 pin and a USB connector. (At shipment, “Low”=DSUB9)
When connecting with PC for consoles using USB, the COM Driver for PC of exclusive use is needed.

Switch No.	Connected pin	ON	OFF
S1-1	CPU1	H	L
S1-2	CPU0	H	L
S1-3	IO_BASE2	H	L
S1-4	IO_BASE1	H	L
S1-5	IO_BASE0	H	L
S1-6	Not Connect	H	L
S1-7	Not Connect	H	L
S1-8	DB_BUSSW	H	L

4.2 Push Switches for Debugging

S2, S3 and S4 are switches for debugging. They are dedicated registers connected to the FPGA and can be referenced. Please refer to the FPGA section for the specifications.

Address:0500 0204 h supporting bits:Bit12-14

4.3 Dip Switches for the Debugging

S5 is switches for debugging. They are dedicated registers connected to the FPGA and can be referenced. Please refer to the FPGA section for the specifications.

Address:0500 0204 h supporting bits:Bit0-7

【RMAIN_BWBRP-1】

1. Scope

This board is combined with RSUB_BWBRP-1. And are R7780RP-1, R7770RP-1, and a board for in addition to this mounting an extended board. It is attached in the cage for attaching an extended board.

2. System Configuration

Figure 2-1 shows the system configuration.

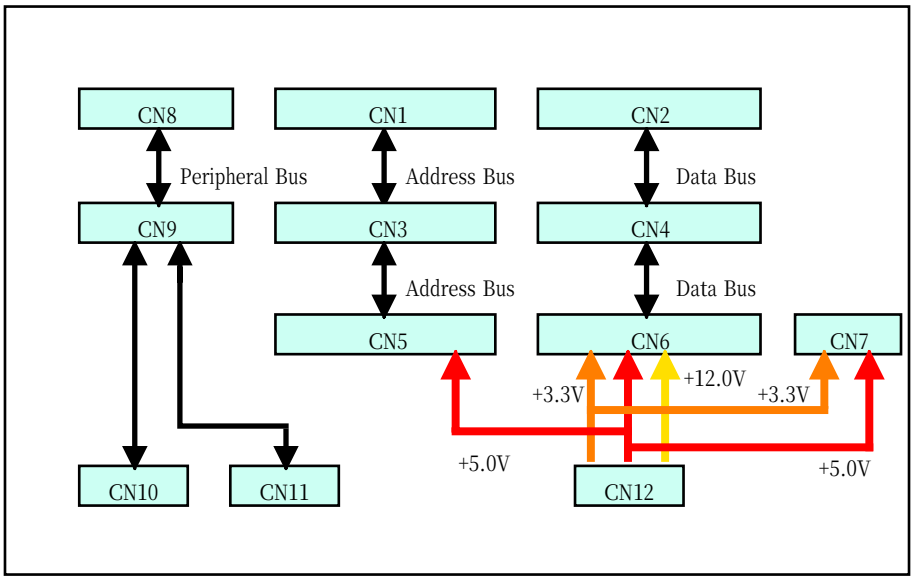


Figure .2-1 System Configuration

3. Connector Specification

Figure 3-1 shows the allocation of parts. Table 3-1 shows a list of connectors. The specifications are described below.

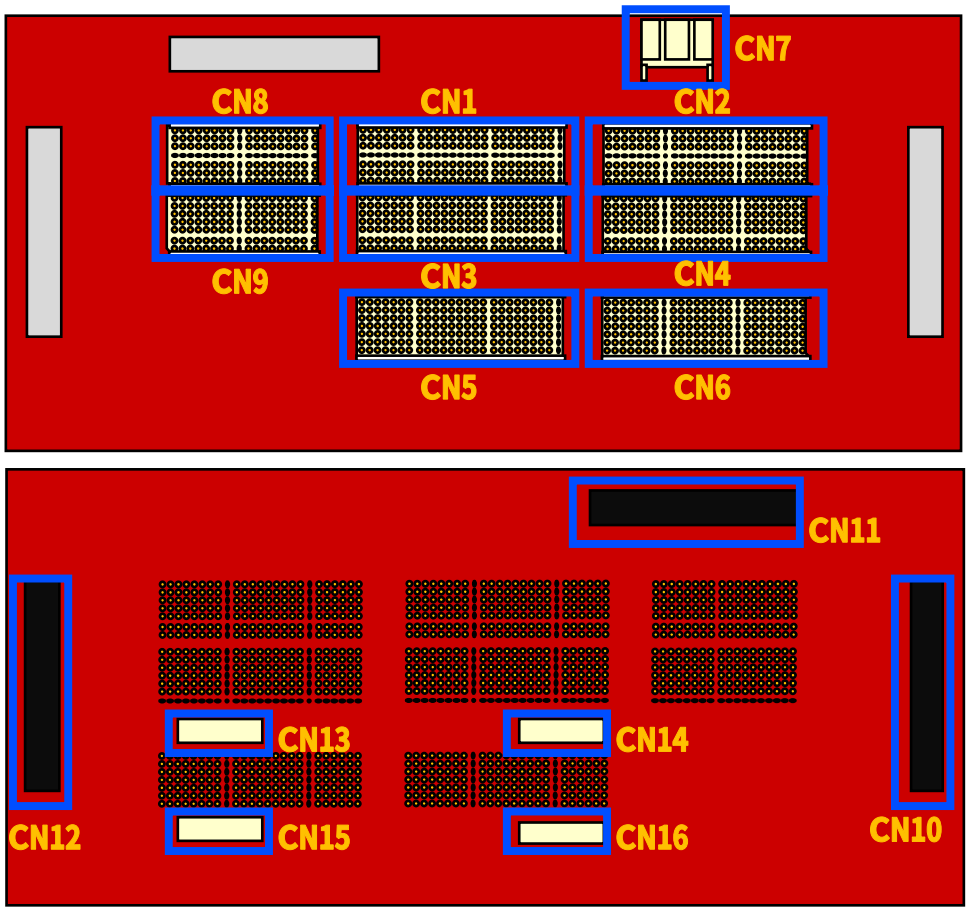


Figure3-1 Parts Allocation

Table3-1List of Connectors

Ref No.	Function	Note	Ref No.	Function	Note
CN1	Board Connector	Address Bus	CN10	SUB_BWB B to B	
CN2	Board Connector	Data Bus	CN11	SUB_BWB B to B	
CN3	Board Connector	Address Bus	CN12	SUB_BWB B to B	
CN4	Board Connector	Data Bus	CN13	Terminator Connector	
CN5	Board Connector	Address Bus	CN14	Terminator Connector	
CN6	Board Connector	Data Bus	CN15	Terminator Connector	
CN7	PCI Power Supply	to RPCIRP-1	CN16	Terminator Connector	
CN8	Board Connector	MISC			
CN9	Board Connector	MISC			

3.1 Connector for External Expansion

CN1, 3 and 5 are connectors to R7780RP-1, RSOUNDRP-1 and others. The same pins are connected on the board.

Connector type:PCN21A-125PB-2PF-G Manufacturer: HIROSE					
Pin No.	Signal	Function	Pin No.	Signal	Function
1a	+3.3V	Supply +3.3V	1b	+3.3V	Supply +3.3V
2a	GND	Ground	2b	GND	Ground
3a	SH_A21	Address	3b	SH_A22	Address
4a	SH_A16	Address	4b	SH_A17	Address
5a	GND	Ground	5b	GND	Ground
6a	SH_A11	Address	6b	SH_A12	Address
7a	SH_A6	Address	7b	SH_A7	Address
8a	GND	Ground	8b	GND	Ground
9a	SH_A1	Address	9b	SH_A2	Address
10a	GND	Ground	10b	GND	Ground
11a	GND	Ground	11b	SH_WE3N	Write Enable
12a	SH_WE0N	Write Enable	12b	GND	Ground
13a	GND	Ground	13b	SH_RDWEN	Read Write
14a	EXT_WAITB	External Wait	14b	GND	Ground
15a	EX_WAITA	External Wait	15b	EX_CSB	External Chip Select
16a	SH_DACK0	DMA Acknowledge	16b	SH_DACK1	DMA Acknowledge
17a	USB20_RSTN	USB_IC Reset	17b	SH_DREQ0	DMA Request
18a	GND	Ground	18b	GND	Ground
19a	USB20_CSN	USB Chip Select	19b	USB20_INTN	USB Interrupt
20a	USB20_SD5	USB Data	20b	USB20_SD6	USB Data
21a	USB20_SD0	USB Data	21b	USB20_SD1	USB Data
22a	GND	Ground	22b	IF_ID0	For R77703DRP-1
23a	IF_ID2	For R77703DRP-1	23b	IF_ID3	For R77703DRP-1
24a	SD_CS1N	SD Chip Select	24b	SD_CS2N	SD Chip Select
25a	+3.3V	Supply +3.3V	25b	+3.3V	Supply +3.3V

Connector type:PCN21A-125PB-2PF-G Manufacturer: HIROSE					
Pin No.	Signal	Function	Pin No.	Signal	Function
1c	+3.3V	Supply +3.3V	1d	+3.3V	Supply +3.3V
2c	GND	Ground	2d	GND	Ground
3c	SH_A23	Address	3d	SH_A24	Address
4c	SH_A18	Address	4d	SH_A19	Address
5c	GND	Ground	5d	GND	Ground
6c	SH_A13	Address	6d	SH_A14	Address
7c	SH_A8	Address	7d	SH_A9	Address
8c	GND	Ground	8d	GND	Ground
9c	SH_A3	Address	9d	SH_A4	Address
10c	GND	Ground	10d	GND	Ground
11c	GND	Ground	11d	SH_BSN	Bus Start
12c	SH_WE1N	Write	12d	GND	Ground
13c	GND	Ground	13d	SH_RDN	Read
14c	I2C_SDA	I2C Data	14d	GND	Ground
15c	GND	Ground	15d	EX_CSA	External Chip Select
16c	SH_DACK2	DMA Acknowledge	16d	SH_DACK3	DMA Acknowledge
17c	SH_DREQ1	DMA Request	17d	SH_DREQ2	DMA Request
18c	USB20_SOEN	Not connected	18d	GND	Ground
19c	SH_BREQN	Bus Request	19d	SH_BACKN	Bus Acknowledge
20c	USB20_SD7	USB Data	20d	USB20_DEND1N	USB Data Enable
21c	USB20_SD2	USB Data	21d	USB20_SD3	USB Data
22c	IVDR0	For R77703DRP-1	22d	IF_ID1	For R77703DRP-1
23c	PW_ID0	For R77703DRP-1	23d	PW_ID1	For R77703DRP-1
24c	SD_INTN	SD Card Interrupt	24d	SD_RSTN	SD Card Reset
25c	+3.3V	Supply +3.3V	25d	+3.3V	Supply +3.3V

Connector type:PCN21A-125PB-2PF-G Manufacturer: HIROSE					
Pin No.	Signal	Function	Pin No.	Signal	Function
1e	+3.3V	Supply +3.3V	1f	FDGND	Ground
2a	GND	Ground	2f	FDGND	Ground
3e	SH_A25	Address	3f	FDGND	Ground
4e	SH_A20	Address	4f	FDGND	Ground
5e	GND	Ground	5f	FDGND	Ground
6e	SH_A15	Address	6f	FDGND	Ground
7e	SH_A10	Address	7f	FDGND	Ground
8e	GND	Ground	8f	FDGND	Ground
9e	SH_A5	Address	9f	FDGND	Ground
10e	SH_A0	Address	10f	FDGND	Ground
11e	GND	Ground	11f	FDGND	Ground
12e	SH_WE2N	Write Enable	12f	FDGND	Ground
13e	GND	Ground	13f	FDGND	Ground
14e	I2C_SCL	IIC Clock	14f	FDGND	Ground
15e	GND	Ground	15f	FDGND	Ground
16e	SH_EXCPUCS0N	For R77703DRP-1	16f	FDGND	Ground
17e	SH_DREQ3	DMA Request	17f	FDGND	Ground
18e	GND	Ground	18f	FDGND	Ground
19e	SH_DACK0	DMA Acknowledge	19f	FDGND	Ground
20e	USB20_DEN0N	USB Data Enable	20f	FDGND	Ground
21e	USB20_SD4	USB Data	21f	FDGND	Ground
22e	GND	Ground	22f	FDGND	Ground
23e	IVDR_PWR_ON	For R77703DRP-1	23f	FDGND	Ground
24e	SD_PE	SD Power Control	24f	FDGND	Ground
25e	+3.3V	Supply +3.3V	25f	FDGND	Ground

3.2 Connector for External Expansion

CN2, 4 and 6 are connectors to R7780RP-1, RSOUNDRP-1 and others. The same pins are connected on the board.

Connector type:PCN21A-125PB-2PF-G Manufacturer: HIROSE					
Pin No.	Signal	Function	Pin No.	Signal	Function
1a	+5V	Supply +5.0V	1b	+5V	Supply +5.0V
2a	GND	Ground	2b	GND	Ground
3a	EXT_INTBN	Interrupt B	3b	EXT_INTAN	Interrupt A
4a	VI_DATA0	For R77703DRP-1	4b	VI_DATA1	For R77703DRP-1
5a	VI_DATA5	For R77703DRP-1	5b	VI_DATA6	For R77703DRP-1
6a	GND	Ground	6b	GND	Ground
7a	HAC_SDATA_OUT	Tx Frame Serial Data	7b	HAC_SDATA_IN	Rx Frame Serial Data
8a	PCIBO_INT0N	For R77703DRP-1	8b	PCIBO_INT1N	For R77703DRP-1
9a	PCIB_CSSDN	For R77703DRP-1	9b	PCIBCSPCN	For R77703DRP-1
10a	GND	Ground	10b	SSI_RSTN	Module Reset
11a	SH_CKIO	Clock	11b	GND	Ground
12a	GND	Ground	12b	SH_D2	Data
13a	SH_D4	Data	13b	GND	Ground
14a	GND	Ground	14b	SH_D7	Data
15a	SH_D9	Data	15b	GND	Ground
16a	GND	Ground	16b	SH_D12	Data
17a	SH_D14	Data	17b	GND	Ground
18a	GND	Ground	18b	SH_D17	Data
19a	SH_D19	Data	19b	GND	Ground
20a	GND	Ground	20b	SH_D22	Data
21a	SH_D24	Data	21b	GND	Ground
22a	GND	Ground	22b	SH_D27	Data
23a	SH_D29	Data	23b	GND	Ground
24a	GND	Ground	24b	GND	Ground
25a	+5V	Supply	25b	+5V	Supply

Connector type:PCN21A-125PB-2PF-G Manufacturer: HIROSE					
Pin No.	Signal	Function	Pin No.	Signal	Function
1c	+5V	Supply +5.0V	1d	+5V	Supply +5.0V
2c	GDN	Ground	2d	GDN	Ground
3c	EX_RSTN	Reset Out	3d	VI_HSYNC	For R77703DRP-1
4c	VI_DATA2	For R77703DRP-1	4d	VI_DATA3	For R77703DRP-1
5c	VI_DATA7	For R77703DRP-1	5d	VI_CLK	For R77703DRP-1
6c	GND	Ground	6d	GND	Ground
7c	HAC_SYNC	HAC Sync Signal	7d	HAC_BITCLK	HAC Clock
8c	PCIBO_INT2N	For R77703DRP-1	8d	PCIBO_INT3N	For R77703DRP-1
9c	PCIB_CSREGN	For R77703DRP-1	9d	PCIB_RSTN	For R77703DRP-1
10c	GND	Ground	10d	SSI_SCK0	SSI Clock
11c	SH_D0	Data	11d	GND	Ground
12c	GND	Ground	12d	SH_D3	Data
13c	SH_D5	Data	13d	GND	Ground
14c	GND	Ground	14d	SH_D8	Data
15c	SH_D10	Data	15d	GND	Ground
16c	GND	Ground	16d	SH_D13	Data
17c	SH_D15	Data	17d	GND	Ground
18c	GND	Ground	18d	SH_D18	Data
19c	SH_D20	Data	19d	GND	Ground
20c	GND	Ground	20d	SH_D23	Data
21c	SH_D25	Data	21d	GND	Ground
22c	GND	Ground	22d	SH_DF28	Data
23c	SH_D30	Data	23d	GND	Ground
24c	GND	Ground	24d	GND	Ground
25c	+5V	Supply +5.0V	25d	+5V	Supply +5.0V

Connector type:PCN21A-125PB-2PF-G Manufacturer: HIROSE					
Pin No.	Signal	Function	Pin No.	Signal	Function
1e	+5V	Supply +5.0V	1f	FDGND	Ground
2a	GND	Ground	2f	FDGND	Ground
3e	VI_VSYNC	For R77703DRP-1	3f	FDGND	Ground
4e	VI_DATA4	For R77703DRP-1	4f	FDGND	Ground
5e	VI_EN	For R77703DRP-1	5f	FDGND	Ground
6e	GND	Ground	6f	FDGND	Ground
7e	HAC_RESN	Module Reset	7f	FDGND	Ground
8e	SSI_WS0	SSI Ward Select	8f	FDGND	Ground
9e	SSI_SDATA0	SSI Data	9f	FDGND	Ground
10e	GND	Ground	10f	FDGND	Ground
11e	SH_D1	Data	11f	FDGND	Ground
12e	GND	Ground	12f	FDGND	Ground
13e	SH_D6	Data	13f	FDGND	Ground
14e	GND	Ground	14f	FDGND	Ground
15e	SH_D11	Data	15f	FDGND	Ground
16e	GND	Ground	16f	FDGND	Ground
17e	SH_D16	Data	17f	FDGND	Ground
18e	GND	Ground	18f	FDGND	Ground
19e	SH_D21	Data	19f	FDGND	Ground
20e	GND	Ground	20f	FDGND	Ground
21e	SH_D26	Data	21f	FDGND	Ground
22e	GND	Ground	22f	FDGND	Ground
23e	SH_D31	Data	23f	FDGND	Ground
24e	GND	Ground	24f	FDGND	Ground
25e	+5V	Supply +5.0V	25f	FDGND	Ground

＊ HAC＝Audio Codec Interface (Audio Codec 97 (AC'97) Version 2.1)

＊ SSI＝Serial Sound Interface

＊ VI＝Video Interface

＊ PCIB＝PCI Bus Bridge

3.3 Connector for External Expansion

CN8 and 9 are connectors to R7780RP-1, RSOUNDRP-1 and others. The same pins are connected on the board.

Connector type:PCN21A-95PB-2PF-G Manufacturer: HIROSE					
Pin No.	Signal	Function	Pin No.	Signal	Function
1a	AN_GND	For R77703DRP-1	1b	SH_HSYNC	For R77703DRP-1
2a	SH_VSYNC	For R77703DRP-1	2b	AN_GND	For R77703DRP-1
3a	GND	Ground	3b	TP_CSN	Touch Panel Select
4a	IDENT0	Extension ID	4b	TP_IRQN	Touch Panel Interrupt
5a	IDENT1	Extension ID	5b	EXT_GPIO3	Extension GPIO
6a	IDENT2	Extension ID	6b	EXT_GPIO7	Extension GPIO
7a	SSI_SCK	Not connected	7b	GND	Ground
8a	GND	Ground	8b	SSI_CLK	Not connected
9a	TFT_R3	For R77703DRP-1	9b	GND	Ground
10a	TFT_G2	For R77703DRP-1	10b	TFT_G1	For R77703DRP-1
11a	TFT_B1	For R77703DRP-1	11b	TFT_B0	For R77703DRP-1
12a	GND	Ground	12b	TFT_B5	For R77703DRP-1
13a	TFT_DOTCLK	For R77703DRP-1	13b	GND	Ground
14a	TFT_VDD	For R77703DRP-1	14b	TFT_VDD	For R77703DRP-1
15a	GND	Ground	15b	RESET_LED	POW_ON Reset
16a	CAN_ERRN	For R77703DRP-1	16b	GND	Ground
17a	GND	Ground	17b	SCI_SCK9	For R77703DRP-1
18a	SH_GPIO28	For R77703DRP-1	18b	SH_GPIO27	For R77703DRP-1
19a	GND	Ground	19b	GPS_IN	For R77703DRP-1

Connector type:PCN21A-95PB-2PF-G Manufacturer: HIROSE					
Pin No.	Signal	Function	Pin No.	Signal	Function
1c	AN_GND	For R77703DRP-1	1d	SH_R	For R77703DRP-1
2c	SH_B	For R77703DRP-1	2d	AN_GND	For R77703DRP-1
3c	GND	Ground	3d	TP_CLK	Touch Panel Clock
4c	TP_DOUT	Touch Panel Data Out	4d	TP_BUSY	Touch Panel Busy
5c	EXT_GPIO2	Extension GPIO	5d	EXT_GPIO1	Extension GPIO
6c	EXT_GPIO6	Extension GPIO	6d	EXT_GPIO2	Extension GPIO
7c	SCI_SCK0	Serial Clock	7d	SCI_TX0	Serial Data Out
8c	GND	Ground	8d	SSI_WS	Not connected
9c	TFT_R2	For R77703DRP-1	9d	TFT_R1	For R77703DRP-1
10c	TFT_G0	For R77703DRP-1	10d	TFT_R5	For R77703DRP-1
11c	TFT_G5	For R77703DRP-1	11d	TFT_G4	For R77703DRP-1
12c	TFT_B4	For R77703DRP-1	12d	TFT_B3	For R77703DRP-1
13c	TFT_ENB	For R77703DRP-1	13d	TFT_VSYNC	For R77703DRP-1
14c	TFT_VDD	For R77703DRP-1	14d	TFT_BKLED_EN	For R77703DRP-1
15c	CF/HDD_LED	CF_DASP	15d	TFT_CDE	For R77703DRP-1
16c	CAN_RX	For R77703DRP-1	16d	GND	Ground
17c	SCI_RX9	For R77703DRP-1	17d	SCI_TX9	For R77703DRP-1
18c	SH_GPIO26	For R77703DRP-1	18d	SH_GPIO25	For R77703DRP-1
19c	GPS_CLK	For R77703DRP-1	19d	GND	Ground

Connector type:PCN21A-95PB-2PF-G Manufacturer: HIROSE					
Pin No.	Signal	Function	Pin No.	Signal	Function
1e	AN_GND	For R77703DRP-1	1f	FDGND	Ground
2e	SH_G	For R77703DRP-1	2f	FDGND	Ground
3e	GND	Ground	3f	FDGND	Ground
4e	TP_DIN	Touch Panel Data In	4f	FDGND	Ground
5e	EXT_GPIO0	Extension GPIO	5f	FDGND	Ground
6e	EXT _GPIO4	Extension GPIO	6f	FDGND	Ground
7e	SCI_RX0	Serial Data In	7f	FDGND	Ground
8e	SSI_DATA	Not connected	8f	FDGND	Ground
9e	TFT_R0	For R77703DRP-1	9f	FDGND	Ground
10e	TFT_R4	For R77703DRP-1	10f	FDGND	Ground
11e	TFT_G3	For R77703DRP-1	11f	FDGND	Ground
12e	TFT_B2	For R77703DRP-1	12f	FDGND	Ground
13e	GND	Ground	13f	FDGND	Ground
14e	TFT_HSYNC	For R77703DRP-1	14f	FDGND	Ground
15e	TFT_CLAMP	For R77703DRP-1	15f	FDGND	Ground
16e	CAN_TX	For R77703DRP-1	16f	FDGND	Ground
17e	GND	Ground	17f	FDGND	Ground
18e	SH_GPIO24	For R77703DRP-1	18f	FDGND	Ground
19e	SH_GPIO29	For R77703DRP-1	19f	FDGND	Ground

3.4 RSUB_BWBRP-1 Connection

CN10 is RSUBRP-1 connector. The pin assignment specifications are as follows:

Connector type:TX24-60P-12ST-H1 Manufacturer: JAE					
Pin No.	Signal	Function	Pin No.	Signal	Function
1	+3.3V	Supply +3.3V	31	+3.3V	Supply +3.3V
2	+3.3V	Supply +3.3V	32	+3.3V	Supply +3.3V
3	+3.3V	Supply +3.3V	33	+3.3V	Supply +3.3V
4	+3.3V	Supply +3.3V	34	+3.3V	Supply +3.3V
5	+3.3V	Supply +3.3V	35	+3.3V	Supply +3.3V
6	+3.3V	Supply +3.3V	36	+3.3V	Supply +3.3V
7	GND	Ground	37	GND	Ground
8	+5V	Supply +5.0V	38	+5V	Supply +5.0V
9	+5V	Supply +5.0V	39	GND	Ground
10	+5V	Supply +5.0V	40	SSI_DATA	SSI Data
11	SSI_CLK	SSI Clock	41	SSI_WS	SSI
12	GND	Ground	42	GND	Ground
13	SCI_TX0		43	GND	Ground
14	SCI_RX0		44	SCII_SCK	
15	SCI_SCK0		45	EXT _GPIO3	
16	EXT_GPIO7		46	EXT _GPIO2	
17	EXT _GPIO6		47	EXT _GPIO1	
18	EXT _GPIO5		48	EXT _GPIO0	
19	EXT _GPIO4		49	IDENT2	Extension ID
20	IDENT1	Extension ID	50	IDENT0	Extension ID
21	TP_DIN		51	TP_DOUT	
22	TP_BUSY		52	GND	Ground
23	TP_IRQ		53	TP_CLK	
24	GND	Ground	54	GND	Ground
25	SH_G		55	TP_CSN	
26	AGND	Analog Ground	56	GND	Ground
27	SH_B		57	SH_R	
28	AGND	Analog Ground	58	AGND	Analog Ground
29	SH_VSYNC		59	SH_HSYNC	
30	AGND	Analog Ground	60	GND	Analog Ground

3.5 RSUB_BWBRP-1 Connection

CN11 is RSUBRP-1 connector. The pin assignment specifications are as follows:

Connector type:TX24-60P-12ST-H1 Manufacturer: JAE					
Pin No.	Signal	Function	Pin No.	Signal	Function
1	+5V	Supply +5.0V	31	TFT_R0	
2	+5V	Supply +5.0V	32	TFT_R1	
3	+5V	Supply +5.0V	33	TFT_R2	
4	+5V	Supply +5.0V	34	GND	Ground
5	GND	Ground	35	TFT_R3	
6	TFT_G0		36	TFT_R4	
7	TFT_G1		37	TFT_R5	
8	TFT_G2		38	TFT_B0	
9	TFT_G3		39	TFT_B1	
10	TFT_G4		40	TFT_B2	
11	TFT_G5		41	TFT_B3	
12	GND	Ground	42	TFT_B4	
13	TFT_VSYNC		43	TFT_B5	
14	TFT_ENB		44	GND	Ground
15	GND	Ground	45	TFT_DOTCLK	
16	TFT_VDD		46	TFT_HSYNC	
17	TFT_VDD		47	TFT_BKLED_EN	
18	TFT_VDD		48	TFT_CLAMP	
19	CF/HDD_LED		49	TFT_CDE	
20	RESET_LED		50	GND	Ground
21	CAN_ERRN		51	CAN_RX	
22	GND	Ground	52	GND	Ground
23	SCI_TX9		53	CAN_TX	
24	SCI_RX9		54	GND	Ground
25	SCI_SCK9		55	SH_GPIO29	
26	GND	Ground	56	SH_GPIO28	
27	GPS_CLK		57	SH_GPIO27	
28	GPS_IN		58	SH_GPIO26	
29	GND	Ground	59	SH_GPIO25	
30	GND	Ground	60	SH_GPIO24	

3.6 RSUB_BWBRP-1 Connection

CN12 is RSUBRP-1 connector. The pin assignment specifications are as follows:

Connector type:TX24-60P-12ST-H1 Manufacturer: JAE					
Pin No.	Signal	Function	Pin No.	Signal	Function
1	+3.3V	Supply +3.3V	31	+3.3V	Supply +3.3V
2	+3.3V	Supply +3.3V	32	+3.3V	Supply +3.3V
3	+3.3V	Supply +3.3V	33	+3.3V	Supply +3.3V
4	+3.3V	Supply +3.3V	34	+3.3V	Supply +3.3V
5	+3.3V	Supply +3.3V	35	+3.3V	Supply +3.3V
6	+3.3V	Supply +3.3V	36	+3.3V	Supply +3.3V
7	GND	Ground	37	GND	Ground
8	GND	Ground	38	GND	Ground
9	GND	Ground	39	GND	Ground
10	GND	Ground	40	GND	Ground
11	GND	Ground	41	GND	Ground
12	GND	Ground	42	GND	Ground
13	+5V	Supply +5.0V	43	+5V	Supply +5.0V
14	+5V	Supply +5.0V	44	+5V	Supply +5.0V
15	+5V	Supply +5.0V	45	+5V	Supply +5.0V
16	+5V	Supply +5.0V	46	+5V	Supply +5.0V
17	+5V	Supply +5.0V	47	+5V	Supply +5.0V
18	+5V	Supply +5.0V	48	+5V	Supply +5.0V
19	GND	Ground	49	GND	Ground
20	GND	Ground	50	GND	Ground
21	GND	Ground	51	GND	Ground
22	GND	Ground	52	GND	Ground
23	GND	Ground	53	GND	Ground
24	GND	Ground	54	GND	Ground
25	+12V	Supply +12.0V	55	+12V	Supply +12.0V
26	+12V	Supply +12.0V	56	+12V	Supply +12.0V
27	+12V	Supply +12.0V	57	+12V	Supply +12.0V
28	GND	Ground	58	GND	Ground
29	GND	Ground	59	GND	Ground
30	GND	Ground	60	GND	Ground

3.7 Connector for External Power-Supply

CN7 is Power-Supply connector. A power is supplied to a RPCIRP-1. The pin assignment specifications are as follows:

Connector type:DF1E-4P-2.54DS Manufacturer: HIROSE					
Pin No.	Signal	Function	Pin No.	Signal	Function
1	+5V	Supply +5.0V	3	+3.3V	Supply +3.3V
2	GND	Ground	4	GND	Ground

【RSUB_BWBRP-1】

1. Scope

This board is combined with RMAIN_BWBRP-1 and conversion for making external connection is performed.

It connects with External GPIO, LCD, CRT and a touch panel board as the external interface.

Power supply (5.0V, 3.3V, 12.0V) to RMAIN_BWBRP-1.

2. System Configuration

Figure 2-1 shows the system configuration.

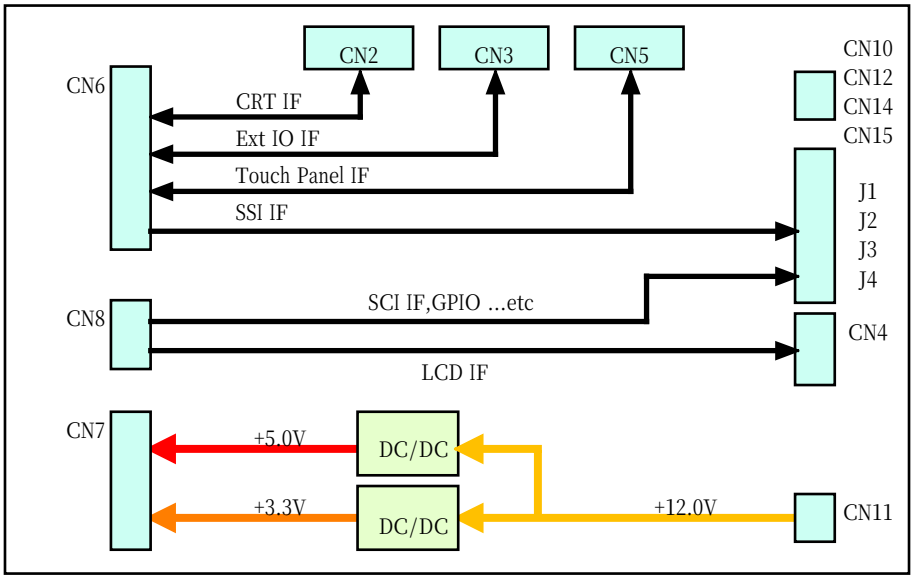


Figure 2-1 System Configuration

3. Connector Specification

Figure 3-1 shows the allocation of parts. Table 3-1 shows a list of connectors. The specifications are described below.

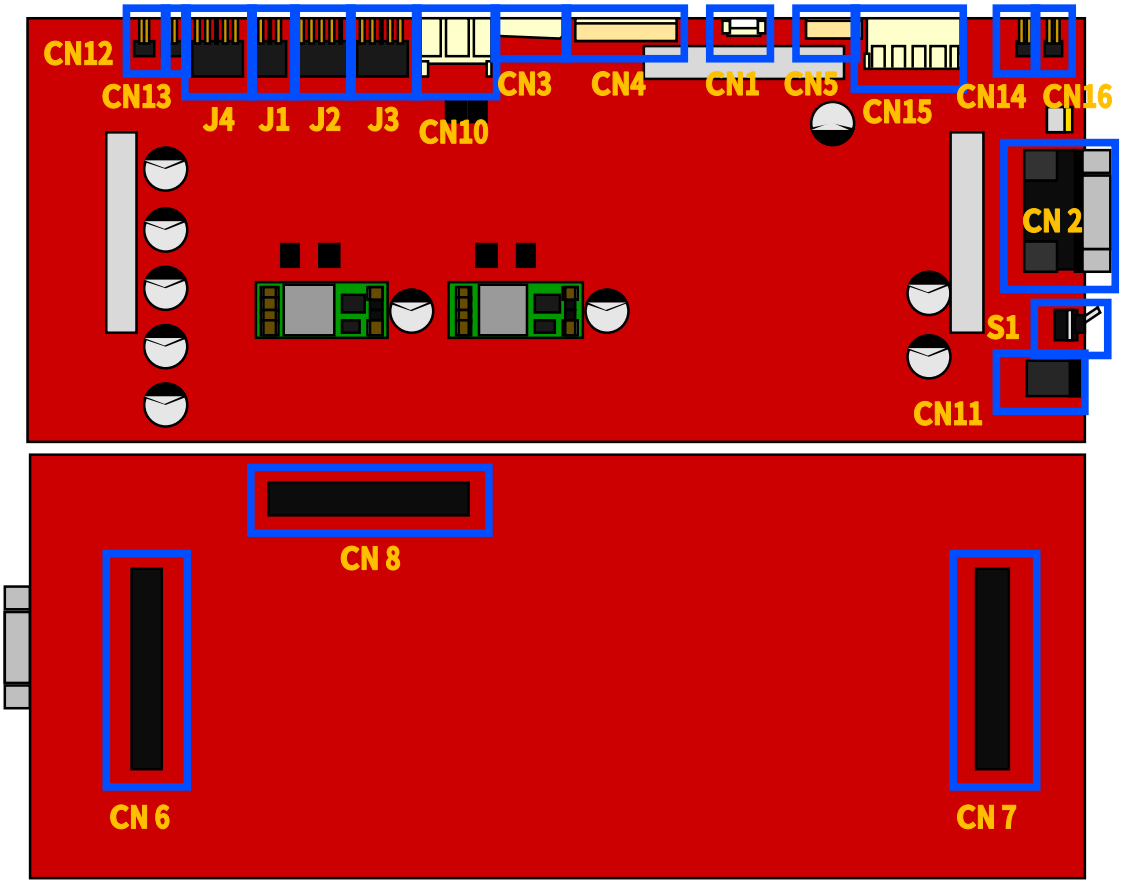


Figure3-1 Parts Allocation

Table3-1 List of Connectors

Ref No.	Function	Note	Ref No.	Function	Note
CN1	LCD Inverter Connector		CN10	Extension Power Supply	
CN2	CRT Connector	Shrink DSUB 15	CN11	AC Adapter Connector	
CN3	Ext IO Board Connector		CN12.13.14.16	FAN Power Supply	DC12V
CN4	LCD Connector		CN15	HDD Power Supply	
CN5	Touch Panel Connector		J1	Internal Signal Monitor	
CN6	MAIN_BWB B to B		J2	Reserved	
CN7	MAIN_BWB B to B		J3	Reserved	
CN8	MAIN_BWB B to B		J4	Extension Power Control	
CN9	ATX Power Connector	Option			

3.1 LCD Cable Connection

CN4 is LCD connector. The pin assignment specifications are as follows:

Connector type: 40FLH_SM1 Manufacturer: JST					
Pin No.	Signal	Function	Pin No.	Signal	Function
1	GND	Ground	21	GND	Ground
2	TFT_DOTCLK		22	TFT_B0	
3	GND	Ground	23	TFT_B1	
4	TFT_HSYNC		24	TFT_B2	
5	GND	Ground	25	TFT_B3	
6	TFT_VSYNC		26	TFT_B4	
7	GND	Ground	27	TFT_B5	
8	TFT_R0		28	GND	Ground
9	TFT_R1		29	TFT_ENB	
10	TFT_R2		30	GND	Ground
11	TFT_R3		31	GND	Ground
12	TFT_R4		32	R/L	
13	TFT_R5		33	U/D	
14	GND	Ground	34	TFT_VDD	
15	TFT_G0		35	TFT_VDD	
16	TFT_G1		36	TFT_VDD	
17	TFT_G2		37	TFT_VDD	
18	TFT_G3		38	TFT_VDD	
19	TFT_G4		39	TFT_VDD	
20	TFT_G5		40	TFT_VDD	

3.2 LCD Inverter Cable Connection

CN1 is inverter cable connector. ON/OFF control of an inverter and brightness adjustment of LCD.

The pin assignment specifications are as follows:

Connector type:53261-0590 Manufacturer: Molex					
Pin No.	Signal	Function	Pin No.	Signal	Function
1	VCC	Supply +12.0V	4	VR0	Brightness 0
2	GND	Ground	5	VR1	Brightness 1
3	VRMT	ON/OFF			

3.3 Connector for the CRT Monitor

CN2 is CRT connector. The pin assignment specifications are as follows:

Connector type:KEY-15S-2A2B Manufacturer: JAE					
Pin No.	Signal	Function	Pin No.	Signal	Function
1	SH_R		9	NC	Not connected
2	SH_G		10	AGND	Analog Ground
3	SH_B		11	NC	Not connected
4	NC	Not connected	12	NC	Not connected
5	AGND	Analog Ground	13	SH_HSYNC	
6	AGND	Analog Ground	14	SH_VSYNC	
7	AGND	Analog Ground	15	NC	Not connected
8	AGND	Analog Ground			

3.4 External GPIO board Connection

CN3 is External GPIO board connector. The pin assignment specifications are as follows:

Connector type:DF20-30DP-1V Manufacturer: HIROSE					
Pin No.	Signal	Function	Pin No.	Signal	Function
1	EXT_GPIO0		2	EXT_GPIO1	
3	EXT_GPIO2		4	EXT_GPIO3	
5	EXT_GPIO4		6	EXT_GPIO5	
7	EXT_GPIO6		8	EXT_GPIO7	
9	GND	Ground	10	GND	Ground
11	SCI_TX0		12	SCI_RX0	
13	SCI_SCK0		14	IDENT0	Extension ID
15	GND	Ground	16	GND	Ground
17	SSI_DATA		18	SSI_SCK	
19	SSI_CK		20	IDENT1	Extension ID
21	GND	Ground	22	NC	Not connected
23	NC	Not connected	24	+5V	
25	+5V		26	IDENT2	Extension ID
27	+3.3V		28	+3.3V	
29	+3.3V		30	+3.3V	

3.5 Touch Panel Interface board Connection (Option)

CN5 is touch panel Interface board connector. The pin assignment specifications are as follows:

Connector type:14FLH-SM1 Manufacturer: JST					
Pin No.	Signal	Function	Pin No.	Signal	Function
1	+3.3V	Supply +3.3V	8	GND	Ground
2	+3.3V	Supply +3.3V	9	TP_BUSY	
3	TP_CLK		10	GND	Ground
4	GND	Ground	11	TP_DOUT	
5	TP_CSN		12	GND	Ground
6	GND	Ground	13	TP_IRQN	
7	TP_DIN		14	GND	Ground

3.6 RMAIN_BWBRP-1 Connection

CN6 is RMAIN_BWBRP-1 connector. The pin assignment specifications are as follows:

Connector type:TX25-60P-12St-H1 Manufacturer: JAE					
Pin No.	Signal	Function	Pin No.	Signal	Function
1	+3.3V	Supply +3.3V	31	+3.3V	Supply +3.3V
2	+3.3V	Supply +3.3V	32	+3.3V	Supply +3.3V
3	+3.3V	Supply +3.3V	33	+3.3V	Supply +3.3V
4	+3.3V	Supply +3.3V	34	+3.3V	Supply +3.3V
5	+3.3V	Supply +3.3V	35	+3.3V	Supply +3.3V
6	+3.3V	Supply +3.3V	36	+3.3V	Supply +3.3V
7	GND	Ground	37	GND	Ground
8	+5V	Supply +5.0V	38	+5V	Supply +5.0V
9	+5V	Supply +5.0V	39	GND	Ground
10	+5V	Supply +5.0V	40	SSI_DATA	
11	SSI_CLK		41	SSI_WS	
12	GND	Ground	42	GND	Ground
13	SCI_TX0		43	GND	Ground
14	SCI_RX0		44	SCI_SCK	
15	SCI_SCK0		45	EXT _GPIO3	
16	EXT _GPIO7		46	EXT _GPIO2	
17	EXT _GPIO6		47	EXT _GPIO1	
18	EXT _GPIO5		48	EXT _GPIO0	

19	EXT _GPIO4		49	IDENT2	Extension ID
20	IDENT1	Extension ID	50	IDENT0	Extension ID
21	TP_DIN		51	TP_DOUT	
22	TP_BUSY		52	GND	Ground
23	TP_IRQ		53	TP_CLK	
24	GND	Ground	54	GND	Ground
25	SH_G		55	TP_CSN	
26	AGND	Analog Ground	56	GND	Ground
27	SH_B		57	SH_R	
28	AGND	Analog Ground	58	AGND	Analog Ground
29	SH_VSYNC		59	SH_HSYNC	
30	AGND	Analog Ground	60	GND	Ground

3.7 RMAIN_BWBRP-1 Connection

CN7 is RMAIN_BWBRP-1 connector. The pin assignment specifications are as follows:

Connector type:TX25-60P-12St-H1 Manufacturer: JAE					
Pin No.	Signal	Function	Pin No.	Signal	Function
1	+3.3V	Supply +3.3V	31	+3.3V	Supply +3.3V
2	+3.3V	Supply +3.3V	32	+3.3V	Supply +3.3V
3	+3.3V	Supply +3.3V	33	+3.3V	Supply +3.3V
4	+3.3V	Supply +3.3V	34	+3.3V	Supply +3.3V
5	+3.3V	Supply +3.3V	35	+3.3V	Supply +3.3V
6	+3.3V	Supply +3.3V	36	+3.3V	Supply +3.3V
7	GND	Ground	37	GND	Ground
8	GND	Ground	38	GND	Ground
9	GND	Ground	39	GND	Ground
10	GND	Ground	40	GND	Ground
11	GND	Ground	41	GND	Ground
12	GND	Ground	42	GND	Ground
13	+5V	Supply +5.0V	43	+5V	Supply +5.0V
14	+5V	Supply +5.0V	44	+5V	Supply +5.0V
15	+5V	Supply +5.0V	45	+5V	Supply +5.0V
16	+5V	Supply +5.0V	46	+5V	Supply +5.0V
17	+5V	Supply +5.0V	47	+5V	Supply +5.0V
18	+5V	Supply +5.0V	48	+5V	Supply +5.0V

19	GND	Ground	49	GND	Ground
20	GND	Ground	50	GND	Ground
21	GND	Ground	51	GND	Ground
22	GND	Ground	52	GND	Ground
23	GND	Ground	53	GND	Ground
24	GND	Ground	54	GND	Ground
25	+12V	Supply +12.0V	55	+12V	Supply +12.0V
26	+12V	Supply +12.0V	56	+12V	Supply +12.0V
27	+12V	Supply +12.0V	57	+12V	Supply +12.0V
28	GND	Ground	58	GND	Ground
29	GND	Ground	59	GND	Ground
30	GND	Ground	60	GND	Ground

3.8 RMAIN_BWBRP-1 Connection

CN8 is RMAIN_BWBRP-1 connector. The pin assignment specifications are as follows:

Connector type:TX25-60P-12St-H1 Manufacturer: JAE					
Pin No.	Signal	Function	Pin No.	Signal	Function
1	+5V	Supply +5.0V	31	TFT_R0	
2	+5V	Supply +5.0V	32	TFT_R1	
3	+5V	Supply +5.0V	33	TFT_R2	
4	+5V	Supply +5.0V	34	GND	Ground
5	GND	Ground	35	TFT_R3	
6	TFT_G0		36	TFT_R4	
7	TFT_G1		37	TFT_R5	
8	TFT_G2		38	TFT_B0	
9	TFT_G3		39	TFT_B1	
10	TFT_G4		40	TFT_B2	
11	TFT_G5		41	TFT_B3	
12	GND	Ground	42	TFT_B4	
13	TFT_VSYNC		43	TFT_B5	
14	TFT_ENB		44	GND	Ground
15	GND	Ground	45	TFT_DOTCLK	
16	TFT_VDD		46	TFT_HSYNC	
17	TFT_VDD		47	TFT_BKLED_EN	
18	TFT_VDD		48	TFT_CLAMP	

19	CF/HDD_LED		49	TFT_CDE	
20	RESET_LED		50	GND	Ground
21	CAN_ERRN		51	CAN_RX	
22	GND	Ground	52	GND	Ground
23	SCI_TX9		53	CAN_TX	
24	SCI_RX9		54	GND	Ground
25	SCI_SCK9		55	SH_GPIO29	
26	GND	Ground	56	SH_GPIO28	
27	GPS_CLK		57	SH_GPIO27	
28	GPS_IN		58	SH_GPIO26	
29	GND	Ground	59	SH_GPIO25	
30	GND	Ground	60	SH_GPIO24	

3.9 Power Out for External board

CN10 is a connector for cable splicing for extended board power supply. The pin assignment specifications are as follows:

Connector type:DF1E-6P-2.54DS Manufacturer: HIROSE					
Pin No.	Signal	Function	Pin No.	Signal	Function
1	+5V	Supply +5.0V	4	GND	Ground
2	GND	Ground	5	+12V	Supply +12.0V
3	+3.3V	Supply +3.3V	6	GND	Ground

3.10 DC12V Input

CN11 is a connector for supplying DC12V from an external AC/DC adaptor.

3.11 Power-Supply for FANs

CN12, 13, 14 and 16 are power supply for FANs. The pin assignment specifications are as follows:

Connector type:A2-2PA-2.54DS Manufacturer: HIROSE					
Pin No.	Signal	Function	Pin No.	Signal	Function
1	+12V	Supply +12.0V	2	GND	Ground

3.12 Power-Supply for the HDD

CN15 is power supply for HDD drive. The pin assignment specifications are as follows:

Please use the commercial power supply extension cable.

Connector type:770149-1 Manufacturer: AMP					
Pin No.	Signal	Function	Pin No.	Signal	Function
1	+12V	Supply +12.0V	3	GND	Ground
2	GND	Ground	4	+5V	Supply +5.0V

3.13 LED Board Connection (Option)

J1 is internal signal monitor connector. This connector connects with an LED board. The pin assignment specifications are as follows:

Connector type:A1-6PA-2.54DS Manufacturer: HIROSE					
Pin No.	Signal	Function	Pin No.	Signal	Function
1	TFT_CLAMP		2	+3.3V	Supply +3.3V
3	TFT_CDE		4	GND	Ground
5	CF/HDD_LED		6	RESET_LED	

3.14 Reserved Connector

J2 is reserved connector. It is used when required. The pin assignment specifications are as follows:

Connector type:A1=10PA-2.54DS Manufacturer: HIROSE					
Pin No.	Signal	Function	Pin No.	Signal	Function
1	GPS_CLK		2	SCI_TX9	
3	GPS_IN		4	SCI_RX9	
5	CAN_ERRN		6	SCI_SCK9	
7	CAN_RX		8	GND	Ground
9	CAN_TX		10	GND	Ground

3.15 Reserved Connector

J3 is reserved connector. It is used when required. The pin assignment specifications are as follows:

Connector type:A1-10PA-2.54DS Manufacturer: HIROSE					
Pin No.	Signal	Function	Pin No.	Signal	Function
1	SH_GPIO5		2	SH_GPIO0	
3	SH_GPIO4		4	+3.3V	Supply +3.3V
5	SH_GPIO3		6	+3.3V	Supply +3.3V
7	SH_GPIO2		8	GND	Ground
9	SH_GPIO1		10	GND	Ground

3.16 Remote Power Control Connection

J4 is Power monitor and Power control connector. This connector connects with a Power control board. The pin assignment specifications are as follows:

Connector type:A1-10PA-2.54DS Manufacturer: HIROSE					
Pin No.	Signal	Function	Pin No.	Signal	Function
1	POW_ON/OFF	External SW Input	2	GND	Ground
3	VCC12V_LED	+12.0V Power Monitor	4	GND	Ground
5	VCC5V_LED	+5.0V Power Monitor	6	GND	Ground
7	VCC3.3V_LED	+3.3V Power Monitor	8	GND	Ground
9	+3.3V	Supply +3.3V	10	GND	Ground

4. Switch Specification

S1 is main power control switch.

Ref No.	Function
S1	Power ON/OFF

5. LED Specification

LED1-4 are used for power monitor. Each function is as follows.

Ref No.	Function
LED1	ATX5V SUB
LED2	Supply +12.0V
LED3	Supply +5.0V
LED4	Supply +3.3V