User's Manual

32

SH7372

User's Manual: Hardware

Renesas 32-Bit RISC Microcomputer
SH-Mobile Series

— Preliminary —

Renesas Electronics
www.renesas.com

Rev. 0.54 Nov. 26, 2010

Section 1-A SH-Mobile AP4 Overview

1-A.1 Overview of SH-Mobile AP4

The features of this LSI are listed in table 1.1.

Table1-A.1 Features of this LSI

Item		Features
System CPU	CPU	- ARM Cortex-A8 - 800MHz operation - VIC (vector interrupt function) incorporated - Supports the core standby mode - Trust Zone support - Jazzle-RCT
	VFP	- VFP support
	DSP	- NEON support
	MMU	- MMU support
	Cache	- I-Cache 32K Bytes(L1) - D-Cache 32K Bytes(L1) - Unified Cache 256K Bytes(L2)
	ETM	- Cortex-A8 ETM support - Coresignt ETB (4K Bytes) incorporated
Realtime CPU	CPU	- Renesas Technology original architecture (SH4AL-DSP) - 400MHz operation - RISC-type instruction set (upward compatible with SH series) - Super scalar design which executes two instructions simultaneously - Virtual address space: 4Gbytes - Eight-stage pipeline - Supports the core standby mode
	User break controller (UBC)	- For AP realtime CPU All of address, data values, access types, and data sizes can be specified as break conditions - Sequential break function supported Two break channels
	User debugging interface (H-UDI)	- E10A emulator for AP realtime CPU supported - Realtime branch trace - 4-Kbyte on-chip memory for executing high-speed emulation program

Item		Features
	DSP	- 400MHz operation - Mixture of 16-bit and 32-bit instructions - Multiplier, ALU, and barrel shifter - Extended Hardvard architecture for DSP data bus - Maximum of four parallel operations - Zero-overhead repeat loop control
	Memory management unit (MMU)	- 4-Gbyte address space, 256 address spaces (8-bit ASID) - Single virtual memory mode and multiple virtual memory mode - Supports multiple page sizes: 1 Kbyte, 4 Kbytes, 8 Kbytes, 64 Kbytes, 256 Kbytes, 1 Mbyte, 4 Mbytes, and 64 Mbytes - 4-entry full associative TLB for instructions - 64-entry full associative TLB for instructions and operands - Address mapping allows direct access to TLB contents
	Cache memory	- Instruction cache (IC) 32-Kbyte, 4-way set associative 32-byte block length - Operand cache (OC) 32-Kbyte, 4-way set associative 32-byte block length Selectable write mode (copy-back or write-through)
	X/Y memory	- Four independent read/write ports 8-/16-/32-bit operand access from CPU with virtual address Maximum two 16-bit access from DSP 8-/16-/32-bit operand access from CPU with physical address or instruction fetch access from CPU 8-/16-/32-/64-bit or 16-/32-byte access by external requests - Total of 16 Kbytes Memory protective functions specialized for DSP access in addition to memory protective functions for CPU access
Interrupt controller (INTC)		- 32 interrupt pins which can detect external interrupts - Fall/rise/high level/low level detection is selectable. - On-chip peripheral interrupts: Priority can be specified for each module - Supports Trust Zone

Item	Features
Direct memory access controller (DMAC)	- 18 channels for system domain, 12 channels for realtime domain - Address space: 4 Gbytes on architecture - Data transfer length: Bytes, words(2 bytes), longwords(4 bytes), 8 bytes, 16 bytes, 32 bytes and 64bytes - Maximum number of transfer times: 16,777,216 times - Address mode: Dual address mode - Transfer request: Selectable from on-chip peripheral module request and auto request - Bus mode: Selectable from cycle steal mode (normal mode and intermittent mode) and burst mode - Priority: Selectable from fixed channel priority mode and round-robin mode - Interrupt request: Supports interrupt request to CPU at the end of data transfer - Repeat function: Automatically resets the transfer source, destination, and count at the end of DMA transfer - Reload function: Automatically resets the transfer source, destination at the end of the specified number of DMA transfers - Half end interrupt, n/4 transfer end interrupt, m/8 transfer end interrupt support - High-speed transfer to peripheral modules with multi-byte transfer function(16 bit x 8, 32 bit x 4)
Timer Unit (TMU)	- 2 sets of 3 channel 32-bit timer (in realtime domain) - Auto-reload type 32-bit down counter - Internal prescaler for SUBϕ - Interrupt request
Timer pulse Unit (TPU)	- 4 channel 16-bit timers - Each channel outputs PWM
Compare match Timer (CMT)	- 32-bit timer, 10 channel (16 bits/32 bits can be selected) - Source clock : RCLK/system clock - Compare match function provided - Interrupt requests - 1 of 10 channel supports DMA request

Item	Features
Clock-synchronized serial interface with FIFO (MSIOF)	- Internal 5 channels (MSIOF: 4 channels on system domain, 1 channel on real-time domain) - Internal 64 Byte transmit FIFOs/internal 256 Byte receive FIFOs - Clock synchronous serial master/slave mode, support full-duplex communication Supports 8/16 bit data and 16-bit stereo audio input/output Support 24bit stereo audio input/output Sampling rate clock input selectable from SUBϕ and external pin Internal prescaler - SPI master/slave mode, support full-duplex communication Serial clock(SCK) rise/fall edge selectable for data sampling timig SCK clock phase selectable for transmit timing 3 slave devices selectable Transmit/receive data length selectable from 8, 16, 32bits - Interrupt request, DMAC request, and DMA multi-byte transfer supported
Serial communication interface with FIFO (SCIFA)	- 6 channels - Internal 64-byte transmit/receive FIFOs - High-speed UART - Internal prescaler for SUBϕ - Clock synchronous serial communications possible - Support edge selection function - Interrupt request, DMAC request and DMA multi-byte transfer supported
Serial communication interface with FIFO (SCIFB)	- 1channel - Internal 256-byte transmit/receive FIFOs - High-speed UART - Internal prescaler for SUBϕ - Clock synchronous serial communications possible - Support edge selection function - Interrupt request, DMAC request and DMA multi-byte transfer supported
I2C bus interface (IIC)	- 5 channels - Supports single master transmission/reception - Interrupt request - DMAC request

Item	Features
NAND flash memory controller (FLCTL)	- Directly connected memory interface with NAND-type flash memory - Read/write in sectors - Two types of transfer modes: Command access mode and sector access mode (512-byte data + 16-byte management code: with ECC) - Supports up to 16Gbit of flash memory - 4 symbols correction - Interrupt request, DMAC request and DMA multi-byte transfer supported - Bus arbitration functions between BSC(NOR Flash) access and FLCTL access - Supports 2K Byte page
Multifunctional interface (MFI)	- One channel (BSC and asynchronous bus are connected between 2 CPUs) - Data can be read/written in 32 bits from/to shared on-chip RAM (MFRAM: 1 Kbyte) between CPUs - MFRAM is accessible from MFI/CPU. - Data can be transferred between CPUs using MFRAM and interrupt function along with software. - Seven external source bits for controlling 128 types of interrupts
Multifunctional interface2 (MFI2)	- Interface providing high-speed data transfer to/from external devices that cannot share any system buses - Data can be read/written in 32 bits from/to on-chip RAM (MFRAM: 8 KBytes) - Also direct accessing to DDR-RAM of SH-Mobile is available. - MFRAM is accessible from MFI/CPU. - Data can be transferred between this LSI and external devices using MFRAM and interrupt function along with software. - Internal boot access that considers MFRAM a reset vector - Internal semaphore register in MFI that allows read modify write transfer when reading data from baseband side - Seven external source bits for controlling 128 types of interrupts
USB Host & Function Module (USB)	- 2 channels supported - USB Host -Compliance with USB2.0 -Support OTG Dual-Role devices - USB Function -Compliance with USB2.0 (High-Speed) -Module input Clock: 48MHz, internally 480MHz generated - Interrupt request - Internal dedicated DMA - 3.3V power for USB-PHY can be off while not using.

Item	Features
Encryption Engine (Crypto Cell5.2)	- PKA Engine -Diffie-Hellman -RSA - Hash Engine -SHA1 -SHA-256 -MD5 - Bulk Encryption Engine -DES,3DES -AES - Internal Digital Random Number Generator (RNG) - On-chip secure DMA as SHwy master - Multi-Flow Manager function is added.
Sound Processing Unit (SPU2)	- On-chip Audio-DSP (24-bit Dual MAC) - Dedicated DMAC: 3 channels - Direct connection interface with FSI, FMSI, and BBIF2 - PRAM 192K Byte, XRAM 192K Byte, YRAM 96K Byte
IPMMU	- Hardware IP makes memory area (controlled by OS) accessible by virtual address. - Compatible with MMU of ARMv6 architecture - Hardware page table walk function - 64 entry TLB - IP which can use IPMMU is as below. ISP, CEU, VEU, BEU, VPU, 2D-DMAC, LCDC, JPU, RT-DMAC
Capture Engine Unit (CEU)	- CEU Block (image capturing from camera module) (a)Camera module interface Data (8 bits: YCbCr 4:2:2), horizontal sync signal (HD), vertical sync signal (VD) JPEG camera interface with data enable and variable data length capturing as parallel interface Connection with MIPI-CSI2 interface (b) Size of captured image: 15M pixels, 8M pixels, 5M pixels, 3M pixels, 2M pixels UXGA, SXGA, XGA, VGA, CIF, QVGA, QCIF, QQVGA, Sub-QCIF,48 x 48, (configuration is up to 8000 x 8000) (c) Output image format: YCbCr4:2:2, YCbCr4:2:0, JPEG data (d) Image format conversion function Reduced image generating prefilter function YCbCr 4:2:2 to YCbCr4:2:2, YCbCr4:2:0 YCbCr format(Y:8bit /CbCr:16bit) (e) Edge selection for capture clock (f) Frame drop function (1/2, 1/3, 1/4, 1/5, 1/6 drop)

Item	Features
Video Engine Unit (VEU)	VEU block (Image processing in memory) - 4 blocks are embedded. (2 blocks have FIR filter) (a) Video image processing function Input image format: YCbCr image (Y/CbCr plane image), RGB image (RGB pack image) Output image format: YCbCr image (Y/CbCr plane image), RGB image (RGB pack image) Image processing function: -Scaling image generating filter function (input up to 8188 x 8188, output up to 4092 x 4092) - YcbCr to RGB / RGB to YCbCr conversion function - Dithering function (in RGB color subtraction) (b) Filter processing function - Mirroring, vertical inversion, point symmetry - Deblocking filter - Median filter (c) Video image processing and filter processing combined operation.
Blend Engine unit (BEU)	BEU block (Image blending) - 3 blocks are embedded. (a) Blend function - Input image format: YCbCr image (Y/CbCr plane image), A+YCbCr image (A+YCbCr pack image), RGB image (RGB pack image), ARGB Image (ARGB pack image), A+RGB image (A + RGB pack image) - Output image format: YCbCr image (Y/CbCr plane image), A+YCbCr image (A+YCbCr pack image),RGB image (RGB pack image), ARGB image (ARGB pack image), A+RGB image (A + RGB pack image) (b) OSD function - Input format: RGB, ARGB/ YCbCr, AYCbCr image - Output format: RGB, ARGB/ YCbCr, AYCbCr image (c) Blend and OSD operation Two PinP planes and one OSD plane can be blended simultaneously (d) Results of processing are written back to memory
2 Dimensional DMAC (2DDMAC)	- Supports 8 channels transfer (In case of YUV, channels are assigned to Y plane and UV plane respectively). - Supports the image clipping by 1-pixel for RGB and by 2-pixel for YUV. - Function to inverse vertically or horizontally and rotate 90, 270 degree - The format conversion between various RGB formats - The image is scaled up by a factor of 2 in the X direction and the Y direction, respectively

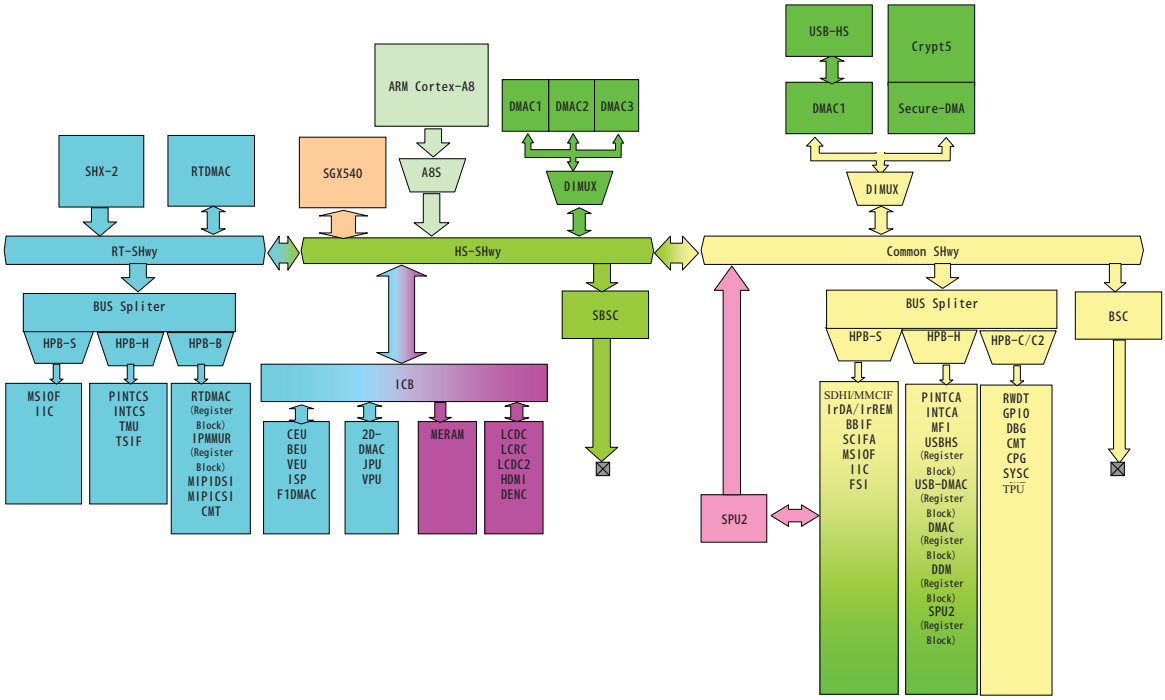
Item	Features
Video Processing Unit (VPU)	- Applicable standard: - H.264 : High Profile, Main Profile, Baseline Profile - MPEG-2: Main Profile - MPEG-4: Advanced Simple Profile (*) - H.263: Baseline - VC-1: Simple Profile, Main Profile, Advanced Profile Note: (*) Some Tools (ASO/FMO/RS) are not supported - Image size: Sub-QCIF to D1, 1280X720, 1920X1080 - Bit Rate: Maximum 40 Mbps
LCD- Controller (LCDC)	- Supported LCD panel: TFT color LCD, WXGA+ - Input data format: 8, 12, 16, 18, 24, or 32bpp - LCD driver interface — Specialized LCD bus, independent of memory bus — RGB interface or 80-series CPU bus interface selectable — Bus width: 8, 9, 12, 16, 18, or 24 bits — One-pixel one-time, two-time, or three-time transfer mode selectable — Signal polarity and SYNC output timing and width programmable in RGB interface — Access cycle programmable in 80-series CPU bus interface - Dot clock: Bus clock, peripheral clock, or external clock selectable as the source clock - Display data fetch: Continuous mode according to the refresh rate of the LCD panel and one-shot mode according to the frame rate of the movie are supported. Image data can be fetched only for updated sections. - Maximum Display Size : 1440 x 900 - Built-in 256-entry, 24-bit-output color palette - Interrupt can be generated it on the user-specified line - Maximum 1.5MByte Frame data cache available on ICB. Auto-refresh on ICB without external memory accessing - Blend function - MIPI-DSI (Max. 850MHz, 4lane) connectable
Media RAM (MERAM)	- 1.5MByte size - Manageable up to maximum 32line buffer - Can be used as Read-fill Buffer & Write-back Buffer for Multi-Media-IPs such as VPU, VEU,etc. - Can be used as intermediate buffer between 2 Multi-Media-IPs. - On-chip tile linear conversion supported in IPMMU of MERAM. - Read-fill and Write-back Buffers are managable by a block. Buffer size for IP which performs tile access can be reduced. - Relevant IPs : CEU, VEU0-3, BEU0-2, 2D-DMAC, VPU, LCDC, JPU, ISP & SHwy Bus target.

Item	Features
JPEG Processing Unit (JPU)	- Conforming specification: JPEG baseline - Operating precision: Conforming to JPEG Part 2, ISO-IEC10918-2 - Color format: YCbCr 4:2:2, YCbCr 4:2:0 - Quantization tables: Four tables - Huffman tables: Four tables (two AC tables, two DC tables) - Target markers: Start of image (SOI), start of frame type 0 (SOF0), start of scan (SOS), define quantization tables (DQT), define Huffman tables (DHT), define restart interval (DRI), restart (RSTm), end of image (EOI)
3D Graphic Engine	- Imagination Technologies SGX 540 - Universal Scalable Shader Engine(USSE) - Programmable architecture - Latency tolerant architecture - Internal True Colour - Video processing for multi-standard video decode and encode - API Support :OpenGL ES1.1/2.0,Open VG, Direct 3D Mobile
TS Interface (TSIF)	- 1 channel - Serial TS data input - Filters for 26 kinds of PIDs in total (The PID values of PAT and CAT packets are fixed. For PCR, video, and audio packets, the PID values are predefined.) - ISDB-T 3-segment compliant (Max. 2Mbps) - DMA Multi byte transfer
FIFO attached Serial Interface (FSI/FMSI)	- 24bit Stereo Quality (FMSI also supports 16bit) - Supports PCM & I2S formats - Supports SPDIF - Serial Input/Output can be directly connected with external A/D, D/A converter. - Connected with SPU2 internally
IrDA controller (IrDA)	- IrDA 1.1/1.3 compliant , SIR/MIR/FIR supported - Auto receive mode available. - Transfer unit : Frame
MIPI camera serial interface 2 (CSI2)	- 2 channels (MAIN:4 lanes , SUB :2 lanes) data interface - SUB channels can receive YUB420, YUB422 and generic format packet with CEU. - MAIN channels can receive RAW8,RAW10 and RAW12 format packet with ISP. - Frequency: up to 850MHz / Lane
MIPI display serial interface (DSI)	- 2 channels (4 lanes and 2 lanes) for main and sub displays - Supports video mode output linked to LCDC(RGB565, RGB666, loosely-packed666, RGB888) - DMA controller included for command mode, 4ch transfer available - Interleaved command packet output in video mode supported. - Frequency: up to 850MHz / Lane
HDMI	- HDMI v1.3a / DVI v1.0 Transmitter with HDCP v1.2 compliant - HDMI PHY Integrated - Internal NV memory for HDCP Key - 5.1ch multi-channel Audio supported up to 192kHz - CEC support

Item	Features
Image Signal Processor (ISP)	- Max 16M pixels Still Images & Full HD1080p Movie images - Recoding format: JPEG (DCF / Exif2.21 compliant), DPOF (Ver1.1), YCbCr4:2:2 file - Sensor format: 8/10bit RAW - 3A controller: AF, AE and AWB - Lens Shading & Distortion Compensation for Sensor - Defect Pixel Correction for Sensor - Anti-Shake Image Stabilization Functions - Intelligent Image Noise Reduction Features: Multi-band Filter, Specific Color Filter
MIPI-HSI	- Interface providing high-speed data transfer to/from external devices. - MIPI HSI ver 1.01.00 base - Two pairs of uni-directional transmitter/receiver pairs, where both pairs consist of two data signals and two control signals. - Transfer speed: 100Mbit/sec(Max)
MMCIF	- eMMC controllable - Data bus : 1/4/8 bit MMC mode (not support SPI mode) - Support block transfer (not support stream transfer) - Block size in multi-block transfer : 512 byte
SD card host interface (SDHI)	- 3 channels supported - SD memory & I/O card interface - Card Detection Function - Interrupt Request & DMA transfer request - High-Speed support - High Capacity support
Bus State Controller (BSC)	- Supports 6 Physical address areas in total: two areas (areas 0 and 2) of up to 128 Mbytes each, one area (area 4) of up to 64 Mbytes, and three areas (areas 5A, 5B and 6A) of up to 32 Mbytes each. Chip select signal assigned to each area respectively. - Data bus width: 16 bits - Setup/Hold timing setting individually at Read/Write - Address/Data Multiplexed memory support (Up to 1Gbit case) - Address/Data Non-Multiplexed memory support (Up to 1Gbit case) - Synchronous access & Page access functions of the asynchronous bus added - 4/8 word changeable in Page-mode - BS Pulse width adjustment function available
Bus State controller for SDRAM (SBSC)	- LPDDR2-SDRAM(S4) can be directly connected - Up to 2Git memory x2 can be connected - Data bus width 64/32 bit - Auto Refresh / Self Refresh/ Partial Refresh Supported - Deep-Power-Down-Mode supported - Auto Pre-charge Mode / Bank Active Mode

Item	Features
Clock Pulse Generator (CPG)	- Generates the clocks from 26MHz External Clock (EXTAL1). Maximum CPU Clock System : 806MHz (Zϕ), Real Time : 398.6MHz(Iϕ) Maximum BUS Clock SHwy (RT/HS/Common) : 199.3MHz(ZSϕ) Maximum SDRAM bus clock : 199.3MHz(ZB3ϕ) Media Clock : 99.7MHz (Bϕ) BSC bus clock : 99,7MHz(ZBϕ) Maximum Peripheral Clock 99.7MHz(HPϕ) - Power-Down Mode supported. Core-Standby Mode supported. Module-Standby Mode supported
System Controller (SYSC)	- Control for Internal Power-Domain (Power-On, Shut Down & Resume) - Booting & reset controls for System-CPU, Real-Time CPU
RCLK Watchdog timer (RWDT)	- Internal 32-bit watchdog timer operated by RCLK RCLK input is necessary for LSI operation. - Programmable Overflow time-period : minimum 7.8ms~maximun 30min
I/O Port	- Individual setting below available for pins except some pins. Output ON/Off, Input On/Off, Pull-Down On/Off, Pull-Up On/Off, GPIO On/Off - Set & reset function for Port Data Register supported.
Endien	- Little Endian support
Package	- 12mm x 12mm , Height is T.B.D., Number of pins is 561., POP
Voltage	- I/O: 2.7~3.6V (Power Switching Macro) 1.65V~1.95V(eSD)/2.7V~3.6V (SDHI) 3.0V~3.6V (USB) 1.65V~1.95V (Others) - LPDDR2-SDRAM I/O: 1.14V~1.28V (1.2V typ.) - HDMI: 1.1V~1.2V , 2.25V~ 2.75V - Core: 1.1V~1.2V (1.15VTyp.)
Process	45nm Low Power CMOS Process Technology

1-A.2 SH-Mobile AP4 Block



Section 1-B Address Maps

1-B.1 Overview of Address Map

In this LSI, the domains are connected by a bridge, and each domain can access the other domain's resource through the bridge address defined by each domain. The address defined by each domain is used to access the same position in the memory space and common resources.

Table 1-B.1 Address Maps 1

Address	Target	Remarks
H'00000000 to H'07FFFFFF	BSC	Area 0 *4
H'08000000 to H'0FFFFFFF	BSC	Area 2 *4
H'10000000 to H'13FFFFFF	BSC	Area 4
H'14000000 to H'15FFFFFF	BSC	Area 5A
H'16000000 to H'17FFFFFF	BSC	Area 5B
H'18000000 to H'19FFFFFF	BSC	Area 6A
H'1A000000 to H'1BFFFFFF	BSC	Area 6B
H'1C000000 to H'1DFFFFFF	BSC	Area 7A
H'1E000000 to H'1FFFFFFF	BSC	Area 7B
H'20000000 to H'2FFFFFFF	BSC	H'00000000 to H'0FFFFFFF mirrored
H'30000000 to H'37FFFFFF	BSC	H'00000000 to H'07FFFFFF mirrored
H'38000000 to H'3FFFFFFF	Router	Address error *1
H'40000000 to H'5FFFFFFF	SBSC1	DRAM areas 0 and 1 *3
H'60000000 to H'7FFFFFFF	Router	Address error *1
H'80000000 to H'BFFFFFFF	Router	Address error *1
H'C0000000 to H'DFFFFFFF	Router	Address error *1
H'E0000000 to H'E0FFFFFF	Router	Address error *1
H'E1000000 to H'E1FFFFFF	Router	Address error *1
H'E2000000 to H'E2FFFFFF	Router	Address error *1
H'E3000000 to H'E3FFFFFF	Router	Address error *1
H'E4000000 to H'E4FFFFFF	Router	Address error *1

Address	Target	Remarks
H'E5000000 to H'E54FFFFF	AP realtime core	On-chip memory in AP-realtime core (XYRAM)
H'E5500000 to H'E56FFFFF	ICB register/MERAM	MERAM start address is H'E5580000
H'E5700000 to H'E5FFFFFF	Router	Address error *1
H'E6000000 to H'E6FFFFFF	HPBC	Peripheral module (system domain)
H'E7000000 to H'E7FFFFFF	HPBD	Peripheral module (system domain)
H'E8000000 to H'E81FFFFF	ICB register/MERAM	MERAM start address is H'E8080000 (mirror address for AP RT core)
H'E8200000 to H'EFFFFFFF	Router	Address error *1
H'F0000000 to H'FB3FFFFF	Router	Address error *1
H'FB400000 to H'FB7FFFFF	Router	Address error *1
H'FB800000 to H'FBFFFFFF	Router	Address error *1
H'FC000000 to H'FCFFFFFF	DBG/H-UDI	DBG/H-UDI
H'FD000000 to H'FDFFFFFF	3DG	Control register
H'FE000000 to H'FE0FFFFF	DMAC	Control register
H'FE100000 to H'FE3FFFFF	SPU	Control register
H'FE400000 to H'FE7FFFFF	SBSC1	Control register
H'FE800000 to H'FE8FFFFF	ICB	Image IP (VPU, VIO, JPU, or LCDC)
H'FE900000 to H'FEBFFFFF	ICB	Image IP (VPU, VIO, JPU, or LCDC)
H'FEC00000 to H'FEFFFFFF	BSC	Control register
H'FF000000 to H'FF1FFFFF	AP-realtime core	Error
H'FF200000 to H'FF3FFFFF	UBC/VCR	UBC/VCR
H'FF400000 to H'FF6FFFFF	Router	Note: The AP-system core indicates memory in the core.
H'FF700000 to H'FFBFFFFF	Router	Router registers and reserved area for router *2
H'FFC00000 to H'FFFFFFFF	HPB	Peripheral module (realtime domain)

Notes: 1. If access is made to an address error area, an error log is generated in the AP realtime core or a data abort is generated in the AP system core.
2. The router registers are the arbitration registers (RTPRARCR*, HSPRARCR* and CMPRARCR*) described in section 1-F, Bus Functions. The other addresses are reserved for use by the router. If access is made to such an address, an error response or an undefined value will be read.
3. For SDRAM area divisions, refer to section 7, Bus State Controller for SDRAM (SBSC).
4. If the EXTEND bit in the BSC common control register (CMNCR) is set to 1, CS0 and CS2 are merged to create a space of 256 Mbytes.

Table 1-B.2 Address Map 2

	Address [31:24]	Address [23:0]	Module	Power-Supply Area	SYS Interrupt	RT Interrupt	SYS DREQ	RT DREQ	Remarks
HPBC HPBD	E6/E7 *3 HPB1 (cpck)	00 0000	HPB	COMMON C5					
		02 0000	RWDT0		√	√			
		05 0000	GPIO						
		10 0000	DBG						
		13 0000	CMT2		√	√			
		13 8000	CMT1		√		√	√	
		14 0000	CMT3		√				
		14 8000	CMT4			√			
		15 0000	CPGA						
		18 0000	SYSC						
		1B 0000	KEYSCAN		√	√			
HPBC HPBD	E6/E7 *3 HPB2 (cpck)	40 0000		SYS A3SP					
		60 0000	TPU0		√		√	√	Zoom
HPBC HPBD	E6/E7 *3 HPB3 (hpck)	80 0000		SYS A3SP					
		85 0000	SDHI0		√		√	√	
		86 0000	SDHI1		√		√	√	
		87 0000	SDHI2		√		√	√	
		89 0000	USBHS0		√				
		8A 0000	USBHS-DMAC0		√				
		8B 0000	USBHS1		√				
		8C 0000	USBHS-DMAC1		√				
		90 0000	PINTC	A4S	√				
		94 0000	INTCA2						
		95 0000	INTCA3						
		98 0000	INTCA			√*1			
		9C 0000	INTCAUM						
		A0 0000	CC5	A3SP	√				
		A3 0000	FLCTL		√		√	√	

	Address [31:24]	Address [23:0]	Module	Power-Supply Area	SYS Interrupt	RT Interrupt	SYS DREQ	RT DREQ	Remarks
		A4 0000	HSI		√		√	√	
		A6 0000	MFIS	A4S	√				
		A7 0000	MFRAMS	C5					
		A8 0000	MFIM	A4S					
		B0 0000	BootROM						
		B1 0000							
		B7 0000	ACMFI1		√				
		B8 0000	ACMFI2		√				
		B9 0000	ACMFRAM				√	√	
		BA 0000							
		BD 0000	MMC	A3SP	√		√	√	
		BE 0000	HDMI		√	√	√	√	
		BF 0000	CEC		√	√			
HPBC HPBD	E6/E7 *3 HPB4 (subck)	C0 0000		A3SP					
		C2 0000	IIC1		√		√	√	
		C3 0000	SCIFB		√		√	√	Blue-Tooth
		C4 0000	SCIFA0		√		√	√	Felica
		C5 0000	SCIFA1		√		√	√	GPS
		C6 0000	SCIFA2		√		√	√	Finger-print
		C7 0000	SCIFA3		√		√	√	
		C8 0000	SCIFA4		√		√	√	UART
		C9 0000	BBIF1		√		√	√	Internally connected to MMIF in BB block
		CA 0000	BBIF2	A4MP	√		√	√	Switchable between system and realtime*2; internally connected to PCMSEL in BB block
		CB 0000	SCIFA5	A3SP	√		√	√	
		D0 0000	IrDA		√		√	√	
		D1 0000	IREM		√				
		D2 0000	IIC3		√		√	√	

	Address [31:24]	Address [23:0]	Module	Power-Supply Area	SYS Interrupt	RT Interrupt	SYS DREQ	RT DREQ	Remarks
		D3 0000	IIC4		√		√	√	
		E0 0000	MSIOF2		√		√	√	
		E1 0000	MSIOF1		√		√	√	
	E6 (There is no E7) HPB3 (hpck)	F0 0000							
		F1 0000	AP system core	A4S					
		F2 0000	SHWYSTATC		√		√	√	
		F3 0000	SHWYSTATH		√		√	√	
		F8 0000	CoreSight APB Bridge	D4					
		F9 0000	CoreSight APB Bridge						
	FE HPB3 (hpck)	00 0000	DMAC1	A3SP	√				
		01 0000	DMAC2		√				
		02 0000	DMAC3		√				
		04 0000	IPMMUD						
		08 0000	DDM		√				
		1F 0000	FSI2	A4MP	√		√	√	
		1F 8000	BCKDIV						
		20 0000	SPU		√	√			
LMB (bck)	FE	80 0000							
		88 0000	ISP	A3RI		√			
		90 0000	VPU	A3RV		√			
		91 0000	CEU	A4R		√			
		92 0000	VEU			√			
		92 4000	VEU(2)			√			
		92 8000	VEU(3)			√			
		92 C000	VEU(4)			√			
		93 0000	BEU			√			
		93 4000	BEU(2)			√			
		93 8000	BEU(3)			√			

	Address [31:24]	Address [23:0]	Module	Power-Supply Area	SYS Interrupt	RT Interrupt	SYS DREQ	RT DREQ	Remarks
		94 0000	LCDC	A4LC		√			
		95 1000	IPMMUI	A4R					
		98 0000	JPU			√			
		A0 0000	2DDMAC			√			
HPB (RT)	FF HPB1 (bck)	C0 0000		A4R					
		C1 0000	RTDMAC1			√			
		C2 0000	RTDMAC2			√			
		C3 0000	IPMMUR			√			
		C4 0000	IPMMUR2			√			
		C6 0000	DSI0	A4LC		√	√	√	
		C7 0000	DSI1			√	√	√	
		C9 0000	CSIRX	A4R		√			
		CA 0000	CMT0			√			
		CF 0000	SHWYSTATR		√		√	√	
	FF HPB2 (hpck)	D0 0000		A4R					
		D1 0000	PINTCS						
		D2 0000	INTCS2						
		D3 0000	INTCS		√*1				
		D4 0000	INTCSUM						
		D5 0000	INTCS3						
		E8 0000	TSIF0			√	√	√	
		E9 0000	TSIF1			√	√	√	
	FF HPB3 (subck)	F0 0000		A4R					
		F1 0000	MSIOF0			√	√	√	
		F2 0000	IIC0			√	√	√	
		F3 0000	IIC2			√	√	√	
		F6 0000	TMU			√			For OS
		F7 0000	TMU1			√			

Address [31:24]	Address [23:0]	Module	Power-Supply Area	SYS Interrupt	RT Interrupt	SYS DREQ	RT DREQ	Remarks
	FA 0000	BBIF2	A4MP		√	√	√	Switchable between system and realtime*2; internally connected to PCMSE in BB block

Notes: 1. The relevant interrupt is processed as one interrupt source in the belonging domain, and it is necessary to read the interrupt source register to determine the interrupt.
2. For details on the register for switching the BBIF2 address, refer to section 1-F.4, HPB Bus Functions.
3. Accessed either from H'E6xx xxxx or H'E7xx xxxx. There is no functional difference due to the address selected. The arbitration of the access from H'E6xx xxxx or H'E7xx xxxx is done by hardware.

1-B.1.1 32-Bit Addressing Mode of AP-Realtime Core and Virtual and Physical Addresses

This LSI has the SH4AL-DSP core with extended functions and the addressing mode is changed from 29-bit mode in a conventional product to 32-bit mode. The differences between 29-bit addressing mode and 32-bit addressing mode are the relationship between the virtual addresses and physical addresses and their control method. For details, refer to section 3.3.

1-B.1.2 ROM Debugging Mode

This LSI supports ROM debugging mode. By using ROM debugging mode, a ROM program which is used for booting the internal ROM can be placed in an external memory to be debugged. This function is performed by switching the destination address to be fetched immediately after a boot from the internal ROM (for usual ROM boot mode) to BSC (for ROM debugging mode). The addresses to be accessed are automatically changed by hardware, which allows the software to debug the ROM program without any specific processing for ROM debugging mode. For details on the LSI boot mode settings, see section 11.1.3, Operating Modes.

Table 1-B.3 Address translation in ROM debugging mode

	AP-System Core
Address before translation by hardware *1	From 0x0000_0000
Address after translation by hardware	From 0x1000_0000
Range for address translation	Variable within range from 4 Kbytes to 512 Kbytes (Initial value: 4 Kbytes*2)

Notes: 1. The CPU starts program execution from PC address 0, which is translated to 0x1000_0000 by hardware.
2. APARMABAREA can be changed by using an instruction within 4 Kbytes after the ROM debugging mode booting. For details on APARMBAREA, see section 2.2.2.

1-B.1.3 Chip Version Registers

This LSI has the following three chip version registers. The register values are determined as shown in the bit field description in the following table unless otherwise specified in Errata or Technical Update.

Table 1-B.4 Chip Version Registers

Address	Register Name	Bit Field	Remarks
0xE600101C	CCCR (Common chip code register)	[31:16] Reserved [15:8]: Major number (AP4 = 0x2D) [7:4]: ES number (integer part –1) [3:0]: ES number (fraction part)	Accessible from all CPUs
0xFF000044	PRR (Product register)	[31:16] Reserved [15:8]: Major number (AP4 = 0x2D) [7:4]: ES number (integer part –1) [3:0]: ES number (fraction part)	Accessible only from AP_RT

Section 1-C Overview of Power Management

1-C.1 Power supply Management

To reduce the Leakage power consumption, this LSI is divided into various functional groups. Each functional group is assigned to a separate or multiple hierarchal power domains. The power supply to each area is controlled independently by a module called system controller (SYSC) which is located in C5 area whose power is always on. The leakage power can be reduced by shutting down the power supply of areas which are not required to operate according to the operating scenario.

As explained above, the power of areas which are not required to operate for a particular operating scenario can be turned off. To avoid the functional conflicts, the overall power domain is structured in hierarchal fashion as shown in figure 1-C.1. The bottom layer is an always power on area which is named as C5. Modules that are required to operate at all time are placed in this area. For example, modules required to process wakeup requests (System controller, Wakeup Controller) are placed in C5 area. Refer to Table 1-C.1 for list of module placed in each power domain. Modules that are rarely used are located in upper layers and modules used very often are located in lower layers

Figure 1-C.1 shows the power domain view and hierarchal relation between various power domains.

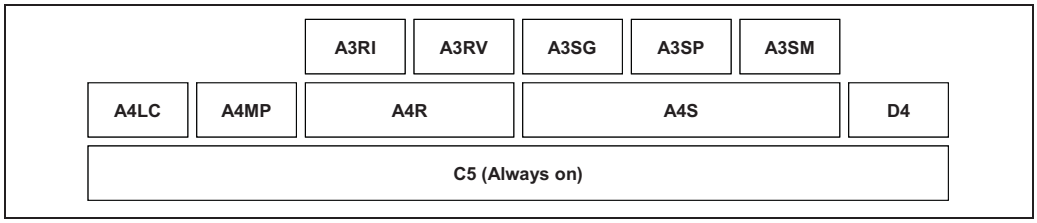


Figure 1-C.1 Power supply area hierarchy

Table 1-C.1 shows the modules located in each power Domain.

Table 1-C.1 Module assignment of each power Domain

	Area	Module
Common	C5	SYSC, PowerControlParts, GPIO, PAD (IO macro), HDMI-Phy, DBG
		Backup registers, CPG, CMT1/2/3/4, RWDT, KEYSC, SMFRAM
Debug	D4	Coresight-ETM
System	A4S	Common-SHwy, Common-HPB, BSC, MFIS,MFIM, MMFROM ACMFI1,ACMFI2, HS-SHwy, SYS-HPB, INTCA modules, SBSC
	A3SM	System CPU (Cortex-A8)
	A3SP	DMAC1/2/3, IPMMUD, DDM, FLCTL, SYS-HPB, BBIF1, MSIOF1/2, SCIFA,SCIFB, IIC1/3/4, IrDA, HDMI-Link, USBHS0/1, USBDMAC, SDHI0/1/2, CMT1, TPU, Crypt, DREQPAK (Sys), MIPI-HSI, MMCIF
	A3SG	SGX540
Realtime	A4R	Realtime CPU(SH-X2), Realtime CPU debug modules, H-UDI, RT-SHwy, INTCS modules, RT-HPB, TSIF, VPU, CEU, VEU, BEU, VOU, JPU, RTDMAC1/2,TSIF TMU, IIC0/2, MSIOF0, CMT0, ICB, DREQPAK (RT), 2DDMAC, IPMMUI,IPMMUR, IPMMUR2, CSI2
	A3RV	VPU
	A3RI	ISP
	A4LC	MERAM, LCDC, DSI
	A4MP	SPU2, FSI, FMSI, BBIF2

1-C.1.1 Backup registers

To speed up the wakeup time, the contents of some resources whose power is going to be turned off need to be preserved. The basic idea to implement it is to take a back up of those registers before shutting them down. So each resource will have a corresponding backup register which is placed in always power on area. All these backup registers are collectively placed in a module called Backup Module.

When the power is turned on these resources are initialized with the value stored in backup registers. The Backup registers are initialized only on power on reset or C5 area reset.

1-C.1.2 Power supply ON/OFF sequence

Power supply of each area of this LSI is controlled by SYSC. By Setting Power Down/Wakeup Control registers of SYSC, power down, wakeup requests can be generated .By accessing Power Status Control Register of SYSC, status of each power area can be monitored. Wakeup requests are also generated by wake up interrupts from external pin and peripheral modules. The areas (other than CPU) which can be waken up by wakeup interrupts are selected by SYSC configuration Registers.

The Basic flow of Power down and wakeup sequences is as follows.

(1) Power down Sequence

1. Check the write permission of bits in power down control registers by performing a read access to the corresponding Write block Control register.
2. Write 1 to the bit/bits of power down control registers to generate a power down request for corresponding areas. If the DLYED bit is also set along with these bits, the power down request is generated when CPU executes SLEEP/WFI instruction. If the DLYED bit is not set the power-down request is generated immediately. The power-down sequence starts immediately when the power-down request is issued and the system controller is in IDLE state. When the System controller is not IDLE, the generated requests are stored internally and power down sequence is executed when the System controller returns to the IDLE state.

The power down sequence is executed by SYSC in conjunction with CPG. The power down sequence is implements as follows.

A. The SYSC provides information of areas whose power is going to be turned off and issues a power down request to CPG.

B. The CPG issues area reset to the areas which are going to be turned off after bringing down the internal busses to IDLE state. Once it confirms that all the modules in that area are initialized, it stops the clock supply to that area even turns off PLL if the PLL off condition is met. Then, CPG sends back a power-down acknowledgement to the SYSC.

C. When power of an area is turned down, the output signals of that area are driven to unknown state, which might lead to drive the modules connected to those outputs also into unknown state. Therefore SYSC broadcasts a signal to all the modules which are receiving the outputs of modules whose areas is going to be turned down. From here on this broadcasting signal is called as ***Power isolation request*1*** and cell used by this signal to mask those unknown outputs are called as ***Power isolation Cell*1***.

D. As a last step in the sequence, SYSC issues a power down request to the corresponding Power Switch Controller .When the SYSC receives an acknowledgement from the Power

Switch Controller SYSC returns to IDLE state and clears the bits of the power control register.

(1) Wakeup Control

Wakeup sequence is triggered by wakeup request. The sources of Wakeup Requests

① By Setting up Wakeup control registers of SYSC
② By Wakeup interrupts generated by external pins and peripheral modules.

The sequence of operations when wakeup request is generated by Wakeup control register is as follows.

1. Check the write permission of bits in wakeup control registers by performing a read access to the corresponding Write block Control register.
2. Write 1 to the bit/bits of Wakeup control registers to generate a wakeup request for corresponding areas. The Wakeup request is generated immediately when bits in the wakeup control register are set. The wakeup sequence starts immediately when the wakeup request is issued and the system controller is in IDLE state. When the System controller is not IDLE, the generated requests are stored internally and wakeup sequence is executed when the System controller returns to the IDLE state.

The Wakeup sequence is also executed by SYSC in conjunction with CPG. The Wakeup sequence is implements as follows.

A. The SYSC issues a power-on request to the corresponding power switch controller and waits for acknowledgement signal.
   When turning on power switches of multiple areas, SYSC issues the power-on requests one at a time, it does not issue the request to all power switch controllers simultaneously. At first the power-on request is issued to area in the lower hierarchy. When it receives acknowledgement from the power switch controller of that area, it issues a power on request to the areas in the next level of that hierarchy and so on. When two areas of the same hierarchy are to wake up, the order of request generation is hardware dependent.
B. The SYSC issues a wakeup request to the CPG after all power switches are turned on and stable external clock is supplied to LSI.
C. The CPG continues to assert area reset which was issued at the time of power down sequence. CPG starts providing clock supply to all the modules which are going to be waken up. It restarts PLL circuits if PLL on condition is met. Once CPG confirms that all the modules of that area are properly initialized, it sends back wakeup acknowledgement to the SYSC.

D. When the SYSC receives the wakeup acknowledgment signal from CPG, it cancels power isolation request and signals CPG to release area reset to all modules. Then SYSC returns to IDLE state and clears the bits of wakeup control register are cleared to 0.

E. As a final step, CPG release area reset to all modules of that area

The wakeup procedure is same for wakeup requests generated by wakeup interrupts also. The wakeup interrupts are detected from various sources and a cumulative wakeup interrupt signals is generated for both SYS and RT domains as WakekupS, WakeupR respectively. Asserting these signals generates wakeup requests to the corresponding CPU. The areas that can be waken up by WakeUpS or WakeUpR are selected by Wakeup Selection control registers of SYSC.

.

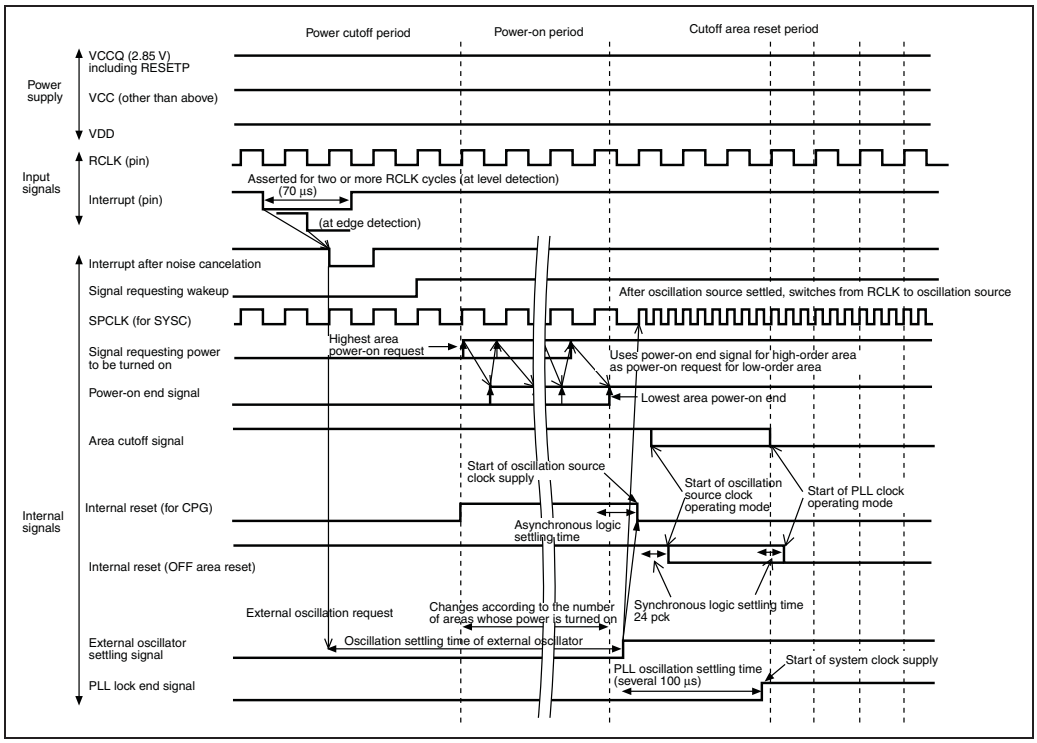


Figure 1-C.2 Wakeup Sequence by WakeUpR/WakeUpS Signal

1-C.2 Low Power State Definitions

The Following Low Power States are supported for this LSI

(1) CPU Power saving modes

- Sleep mode
  Clock supply to CPU is halted. The power of the CPU is on.
- Core Standby mode
  Clock supply to CPU is halted. The power of logic block of the CPU core is turned off, but the contents of memory modules of CPU (Cache, etc.,) are retained.

(2) Low Leakage mode

- Power-off
  Power supply of a specified power area is turned off. Refer to 1-C.1 and section 13, System controller (SYSC).

(3) Clock supply control

- Module stop
  Clock supply to a specified module is halted. Module stop is controlled by Module Stop control registers in CPG.
- Clock stop
  Whole clock domain of the specified clock is halted. Clock stop is controlled by clock control registers in CPG.

Section 1-D Overview of Reset

1-D.1 Reset Types

This LSI has five types of resets: power-on reset, system reset, power supply area reset, manual reset and software reset.

(1) Power-on Reset

A power-on reset is a reset to initialize all internal resources of this LSI. A power-on reset stops all processing and cancels the processing of all events that are yet to be processed. Two types of power on reset are defined for this LSI: “hard power-on reset” and “soft power on reset”.

A hard power-on reset is a reset controlled through the input pin RESETP, and it must be used when power is supplied to this LSI. The RESETP pin is a reset pin assumed to be asserted only when the power supply to this LSI is turned on, but asserting this pin in the normal operating state does not cause a problem. Following is a hard power-on reset sequence:

1. All external pins of the LSI are immediately transited to the reset state and kept that state until the hard power-on sequence finishes.
2. During power-on reset by RESETP pin is asserted, the power supply to internal power supply area are cut off, except an area which power is always on. After releasing RESETP pin, all internal power supply areas of the LSI are turned on sequentially.
3. Oscillation of the external clock (EXTAL1 and EXTAL2) inputs is enabled and operation is halted until the external clock input becomes stable.
4. All internal resources of the LSI are initialized.
5. The external pins are released from the reset state, and the boot sequence is started. Internal resets are negated and master processor starts instruction fetch from boot address.

A soft power-on reset is a reset controlled by reset control registers (RESCNT, RESCNT2) in the SYSC. The SRESLNK bit of RESCNT register in SYSC specifies whether the reset is handled as soft power on reset or as a system reset. See table 1-D.2 for detail of trigger of soft power on reset. Following is a soft power-on reset sequence:

1. If the power supply to certain area is off, the power supply is turned on until all of internal power supply areas of the LSI become powered on. If all of the internal power area is already on, this step is skipped.

2. If oscillation of the external clock (EXTAL1) input is halted, oscillation is enabled and operation is halted until the external clock input becomes stable. If the external clock input is already supplied, this step is skipped.
3. All internal resources of the LSI are initialized except some registers in SYSC.
4. Internal resets are negated and master processor starts instruction fetch from boot address.

Followings are example of internal resource not initialized by a soft power on reset.

- Example 1: Resources related to on-chip debugger in debug mode.
  Since these resources are saved, debugging of the reset sequence is possible.
- Example 2: Resources related to boot
  Though boot address of a hard power-on reset is determined by the setting of the mode pins, boot address after soft power-on reset can be set by the following registers: RBAR, SBAR of SYSC.

(2) System Reset

A system reset is a reset to re-execute from the initial state but keeping the status of D4 area and C5 area. A system reset is controlled through the input pin RESETA and reset control registers (RESCNT, RESCNT2) in the SYSC. A system reset stops all processing and cancels processing of all events that are yet to be processed. The SRESLNK bit of RESCNT register in SYSC specifies whether the reset is handled as soft power on reset or as a system reset. See table 1-D.2 for detail of trigger of system reset. Following is a system reset sequence:

1. If the power supply to certain area is off, the power supply is turned on until all of internal power supply areas of the LSI become powered on. If all of the internal power area is already on, this step is skipped.
2. If oscillation of the external clock (EXTAL1) input is halted, oscillation is enabled and operation is halted until the external clock input becomes stable. If the external clock input is already supplied, this step is skipped.
3. All internal resources of the LSI are initialized except D4 area and C5 area.
4. Internal resets are negated and master processor starts instruction fetch from boot address.

(3) Power Supply Area Reset

A power-supply area reset is a reset to initialize certain power supply area when the power supply of the area becomes off, and the power supply of the area becomes on. This reset is kept asserted until power of the relevant area is turned on again.

(4) Software Reset

A software reset is a reset to initialize specified module. A software reset can be issued by writing to the software reset register in CPG. For details, refer to the section 11.CPG.

Figure 1.13 is a diagram which shows the relationship between the power-on reset, system reset, power supply area reset, and software reset in this LSI.

(5) Manual Reset

A manual reset is a reset generated by RT-CPU core. Power supply area of RT domain (A3RI, A3RV and A4R) is initialized by the manual reset.

Figure 1-D.1 is a diagram of reset in this LSI.

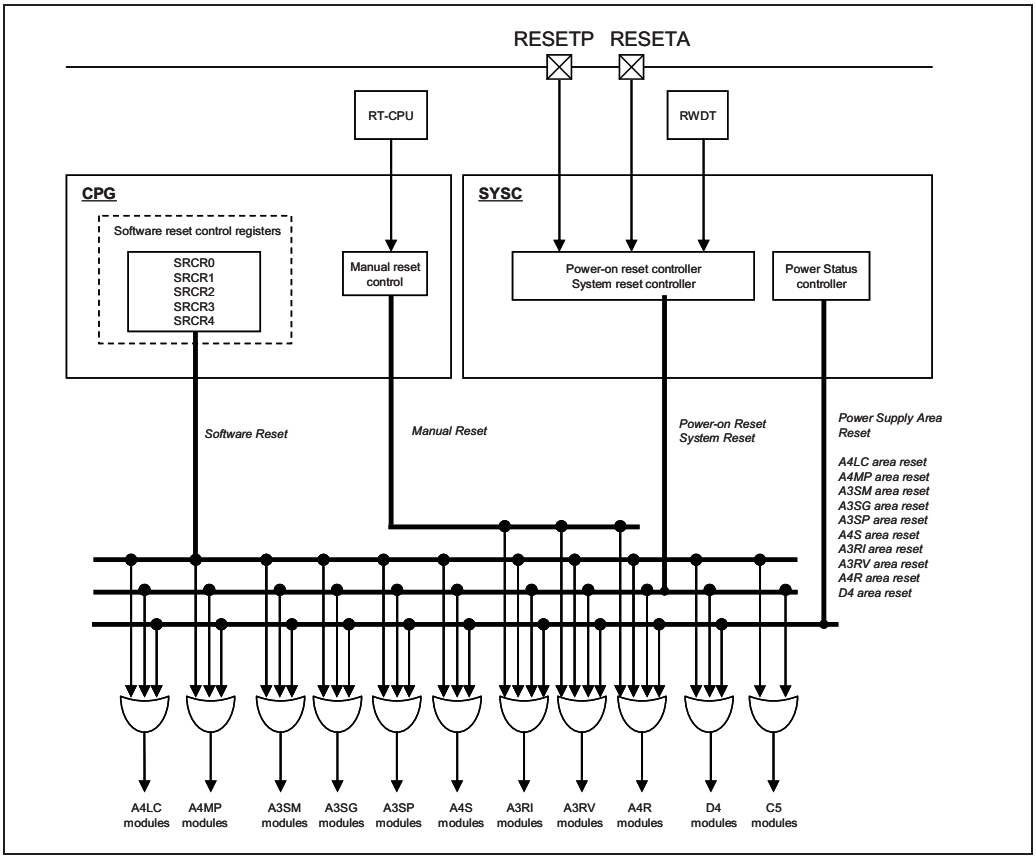


Figure 1-D.1 Reset Diagram

1-D.1.2 Reset condition of each module

Table 1-D.1 shows the reset condition of each module.

Table 1-D.1 Reset condition of each module

No	Domain	Module	Hard Power On Reset	Soft Power On Reset	Sytem reset	Power Area Reset												SH-X manual	Software reset (CPG)
						SYS-CPU core standby	A3SM	A3SP	A3SG	A4S	RT-CPU core standby	A3RV	A3RI	A4R	A4LC	A4MP	D4		
1	RT	Realtime CPU core	√	√	√	—	—	—	—	—	√	—	—	√	—	—	—	√	√
2		Realtime CPU DBG	√	√	√	—	—	—	—	—	√	—	—	√	—	—	—	√	√
3		H-UDI	√	√	√	—	—	—	—	—	√	—	—	√	—	—	—	√	√
4		SUBC	√	√	√	—	—	—	—	—	√	—	—	√	—	—	—	√	√
5		RT-SHwy	√	√	√	—	—	—	—	—	—	—	—	√	—	—	—	√	√
6		SHWYSTAT(RT)	√	√	√	—	—	—	—	—	—	—	—	√	—	—	—	—	—
7		INTCS	√	√	√	—	—	—	—	—	—	—	—	√	—	—	—	√	√
8		IPMMUR	√	√	√	—	—	—	—	—	—	—	—	√	—	—	—	√	√
9		IPMMUR2	√	√	√	—	—	—	—	—	—	—	—	√	—	—	—	√	√
10		RT-DMAC	√	√	√	—	—	—	—	—	—	—	—	√	—	—	—	√	√
11		RT-DMAC2	√	√	√	—	—	—	—	—	—	—	—	√	—	—	—	√	√
12		TMU0	√	√	√	—	—	—	—	—	—	—	—	√	—	—	—	√	√
13		TMU1	√	√	√	—	—	—	—	—	—	—	—	√	—	—	—	√	√
14		CMT0	√	√	√	—	—	—	—	—	—	—	—	√	—	—	—	√	√
15		CMT0 (Counter)	√	√	—	—	—	—	—	—	—	—	—	—	—	—	—	—	√
16		MSIOF0	√	√	√	—	—	—	—	—	—	—	—	√	—	—	—	√	√
17		IIC0	√	√	√	—	—	—	—	—	—	—	—	√	—	—	—	√	√
18		IIC2	√	√	√	—	—	—	—	—	—	—	—	√	—	—	—	√	√
19		CSI2-RX	√	√	√	—	—	—	—	—	—	—	—	√	—	—	—	√	√
20		CMOSIF	√	√	√	—	—	—		—	—	—	—	√	—	—		√	√
21		CEU	√	√	√	—	—	—	—	—	—	—	—	√	—	—	—	√	√
22		BEU0	√	√	√	—	—	—	—	—	—	—	—	√	—	—	—	√	√
23		BEU1	√	√	√	—	—	—	—	—	—	—	—	√	—	—	—	√	√
24		BEU2	√	√	√	—	—	—	—	—	—	—	—	√	—	—	—	√	√
25		VEU0	√	√	√	—	—	—	—	—	—	—	—	√	—	—	—	√	√
26		VEU1	√	√	√	—	—	—	—	—	—	—	—	√	—	—	—	√	√
27		VEU2	√	√	√	—	—	—	—	—	—	—	—	√	—	—	—	√	√
28		VEU3	√	√	√	—	—	—	—	—	—	—	—	√	—	—	—	√	√
29		VEU3	√	√	√	—	—	—	—	—	—	—	—	√	—	—	—	√	√
30		VPU	√	√	√	—	—	—	—	—	—	√	—	√	—	—	—	√	√

No	Domain	Module	Hard Power On Reset	Soft Power On Reset	Sytem reset	Power Area Reset												SH-X manual	Software reset (CPG)
						SYS-CPU core standby	A3SM	A3SP	A3SG	A4S	RT-CPU core standby	A3RV	A3RI	A4R	A4LC	A4MP	D4		
31	RT	2D-DMAC	√	√	√	—	—	—	—	—	—	—	—	√	—	—	—	√	√
32		ICB	√	√	√	—	—	—	—	—	—	—	—	√	—	—	—	√	√
33		MERAM	√	√	√	—	—	—	—	—	—	—	—	—	√	—	—	—	√
34		LCDC0	√	√	√	—	—	—	—	—	—	—	—	—	√	—	—	—	√
35		LCDC1	√	√	√	—	—	—	—	—	—	—	—	—	√	—	—	—	√
36		DSI-TX	√	√	√	—	—	—	—	—	—	—	—	—	√	—	—	—	√
37		JPU	√	√	√	—	—	—	—	—	—	—	—	√	—	—	—	√	√
38		ISP	√	√	√	—	—	—	—	—	—	—	√	√	—	—	—	√	√
39		TSIF0	√	√	√	—	—	—	—	—	—	—	—	√	—	—	—	√	√
40		TSIF1	√	√	√	—	—	—	—	—	—	—	—	√	—	—	—	√	√
41	SY	System CPU core	√	√	√	√	√	—	—	√	—	—	—	—	—	—	—	—	√
42		Coresight	√	√	—	—	—	—	—	—	—	—	—	—	—	—	√	—	—
43		HS-SHwy	√	√	√	—	—	—	—	√	—	—	—	—	—	—	—	—	—
44		SHWYSTAT(HS)	√	√	√	—	—	—	—	√	—	—	—	—	—	—	—	—	—
45		INTCA	√	√	√	—	—	—	—	√	—	—	—	—	—	—	—	—	√
46		IPMMUD	√	√	√	—	—	√	—	√	—	—	—	—	—	—	—	—	√
47		DMAC1	√	√	√	—	—	√	—	√	—	—	—	—	—	—	—	—	√
48		DMAC2	√	√	√	—	—	√	—	√	—	—	—	—	—	—	—	—	√
49		DMAC3	√	√	√	—	—	√	—	√	—	—	—	—	—	—	—	—	√
50		DDM	√	√	√	—	—	√	—	√	—	—	—	—	—	—	—	—	√
51		TPU	√	√	√	—	—	√	—	√	—	—	—	—	—	—	—	—	√
52		SCIFA0	√	√	√	—	—	√	—	√	—	—	—	—	—	—	—	—	√
53		SCIFA1	√	√	√	—	—	√	—	√	—	—	—	—	—	—	—	—	√
54		SCIFA2	√	√	√	—	—	√	—	√	—	—	—	—	—	—	—	—	√
55		SCIFA3	√	√	√	—	—	√	—	√	—	—	—	—	—	—	—	—	√
56		SCIFA4	√	√	√	—	—	√	—	√	—	—	—	—	—	—	—	—	√
57		SCIFA5	√	√	√	—	—	√	—	√	—	—	—	—	—	—	—	—	√
58		SCIFB	√	√	√	—	—	√	—	√	—	—	—	—	—	—	—	—	√
59		BBIF1	√	√	√	—	—	√	—	√	—	—	—	—	—	—	—	—	√
60		IIC1	√	√	√	—	—	√	—	√	—	—	—	—	—	—	—	—	√
61		IIC3	√	√	√	—	—	√	—	√	—	—	—	—	—	—	—	—	√
62		IIC4	√	√	√	—	—	√	—	√	—	—	—	—	—	—	—	—	√
63		FLCTL	√	√	√	—	—	√	—	√	—	—	—	—	—	—	—	—	√
64		MFIS	√	√	√	—	—	—	—	√	—	—	—	—	—	—	—	—	√
65		MFIM	√	√	√	—	—	—	—	√	—	—	—	—	—	—	—	—	√
66	SY	ACMFI1	√	√	√	—	—	—	—	√	—	—	—	—	—	—	—	—	√
67		ACMFI2	√	√	√	—	—	—	—	√	—	—	—	—	—	—	—	—	√

No	Domain	Module	Hard Power On Reset	Soft Power On Reset	Sytem reset	Power Area Reset												SH-X manual	Software reset (CPG)
						SYS-CPU core standby	A3SM	A3SP	A3SG	A4S	RT-CPU core standby	A3RV	A3RI	A4R	A4LC	A4MP	D4		
68		MMCIF	√	√	√	—	—	√	—	√	—	—	—	—	—	—	—	—	√
69		SDHI0	√	√	√	—	—	√	—	√	—	—	—	—	—	—	—	—	√
70		SDHI1	√	√	√	—	—	√	—	√	—	—	—	—	—	—	—	—	√
71		SDHI2	√	√	√	—	—	√	—	√	—	—	—	—	—	—	—	—	√
72		USBHS0	√	√	√	—	—	√	—	√	—	—	—	—	—	—	—	—	√
73		USBHS1	√	√	√	—	—	√	—	√	—	—	—	—	—	—	—	—	√
74		USB-DMAC0	√	√	√	—	—	√	—	√	—	—	—	—	—	—	—	—	√
75		USB-DMAC1	√	√	√	—	—	√	—	√	—	—	—	—	—	—	—	—	√
76		HDMI	√	√	√	—	—	√	—	√	—	—	—	—	—	—	—	—	√
77		CEC	√	√	√	—	—	√	—	√	—	—	—	—	—	—	—	—	√
78		Crypt	√	√	√	—	—	√	—	√	—	—	—	—	—	—	—	—	√
79		IrDA	√	√	√	—	—	√	—	√	—	—	—	—	—	—	—	—	√
81		HSI	√	√	√	—	—	√	—	√	—	—	—	—	—	—	—	—	√
82		MSU	√	√	√	—	—	√	—	√	—	—	—	—	—	—	—	—	√
84		SPU2	√	√	√	—	—	—	—	—	—	—	—	—	—	√	—	—	√
85		FSI	√	√	√	—	—	—	—	—	—	—	—	—	—	√	—	—	√
86		FMSI	√	√	√	—	—	—	—	—	—	—	—	—	—	√	—	—	√
87		BBIF2	√	√	√	—	—	—	—	—	—	—	—	—	—	√	—	—	√
88		SGX540	√	√	√	—	—	—	√	√	—	—	—	—	—	—	—	—	√
89		CM-SHwy	√	√	√	—	—	—	—	√	—	—	—	—	—	—	—	—	—
90		SHWYSTAT(CM)	√	√	√	—	—	—	—	√	—	—	—	—	—	—	—	—	—
91		BSC	√	√	√	—	—	—	—	√	—	—	—	—	—	—	—	—	√
92		SBSC	√	√	√	—	—	—	—	√	—	—	—	—	—	—	—	—	√
93	CM	CMT1	√	√	—	—	—	—	—	—	—	—	—	—	—	—	—	—	√
94		CMT1 (counter)	√	√	—	—	—	—	—	—	—	—	—	—	—	—	—	—	√
95		CMT2	√	√	—	—	—	—	—	—	—	—	—	—	—	—	—	—	√
96		CMT2 (counter)	√	√	—	—	—	—	—	—	—	—	—	—	—	—	—	—	√
97		CMT3	√	√	—	—	—	—	—	—	—	—	—	—	—	—	—	—	√
98		CMT3 (counter)	√	√	—	—	—	—	—	—	—	—	—	—	—	—	—	—	√
99		CMT4	√	√	—	—	—	—	—	—	—	—	—	—	—	—	—	—	√
100		CMT4 (counter)	√	√	—	—	—	—	—	—	—	—	—	—	—	—	—	—	√
101		RWDT	√	√	—	—	—	—	—	—	—	—	—	—	—	—	—	—	√
102		KEYSC	√	√	—	—	—	—	—	—	—	—	—	—	—	—	—	—	√
103		GPIO	√	√	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
104		PAD	√	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
105		Backup Registers	√	√	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
106		CPG	√	√	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

No	Domain	Module	Hard Power On Reset	Soft Power On Reset	Sytem reset	Power Area Reset												SH-X manual	Software reset (CPG)
						SYS-CPU core standby	A3SM	A3SP	A3SG	A4S	RT-CPU core standby	A3RV	A3RI	A4R	A4LC	A4MP	D4		
107		SYSC	√	√	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

1-D.1.3 Trigger of Reset

Table 1-D.2 shows the type of reset and its trigger.

Table 1-D.2 Reset type and trigger of reset

Reset Type	Trigger of reset
Hard Power-on reset	External pin (RESETP) input
Soft Power-on reset	Writing 1 to SYSC.RESCNT PRES bit One of the following events while SYSC.RESCNT.SRESLNK=1 - External pin (RESETA) input - Writing 1 to SYSC.RESCNT MRES bit - RWDT overflow (if it is enabled by register)
System reset	One of the following events while SYSC.RESCNT.SRESLNK=1 - External pin (RESETA) input - Writing 1 to SYSC.RESCNT MRES bit - RWDT overflow (if it is enabled by register)
Power supply area reset	Turning off of power supply area
Software reset	Writing to software reset register in CPG
Manual Reset	Exception event of RT-CPU core

Section 1-E Overview of Clock

Figure 1-E.1 is a diagram of clock in this LSI. The clock frequency internal this LSI is configurable by settings of Clock Pulse Generator (CPG) registers.

The clock pulse generator has three PLL: PLLC0, PLLC1 and PLLC2. Clock output of PLLC0, PLLC1 and PLLC2 are supplied to the divider circuits in the subsequent stage.

The PLLC0 generates a base clock for SYS-CPU core (Zϕ).

The PLLC1 generates a base clock for the common divider which generates system clocks (Iϕ, ZGϕ, Bϕ, M1ϕ, CSIRϕ, ZTRϕ, ZTϕ, HPϕ, ISPBϕ, ISPMϕ, ZSϕ, ZBϕ, ZB3ϕ, CPϕ, DLLϕ)

The PLLC2 generates a base clock for the dedicated dividers which are prepared as special clock sources for the auxiliary clocks (SUBϕ, SUB2ϕ, SPUϕ, FMSIϕ, FMSOϕ, FSIAϕ, FSIBϕ, DSITϕ, DSIP0ϕ, DSIP1ϕ, HDMIϕ, VOUϕ, VCK1ϕ VCK2ϕ, VCK3ϕ). The input of dedicated dividers is selectable such as 1/2 of the PLLC1 output, the PLLC2 output, etc.

The division ratios supported by the common divider are 1/2, 1/3, 1/4, 1/6, 1/8, 1/12, 1/16, 1/18, 1/24, 1/32, 1/36, 1/48, 1/72 and 1/96. The division ratios supported by the dedicated dividers are 1/1 to 1/64.

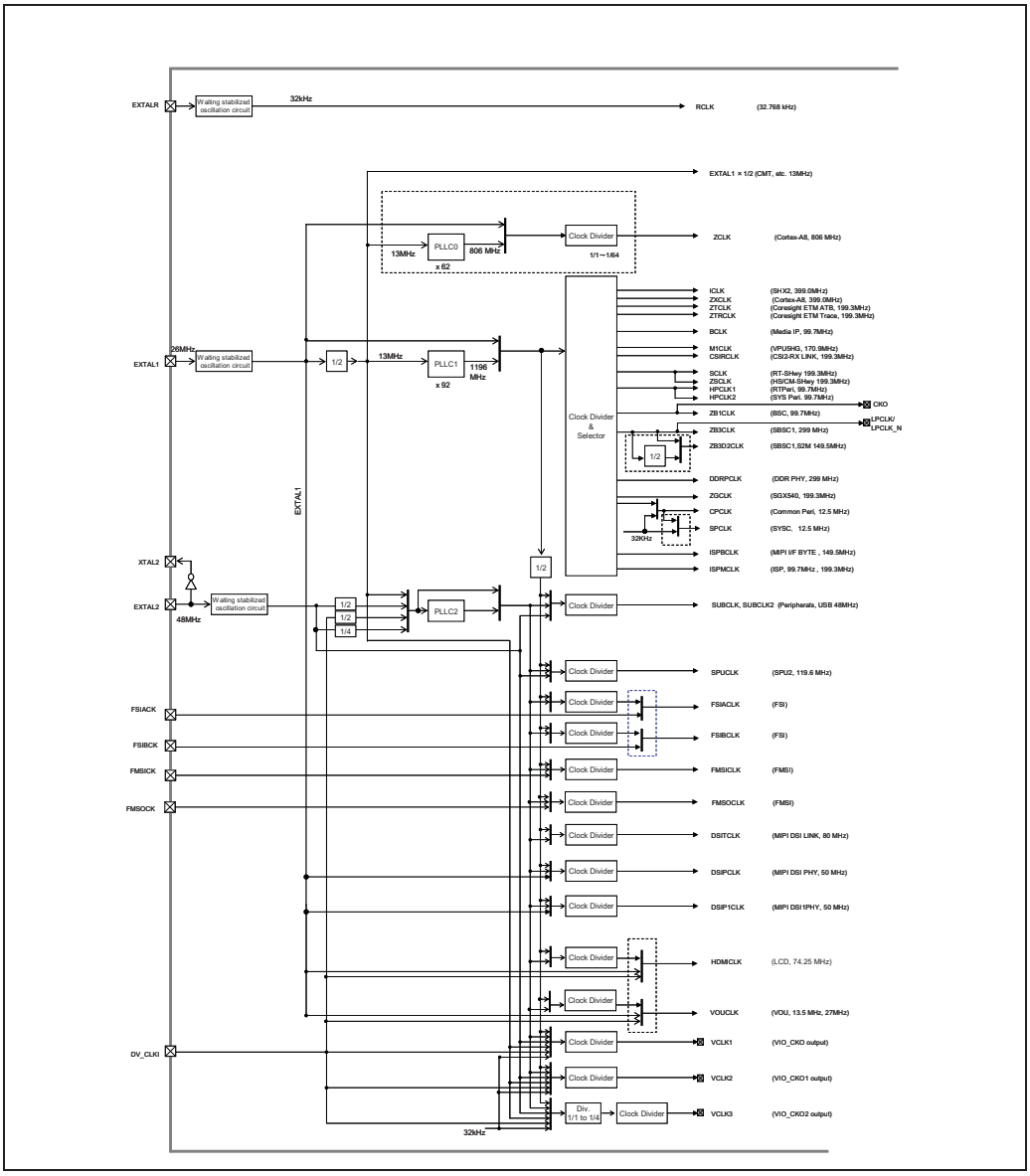


Figure 1-E.1 Clock Diagram

1-E.1 Clock Domain

Table 1-E.1 shows clock domain in this LSI.

Table 1-E.1 Clock Domain

Domain	Name	Source	Function
SYS	Zϕ	SYS-CPU divider	SYS-CPU core clock
RT	Iϕ	Common divider	RT-CPU core clock
SYS	ZXϕ	Common divider	SYS-CPU SHwy I/F clock
SYS	ZGϕ	Common divider	SGX540 clock
RT	Bϕ	Common divider	Multimedia module clock
RT	M1ϕ	Common divider	Video Processing Unit clock
RT/SYS	HPϕ	Common divider	High-speed peripheral clock
RT	CSIRϕ	Common divider	CSI2-RX Link module
RT	ISPBϕ	Common divider	Camera ISP byte clock
RT	ISPMϕ	Common divider	Camera ISP main clock
SYS	ZTRϕ	Common divider	Debug trace clock
SYS	ZTϕ	Common divider	ATB clock
RT/SYS/ COM	ZSϕ	Common divider	RT-SHwy, HS-SHwy, COM-SHwy
COM	ZBϕ	Common divider	BSC clock (External bus)
COM	ZB3ϕ	Common divider	SBSC clock
COM	DDRPϕ	Common divider	DDR PHY
COM	CPϕ	Common divider	Common domain peripheral clock
RT/SYS	SUBϕ	SUB clock divider	Sub clock, USB clock
SYS	SUB2ϕ	SUB clock divider	Sub clock (for A4MP domain)
SYS	SPUϕ	SPU clock divider	SPU2
SYS	FMSIϕ	FMSI clock divider	FMSI
SYS	FMSOϕ	FMSO clock divider	FMSI
SYS	FSIAϕ	FSIA clock divider	FSI
SYS	FSIBϕ	FSIB clock divider	FSI
RT	DSITϕ	DSIT clock divider	DSI-TX Link
RT	DSIPϕ	DSIP clock divider	DSI-TX PHY0
RT	DSIPϕ	DSIP clock divider	DSI-TX PHY1
SYS	HDMIϕ	HDMI clock divider	HDMI
RT	VOUϕ	VOU clock divider	VOU
RT/SYS/COM	-	-	EXTAL1 x 1/2
RT/SYS/COM	RCLK	EXTALR	RTC clock (32.768 kHz)

1-E.2 Clock Inputs

Table 1.E-2 shows the clock sources and their related pins.

Table 1.E-2 Clock Sources and Related Pins

Pin Name	Description
EXTALR	The RTC clock (32.768kHz) input. The RTC clock oscillation setup cycles are fixed at 64 RCLK cycles.
EXTAL1	The main clock (26 MHz) input.
XTAL1L	Enables the TCXO output. A high-current output buffer (16 mA) is used in consideration of the TCXO element power being driven directly. This pin becomes high-level output at a power-on.
EXTAL2	The sub clock (48 MHz, etc.) input.
XTAL2	Outputs amplified negative feedback of EXTAL2 for a crystal oscillating circuit. At a power-on reset, output of the oscillator is enabled. When a clock generated by an oscillator is input to the EXTAL2 pin, the XTAL2 pin should be open.

1-E.3 PLL Configuration

Table 1-E.3 shows the setting of each PLL.

Table 1-E.3 Setting of Each PLL

Domain	Reference Clock	Maximum Operating Frequency	Multiplication Ratio	Function
PLLC0	EXTAL1 × 1/2 (13 MHz when EXTAL1 = 26 MHz)	806 MHz	40 to 62 (valiable)	SYS-CPU core
PLLC1	EXTAL1 × 1/2 (13 MHz when EXTAL1 = 26 MHz)	1196 MHz	40 to 92 (variable)	RT-CPU core System bus
PLLC2	EXTAL1 × 1/2 EXTAL2 × 1/2 DV_CLKI × 1/2 EXTAL2 × 1/4	1040 MHz	40 to 80 (variable)	Sub clock system Peripheral modules

1-E.4 Oscillation Control

Clock oscillation can be halted when a clock input is unnecessary in a low power consumption mode. For EXTAL2/XTAL2 input clocks, clock oscillation circuit is turned-off by register. For EXTAL1, XTAL1L signal is asserted at specified condition, and halt external TCXO.

Each clock input is re-oscillated when clock input is required. At this time, the oscillation setup time is automatically counted by hardware, and clock supply restarts after oscillation setup time expired.

Figure 1-E.2 is a diagram of the oscillation control circuit.

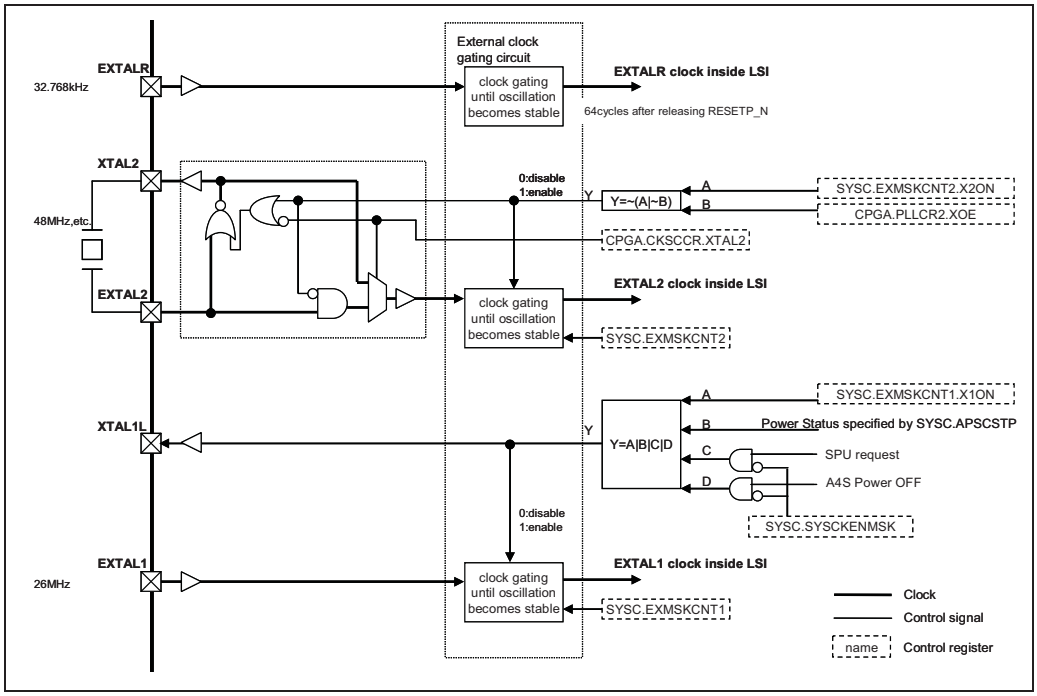


Figure 1-E.2 Oscillation Control Circuit

1-E.5 Limitations on Clock frequency ratio

Table 1-E.4 shows the limitations of clock frequency ratio.

Table 1-E.4 Limitations on Clock frequency ratio

Domain	Clock	Clock Limitation	Clock frequency Ratio	Remarks
RT	Iϕ:ZSϕ	Clock ratio of integers	Iϕ:Sϕ=N:1 (N=16,12,8,6,4,3,2,1)	
	Iϕ:HPϕ	Clock ratio of integers	Iϕ:HPϕ=N:1 (N=16,12,8,6,4,3,2,1)	
	ZSϕ:Bϕ	Clock ratio of integers	ZSϕ:Bϕ=N:1 (N=16,12,8,6,4,3,2,1)	ZSϕ:Bϕ=1:1is not available if CSI2-RX is operating.
System	ZXϕ:ZSϕ	Clock ratio of integers	ZXϕ:ZSϕ=N:1 (N=16,12,8,6,4,3,2,1)	
	ZSϕ:HPϕ	Clock ratio of integers	ZSϕ:HPϕ=N:1 (N=16,12,8,6,4,3,2,1)	
	ZSϕ:ZBϕ	Clock ratio of integers	ZSϕ:ZBϕ=N:1 (N=16,12,8,6,4,3,2,1)	
Other	HPϕ, TCK	Relation between frequency values	HPϕ>TCK	

Section 1-F Bus Functions

1-F.1 Bus Configuration

Bus and bridge connection diagrams

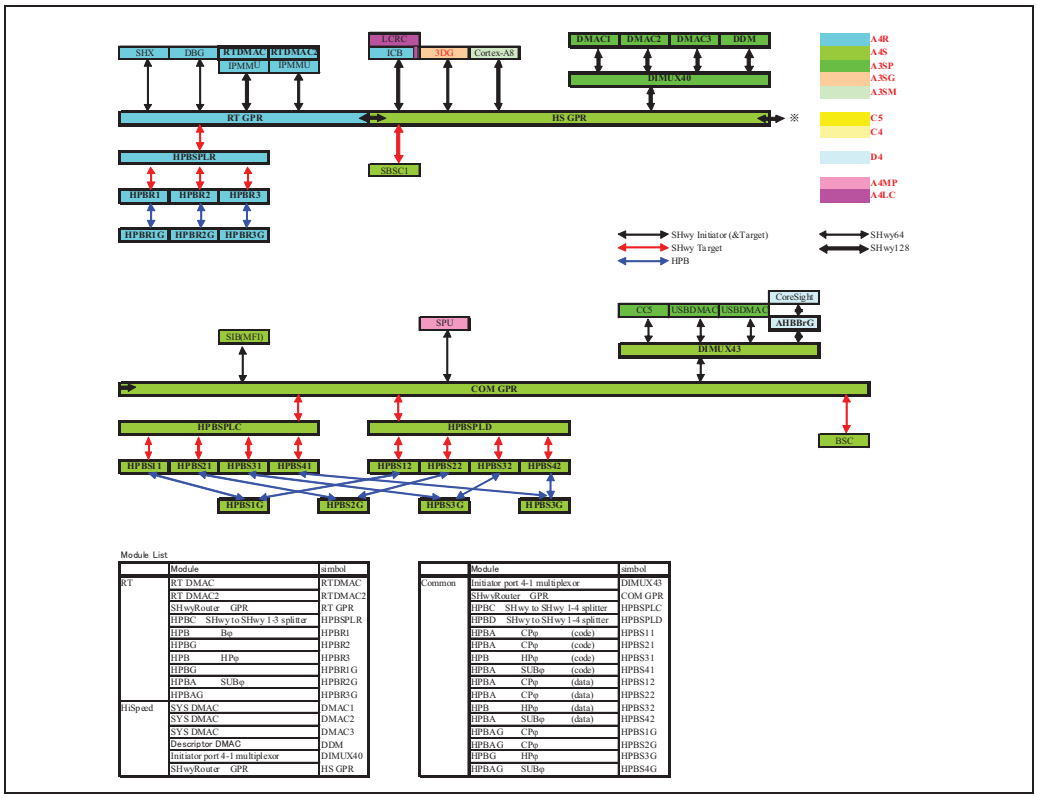


Fig 1-F-1SHwy Bus Connection Diagram

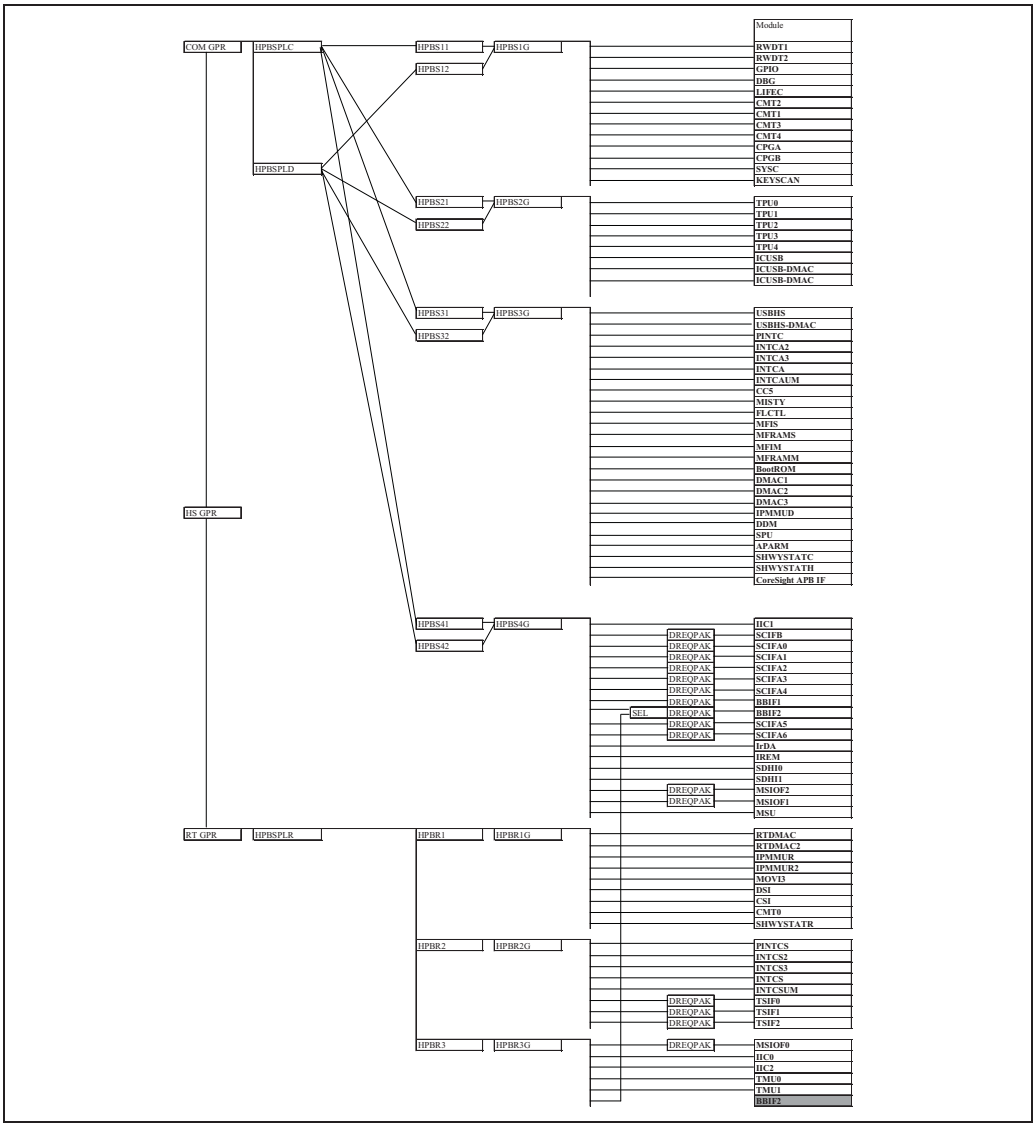


Fig 1-F -2HPB Bus Connection Diagram

Data bus widths and operating clocks of buses

The table below shows the data bus widths and operating clocks of the buses that appear in the above figure.

Bus		Data Bus Width	Operating Clock
1	Media Bus	32 bits, 64 bits	Bϕ (bck)
2	SHwy(RT/SYS/Common)	128bits,64 bits	ZSϕ (zsck)
3	HP Bus(RT)	8 bits, 16 bits, 32 bits	Bϕ (bck), HPϕ (hpck)
4	HP Bus(Common/System)	8 bits, 16 bits, 32 bits	CPϕ (cpck), HPϕ (hpck)
5	HP Bus (UART modules)	8 bits, 16 bits, 32 bits	SUBϕ (subck)

Bridges

The buses shown in Fig1-F-1. ”SHwy connection diagram” are mutually connected by the following bridges:

Bridge	Connected Data Bus (A)	Connected Data Bus (B)
Inter Connect Buffer (ICB)	1. Media Bus	2. SHwy (HS)
HPB Splitter(RT/Common)	3. SHwy (RT/Common)	3. SHwy (RT/Common)
SHwy-HPB Bridge (RT)	2. SHwy (RT)	4. HP Bus (RT)
SHwy-HPB Bridge (Common/System)	3. SHwy (Common)	5. HP Bus (Common/System)

Latencies that pass bridges are approximately as follows:

Bridge	Latency (Unit: Cycle)	Number of Pass Cycles When Clock Ratio Is 1:1
SHwy router	Both read and write: Request: 1 Response: 1	(Despite the access size): total 2 cycles
HPBC/D SHwy Target Bridge	Read: Request: Bus (A) 1 + bus (B) 1*[1] Response: Bus (B) 1 to bus (B) 4 + bus (A) 1*[1] Write: Request: Bus (A) 1 to bus (A) 4 + bus (B) 1*[1] Response: Bus (B) 1 + bus (A) 1*[1]	4-byte read (write): total 4 cycles 32-byte read (write): total 7 cycles
SHwy-HPB Bridge	Both read and write: Request: Bus (A) 1 + bus (B) 2 Response: Bus (B) 1 + bus (A) 1	(Despite the access size):total 5 cycles (The total number of cycles of the request depends on the HPB data bus width.)

Notes: 1. This depends on the data burst length.

When the CPU accesses main memory targets, the total latencies of the bridges and buses are as follows: In this case, the clock ratio is 1:1 and 32-byte burst transfer is used.

Bus Master	Memory Target	Number of Cycles
AP-System core	SDRAM(AP)	2
	MERAM	7
	XYRAM	7
	Asynchronous RAM, flash memory	2
	MFI RAM (Sys)	16
	MFI RAM (RT)	19
AP-Realtime core	SDRAM (AP)	2
	MERAM	2
	XYRAM	0
	Asynchronous RAM, flash memory	7
	MFI RAM (RT)	16
	MFI RAM (Sys)	19

Asynchronous RAM and flash memory connection

BSC and FLCTL modules access asynchronous RAM and flash memory. The BSC module arbitrates between asynchronous RAM and flash memory.

The arbitration method is as follows:

BSC < FLCTL: Fixed priority

1-F.2 SHwy Bus Functions

1-F.2.1 Arbitration Functions

The following two arbitration modes are supported for SBSC1 and MERAM of SHwy GPR(Global Packet Router) .

- Urgent Transfer arbitration
- Grant-Times-Based arbitration

Capture/Display IP requests are High-Priority by default, and always proceed to Grant-times-based arbitration.

Grant-Times-Based arbitration is used by the other normal priority IP, or the case that suppress high-priority request by setting PRI control register.

(1) Urgent Transfer Arbitration

A specific initiator (bus master) can request urgent transfer. Each initiator sets a Pri value. The request having the maximum Pri value precedes other requests. If the Pri value is urgent transfer (H'9 to H'F), the request having this values precedes the priority settings of the normal transfer arbitration result.

Initiator	Normal Transfer (H'0, H'8)*1	Urgent Transfer (H'9 to H'F)	Purpose of Urgent Transfer
AP-Realtime core	H'8	H'C	Interrupt (BL=1)
DBG	H'8	H'E	Debugging by debugger
RTDMAC	H'0	H'9 to H'F	Any values can be set in registers.
SYSDMAC, USBDMAC	H'0	H'9 to H'F	Any values can be set in registers.
ICB	H'0	H'1 to H'F	Insufficient remaining quantity of image IP buffer
AP-SYSTEM core	H'0	H'9 to H'F	Any values can be set in registers.

Note: *1 In the SHwy standard, only H'8 indicates "normal transfer." H'0 to H'7 indicate "low priority transfer." This chip treats also H'0 as normal transfer because it is not equipped with the low priority transfer function.

The table below shows the registers that control Pri values.

Initiator	Register	Address	Bit
RTDMAC	RDM1CHCRB_0	H'FFC1 812C	3-0
	RDM1CHCRB_1	H'FFC1 813C	3-0
	RDM1CHCRB_2	H'FFC1 814C	3-0
	RDM1CHCRB_3	H'FFC1 815C	3-0

	RDM1CHCRB_4	H'FFC1 817C	3-0
	RDM1CHCRB_5	H'FFC1 818C	3-0
RTDMAC2	RDM2CHCRB_0	H'FFC2 812C	3-0
	RDM2CHCRB_1	H'FFC2 813C	3-0
	RDM2CHCRB_2	H'FFC2 814C	3-0
	RDM2CHCRB_3	H'FFC2 815C	3-0
	RDM2CHCRB_4	H'FFC2 817C	3-0
	RDM2CHCRB_5	H'FFC2 818C	3-0
SYSDMAC	DM1CHCRB_0	H'FE00 812C	3-0
	DM1CHCRB_1	H'FE00 813C	3-0
	DM1CHCRB_2	H'FE00 814C	3-0
	DM1CHCRB_3	H'FE00 815C	3-0
	DM1CHCRB_4	H'FE00 817C	3-0
	DM1CHCRB_5	H'FE00 818C	3-0
	DM2CHCRB_0	H'FE01 812C	3-0
	DM2CHCRB_1	H'FE01 813C	3-0
	DM2CHCRB_2	H'FE01 814C	3-0
	DM2CHCRB_3	H'FE01 815C	3-0
	DM2CHCRB_4	H'FE01 817C	3-0
	DM2CHCRB_5	H'FE01 818C	3-0
	DM3CHCRB_0	H FE02 812C	3-0
	DM3CHCRB_1	H'FE02 813C	3-0
	DM3CHCRB_2	H'FE02 814C	3-0
	DM3CHCRB_3	H'FE02 815C	3-0
	DM3CHCRB_4	H'FE02 817C	3-0
	DM3CHCRB_5	H'FE02 818C	3-0
USBDMAC	USBDMACHCR_0	H'E68A 0034	11-8
	USBDMACHCR_1	H'E68A 0054	11-8
AP-SYSTEM core	APARMPRI	H'E6F1 0000	3-0

Any values can be set in the above registers. If you want to use urgent transfer, however, set a value from 9 to 15. Operations are not supported that correspond to 1 to 8.

(2) Grant-Times-based arbitration

SHwy router has parameters per initiator, “*acnum* : the number of requests that grants continuously” and ”*wnum* : the number of request-waiting cycle ” by register.

SHwy router has the following counters,

account : the rest of accepting numbers that current initiator’s request

wcount : the rest of waiting cycles that current initiator’s request

SHwy router arbitration acts by these two counters, and adjusts bus occupation by the register.

When *account* is zero and *wcount* is zero, SHwy router switches accepting initiator by round-robin order.

The adjustment of “Grant-Times-based arbitration” is available by setting the register XXPRARCR. The figure below shows an example of setting the SHwy register and the operation of the register.

AI=ICB acnum AS=3DG acnum ADI=SYSCPU acnum ADB=DMAC acnum
WI=ICB wnum WS=3DG wnum WDI=SYSCPU wnum WDB=DMAC wnum

case #1
AI=0 AS=0 ADI=0 ADB=0
WI=0 WS=0 WDI=0 WDB=0
Same as normal round-robin

ICB	req	(1)	1	1	1	(1)	1	1	(1)	1	1
3DG	req	1	(1)					1	1	(1)	
SYSCPU	req	1	1	(1)	1	1	(1)	1	1	1	(1)
DMAC	req	1	1	1	(1)	1	1	(1)	1	1	1
	acount	0	0	0	0	0	0	0	0	0	0
	wcount	0	0	0	0	0	0	0	0	0	0

case #2
AI=3 AS=0 ADI=0 ADB=0
WI=0 WS=0 WDI=0 WDB=0
ICB:3DG:SYSCPU:DMAC = 4:1:1:1

ICB	req	(1)	(1)	(1)	(1)	1	1	1	(1)	(1)	(1)
3DG	req	1	1	1	1	(1)					1
SYSCPU	req	1	1	1	1	1	(1)	1	1	1	1
DMAC	req	1	1	1	1	1	1	(1)	1	1	1
	acount	3	2	1	0	0	0	0	3	2	1
	wcount	0	0	0	0	0	0	0	0	0	0

case #3
AI=2 AS=1 ADI=0 ADB=0
WI=0 WS=2 WDI=0 WDB=0
ICB:3DG:SYSCPU:DMAC = 3:2:1:1
Waits 3DG requests until 3 cycles if 3DG request is not asserted.

ICB	req	(1)	(1)	(1)										
3DG	req	1	1	1	(1)			(1)	1	(1)				1
SYSCPU	req	1	1	1	1	1	1	1	(1)	1	1	1	1	(1)
DMAC	req													
	acount	2	1	0	1	0	0	0	0	1	0	0	0	0
	wcount	0	0	0	0	2	1	0	0	0	2	1	0	0

Example of Setting HS-SHwy Register of Grant-Times-based arbitration

1-F.2.2 Arbitration Registers (RealTime GPR)

Name	Register Abbreviation	R/W	Initial Value	Address	Access Size (Bits)
PRI control register	RTPRPRICR	R/W	H'0000 001E	H'FF800018	32
HS-GPR arbitration register 1	RTPRARCR11	R/W	H'0000 0000	H'FF800030	32
HS-GPR arbitration register 2	RTPRARCR12	R/W	H'0000 0000	H'FF800038	32
Error contorol register	RTPRERRMSK	R/W	H'0000 0000	H'FF800090	32

Register States in Each Operating Mode

Register Abbreviation	Power-on Reset	AP Reset	SYS-CPU Sleep	RT-CPU Sleep
RTPRPRICR	Initialized	Initialized	Retained	Retained
RTPRARCR11	Initialized	Initialized	Retained	Retained
RTPRARCR12	Initialized	Initialized	Retained	Retained
RTPRERRMSK	Initialized	Initialized	Retained	Retained

The above registers are allocated to the A4R power supply area. Turning off the power supply in this area initializes the settings.

PRI Control Register (RTPRPRICR)

RTPRPRICR sets Pri value control. This register enable priority checking when there is a request comes along with priority.

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
init-val	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	HSPR	RDM2	RDMPR	DBPR	SHPR
init-val	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bits 0: RT-CPU Pri control

0:SHwy router ignores Pri value.

1: SHwy router checks Pri value.

Bits 1: Debug Pri control

0:SHwy router ignores Pri value.

1: SHwy router checks Pri value.

Bits 2: RT-DMAC Pri control

0:SHwy router ignores Pri value.

1: SHwy router checks Pri value.

Bits 3: RT-DMAC2 Pri control

0:SHwy router ignores Pri value.

1: SHwy router checks Pri value.

Bits 4: HS-GPR Pri control

0:SHwy router ignores Pri value.

1: SHwy router checks Pri value.

Bits 31 to 5: Reserved

These bits are always read as 0. The write value should always be 0.

HS-GPR Arbitration Control Register 1 (RTPRARCR11)

RTPRARCR11 sets arbitration control parameters.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	WDB[5:0]						ADB[9:0]									
init-val :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WSH[5:0]						ASH[9:0]									
init-val :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 9 to 0: acnum (RT-CPU)

Set the number of requests that accepted continuously when arbitration mode is Grant-Times-based arbitration.

Bits 15 to 10: wnum (RT-CPU)

Set the number of request-waiting cycle when arbitration mode is Grant-Times-based arbitration.

Bits 25 to 16: acnum (Debug)

Set the number of requests that accepted continuously when arbitration mode is Grant-Times-based arbitration.

Bits 31 to 26: wnum (Debug)

Set the number of request-waiting cycle when arbitration mode is Grant-Times-based arbitration.

HS-GPR Arbitration Control Register 2 (RTPRARCR12)

RTPRARCR12 sets arbitration control parameters.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	WRDM2[5:0]						ARDM2[9:0]									
init-val :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WRDM[5:0]						ARDM[9:0]									
init-val :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 9 to 0: acnum (RT-DMAC)

Set the number of requests that accepted continuously when arbitration mode is Grant-Times-based arbitration.

Bits 15 to 10: wnum (RT-DMAC)

Set the number of request-waiting cycle when arbitration mode is Grant-Times-based arbitration.

Bits 25 to 16: acnum (RT-DMAC2)

Set the number of requests that accepted continuously when arbitration mode is Grant-Times-based arbitration.

Bits 31 to 26: wnum (RT-DMAC2)

Set the number of request-waiting cycle when arbitration mode is Grant-Times-based arbitration.

Error Control Register (RTPRERRMSK)

RTPRERRMSK sets error response control parameters.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
init-val :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	ERRMSK[1:0]	
init-val :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	0	R/W	R/W

Bit 0: Error mask

0: normal operation

1:Suppress error response when initiator accesses reserved address.

(Caution) If error response is masked, initiator cannot notice these errors. It causes system freeze. Do not set this register as usual.

Bits 1: Error mask

0: normal operation

1:Suppress error response when target ports response are error response.

(Caution) If error response is masked, initiator cannot notice these errors. It causes system freeze. Do not set this register as usual.

Bits 31 and 2: Reserved

These bits are always read as 0. The write value should always be 0.

1-F.2.3 Arbitration Registers (HS GPR)

Name	Register Abbreviation	R/W	Initial Value	Address	Access Size (Bits)
PRI control register	HSPRPRICR	R/W	H'0000 0000	H'FFA00018	32
SBSC1 arbitration register 1	HSPRARCR11	R/W	H'0000 0000	H'FFA00030	32
SBSC1 arbitration register 2	HSPRARCR12	R/W	H'0000 0000	H'FFA00038	32
SBSC1 arbitration register 3	HSPRARCR13	R/W	H'0000 0000	H'FFA00040	32
ICB arbitration register 1	HSPRARCR21	R/W	H'0000 0000	H'FFA00050	32
ICB arbitration register 2	HSPRARCR22	R/W	H'0000 0000	H'FFA00058	32
ICB arbitration register 3	HSPRARCR23	R/W	H'0000 0000	H'FFA00060	32
COM-GPR arbitration register 1	HSPRARCR31	R/W	H'0000 0000	H'FFA00070	32
COM-GPR arbitration register 2	HSPRARCR32	R/W	H'0000 0000	H'FFA00078	32
COM-GPR arbitration register 3	HSPRARCR33	R/W	H'0000 0000	H'FFA00080	32
Error control register	HSPRERRMSK	R/W	H'0000 0000	H'FFA00090	32
SBSC1 priority setting register 1	HSPRPRICNT11	R/W	H'4040 4040	H'FFA000A0	32
SBSC1 priority setting register 2	HSPRPRICNT12	R/W	H'0000 4040	H'FFA000A8	32
SBSC1 priority setting register 3	HSPRPRICNT13	R/W	H'0000 0000	H'FFA000B0	32

Register States in Each Operating Mode

Register Abbreviation	Power-on Reset	AP Reset	SYS-CPU Sleep	RT-CPU Sleep
HSPRPRICR	Initialized	Retained	Retained	Retained
HSPRARCR11	Initialized	Retained	Retained	Retained
HSPRARCR12	Initialized	Retained	Retained	Retained
HSPRARCR13	Initialized	Retained	Retained	Retained
HSPRARCR21	Initialized	Retained	Retained	Retained
HSPRARCR22	Initialized	Retained	Retained	Retained
HSPRARCR23	Initialized	Retained	Retained	Retained
HSPRARCR31	Initialized	Retained	Retained	Retained
HSPRARCR32	Initialized	Retained	Retained	Retained
HSPRARCR33	Initialized	Retained	Retained	Retained
HSPRERRMSK	Initialized	Retained	Retained	Retained
HSPRPRICNT11	Initialized	Retained	Retained	Retained
HSPRPRICNT12	Initialized	Retained	Retained	Retained
HSPRPRICNT13	Initialized	Retained	Retained	Retained

The above registers are allocated to the A4S power supply area. Turning off the power supply in this area initializes the settings.

PRI Control Register 1 (HSPRPRICR)

HSPRPRICR sets Pri value control. This register enable priority checking when there is a request comes along with priority.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
init-val :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	CMPR	DMPR	AMPR	ICPR	G3PR	RTPR
init-val :	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
R/W :	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bits 0: RT-GPR Pri control

0:SHwy router ignores Pri value.

1: SHwy router checks Pri value.

Bits 1: 3DG Pri control

0:SHwy router ignores Pri value.

1: SHwy router checks Pri value.

Bits 2: ICB Pri control

0:SHwy router ignores Pri value.

1: SHwy router checks Pri value.

Bits 3: SYS-CPU Pri control

0:SHwy router ignores Pri value.

1: SHwy router checks Pri value.

Bits 4: SYS-DMAC Pri control

0:SHwy router ignores Pri value.

1: SHwy router checks Pri value.

Bits 5: Com-GPR Pri control

0:SHwy router ignores Pri value.

1: SHwy router checks Pri value.

Bits 31 to 6: Reserved

These bits are always read as 0. The write value should always be 0.

SBSC1 Arbitration Control Register 1 (HSPRARCR11)

HSPRARCR11 sets arbitration control parameters.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	WG3[5:0]						AG3[9:0]									
init-val :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WRT[5:0]						ART[9:0]									
init-val :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 9 to 0: acnum (RT-GPR)

Set the number of requests that accepted continuously when arbitration mode is Grant-Times-based arbitration.

Bits 15 to 10: wnum (RT-GPR)

Set the number of request-waiting cycle when arbitration mode is Grant-Times-based arbitration.

Bits 25 to 16: acnum (3DG)

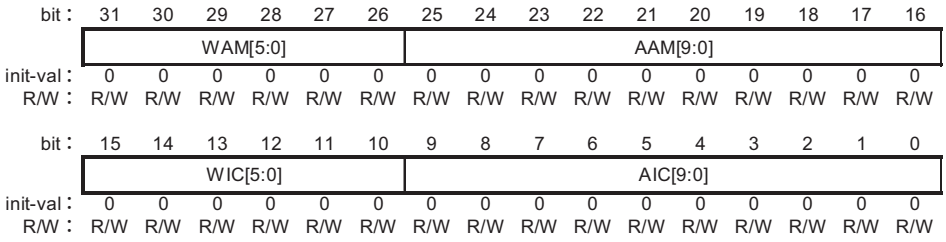
Set the number of requests that accepted continuously when arbitration mode is Grant-Times-based arbitration.

Bits 31 to 26: wnum (3DG)

Set the number of request-waiting cycle when arbitration mode is Grant-Times-based arbitration.

SBSC1 Arbitration Control Register 2 (HSPRARCR12)

HSPRARCR12 sets arbitration control parameters.



Bits 9 to 0: acnum (ICB)

Set the number of requests that accepted continuously when arbitration mode is Grant-Times-based arbitration.

Bits 15 to 10: wnum (ICB)

Set the number of request-waiting cycle when arbitration mode is Grant-Times-based arbitration.

Bits 25 to 16: acnum (SYS-CPU)

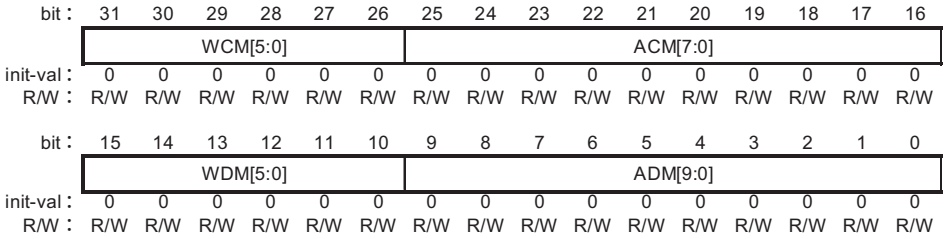
Set the number of requests that accepted continuously when arbitration mode is Grant-Times-based arbitration.

Bits 31 to 26: wnum (SYS-CPU)

Set the number of request-waiting cycle when arbitration mode is Grant-Times-based arbitration.

SBSC1 Arbitration Control Register 3 (HSPRARCR13)

HSPRARCR13 sets arbitration control parameters.



Bits 9 to 0: acnum (SYS-DMAC)

Set the number of requests that accepted continuously when arbitration mode is Grant-Times-based arbitration.

Bits 15 to 10: wnum (SYS-DMAC)

Set the number of request-waiting cycle when arbitration mode is Grant-Times-based arbitration.

Bits 25 to 16: acnum (Com-GPR)

Set the number of requests that accepted continuously when arbitration mode is Grant-Times-based arbitration.

Bits 31 to 26: wnum (Com-GPR)

Set the number of request-waiting cycle when arbitration mode is Grant-Times-based arbitration.

ICB Arbitration Control Register 1 (HSPRARCR21)

HSPRARCR21 sets arbitration control parameters.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	WG3[5:0]						AG3[9:0]									
init-val :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WRT[5:0]						ART[9:0]									
init-val :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 9 to 0: acnum (RT-GPR)

Set the number of requests that accepted continuously when arbitration mode is Grant-Times-based arbitration.

Bits 15 to 10: wnum (RT-GPR)

Set the number of request-waiting cycle when arbitration mode is Grant-Times-based arbitration.

Bits 25 to 16: acnum (3DG)

Set the number of requests that accepted continuously when arbitration mode is Grant-Times-based arbitration.

Bits 31 to 26: wnum (3DG)

Set the number of request-waiting cycle when arbitration mode is Grant-Times-based arbitration.

ICB Arbitration Control Register 2 (HSPRARCR22)

HSPRARCR22 sets arbitration control parameters.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	WAM[5:0]						AAM[9:0]									
init-val :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WIC[5:0]						AIC[9:0]									
init-val :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 9 to 0: acnum (ICB)

Set the number of requests that accepted continuously when arbitration mode is Grant-Times-based arbitration.

Bits 15 to 10: wnum (ICB)

Set the number of request-waiting cycle when arbitration mode is Grant-Times-based arbitration.

Bits 25 to 16: acnum (SYS-CPU)

Set the number of requests that accepted continuously when arbitration mode is Grant-Times-based arbitration.

Bits 31 to 26: wnum (SYS-CPU)

Set the number of request-waiting cycle when arbitration mode is Grant-Times-based arbitration.

ICB Arbitration Control Register 3 (HSPRARCR23)

HSPRARCR23 sets arbitration control parameters.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	WCM[5:0]						ACM[7:0]									
init-val :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WDM[5:0]						ADM[9:0]									
init-val :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 9 to 0: acnum (SYS-DMAC)

Set the number of requests that accepted continuously when arbitration mode is Grant-Times-based arbitration.

Bits 15 to 10: wnum (SYS-DMAC)

Set the number of request-waiting cycle when arbitration mode is Grant-Times-based arbitration.

Bits 25 to 16: acnum (Com-GPR)

Set the number of requests that accepted continuously when arbitration mode is Grant-Times-based arbitration.

Bits 31 to 26: wnum (Com-GPR)

Set the number of request-waiting cycle when arbitration mode is Grant-Times-based arbitration.

Com-GPR Arbitration Control Register 1 (HSPRARCR31)

HSPRARCR31 sets arbitration control parameters.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	WG3[5:0]						AG3[9:0]									
init-val :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WRT[5:0]						ART[9:0]									
init-val :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 9 to 0: acnum (RT-GPR)

Set the number of requests that accepted continuously when arbitration mode is Grant-Times-based arbitration.

Bits 15 to 10: wnum (RT-GPR)

Set the number of request-waiting cycle when arbitration mode is Grant-Times-based arbitration.

Bits 25 to 16: acnum (3DG)

Set the number of requests that accepted continuously when arbitration mode is Grant-Times-based arbitration.

Bits 31 to 26: wnum (3DG)

Set the number of request-waiting cycle when arbitration mode is Grant-Times-based arbitration.

Com-GPR Arbitration Control Register 2 (HSPRARCR32)

HSPRARCR32 sets arbitration control parameters.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	WAM[5:0]						AAM[9:0]									
init-val :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WIC[5:0]						AIC[9:0]									
init-val :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 9 to 0: acnum (ICB)

Set the number of requests that accepted continuously when arbitration mode is Grant-Times-based arbitration.

Bits 15 to 10: wnum (ICB)

Set the number of request-waiting cycle when arbitration mode is Grant-Times-based arbitration.

Bits 25 to 16: acnum (SYS-CPU)

Set the number of requests that accepted continuously when arbitration mode is Grant-Times-based arbitration.

Bits 31 to 26: wnum (SYS-CPU)

Set the number of request-waiting cycle when arbitration mode is Grant-Times-based arbitration.

Com-GPR Arbitration Control Register 3 (HSPRARCR33)

HSPRARCR33 sets arbitration control parameters.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	WCM[5:0]						ACM[7:0]									
init-val :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WDM[5:0]						ADM[9:0]									
init-val :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 9 to 0: acnum (SYS-DMAC)

Set the number of requests that accepted continuously when arbitration mode is Grant-Times-based arbitration.

Bits 15 to 10: wnum (SYS-DMAC)

Set the number of request-waiting cycle when arbitration mode is Grant-Times-based arbitration.

Bits 25 to 16: acnum (Com-GPR)

Set the number of requests that accepted continuously when arbitration mode is Grant-Times-based arbitration.

Bits 31 to 26: wnum (Com-GPR)

Set the number of request-waiting cycle when arbitration mode is Grant-Times-based arbitration.

Error Control Register (HSPRERRMSK)

HSPRERRMSK sets error response control parameters.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
init-val :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	ERRMSK[1:0]	
init-val :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	0	R/W	R/W

Bit 0: Error mask

0: normal operation

1:Suppress error response when initiator accesses reserved address.

(Caution) If error response is masked, initiator cannot notice these errors. It causes system freeze. Do not set this register as usual.

Bits 1: Error mask

0: normal operation

1:Suppress error response when target ports response are error response.

(Caution) If error response is masked, initiator cannot notice these errors. It causes system freeze. Do not set this register as usual.

Bits 31 and 2: Reserved

These bits are always read as 0. The write value should always be 0.

SBSC1 Priority Setting Register 1 (HSPRPRICNT11)

HSPRPRICNT11 sets control parameters of urgent transfer to SBSC1.

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PCNT_AB[7:0]								PCNT_ICB[7:0]							
init-val	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PCNT_G3[7:0]								PCNT_RT[7:0]							
init-val	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 to 0: number of times of urgent transfer requests which is granted continuously (RT-GPR)

Bits 15 to 8: number of times of urgent transfer requests which is granted continuously (3DG)

Bits 23 to 16: number of times of urgent transfer requests which is granted continuously (ICB)

Bits 31 to 24: number of times of urgent transfer requests which is granted continuously (SYS-CPU)

SBSC1 Priority Setting Register 2 (HSPRPRICNT12)

HSPRPRICNT12 sets control parameters of urgent transfer to SBSC1.

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
init-val	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PCNT_CM[7:0]								PCNT_DM[7:0]							
init-val	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 to 0: number of times of urgent transfer requests which is granted continuously (SYS-DMAC)

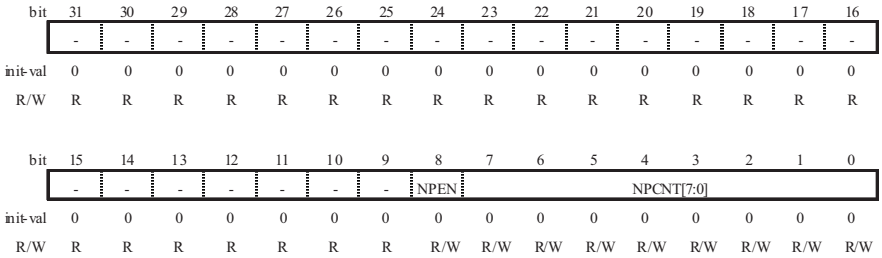
Bits 15 to 8: number of times of urgent transfer requests which is granted continuously (Com-GPR)

Bits 31 to 16: Reserved

SBSC1 Priority Setting Register 3 (HSPRPRICNT13)

HSPRPRICNT13 sets control parameters of urgent transfer to SBSC1.

If this register is set, SHwy router temporally cancels Pri value specified cycles before when the times of urgent transfer to SBSC1 reach the PCNT** register value, and switching to the next urgent transfer.



Bits 7 to 0: ZS cycles of urgent transfer requests canceled when NPEN=1.

Bits 8: enables cancelling cycles of urgent transfer

0 : disable

1: enable

Bits 31 to 9: Reserved

1-F.2.4 Arbitration Registers (Com GPR)

Name	Register Abbreviation	R/W	Initial Value	Address	Access Size (Bits)
PRI control register	CMPRPRICR	R/W	H'0000 01FF	H'FF700018	32
SBSC1 arbitration register 1	CMPRARCR11	R/W	H'0000 0000	H'FF700030	32
SBSC1 arbitration register 2	CMPRARCR12	R/W	H'0000 0000	H'FF700038	32
SBSC1 arbitration register 3	CMPRARCR13	R/W	H'0000 0000	H'FF700040	32
SBSC1 arbitration register 4	CMPRARCR14	R/W	H'0000 0000	H'FF700048	32
SBSC1 arbitration register 5	CMPRARCR15	R/W	H'0000 0000	H'FF700050	32
HS-GPR arbitration register 1	CMPRARCR21	R/W	H'0000 0000	H'FF700060	32
HS-GPR arbitration register 2	CMPRARCR22	R/W	H'0000 0000	H'FF700068	32
HS-GPR arbitration register 3	CMPRARCR23	R/W	H'0000 0000	H'FF700070	32
HS-GPR arbitration register 4	CMPRARCR24	R/W	H'0000 0000	H'FF700078	32
HS-GPR arbitration register 5	CMPRARCR25	R/W	H'0000 0000	H'FF700080	32
Error control register	CMPRERRMSK	R/W	H'0000 0000	H'FF700090	32
SBSC1 priority setting register 1	CMPRPRICNT11	R/W	H'4040 4040	H'FF7000A0	32
SBSC1 priority setting register 2	CMPRPRICNT12	R/W	H'4040 4040	H'FF7000A8	32
SBSC1 priority setting register 3	CMPRPRICNT13	R/W	H'0000 0040	H'FF7000B0	32
SBSC1 priority setting register 3	CMPRPRICNT14	R/W	H'0000 0000	H'FF7000B8	32

Register States in Each Operating Mode

Register Abbreviation	Power-on Reset	AP Reset	SYS-CPU Sleep	RT-CPU Sleep
CMPRPRICR	Initialized	Retained	Retained	Retained
CMPRARCR11	Initialized	Retained	Retained	Retained
CMPRARCR12	Initialized	Retained	Retained	Retained
CMPRARCR13	Initialized	Retained	Retained	Retained
CMPRARCR14	Initialized	Retained	Retained	Retained
CMPRARCR15	Initialized	Retained	Retained	Retained
CMPRARCR21	Initialized	Retained	Retained	Retained
CMPRARCR22	Initialized	Retained	Retained	Retained
CMPRARCR23	Initialized	Retained	Retained	Retained
CMPRARCR24	Initialized	Retained	Retained	Retained
CMPRARCR25	Initialized	Retained	Retained	Retained
CMPRERRMSK	Initialized	Retained	Retained	Retained
CMPRPRICNT11	Initialized	Retained	Retained	Retained
CMPRPRICNT12	Initialized	Retained	Retained	Retained
CMPRPRICNT13	Initialized	Retained	Retained	Retained
CMPRPRICNT14	Initialized	Retained	Retained	Retained

The above registers are allocated to the A4S power supply area. Turning off the power supply in this area initializes the settings.

PRI Control Register 1 (CMPRPRICR)

CMPRPRICR sets Pri value control. This register enable priority checking when there is a request comes along with priority.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
init-val :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	HSPR	HSPR0
init-val :	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bits 0: HS-GPR0 Pri control

0:SHwy router ignores Pri value.

1: SHwy router checks Pri value.

Bits 1: HS-GPR1 Pri control

0:SHwy router ignores Pri value.

1: SHwy router checks Pri value.

Bits 8 to 2: Reserved

No function is assigned. The write value should always be initial value.

Bits 31 to 9: Reserved

These bits are always read as 0. The write value should always be 0.

SBSC2 Arbitration Control Register 1 (CMPRARCR11)

CMPRARCR11 sets arbitration control parameters.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	WHS1[5:0]						AHS1[9:0]									
init-val :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WHS0[5:0]						AHS0[9:0]									
init-val :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 9 to 0: acnum (HS-GPR0)

Set the number of requests that accepted continuously when arbitration mode is Grant-Times-based arbitration.

Bits 15 to 10: wnum (HS-GPR0)

Set the number of request-waiting cycle when arbitration mode is Grant-Times-based arbitration.

Bits 25 to 16: acnum (HS-GPR1)

Set the number of requests that accepted continuously when arbitration mode is Grant-Times-based arbitration.

Bits 31 to 26: wnum (HS-GPR1)

Set the number of request-waiting cycle when arbitration mode is Grant-Times-based arbitration.

SBSC2 Arbitration Control Register 2 (CMPRARCR12)

CMPRARCR12 sets arbitration control parameters.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
init-val :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
init-val :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits 31 to 0: Reserved

These bits are always read as 0. The write value should always be 0.

SBSC2 Arbitration Control Register 3 (CMPRARCR13)

CMPRARCR13 sets arbitration control parameters.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
init-val :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WDMX[5:0]						ADMX[9:0]									
init-val :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 9 to 0: acnum (CC5/USBDMAC/Coresight)

Set the number of requests that accepted continuously when arbitration mode is Grant-Times-based arbitration.

Bits 15 to 10: wnum (CC5/USBDMAC/Coresight)

Set the number of request-waiting cycle when arbitration mode is Grant-Times-based arbitration.

Bits 31 to 16: Reserved

These bits are always read as 0. The write value should always be 0.

SBSC2 Arbitration Control Register 4 (CMPRARCR14)

CMPRARCR14 sets arbitration control parameters.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
init-val :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WSP[5:0]						ASP[9:0]									
init-val :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 9 to 0: acnum (SPU)

Set the number of requests that accepted continuously when arbitration mode is Grant-Times-based arbitration.

Bits 15 to 10: wnum (SPU)

Set the number of request-waiting cycle when arbitration mode is Grant-Times-based arbitration.

Bits 31 to 16: Reserved

These bits are always read as 0. The write value should always be 0.

SBSC2 Arbitration Control Register 5 (CMPRARCR15)

CMPRARCR15 sets arbitration control parameters.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
init-val :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
init-val :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits 31 to 0: Reserved

These bits are always read as 0. The write value should always be 0.

HS-GPR Arbitration Control Register 1 (CMPRARCR21)

CMPRARCR21 sets arbitration control parameters.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
init-val :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
init-val :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits 31 to 0: Reserved

These bits are always read as 0. The write value should always be 0.

HS-GPR Arbitration Control Register 2 (CMPRARCR22)

CMPRARCR22 sets arbitration control parameters.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
init-val :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

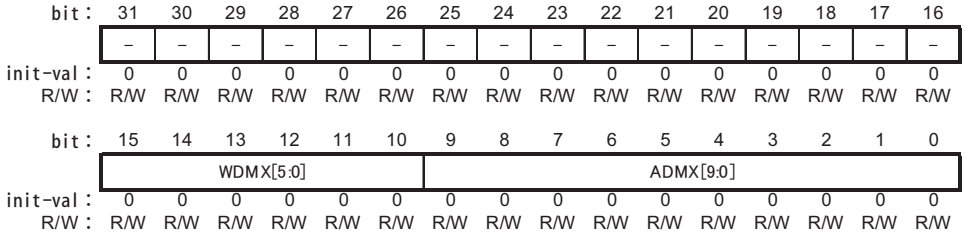
bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
init-val :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits 31 to 0: Reserved

These bits are always read as 0. The write value should always be 0.

HS-GPR Arbitration Control Register 3 (CMPRARCR23)

CMPRARCR23 sets arbitration control parameters.



Bits 9 to 0: acnum (CC5/USBDMAC/Coresight)

Set the number of requests that accepted continuously when arbitration mode is Grant-Times-based arbitration.

Bits 15 to 10: wnum (CC5/USBDMAC/Coresight)

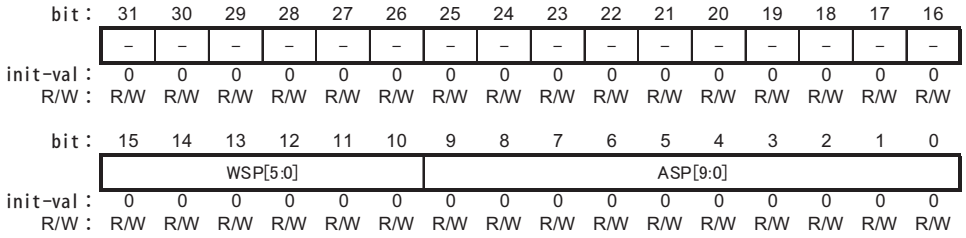
Set the number of request-waiting cycle when arbitration mode is Grant-Times-based arbitration.

Bits 31 to 16: Reserved

These bits are always read as 0. The write value should always be 0.

HS-GPR Arbitration Control Register 4 (CMPRARCR24)

CMPRARCR24 sets arbitration control parameters.



Bits 9 to 0: acnum (SPU)

Set the number of requests that accepted continuously when arbitration mode is Grant-Times-based arbitration.

Bits 15 to 10: wnum (SPU)

Set the number of request-waiting cycle when arbitration mode is Grant-Times-based arbitration.

Bits 31 to 16: Reserved

These bits are always read as 0. The write value should always be 0.

HS-GPR Arbitration Control Register 5 (CMPRARCR25)

CMPRARCR25 sets arbitration control parameters.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
init-val :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
init-val :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits 31 to 0: Reserved

These bits are always read as 0. The write value should always be 0.

Error Control Register (CMPRERRMSK)

CMPRERRMSK sets error response control parameters.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
init-val :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	ERRMSK[1:0]	
init-val :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	0	R/W	R/W

Bit 0: Error mask

0: normal operation

1:Suppress error response when initiator accesses reserved address.

(Caution) If error response is masked, initiator cannot notice these errors. It causes system freeze. Do not set this register as usual.

Bits 1: Error mask

0: normal operation

1:Suppress error response when target ports response are error response.

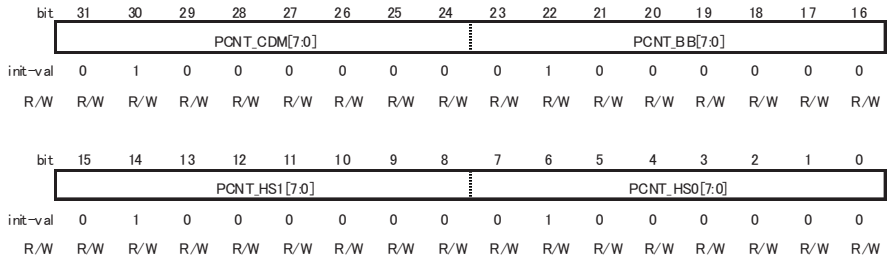
(Caution) If error response is masked, initiator cannot notice these errors. It causes system freeze. Do not set this register as usual.

Bits 31 and 2: Reserved

These bits are always read as 0. The write value should always be 0.

SBSC2 Priority Setting Register 1 (CMPRPRICNT11)

CMPRPRICNT11 sets control parameters of urgent transfer to SBSC2.



Bits 7 to 0: number of times of urgent transfer requests which is granted continuously (HS-GPR)

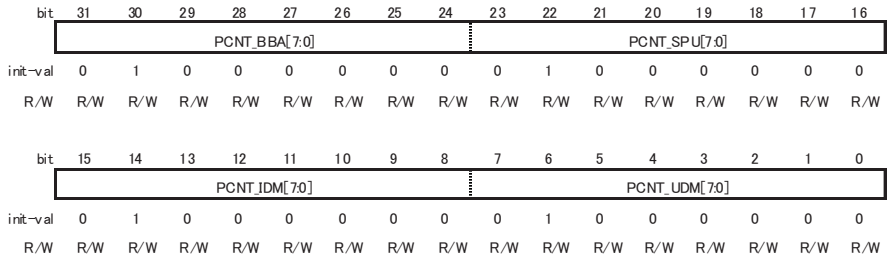
Bits 15 to 8: Reserved

Bits 23 to 16: Reserved

Bits 31 to 24: Reserved

SBSC2 Priority Setting Register 2 (CMPRPRICNT12)

CMPRPRICNT12 sets control parameters of urgent transfer to SBSC2.



Bits 7 to 0: number of times of urgent transfer requests which is granted continuously (CC5/USB-DMAC/CoreSight)

Bits 15 to 8: Reserved

Bits 23 to 16: number of times of urgent transfer requests which is granted continuously (SPU)

Bits 31 to 24: Reserved

SBSC2 Priority Setting Register 3 (CMPRPRICNT13)

CMPRPRICNT13 sets control parameters of urgent transfer to SBSC2.

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
init-val	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	PCNT_SB[7:0]							
init-val	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 31 to 0: Reserved

SBSC2 Priority Setting Register 4 (CMPRPRICNT14)

CMPRPRICNT14 sets control parameters of urgent transfer to SBSC2.

If this register is set, SHwy router temporally cancels Pri value specified cycles before when the times of urgent transfer to SBSC1 reach the PCNT** register value, and switching to the next urgent transfer.

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
init-val	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	NPEN	NPCNT[7:0]							
init-val	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 to 0: ZS cycles of urgent transfer requests canceled when NPEN=1.

Bits 8: enables cancelling cycles of urgent transfer

0 : disable

1: enable

Bits 31 to 9: Reserved

1-F.2.5 Setting a bus-occupancy rate via an arbitration control register

(1) Calculation of register values

(a) *acnum*: Number of requests that grants continuously

In the case register value for each initiator is A,B,C,D,E and F, bus occupation of initiator A is:

A/(A+B+C+D+E+F)

If sum of A to F equal to 100, bus occupation is A% .

For example, setting of HS-GPR can be calculated as follows:
ICB : 15%=int(15/(15+25+25+10+0+25))*100=int(15/100)*100=15
SYS-CPU : 25%=int(25/(15+25+25+10+0+25))*100=int(25/100)*100=25
Com-GPR : 25%=int(25/(15+25+25+10+0+25))*100=int(25/100)*100=25
SYS-DMAC : 10%=int(10/(15+25+25+10+0+25))*100=int(10/100)*100=10
3DG : 0%=0
RT-GPR : 25%=int(25/(15+25+25+10+0+25))*100=int(25/100)*100=25

Bus occupation of each initiator can be calculated if sum of A to F equal to 100 or other value.
Setting value larger, a initiator can access more continuously.
Specially to SDRAM , its effective bus transfer rate increases when accessing address is continuous. So if register value is set larger, total effective bus rate is higher.

On the other hand, arbitration waiting time is increased; worst time of a request is longer.

(b) *wnum*: the number of request-waiting cycle

If initiator's request is not asserted, SHwy router's arbitration switches to other initiator even if register value *acnum* is set to large value.

Register value *wnum* can be used when bus occupation ratio of an initiator is decreased by interruption of other initiator's request.

If *wnum* is set, SHwy router is not switch arbitration to other initiator in *wnum* cycles if current initiator's request is not asserted.

But, setting *wnum* can cause increasing time any initiator's request is not accepted. So if *wnum* is set larger value, total effective bus rate is lower.

(2) About lock transfer

Executing the TAS.B instruction of AP-RTCPU or the SWAP instruction of AP-SYSCPU or BBCPU requires exclusive control of memory. To achieve this, perform lock transfer for SHwy. If any of the three CPUs performs lock transfer, other initiators stop access to SHwy. In the lock transfer control range, the request resource shown in appendix C.2.2 serves as a unit of lock transfer.

(3) Arbitration decision priority

The priority of decision between arbitration controls is as follows:

Lock transfer > urgent transfer > Grant-times-based arbitration

1-F.2.6 Possible Bus Conflict

The SHwy bus (RT/HS/Common) in the AP domain is a star-type bus configuration. The SHwy protocol is a split transaction where request transmission and response reception are independent.

Request resources and response resources are allocated as follows:

Router	req/res	Resource #	Target
RT system	request	0	HS-GPR
		1	Others*[1]
	response	0	AP-Realtime core (SHX)
		1	Others*[2]
HS system	request	0	SBSC1
		1	ICB
		2	Com-GPR
		3	Others*[3]
	response	0	AP-SYSTEM core
		1	ICB
		2	Others*[4]
			Com-GPR
		3	RT-GPR
Common system	request	0	SBSC2
		1	HS-GPR
		2	BSC
		3	Others*[5]
	response	0	HS-GPR
		1	Others*[6]

Notes: 1. RT-HPB, Debug
2. HS-GPR, RTDMAC, Debug
3. 3DG
4. SYSDMAC, 3DG
5. Common-HPB, SPU
6. SPU, MFI

Access destinations where resource allocation differs can be simultaneously accessed without being affected each other. If both CPUs in the AP domain simultaneously access different memory targets, possible conflict in the SHwy request resource is as follows:

From AP-Realtime Core	From AP-SYSTEM Core	Possible Conflict in SHwy
APL SDRAM (SBSC1)	BSC	No conflict
	MERAM	No conflict
	MFI RAM (Sys)	No conflict
Asynchronous RAM, flash memory(BSC)	SBSC1	No conflict
	MERAM	No conflict
	MFI RAM (Sys)	No conflict
MERAM	SBSC1	No conflict
	BSC	No conflict
	MFI RAM (Sys)	No conflict
MFI RAM (Sys)	SBSC1	No conflict
	BSC	No conflict
	MERAM	No conflict

1-F.2.7 HPB Addresses in System Domain

The addresses of peripheral modules connected to the HPB in the system domain are allocated to the following two locations on the memory map:

(1) H'E6000000 to H'E6FFFFFF(HPB Code)

(2) H'E7000000 to H'E7FFFFFF(HPB Data)

(1) and (2) are not mere shadow addresses and are connected to the ports independent of SHwy.

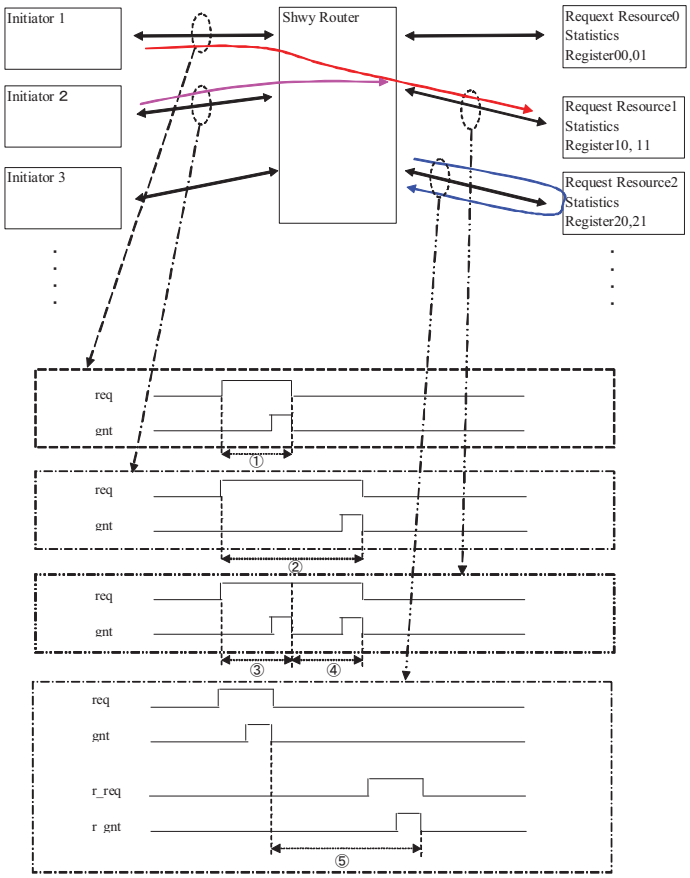
The HPB in SystemDomain is a star-type bus configuration. For this reason, the addresses in (1) and (2) can be accessed independently and simultaneously without intervention to any two modules if they are not the same module.

For example, setting DMA transfer and program read from MFI in H'E7000000 in (2) and reading the register for interrupt processing from H'E6000000 in (1) provides high-speed interrupt processing without being affected by burst RW operations such as DMA transfer that require a long time.

1-F.3 SHwy Statistics Function (SHWYSTAT)

1-F.3.1 Summary

SHWYSTAT is a module that collects the statistical information of pass requests for SHwy. It measures and records time differences between req(request) and gnt(grant) signals of each initiators and targets. Recorded informations can be confirmed the amount of access and the generation of delay by the competition.



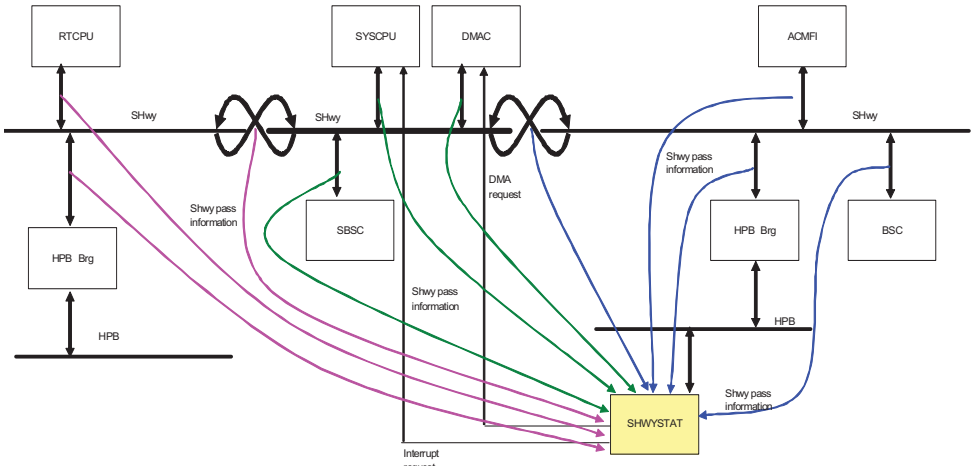
Transaction Filter is OFF:
③、④ is increased to Statistics Register 10,11,12. Statistics Register 40,41.42 is invalid.

Transaction Filter is ON:
When Initiator1 is selected, ① is increased to Statistics Register40,41,42 and ③ is increased to Statistics Register10,11,12.

When Initiator2 is selected, ② is increased to Statistics Register40,41,42 and ④ is increased to Statistics Register10,11,12.

Data that SHWYSTAT collects

Following figure indicates the connection relationship of SHWYSTAT.



SHWYSTAT connection relationship

1-F.3.2 Function

1-F.3.2.1 Summary

- Collecting of statistical information of request waiting time on SHwy
  - Initiator filter
  - Address range filter
  - Enable setting of each filters at the same time
- Collecting of target response information
  - Time from request receipt completion to response arrival completion
  - Initiator filter
- Double registers, Continuous measurement
- Interrupt request signal
- DMA request signal
- Counter that indicate completion of measurement

1-F.3.2.2 SHWYSTAT Registers

(1) **Register List**

Name	Register Abbreviation	R/W	Initial Value	Address	Access Size (Bits)
Transaction statistics control register	SHST??CR	R/W	H'0000 0000	H'XXXX0000	32
Interrupt control register	SHST??IR	R/W	H'0000 0000	H'XXXX0004	32
DMA transfer control register	SHST??DMR	R/W	H'0000 0000	H'XXXX0008	32
DMA transfer data register	SHST??DATA	R	Undefined	H'XXXX0100	32

Name	Register Abbreviation	R/W	Initial Value	Address	Access Size (Bits)
Measurement count register	SHST??CNT	R/W	H'0000 0000	H'XXXX000C	32
Measurement cycle count set register	SHST??TN	R/W	H'0000 0000	H'XXXX0010	32
Pass request count register	SHST??TR	R/W	H'0000 0000	H'XXXX0014	32
Address mask register 1	SHST??AM1	R/W	H'0000 0000	H'XXXX0018	32
Address mask register 2	SHST??AM2	R/W	H'0000 0000	H'XXXX001C	32
Transaction mask register	SHST??TM	R/W	H'0000 0000	H'XXXX0020	32
Transaction statistics register 00	SHST??SR00	R	H'0000 FFFF	H'XXXX0030	32
Transaction statistics register 01	SHST??SR01	R	H'0000 0000	H'XXXX0034	32
Transaction statistics register 02	SHST??SR02	R	H'0000 0000	H'XXXX0038	32
Transaction statistics register 10	SHST??SR10	R	H'0000 FFFF	H'XXXX003C	32
Transaction statistics register 11	SHST??SR11	R	H'0000 0000	H'XXXX0040	32
Transaction statistics register 12	SHST??SR12	R	H'0000 0000	H'XXXX0044	32
Transaction statistics register 20	SHST??SR20	R	H'0000 FFFF	H'XXXX0048	32
Transaction statistics register 21	SHST??SR21	R	H'0000 0000	H'XXXX004C	32
Transaction statistics register 22	SHST??SR22	R	H'0000 0000	H'XXXX0050	32
Transaction statistics register 30	SHST??SR30	R	H'0000 FFFF	H'XXXX0054	32
Transaction statistics register 31	SHST??SR31	R	H'0000 0000	H'XXXX0058	32
Transaction statistics register 32	SHST??SR32	R	H'0000 0000	H'XXXX005C	32
Transaction statistics register 40	SHST??SR40	R	H'0000 FFFF	H'XXXX0060	32
Transaction statistics register 41	SHST??SR41	R	H'0000 0000	H'XXXX0064	32
Transaction statistics register 42	SHST??SR42	R	H'0000 0000	H'XXXX0068	32
Transaction statistics register 50	SHST??SR50	R	H'0000 FFFF	H'XXXX006C	32
Transaction statistics register 51	SHST??SR51	R	H'0000 0000	H'XXXX0070	32
Transaction statistics register 52	SHST??SR52	R	H'0000 0000	H'XXXX0074	32
Transaction statistics register 60	SHST??SR60	R	H'0000 FFFF	H'XXXX0078	32
Transaction statistics register 61	SHST??SR61	R	H'0000 0000	H'XXXX007C	32
Transaction statistics register 70	SHST??SR70	R	H'0000 FFFF	H'XXXX0080	32
Transaction statistics register 71	SHST??SR71	R	H'0000 0000	H'XXXX0084	32
Transaction statistics register 80	SHST??SR80	R	H'0000 FFFF	H'XXXX0088	32
Transaction statistics register 81	SHST??SR81	R	H'0000 0000	H'XXXX008C	32
Transaction statistics register 90	SHST??SR90	R	H'0000 FFFF	H'XXXX0090	32
Transaction statistics register 91	SHST??SR91	R	H'0000 0000	H'XXXX0094	32
Transaction statistics register 100	SHST??SR100	R	H'0000 FFFF	H'XXXX0098	32
Transaction statistics register 101	SHST??SR101	R	H'0000 0000	H'XXXX009C	32
Transaction statistics register 110	SHST??SR110	R	H'0000 FFFF	H'XXXX00A0	32
Transaction statistics register 111	SHST??SR111	R	H'0000 0000	H'XXXX00A4	32

?? : RT/HS/CM

XXXX : RT=H'FFCF, HS=H'E6F3, CM=H'E6F2

(2) Register function

Transaction Statistics Control Register

The transaction statistics control registers specifies statistical collection start and how to collect statistical information.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						AM	SM2	SM1					COM	RUN	MD	GO
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R	R/W	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 11	-	0	R	Reserved These bits are always read as 0. The write value should always be 0.
10	AM	0	R/W	Enable Address mask 0: Disable 1: Enable
9	SM2	0	R/W	Enable Initiator ID mask2 0: Disable 1: Enable
8	SM1	0	R/W	Enable Initiator ID mask1 0: Disable 1: Enable
7 to 4	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
3	COM	0	R/W	Enable synchronized operation to Com-SHWYSTAT 0: Disable 1: Enable
2	RUN	0	R	Operation Status 0: No operating 1: Operating
1	MD	0	R/W	Select execution mode 0: Normal mode 1: Continuous mode
0	GO	0	R/W	Measurement Start

Interrupt Control Register

The interrupt control register controls the enable/disable of interrupt factor from SHWYSTAT.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TEM	ADM	-	-	-	-	-	-	TE	AD	-	-	-	-	-	IE
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31to16	-	0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	TEM	0	R/W	Interrupt mask by the measurement completion(Once measurement completion when the continuous mode is set) 0: Enable interrupt mask 1: Disable interrupt mask
14	ADM	0	R/W	Interrupt mask by the specified access detection. 0: Enable interrupt mask 1: Disable interrupt mask
13to8	-	0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	TE	0	R/W	This bit indicates whether interrupt is occurred or not by the measurement completion(Once measurement completion when the continuous mode is set) It is cleared to 0 when 0 is written, and is retained when 1 is written. 0: The measurement is not completed yet 1: The measurement is completed.
6	AD	0	R/W	This bit indicates whether the interrupt by the specified access detection occurred or not. It is cleared to 0 when 0 is written, and is retained when 1 is written. 0: The specified access is not detected. 1: The specified access is detected.
5to1	-	0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	IE	0	R/W	Enable interrupt output from SHWYSTAT.

DMA Transfer Control Register

The DMA transfer control register controls the DMA request. It is possible to collect measurement results by DMA in the continuous mode.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	DACK_CNT							
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DACK_NUM								-	-	-	-	-	-	DM	DE
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31to24	-	0	R	Reserved These bits are always read as 0. The write value should always be 0.
23to16	DACK_CNT	0	R	These bits indicate the number of registers that DMA transfer is completed. They are always 0 when DE=0. They are initialized to 0, when the measurement is completed at DE=1 and DMA is ready to transfer. When DACK_CNT value is equal to DACK_NUM value, DMA completes.
15to8	DACK_NUM	0	R/W	These bits indicate the number of registers to be transferred by DMA. Set value of “(Number of registers)-1”. In the 32byte DMA transfer, set value rounded up to multiple of four.
7to2	-	0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	DM	0	R/W	DMA transfer unit 0: Long word(4byte) 1: 32byte
0	DE	0	R/W	Enable DMA request output 0: Disable DMA request 1: Enable DMA request

DMA Transfer Data Register

The DMA transfer data register is used as DMA source address to collect measurement results in the continuous mode. DMA can read SHWYSTAT register data sequentially. This register can’t be read by CPU.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DATA31-16															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA15-0															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31to0	DATA	0	R	Register value transferred by DMA.

Measurement Frequency Counter Register

The measurement frequency counter register counts the frequency of measurement completion in the continuous mode. It is cleared to 0 when written.

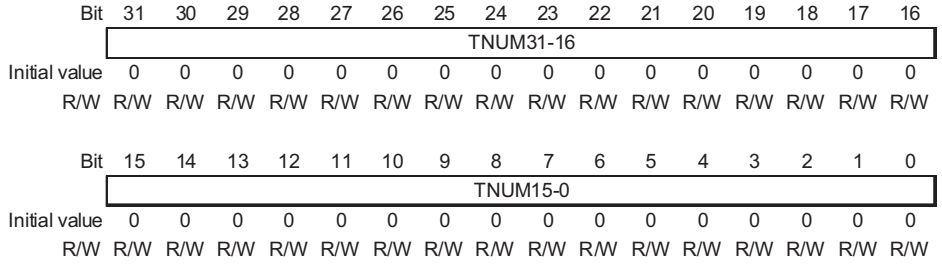
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CNT31-16															
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CNT15-0															
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31to0	CNT	0	R/W	Frequency of the measurement completion

Measurement Cycle Set Register

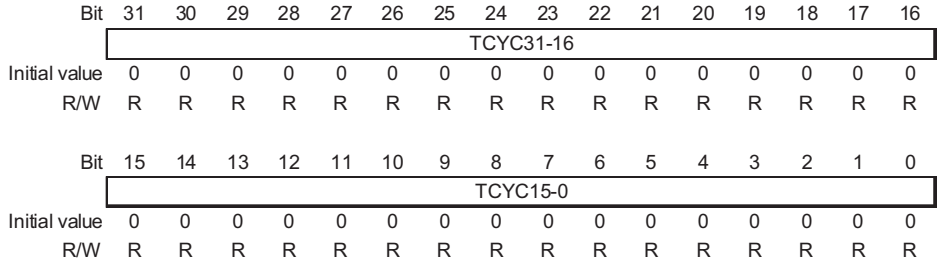
The measurement cycle set register sets the measurement period. In the continuous mode, it sets once setting period. The period of 1 cycle is calculated as 1 SHwy clock cycle.



Bit	Bit Name	Initial Value	R/W	Descriptions
31to0	TNUM	0	R/W	Measurement cycle

Passage Cycle Count Register

The passage cycle count register indicates the number of passage cycle during the measurement period. In the continuous mode, it indicates once setting period.



Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 0	TCYC	0	R	Number of Passage Cycle

Address Mask Register1

The address mask register1 sets the top address to collect statistic information. The address to specify is the 16 byte unit.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ADDMSK1[31:16]															
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ADDMSK1[15:4]												-	-	-	-
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 4	ADDMSK1	0	R/W	Address mask top address
3 to 0	-	0	R	Reserved These bits are always read as 0. The write value should always be 0.

Address Mask Register2

The address mask register2 sets the end address to collect statistic information. The address to specify is the 16 byte unit. It is necessary to set the value more than that of the address mask register1.

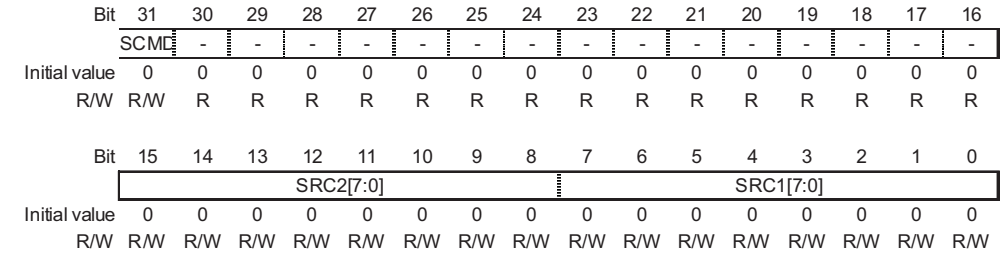
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ADDMSK2[31-16]															
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ADDMSK2[15-4]												-	-	-	-
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 4	ADDMSK2	0	R/W	Address mask end address
3 to 0	-	0	R	Reserved These bits are always read as 0. The write value should always be 0.

Transaction Mask Register

The transaction mask register sets the condition to mask transaction ID.



Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SCMD	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SRC2[7:0]								SRC1[7:0]							
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31	SCMD	0	R/W	Enable direct ID mode. It is used to collect access information from HSGPR to ComGPR. SRC1≦SRC2 Only SM=01 is valid in the direct ID mode.
30to16	-	0	R	Reserved These bits are always read as 0. The write value should always be 0.
15to8	SRC2	0	R/W	Masking by Initiator. Refer to the below table.
7to0	SRC1	0	R/W	Masking by Initiator. Refer to the below table.

SRC1/2	Initiator
H'00	Default
H'01	RT-CPU
H'02	SYS-CPU
H'03	RT-DMAC
H'04	SYS-DMAC,DDM
H'05	ICB
H'06	SGX
H'07	USBDMAC0
H'08	USBDMAC1
H'09	SPU
H'0A	CC5
H'0B	ACMFI
H'0C	CoreSight

The data pass from HS-GPR to Com-GPR has 2 passes, HPB pass and others. To collect statistics information of each passes, it sets as follows.

It is mandatory to set 0 to SM2 bit of SHSTCMCR register to apply the direct ID mode.

It sets 1 to SCMD bit of SHSTCMCR register to apply the direct ID mode.

To collect information of HPB access, set H'01 to SRC1 bits of SHSTCMTM register and set H'50 to SRC2 bits of SHSTCMTM register.

To collect information of other targets access, set H'00 to SRC1 bits of SHSTCMTM register and set H'50 to SRC2 bits of SHSTCMTM register.

Transaction Statistic Register l0

Transaction statistics register l0 indicates the statistical results of request resource l (l = 0,1,2,3).

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MAX[15:0]															
Initila value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MIN[15:0]															
Initial value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 16	MAX[15:0]	H'0000	R	Maximum Number of ZSϕ Cycles from req Assert to gnt Assert
15 to 0	MIN[15:0]	H'FFFF	R	Minimum Number of ZSϕ Cycles from req Assert to gnt Assert

Transaction Statistics Register l1

Transaction statistics register l1 indicates the statistical results of request resource l (l=0,1,2,3).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SUM[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SUM[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 0	SUM[31:0]	H'0000 0000	R	Sum of ZSϕ Cycles from req Assert to gnt Assert The average number of ZSϕ Cycles from req Assert to gnt Assert can be calculated by dividing this sum by the number of pass requests.

Transaction Statistics Register l2

Transaction statistics register l2 indicates the statistical results of request resource l (l=0,1,2,3)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TCNT[31:16]															
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TCNT[15:0]															
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 0	TCNT	0	R	Number of pass requests.

Transaction Statistics Register m0

Transaction statistics register m0 indicates the statistical results between an initiator and router. (m=4,5) It is necessary to specify a filter per initiator.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MAX[15:0]															
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MIN[15:0]															
Initial value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 16	MAX[15:0]	H'0000	R	Maximum Number of ZSϕ Cycles from req Assert to gnt Assert
15 to 0	MIN[15:0]	H'FFFF	R	Minimum Number of ZSϕ Cycles from req Assert to gnt Assert

Transaction Statistics Register m1

Transaction statistics register m1 indicates the statistical results between an initiator and router. (m=4,5) It is necessary to specify a filter per initiator.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SUM[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SUM[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 0	SUM[31:0]	H'0000 0000	R	Sum of ZSϕ Cycles from req Assert to gnt Assert The average number of ZSϕ Cycles from req Assert to gnt Assert can be calculated by dividing this sum by the number of pass requests.

Transaction Statistics Register m2

Transaction statistics register m2 indicates the statistical results between an initiator and router. (m=4,5) It is necessary to specify a filter per initiator.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TCNT[31:16]															
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TCNT[15:0]															
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 0	TCNT	0	R	Number of pass requests.

Transaction Statistics Register n0

Transaction statistics register n0 indicates the statistics results of target n. (n=6,7,8,9,10,11)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MAX[15:0]															
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MIN[15:0]															
Initial value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 16	MAX[15:0]	H'0000	R	Maximum Number of ZSϕ Cycles from req Assert completion to r_req Assert completion.
15 to 0	MIN[15:0]	H'FFFF	R	Minimum Number of ZSϕ Cycles from req Assert completion to r_req Assert completion.

Transaction Statistics Register n1

Transaction statistics register n1 indicates the statistics results of target n. (n=6,7,8,9,10,11)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SUM[31:16]															
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SUM[15:0]															
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 0	SUM[31:0]	H'0000 0000	R	Sum of ZSϕ Cycles from req Assert completion to r_req Assert completion The average number of ZSϕ Cycles from req Assert completion to r_req Assert completion can be calculated by dividing this sum by the number of pass requests.

1-F.3.2.3 Explanation of SHWYSTAT operation

The following process makes collecting SHwy statistic information possible.

(1) Setting parameters to collect statistic information.

(2) Start and Stop.

1-F.3.2.3.1 Method to set parameters

1-F.3.2.3.1.1 Kinds of data that is able to collect

The following information is able to be collected.

- Statistic information of request resources
- Statistic information of target responses
- Generation information of specified accesses

The following section is explained about each setting to collect information.

1-F.3.2.3.1.2 Statistic information of request resources

It is necessary to set the measurement cycle set register before SHWYSTAT execution. Using the transaction mask and the address mask, it is possible to collect more detail information. Statistic information is recorded to registers corresponding to each resource after the measurement cycle was set and it starts the measurement.

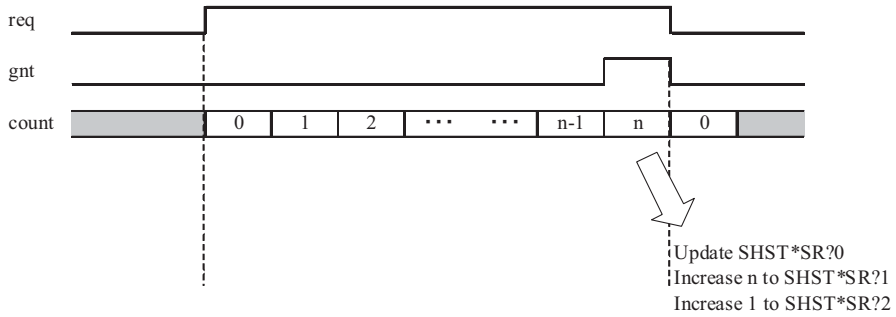


Figure 1-F-3 Cycle recorded in transaction statistics register l0tol2 and m0tom2

	RT SHWYSTAT	HS SHWYSTAT	COM SHWSTAT
Transaction Statistics Register 00to02	HS-GPR	SBSC1	HS-GPR
Transaction Statistics Register 10to12	Other *1	ICB	BSC
Transaction Statistics Register 20to22	n.a.	Com-GPR	Other *3
Transaction Statistics Register 30to32	n.a.	Other *2	n.a.

*1 RT-HPB,SHX,Debug

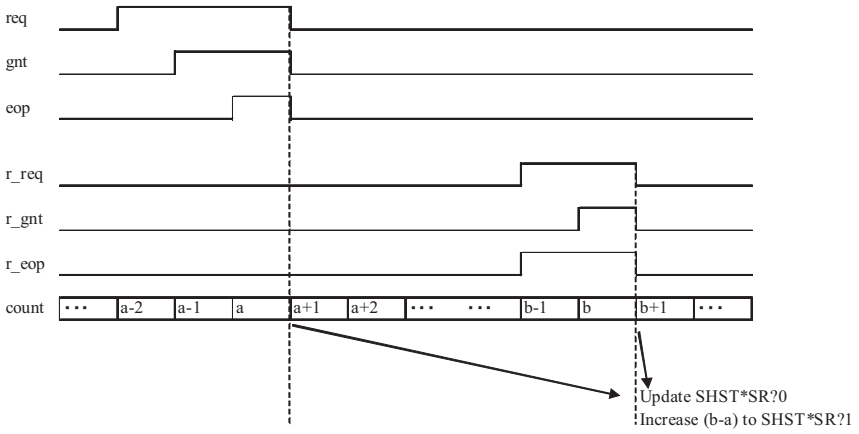
*2 RT-GPR, SGX Registers

*3 Com/SYS-HPB

1-F.3.2.3.1.3 Statistic information of target responses

It is possible to collect statistic information of target responses accessed by the initiator specified to SRC1 bits in the transaction mask register. The address mask is not corresponded. Setting SRC1 bits to collect statistic information is necessary. If not set, the register value is invalid. The average number can be calculated by dividing by the value of the transaction statistics register 42(SHSTXXSR42).

To collect statistic information of target responses, it is mandatory to start SHWYSTAT when there is no access to targets.



	RT SHWYSTAT	HS SHWYSTAT	COM SHWYSTAT
Transaction Statistics Register 60to61	SHX	RT-GPR*	HS-GPR*
Transaction Statistics Register 70to71	DBG	SGX	BSC
Transaction Statistics Register 80to81	RT-HPB	ICB	HPB(0xE6??)
Transaction Statistics Register 90to91	HS-GPR*	SBSC1	HPB(0xE7??)
Transaction Statistics Register 100to101	n.a.	COM-GPR*	n.a.
Transaction Statistics Register 110to111	n.a.	COM-GPR(HPB)*	n.a.

*It can not be measured the correct max/min cycle number because GPR bridge has some targets.

1-F.3.2.3.1.4 Measurement filter

The transaction statistics information register 00-32 can be collected statistic information filtered by the address mask and the transaction ID mask. These filters are specified by SM1, SM2 and AM bits of the transaction control register, the address mask register1, 2 and the transaction mask register.

- Case1: Specified address mask and SRC1 mask, it is recorded in (address & SRC1) conditions.
- Case2: Specified address mask and SRC2 mask, it is recorded in (address & SRC2) conditions.
- Case3: Specified SRC1 mask and SRC2 mask, it is recorded in (SRC1 | SRC2) condition.
- Case 4: Specified all (Address, SRC1 and SRC2) mask, it is recorded in (SRC1|SRC2) & address conditions.

The transaction statistics information register 40-52 can be collected statistic information filtered by the address mask and the transaction ID mask. These filters are specified by SM1,SM2 and AM bits of the transaction control register, the address mask register1,2 and the transaction mask register. It is mandatory for the transaction statistics register 40-42 to specify SRC1 bit, and it is mandatory for the transaction statistics register 50-52 to specify SRC2 bit.

- Case1: Specified address mask and SRC1 mask, it is recorded in address & SRC1 conditions.
- Case2: Specified address mask and SRC2 mask, it is recorded in address & SRC2 conditions.

It is mandatory for the transaction statistics register 60-111 to specify SRC1 bit. It is possible to collect information by specifying only SRC1 bits, however it is mandatory to set SM bit of the transaction control register to get pass request number.

1-F.3.2.3.1.5 Generation information of specified accesses

It sets the address mask register1, 2 or the transaction mask register. If AD bit of the interrupt control register is 1 and the specified access generates, the specified access interruption can be occurred.

1-F.3.2.3.2 Start and Stop

1-F.3.2.3.2.1 Measurement start

- Setting contents of the measurement
- Setting the measurement period

- Clear the measurement frequency counter (the Continuous mode)

After setting above-mentioned, SHWYSTAT can be started when 1 is written to GO bit of the transaction control register.

Setting example:

Getting statistic information of Real-Time CPU

Register : SHST??TM write data: H'00000001

The measurement period = 30ms

ZSϕ200MHz(Cycle: 5ns), 30ms/5ns=6000000 = H'005B8D80

Register: SHST??TN write data: H'005B8D80

Getting the address range of H'E6050000 to H'E6060000

Register: SHST??AM1 write data: H'E6050000

Register: SHST??AM2 write data: H'E6060000

Enable the measurement completed interruption

Register: SHST??IR write data: H'00008001

Start the measurement. (Enable SRC1 mask and address mask)

Register: SHST??CR write data: H'00000501

1-F.3.2.3.2.2 Continuous mode

The continuous mode setting adds the measurement frequency count clear and MD=1 of the control register to 1-F.3.2.3.2.1 settings.

Setting example:

Clear the measurement frequency counter

Register: SHST??CNT write data: H'00000000

Start the measurement. (Enable SRC1 mask and address mask)

Register: SHST??CR write data: H'00000503

In the case of the execution in the continuous mode, it is necessary for the measurement cycle set register to set sufficient measurement period to execute the interrupt handle and DMA transfer. The measurement cycle counter can be checked whether the interrupt handle and DMA transfer are in time or not. If the value of the cycle counter increase by one, their handles are in time, however an increase in two or more is not.

SHWYSTAT repeats the measurement while operating in the continuous mode. The way to stop the continuous mode set MD=0, GO=0 of the statistic control register. Setting MD=0,GO=0 is stopped SHWYSTAT at once. The last measurement period is not guaranteed.

1-F.3.2.3.2.3 Collecting statistic results by DMA

SHWYSTAT can request DMA transfer when the measurement was completed.

Setting example:

Get all register values by DMA

Register: SHST??DMR write data: H'00360001

Set the DMA transfer data register address to the DMA source address register

Register: DM??SAR write data: H'XXXX0100

XXXX: RT=H'FFCF, HS=H'E6F3, CM=H'E6F2

1-F.3.2.3.2.4 Synchronize mode

The synchronize mode can be executed 3-domain (Real-Time, Hi-Speed and Common) SHWYSTAT modules by the trigger of Common-SHWYSTAT execution.

Real-Time and Hi-Speed SHWYSTAT are set 1 to COM bit of each statistic control register. After that, Real-Time, Hi-Speed and Common SHWYSTAT start all together when Common SHWYSTAT is set to start. All SHWYSTAT can stop when set stopping Common-SHWYSTAT (set MD=0, GO=0 of the statistics control register).

1-F.3.2.3.2.5 Measurement end

When the passage cycle count register is 0, SHWYSTAT stops the measurement. It can be stopped SHWYSTAT to write 0 to GO bit of the statistic control register while operating. To stop SHWYSTAT in the continuous mode, it is mandatory to write 0 to MD bit and GO bit at the same time.

1-F.3.2.4 Notes

1-F.3.2.4.1 About the register retained period

The register retained period indicates as follows when it is unreset and unclear.

Normal mode:

All registers are retained until the next execution.

Continuous mode:

When the interruption is valid, all registers are retained until the measurement completion interrupt factor is cleared. After cleared it, they are updated when next measurement is completed. If the interrupt factor is not cleared until the next measurement completion, registers are not updated.

When the DMA transfer is valid, all registers are retained until DMA transfer is completed. After DMA completed, they are updated when next measurement is completed. If DMA is not completed until the next measurement completion, registers are not updated.

When neither the interruption nor DMA request is valid, all registers are updated when the next measurement is completed.

Clear of registers:

All registers are cleared when the measurement frequency cycle register is cleared to 0. It does not depend on the mode.

1-F.3.2.4.2 About the measurement cancel

It forbids to stop SHWYSTAT by the module stop control register in CPG module. Especially in the case of using the interruption and DMA, it causes error to stop by the module stop, because the interruption and DMA may keep request.

1-F.4 HPB Bus Functions

1-F.4.1 Bus Control Registers

The HPB has bus control registers.

HPB Registers

Name	Register Abbreviation	R/W	Initial Value	Address	Access Size (Bits)
HPB control register 0	HPBCTRL0	R/W	H'0000 0000	H'E6001010	32
HPB control register 1	HPBCTRL1	R/W	H'0000 0000	H'E6001014	32
HPB control register 2	HPBCTRL2	R/W	H'0000 0000	H'E6001018	32
Common Chip Code register	CCCR	R	-	H'E600101C	32
HPB control register 4	HPBCTRL4	R/W	H'0000 0000	H'E6001024	32
HPB control register 5	HPBCTRL5	R/W	H'0000 088C	H'E6001028	32

Register States in Each Operating Mode

Register Abbreviation	Power-on Reset	System Reset	A4S Area Reset
HPBCTRL0	Initialized	Initialized	Retained
HPBCTRL1	Initialized	Initialized	Retained
HPBCTRL2	Initialized	Initialized	Retained
CCCR	Initialized	Initialized	Retained
HPBCTRL4	Initialized	Initialized	Retained
HPBCTRL5	Initialized	Initialized	Retained

For details, refer to section 1-D Overview of reset.

HPB Control Register 0

HPB control register 0 switches the addresses of BBIF2 modules both RealTime and System can access. This register also controls the simplified-random number generation bit.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RND	RNDEN	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	BBIF2SEL[1:0]		-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31	RND	0	R	Simplified-Random Number Bit
30	RNDEN	0	R/W	Simplified-Random Number Control Bit 0: Random Number Generation Disable 1: Random Number Generation Enable
29 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5, 4	BBIF2SEL	0	R/W	BBIF2 Address Select Set an BBIF2 address and operating clock. 00: The start address of the BBIF2 register is H'FFFA0000. 01: The start address of the BBIF2 register is H'E6CA0000. 10: Reserved. Setting prohibited. 11: Reserved. Setting prohibited.
3 to 0	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

HPB Control Register 1

HPB control register 1 controls ON/OFF of the dynamic module stop control functions of buses on the RealTime domain.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	DMSENSHR	DMWTSHR[2:0]			-	-	-	-	DMSENHPR	DMWTHPR[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	DMSENHSR	DMWTHSR[2:0]			-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 28	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
27	DMSENSHR	0	R/W	RT-SHwy Dynamic Module Stop Control 0: Disables RT-SHwy dynamic module stop. 1: Enables RT-SHwy dynamic module stop.
26 to 24	DMWTSHR	0	R/W	RT-SHwy Dynamic Module Stop Time *1 000: Module stop 1 cycle after no bus is accessed 001: Module stop 4 cycles after no bus is accessed 010: Module stop 8 cycles after no bus is accessed ..... 111: Module stop 256 cycles after no bus is accessed Cycles are counted based on ZSϕ.
23 to 20	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
19	DMSENHPR	0	R/W	RT-HPB Dynamic Module Stop Control 0: Disables RT-HPB dynamic module stop. 1: Enables RT-HPB dynamic module stop.
18 to 16	DMWTHPR	0	R/W	RT-HPB Dynamic Module Stop Time 000: Module stop 1 cycle after no bus is accessed 001: Module stop 4 cycles after no bus is accessed 010: Module stop 8 cycles after no bus is accessed ..... 111: Module stop 256 cycles after no bus is accessed Cycles are counted based on ZSϕ.
15 to 12	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
11	DMSENHSR	0	R/W	RT-HPB Splitter Dynamic Module Stop Control 0: Disables RT-HPB splitter dynamic module stop. 1: Enables RT-HPB splitter dynamic module stop.
10 to 8	DMWTHSR	0	R/W	RT-HPB Splitter Dynamic Module Stop Time 000: Module stop 1 cycle after no bus is accessed 001: Module stop 4 cycles after no bus is accessed 010: Module stop 8 cycles after no bus is accessed ..... 111: Module stop 256 cycles after no bus is accessed Cycles are counted based on ZSϕ.
7 to 0	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.

Notes: 1. The operation of the 000 setting is really the same as the operation of 001 (4 waits) because SHwy internal operation is generated.

HPB Control Register 2

HPB control register 2 controls ON/OFF of the dynamic module stop control functions of buses on the Common/System domain.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DMSEN HSSD	DMWTHSSD[2:0]			DMS ENSHS	DMWTSHS[2:0]			DMS ENHPS	DMWTHPS[2:0]			-	-	DMS ENHSS	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMWTHSS[2:0]			-	-	DMS ENINT	-	-	-	-	-	-	DMSEN DMX43	DMWTDMX43[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R	R	R/W	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31	DMSENHSSD	0	R/W	Common/Sys-HPB Splitter D Dynamic Module Stop Control* 0: Disables Common-SHwy dynamic module stop. 1: Enables Common-SHwy dynamic module stop.
30 to 28	DMWTHSSD	0	R/W	Common/Sys-HPB Splitter D Dynamic Module Stop Time 000: Module stop 1 cycle after no bus is accessed 001: Module stop 4 cycles after no bus is accessed 010: Module stop 8 cycles after no bus is accessed ..... 111: Module stop 256 cycles after no bus is accessed Cycles are counted based on ZSϕ.

Bit	Bit Name	Initial Value	R/W	Descriptions
27	DMSENSHS	0	R/W	Common-SHwy Dynamic Module Stop Control* 0: Disables Common-SHwy dynamic module stop. 1: Enables Common-SHwy dynamic module stop.
26 to 24	DMWTSHS	0	R/W	Common-SHwy Dynamic Module Stop Time 000: Module stop 1 cycle after no bus is accessed 001: Module stop 4 cycles after no bus is accessed 010: Module stop 8 cycles after no bus is accessed ..... 111: Module stop 256 cycles after no bus is accessed Cycles are counted based on ZSϕ.
23	DMSENHPS	0	R/W	Common/Sys-HPB Dynamic Module Stop Control 0: Disables Common/Sys-HPB dynamic stop. 1: Enables Common/Sys-HPB dynamic stop.
22 to 20	DMWTHPS	0	R/W	Common/Sys-HPB Dynamic Module Stop Time 000: Module stop 1 cycle after no bus is accessed 001: Module stop 4 cycles after no bus is accessed 010: Module stop 8 cycles after no bus is accessed ..... 111: Module stop 256 cycles after no bus is accessed Cycles are counted based on ZSϕ.
19 to 18	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
17	DMSENHSS	0	R/W	Common/Sys-HPB Splitter Dynamic Module Stop Control 0: Disables Common/Sys-HPB splitter dynamic module stop. 1: Enables Common/Sys-HPB splitter dynamic module stop.
16	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
15 to 13	DMWTHSS	0	R/W	Common/Sys-HPB Splitter/DIMUX Splitter Dynamic Module Stop Time 000: Module stop 1 cycle after no bus is accessed 001: Module stop 4 cycles after no bus is accessed 010: Module stop 8 cycles after no bus is accessed ..... 111: Module stop 256 cycles after no bus is accessed Cycles are counted based on ZSϕ.

Bit	Bit Name	Initial Value	R/W	Descriptions
12, 11	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
10	DMSENINT	0	R/W	INT Dynamic Module Stop Control 0: Disables INT dynamic module stop. 1: Enables INT dynamic module stop.
9 to 4	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
3	DMSENDMX43	0	R/W	DIMUX(CC5/USBDMAC/Coresight) Dynamic Module Stop Control 0: Disables Common/Sys-HPB dynamic stop. 1: Enables Common/Sys-HPB dynamic stop.
2 to 0	DMWTDMX43	0	R/W	DIMUX(CC5/USBDMAC/Coresight) Dynamic Module Stop Time 000: Module stop 1 cycle after no bus is accessed 001: Module stop 4 cycles after no bus is accessed 010: Module stop 8 cycles after no bus is accessed ..... 111: Module stop 256 cycles after no bus is accessed Cycles are counted based on ZSϕ.

Note: * The operation of the 000 setting is really the same as the operation of 001 (4 waits) because SHwy internal operation is generated.

Common Chip Code Register

Please refer to sec."1-B Address Map".

HPB Control Register 4

HPB control register 4 controls ON/OFF of the dynamic module stop control functions of buses on the Common/System domain.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DMSEN HSH	DMWTHSH[2:0]			DMSEN DMX40	DMWTDMX40[2:0]			-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31	DMSENHSH	0	R/W	HS-SHwy Dynamic Module Stop Control* 0: Disables Common-SHwy dynamic module stop. 1: Enables Common-SHwy dynamic module stop.
30 to 28	DMWTHSH	0	R/W	HS-SHwy Dynamic Module Stop Time 000: Module stop 1 cycle after no bus is accessed 001: Module stop 4 cycles after no bus is accessed 010: Module stop 8 cycles after no bus is accessed ..... 111: Module stop 256 cycles after no bus is accessed Cycles are counted based on ZSϕ.
27	DMSENDMX40	0	R/W	DIMUX(SYS-DMAC,DDM) Dynamic Module Stop Control* 0: Disables Common-SHwy dynamic module stop. 1: Enables Common-SHwy dynamic module stop.
26 to 24	DMWTDMX40	0	R/W	DIMUX(SYS-DMAC,DDM) Dynamic Module Stop Time 000: Module stop 1 cycle after no bus is accessed 001: Module stop 4 cycles after no bus is accessed 010: Module stop 8 cycles after no bus is accessed ..... 111: Module stop 256 cycles after no bus is accessed Cycles are counted based on ZSϕ.
23 to 16	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 0	—	H'FFFF	R	No Funtion The write value should always be initial value.

Note: * The operation of the 000 setting is really the same as the operation of 001 (4 waits) because SHwy internal operation is generated.

HPB Control Register 5

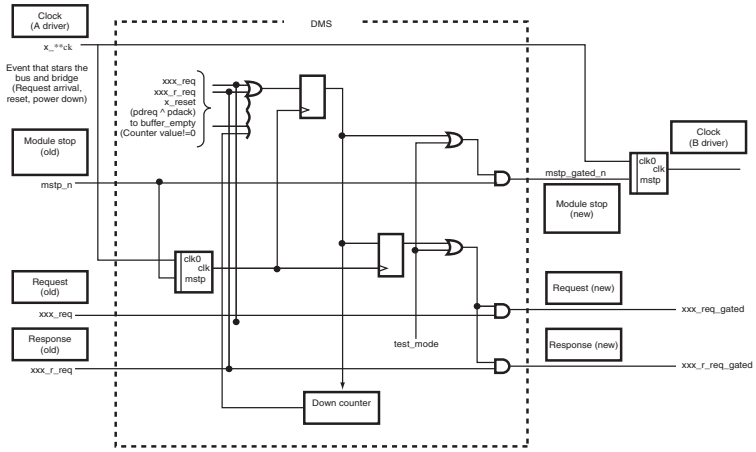
HPB control register 5 controls Pri value of 3DG(SGX).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

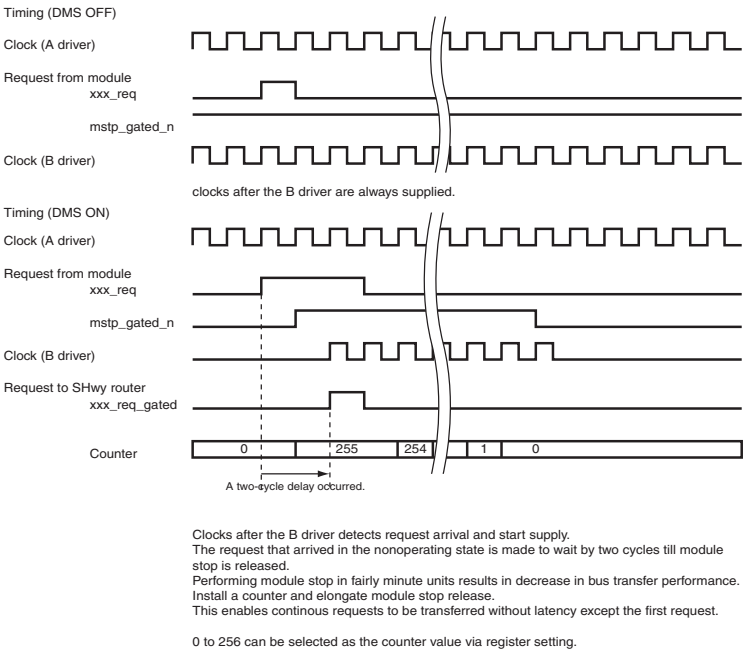
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	SGXPRI[3:0]			
Initial value:	0	0	0	0	1	0	0	0	1	0	0	0	1	1	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 4	—	H'0000 088	R	No Function The write value should always be initial value.
3 to 0	SGXPRI	H'C	R/W	SGX Priority Value

About dynamic module stop (DMS)



The above logic is individually installed in the Bdrivers of the bus and bridge.



However, INT dynamic module stop is clock stop control in the module, so performance changes such as latency increase do not occur according to settings.

1-F.4.2 Bus Semaphore Control Registers

The modules connected to the CommonHPB bus use this bus to support exclusive control via semaphores.

Overview

- Each module has a semaphore.
- In SHwy, the initiator srcID is used to identify the SHwy bus and control access privilege.
- By default (semaphore open status), common resources can be freely accessed.
- The master processor can forcibly acquire semaphores. It can also access common resources even if no semaphore is acquired.
- An access error occurs if an attempt is made to access a common resource when no semaphore is acquired. Information related to this access error is reflected in the register.
- Read access is possible even if no semaphore is acquired.
- Timeout counters support the timeout function based on CPϕ (ON/OFF (initial value) by bit 31).
- The initiator that acquired a semaphore is authorized to write counter values.

1-F.4.2.1 Common HPB Semaphore Control Registers

Name	Register Abbreviation	R/W	Initial Value	Address	Access Size (Bits)
Master ID register	MPSRC	R/W	–	H'E6001600	32
Master access control register	MPACCTL	R/W	H'0000 0000	H'E6001604	32
GPIO semaphore acquisition ID register	SMGPIOSRC	R/W	H'0000 0000	H'E6001820	32
GPIO semaphore error register	SMGPIOERR	R/W	H'0000 0000	H'E6001824	32
GPIO semaphore timeout setting register	SMGPIOTIME	R/W	H'7FFF FFFF	H'E6001828	32
GPIO semaphore timeout counter	SMGPIOCNT	R	H'0000 0000	H'E600182C	32
DBG semaphore acquisition ID register	SMDBGSRC	R/W	H'0000 0000	H'E6001830	32
DBG semaphore error register	SMDBGERR	R/W	H'0000 0000	H'E6001834	32
DBG semaphore timeout setting register	SMDBGTIME	R/W	H'7FFF FFFF	H'E6001838	32
DBG semaphore timeout counter	SMDBGCNT	R	H'0000 0000	H'E600183C	32
CMT2 semaphore acquisition ID register	SMCMT2SRC	R/W	H'0000 0000	H'E6001840	32
CMT2 semaphore error register	SMCMT2ERR	R/W	H'0000 0000	H'E6001844	32
CMT2 semaphore timeout setting register	SMCMT2TIME	R/W	H'7FFF FFFF	H'E6001848	32

Name	Register Abbreviation	R/W	Initial Value	Address	Access Size (Bits)
CMT2 semaphore timeout counter	SMCMT2CNT	R	H'0000 0000	H'E600184C	32
CPGLA semaphore acquisition ID register	SMCPGASRC	R/W	H'0000 0000	H'E6001850	32
CPGLA semaphore error register	SMCPGAERR	R/W	H'0000 0000	H'E6001854	32
CPGLA semaphore timeout setting register	SMCPGATIME	R/W	H'7FFF FFFF	H'E6001858	32
CPGLA semaphore timeout counter	SMCPGACNT	R	H'0000 0000	H'E600185C	32
SYSC semaphore acquisition ID register	SMSYSCSRC	R/W	H'0000 0000	H'E6001870	32
SYSC semaphore error register	SMSYSCERR	R/W	H'0000 0000	H'E6001874	32
SYSC semaphore timeout setting register	SMSYSCTIME	R/W	H'7FFF FFFF	H'E6001878	32
SYSC semaphore timeout counter	SMSYSCCNT	R	H'0000 0000	H'E600187C	32

Register States in Each Operating Mode

Register Abbreviation	Power-on Reset	System Reset	A4S Area Reset
MPSRC	Initialized	Initialized	Retained
MPACCTL	Initialized	Initialized	Retained
SMGPIOSRC	Initialized	Initialized	Retained
SMGPIOERR	Initialized	Initialized	Retained
SMGPIOCNT	Initialized	Initialized	Retained
SMDBGSRC	Initialized	Initialized	Retained
SMDBGERR	Initialized	Initialized	Retained
SMDBGTIME	Initialized	Initialized	Retained
SMDBGCNT	Initialized	Initialized	Retained
SMCMT2SRC	Initialized	Initialized	Retained
SMCMT2ERR	Initialized	Initialized	Retained
SMCMT2TIME	Initialized	Initialized	Retained
SMCMT2CNT	Initialized	Initialized	Retained
SMCPGASRC	Initialized	Initialized	Retained
SMCPGAERR	Initialized	Initialized	Retained
SMCPGATIME	Initialized	Initialized	Retained
SMCPGACNT	Initialized	Initialized	Retained
SMSYSCSRC	Initialized	Initialized	Retained
SMSYSCERR	Initialized	Initialized	Retained

Register Abbreviation	Power-on Reset	System Reset	A4S Area Reset
SMSYSCTIME	Initialized	Initialized	Retained
SMSYSCCNT	Initialized	Initialized	Retained

For details, refer to section 1-D Overview of reset.

Master ID Register

The master ID register indicates SrcID of the master CPU on the SHwy bus.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MPSRC[7:0]								—	—	—	—	—	—	—	—
Initial value:	*	*	*	*	*	*	*	*	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 24	MPSRC7 to MPSRC0	- (Refer to Descriptions)	R	Master CPU ID Indicate the SrcID of the master CPU on the SHwy bus. The initial value depends on and varies with boot mode. H'01: AP realtime CPU H'40: AP system CPU
23 to 0	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.

Master Access Control Register

The master access control register controls the forced acquisition function of the master CPU. Setting of this register is applied to all bus semaphores. Only the master CPU can write this register.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SMF GETC	NOSM	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31	SMFGETC	0	R/W	Forced Semaphore Acquisition Control by Master CPU 0: The master CPU cannot forcibly acquire semaphores. 1: The master CPU can forcibly acquire semaphores.
30	NOSM	0	R/W	Write Access Control by Master CPU when Semaphore Is not Acquired 0: The master CPU cannot be write-accessed when no semaphore is acquired. 1: The master CPU can be write-accessed even if no semaphore is acquired.
29 to 0	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.

(Bit assignment is common to XXXX (GPIO, DBG, CMT2, CPGA, and SYSC).)

XXXX Semaphore Acquisition ID Register

The XXXX semaphore acquisition ID register controls semaphore acquisition and displays the semaphore acquisition state.

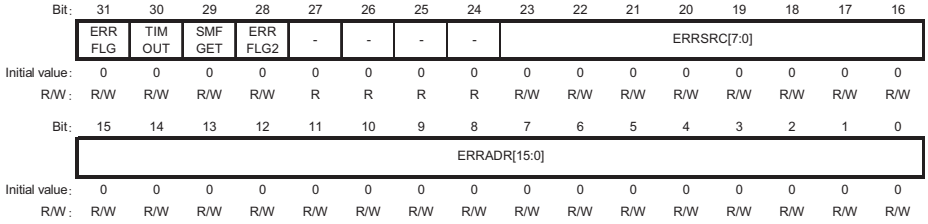
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SMSRC[7:0]								—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SMGET
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	W

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 24	SMSRC7 to SMSRC0	H'00	R	Indicate the SrcID of the SHwy bus of the CPU that acquired the semaphore. H'00: Open state H'01: AP realtime CPU H'40: AP system CPU H'64: ACMFI
23 to 1	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	SMGET	0	W	Acquires and opens semaphores. If SMSRC7 to SMSRC0 are H'00, semaphores can be acquired. If they are not H'00, semaphores cannot be acquired. These bits are automatically cleared to 0 after write. 1: Semaphore acquisition (this bit is read as 0) 0: Semaphore open

XXXX Semaphore Error Register

The XXXX semaphore error register indicates the information displayed if an access error occurs when no semaphore is acquired.



Bit	Bit Name	Initial Value	R/W	Descriptions
31	ERRFLG	0	R/W	Indicates whether an access error occurred when no semaphore is acquired. This bit is cleared to 0 when written to 0. 1: An access error occurred. 0: No access error occurred.
30	TIMOUT	0	R/W	Indicates whether the semaphore was forcibly opened due to timeout. This bit is cleared to 0 when written to 0. 1: The semaphore was forcibly opened. 0: The semaphore was not forcibly opened.
29	SMFGET	0	R/W	Indicates whether the master CPU forcibly acquired semaphores. This bit is cleared to 0 when written to 0. 1: The master CPU forcibly acquired semaphores. 0: The master CPU did not forcibly acquire semaphores.
28	ERRFLG2	0	R/W	Indicates whether an access occurred when semaphore is opened. This bit is cleared to 0 when written to 0. 1: An access occurred when semaphore is opened. 0: No access occurred when semaphore is opened.
27 to 24	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.

23 to 16	ERRSRC7 to ERRSRC0	H'00	R/W	Indicate the SrcID of SHwy bus of the CPU where the access error occurred when no semaphore is acquired. These bits are retained while ERRFLG or ERRFLG2 is 1. These bits are cleared to 0 when written to 0. H'01: AP realtime CPU H'40: AP system CPU H'64: ACMFI
15 to 0	ERRADR15 to ERRADR0	H'0000	R/W	Indicate the lower 16 bits of the address of the CPU where the access error occurred when no semaphore is acquired attempted to access. These bits are retained while ERRFLG or ERRFLG2 is 1. These bits are cleared to 0 when written to 0.

XXXX Semaphore Timeout Setting Register

The XXXX semaphore timeout setting register controls semaphore acquisition timeout and sets time.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TORN	TIMEOUT[30:16]														
Initial value:	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TIMEOUT[15:0]															
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31	TOEN	0	R/W	Enables or disables semaphore acquisition timeout setting. 1: Disables semaphore acquisition timeout setting. 0: Enables semaphore acquisition timeout setting.
30 to 0	TIMEOUT30 to TIMEOUT0	H'7FFF_FFFF	R/W	Set semaphore acquisition timeout time. A unit of semaphore acquisition timeout time is the number of CPϕ cycles.

XXXX Semaphore Timeout Counter

The XXXX semaphore timeout counter displays the time that lasts to semaphore acquisition timeout.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	TIMEOUTCOUNT[30:16]														
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TIMEOUTCOUNT[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
31 to 0	TIMEOUTCOUNT30 to TIMEOUTCOUNT0	H'0000_0000	R	Down counter that indicates the time that lasts to semaphore acquisition timeout. A unit of semaphore acquisition timeout is the number of CPϕ cycles.

1-F.4.2.2 Semaphore Control Range

The registers shown by module in the following address range are subject to semaphore control:

module	Semaphore Control Target Addresses
GPIO	H'E6050000 to H'E605FFFF
DBG	H'E6108000 to H'E610FFFF
CMT2	H'E6134000 to H'E6137FFF
CPG	H'E6158000 to H'E615FFFF
SYSC	H'E6188000 to H'E618FFFF

1-F.4.2.3 Semaphore acquisition and open procedure

When the master CPU forcibly acquires no semaphore

Acquisition:

1. Check if the semaphore is open according to the SMSRC bits of the semaphore acquisition ID register.
2. Write 1 to the SMGET bit of the semaphore acquisition ID register.
3. Check if the SMSRC bits of the semaphore acquisition ID register indicate the own SrcID. If the SMSRC bits indicate the own SrcID, acquire the semaphore. If the SMSRC bits do not indicate the own SrcID, return to Step 1.

Open:

1. Write 0 to the SMGET bit of the semaphore acquisition ID register.

When the master CPU forcibly acquires a semaphore

Acquisition:

1. Check if the semaphore is open according to the SMSRC bits of the semaphore acquisition ID register.
2. Write 1 to the SMGET bit of the semaphore acquisition ID register.
3. Check if the SMSRC bits of the semaphore acquisition ID register indicate the own SrcID. If the SMSRC bits indicate the own SrcID, acquire the semaphore. If the SMSRC bits do not indicate the SrcID, return to Step 1.
4. Clear the error in the semaphore error register in advance.

Open:

1. Check if the own write error exists in the semaphore error register (the master CPU does not require this check).
2. If the own write error exists in the semaphore error register, reacquire the semaphore and open it again from the error location. If the error does not exist, write 0 to the SMGET bit of the semaphore acquisition ID register.

About master processor and semaphore acquisition availability

- Master = ACMFI

		CPUs That Will Acquire Semaphores from Now		
		ACMFI	**APL-SYS**	**APL-RT**
CPUs that Have Already Acquired Semaphores	Open	Yes	Yes	Yes
	ACMFI	—	No	No
	APL-SYS	Yes	—	No
	APL-RT	Yes	No	—

- Master = APL-SYS

		CPUs That Will Acquire Semaphores from Now		
		ACMFI	**APL-SYS**	**APL-RT**
CPUs that Have Already Acquired Semaphores	Open	Yes	Yes	Yes
	ACMFI	—	Yes	No
	APL-SYS	No	—	No
	APL-RT	No	Yes	—

- Master = APL-RT

		CPUs That Will Acquire Semaphores from Now		
		ACMFI	**APL-SYS**	**APL-RT**
CPUs that Have Already Acquired Semaphores	Open	Yes	Yes	Yes
	ACMFI	—	No	Yes
	APL-SYS	No	—	Yes
	APL-RT	No	No	—

About master processor and common resource access availability

- Master = ACMFI

		CPUs That Will Access Common Resources		
		ACMFI	**APL-SYS**	**APL-RT**
CPUs that Have Already Acquired Semaphores	Open	Readable/writable	Readable/writable	Readable/writable
	ACMFI	Readable/writable	Readable only	Readable only
	APL-SYS	Readable/writable	Readable/writable	Readable only
	APL-RT	Readable/writable	Readable only	Readable/writable

- Master = APL-SYS

		CPUs That Will Access Common Resources		
		ACMFI	**APL-SYS**	**APL-RT**
CPUs that Have Already Acquired Semaphores	Open	Readable/writable	Readable/writable	Readable/writable
	ACMFI	Readable/writable	Readable/writable	Readable only
	APL-SYS	Readable only	Readable/writable	Readable only
	APL-RT	Readable only	Readable/writable	Readable/writable

- Master = APL-RT

		CPUs That Will Access Common Resources		
		ACMFI	**APL-SYS**	**APL-RT**
CPUs that Have Already Acquired Semaphores	Open	Readable/writable	Readable/writable	Readable/writable
	ACMFI	Readable/writable	Readable only	Readable/writable
	APL-SYS	Readable only	Readable/writable	Readable/writable
	APL-RT	Readable only	Readable only	Readable/writable

When not used, bus semaphores can be accessed in the same way when there is no bus semaphore. The master processor also has the access function that ignores semaphore acquisition and the forced semaphore acquisition function. These functions are provided mainly to prevent deadlocks resulting from semaphores.

Due to these specifications, a hardware function is unavailable that fully blocks semaphore access when no semaphore is acquired. For this reason, it is important to honor the following software agreement between CPUs: When exclusive control is performed, semaphores are accessed after they are acquired and they are not accessed if they are not acquired.

1-F.4.2.4 About the timeout counter register

The timeout counter register sets a semaphore acquisition timeout time. When a semaphore is acquired, the values in this semaphore timeout setting register are set in the down counter in the semaphore controller. When the down counter becomes 0, the semaphore is forcibly opened. The timeout counter register indicates the current values of the down counter. The current values of the down counter are reset to the values set in the TIMEOUT30 to TIMEOUT0 bits of the semaphore timeout setting register:

- When a semaphore is acquired
- When the semaphore timeout setting register is write-accessed

When set 0 to the TIMEOUT30 to TIMEOUT0 bits, the semaphore is forcibly opened. It doesn't depend on the timeout counter operation.

1-F.5 Security Function

To prevent the entire system from being destroyed and altered by an incorrect program, install the access protection function in registers related to the system.

Name	Register Abbreviation	R/W	Initial Value	Address	Access Size (Bits)
RBAR protection setting register	GRDRBAR	R/W	H'0000 0000	H'E6001500	32
SBAR protection setting register	GRDSBAR	R/W	H'0000 0000	H'E6001504	32

Register States in Each Operating Mode

Register Abbreviation	Power-on Reset	System Reset	A4S Area Reset
GRDRBAR	Initialized	Initialized	Retained
GRDSBAR	Initialized	Initialized	Retained

For details, refer to section 1-D Overview of reset.

1-F.5.1 SBAR Protection Setting Register

The 32-bit SBAR protection setting register protects SBAR register write protection.

This register has the register write protection function that authorizes only CPUs with access permission to change the settings.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	CPUTYPE[1:0]		REGWP	—	—	—	—	—	—	—	WPRSP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BBWP	APWP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 27	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
26, 25	CPUTYPE [1:0]	00	R	These bits indicate which CPUs are authorized to change the settings of this register. 00: All CPUs are authorized to change the settings. 01: Only AP-SH is authorized to change the settings. 10: Only AP-ARM is authorized to change the settings. 11: Only ACMFI is authorized to change the settings. To set the setting change authorization of this register, write 1 to the REGWP bit at the same time. The CPU that set this register is automatically set as the CPU authorized to change the settings. When B'0 is written to the REGWP bit, these bits are cleared to B'00. This clearing authorizes all CPUs to change the settings.

Bit	Bit Name	Initial Value	R/W	Descriptions
24	REGWP	0	R/W	Register Change Authorization Setting Bit This bit sets whether the CPU that set this register allows other CPUs to change the settings of this register. 0: Allows all CPUs to change the settings of this register. 1: Allows only the CPU that set this register to change the settings of this register. After 1 is written, this bit is automatically cleared to 0. When this bit is set to 1, the type of CPU that set this register is set in CPUTYPE. After changing the values of this register, read this register and check via software to see if this bit is cleared to 0 and the set CPU type is reflected in CPUTYPE. Then start memory area access. Write from the CPU, which is indicated by CPUTYPE and not authorized to change the settings, is disabled.
23 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	WP_RSP	0	R/W	This bit sets whether to respond to the error when the write-protected area is write-accessed. 0: Responds to the error. 1: Does not respond to the error. Write from the CPU, which is indicated by CPUTYPE and not authorized to change the settings, is disabled.
15 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	BB_WP	0	R/W	BB Resource* Write Authorization Setting Bit 0: Write to SBAR is authorized. 1: Write to SBAR is not authorized. Write from the CPU, which is indicated by CPUTYPE and not authorized to change the settings, is disabled.
0	AP_WP	0	R/W	AP Resource* Write Authorization Setting Bit 0: Write to SBAR is authorized. 1: Write to SBAR is not authorized. Write from the CPU, which is indicated by CPUTYPE and not authorized to change the settings, is disabled.

Note: * AP resources: AP-SH, AP-ARM, AP-DMAC (RT-DMAC, SYS-DMAC), AP-JTAG, and others (image IP, MBXL)
BB resources: ACMFI

1-F.5.2 RBAR Protection Setting Register

The contents of the RBAR protection setting register are the same as those of the SBAR protection setting register.

Section 2 AP-System Core

2.1 Overview

The AP-System core is a core block equipped with ARM Cortex-A8. For details on the functions of Cortex-A8, see its respective Technical Reference Manual.

Table2.1 Feature of the AP-System Core Block

Item	Features
CPU(*1)	• ARM Cortex-A8：r3p1 • ARM architecture v7-A • TrustZone Security Extensions • Configurations Level 1 Instruction cache: 32k bytes (8k bytes x 4 ways) Level 1 Data cache : 32k bytes (8k bytes x 4 ways) Level 2 cache: 256k bytes (32k bytes x 8 ways) • MMU support • NEON and VFPv3 support • Operating clock CPU core : 800MHz(Zϕ), AXI bus : 400MHz(ZXϕ) • Low power mode Power shutdown mode Core standby mode(*2) Power is shut down except for the level 2 cache. Because level 2 cache information remains, boot can be performed faster than usual reset. Sleep mode • Trace macro (ETM) ETM architecture: Ver.3.3 External trace data output data width: 8 bits External trace clock output (TRACECLK): Divide ATCLK by 2. (Data is output at edges of a clock.)
Bus Bridge	• A8S bus bridge connects AXI bus and SHwy bus. • Address translation is performed to the physical address start space (Max: 512 kbytes) according to the settings of the SBAR register in the SYSC. • Commutative SHwy access priority (register setting) • Supports N:1 as the clock ratio of the AXI bus clock (ZXϕ) and SHwy (ZSϕ) (See the clock ratio restrictions in the chapter of CPG)
Debug	• Supports the cross break between AP-System core and AP-Realtime core.

*1 For details, see related ARM manuals.

CPU : Cortex™-A8 Revision r3p1 Technical Reference Manual

*2 “Dormant Mode” in ARM documents.

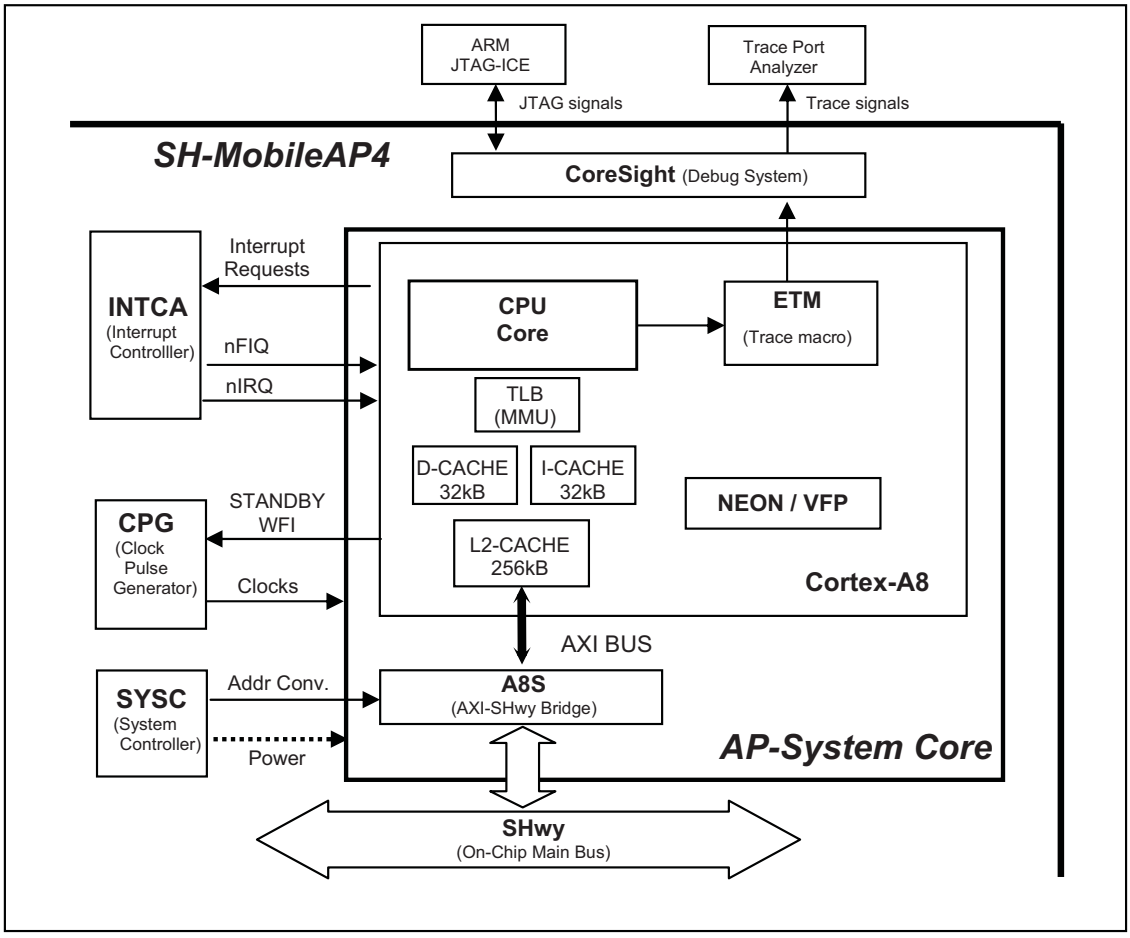


Figure2.1 AP-System Core Block Diagram

2.2 Control Registers

Table 2.2 shows the control register configuration related to the AP-System core. Table 2.3 shows the register state in each operating mode. These AP-System core registers are initialized by A4S area reset because of they are not on A3SM area on which AP-System core is but on A4S area.

Table2.2 Register Configuration

Register Name	Register Abbreviation	R/W	Address	Access Size
Priority register	APARMPRI	R/W	H'E6F1 0000	32
Address translation area register	APARMBAREA	R/W	H'E6F1 0020	32

Table2.3 Register State in Operating Mode

Register Abbreviation	Power-On Reset	AP System Reset	A3SM Area Reset	A4S Area Reset	SYS Domain Software Reset	AP-System Core Software Reset	Core Standby/ Sleep*
APARMPRI	Initialized	Initialized	Retained	Initialized	Initialized	Retained	Retained
APARMBAREA	Initialized	Initialized	Retained	Initialized	Initialized	Retained	Retained

* See “2.7 Power-Down Mechanism”

2.2.1 Priority Register (APARMPRI)

APARMPRI controls priority values when the APL-ARM block accesses SHwy. The value of the PRI bits is output as a priority value. For details on SHwy including how to use the PRI signal, see chapter 1-F, Bus Function.

Note: The setting of this register takes effect after a few cycles. It depends on the bus clock ratio of SHwy and HPB.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	PRI[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R	Reserved This bit is always read as 0. The write value should always be 0.
3 to 0	PRI[3:0]	1000	R/W	Priority value This bit is a priority value for access to SHwy.

2.2.2 Address Translation Area Register (APARMBAREA)

The bus bridge circuit has the physical address translation function. This function is controlled by the SYSC boot address register (SBAR). Access to the start space (maximum 512k bytes) including the reset address is translated into access to the physical address space indicated with the SBAR[31:12] bit. For details on the SBAR bits, see the SYSC manual.

The APARMBAREA register specifies an address area to be translated. Table 2.4 shows the details of the address translation using the APARMBAREA register and the SBAR[31:12] bit.

Note: When changing registers related to the address translation function, be careful not to switch an area that is being accessed from a translation target to an out-of-translation target or from an out-of-translation target to a translation target. There is no problem with changes for increasing the translation target area by changing the APARMBAREA register by programming the translation target area.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	BAREA[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	—	All 0	R	Reserved This bit is always read as 0. The write value should always be 0.
2 to 0	BAREA[2:0]	100	R/W	Area size of the address translation target (from address 0) 000：4k bytes 001：8k bytes 010：16k bytes 011：32k bytes 100：64k bytes 101：128k bytes 110：256k bytes 111：512k bytes

Table2.4 Address Translation with the BAREA Bits and SBAR Register

(ADDR[31:0] are physical addresses before translation)

BAREA[2:0]	Translation target area	Physical address after translation
B'000	H'0000 0000～H'0000 0FFF	{SBAR[31:12],ADDR[11:0]}
B'001	H'0000 0000～H'0000 1FFF	{SBAR[31:13],ADDR[12:0]}
B'010	H'0000 0000～H'0000 3FFF	{SBAR[31:14],ADDR[13:0]}
B'011	H'0000 0000～H'0000 7FFF	{SBAR[31:15],ADDR[14:0]}
B'100	H'0000 0000～H'0000 FFFF	{SBAR[31:16],ADDR[15:0]}
B'101	H'0000 0000～H'0001 FFFF	{SBAR[31:17],ADDR[16:0]}
B'110	H'0000 0000～H'0003 FFFF	{SBAR[31:18],ADDR[17:0]}
B'111	H'0000 0000～H'0007 FFFF	{SBAR[31:19],ADDR[18:0]}

2.3 AXI-SHwy Bridge (A8S)

A8S is the bus bridge between AXI bus from Cortex-A8 and SHwy that is the on-chip main bus. The AXI buses and SHwy can operate at different frequencies. Only the frequencies of an integral ratio N that is set with the FRQCRB and FRQCRC registers of the CPG are supported. The AXI buses must be set to a clock frequency that is the same as or faster than that of SHwy. Priority values for access to SHwy can be changed with the APARMPRI register.

The notes and restrictions of the load/store function of the Cortex-A8 are described below:

[Notes and restrictions of the load/store function of Cortex-A8]

- Exclusive load/store instruction

  Even if using the LDREX, STREX, or CLREX instruction, it is not reflected on SHwy. Thus, these instructions can be used only for the exclusion between threads on Cortex-A8. These instructions cannot be used for the exclusive processing between Cortex-A8 and other bus masters (AP-Realtime Core).

- Load multiple instruction (LDM)

  Use the LDM instruction only for memory devices (external memories via BSC or SBSC, or internal memories such as MFRAM, MERAM, and XYRAM).

  When the start and end addresses are not on an 8 bytes boundary, read access for an area not to be accessed occurs. Specifically, in the case that (8m + 4) bytes are read from address 8n (n, m: integer), and the case that 8m bytes are read from address (8n + 4), 4 bytes may be read from address (8n + 8m + 4). If this instruction is used for access to control registers whose state or contents, such as FIFO, is changed by read operation, unexpected operation may occur. This problem does not apply to the Store Multiple (STM) instruction. Thus, writing is not performed to an area not to be accessed.

  For details of the cache control and the memory attribute setting, see 2.5.1.

2.4 Internal Memory

The Cortex-A8 core is equipped with the instruction cache (32k bytes), data cache (32k bytes), and level 2 cache (256k bytes). The TCM is not mounted. In core standby mode that is one of the power-down mechanisms, power is supplied to the SRAM of level 2 cache. For details, see section 2.7.2, Core Standby Mode.

2.5 Notes for Settings

2.5.1 Memory Attribute

The followings are restrictions on the memory attributes in the case of the memory write access. If you ignore these restrictions, the write access will cause unexpected results. There is not restriction in case of the read access.

MERAM and External memories accessed via SBSC

No restriction

SMFRAM, ACMFRAM

The memory attribute must be the below.

- Strongly-ordered(default) ({TEX,C,B}=00000)(*)
- Shareable/Non-Shareable Device({TEX,C,B}=00001 or 01000)(*)
- L2 Read/Write-Back Write-Allocate Cacheable({TEX,C,B}=101xx)(*)

External memories accessed via BSC

The memory attribute must be the below.

- Strongly-ordered(default)({TEX,C,B}=00000)(*)
- Shareable/Non-Shareable Device({TEX,C,B}=00001 or 01000)(*)

(*) In case that “Memory Region Remap” is enabled in OS, the bit pattern of {TEX,C,B} is different.

2.5.2 Level 2 Cache Setting

- The latency of both L2 Data RAM and L2 Tag RAM has to be 3 cycles. The default value of “Tag RAM latency” bit of “c9, L2 Cache Auxiliary Control Register” is 2 cycles. Before you enable level 2 cache, “Tag RAM latency” bit must be set to 3cycles. The default value of “Data RAM latency” bit is 3 cycles.
- The default setting of “Way-Size” is 32k bytes and the default setting of “Associativity” is 8-Way. You can not change them.
- The followings are necessary to enable level 2 cache.
  - Enable level 1 cache with setting “C” bit of “c1, Control Register” to 1(ON).
  - Set “L2EN” bit of “c1, Auxiliary Control Register” to 1(ON).
    The default setting of “L2EN” bit of “c1, Auxiliary Control Register” is 1(ON). Usually, you do not have to set “L2EN” bit.

For detail of CP15 register, see Cortex-A8 manual.

2.6 Interface with the Interrupt Controller

The Cortex-A8 core supports interrupts by two interrupt signals (nFIQ and nIRQ). The AP-System core creates seven types of interrupt request signals listed in table 2.5 for INTCA.

Table2.5 Interrupt Sources Created by the AP-System Core

Interrupt Source	Interrupt generation module	Description
PMUIRQ	Cortex-A8	Interrupt request of the performance monitor
COMMTX	Cortex-A8	Transmission of the debugger communication channel
COMMRX	Cortex-A8	Reception of the debugger communication channel
CTIIRQ	Cortex-A8	CTI(Cross Trigger I/F) interrupt
DMAEXTERRIRQ	Cortex-A8	PLE error interrupt
DMAIRQ	Cortex-A8	Interrupt of PLE non-secure transmission complete
DMASIRQ	Cortex-A8	Interrupt of PLE secure transmission complete

2.7 Power-Down Mechanism

2.7.1 Overview

The AP-System core supports the following three power-down modes.

- Power shutdown mode
- Core standby mode (Power shutdown except for some SRAMs)
- Sleep mode (Clock stop)

In power shutdown mode, the power of the AP-System core is shut down. This mode is intended to be used at long-time interrupt wait, and achieves the reduction of power consumption including leakage current cut-off. The system boots up from the reset vector at its return from power shutdown mode. For detail of the power-down mode control, see chapter 13 “SYSC”.

Core standby mode is a power shutdown mode in a state where the power of some SRAMs in the Cortex-A8 core is maintained (the contents of them are maintained). Because the contents of SRAMs are maintained, boot return time is shorter than the power shutdown mode. In this mode, level 2 cache is retained and the application is expected to be executed in a cache hit state immediately after boot because the cache contents are maintained.

Sleep mode is a mode stopping only clocks. This mode does not perform power shutdown. Although the reduction of power consumption can be achieved as compared with a state where clocks are supplied, leakage current still exists. For details of sleep mode and core standby mode, see chapter 11 “CPG”.

note: MSTPAS(AP-System core module stop) bit in RESCNT register of SYSC is for control only A8S bridge clock and program execution of CPU. You can not use MSTPAS bit to cut off the power consumption because AP-System core clock is not stopped by the bit.

2.7.2 Core Standby Mode

Figure 2.2 shows a block diagram of continuous power supply in core standby mode. Power supply to the SRAMs of level2 cache is kept. The power of SRAMs used for the instruction cache, the data cache and branch prediction system is shut down.

The system boots up from the reset vector at its return from core standby mode. ACMFRAM in AP4 is recommended to be used as a boot memory to avoid the access to a low-speed extrinsic memory.

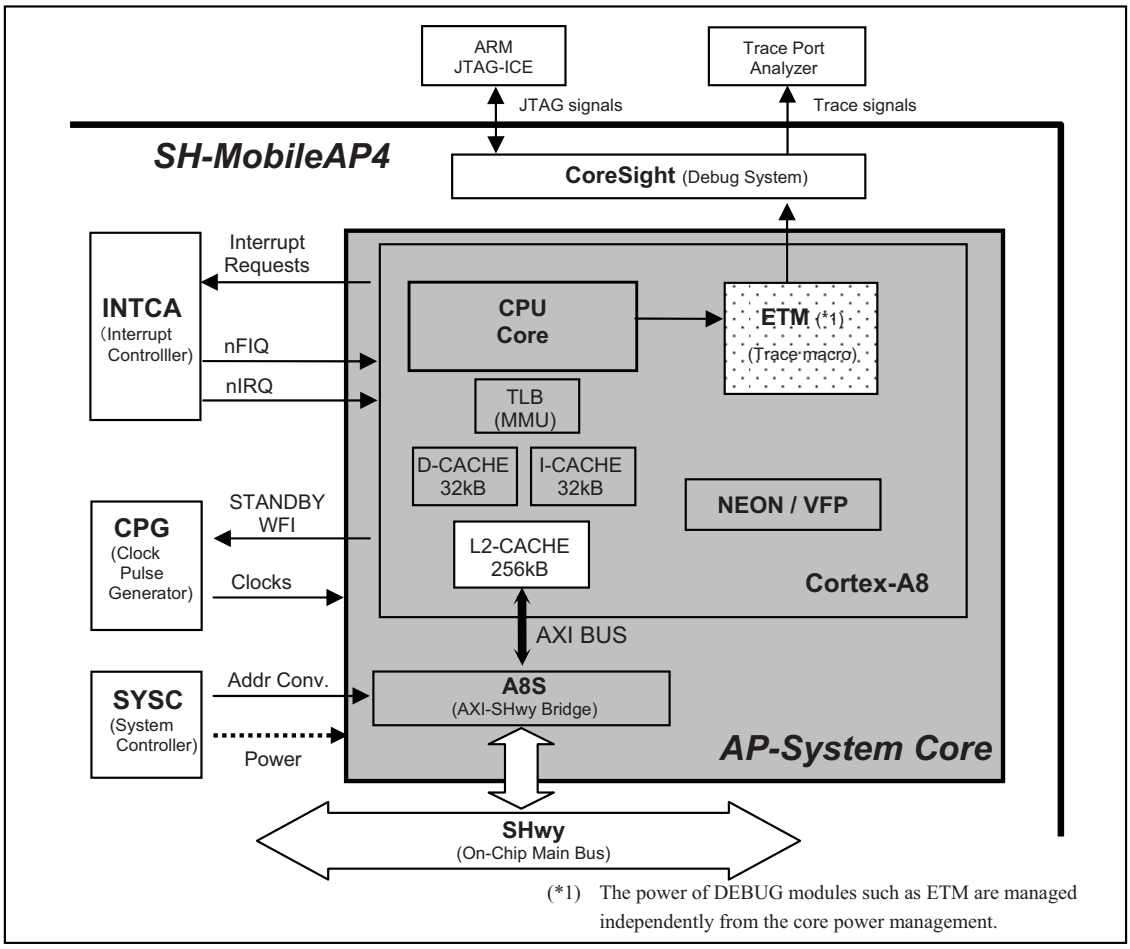


Figure2.2 Power Supply Parts in Core Standby Mode (white area)

2.8 APB Interface for DEBUG

Cortex-A8 has APB interface to access DEBUG modules register. You can access the interface via SHwy and CoreSignt block. Table2.6 shows the address of the APB interface.

Table2.6 Address of APB interface and Access Target

Address	Target
H'E6F8 E000～H'E6F8 EFFF	DEBUG Register
H'E6F8 F000～H'E6F8 FFFF	ETM Control Register
H'E6F9 0000～H'E6F9 0FFF	CTI Control Register

Section 3 AP-Realtime Core

3.1 Overview of the AP-Realtime Core

The AP-Realtime (AP-RT) core block is a RISC microprocessor equipped with a 32-kbyte instruction cache, a 32-kbyte operand cache, a 16-kbyte X/Y memory, and a 4-kbyte instruction memory (IL memory). The architecture of the core is SH4AL-DSP, which is 32-bit RISC type Super H architecture CPU (SH) with the digital signal processing (DSP) extended function.

Table 3.1 shows the features of the AP-RT core block.

For details on the SH4AL-DSP core, see SH4AL-DSP Software Manual and SH4AL-DSP Extended Function Software Manual.

The SH4AL-DSP core of the AP-RT core block supports the extended functions.

Table 3.1 Features of the AP-Realtime Core Block

Item	Features
CPU (SH4AL-DSP) (Extended function support)	• Renesas Technology original architecture • Upward compatible with SH-1, SH-2, and SH3-DSP at object code level • 32-bit internal data bus • General register file Sixteen 32-bit general registers (eight 32-bit shadow registers) Seven 32-bit control registers Four 32-bit system registers • RISC-type instruction set (upward compatible with SH series) Instruction length: 16-bit fixed length for improved code efficiency Load/store architecture Delayed branch instructions Conditional execution Instruction set based on C language • Superscalar architecture (providing simultaneous execution of two instructions) • Instruction execution time: Up to two instructions/cycle • Virtual address space: 4 Gbytes • Space identifier ASIDs: 8 bits, 256 virtual address spaces • Internal multiplier • Supports core standby mode • Eight-stage pipeline

Item	Features
DSP unit	• Mixture of 16-bit and 32-bit instructions • 32-bit or 40-bit internal data bus • Supports a multiplier, ALU, and barrel shifter 32-bit multiplier supporting 16 bits × 16 bits • Supports large DSP data register files Six 32-bit data registers Two 40-bit data registers • Supports the extended Harvard architecture for the DSP data bus Two data buses One instruction bus • Four parallel operations can be performed at the maximum. ALU, multiplication, and two load/store operations • Two addressing units to generate two simultaneous memory access addresses • Supports DSP data addressing modes Increment, and indexing (with or without modulo addressing) • Supports the zero-overhead repeat loop control • Supports conditional execution instructions • Supports user DSP mode and privileged DSP mode
Memory management unit (MMU)	• 256 address spaces (identified by an 8-bit ASID) of 4 Gbytes each • 32-bit physical address space • Single virtual memory mode and multiple virtual memory mode • Supports multiple page sizes: 1 kbyte, 4 kbytes, 8 kbytes, 64 kbytes, 256 kbytes, 1 Mbyte, 4 Mbytes, and 64 Mbytes • Four-entry full associative TLB for instructions • 64-entry full associative TLB for instructions and operands • Supports software-controlled replacement and random-counter replacement algorithm • TLB contents can be accessed directly by address mapping.

Item	Features
Cache memory	• Instruction cache (IC) 32-kbyte, 4-way set associative 32-byte block length • Operand cache (OC) 32-kbyte, 4-way set associative 32-byte block length Selectable write methods (copy-back/write-through)
X/Y memory	• Four independent read/write ports 8-, 16-, or 32-bit operand access from the CPU with virtual addresses Up to two 16-bit accesses from the DSP 8-, 16-, or 32-bit operand access from the CPU with physical addresses, and instruction fetch access from the CPU 8-, 16-, 32-, or 64-bit and 16- or 32-byte access through external requests • Total of 16 kbytes • Supports the memory protective mechanism dedicated to DSP access as well as to CPU access
IL memory	• Three independent read/write ports Instruction fetch access from the CPU with virtual addresses Instruction fetch access from the CPU with physical addresses and 8-, 16-, or 32-bit operand access from the CPU 8-, 16-, 32-, or 64-bit and 16- or 32-byte access through external requests • Total of 4 kbytes

3.2 AP-Realtime (SH) Core Block Diagram

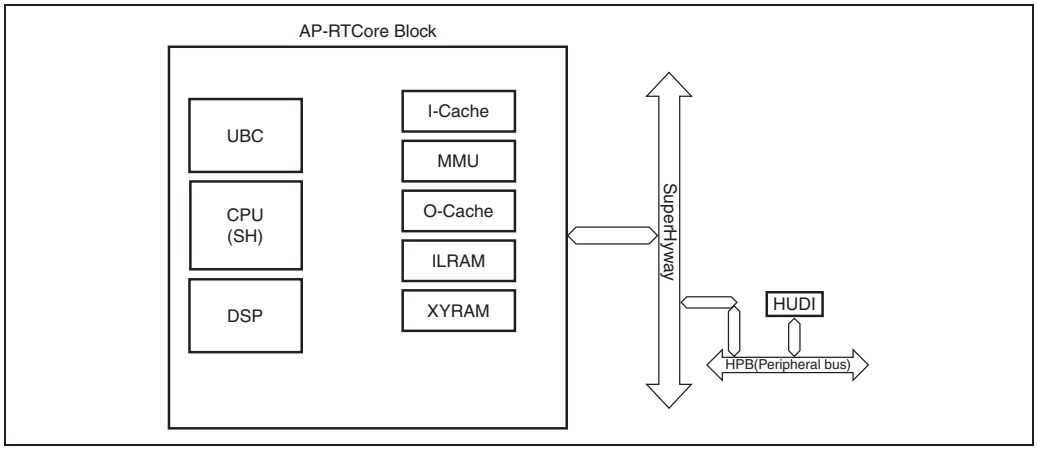


Figure 3.1 AP-Realtime (SH) Core Block Diagram

3.3 32-bit Address Extended Mode

The SH4AL-DSP core embedded in this LSI supports 32-bit address extended mode and the 32-bit boot function. For details on 32-bit address extended mode and the 32-bit boot function, see SH4AL-DSP Extended Function Software Manual.

After the AP-RT (SH) core is booted, the privileged space mapping buffer (PMB) is initialized by the hardware as described below. "SZ=B'11" indicates 512 Mbytes. Entry 0 specifies the mapping of the P1 area, and entry 1 specifies that of the P2 area. The treatment of the P1 area and P2 area is compatible with former products using the SH4AL-DSP core.

Table 3.2 PMB Configuration after Boot

Entry	VPN31 to VP24	PPN31 to PPN24	V	SZ21 and SZ0	C	UB	WT
0	B'1000 0000	B'0000 0000	1	B'11	1	0	1
1	B'1010 0000	B'0000 0000	1	B'11	0	0	0

[Legend]

VPN : Virtual page number

PPN : Physical page number

V : Validity bit (0: Invalid, 1: Valid)

SZ : Page size bits
(B'00: 16-Mbyte page, B'01: 64-Mbyte page, B'10: 128-Mbyte page, B'11: 512-Mbyte page)

C : Cacheability bit (0: Not cacheable, 1: Cacheable)

UB : Buffered write bit (0: Buffered write, 1: Unbuffered write)

WT : Write-through bit (0: Copy-back mode, 1: Write-through mode)

For this LSI, it is recommended to change the PMB configuration from the initial configuration described in Table 3.2 to the appropriate configuration for the system just after boot by the software running on the AP-Realtime core.

Table 3.3 Sample PMB Configuration

Entry	VPN31 to VP24	PPN31 to PPN24	V	SZ21 and SZ0	C	UB	WT
0	B'1000 0000	B'0100 0000	1	B'11	1	0	0
1	B'1010 0000	B'0000 0000	1	B'11	0	0	0

Table 3.3 shows a sample PMB configuration.

Entry 0 is a 512-Mbyte page. Accesses to virtual addresses from H'8000 0000 to H'9FFF FFFF are translated to physical addresses H'4000 0000 to H'5FFF FFFF. This is a setting for treating the SDRAM space as a cachable region. Note that accesses to virtual addresses from H’80000000 to H’9FFFFFFF are incompatible with the former P1 area, which was mapped to physical addresses from H'0000 0000 to H'1FFF FFFF.

Entry 1 is a 512-Mbyte page. With this configuration, accesses to the former P2 area (virtual addresses from H'A000 0000 to H'BFFF FFFF) are translated to physical addresses H'0000 0000 to H'1FFF FFFF with non-cachable attribute, that is, compatible mapping with 29-bit physical address mode.

The above PMB configuration is a sample. Please build the suitable configuration to your system combining page sizes and attributes.

3.4 Core Standby Mode

The SH4AL-DSP core embedded in this LSI supports the core standby mode in which power supply to the logical block in the core is shut off. Power to the memories (I-Cache, O-Cache, ILRAM, and XYRAM) in the core is not shut off to keep the contents of them. To enter the core standby mode, issue the SLEEP instruction in a state where the CPU core standby bit (CSTBY) of the CPGA RealTime Standby Control Register (RTSTBCR) is set. The core exits from the core standby mode by usual interrupts. At this time, registers in the core are initialized because the logical block of the core is reset. Save the contents of the registers into the memory before entering the core standby mode and restore the register values after exit in order to return the core to the state before the core standby mode. The IL memory is recommended as the save area of register values. In addition, the IL memory can be the place locating the routines for entering and exiting the core standby mode.

Section 4 IPMMU

This LSI has three IPMMU modules. Each IPMMU module provides the translation function that translates virtual addresses into physical addresses (= SHwy addresses) to respective SHwy initiator modules. With this function, initiator modules (for ICB/LMB, IP accessing SHwy via ICB/LMB) can access memory with virtual addresses.

4.1 Overview of IPMMUs

4.1.1 Features

- One IPMMU module exists for each SHwy initiator (total of three IPMMU modules).
  - IPMMUI: For ICB/LMB
  - IPMMUR: For RT-DMAC1
  - IPMMUR2: For RT-DMAC2
- Provides the MMU function compatible with ARMv6 to the first 2 Gbytes of the virtual address space (H'0000 0000 to H'7FFF FFFF).
  - Each of IPMMUR and IPMMUR2 has a 64-entry TLB.
  - IPMMUI has a 96-entry TLB.
  - Hardware page table walk function
  - Treats access rights as privileges.
  - Protects access rights in three levels: read/write approved, only read approved, access disapproved.
  - Does not support protection with domains.
- Provides the PMB (privileged space mapping buffer) function compatible with SH4AL-DSP to the latter 1 Gbyte of the virtual address space (H'8000 0000 to H'BFFF FFFF).
  - Includes a 16-entry PMB.

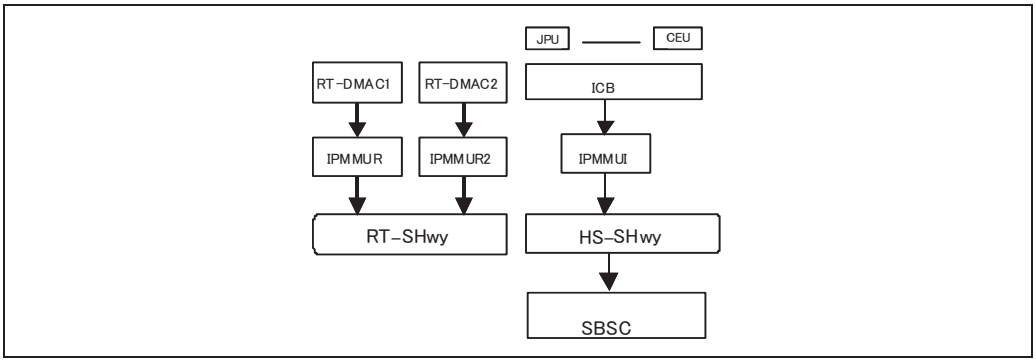


Figure 4.1 Relationship between IPMMUs and Other Modules

4.1.2 Address Space

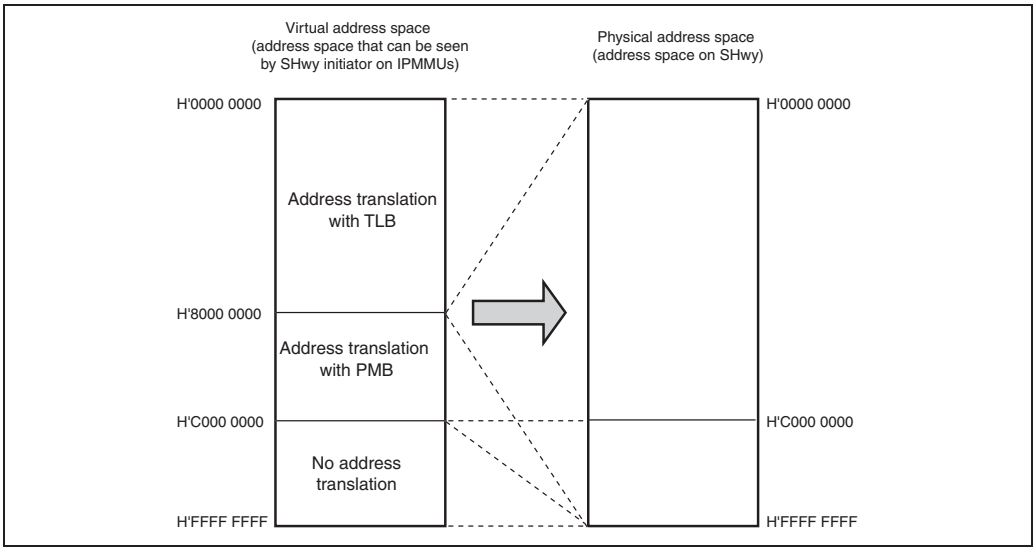


Figure 4.2 Relationship between the Address Spaces

4.2 Register Description

Table 4.1 shows the register configuration and memory configuration of IPMMUs. Table 4.2 shows the register state in each processing mode.

Table 4.1 Register Configuration and Memory Configuration

Register Name	Register Abbreviation	R/W	Address *1	Access Size
IPMMU control register 1	IMCTR1	R/W	H'xxxx x000	32
IPMMU control register 2	IMCTR2	R/W	H'xxxx x004	32
IPMMU status register	IMSTR	R/W	H'xxxx x008	32
IPMMU exception address register	IMEAR	R/W	H'xxxx x00C	32
IPMMU ASID register	IMASID	R/W	H'xxxx x010	32
IPMMU translation table base register	IMTTBR	R/W	H'xxxx x014	32
IPMMU translation table base control register	IMTTBCR	R/W	H'xxxx x018	32
IPMMU DMAC channel enable control register *2	IMDCEN	R/W	H'xxxx x020	32
IPMMU PMB address array 0 to IPMMU PMB address array 15	IMPMBA0 to IMPMBA15	R/W	H'xxxx x080 to H'xxxx x0BC	32
IPMMU PMB data array 0 to IPMMU PMB data array 15	IMPMBD0 to IMPMBD15	R/W	H'xxxx x0C0 to H'xxxx x0FC	32

Note: *1 The "xxxx x" parts in the Address column are as follows according to IPMMUs:
IPMMUI: FE951
IPMMUR: FFC30
IPMMUR2:FFC40
*2 IMDCEN exist only on IPMMUR and IPMMUR2

Table 4.2 Register State in Each Processing Mode

Register Abbreviation	Reset [*1]	Module Standby
IMCTR1	Initialized	Retained
IMCTR2	Initialized	Retained
IMSTR	Initialized	Retained
IMEAR	Initialized	Retained
IMASID	Initialized	Retained
IMTTBR	Initialized	Retained
IMTTBCR	Initialized	Retained
IMDCEN [*2]	Initialized	Retained
IMPMBA0 to IMPMBA15	Initialized	Retained
IMPMBD0 to IMPMBD15	Initialized	Retained

Note: *1 Please refer to “1-D. Overview of Reset” for the reset condition.
In case of IPMMUI, these registers are initialized by ICB’s software reset.
*2 IMDCEN exist only on IPMMUR and IPMMUR2

4.2.1 IPMMU Control Register 1 (IMCTR1)

IMCTR1 controls the address translation function with the TLB of IPMMUs.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	-	INTEN	FLUSH	TLBEN
Initial value:	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	—	—	R	Reserved These bits are always read as 0. The write value should always be 0.
2	INTEN	0	R/W	Specifies whether to issue interrupt requests when an exception event occurs. Interrupt requests are reported to INTCS. 0: Interrupt requests are not issued. 1: Interrupt requests are issued.
1	FLUSH	0	W	When this bit is set to 1, all entries of TLB are disabled. This bit is always read as 0.
0	TLBEN	0	R/W	TLB Enable When this bit is 0, address translation is not performed to access to addresses H'0000 0000 to H'7FFF FFFF. Addresses are passed to SHwy without translation. 0: Address translation with TLB is disabled. 1: Address translation with TLB is enabled.

4.2.2 IPMMU Control Register 2 (IMCTR2)

IMCTR2 specifies the address translation function with the PMB of IPMMUs.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	PMBEN
Initial value:	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	—	R	Reserved These bits are always read as 0. The write value should always be 0.
0	PMBEN	0	R/W	PMB Enable When this bit is 0, address translation is not performed to access to addresses H'8000 0000 to H'BFFF FFFF. Addresses are passed to SHwy without translation. 0: Address translation with PMB is disabled. 1: Address translation with PMB is enabled.

4.2.3 IPMMU Status Register（IMSTR）

IMSTR records exception events that have occurred while IPMMUs are running.

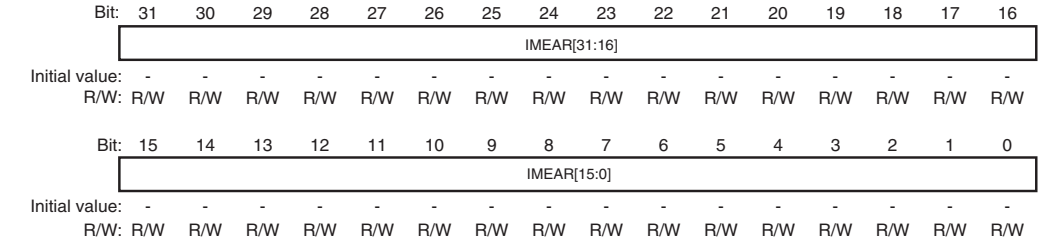
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	MHIT	-	ABORT	PF	TF
Initial value:	-	-	-	-	-	-	-	-	-	-	-	0	-	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	—	R	Reserved These bits are always read as 0. The write value should always be 0.
4	MHIT	0	R/W	This bit is automatically set to 1 by the hardware when either of the following exceptions occurs. TLB multiple hits PMB multiple hits PMB miss This bit can be cleared by writing 0 with software.
3	—	—	R	Reserved This bit is always read as 0. The write value should always be 0.
2	ABORT	0	R/W	This bit is automatically set to 1 by the hardware when an error response is returned for a hardware page table walk. This bit can be cleared by writing 0 with software.
1	PF	0	R/W	This bit is automatically set to 1 by the hardware when an access right violation occurs. This bit can be cleared by writing 0 with software.
0	TF	0	R/W	This bit is automatically set to 1 by the hardware when a translation fault occurs due to a hardware page table walk. This bit can be cleared by writing 0 with software.

4.2.4 IPMMU Exception Address Register (IMEAR)

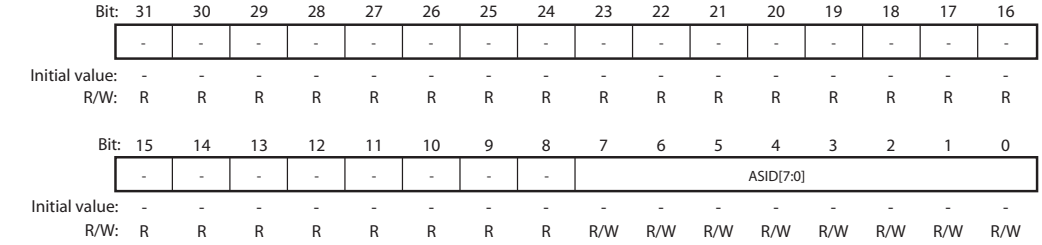
IMEAR records the virtual address causing the last exception event that has occurred while IPMMUs are running.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	EAR[31:0]	Undefined	R/W	These bits record the virtual address causing the last exception event that has occurred.

4.2.5 IPMMU ASID Register (IMASID)

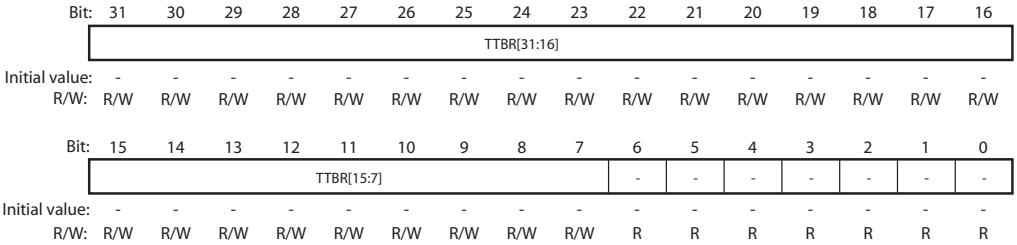
IMASID specifies ASID values used when IPMMUs perform address translation with TLB.



Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	—	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	ASID	Undefined	R/W	These bits specify ASID values used for address translation with TLB.

4.2.6 IPMMU Translation Table Base Register（IMTTBR）

IMTTBR specifies the physical address that is the base of the first level page table seen by IPMMUs.



Bit	Bit Name	Initial Value	R/W	Description
31 to 7	TTBR	Undefined	R/W	These bits specify the physical address that is the base of the first level page table. When TTBCR2 to TTBCR0 = B'001, TTBR31 to TTBR13 are used. When TTBCR2 to TTBCR0 = B'010, TTBR31 to TTBR12 are used. When TTBCR2 to TTBCR0 = B'011, TTBR31 to TTBR11 are used. When TTBCR2 to TTBCR0 = B'100, TTBR31 to TTBR10 are used. When TTBCR2 to TTBCR0 = B'101, TTBR31 to TTBR9 are used. When TTBCR2 to TTBCR0 = B'110, TTBR31 to TTBR8 are used. When TTBCR2 to TTBCR0 = B'111, TTBR31 to TTBR7 are used.
6 to 0	—	—	R	Reserved These bits are always read as 0. The write value should always be 0.

4.2.7 IPMMU Translation Table Base Control Register（IMTTBCR）

IMTTBCR specifies the size of the first level page table seen by IPMMUs.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	-	TTBCR[2:0]		
Initial value:	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	—	—	R	Reserved These bits are always read as 0. The write value should always be 0.
2 to 0	TTBCR	B'001	R/W	These bits specify the size of the first level page table. B'000: Reserved (Do not set this value.) B'001: 8 kbytes (Address space is 2 Gbytes.) B'010: 4 kbytes (Address space is 1 Gbyte.) B'011: 2 kbytes (Address space is 512 Mbytes.) B'100: 1 kbyte (Address space is 256 Mbytes.) B'101: 512 bytes (Address space is 128 Mbytes.) B'110: 256 bytes (Address space is 64 Mbytes.) B'111: 128 bytes (Address space is 32 Mbytes.) Allocate the first level page table to the boundary of the above table sizes. For example, when TTBCR2 to TTBCR0 = B'001, allocate the first level page table to an 8-kbyte boundary.

4.2.8 IPMMU DMAC channel enable (IMDCEN)[*1]

IMDCEN specifies a validity of TLB address translation for each channel of RT-DMAC[*2].

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value :	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	CH5EN	CH4EN	CH3EN	CH2EN	CH1EN	CH0EN
Initial value :	–	–	–	–	–	–	–	–	–	–	1	1	1	1	1	1
R/W :	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 6	—	—	R	Reserved These bits are always read as 0. The write value should always be 0.
5	CH5EN	B’1	R/W	This bit specifies a validity of TLB address translation for RT-DMAC channel 5.
4	CH4EN	B’1	R/W	This bit specifies a validity of TLB address translation for RT-DMAC channel 4.
3	CH3EN	B’1	R/W	This bit specifies a validity of TLB address translation for RT-DMAC channel 3.
2	CH2EN	B’1	R/W	This bit specifies a validity of TLB address translation for RT-DMAC channel 2
1	CH1EN	B’1	R/W	This bit specifies a validity of TLB address translation for RT-DMAC channel 1
0	CH0EN	B'1	R/W	This bit specifies a validity of TLB address translation for RT-DMAC channel 0.

Note: *1 IMDCEN exist only on IPMMUR and IPMMUR2.

*2 In case of IPMMUR ,this shows RT-DMAC1. In case of IPMMUR2, this shows RT-DMAC2.

4.2.9 IPMMU PMB Address Array n (IMPMBAn)

IMPMBAn (n = 0 to15) specifies the virtual page number of the PMB of IPMMUs.

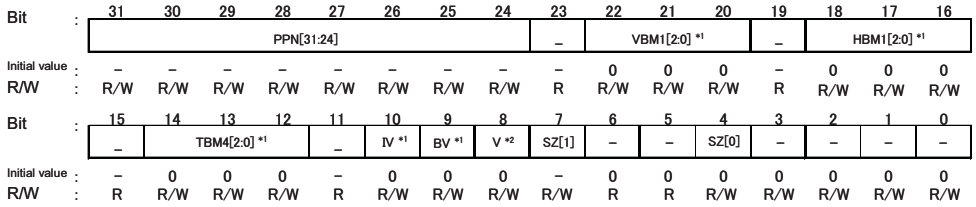
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VPN[31:24]								-	-	-	-	-	-	-	-
Initial value:	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	V	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	VPN[31:24]	Undefined	R/W	Virtual Page Number For 16-Mbyte page, VPN31 to VPN24 are used. For 64-Mbyte page, VPN31 to VPN26 are used. For 128-Mbyte page, VPN31 to VPN27 are used. For 512-Mbyte page, VPN31 to VPN29 are used.
23 to 9	—	All 0	R	Reserved Writing to this bit is ignored.
8	V	0	R/W	Validity Bit 0: Invalid 1: Valid
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

4.2.10 IPMMU PMB Data Array n (IMPMBDn)

IMPMBDn (n=0 to15) specifies the physical page number and page size of the PMB of IPMMUs.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	PPN[31:24]	Undefined	R/W	Physical Page Number For 16-Mbyte page, PPN31 to PPN24 are used. For 64-Mbyte page, PPN31 to PPN26 are used. For 128-Mbyte page, PPN31 to PPN27 are used. For 512-Mbyte page, PPN31 to PPN29 are used.
23	—	0	R	Reserved Writing to this bit is ignored.
22 to 20	VBM1[2:0] *1	All 0	R/W	Set (number of vertical bits to apply tile-linear translation) −1 in this bit.
19	—	0	R	Reserved Writing to this bit is ignored.
18 to 16	HBM1[2:0] *1	All 0	R/W	Set (number of horizontal bits to apply tile-linear translation) −1 in this bit.
15	—	0	R	Reserved Writing to this bit is ignored.
14 to 12	TBM4[2:0] *1	All 0	R/W	Set (number of horizontal bits not to apply tile-linear translation) −4 in this bit
11	—	0	R	Reserved Writing to this bit is ignored.

Bit	Bit Name	Initial Value	R/W	Description
10	IV *1	0	R/W	Line-Interleaved Address Translation Enable When this bit is set to 1, line-interleaved address conversion is performed with SB = HBM1 + 1 + TBM4 + 4. 0: Disabled 1: Enabled
9	BV *1	0	R/W	Tile-Linear Address Translation Enable When this bit is set to 1, line-interleaved address conversion is performed with SB = HBM1 + 1 + TBM4 + 4. 0: Disabled 1: Enabled
8	V *2	0	R/W	Validity Bit 0: Invalid 1: Valid
7	SZ[1]	Undefined	R/W	Page size [1] This bit specifies the page size together with bit 4. 00: 16-Mbyte page 01: 64-Mbyte page 10: 128-Mbyte page 11: 512-Mbyte page
6 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	SZ[0]	Undefined	R/W	Page size [0]
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Note: *1 These bits exists only on IPMMUI. These bits are reserved bits on IPMMUR and IPMMUR2. If BV or IV are set 1 in IPMMUI, the address which is after translation becomes the target of TLB/PMB translation again.

*2 In the case of IPMMUI, the address translation become valid by setting 1 to this bit. However IPPMBAn.V should be set 1'b1 in case of BV=1'b1 or IV=1'b1.

4.3 Functions of IPMMUs

4.3.1 Access with TLB

When the TLBEN bit in IMCTR1. is set to 1, address translation with TLB is applied to access to the address area from H'0000 0000 to H'7FFF FFFF.

Figure 4.3 shows the translation flow.

When a translation fault occurred due to a hardware page table walk, or an access right violation occurred, or a hardware page table walk failed (an error response was returned), an address to be accessed is translated to an address for which an error response is surely returned, and access is performed. Additionally, the corresponding exception event bit in IMSTR is set to 1.

When multiple TLB entries are hit, an address to be accessed is translated to an undefined address, and access is performed. Additionally, the MHIT bit in IMSTR is set to 1.

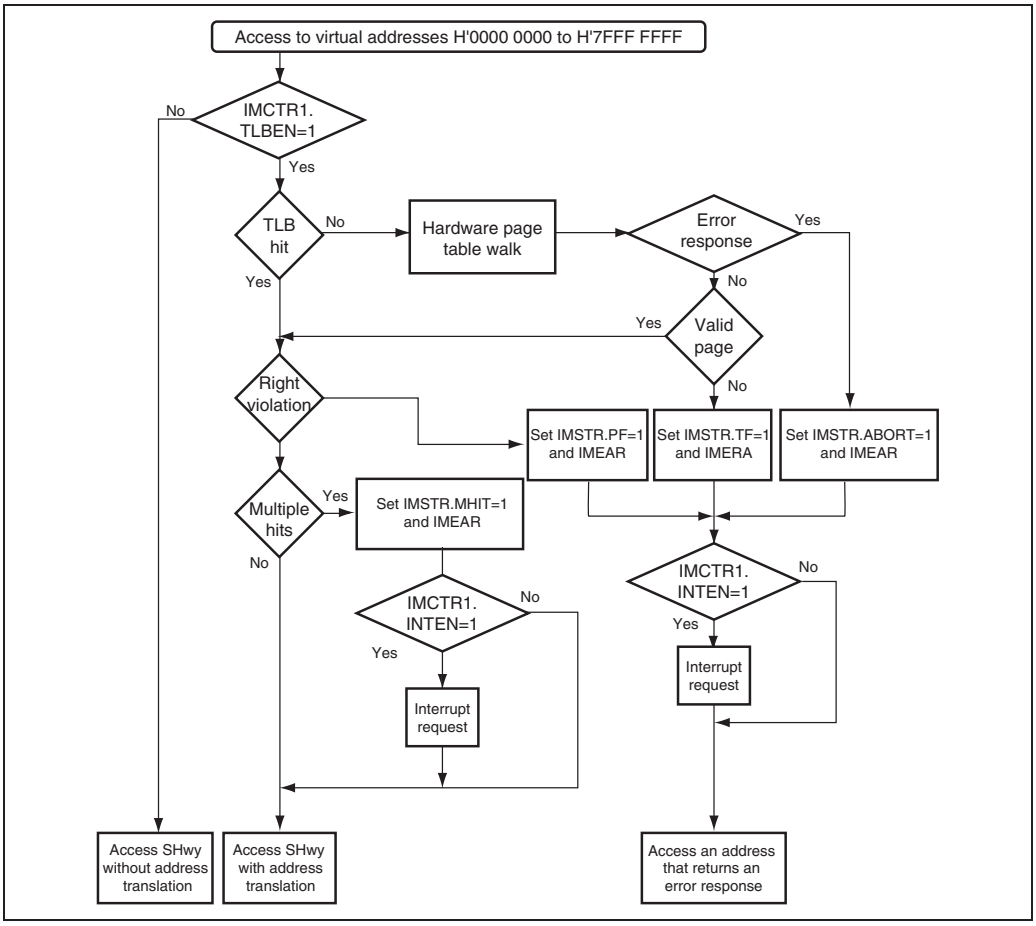


Figure 4.3 Translation Flow with TLB

4.3.2 Access with PMB

When the PMBEN bit in IMCTR2. is set to 1, address translation with PMB is applied to access to the address area from H'8000 0000 to H'BFFF FFFF.

Figure 4.4 shows the translation flow.

When no PMB entry is hit, an address to be accessed is translated to an address for which an error response is surely returned, and access is performed. Additionally, the MHIT bit in IMSTR is set to 1.

When multiple PMB entries are hit, an address to be accessed is translated to an undefined address, and access is performed. Additionally, the MHIT bit of IMSTR is set to 1.

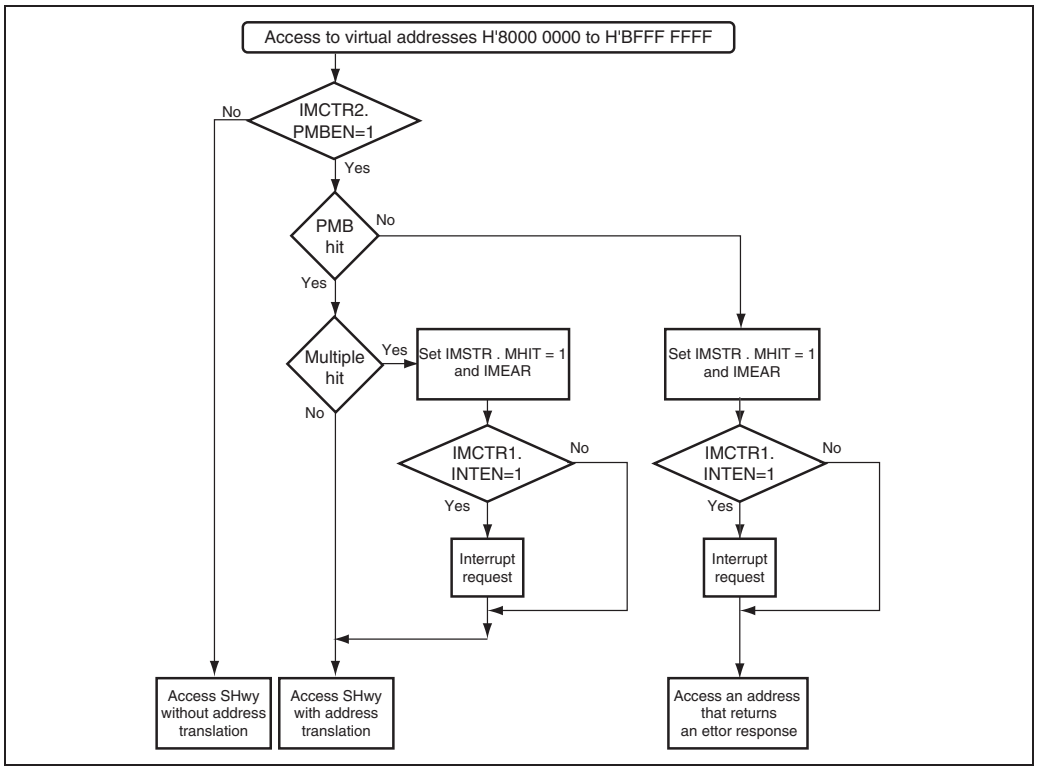


Figure 4.4 Translation Flow with PMB

4.3.3 Tile-Linear Address Translation (only on IPMMUI)

When the associated modules make tiled access to the virtual address space, it is to discrete addresses. This degrades the efficiency in accessing the external SDRAM. The PMB translation of IPMMU can reorder addresses to be accessed during virtual to physical translation so that they are accessed in a liner order instead of in a tiled order.

As an example, assume (image) data that is stride bytes wide is located in a virtual address space, and an initiator divides the space into tiles, each of them Blk_h bytes wide with Blk_v lines, to access it on a per tile basis.

If the lower address of the initiator is VADR[m:0], the access pattern in the physical address space can be rearranged linearly by generating the physical address PADR[m:0] as follows (m is 23, 25, 26, or 28 depending on the page size of the PMB):

PADR[m:TB+VB+HB] ←VADR[m:TB+VB+HB]

PADR[TB+VB+HB-1:TB+VB] ←VADR[TB+HB-1:TB]

PADR[TB+VB-1:TB] ←VADR[TB+HB+VB-1:TB+HB]

PADR[TB-1:0] ←VADR[TB-1:0]

Provided

TB = log2(Blk_h)

HB = log2(stride)TB,

VB = log2(Blk_v)

where stride, Blk_h, and Blk_v must be a 2's power

Since access by the VPU to the encoding or reference plane and access that the 2D-DMAC makes to use the rotation function are tile addressing, it is possible to improve the efficiency of access to the external SDRAM by accessing it via the virtual address space with tile-linear translation by this translation function.

Note that in order to access data correctly in the physical address space generated via the virtual address space by the tile-linear address translation function the access must be made via the virtual address space with the same translation setting.

Note also that accessing the virtual address space with tile-linear address translation from the modules that use linear addressing (all modules other than the VPU and 2D-DMAC if it is not set for rotation) leads to degrade of the efficiency of SDRAM access. If this access is needed, set the ICB function to block line transfer mode and horizontal division mode (the HDV bit in the MEnnSSARA register is 1) and use the horizontal division size along with Blk_h. In doing so, the number of block lines set for the ICB does not need to be equal to Blk_v and may be smaller, but the greater value improves the efficiency of SDRAM access.

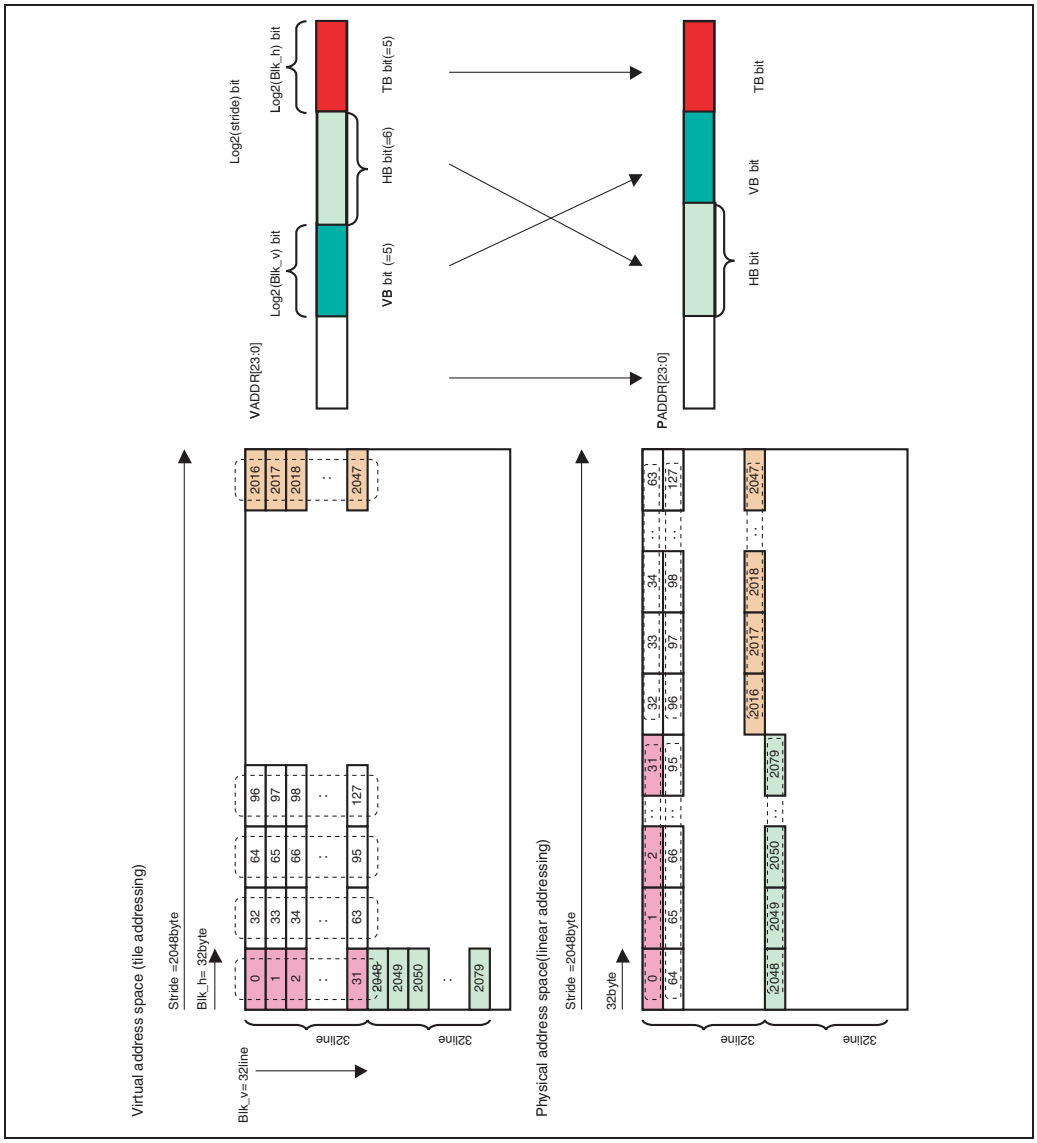


Figure 4.5 Virtual Address Space (Tile Addressing) and Physical Address Space (Linear Addressing)

4.3.4 Line-Interleaved Address Translation (Only on IPMMUI)

This function is intended mainly to handle CbCr planes for the YUV420 format. The CbCr planes in the YUV420 format are accessed in units of the same line width and the half number of lines compared to Y planes. Line-interleaved address translation allows them to be accessed in units of the half of the line width and the same number of lines compared to Y planes.

For example, if an image that is 1280 bytes wide is to be located to an area with stride = 2Kbytes, normally large areas in both Y/CbCr planes are wasted. However, data in the CbCr plane can be located to the area that was to be wasted in the Y plane by using the line-interleaved address translation function on the CbCr plane.

PADR[m:SB+1] ←VADR[m-1:SB]

PADR[SB] ←VADR[6]

PADR[SB-1] ←VADR[m]

PADR[SB-2:6] ←VADR[SB-1:7]

PADR[5:0] ←VADR[5:0]

Note that SB is log2(stride) and stride must be a 2's power. Note also that m is 23, 25, 26, or 28 depending on the page size of the PMB. If both line-interleaved address translation and tile-linear address translation are enabled simultaneously, tile-linear address translation is applied after line-interleaved address translation.

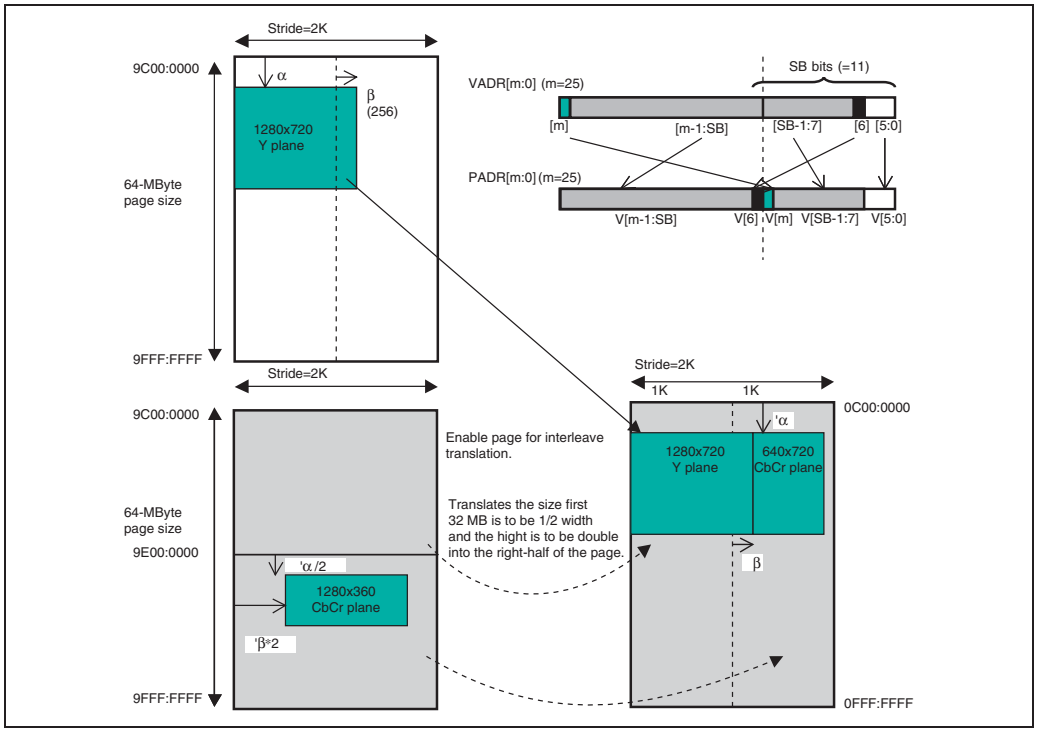


Figure 4.6 Line-Interleaved Address Translation

4.3.5 Access that is out of Address Translation

Access to the address area from H'C000 0000 to H'FFFF FFFF is out of address translation regardless of the settings of IPMMUs. SHwy is accessed with an original address without address translation.

4.4 How to Set IPMMUs

4.4.1 TLB Setting

- Set the ASID of a process that has a virtual address space to be shared by the IPMMUs in IMASID register.
- Set the base address of the first level page table of the above process in the IMTTBR register.
- In the following cases, write 1 to the FLUSH bit in IMCTR1 to disable the TLB in IPMMUs.
  - Virtual pages are deleted from the page table on the memory.
  - Another physical page is allocated to the existing virtual page.
  - The attribute of the existing page is changed.
- When a page that has not existed before is newly added, TLB does not need to be disabled (because a new page is not cached originally).

4.5 Usage Notes

The module stop of IPMMUs interworks with the module stop of modules connected to higher levels. Before setting values to the register or PMB of IPMMUs, cancel the module stop.

- IPMMUI is controlled by the module stop bit (MSTPCR0[7]) of ICB.
- IPMMUR is controlled by the module stop bit (MSTPCR0[21]) of RT-DMAC1.
- IPMMUR2 is controlled by the module stop bit (MSTPCR0[23]) of RT-DMAC2.

The power area of IPMMUs is the same as that of modules connected to higher levels.

- The power area of IPMMUI is A4R that is the same as ICB/LMB.
- The power area of IPMMUR is A4R that is the same as RT-DMAC1.
- The power area of IPMMUR2 is A4R that is the same as RT-DMAC2.

When you invalidate specific PMB entry n among the PMB entries which are validated once, please perform the following procedure.

(1) Write 1’b0 to IMPMBDn[8]. (In case of IPMMUI, write 2’b00 to IMPMBDn[10:9], too)
(2) Write 1’b1 to IMCRT1[1] to Flush TLB.

When you have performed (2), the invalidation of PMB's entry n is finished.

Section 5 Interrupt Controller (INTC)

The interrupt controller (INTC) determines the priority of interrupt sources and controls interrupt requests to the AP-Realtime core and AP-System core.

The INTC consists of the interrupt controller for the AP-System core (INTCA), the interrupt controller for the AP-Realtime core (INTCS), and the pin interrupt controller (PINTC); they respectively control interrupts to the AP-System core, those to the AP-Realtime core, and those from external pins. Some of the INTCA and INTCS registers set the priority of each interrupt, and interrupt requests are processed according to the user-set priority.

5.1 Features

(a) INTCA

- Fifteen levels of interrupt priority can be set
- IRQ pins interrupts can be set

  Thirty-two interrupts (IRQ pins interrupts) can be input through external pins, which can be used to request wakeup from power cutoff state. For each interrupt, detection of the rising or falling edge, detection of the level or edge, priority level, and enabling or disabling of the interrupt can be specified separately through the INTCA. interrupts can also be sent to the INTCS from the same IRQ pins and the conditions for those interrupts can be specified separately from the INTCA settings.
- IRQ pins interrupts and ARM-IRQ exception by INTCA peripheral modules interrupts can be set. IRQ pins interrupts and INTCA peripheral request are combined into one signal, and it is sent to IRQ port of AP-System core. Request from INTCA can be controlled by IRQ disable bit (7th bit) of program status register (CPSR) of AP-System core. The ARM-IRQ exception interrupt handler reads INTFLGA only once and determines the interrupt source. Reading from INTFLGA automatically sets the level of the accepted interrupt source to INTLVLA and automatically masks interrupts whose priority levels are equal to or lower than the INTLVLA value.
- INTCS peripheral interrupts can be sent to the AP-System core

  Interrupt signals from the peripheral modules assigned to the INTCS are combined into one signal, and it is sent to the INTCA as one peripheral interrupt. This interrupt signal can be masked independently from the mask settings for the AP-Realtime core. When the AP-System core accepts this interrupt, the AP-System core can read the AP-System core individual interrupt source register (INTEVTSA) in the INTCS during AP-System core interrupt handler processing and process the peripheral interrupt assigned to the INTCS. A setting can be made in the INTCA to mask all peripheral interrupts sent from the INTCS.

- User-mode interrupt disabling function
  Specifying an interrupt mask level in the user interrupt mask level register A (USERIMASKA) disables interrupts that are not higher in priority than the specified mask level in user mode.

(b) INTCS

- Fifteen levels of interrupt priority can be set
  By setting the interrupt priority registers, the priority levels of on-chip peripheral module interrupts can be selected from 15 levels for individual request sources.
- NMI interrupt can be set
  The NMI interrupt can be generated through the register settings in the CPG. The INTCS detects an interrupt request when the register value is changed from 1 to 0. The NMI interrupt is kept pending while the BL bit in SR is 1.

- IRQ pins interrupts can be set

  Thirty-two interrupts (IRQ pins interrupts) can be input through external pins, which can be used to request wakeup from power cutoff state. For each interrupt, detection of the rising or falling edge, detection of the level or edge, priority level, and enabling or disabling of the interrupt can be specified through the INTCS. Interrupts can also be sent to the INTCA from the same IRQ pins and the conditions for those interrupts can be specified separately from the INTCS settings.
- INTCA peripheral interrupts can be sent to the AP-Realtime core

  Interrupt signals from the peripheral modules assigned to the INTCA are combined into one signal, and it is sent to the INTCS as one peripheral interrupt. This interrupt signal can be masked independently from the mask settings for the AP-System core. When the AP-Realtime core accepts this interrupt, the AP-Realtime core can read the AP-Realtime core individual interrupt source register (INTEVTAS) in the INTCA during AP-Realtime core interrupt handler processing and process the peripheral interrupt assigned to the INTCA. A setting can be made in the INTCS to mask all peripheral interrupts sent from the INTCA.
- User-mode interrupt disabling function

  Specifying an interrupt mask level in the user interrupt mask level register S (USERIMASKS) disables interrupts that are not higher in priority than the specified mask level in user mode.

(c) LSI Internal Communication Interrupts and Wakeup Function

- A specified event in the internal connections of the LSI can be used to generate a request to the AP-System core for wakeup from power cutoff state or an interrupt.
- A specified event in the internal connections of the LSI can be used to generate a request to the AP-RealTime core for wakeup from power cutoff state or an interrupt.

A block diagram of the INTC is shown in figure 5.1.

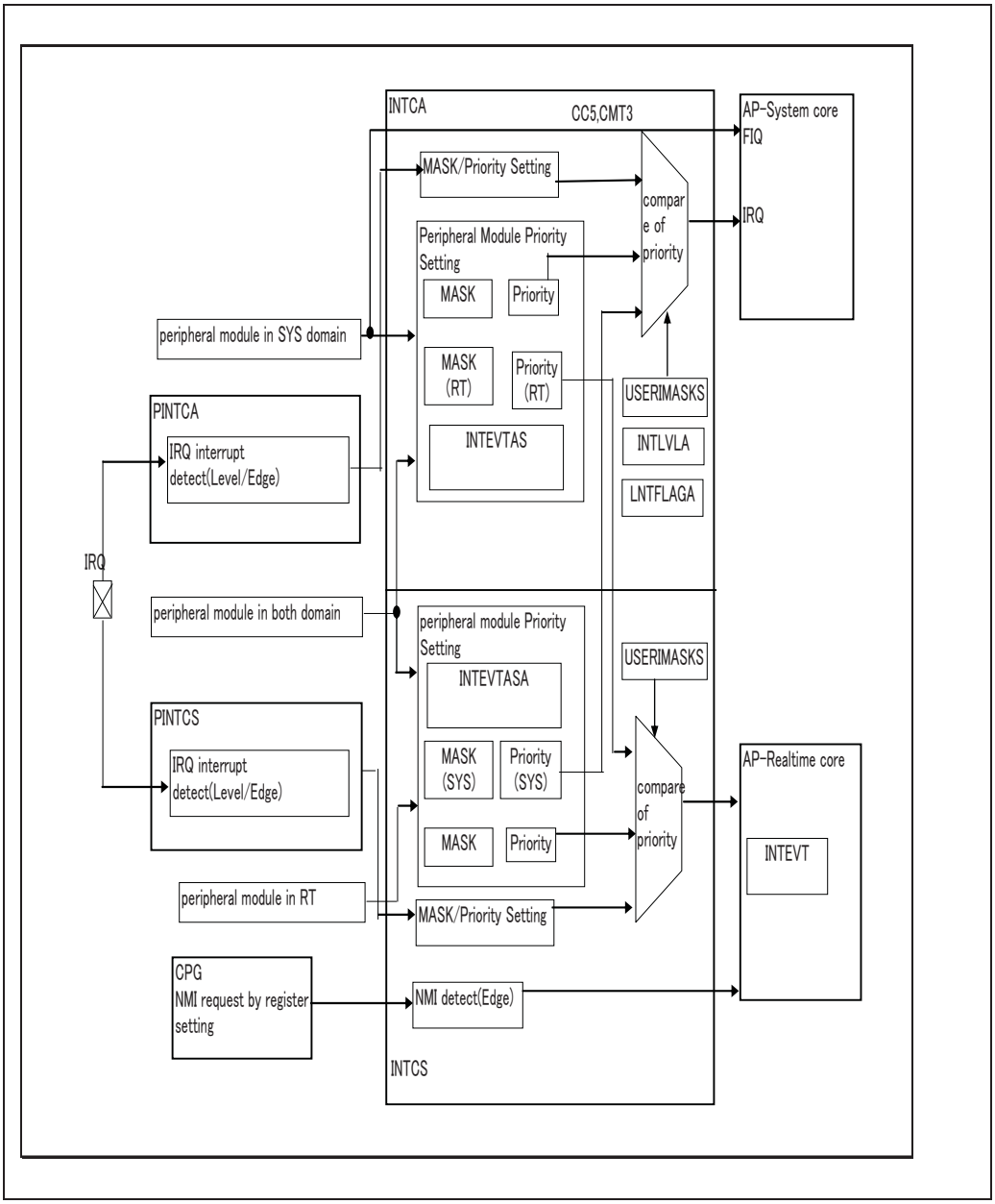


Figure 5.1 Block Diagram of INTC

5.2 Input/Output Pins

Table 5.1 shows the INTC pin configuration.

Table 5.1 Pin Configuration

Pin Name	Function	I/O	Description
IRQ31 to IRQ0	Interrupt input pins IRQ31 to IRQ0	Input	Input of IRQ31 to IRQ0 interrupt request signals

5.3 Register Descriptions

This section describes the registers of INTCA, INTCS.

5.3.1 INTCA Register Configuration

Table 5.2 shows the INTCA register configuration. Table 5.3 shows the register states in each operating mode.

Table 5.2 Register Configuration

Register Name	Abbreviation	R/W	Address	Access Size
Interrupt control register 1A	ICR1A	R/W	H'E690 0000	32
Interrupt control register 2A	ICR2A	R/W	H'E690 0004	32
Interrupt control register 3A	ICR3A	R/W	H'E690 0008	32
Interrupt control register 4A	ICR4A	R/W	H'E690 000C	32
Interrupt flag register	INTFLGA	R	H'E698 0018	32
Interrupt event register	INTEVTA	R/W	H'E698 0020	32
Interrupt level register A	INTLVLA	R/W	H'E698 0030	8
Interrupt level register B	INTLVLB	R/W	H'E698 0034	8
AP-Realtime core individual interrupt source register	INTEVTAS	R	H'E694 0100	32

Register Name	Abbreviation	R/W	Address	Access Size
AP-Realtime core interrupt mask register	INTSMASK	R/W	H'E694 0104	16
Interrupt priority register 00A	INTPRI00A	R/W	H'E690 0010	32
Interrupt priority register 10A	INTPRI10A	R/W	H'E690 0014	32
Interrupt priority register 20A	INTPRI20A	R/W	H'E690 0018	32
Interrupt priority register 30A	INTPRI30A	R/W	H'E690 001C	32
Interrupt source register 00A	INTREQ00A	R/W	H'E690 0020	8
Interrupt source register 10A	INTREQ10A	R/W	H'E690 0024	8
Interrupt source register 20A	INTREQ20A	R/W	H'E690 0028	8
Interrupt source register 30A	INTREQ30A	R/W	H'E690 002C	8
Interrupt mask register 00A	INTMSK00A	R/W	H'E690 0040	8
Interrupt mask register 10A	INTMSK10A	R/W	H'E690 0044	8
Interrupt mask register 20A	INTMSK20A	R/W	H'E690 0048	8
Interrupt mask register 30A	INTMSK30A	R/W	H'E690 004C	8
Interrupt mask clear register 00A	INTMSKCLR00A	W	H'E690 0060	8
Interrupt mask clear register 10A	INTMSKCLR10A	W	H'E690 0064	8
Interrupt mask clear register 20A	INTMSKCLR20A	W	H'E690 0068	8
Interrupt mask clear register 30A	INTMSKCLR30A	W	H'E690 006C	8
FIQ status register A	FIQSRA	R/W	H'E698 00C0	16
User interrupt mask level register A	USERIMASKA	R/W	H'E69C 0000	32
Peripheral interrupt priority register AA	IPRAA	R/W	H'E694 0000	16
Peripheral interrupt priority register BA	IPRBA	R/W	H'E694 0004	16
Peripheral interrupt priority register CA	IPRCA	R/W	H'E694 0008	16
Peripheral interrupt priority register DA	IPRDA	R/W	H'E694 000C	16
Peripheral interrupt priority register EA	IPREA	R/W	H'E694 0010	16
Peripheral interrupt priority register FA	IPRFA	R/W	H'E694 0014	16
Peripheral interrupt priority register GA	IPRGA	R/W	H'E694 0018	16
Peripheral interrupt priority register HA	IPRHA	R/W	H'E694 001C	16
Peripheral interrupt priority register IA	IPRIA	R/W	H'E694 0020	16
Peripheral interrupt priority register JA	IPRJA	R/W	H'E694 0024	16
Peripheral interrupt priority register KA	IPRKA	R/W	H'E694 0028	16
Peripheral interrupt priority register LA	IPRLA	R/W	H'E694 002C	16
Peripheral interrupt priority register MA	IPRMA	R/W	H'E694 0030	16

Peripheral interrupt priority register NA	IPRNA	R/W	H'E694 0034	16
Peripheral interrupt priority register OA	IPROA	R/W	H'E694 0038	16
Peripheral interrupt priority register AA3	IPRAA3	R/W	H'E695 0000	16
Peripheral interrupt priority register BA3	IPRBA3	R/W	H'E695 0004	16
Peripheral interrupt priority register CA3	IPRCA3	R/W	H'E695 0008	16
Peripheral interrupt priority register DA3	IPRDA3	R/W	H'E695 000C	16
Peripheral interrupt priority register EA3	IPREA3	R/W	H'E695 0010	16
Peripheral interrupt priority register FA3	IPRFA3	R/W	H'E695 0014	16
Peripheral interrupt priority register GA3	IPRGA3	R/W	H'E695 0018	16
Peripheral interrupt priority register HA3	IPRHA3	R/W	H'E695 001C	16
Peripheral interrupt priority register IA3	IPRIA3	R/W	H'E695 0020	16
Peripheral interrupt priority register JA3	IPRJA3	R/W	H'E695 0024	16
Peripheral interrupt priority register KA3	IPRKA3	R/W	H'E695 0028	16
Peripheral interrupt priority register LA3	IPRLA3	R/W	H'E695 002C	16
Peripheral interrupt priority register MA3	IPRMA3	R/W	H'E695 0030	16
Peripheral interrupt priority register NA3	IPRNA3	R/W	H'E695 0034	16
Peripheral interrupt priority register OA3	IPROA3	R/W	H'E695 0038	16
Peripheral interrupt priority register PA3	IPRPA3	R/W	H'E695 003C	16
Peripheral interrupt priority register RA3	IPRRA3	R/W	H'E6950040	16
Peripheral interrupt priority register SA3	IPRSA3	R/W	H'E6950044	16
Peripheral interrupt priority register SA3	IPRSA3	R/W	H'E6950048	16
Peripheral interrupt priority register TA3	IPRTA3	R/W	H'E695004C	16
Peripheral interrupt priority register UA3	IPRUA3	R/W	H'E6950050	16
Peripheral interrupt mask register 0A	IMR0A	R/W	H'E694 0080	8
Peripheral interrupt mask register 1A	IMR1A	R/W	H'E694 0084	8
Peripheral interrupt mask register 2A	IMR2A	R/W	H'E694 0088	8
Peripheral interrupt mask register 3A	IMR3A	R/W	H'E694 008C	8
Peripheral interrupt mask register 4A	IMR4A	R/W	H'E694 0090	8

Register Name	Abbreviation	R/W	Address	Access Size
Peripheral interrupt mask register 5A	IMR5A	R/W	H'E694 0094	8
Peripheral interrupt mask register 6A	IMR6A	R/W	H'E694 0098	8
Peripheral interrupt mask register 7A	IMR7A	R/W	H'E694 009C	8
Peripheral interrupt mask register 8A	IMR8A	R/W	H'E694 00A0	8
Peripheral interrupt mask register 9A	IMR9A	R/W	H'E694 00A4	8
Peripheral interrupt mask register 10A	IMR10A	R/W	H'E694 00A8	8
Peripheral interrupt mask register 11A	IMR11A	R/W	H'E694 00AC	8
Peripheral interrupt mask register 12A	IMR12A	R/W	H'E694 00B0	8
Peripheral interrupt mask register 13A	IMR13A	R/W	H'E694 00B4	8
Peripheral interrupt mask register 0A3	IMR0A3	R/W	H'E695 0080	8
Peripheral interrupt mask register 1A3	IMR1A3	R/W	H'E695 0084	8
Peripheral interrupt mask register 2A3	IMR2A3	R/W	H'E695 0088	8
Peripheral interrupt mask register 3A3	IMR3A3	R/W	H'E695 008C	8
Peripheral interrupt mask register 4A3	IMR4A3	R/W	H'E695 0090	8
Peripheral interrupt mask register 5A3	IMR5A3	R/W	H'E695 0094	8
Peripheral interrupt mask register 6A3	IMR6A3	R/W	H'E695 0098	8
Peripheral interrupt mask register 7A3	IMR7A3	R/W	H'E695 009C	8
Peripheral interrupt mask register 8A3	IMR8A3	R/W	H'E69500A0	8
Peripheral interrupt mask register 9A3	IMR9A3	R/W	H'E69500A4	8
Peripheral interrupt mask register 10A3	IMR10A3	R/W	H'E69500A8	8
Peripheral interrupt mask clear register 0A	IMCR0A	W	H'E694 00C0	8
Peripheral interrupt mask clear register 1A	IMCR1A	W	H'E694 00C4	8
Peripheral interrupt mask clear register 2A	IMCR2A	W	H'E694 00C8	8
Peripheral interrupt mask clear register 3A	IMCR3A	W	H'E694 00CC	8
Peripheral interrupt mask clear register 4A	IMCR4A	W	H'E694 00D0	8
Peripheral interrupt mask clear register 5A	IMCR5A	W	H'E694 00D4	8
Peripheral interrupt mask clear register 6A	IMCR6A	W	H'E694 00D8	8
Peripheral interrupt mask clear register 7A	IMCR7A	W	H'E694 00DC	8
Peripheral interrupt mask clear register 8A	IMCR8A	W	H'E694 00E0	8
Peripheral interrupt mask clear register 9A	IMCR9A	W	H'E694 00E4	8
Peripheral interrupt mask clear register 10A	IMCR10A	W	H'E694 00E8	8
Peripheral interrupt mask clear register 11A	IMCR11A	W	H'E694 00EC	8

Peripheral interrupt mask clear register 12A	IMCR12A	W	H'E694 00F0	8
Peripheral interrupt mask clear register 13A	IMCR13A	W	H'E694 00F4	8
Peripheral interrupt mask clear register 0A3	IMCR0A3	W	H'E695 00C0	8
Peripheral interrupt mask clear register 1A3	IMCR1A3	W	H'E695 00C4	8
Peripheral interrupt mask clear register 2A3	IMCR2A3	W	H'E695 00C8	8
Peripheral interrupt mask clear register 3A3	IMCR3A3	W	H'E695 00CC	8
Peripheral interrupt mask clear register 4A3	IMCR4A3	W	H'E695 00D0	8
Peripheral interrupt mask clear register 5A3	IMCR5A3	W	H'E695 00D4	8
Peripheral interrupt mask clear register 6A3	IMCR6A3	W	H'E695 00D8	8
Peripheral interrupt mask clear register 7A3	IMCR7A3	W	H'E695 00DC	8
Peripheral interrupt mask clear register 8A3	IMCR8A3	W	H'E69500E0	8
Peripheral interrupt mask clear register 9A3	IMCR9A3	W	H'E69500E4	8
Peripheral interrupt mask clear register 10A3	IMCR10A3	W	H'E69500E8	8
Peripheral interrupt mask register 0AS	IMR0AS	R/W	H'E694 0180	8
Peripheral interrupt mask register 1AS	IMR1AS	R/W	H'E694 0184	8
Peripheral interrupt mask register 2AS	IMR2AS	R/W	H'E694 0188	8
Peripheral interrupt mask register 3AS	IMR3AS	R/W	H'E694 018C	8
Peripheral interrupt mask register 4AS	IMR4AS	R/W	H'E694 0190	8
Peripheral interrupt mask register 5AS	IMR5AS	R/W	H'E694 0194	8
Peripheral interrupt mask register 6AS	IMR6AS	R/W	H'E694 0198	8
Peripheral interrupt mask register 7AS	IMR7AS	R/W	H'E694 019C	8

Register Name	Abbreviation	R/W	Address	Access Size
Peripheral interrupt mask register 8AS	IMR8AS	R/W	H'E694 01A0	8
Peripheral interrupt mask register 9AS	IMR9AS	R/W	H'E694 01A4	8
Peripheral interrupt mask register 10AS	IMR10AS	R/W	H'E694 01A8	8
Peripheral interrupt mask register 11AS	IMR11AS	R/W	H'E694 01AC	8
Peripheral interrupt mask register 12AS	IMR12AS	R/W	H'E694 01B0	8
Peripheral interrupt mask register 13AS	IMR13AS	R/W	H'E694 01B4	8
Peripheral interrupt mask register 0AS3	IMR0AS3	R/W	H'E695 0180	8
Peripheral interrupt mask register 1AS3	IMR1AS3	R/W	H'E695 0184	8
Peripheral interrupt mask register 2AS3	IMR2AS3	R/W	H'E695 0188	8
Peripheral interrupt mask register 3AS3	IMR3AS3	R/W	H'E695 018C	8
Peripheral interrupt mask register 4AS3	IMR4AS3	R/W	H'E695 0190	8
Peripheral interrupt mask register 5AS3	IMR5AS3	R/W	H'E695 0194	8
Peripheral interrupt mask register 6AS3	IMR6AS3	R/W	H'E695 0198	8
Peripheral interrupt mask register 7AS3	IMR7AS3	R/W	H'E695 019C	8
Peripheral interrupt mask register 8AS3	IMR8AS3	R/W	H'E69501A0	8
Peripheral interrupt mask register 9AS3	IMR9AS3	R/W	H'E69501A4	8
Peripheral interrupt mask register 10AS3	IMR10AS3	R/W	H'E69501A8	8
Peripheral interrupt mask clear register 0AS	IMCR0AS	W	H'E694 01C0	8
Peripheral interrupt mask clear register 1AS	IMCR1AS	W	H'E694 01C4	8
Peripheral interrupt mask clear register 2AS	IMCR2AS	W	H'E694 01C8	8
Peripheral interrupt mask clear register 3AS	IMCR3AS	W	H'E694 01CC	8
Peripheral interrupt mask clear register 4AS	IMCR4AS	W	H'E694 01D0	8
Peripheral interrupt mask clear register 5AS	IMCR5AS	W	H'E694 01D4	8
Peripheral interrupt mask clear register 6AS	IMCR6AS	W	H'E694 01D8	8
Peripheral interrupt mask clear register 7AS	IMCR7AS	W	H'E694 01DC	8
Peripheral interrupt mask clear register 8AS	IMCR8AS	W	H'E694 01E0	8
Peripheral interrupt mask clear register 9AS	IMCR9AS	W	H'E694 01E4	8
Peripheral interrupt mask clear register 10AS	IMCR10AS	W	H'E694 01E8	8
Peripheral interrupt mask clear register 11AS	IMCR11AS	W	H'E694 01EC	8
Peripheral interrupt mask clear register 12AS	IMCR12AS	W	H'E694 01F0	8
Peripheral interrupt mask clear register 13AS	IMCR13AS	W	H'E694 01F4	8
Peripheral interrupt mask clear register 0AS3	IMCR0AS3	W	H'E695 01C0	8

Peripheral interrupt mask clear register 1AS3	IMCR1AS3	W	H'E695 01C4	8
Peripheral interrupt mask clear register 2AS3	IMCR2AS3	W	H'E695 01C8	8
Peripheral interrupt mask clear register 3AS3	IMCR3AS3	W	H'E695 01CC	8
Peripheral interrupt mask clear register 4AS3	IMCR4AS3	W	H'E695 01D0	8
Peripheral interrupt mask clear register 5AS3	IMCR5AS3	W	H'E695 01D4	8
Peripheral interrupt mask clear register 6AS3	IMCR6AS3	W	H'E695 01D8	8
Peripheral interrupt mask clear register 7AS3	IMCR7AS3	W	H'E695 01DC	8
Peripheral interrupt mask clear register 8AS3	IMCR8AS3	W	H'E69501E0	8
Peripheral interrupt mask clear register 9AS3	IMCR9AS3	W	H'E69501E4	8
Peripheral interrupt mask clear register 10AS3	IMCR10AS3	W	H'E69501E8	8
IRQ status check register0	ISCR0	R/W	H'E690 00C4	32
IRQ status check register1	ISCR1	R/W	H'E690 00C8	32
Pulse interrupt flag register 0A	IFLG0A	R/W	H'E694 0110	8
Pseudo-interrupt setting register 0A	SIR0A	R/W	H'E694 0114	8
DIRC interrupt setting register 0A	DIRCR	R/W	H'E694 0118	8
Secure control register	LIFEC_SEC_SRC	R/W	H’E611 0008	32

Table 5.3 Register States in Each Operating Mode

Abbreviation	Reset *	Module Standby
ICR1A to ICR4A	Initialized	Retained
INTFLGA	Initialized	Retained
INTEVTA	Initialized	Retained
INTLVLA	Initialized	Retained
INTLVLB	Initialized	Retained
VTB	Initialized	Retained
INTEVTAS	Initialized	Retained
INTSMASK	Initialized	Retained
INTPRI00A to INTPRI30A	Initialized	Retained
INTREQ00A to INTREQ30A	Initialized	Retained
INTMSK00A to INTMSK30A	Initialized	Retained
INTMSKCLR00A to INTMSKCLK30A	—	—
USERIMASKA	Initialized	Retained
IPRAA to IPROA	Initialized	Retained
IPRAA3 to IPRUA3	Initialized	Retained
IMR0A to IMR13A	Initialized	Retained
IMR0A3 to IMR10A3	Initialized	Retained
IMCR0A to IMCR13A	—	—
IMCR0A3 to IMCR10A3	—	—
IMR0AS to IMR13AS	Initialized	Retained
IMR0AS3 to IMR10AS3	Initialized	Retained
IMCR0AS to IMCR13AS	—	—
IMCR0AS3 to IMCR10AS3	—	—
ISCR0	Initialized	Retained
ISCR1	—	—
IFLG0A	Initialized	Retained
SIR0A	Initialized	Retained
DIRCR	Initialized	Retained
LIFEC_SEC_SRC	Initialized	Retained

Note: * For details, refer to section 1-D Overview of reset.

(1) Interrupt Control Register 1A (ICR1A)

ICR1A specifies the detection mode for external interrupt input pins IRQ7 to IRQ0 individually: rising edge, falling edge, low level, or high level. Note that the chattering removal period is set by ICR3 , ICR4.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IRQ0SA				IRQ1SA				IRQ2SA				IRQ3SA			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IRQ4SA				IRQ5SA				IRQ6SA				IRQ7SA			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	IRQ0SA	0000	R/W	IRQn Sense Select
27 to 24	IRQ1SA	0000	R/W	These bits select whether interrupt request signals from pins IRQ7 to IRQ0 are detected at a rising edge, a falling edge, a low level, a high level, or at both of a rising edge and a falling edge.
23 to 20	IRQ2SA	0000	R/W	
19 to 15	IRQ3SA	0000	R/W	
15 to 12	IRQ4SA	0000	R/W	
11 to 8	IRQ5SA	0000	R/W	
7 to 4	IRQ6SA	0000	R/W	
3 to 0	IRQ7SA	0000	R/W	

IRQnSA	Detection Mode
0000	Interrupt request is detected at a falling edge of IRQn input
0001	Interrupt request is detected at a rising edge of IRQn input
0010	Interrupt request is detected at a low level of IRQn input
0011	Interrupt request is detected at a high level of IRQn input
0100	Interrupt request is detected at both edges of IRQn input

[Legend]
n = 0 to 7

(2) Interrupt Control Register 2A (ICR2A)

ICR2A specifies the detection mode for external interrupt input pins IRQ15 to IRQ8 individually: rising edge, falling edge, low level, or high level. Note that the chattering removal period is set by ICR5 , ICR6.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IRQ8SA				IRQ9SA				IRQ10SA				IRQ11SA			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IRQ12SA				IRQ13SA				IRQ14SA				IRQ15SA			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

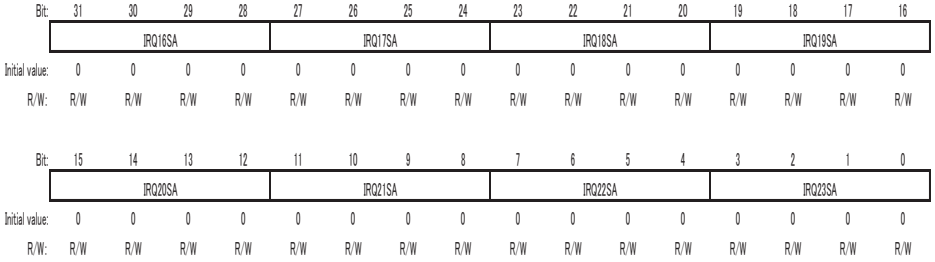
Bit	Bit Name	Initial Value	R/W	Description
31 to 28	IRQ8SA	0000	R/W	IRQn Sense Select
27 to 24	IRQ9SA	0000	R/W	These bits select whether interrupt request signals from pins IRQ8 to IRQ15 are detected at a rising edge, a falling edge, a low level, a high level, or at both of a rising edge and a falling edge.
23 to 20	IRQ10SA	0000	R/W	
19 to 15	IRQ11SA	0000	R/W	
15 to 12	IRQ12SA	0000	R/W	
11 to 8	IRQ13SA	0000	R/W	
7 to 4	IRQ14SA	0000	R/W	
3 to 0	IRQ15SA	0000	R/W	

IRQnSA	Detection Mode
0000	Interrupt request is detected at a falling edge of IRQn input
0001	Interrupt request is detected at a rising edge of IRQn input
0010	Interrupt request is detected at a low level of IRQn input
0011	Interrupt request is detected at a high level of IRQn input
0100	Interrupt request is detected at both edges of IRQn input

[Legend]
n = 8 to 15

(3) Interrupt Control Register 3A (ICR3A)

ICR3A specifies the detection mode for external interrupt input pins IRQ23 to IRQ16 individually: rising edge, falling edge, low level, or high level. Note that the chattering removal period is set by ICR7, ICR8.



Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IRQ16SA				IRQ17SA				IRQ18SA				IRQ19SA			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IRQ20SA				IRQ21SA				IRQ22SA				IRQ23SA			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

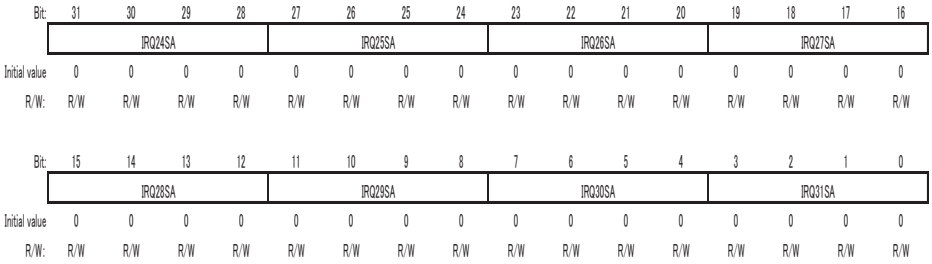
31 to 28	IRQ16SA	0000	R/W	IRQn Sense Select These bits select whether interrupt request signals from pins IRQ16 to IRQ23 are detected at a rising edge, a falling edge, a low level, a high level, or at both of a rising edge and a falling edge.
27 to 24	IRQ17SA	0000	R/W	
23 to 20	IRQ18SA	0000	R/W	
19 to 15	IRQ19SA	0000	R/W	
15 to 12	IRQ20SA	0000	R/W	
11 to 8	IRQ21SA	0000	R/W	
7 to 4	IRQ22SA	0000	R/W	
3 to 0	IRQ23SA	0000	R/W	

IRQnSA	Detection Mode
0000	Interrupt request is detected at a falling edge of IRQn input
0001	Interrupt request is detected at a rising edge of IRQn input
0010	Interrupt request is detected at a low level of IRQn input
0011	Interrupt request is detected at a high level of IRQn input
0100	Interrupt request is detected at both edges of IRQn input

[Legend]
n = 16 to 23

(4) Interrupt Control Register 4A (ICR4A)

ICR4A specifies the detection mode for external interrupt input pins IRQ31 to IRQ24 individually: rising edge, falling edge, low level, or high level. Note that the chattering removal period is set by ICR9, ICR10.



31 to 28	IRQ24SA	0000	R/W	IRQn Sense Select These bits select whether interrupt request signals from pins IRQ24 to IRQ31 are detected at a rising edge, a falling edge, a low level, a high level, or at both of a rising edge and a falling edge.
27 to 24	IRQ25SA	0000	R/W	
23 to 20	IRQ26SA	0000	R/W	
19 to 15	IRQ27SA	0000	R/W	
15 to 12	IRQ28SA	0000	R/W	
11 to 8	IRQ29SA	0000	R/W	
7 to 4	IRQ30SA	0000	R/W	
3 to 0	IRQ31SA	0000	R/W	

IRQnSA	Detection Mode
0000	Interrupt request is detected at a falling edge of IRQn input
0001	Interrupt request is detected at a rising edge of IRQn input
0010	Interrupt request is detected at a low level of IRQn input
0011	Interrupt request is detected at a high level of IRQn input
0100	Interrupt request is detected at both edges of IRQn input

[Legend]
n = 24 to 31

(5) Interrupt Flag Register (INTFLGA)

INTFLGA is a 32-bit read-only register that can only be accessed by the CPU. It holds the encoded interrupt request flag. When this register is read, the accepted interrupt code is stored in INTEVTA, the interrupt level of the accepted interrupt source is stored in the lower four bits of INTLVLA, and the INTLVLA value before update is stored in INTLVLB.

The ARM-IRQ interrupt handler reads INTFLGA only once and determines the interrupt source. If this register is read multiple times, the interrupt flag may be cleared unexpectedly.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	EVTCODEA									-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13 to 5	EVTCODEA	H'000	R	Interrupt Code These bits hold the interrupt code. For details, see table 5.10 and 5.11.
4 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

(6) Interrupt Event Register (INTEVTA)

INTEVTA is a 32-bit register that can be read from or written to by the CPU.

The INTFLGA value is written to this register through hardware by reading from INTFLGA with the ARM-IRQ interrupt handler.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	EVTCODEA									-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13 to 5	EVTCODEA	H'000	R/W	Interrupt Code These bits hold the interrupt code. For details, see table 5.10 and 5.11.
4 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

(7) Interrupt Level Register A (INTLVLA)

INTLVLA is an 8-bit readable/writable register that specifies the level to mask interrupts. When the level of an interrupt is not higher in priority than the level specified in this register, the interrupt is masked.

The interrupt level of the accepted interrupt source is stored in the lower four bits of this register by reading from INTFLGA. This automatically masks the interrupts whose priority levels are equal to or lower than that of the accepted interrupt source.

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	LEVELA			
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	LEVELA	H'00	R/W	Interrupt Level When the level of an interrupt is not higher than the level specified in these bits, the interrupt is masked.

(8) Interrupt Level Register B (INTLVLB)

When INTLVLA is automatically updated by INTFLGA reading, the previous INTLVLA value is saved in INTLVLB. This register can be read and written to by the CPU.

When execution returns from the interrupt handler, the INTLVLB value should be written back to INTLVLA by software to restore the interrupt mask level.

Note that the INTLVLB should be saved in the stack when multiple interrupts are accepted.

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	LEVELB			
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	LEVELB	H'00	R/W	Interrupt Level These bits store a backup of the INTLVLA value.

(9) Interrupt Priority Register 00A (INTPRI00A)

INTPRI00A is a register that specifies priority levels from 15 to 0 for external interrupt input pins IRQ7 to IRQ0.

Each 4-bit group is set with a value from H'F (1111) to H'0 (0000) to specify the interrupt priority level for the corresponding interrupt. Setting H'F means priority level 15 (the highest level); H'0 means priority level 0 (the request is masked).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IRQ0A				IRQ1A				IRQ2A				IRQ3A			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IRQ4A				IRQ5A				IRQ6A				IRQ7A			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	IRQ0A	H'0	R/W	These bits specify the priority level for each interrupt source in 4-bit units.
27 to 24	IRQ1A	H'0	R/W	
23 to 20	IRQ2A	H'0	R/W	
19 to 16	IRQ3A	H'0	R/W	
15 to 12	IRQ4A	H'0	R/W	
11 to 8	IRQ5A	H'0	R/W	
7 to 4	IRQ6A	H'0	R/W	
3 to 0	IRQ7A	H'0	R/W	

(10) Interrupt Priority Register 10A (INTPRI10A)

INTPRI10A is a register that specifies priority levels from 15 to 0 for external interrupt input pins IRQ15 to IRQ8.

Each 4-bit group is set with a value from H'F (1111) to H'0 (0000) to specify the interrupt priority level for the corresponding interrupt. Setting H'F means priority level 15 (the highest level); H'0 means priority level 0 (the request is masked).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IRQ8A				IRQ9A				IRQ10A				IRQ11A			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

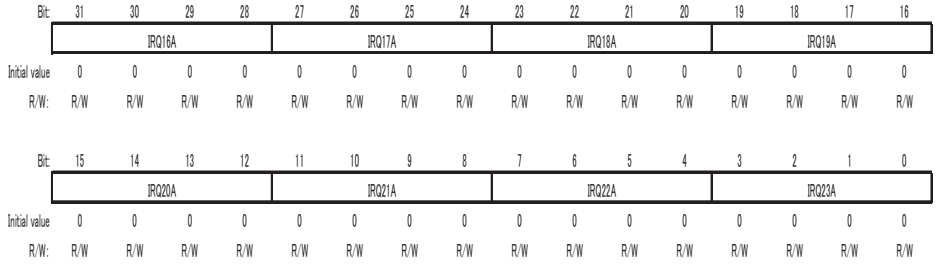
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IRQ12A				IRQ13A				IRQ14A				IRQ15A			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	IRQ8A	H'0	R/W	These bits specify the priority level for each interrupt source in 4-bit units.
27 to 24	IRQ9A	H'0	R/W	
23 to 20	IRQ10A	H'0	R/W	
19 to 16	IRQ11A	H'0	R/W	
15 to 12	IRQ12A	H'0	R/W	
11 to 8	IRQ13A	H'0	R/W	
7 to 4	IRQ14A	H'0	R/W	
3 to 0	IRQ15A	H'0	R/W	

(11) Interrupt Priority Register 20A (INTPRI20A)

INTPRI20A is a register that specifies priority levels from 15 to 0 for external interrupt input pins IRQ23 to IRQ16.

Each 4-bit group is set with a value from H'F (1111) to H'0 (0000) to specify the interrupt priority level for the corresponding interrupt. Setting H'F means priority level 15 (the highest level); H'0 means priority level 0 (the request is masked).

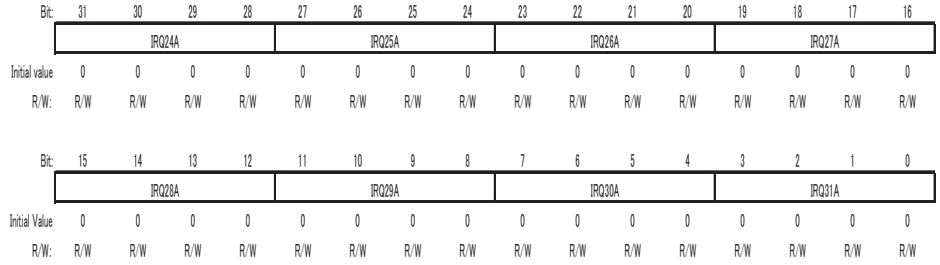


Bit	Bit Name	Initial Value	R/W	Description
31 to 28	IRQ16A	H'0	R/W	These bits specify the priority level for each interrupt source in 4-bit units.
27 to 24	IRQ17A	H'0	R/W	
23 to 20	IRQ18A	H'0	R/W	
19 to 16	IRQ19A	H'0	R/W	
15 to 12	IRQ20A	H'0	R/W	
11 to 8	IRQ21A	H'0	R/W	
7 to 4	IRQ22A	H'0	R/W	
3 to 0	IRQ23A	H'0	R/W	

(12) Interrupt Priority Register 30A (INTPRI30A)

INTPRI30A is a register that specifies priority levels from 15 to 0 for external interrupt input pins IRQ31 to IRQ24.

Each 4-bit group is set with a value from H'F (1111) to H'0 (0000) to specify the interrupt priority level for the corresponding interrupt. Setting H'F means priority level 15 (the highest level); H'0 means priority level 0 (the request is masked).



Bit	Bit Name	Initial Value	R/W	Description
31 to 28	IRQ24A	H'0	R/W	These bits specify the priority level for each interrupt source in 4-bit units.
27 to 24	IRQ25A	H'0	R/W	
23 to 20	IRQ26A	H'0	R/W	
19 to 16	IRQ27A	H'0	R/W	
15 to 12	IRQ28A	H'0	R/W	
11 to 8	IRQ29A	H'0	R/W	
7 to 4	IRQ30A	H'0	R/W	
3 to 0	IRQ31A	H'0	R/W	

(13) Peripheral Interrupt Priority Registers AA to OA, AA3 to UA3 (IPRAA to IPROA, IPRAA3 to IPRUA3)

IPRAA to IPROA and IPRAA3 to IPRUA3 are registers that specify priority levels from 15 to 0 for on-chip peripheral module interrupts.

Four modules are assigned to each register. Each 4-bit group is set with a value from H'F (1111) to H'0 (0000) to specify the interrupt priority level for the corresponding interrupt. Setting H'F means priority level 15 (the highest level); H'0 means priority level 0 (the request is masked).

Table 5.4 shows the correspondence between the peripheral modules requesting interrupts and the peripheral interrupt priority registers.

IPRAA to IPROA:

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IPR0nA				IPR1nA				IPR2nA				IPR3nA			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

IPRAA3 to IPRUA3:

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IPR0mA3				IPR1mA3				IPR2mA3				IPR3mA3			
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

IPRAA to IPROA:

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	IPR0nA	H'0	R/W	These bits specify the priority level for each interrupt source in 4-bit units. For details, see table 5.4.
11 to 8	IPR1nA	H'0	R/W	
7 to 4	IPR2nA	H'0	R/W	
3 to 0	IPR3nA	H'0	R/W	

[Legend]
n = A to O

IPRAA3 to IPRUA3:

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	IPR0mA3	H'0	R/W	These bits specify the priority level for each interrupt source in 4-bit units. For details, see table 5.4.
11 to 8	IPR1mA3	H'0	R/W	
7 to 4	IPR2mA3	H'0	R/W	
3 to 0	IPR3mA3	H'0	R/W	

n = A to U

Table 5.4 Interrupt Sources , IPRAA to IPROA and IPRAA3 to IPRUA3

Register Name	IPR0nA	IPR1nA	IPR2nA	IPR3nA
IPRAA	DMAC3(1)	DMAC3(2)	CMT2	—
IPRBA	IrDA	—	BBIF1	BBIF2
IPRCA	—	Crypt	CMT11	AP-ARM※1
IPRDA	—	—	CMT12	—
IPREA	DMAC1(1)	MFIS	ACMFI1/2	—
IPRFA	KEYSC	DMAC1(2)	3DG	CMT10
IPRGA	SCIFA0	SCIFA1	SCIFA2	SCIFA3
IPRHA	MSIOF2	USBHSDMAC	FLCTL	SDHI0
IPRIA	MSIOF1	SCIFA4	MSU	IIC1
IPRJA	DMAC2(1)	DMAC2(2)	MSUG	TTI20
IPRKA	—	CMT13	—	SDHI1
IPRLA	TPU0	—	—	—
IPRMA	—	CMT3	—	RWDT0
IPRNA	SCIFB	SCIFA5	—	DDM
IPROA	—	—	DIRC	SDHIF2
IPRAA3	SHWYSTAT	—	—	—
IPRBA3	—	—	—	—
IPRCA3	—	—	—	—
IPRDA3	—	—	—	—
IPREA3	—	—	—	—
IPRFA3	—	—	—	—
IPRGA3	—	—	—	—
IPRHA3	—	—	—	—
IPRIA3	—	—	—	—

Register Name	IPR0nA	IPR1nA	IPR2nA	IPR3nA
IPRJA3	—	—	—	HDMI
IPRKA3	SPU2	—	FSI	FMSI
IPRLA3	—	—	—	MIPI-HSI
IPRMA3	IPMMU	—	CEC_1	CEC_2
IPRNA3	AP-ARM※2	—	—	—
IPROA3	MFIS2	CPORTR2S	CMT14	CMT15
IPRPA3	—	—	MMC_ERR	MMC_NOR
IPRQA3	ALI4(IIC4)	TACKI4(IIC4)	WAITI4(IIC4)	DTEI4(IIC4)
IPRRA3	ALI3(IIC3)	TACKI3(IIC3)	WAITI3(IIC3)	DTEI3(IIC3)
IPRSA3	ERI	RXI	TXI	TEI
IPRTA3	USBI1 (ch0)	USBI0 (ch0)	USBI1 (ch1)	USBI0 (ch1)
IPRUA3	USBHSDMAC1	—	—	—

Note: —: Reserved. An undefined value will be read. Writing is ignored.

※1 IRQPMU、COMMTX、COMMRX

※2 CTIIRQ、DMAEXTERRIRQ、DMAIRQ、DMASIRQ

(14) Interrupt Source Register 00A (INTREQ00A)

INTREQ00A is a register that indicates interrupt requests from external input pins IRQ7 to IRQ0. This register value is not affected by the INTPRI00A setting or the interrupt masks specified with INTMSK00A.

When edge-detection mode is set for an IRQ pin (ICR1A.IRQnSA = B'00 or B'01), an interrupt request is cleared by writing 0 to the corresponding IRQnA bit after reading IRQnA = 1; write 1 to the other bits.

Bit:	7	6	5	4	3	2	1	0
	IRQ0A	IRQ1A	IRQ2A	IRQ3A	IRQ4A	IRQ5A	IRQ6A	IRQ7A
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	IRQ0A	0	R/W	IRQn Interrupt Request
6	IRQ1A	0	R/W	Indicates whether there is an interrupt request input to the IRQn pin.
5	IRQ2A	0	R/W	[When edge-detection mode is selected (ICR1A.IRQnSA = B'00 or B'01)]
4	IRQ3A	0	R/W	When reading:
3	IRQ4A	0	R/W	0: No interrupt request has been detected
2	IRQ5A	0	R/W	1: An interrupt request has been detected
1	IRQ6A	0	R/W	When writing:
0	IRQ7A	0	R/W	0: Each bit is cleared by writing 0 after reading 1
				1: Writing 1 is ignored
				[When level-detection mode is selected (ICR1A.IRQnSA = B'10 or B'11)]
				When reading:
				0: The corresponding interrupt pin has not been asserted
				1: The corresponding interrupt pin has been asserted
				When writing:
				Writing 0 or 1 is ignored.

[Legend]
n = 0 to 7

(15) Interrupt Source Register 10A (INTREQ10A)

INTREQ10A is a register that indicates interrupt requests from external input pins IRQ15 to IRQ8. This register value is not affected by the INTPRI10A setting or the interrupt masks specified with INTMSK10A.

When edge-detection mode is set for an IRQ pin (ICR2A.IRQnSA = B'00 or B'01), an interrupt request is cleared by writing 0 to the corresponding IRQnA bit after reading IRQnA = 1; write 1 to the other bits.

Bit:	7	6	5	4	3	2	1	0
	IRQ 8A	IRQ 9A	IRQ 10A	IRQ 11A	IRQ 12A	IRQ 13A	IRQ 14A	IRQ 15A
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

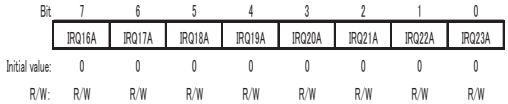
Bit	Bit Name	Initial Value	R/W	Description
7	IRQ8A	0	R/W	IRQn Interrupt Request
6	IRQ9A	0	R/W	Indicates whether there is an interrupt request input to the IRQn pin.
5	IRQ10A	0	R/W	[When edge-detection mode is selected (ICR2A.IRQnSA = B'00 or B'01)]
4	IRQ11A	0	R/W	When reading:
3	IRQ12A	0	R/W	0: No interrupt request has been detected
2	IRQ13A	0	R/W	1: An interrupt request has been detected
1	IRQ14A	0	R/W	When writing:
0	IRQ15A	0	R/W	0: Each bit is cleared by writing 0 after reading 1
				1: Writing 1 is ignored
				[When level-detection mode is selected (ICR2A.IRQnSA = B'10 or B'11)]
				When reading:
				0: The corresponding interrupt pin has not been asserted
				1: The corresponding interrupt pin has been asserted
				When writing:
				Writing 0 or 1 is ignored.

[Legend]
n = 8 to 15

(16) Interrupt Source Register 20A (INTREQ20A)

INTREQ20A is a register that indicates interrupt requests from external input pins IRQ23 to IRQ16. This register value is not affected by the INTPRI20A setting or the interrupt masks specified with INTMSK20A.

When edge-detection mode is set for an IRQ pin (ICR3A.IRQnSA = B'00 or B'01), an interrupt request is cleared by writing 0 to the corresponding IRQnA bit after reading IRQnA = 1; write 1 to the other bits.



Bit	7	6	5	4	3	2	1	0
	IRQ16A	IRQ17A	IRQ18A	IRQ19A	IRQ20A	IRQ21A	IRQ22A	IRQ23A
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

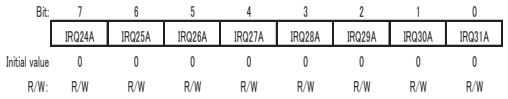
Bit	Bit Name	Initial Value	R/W	Description
7	IRQ16A	0	R/W	IRQn Interrupt Request
6	IRQ17A	0	R/W	Indicates whether there is an interrupt request input to the IRQn pin.
5	IRQ18A	0	R/W	[When edge-detection mode is selected (ICR3A.IRQnSA = B'00 or B'01)]
4	IRQ19A	0	R/W	When reading:
3	IRQ20A	0	R/W	0: No interrupt request has been detected
2	IRQ21A	0	R/W	1: An interrupt request has been detected
1	IRQ22A	0	R/W	When writing:
0	IRQ23A	0	R/W	0: Each bit is cleared by writing 0 after reading 1
				1: Writing 1 is ignored
				[When level-detection mode is selected (ICR3A.IRQnSA = B'10 or B'11)]
				When reading:
				0: The corresponding interrupt pin has not been asserted
				1: The corresponding interrupt pin has been asserted
				When writing:
				Writing 0 or 1 is ignored.

[Legend]
n = 16 to 23

(17) Interrupt Source Register 30A (INTREQ30A)

INTREQ30A is a register that indicates interrupt requests from external input pins IRQ31 to IRQ24. This register value is not affected by the INTPRI30A setting or the interrupt masks specified with INTMSK30A.

When edge-detection mode is set for an IRQ pin (ICR4A.IRQnSA = B'00 or B'01), an interrupt request is cleared by writing 0 to the corresponding IRQnA bit after reading IRQnA = 1; write 1 to the other bits.



Bit:	7	6	5	4	3	2	1	0
	IRQ24A	IRQ25A	IRQ26A	IRQ27A	IRQ28A	IRQ29A	IRQ30A	IRQ31A
Initial value	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	IRQ24A	0	R/W	IRQn Interrupt Request
6	IRQ25A	0	R/W	Indicates whether there is an interrupt request input to the IRQn pin.
5	IRQ26A	0	R/W	[When edge-detection mode is selected (ICR4A.IRQnSA = B'00 or B'01)]
4	IRQ27A	0	R/W	When reading:
3	IRQ28A	0	R/W	0: No interrupt request has been detected
2	IRQ29A	0	R/W	1: An interrupt request has been detected
1	IRQ30A	0	R/W	When writing:
0	IRQ31A	0	R/W	0: Each bit is cleared by writing 0 after reading 1
				1: Writing 1 is ignored
				[When level-detection mode is selected (ICR4A.IRQnSA = B'10 or B'11)]
				When reading:
				0: The corresponding interrupt pin has not been asserted
				1: The corresponding interrupt pin has been asserted
				When writing:
				Writing 0 or 1 is ignored.

[Legend]
n = 31 to 24

(18) Interrupt Mask Register 00A (INTMSK00A)

INTMSK00A is a register that masks interrupt requests from external interrupt input pins IRQ7 to IRQ0.

To clear an interrupt mask, write 1 to the corresponding bit in INTMSKCLR00A. Writing 0 to the corresponding bit in INTMSK00A does not affect the bit value.

Bit:	7	6	5	4	3	2	1	0
	IRQ0A	IRQ1A	IRQ2A	IRQ3A	IRQ4A	IRQ5A	IRQ6A	IRQ7A
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	IRQ0A	0	R/W	IRQn Interrupt Mask
6	IRQ1A	0	R/W	0: The corresponding interrupt is not masked
5	IRQ2A	0	R/W	1: The corresponding interrupt is masked
4	IRQ3A	0	R/W	
3	IRQ4A	0	R/W	
2	IRQ5A	0	R/W	
1	IRQ6A	0	R/W	
0	IRQ7A	0	R/W	

[Legend]
n = 0 to 7

(19) Interrupt Mask Register 10A (INTMSK10A)

INTMSK10A is a register that masks interrupt requests from external interrupt input pins IRQ15 to IRQ8.

To clear an interrupt mask, write 1 to the corresponding bit in INTMSKCLR10A. Writing 0 to the corresponding bit in INTMSK10A does not affect the bit value.

Bit:	7	6	5	4	3	2	1	0
	IRQ8A	IRQ9A	IRQ 10A	IRQ 11A	IRQ 12A	IRQ 13A	IRQ 14A	IRQ 15A
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	IRQ8A	0	R/W	IRQn Interrupt Mask
6	IRQ9A	0	R/W	0: The corresponding interrupt is not masked
5	IRQ10A	0	R/W	1: The corresponding interrupt is masked
4	IRQ11A	0	R/W	
3	IRQ12A	0	R/W	
2	IRQ13A	0	R/W	
1	IRQ14A	0	R/W	
0	IRQ15A	0	R/W	

[Legend]
n = 8 to 15

(20) Interrupt Mask Register 20A (INTMSK20A)

INTMSK20A is a register that masks interrupt requests from external interrupt input pins IRQ23 to IRQ16.

To clear an interrupt mask, write 1 to the corresponding bit in INTMSKCLR20A. Writing 0 to the corresponding bit in INTMSK20A does not affect the bit value.

Bit	7	6	5	4	3	2	1	0
	IRQ16A	IRQ17A	IRQ18A	IRQ19A	IRQ20A	IRQ21A	IRQ22A	IRQ23A
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	IRQ16A	0	R/W	IRQn Interrupt Mask
6	IRQ17A	0	R/W	0: The corresponding interrupt is not masked
5	IRQ18A	0	R/W	1: The corresponding interrupt is masked
4	IRQ19A	0	R/W	
3	IRQ20A	0	R/W	
2	IRQ21A	0	R/W	
1	IRQ22A	0	R/W	
0	IRQ23A	0	R/W	

[Legend]
n = 23 to 16

(21) Interrupt Mask Register 30A (INTMSK30A)

INTMSK20A is a register that masks interrupt requests from external interrupt input pins IRQ31 to IRQ24.

To clear an interrupt mask, write 1 to the corresponding bit in INTMSKCLR30A. Writing 0 to the corresponding bit in INTMSK30A does not affect the bit value.

Bit:	7	6	5	4	3	2	1	0
	IRQ24A	IRQ25A	IRQ26A	IRQ27A	IRQ28A	IRQ29A	IRQ30A	IRQ31A
Initial value	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	IRQ24A	0	R/W	IRQn Interrupt Mask
6	IRQ25A	0	R/W	0: The corresponding interrupt is not masked
5	IRQ26A	0	R/W	1: The corresponding interrupt is masked
4	IRQ27A	0	R/W	
3	IRQ28A	0	R/W	
2	IRQ29A	0	R/W	
1	IRQ30A	0	R/W	
0	IRQ31A	0	R/W	

[Legend]
n = 31 to 24

(22) Interrupt Mask Clear Register 00A (INTMSKCLR00A)

INTMSKCLR00A is a write-only register that clears the mask settings for interrupts from external interrupt input pins IRQ7 to IRQ0.

Bit:	7	6	5	4	3	2	1	0
	IRQ0A	IRQ1A	IRQ2A	IRQ3A	IRQ4A	IRQ5A	IRQ6A	IRQ7A
Initial value:	-	-	-	-	-	-	-	-
R/W:	W	W	W	W	W	W	W	W

Bit	Bit Name	Initial Value	R/W	Description
7	IRQ0A	—	W	IRQn Interrupt Mask Clear
6	IRQ1A	—	W	0: Writing 0 is ignored
5	IRQ2A	—	W	1: Clears the corresponding interrupt mask
4	IRQ3A	—	W	When reading:
3	IRQ4A	—	W	An undefined value will be read.
2	IRQ5A	—	W	
1	IRQ6A	—	W	
0	IRQ7A	—	W	

[Legend]
n = 0 to 7

(23) Interrupt Mask Clear Register 10A (INTMSKCLR10A)

INTMSKCLR10A is a write-only register that clears the mask settings for interrupts from external interrupt input pins IRQ15 to IRQ8.

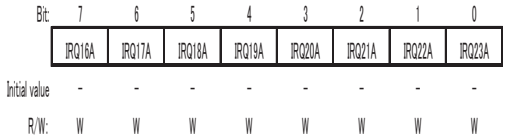
Bit:	7	6	5	4	3	2	1	0
	IRQ 8A	IRQ 9A	IRQ 10A	IRQ 11A	IRQ 12A	IRQ 13A	IRQ 14A	IRQ 15A
Initial value:	-	-	-	-	-	-	-	-
R/W:	W	W	W	W	W	W	W	W

Bit	Bit Name	Initial Value	R/W	Description
7	IRQ8A	—	W	IRQn Interrupt Mask Clear
6	IRQ9A	—	W	0: Writing 0 is ignored
5	IRQ10A	—	W	1: Clears the corresponding interrupt mask
4	IRQ11A	—	W	When reading:
3	IRQ12A	—	W	An undefined value will be read.
2	IRQ13A	—	W	
1	IRQ14A	—	W	
0	IRQ15A	—	W	

[Legend]
n = 8 to 15

(24) Interrupt Mask Clear Register 20A (INTMSKCLR20A)

INTMSKCLR20A is a write-only register that clears the mask settings for interrupts from external interrupt input pins IRQ23 to IRQ16.



Bit:	7	6	5	4	3	2	1	0
	IRQ16A	IRQ17A	IRQ18A	IRQ19A	IRQ20A	IRQ21A	IRQ22A	IRQ23A
Initial value	-	-	-	-	-	-	-	-
R/W:	W	W	W	W	W	W	W	W

Bit	Bit Name	Initial Value	R/W	Description
7	IRQ16A	—	W	IRQn Interrupt Mask Clear
6	IRQ17A	—	W	0: Writing 0 is ignored
5	IRQ18A	—	W	1: Clears the corresponding interrupt mask
4	IRQ19A	—	W	When reading:
3	IRQ20A	—	W	An undefined value will be read.
2	IRQ21A	—	W	
1	IRQ22A	—	W	
0	IRQ23A	—	W	

[Legend]
n = 16 to 23

(25) Interrupt Mask Clear Register 30A (INTMSKCLR30A)

INTMSKCLR30A is a write-only register that clears the mask settings for interrupts from external interrupt input pins IRQ31 to IRQ24.

Bit:	7	6	5	4	3	2	1	0
	IRQ24A	IRQ25A	IRQ26A	IRQ27A	IRQ28A	IRQ29A	IRQ30A	IRQ31A
Initial value:	-	-	-	-	-	-	-	-
R/W:	W	W	W	W	W	W	W	W

Bit	Bit Name	Initial Value	R/W	Description
7	IRQ24A	—	W	IRQn Interrupt Mask Clear
6	IRQ25A	—	W	0: Writing 0 is ignored
5	IRQ26A	—	W	1: Clears the corresponding interrupt mask
4	IRQ27A	—	W	When reading:
3	IRQ28A	—	W	An undefined value will be read.
2	IRQ29A	—	W	
1	IRQ30A	—	W	
0	IRQ31A	—	W	

[Legend]
n = 24 to 31

(26) Peripheral Interrupt Mask Registers 0A to 13A,0A3 to 10A3 (IMR0A to IMR13A,IMR0A3 to IMR10A3)

IMR0A to IMR13A and IMR0A3 to IMR10A3 are registers that mask on-chip peripheral module interrupts. To mask an interrupt, write 1 to the corresponding bit in IMR0A to IMR13A and IMR0A3 to IMR10A3. Peripheral module interrupts not used should be masked.

To clear an interrupt mask, write 1 to the corresponding bit in IMCR0A to IMCR13A and IMR0A3 to IMR10A3. Writing 0 to the corresponding bit in IMR0A to IMR13A and IMR0A3 to IMR10A3 does not affect the bit value.

Table 5.5 shows the correspondence between the bits in IMR0A to IMR13A and IMR0A3 to IMR10A3 and the interrupt sources.

IMR0A to IMR13A:

Bit:	7	6	5	4	3	2	1	0
	IMRn 0A	IMRn 1A	IMRn 2A	IMRn 3A	IMRn 4A	IMRn 5A	IMRn 6A	IMRn 7A
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

IMR0A3 to IMR10A3:

Bit:	7	6	5	4	3	2	1	0
	IMRm 0A3	IMRm 1A3	IMRm 2A3	IMRm 3A3	IMRm 4A3	IMRm 5A3	IMRm 6A3	IMRm 7A3
Initial value	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

IMR0A to IMR13A:

Bit	Bit Name	Initial Value	R/W	Description
7	IMRn0A	0	R/W	Interrupt Mask
6	IMRn1A	0	R/W	Masks the interrupt request corresponding to each bit. See table 5.5 for the correspondence between IMR and each interrupt source.
5	IMRn2A	0	R/W	
4	IMRn3A	0	R/W	When writing:
3	IMRn4A	0	R/W	0: Writing 0 is ignored
2	IMRn5A	0	R/W	1: Masks the corresponding interrupt request
1	IMRn6A	0	R/W	When reading:
0	IMRn7A	0	R/W	0: The corresponding interrupt request is accepted
				1: The corresponding interrupt request is masked

[Legend]
n = 0 to 13

IMR0A3 to IMR10A3:

Bit	Bit Name	Initial Value	R/W	Description
7	IMRm0A3	0	R/W	Interrupt Mask
6	IMRm1A3	0	R/W	Masks the interrupt request corresponding to each bit. See table 5.5 for the correspondence between IMR and each interrupt source.
5	IMRm2A3	0	R/W	
4	IMRm3A3	0	R/W	When writing:
3	IMRm4A3	0	R/W	0: Writing 0 is ignored
2	IMRm5A3	0	R/W	1: Masks the corresponding interrupt request
1	IMRm6A3	0	R/W	When reading:
0	IMRm7A3	0	R/W	0: The corresponding interrupt request is accepted
				1: The corresponding interrupt request is masked

[Legend]
m = 0 to 10

(27) Peripheral Interrupt Mask Clear Registers 0A to 13A, 0A3 to 10A3 (IMCR0A to IMCR13A,IMCR0A3 to IMCR10A3)

IMCR0A to IMCR13A and IMCR0A3 to IMCR10A3 are write-only registers that clear the mask settings for the on-chip peripheral module interrupts. Table 5.5 shows the correspondence between the bits in IMCR0A to IMCR13A and IMCR0A3 to IMCR10A3 and the interrupt sources.

IMCR0A to IMCR13A:

Bit:	7	6	5	4	3	2	1	0
	IMCRn 0A	IMCRn 1A	IMCRn 2A	IMCRn 3A	IMCRn 4A	IMCRn 5A	IMCRn 6A	IMCRn 7A
Initial value:	-	-	-	-	-	-	-	-
R/W:	W	W	W	W	W	W	W	W

IMCR0A3 to IMCR10A3:

Bit:	7	6	5	4	3	2	1	0
	IMCRm 0A3	IMCRm 1A3	IMCRm 2A3	IMCRm 3A3	IMCRm 4A3	IMCRm 5A3	IMCRm 6A3	IMCRm 7A3
Initial value	-	-	-	-	-	-	-	-
R/W:	W	W	W	W	W	W	W	W

IMCR0A to IMCR13A:

Bit	Bit Name	Initial Value	R/W	Description
7	IMCRn0A	—	W	Interrupt Mask Clear
6	IMCRn1A	—	W	Clears the mask setting for the interrupt corresponding to each bit. See table 5.5 for the correspondence between IMCR and each interrupt source.
5	IMCRn2A	—	W	
4	IMCRn3A	—	W	When writing:
3	IMCRn4A	—	W	0: Writing 0 is ignored
2	IMCRn5A	—	W	1: Clears the corresponding interrupt mask
1	IMCRn6A	—	W	When reading:
0	IMCRn7A	—	W	An undefined value will be read.

[Legend]
n = 0 to 13

IMCR0A3 to IMCR10A3:

Bit	Bit Name	Initial Value	R/W	Description
7	IMCRm0A3	—	W	Interrupt Mask Clear
6	IMCRm1A3	—	W	Clears the mask setting for the interrupt corresponding to each bit. See table 5.5 for the correspondence between IMCR and each interrupt source.
5	IMCRm2A3	—	W	
4	IMCRm3A3	—	W	When writing:
3	IMCRm4A3	—	W	0: Writing 0 is ignored
2	IMCRm5A3	—	W	1: Clears the corresponding interrupt mask
1	IMCRm6A3	—	W	When reading:
0	IMCRm7A3	—	W	An undefined value will be read.

[Legend]
m = 0 to 10

(28) Peripheral Interrupt Mask Registers 0AS to 13AS, 0AS3 to 10AS3 (IMR0AS to IMR13AS, IMR0AS3 to IMR10AS3)

IMR0AS to IMR13AS and IMR0AS3 to IMR10AS3 are registers that mask on-chip peripheral module interrupts to be sent to the INTCS. To mask an interrupt, write 1 to the corresponding bit in IMR0AS to IMR13AS and IMR0AS3 to IMR10AS3. Peripheral module interrupts not used should be masked.

To clear an interrupt mask, write 1 to the corresponding bit in IMCR0AS to IMCR13AS. Writing 0 to the corresponding bit in IMR0AS to IMR13AS and IMR0AS3 to IMR10AS3 does not affect the bit value.

Table 5.5 shows the correspondence between the bits in IMR0AS to IMR13AS and IMR0AS3 to IMR10AS3 and the interrupt sources.

IMR0AS to IMR13AS:

Bit:	7	6	5	4	3	2	1	0
	IMRn 0AS	IMRn 1AS	IMRn 2AS	IMRn 3AS	IMRn 4AS	IMRn 5AS	IMRn 6AS	IMRn 7AS
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

IMR0AS3 to IMR10AS3:

Bit:	7	6	5	4	3	2	1	0
	IMRm 0AS3	IMRm 1AS3	IMRm 2AS3	IMRm 3AS3	IMRm 4AS3	IMRm 5AS3	IMRm 6AS3	IMRm 7AS3
Initial value	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	IMRn0AS	0	R/W	Interrupt Mask
6	IMRn1AS	0	R/W	Masks the interrupt request corresponding to each bit. See table 5.5 for the correspondence between IMR and each interrupt source.
5	IMRn2AS	0	R/W	
4	IMRn3AS	0	R/W	When writing:
3	IMRn4AS	0	R/W	0: Writing 0 is ignored
2	IMRn5AS	0	R/W	1: Masks the corresponding interrupt request
1	IMRn6AS	0	R/W	When reading:
0	IMRn7AS	0	R/W	0: The corresponding interrupt request is accepted
				1: The corresponding interrupt request is masked

[Legend]
n = 0 to 13

IMR0AS3 to IMR10AS3:

Bit	Bit Name	Initial Value	R/W	Description
7	IMRm0AS3	0	R/W	Interrupt Mask
6	IMRm1AS3	0	R/W	Masks the interrupt request corresponding to each bit. See table 5.5 for the correspondence between IMR and each interrupt source.
5	IMRm2AS3	0	R/W	
4	IMRm3AS3	0	R/W	When writing:
3	IMRm4AS3	0	R/W	0: Writing 0 is ignored
2	IMRm5AS3	0	R/W	1: Masks the corresponding interrupt request
1	IMRm6AS3	0	R/W	When reading:
0	IMRm7AS3	0	R/W	0: The corresponding interrupt request is accepted
				1: The corresponding interrupt request is masked

[Legend]
n = 0 to 10

(29) Peripheral Interrupt Mask Clear Registers 0AS to 13AS, 0AS3 to 10AS3（IMCR0AS to IMCR13AS,IMCR0AS3 to IMCR10AS3）

IMCR0AS to IMCR13AS and IMCR0AS3 to IMCR10AS3 are write-only registers that clear the mask settings for the on-chip peripheral module interrupts to be sent to the INTCS. Table 5.5

shows the correspondence between the bits in IMCR0AS to IMCR13AS and IMCR0AS3 to IMCR10AS3 and the interrupt sources.

IMCR0AS to IMCR13AS：

Bit:	7	6	5	4	3	2	1	0
	IMCRn 0AS	IMCRn 1AS	IMCRn 2AS	IMCRn 3AS	IMCRn 4AS	IMCRn 5AS	IMCRn 6AS	IMCRn 7AS
Initial value:	-	-	-	-	-	-	-	-
R/W:	W	W	W	W	W	W	W	W

IMCR0AS3 to IMCR10AS3：

Bit:	7	6	5	4	3	2	1	0
	IMCRm 0AS3	IMCRm 1AS3	IMCRm 2AS3	IMCRm 3AS3	IMCRm 4AS3	IMCRm 5AS3	IMCRm 6AS3	IMCRm 7AS3
Initial value	-	-	-	-	-	-	-	-
R/W:	W	W	W	W	W	W	W	W

IMCR0AS to IMCR13AS：

Bit	Bit Name	Initial Value	R/W	Description
7	IMCRn0AS	—	W	Interrupt Mask Clear
6	IMCRn1AS	—	W	Clears the mask setting for the interrupt corresponding to each bit. See table 5.5 for the correspondence between IMCR and each interrupt source.
5	IMCRn2AS	—	W	
4	IMCRn3AS	—	W	When writing:
3	IMCRn4AS	—	W	0: Writing 0 is ignored
2	IMCRn5AS	—	W	1: Clears the corresponding interrupt mask
1	IMCRn6AS	—	W	When reading:
0	IMCRn7AS	—	W	An undefined value will be read.

[Legend]
n = 0 to 13

IMCR0AS3 to IMCR10AS3：

Bit	Bit Name	Initial Value	R/W	Description
7	IMCRm0AS3	—	W	Interrupt Mask Clear
6	IMCRm1AS3	—	W	Clears the mask setting for the interrupt corresponding to each bit. See table 5.5 for the correspondence between IMCR and each interrupt source.
5	IMCRm2AS3	—	W	
4	IMCRm3AS3	—	W	When writing:
3	IMCRm4AS3	—	W	0: Writing 0 is ignored
2	IMCRm5AS3	—	W	1: Clears the corresponding interrupt mask
1	IMCRm6AS3	—	W	When reading:
0	IMCRm7AS3	—	W	An undefined value will be read.

[Legend]
m = 0 to 13

Table 5.5 Correspondence between On-Chip Peripheral Module Interrupt Sources and IMR0A to IMR13A, IMR0A3 to IMR10A3 ,IMCR0A to IMCR13A, IMCR0A3 to IMCR10A3 , IMR0AS to IMR13AS, IMR0AS3 to IMR10AS3 , IMCR0AS to IMCR13AS and IMCR0AS3 to IMCR10AS3

Register Name	Bit Name(Function Name)							
	7	6	5	4	3	2	1	0
IMR0A/IMCR0A	DEI3	DEI2	DEI1	DEI0	IRQPMU	—	COMMTX	COMMRX
IMR0AS/IMCR0AS	(DMAC2(1))				(AP-ARM)			
IMR1A/IMCR1A	—	STD	DIRC	—	DEI3	DEI2	DEI1	DEI0
IMR1AS/IMCR1AS	—	(Crypt)	(INTCA)	—	(DMAC1(1))			
IMR2A/IMCR2A	—	—	—	—	BBIF1	BBIF2	MFIS	ACMFI1/2
IMR2AS/IMCR2AS	(PINTCA)		—	—	(BBIF1)	(BBIF2)	(MFIS)	MFI
IMR3A/IMCR3A	DEI3	DEI2	DEI1	DEI0	DADERR	DEI5	DEI4	IrDA
IMR3AS/IMCR3AS	(DMAC3(1))				(DMAC3(2))			(IrDA)
IMR4A/IMCR4A	DDM	—	—	—	—	—	—	—
IMR4AS/IMCR4AS	(DDM)	—	—	—	—	—	—	
IMR5A/IMCR5A	KEY	DADERR	DEI5	DEI4	SCIFA3	SCIFA2	SCIFA1	SCIFA0
IMR5AS/IMCR5AS	(KEYSC)	(DMAC1(2))			(SCIFA3)	(SCIFA2)	(SCIFA1)	(SCIFA0)
IMR6A/IMCR6A	SCIFB	SCIFA5	SCIFA4	MSIOF1	—	—	MSIOF2	—
IMR6AS/IMCR6AS	(SCIFB)	(SCIFA5)	(SCIFA4)	(MSIOF1)	—	—	(MSIOF2)	—
IMR7A/IMCR7A	SDHI0I3	SDHI0I2	SDHI0I1	SDHI0I0	FLTREQ1I	FLTREQ0I	FLTENDI	FLSTEI

Register Name	Bit Name(Function Name)							
	7	6	5	4	3	2	1	0
IMR7AS/IMCR7AS	(SDHI0)				(FLCTL)			
IMR8A/IMCR8A	–	SDHI1I2	SDHI1I1	SDHI1I0	TTI20*	USHDMI	–	–
IMR8AS/IMCR8AS	(SDHI1)				(TTI20)	(USBHSDMAC)	–	–
IMR9A/IMCR9A	CMT13	CMT12	CMT11	CMT10	CMT2	–	–	SGX540
IMR9AS/IMCR9AS	(CMT1)				(CMT2)	–		(3DG)
IMR10A/IMCR10A	–	DADERR	DEI5	DEI4	–	–	–	–
IMR10AS/IMCR10AS	–	(DMAC2(2))			–	–	–	–
IMR11A/IMCR11A	DTEI1	WAITI1	TACKI1	ALI1	–	–	–	–
IMR11AS/IMCR11AS	(IIC1)				–	(MSU)	–	–
IMR12A/IMCR12A	–	–	TPU0	–	–	–	–	–
IMR12AS/IMCR12AS	–	–	(TPU0)	–	–	–	–	–
IMR13A/IMCR13A IMR13AS/IMCR13AS	SDHI2I3	SDHI2I2	SDHI2I1	SDHI2I0	–	CMT3	–	RWDT0
	SDHIF2				–)	(CMT3)	–	(RWDT0)
IMR0A3/IMCR0A3 IMR0AS3/IMCR0AS3	SHWYSTAT(RT)	SHWYSTAT(HS)	SHWYSTAT(Com)	–	–	–	–	–
	SHWYSTAT			–	–	–	–	–
IMR1A3/IMCR1A3	–	–	–	–	–	–	–	–
IMR1AS3/IMCR1AS3	–	–	–	–	–	–	–	–
IMR2A3/IMCR2A3	–	–	–	–	–	–	–	–
IMR2AS3/IMCR2AS3	–	–	–	–	–	–	–	–
IMR3A3/IMCR3A3	–	–	–	–	–	–	–	–
IMR3AS3/IMCR3AS3	–	–	–	–	–	–	–	–
IMR4A3/IMCR4A3	–	–	–	–	–	–	–	HDMI
IMR4AS3/IMCR4AS3	–		–	–	–	–	–	(HDMI)
IMR5A3/IMCR5A3	SPU0	SPU1	FSI	FMSI	–	–	–	MIPI-HSI
IMR5AS3/IMCR5AS3	SPU2		FSI	FMSI	–	–	–	(MIPI-HSI)
IMR6A3/IMCR6A3 IMR6AS3/IMCR6AS3	–	IPMMUD	CEC_1	CEC_2	CTIIRQ	DMAEXTERRIRQ	DMAIRQ	DMASIRQ
	–	IPMMUD	(CEC)		AP-ARM			
IMR7A3/IMCR7A3 IMR7AS3/IMCR7AS3	MFIS2	CPORTR2S	CMT14	CMT15	–	–	MMC_ERR	MMC_NOR
	MFIS2	CPORTR2S	CMT14	CMT15	–	(MMC)		

Register Name	Bit Name(Function Name)							
	7	6	5	4	3	2	1	0
IMR8A3/IMCR8A3	ALI 4	TACKI 4	WAITI 4	DTEI 4	ALI 3	TACKI3	WAITI 3	DTEI 3
IMR8AS3/IMCR8AS3	(I2C(4))				(I2C(3))			
IMR9A3/IMCR9A3	—	—	—	—	USBI1 (ch0)	USBI0 (ch0)	USBI1 (ch1)	USBI0 (ch1)
IMR9AS3/IMCR9AS3	—				(USB0)		(USB1)	
IMR10A3/IMCR10A3	USHDMI	—	—	—	—	—	—	—
IMR10AS3/IMCR10AS3	(USBHSDMAC1)	—	—	—	—	—	—	—

Note: —: Reserved. An undefined value will be read. Writing is ignored.

* Bit 3 of IMR8AS/IMCR8AS is reserved. In the AP-Realtime core, the TTI20 interrupt should be handled directly by the INTCS.

(30) User Interrupt Mask Level Register A (USERIMASKA)

USERIMASKA is a register that specifies the level of interrupts to be accepted. As this register is allocated to a 64-Kbyte page that differs from the area of the other INTCA registers, only USERIMASKA can be accessed in user mode by translating its address to the domain that can be accessed in user mode through the MMU.

When the level of an interrupt is not higher than the interrupt level specified in the UIMASKA bit, the interrupt is masked. Specifying H'F masks all interrupts except for NMI. The interrupt with a higher level than that specified in the UIMASKA bit is accepted only when the corresponding interrupt mask bit in the interrupt mask register is 0 (interrupt enabled) and the INTLVLA setting is lower than the level of that interrupt. The UIMASKA value does not change even after an interrupt is accepted.

This register is initialized to H'00000000 (all interrupts enabled) by a power-on reset. To prevent unintentional modification, this register can only be written to with bits 31 to 24 set to H'A5.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	UIMASKA				-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R/W	Reserved These bits are always read as 0. Be sure to write H'A5 to these bits when writing to the UIMASKA bit.
23 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 4	UIMASKA	H'0	R/W	User Interrupt Mask Level The interrupt is masked when the level of an interrupt is not higher than this value.
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

(31) AP-Realtime Core Individual Interrupt Source Register (INTEVTAS)

INTEVTAS is a read-only register that indicates the code for the source of the interrupt sent from each peripheral module to the AP-Realtime core.

For the interrupt source code, refer to the list of INTCA interrupt sources (table 5.11). The interrupt signals from the peripheral modules assigned to the INTCA are combined into one signal, and this signal is sent to the INTCS as a peripheral interrupt. The code for this interrupt signal is H'FE0 as shown in the list of INTCS interrupt sources (table 5.13). When the AP-Realtime core accepts this interrupt, the AP-Realtime core can process the peripheral interrupt assigned to the INTCA by reading this register within the AP-Realtime interrupt handler.

The interrupt signal sent from the INTCA to the AP-Realtime core can be masked by the INTAMASK setting.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	EVTCODEAS									-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13 to 5	EVTCODEAS	H'02F	R	Interrupt Code These bits hold the interrupt code. For details, see table 5.11.
4 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

(32) AP-Realtime Core Interrupt Mask Register (INTSMASK)

INTSMASK indicates whether to mask all interrupts sent to the AP-System core from the peripheral modules on the INTCS side. INTSMASK is located in the INTCA and controlled by the AP-System core. When the MASK bit in this register is set to 1, no interrupts are sent to the AP-System core regardless of the IMCR*SA setting.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	MASK
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	MASK	0	R/W	Interrupt Mask Indicates masking of interrupt requests sent to the AP-System core. When reading: 0: Interrupt requests are not masked 1: Interrupt requests are masked

(33) FIQ status register A (FIQSRA)

FIQSRA is a read-only register. FIQ interrupt can be confirmed by reading this register when ARM-FIQ interrupt.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NMIL	-	-	-	-	-	-	-	-	-	-	-	-	CRYFL	CMT 3FL	NMIFL
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	CC5FL	0	R	CC5 Interrupt Request Detection Indicates whether a CC5 interrupt request signal has been detected. This is a read-only bit. 0: CC5 interrupt request has not been detected 1: CC5 interrupt request has been detected
1	CMT3FL	0	R	CMT3 Interrupt Request Detection Indicates whether a CMT3 interrupt request signal has been detected. This is a read-only bit. 0: CMT3 interrupt request has not been detected 1: CMT3 interrupt request has been detected
0	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.

(34) IRQ Status Check Register 0(ISCR0)

ISCR0 has bits that can monitor the status of the IRQ pins and a block bit (FIQBL) that can mask the NMI pin interrupt. When the FIQBL bit is set to 1, the FIQ interrupt sent to the AP-System core can be masked but this does not affect the operation of the NMIFCRA.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	FIQBL
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SC0	SC1	SC2	SC3	SC4	SC5	SC6	SC7	SC8	SC9	SC10	SC11	SC12	SC13	SC14	SC15
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. To prevent unintentional modification, the write value should always be 1010 0101 0101 1010.
15	SC0	X	R	IRQ0 Pin Status Check 0: Low-level input to the IRQ0 pin 1: High-level input to the IRQ0 pin
14	SC1	X	R	IRQ1 Pin Status Check 0: Low-level input to the IRQ1 pin 1: High-level input to the IRQ1 pin
13	SC2	X	R	IRQ2 Pin Status Check 0: Low-level input to the IRQ2 pin 1: High-level input to the IRQ2 pin
12	SC3	X	R	IRQ3 Pin Status Check 0: Low-level input to the IRQ3 pin 1: High-level input to the IRQ3 pin
11	SC4	X	R	IRQ4 Pin Status Check 0: Low-level input to the IRQ4 pin 1: High-level input to the IRQ4 pin

10	SC5	X	R	IRQ5 Pin Status Check 0: Low-level input to the IRQ5 pin 1: High-level input to the IRQ5 pin
9	SC6	X	R	IRQ6 Pin Status Check 0: Low-level input to the IRQ6 pin 1: High-level input to the IRQ6 pin
8	SC7	X	R	IRQ7 Pin Status Check 0: Low-level input to the IRQ7 pin 1: High-level input to the IRQ7 pin
7	SC8	X	R	IRQ8 Pin Status Check 0: Low-level input to the IRQ8 pin 1: High-level input to the IRQ8 pin
6	SC9	X	R	IRQ9 Pin Status Check 0: Low-level input to the IRQ9 pin 1: High-level input to the IRQ9 pin

Bit	Bit Name	Initial Value	R/W	Description
5	SC10	X	R	IRQ10 Pin Status Check 0: Low-level input to the IRQ10 pin 1: High-level input to the IRQ10 pin

Bit	Bit Name	Initial Value	R/W	Description
4	SC11	X	R	IRQ11 Pin Status Check 0: Low-level input to the IRQ11 pin 1: High-level input to the IRQ11 pin
3	SC12	X	R	IRQ12 Pin Status Check 0: Low-level input to the IRQ12 pin 1: High-level input to the IRQ12 pin
2	SC13	X	R	IRQ13 Pin Status Check 0: Low-level input to the IRQ13 pin 1: High-level input to the IRQ13 pin
1	SC14	X	R	IRQ14 Pin Status Check 0: Low-level input to the IRQ14 pin 1: High-level input to the IRQ14 pin
0	SC15	x	R	IRQ15 Pin Status Check 0: Low-level input to the IRQ15 pin 1: High-level input to the IRQ15 pin

(35) IRQ Status Check Register 1(ISCR1)

ISCR1 has bits that can monitor the status of the IRQ pins.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SC0	SC1	SC2	SC3	SC4	SC5	SC6	SC7	SC8	SC9	SC10	SC11	SC12	SC13	SC14	SC15
Initial value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SC16	SC17	SC18	SC19	SC20	SC21	SC22	SC23	SC24	SC25	SC26	SC27	SC28	SC29	SC30	SC31
initial value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	SC0	X	R	IRQ0 Pin Status Check 0: Low-level input to the IRQ0 pin 1: High-level input to the IRQ0 pin
30	SC1	X	R	IRQ1 Pin Status Check 0: Low-level input to the IRQ1 pin 1: High-level input to the IRQ1 pin
29	SC2	X	R	IRQ2 Pin Status Check 0: Low-level input to the IRQ2 pin 1: High-level input to the IRQ2 pin
28	SC3	X	R	IRQ3 Pin Status Check 0: Low-level input to the IRQ3 pin 1: High-level input to the IRQ3 pin
27	SC4	X	R	IRQ4 Pin Status Check 0: Low-level input to the IRQ4 pin 1: High-level input to the IRQ4 pin
26	SC5	X	R	IRQ5 Pin Status Check 0: Low-level input to the IRQ5 pin 1: High-level input to the IRQ5 pin
25	SC6	X	R	IRQ6 Pin Status Check 0: Low-level input to the IRQ6 pin 1: High-level input to the IRQ6 pin

24	SC7	X	R	IRQ7 Pin Status Check 0: Low-level input to the IRQ7 pin 1: High-level input to the IRQ7 pin
23	SC8	X	R	IRQ8 Pin Status Check 0: Low-level input to the IRQ8 pin 1: High-level input to the IRQ8 pin
22	SC9	X	R	IRQ9 Pin Status Check 0: Low-level input to the IRQ9 pin 1: High-level input to the IRQ9 pin
21	SC10	X	R	IRQ10 Pin Status Check 0: Low-level input to the IRQ10 pin 1: High-level input to the IRQ10 pin
20	SC11	X	R	IRQ11 Pin Status Check 0: Low-level input to the IRQ11 pin 1: High-level input to the IRQ11 pin
19	SC12	X	R	IRQ12 Pin Status Check 0: Low-level input to the IRQ12 pin 1: High-level input to the IRQ12 pin
18	SC13	X	R	IRQ13 Pin Status Check 0: Low-level input to the IRQ13 pin 1: High-level input to the IRQ13 pin
17	SC14	X	R	IRQ14 Pin Status Check 0: Low-level input to the IRQ14 pin 1: High-level input to the IRQ14 pin
16	SC15	X	R	IRQ15 Pin Status Check 0: Low-level input to the IRQ15 pin 1: High-level input to the IRQ15 pin
15	SC16	X	R	IRQ16 Pin Status Check 0: Low-level input to the IRQ16 pin 1: High-level input to the IRQ16 pin
14	SC17	X	R	IRQ17 Pin Status Check 0: Low-level input to the IRQ17 pin 1: High-level input to the IRQ17 pin

13	SC18	X	R	IRQ18 Pin Status Check 0: Low-level input to the IRQ18 pin 1: High-level input to the IRQ18 pin
12	SC19	X	R	IRQ19 Pin Status Check 0: Low-level input to the IRQ19 pin 1: High-level input to the IRQ19 pin
11	SC20	X	R	IRQ20 Pin Status Check 0: Low-level input to the IRQ20 pin 1: High-level input to the IRQ20 pin
10	SC21	X	R	IRQ21 Pin Status Check 0: Low-level input to the IRQ21 pin 1: High-level input to the IRQ21 pin
9	SC22	X	R	IRQ22 Pin Status Check 0: Low-level input to the IRQ22 pin 1: High-level input to the IRQ22 pin
8	SC23	X	R	IRQ23 Pin Status Check 0: Low-level input to the IRQ23 pin 1: High-level input to the IRQ23 pin
7	SC24	X	R	IRQ24 Pin Status Check 0: Low-level input to the IRQ24 pin 1: High-level input to the IRQ24 pin
6	SC25	X	R	IRQ25 Pin Status Check 0: Low-level input to the IRQ25 pin 1: High-level input to the IRQ25 pin
5	SC26	X	R	IRQ26 Pin Status Check 0: Low-level input to the IRQ26 pin 1: High-level input to the IRQ26 pin
4	SC27	X	R	IRQ27 Pin Status Check 0: Low-level input to the IRQ27 pin 1: High-level input to the IRQ27 pin
3	SC28	X	R	IRQ28 Pin Status Check 0: Low-level input to the IRQ28 pin 1: High-level input to the IRQ28 pin

2	SC29	X	R	IRQ29 Pin Status Check 0: Low-level input to the IRQ29 pin 1: High-level input to the IRQ29 pin
1	SC30	X	R	IRQ30 Pin Status Check 0: Low-level input to the IRQ30 pin 1: High-level input to the IRQ30 pin
0	SC31	X	R	IRQ31 Pin Status Check 0: Low-level input to the IRQ31 pin 1: High-level input to the IRQ31 pin

Pulse Interrupt Flag Register 0A (IFLG0A)

IFLG0A is a register that has a flag bit for indicating the TTI20 interrupt request to the AP-System core. This bit does not change when the TTI20 interrupt is masked with IMR8A.

The interrupt request can be cleared by writing 0 to the TTI20 bit after reading TTI20 = 1.

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	TTI20
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	TTI20	0	R/W	TTI20 Interrupt Request Indicates a TTI20 interrupt request. When reading: 0: No TTI20 interrupt has been requested to the AP-System core 1: A TTI20 interrupt request has been requested to the AP-System core When writing: 0: Cleared to 0 only after reading 1 1: Writing 1 is ignored

(36) Pseudo-Interrupt Setting Register 0A (SIR0A)

SIR0A is a register to generate an interrupt from a source that is different from the usual one in a specific interrupt.

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	TTI20
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	TTI20	0	R/W	TTI20 Pseudo-Interrupt Setting This bit can be used to debug the TTI20 interrupt routine when the BB side is stopped. 0: TTI20 interrupt 1: RCLK/512 is changed to a TTI20 interrupt detection signal

(37) DIRC Interrupt Setting Register (DIRCR)

DIRCR is a register to generate an interrupt when a specific bit is set to 1.

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	DIRC
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	DIRC	0	R/W	DIRC Interrupt Setting 0: DIRC interrupt is not generated 1: DIRC interrupt is generated

(38) Secure control register (LIFEC_SEC_SRC)

LIFEC_SEC_SRC is register that control interrupt from IP of CIPHER.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	CC5	–	–	–
Initial value:	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31～5	—	All 1	R	These bits are always read as 0. The write value should always be 0.
4	—	1	R/W	Don’t write this bit 0.
3	CC5INT	1	R/W	CC5 interrupt setting 0: CC5 is issued to AP-System core as usual interrupt 1: CC5 is issued to AP-System core as FIQ (fast interrupt)
2～0	—	All 1	R/W	Don’t write this bit 0.

5.3.2 INTCS Register Configuration

Table 5.6 shows the INTCS register configuration. Table 5.7 shows the register states in each operating mode.

Table 5.6 Register Configuration

Register Name	Abbreviation	R/W	Address	Access Size
Interrupt control register 0S	ICR0S	R/W	H'FFD1 0000	32
Interrupt control register 1S	ICR1S	R/W	H'FFD1 0004	32
Interrupt control register 2S	ICR2S	R/W	H'FFD1 0008	32
Interrupt control register 3S	ICR3S	R/W	H'FFD1 000C	32
Interrupt control register 3	ICR3	R/W	H'E605 8040	32
Interrupt control register 4	ICR4	R/W	H'E605 8044	32
Interrupt control register 5	ICR5	R/W	H'E605 8048	32
Interrupt control register 6	ICR6	R/W	H'E605 804C	32
Interrupt control register 7	ICR7	R/W	H'E605 8050	32
Interrupt control register 8	ICR8	R/W	H'E605 8054	32
Interrupt control register 9	ICR9	R/W	H'E605 8058	32
Interrupt control register 10	ICR10	R/W	H'E605 805C	32
Interrupt priority register 00S	INTPRI00S	R/W	H'FFD1 0010	32
Interrupt priority register 10S	INTPRI10S	R/W	H'FFD1 0014	32
Interrupt priority register 20S	INTPRI20S	R/W	H'FFD1 0018	32
Interrupt priority register 30S	INTPRI30S	R/W	H'FFD1 001C	32
Interrupt source register 00S	INTREQ00S	R/W	H'FFD1 0020	8
Interrupt source register 10S	INTREQ10S	R/W	H'FFD1 0024	8
Interrupt source register 20S	INTREQ20S	R/W	H'FFD1 0028	8
Interrupt source register 30S	INTREQ30S	R/W	H'FFD1 002C	8
Interrupt mask register 00S	INTMSK00S	R/W	H'FFD1 0040	8
Interrupt mask register 10S	INTMSK10S	R/W	H'FFD1 0044	8
Interrupt mask register 20S	INTMSK20S	R/W	H'FFD1 0048	8
Interrupt mask register 30S	INTMSK30S	R/W	H'FFD1 004C	8
Interrupt mask clear register 00S	INTMSKCLR00S	W	H'FFD1 0060	8
Interrupt mask clear register 10S	INTMSKCLR10S	W	H'FFD1 0064	8

Interrupt mask clear register 20S	INTMSKCLR20S	W	H'FFD1 0068	8
Interrupt mask clear register 30S	INTMSKCLR30S	W	H'FFD1 006C	8
AP-System core individual interrupt source register	INTEVTSA	R	H'FFD2 0100	32
NMI flag control register S	NMIFCRS	R/W	H'FFD3 00C0	16
AP-System core interrupt mask register	INTAMASK	R/W	H'FFD2 0104	16
User interrupt mask level register S	USERIMASKS	R/W	H'FFD4 0000	32
Peripheral interrupt priority register AS	IPRAS	R/W	H'FFD2 0000	16
Peripheral interrupt priority register BS	IPRBS	R/W	H'FFD2 0004	16
Peripheral interrupt priority register CS	IPRCS	R/W	H'FFD2 0008	16
Peripheral interrupt priority register DS	IPRDS	R/W	H'FFD2 000C	16
Peripheral interrupt priority register ES	IPRES	R/W	H'FFD2 0010	16
Peripheral interrupt priority register FS	IPRFS	R/W	H'FFD2 0014	16

Register Name	**Abbreviation**	**R/W**	**Address**	**Access Size**
Peripheral interrupt priority register GS	IPRGS	R/W	H'FFD2 0018	16
Peripheral interrupt priority register HS	IPRHS	R/W	H'FFD2 001C	16
Peripheral interrupt priority register IS	IPRIS	R/W	H'FFD2 0020	16
Peripheral interrupt priority register JS	IPRJS	R/W	H'FFD2 0024	16
Peripheral interrupt priority register KS	IPRKS	R/W	H'FFD2 0028	16
Peripheral interrupt priority register LS	IPRLS	R/W	H'FFD2 002C	16
Peripheral interrupt priority register MS	IPRMS	R/W	H'FFD2 0030	16
Peripheral interrupt priority register AS3	IPRAS3	R/W	H'FFD5 0000	16
Peripheral interrupt priority register BS3	IPRBS3	R/W	H'FFD5 0004	16
Peripheral interrupt priority register CS3	IPRCS3	R/W	H'FFD5 0008	16
Peripheral interrupt priority register DS3	IPRDS3	R/W	H'FFD5 000C	16
Peripheral interrupt priority register ES3	IPRES3	R/W	H'FFD5 0010	16
Peripheral interrupt priority register FS3	IPRFS3	R/W	H'FFD5 0014	16
Peripheral interrupt priority register GS3	IPRGS3	R/W	H'FFD5 0018	16
Peripheral interrupt priority register HS3	IPRHS3	R/W	H'FFD5 001C	16
Peripheral interrupt priority register IS3	IPRIS3	R/W	H'FFD5 0020	16
Peripheral interrupt priority register JS3	IPRJS3	R/W	H'FFD5 0024	16
Peripheral interrupt priority register KS3	IPRKS3	R/W	H'FFD5 0028	16

Peripheral interrupt priority register LS3	IPRLS3	R/W	H'FFD5 002C	16
Peripheral interrupt priority register MS3	IPRMS3	R/W	H'FFD5 0030	16
Peripheral interrupt priority register NS3	IPRNS3	R/W	H'FFD5 0034	16
Peripheral interrupt priority register OS3	IPROS3	R/W	H'FFD5 0038	16
Peripheral interrupt priority register PS3	IPRPS3	R/W	H'FFD5003C	16
Peripheral interrupt mask register 0S	IMR0S	R/W	H'FFD2 0080	8
Peripheral interrupt mask register 1S	IMR1S	R/W	H'FFD2 0084	8
Peripheral interrupt mask register 2S	IMR2S	R/W	H'FFD2 0088	8
Peripheral interrupt mask register 3S	IMR3S	R/W	H'FFD2 008C	8
Peripheral interrupt mask register 4S	IMR4S	R/W	H'FFD2 0090	8
Peripheral interrupt mask register 5S	IMR5S	R/W	H'FFD2 0094	8
Peripheral interrupt mask register 6S	IMR6S	R/W	H'FFD2 0098	8
Peripheral interrupt mask register 7S	IMR7S	R/W	H'FFD2 009C	8
Peripheral interrupt mask register 8S	IMR8S	R/W	H'FFD2 00A0	8
Peripheral interrupt mask register 9S	IMR9S	R/W	H'FFD2 00A4	8
Peripheral interrupt mask register 10S	IMR10S	R/W	H'FFD2 00A8	8
Peripheral interrupt mask register 11S	IMR11S	R/W	H'FFD2 00AC	8
Peripheral interrupt mask register 12S	IMR12S	R/W	H'FFD2 00B0	8
Peripheral interrupt mask register 0S3	IMR0S3	R/W	H'FFD5 0080	8
Peripheral interrupt mask register 1S3	IMR1S3	R/W	H'FFD5 0084	8
Peripheral interrupt mask register 2S3	IMR2S3	R/W	H'FFD5 0088	8
Peripheral interrupt mask register 3S3	IMR3S3	R/W	H'FFD5 008C	8
Peripheral interrupt mask register 4S3	IMR4S3	R/W	H'FFD5 0090	8
Peripheral interrupt mask register 5S3	IMR5S3	R/W	H'FFD5 0094	8
Peripheral interrupt mask register 6S3	IMR6S3	R/W	H'FFD5 0098	8
Peripheral interrupt mask register 7S3	IMR7S3	R/W	H'FFD5 009C	8
Peripheral interrupt mask clear register 0S	IMCR0S	W	H'FFD2 00C0	8
Peripheral interrupt mask clear register 1S	IMCR1S	W	H'FFD2 00C4	8
Peripheral interrupt mask clear register 2S	IMCR2S	W	H'FFD2 00C8	8
Peripheral interrupt mask clear register 3S	IMCR3S	W	H'FFD2 00CC	8
Peripheral interrupt mask clear register 4S	IMCR4S	W	H'FFD2 00D0	8
Peripheral interrupt mask clear register 5S	IMCR5S	W	H'FFD2 00D4	8
Peripheral interrupt mask clear register 6S	IMCR6S	W	H'FFD2 00D8	8

Peripheral interrupt mask clear register 7S	IMCR7S	W	H'FFD2 00DC	8
Peripheral interrupt mask clear register 8S	IMCR8S	W	H'FFD2 00E0	8
Peripheral interrupt mask clear register 9S	IMCR9S	W	H'FFD2 00E4	8

Register Name	Abbreviation	R/W	Address	Access Size
Peripheral interrupt mask clear register 10S	IMCR10S	W	H'FFD2 00E8	8
Peripheral interrupt mask clear register 11S	IMCR11S	W	H'FFD2 00EC	8
Peripheral interrupt mask clear register 12S	IMCR12S	W	H'FFD2 00F0	8
Peripheral interrupt mask clear register 0S3	IMCR0S3	W	H'FFD5 00C0	8
Peripheral interrupt mask clear register 1S3	IMCR1S3	W	H'FFD5 00C4	8
Peripheral interrupt mask clear register 2S3	IMCR2S3	W	H'FFD5 00C8	8
Peripheral interrupt mask clear register 3S3	IMCR3S3	W	H'FFD5 00CC	8
Peripheral interrupt mask clear register 4S3	IMCR4S3	W	H'FFD5 00D0	8
Peripheral interrupt mask clear register 5S3	IMCR5S3	W	H'FFD5 00D4	8
Peripheral interrupt mask clear register 6S3	IMCR6S3	W	H'FFD5 00D8	8
Peripheral interrupt mask clear register 7S3	IMCR7S3	W	H'FFD5 00DC	8
Peripheral interrupt mask register 0SA	IMR0SA	R/W	H'FFD2 0180	8
Peripheral interrupt mask register 1SA	IMR1SA	R/W	H'FFD2 0184	8
Peripheral interrupt mask register 2SA	IMR2SA	R/W	H'FFD2 0188	8

Peripheral interrupt mask register 3SA	IMR3SA	R/W	H'FFD2 018C	8
Peripheral interrupt mask register 4SA	IMR4SA	R/W	H'FFD2 0190	8
Peripheral interrupt mask register 5SA	IMR5SA	R/W	H'FFD2 0194	8
Peripheral interrupt mask register 6SA	IMR6SA	R/W	H'FFD2 0198	8
Peripheral interrupt mask register 7SA	IMR7SA	R/W	H'FFD2 019C	8
Peripheral interrupt mask register 8SA	IMR8SA	R/W	H'FFD2 01A0	8
Peripheral interrupt mask register 9SA	IMR9SA	R/W	H'FFD2 01A4	8
Peripheral interrupt mask register 10SA	IMR10SA	R/W	H'FFD2 01A8	8
Peripheral interrupt mask register 11SA	IMR11SA	R/W	H'FFD2 01AC	8
Peripheral interrupt mask register 12SA	IMR12SA	R/W	H'FFD2 01B0	8
Peripheral interrupt mask register 0SA3	IMR0SA3	R/W	H'FFD5 0180	8
Peripheral interrupt mask register 1SA3	IMR1SA3	R/W	H'FFD5 0184	8
Peripheral interrupt mask register 2SA3	IMR2SA3	R/W	H'FFD5 0188	8
Peripheral interrupt mask register 3SA3	IMR3SA3	R/W	H'FFD5 018C	8
Peripheral interrupt mask register 4SA3	IMR4SA3	R/W	H'FFD5 0190	8
Peripheral interrupt mask register 5SA3	IMR5SA3	R/W	H'FFD5 0194	8
Peripheral interrupt mask register 6SA3	IMR6SA3	R/W	H'FFD5 0198	8
Peripheral interrupt mask register 7SA3	IMR7SA3	R/W	H'FFD5 019C	8
Peripheral interrupt mask clear register 0SA	IMCR0SA	W	H'FFD2 01C0	8
Peripheral interrupt mask clear register 1SA	IMCR1SA	W	H'FFD2 01C4	8
Peripheral interrupt mask clear register 2SA	IMCR2SA	W	H'FFD2 01C8	8
Peripheral interrupt mask clear register 3SA	IMCR3SA	W	H'FFD2 01CC	8
Peripheral interrupt mask clear register 4SA	IMCR4SA	W	H'FFD2 01D0	8
Peripheral interrupt mask clear register 5SA	IMCR5SA	W	H'FFD2 01D4	8
Peripheral interrupt mask clear register 6SA	IMCR6SA	W	H'FFD2 01D8	8
Peripheral interrupt mask clear register 7SA	IMCR7SA	W	H'FFD2 01DC	8
Peripheral interrupt mask clear register 8SA	IMCR8SA	W	H'FFD2 01E0	8
Peripheral interrupt mask clear register 9SA	IMCR9SA	W	H'FFD2 01E4	8
Peripheral interrupt mask clear register 10SA	IMCR10SA	W	H'FFD2 01E8	8
Peripheral interrupt mask clear register 11SA	IMCR11SA	W	H'FFD2 01EC	8
Peripheral interrupt mask clear register 12SA	IMCR12SA	W	H'FFD2 01F0	8
Peripheral interrupt mask clear register 0SA3	IMCR0SA3	W	H'FFD5 01C0	8
Peripheral interrupt mask clear register 1SA3	IMCR1SA3	W	H'FFD5 01C4	8

Peripheral interrupt mask clear register 2SA3	IMCR2SA3	W	H'FFD5 01C8	8
Peripheral interrupt mask clear register 3SA3	IMCR3SA3	W	H'FFD5 01CC	8
Peripheral interrupt mask clear register 4SA3	IMCR4SA3	W	H'FFD5 01D0	8
Peripheral interrupt mask clear register 5SA3	IMCR5SA3	W	H'FFD5 01D4	8
Peripheral interrupt mask clear register 6SA3	IMCR6SA3	W	H'FFD5 01D8	8
Peripheral interrupt mask clear register 7SA3	IMCR7SA3	W	H'FFD5 01DC	8
Pulse interrupt flag register 0S	IFLG0S	R/W	H'FFD2 0110	8
Pseudo-interrupt register 0S	SIR0S	R/W	H'FFD2 0114	8

Table 5.7 Register States in Each Operating Mode

Abbreviation	Reset *	Module Standby
ICR0S to ICR3S	Initialized	Retained
INTPRI00S to INTPR30S	Initialized	Retained
INTREQ00S to INTREQ30S	Initialized	Retained
INTMSK00S to INTMSK 30S	Initialized	Retained
INTMSKCLR00S to INTMSKCLR30S	—	—
NMIFCRS	Initialized	Retained
INTEVTSA	Initialized	Retained
INTAMASK	Initialized	Retained
USERIMASKS	Initialized	Retained
IPRAS to IPRMS, IPRAS3 to IPRPS3	Initialized	Retained
IMR0S to IMR12S, IMR0S3 to IMR7S3	Initialized	Retained
IMCR0S to IMCR12S, IMCR0S3 to IMCR7S3	—	—
IMR0SA to IMR12SA, IMR0SA3 to IMR7SA3	Initialized	Retained
IMCR0SA to IMCR12SA, IMCR0SA3 to IMCR7SA3	—	—
IFLG0S	Initialized	Retained
ICR3 to ICR10	Initialized	Retained

Note: * For details, refer to section 1-D Overview of reset.

(1) Interrupt Control Register 0S (ICR0S)

ICR0S specifies the detection mode for external interrupt input pins IRQ7 to IRQ0 individually: rising edge, falling edge, low level, or high level.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IRQ0SS				IRQ1SS				IRQ2SS				IRQ3SS			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IRQ4SS				IRQ5SS				IRQ6SS				IRQ7SS			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	IRQ0SS	0000	R/W	IRQn Sense Select
27 to 24	IRQ1SS	0000	R/W	These bits select whether interrupt request signals from pins IRQ7 to IRQ0 are detected at a rising edge, a falling edge, a low level, a high level, or at both of a rising edge and a falling edge.
23 to 20	IRQ2SS	0000	R/W	
19 to 16	IRQ3SS	0000	R/W	
15 to 12	IRQ4SS	0000	R/W	
11 to 8	IRQ5SS	0000	R/W	
7 to 4	IRQ6SS	0000	R/W	
3 to 0	IRQ7SS	0000	R/W	

IRQnSS	Detection Mode
0000	Interrupt request is detected at a falling edge of IRQn input
0001	Interrupt request is detected at a rising edge of IRQn input
0010	Interrupt request is detected at a low level of IRQn input
0011	Interrupt request is detected at a high level of IRQn input
0100	Interrupt request is detected at both edges of IRQn input

[Legend]
n = 0 to 7

(2) Interrupt Control Register 1S (ICR1S)

ICR1S specifies the detection mode for external interrupt input pins IRQ15 to IRQ8 individually: rising edge, falling edge, low level, or high level.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IRQ8SS				IRQ9SS				IRQ10SS				IRQ11SS			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IRQ12SS				IRQ13SS				IRQ14SS				IRQ15SS			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

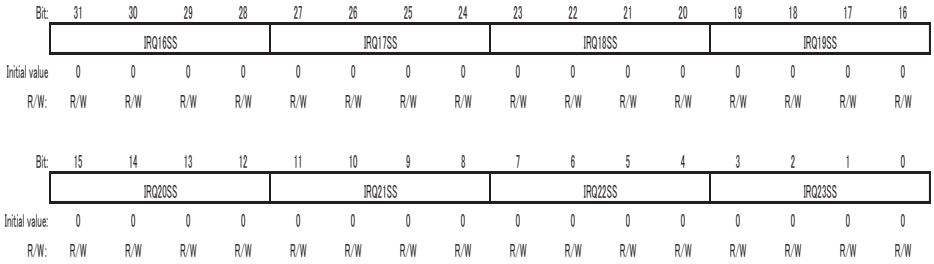
Bit	Bit Name	Initial Value	R/W	Description
31 to 28	IRQ8SS	0000	R/W	IRQn Sense Select
27 to 24	IRQ9SS	0000	R/W	These bits select whether interrupt request signals from pins IRQ8 to IRQ15 are detected at a rising edge, a falling edge, a low level, a high level, or at both of a rising edge and a falling edge.
23 to 20	IRQ10SS	0000	R/W	
19 to 16	IRQ11SS	0000	R/W	
15 to 12	IRQ12SS	0000	R/W	
11 to 8	IRQ13SS	0000	R/W	
7 to 4	IRQ14SS	0000	R/W	
3 to 0	IRQ15SS	0000	R/W	

IRQnSS	Detection Mode
0000	Interrupt request is detected at a falling edge of IRQn input
0001	Interrupt request is detected at a rising edge of IRQn input
0010	Interrupt request is detected at a low level of IRQn input
0011	Interrupt request is detected at a high level of IRQn input
0100	Interrupt request is detected at both edges of IRQn input

[Legend]
n = 8 to 15

(3) Interrupt Control Register 2S (ICR2S)

ICR2S specifies the detection mode for external interrupt input pins IRQ23 to IRQ16 individually: rising edge, falling edge, low level, or high level.



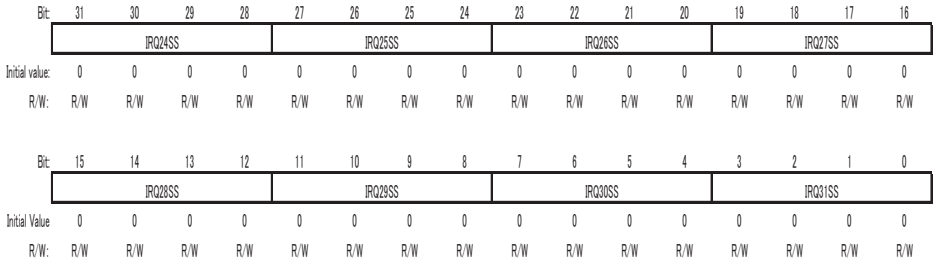
Bit	Bit Name	Initial Value	R/W	Description
31 to 28	IRQ16SS	0000	R/W	IRQn Sense Select
27 to 24	IRQ17SS	0000	R/W	These bits select whether interrupt request signals from pins IRQ16 to IRQ23 are detected at a rising edge, a falling edge, a low level, a high level, or at both of a rising edge and a falling edge.
23 to 20	IRQ18SS	0000	R/W	
19 to 16	IRQ19SS	0000	R/W	
15 to 12	IRQ20SS	0000	R/W	
11 to 8	IRQ21SS	0000	R/W	
7 to 4	IRQ22SS	0000	R/W	
3 to 0	IRQ23SS	0000	R/W	

IRQnSS	Detection Mode
0000	Interrupt request is detected at a falling edge of IRQn input
0001	Interrupt request is detected at a rising edge of IRQn input
0010	Interrupt request is detected at a low level of IRQn input
0011	Interrupt request is detected at a high level of IRQn input
0100	Interrupt request is detected at both edges of IRQn input

[Legend]
n = 16 to 23

(4) Interrupt Control Register 3S (ICR3S)

ICR3S specifies the detection mode for external interrupt input pins IRQ31 to IRQ24 individually: rising edge, falling edge, low level, or high level.



Bit	Bit Name	Initial Value	R/W	Description
31 to 28	IRQ24SS	0000	R/W	IRQn Sense Select
27 to 24	IRQ25SS	0000	R/W	These bits select whether interrupt request signals from pins IRQ24 to IRQ31 are detected at a rising edge, a falling edge, a low level, a high level, or at both of a rising edge and a falling edge.
23 to 20	IRQ26SS	0000	R/W	
19 to 16	IRQ27SS	0000	R/W	
15 to 12	IRQ28SS	0000	R/W	
11 to 8	IRQ29SS	0000	R/W	
7 to 4	IRQ30SS	0000	R/W	
3 to 0	IRQ31SS	0000	R/W	

IRQnSS	Detection Mode
0000	Interrupt request is detected at a falling edge of IRQn input
0001	Interrupt request is detected at a rising edge of IRQn input
0010	Interrupt request is detected at a low level of IRQn input
0011	Interrupt request is detected at a high level of IRQn input
0100	Interrupt request is detected at both edges of IRQn input

[Legend]
n = 24 to 31

(5) Interrupt Control Register 3 (ICR3)

ICR3 is a register to set the chattering removal time for edge detection with external interrupt input pins IRQ3 to IRQ0.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IRQ0STS1[1:0]		IRQ0STS2[5:0]						IRQ1STS1[1:0]		IRQ1STS2[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IRQ2STS1[1:0]		IRQ2STS2[5:0]						IRQ3STS1[1:0]		IRQ3STS2[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31, 30	IRQ0STS1	B'00	R/W	IRQn Scan Timing
29 to 24	IRQ0STS2	H'00	R/W	These bits set the chattering removal time for the IRQ0 to IRQ3 pins
23, 22	IRQ1STS1	B'00	R/W	
21 to 16	IRQ1STS2	H'00	R/W	
15,14	IRQ2STS1	B'00	R/W	
13 to 8	IRQ2STS2	H'00	R/W	
7, 6	IRQ3STS1	B'00	R/W	
5 to 0	IRQ3STS2	H'00	R/W	

IRQnSTS1	Chattering Period Clock
B'00	1 ms
B'01	2 ms
B'10	4 ms
B'11	8 ms

IRQnSTS2	Chattering removal time
H'00	None
H'01 to H'3F	Chattering period clock × IRQnSTS2 ms

[Legend]
n = 0 to 3

(6) Interrupt Control Register 4 (ICR4)

ICR4 is a register to set the chattering removal time for edge detection with external interrupt input pins IRQ7 to IRQ4.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IRQ4STS1[1:0]		IRQ4STS2[5:0]						IRQ5STS1[1:0]		IRQ5STS2[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IRQ6STS1[1:0]		IRQ6STS2[5:0]						IRQ7STS1[1:0]		IRQ7STS2[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31, 30	IRQ4STS1	B'00	R/W	IRQn Scan Timing
29 to 24	IRQ4STS2	H'00	R/W	These bits set the chattering removal time for the IRQ4 to IRQ7 pins
23, 22	IRQ5STS1	B'00	R/W	
21 to 16	IRQ5STS2	H'00	R/W	
15 to 14	IRQ6STS1	B'00	R/W	
13 to 8	IRQ6STS2	H'00	R/W	
7, 6	IRQ7STS1	B'00	R/W	
5 to 0	IRQ7STS2	H'00	R/W	

IRQnSTS1	Chattering Period Clock
B'00	1 ms
B'01	2 ms
B'10	4 ms
B'11	8 ms

IRQnSTS2	Chattering Removal Time
H'00	None
H'01 to H'3F	Chattering period clock × IRQnSTS2 ms

[Legend]
n = 4 to 7

(7) Interrupt Control Register 5 (ICR5)

ICR5 is a register to set the chattering removal time for edge detection with external interrupt input pins IRQ7 11 IRQ8.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IRQ8STS1[1:0]		IRQ8STS2[5:0]						IRQ9STS1[1:0]		IRQ9STS2[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IRQ10STS1[1:0]		IRQ10STS2[5:0]						IRQ11STS1[1:0]		IRQ11STS2[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31, 30	IRQ8STS1	B'00	R/W	IRQn Scan Timing
29 to 24	IRQ8STS2	H'00	R/W	These bits set the chattering removal time for the IRQ8 to IRQ11 pins
23, 22	IRQ9STS1	B'00	R/W	
21 to 16	IRQ9STS2	H'00	R/W	
15, 14	IRQ10STS1	B'00	R/W	
13 to 8	IRQ10STS2	H'00	R/W	
7, 6	IRQ11STS1	B'00	R/W	
5 to 0	IRQ11STS2	H'00	R/W	

IRQnSTS1	Chattering Period Clock
B'00	1 ms
B'01	2 ms
B'10	4 ms
B'11	8 ms

IRQnSTS2	Chattering Removal Time
H'00	None
H'01 to H'3F	Chattering period clock × IRQnSTS2 ms

[Legend]
n = 8 to 11

(8) Interrupt Control Register 6 (ICR6)

ICR6 is a register to set the chattering removal time for edge detection with external interrupt input pins IRQ15 to IRQ12.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IRQ12STS1[1:0]		IRQ12STS2[5:0]						IRQ13STS1[1:0]		IRQ13STS2[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IRQ14STS1[1:0]		IRQ14STS2[5:0]						IRQ15STS1[1:0]		IRQ15STS2[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31, 30	IRQ12STS1	B'00	R/W	IRQn Scan Timing
29 to 24	IRQ12STS2	H'00	R/W	These bits set the chattering removal time for the IRQ12 to IRQ15 pins
23, 22	IRQ13STS1	B'00	R/W	
21 to 16	IRQ13STS2	H'00	R/W	
15, 14	IRQ14STS1	B'00	R/W	
13 to 8	IRQ14STS2	H'00	R/W	
7, 6	IRQ15STS1	B'00	R/W	
5 to 0	IRQ15STS2	H'00	R/W	

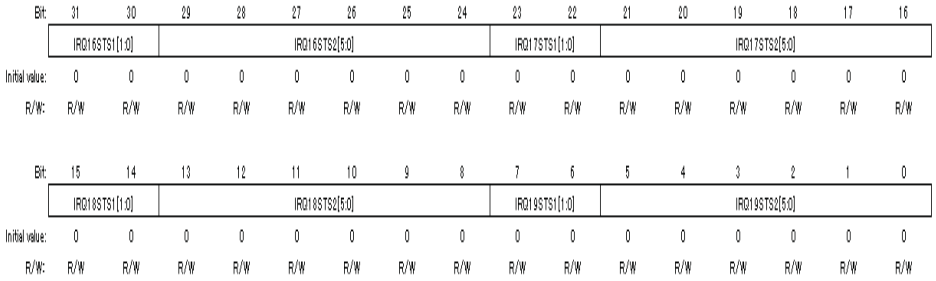
IRQnSTS1	Chattering Period Clock
B'00	1 ms
B'01	2 ms
B'10	4 ms
B'11	8 ms

IRQnSTS2	Chattering Removal Time
H'00	None
H'01 to H'3F	Chattering period clock × IRQnSTS2 ms

[Legend]
n = 12 to 15

(9) Interrupt Control Register 7 (ICR7)

ICR7 is a register to set the chattering removal time for edge detection with external interrupt input pins IRQ19 to IRQ16.



Bit	Bit Name	Initial Value	R/W	Description
31, 30	IRQ16STS1	B'00	R/W	IRQn Scan Timing
29 to 24	IRQ16STS2	H'00	R/W	These bits set the chattering removal time for the IRQ16 to IRQ19 pins
23, 22	IRQ17STS1	B'00	R/W	
21 to 16	IRQ17STS2	H'00	R/W	
15, 14	IRQ18STS1	B'00	R/W	
13 to 8	IRQ18STS2	H'00	R/W	
7, 6	IRQ19STS1	B'00	R/W	
5 to 0	IRQ19STS2	H'00	R/W	

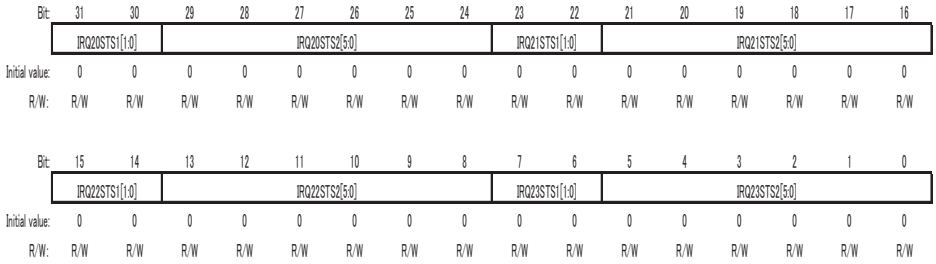
IRQnSTS1	Chattering Period Clock
B'00	1 ms
B'01	2 ms
B'10	4 ms
B'11	8 ms

IRQnSTS2	Chattering Removal Time
H'00	None
H'01 to H'3F	Chattering period clock × IRQnSTS2 ms

[Legend]
n = 16 to 19

(10) Interrupt Control Register 8 (ICR8)

ICR8 is a register to set the chattering removal time for edge detection with external interrupt input pins IRQ23 to IRQ20.



Bit	Bit Name	Initial Value	R/W	Description
31, 30	IRQ20STS1	B'00	R/W	IRQn Scan Timing
29 to 24	IRQ20STS2	H'00	R/W	These bits set the chattering removal time for the IRQ20 to IRQ23 pins
23, 22	IRQ21STS1	B'00	R/W	
21 to 16	IRQ21STS2	H'00	R/W	
15, 14	IRQ22STS1	B'00	R/W	
13 to 8	IRQ22STS2	H'00	R/W	
7, 6	IRQ23STS1	B'00	R/W	
5 to 0	IRQ23STS2	H'00	R/W	

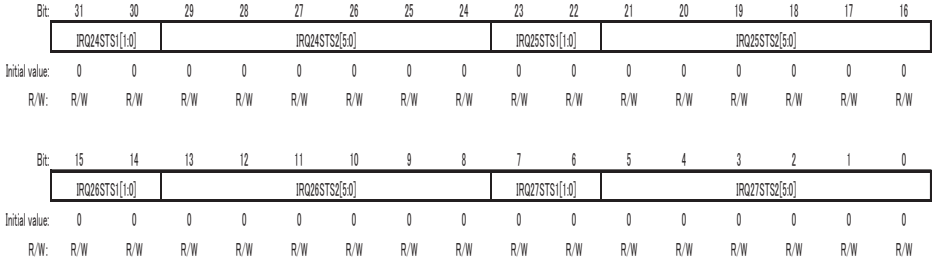
IRQnSTS1	Chattering Period Clock
B'00	1 ms
B'01	2 ms
B'10	4 ms
B'11	8 ms

IRQnSTS2	Chattering Removal Time
H'00	None
H'01 to H'3F	Chattering period clock × IRQnSTS2 ms

[Legend]
n = 23 to 20

(11) Interrupt Control Register 9 (ICR9)

ICR9 is a register to set the chattering removal time for edge detection with external interrupt input pins IRQ27 to IRQ24.



Bit	Bit Name	Initial Value	R/W	Description
31, 30	IRQ24STS1	B'00	R/W	IRQn Scan Timing
29 to 24	IRQ24STS2	H'00	R/W	These bits set the chattering removal time for the IRQ24 to IRQ27 pins
23, 22	IRQ25STS1	B'00	R/W	
21 to 16	IRQ25STS2	H'00	R/W	
15, 14	IRQ26STS1	B'00	R/W	
13 to 8	IRQ26STS2	H'00	R/W	
7, 6	IRQ27STS1	B'00	R/W	
5 to 0	IRQ27STS2	H'00	R/W	

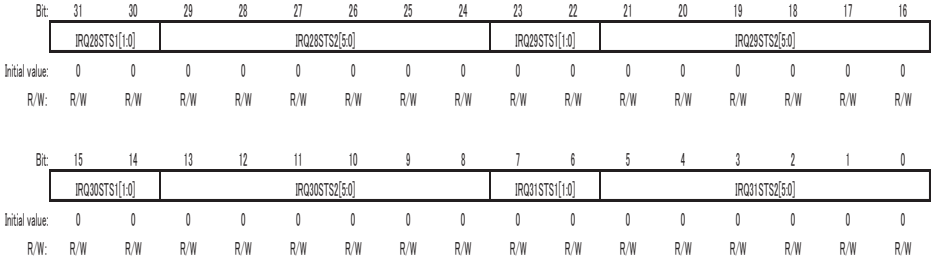
IRQnSTS1	Chattering Period Clock
B'00	1 ms
B'01	2 ms
B'10	4 ms
B'11	8 ms

IRQnSTS2	Chattering Removal Time
H'00	None
H'01 to H'3F	Chattering period clock × IRQnSTS2 ms

[Legend]
n = 27 to 24

(12) Interrupt Control Register 10 (ICR10)

ICR10 is a register to set the chattering removal time for edge detection with external interrupt input pins IRQ31 to IRQ28.



Bit	Bit Name	Initial Value	R/W	Description
31, 30	IRQ28STS1	B'00	R/W	IRQn Scan Timing
29 to 24	IRQ28STS2	H'00	R/W	These bits set the chattering removal time for the IRQ28 to IRQ31 pins
23, 22	IRQ29STS1	B'00	R/W	
21 to 16	IRQ29STS2	H'00	R/W	
15, 14	IRQ30STS1	B'00	R/W	
13 to 8	IRQ30STS2	H'00	R/W	
7, 6	IRQ31STS1	B'00	R/W	
5 to 0	IRQ31STS2	H'00	R/W	

IRQnSTS1	Chattering Period Clock
B'00	1 ms
B'01	2 ms
B'10	4 ms
B'11	8 ms

IRQnSTS2	Chattering Removal Time
H'00	None
H'01 to H'3F	Chattering period clock × IRQnSTS2 ms

[Legend]
n = 28 to 31

(13) Interrupt Priority Register 00S (INTPRI00S)

INTPRI00S is a register that specifies priority levels from 15 to 0 for external interrupt input pins IRQ7 to IRQ0.

Each 4-bit group is set with a value from H'F (1111) to H'0 (0000) to specify the interrupt priority level for the corresponding interrupt. Setting H'F means priority level 15 (the highest level); H'0 means priority level 0 (the request is masked).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IRQ0S				IRQ1S				IRQ2S				IRQ3S			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IRQ4S				IRQ5S				IRQ6S				IRQ7S			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	IRQ0S	H'0	R/W	These bits specify the priority level for each interrupt source in 4-bit units.
27 to 24	IRQ1S	H'0	R/W	
23 to 20	IRQ2S	H'0	R/W	
19 to 16	IRQ3S	H'0	R/W	
15 to 12	IRQ4S	H'0	R/W	
11 to 8	IRQ5S	H'0	R/W	
7 to 4	IRQ6S	H'0	R/W	
3 to 0	IRQ7S	H'0	R/W	

(14) Interrupt Priority Register 10S (INTPRI10S)

INTPRI10S is a register that specifies priority levels from 15 to 0 for external interrupt input pins IRQ15 to IRQ8.

Each 4-bit group is set with a value from H'F (1111) to H'0 (0000) to specify the interrupt priority level for the corresponding interrupt. Setting H'F means priority level 15 (the highest level); H'0 means priority level 0 (the request is masked).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IRQ8S				IRQ9S				IRQ10S				IRQ11S			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

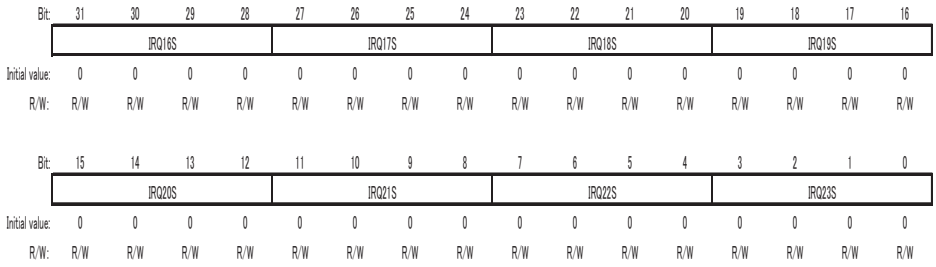
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IRQ12S				IRQ13S				IRQ14S				IRQ15S			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	IRQ8S	H'0	R/W	These bits specify the priority level for each interrupt source in 4-bit units.
27 to 24	IRQ9S	H'0	R/W	
23 to 20	IRQ10S	H'0	R/W	
19 to 16	IRQ11S	H'0	R/W	
15 to 12	IRQ12S	H'0	R/W	
11 to 8	IRQ13S	H'0	R/W	
7 to 4	IRQ14S	H'0	R/W	
3 to 0	IRQ15S	H'0	R/W	

(15) Interrupt Priority Register 20S (INTPRI20S)

INTPRI20S is a register that specifies priority levels from 15 to 0 for external interrupt input pins IRQ23 to IRQ16.

Each 4-bit group is set with a value from H'F (1111) to H'0 (0000) to specify the interrupt priority level for the corresponding interrupt. Setting H'F means priority level 15 (the highest level); H'0 means priority level 0 (the request is masked).

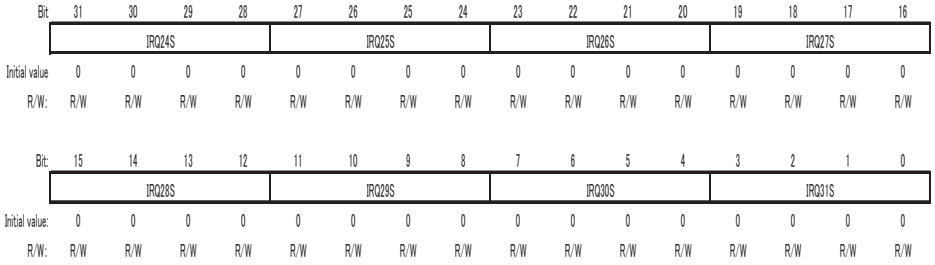


Bit	Bit Name	Initial Value	R/W	Description
31 to 28	IRQ16S	H'0	R/W	These bits specify the priority level for each interrupt source in 4-bit units.
27 to 24	IRQ17S	H'0	R/W	
23 to 20	IRQ18S	H'0	R/W	
19 to 16	IRQ19S	H'0	R/W	
15 to 12	IRQ20S	H'0	R/W	
11 to 8	IRQ21S	H'0	R/W	
7 to 4	IRQ22S	H'0	R/W	
3 to 0	IRQ23S	H'0	R/W	

(16) Interrupt Priority Register 30S (INTPRI30S)

INTPRI10S is a register that specifies priority levels from 15 to 0 for external interrupt input pins IRQ31 to IRQ24.

Each 4-bit group is set with a value from H'F (1111) to H'0 (0000) to specify the interrupt priority level for the corresponding interrupt. Setting H'F means priority level 15 (the highest level); H'0 means priority level 0 (the request is masked).



Bit	Bit Name	Initial Value	R/W	Description
31 to 28	IRQ24S	H'0	R/W	These bits specify the priority level for each interrupt source in 4-bit units.
27 to 24	IR25S	H'0	R/W	
23 to 20	IRQ26S	H'0	R/W	
19 to 16	IRQ27S	H'0	R/W	
15 to 12	IRQ28S	H'0	R/W	
11 to 8	IRQ29S	H'0	R/W	
7 to 4	IRQ30S	H'0	R/W	
3 to 0	IRQ31S	H'0	R/W	

(17) Peripheral Interrupt Priority Registers AS to MS ,AS3 to PS3（IPRAS to IPRMS,IPRAS3 to IPRPS3）

IPRAS to IPRMS and IPRAS3 to IPRPS3 are registers that specify priority levels from 15 to 0 for on-chip peripheral module interrupts.

Four modules are assigned to each register. Each 4-bit group is set with a value from H'F (1111) to H'0 (0000) to specify the interrupt priority level for the corresponding interrupt. Setting H'F means priority level 15 (the highest level); H'0 means priority level 0 (the request is masked).

Table 5.8 shows the correspondence between the peripheral modules requesting interrupts and the peripheral interrupt priority registers.

IPRAS to IPRMS:

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IPR0nS				IPR1nS				IPR2nS				IPR3nS			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

IPRAS3 to IPRPS3:

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IPR0nS3				IPR1nS3				IPR2nS3				IPR3nS3			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

IPRAS to IPRMS:

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	IPR0nS	H'0	R/W	These bits specify the priority level for each interrupt source in 4-bit units. For details, see table 5.8.
11 to 8	IPR1nS	H'0	R/W	
7 to 4	IPR2nS	H'0	R/W	
3 to 0	IPR3nS	H'0	R/W	

[Legend]

n = A to M

IPRAS3 to IPRPS3:

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	IPR0mS3	H'0	R/W	These bits specify the priority level for each interrupt source in 4-bit units. For details, see table 5.8.
11 to 8	IPR1mS3	H'0	R/W	
7 to 4	IPR2mS3	H'0	R/W	
3 to 0	IPR3mS3	H'0	R/W	

[Legend]
m = A to P

Table 5.8 Interrupt Sources and IPRAS to IPRMS,IPRAS3 to IPRPS3

Register name	IPR0nS	IPR1nS	IPR2nS	IPR3nS
IPRAS	CTI	—	2DDMAC	ICB
IPRBS	JPU	LCDC	—	LCRC
IPRCS	BBIF2	—	—	—
IPRDS	—	—	—	—
IPRES	RTDMAC(1)	CEU	MFI	VPU
IPRFS	KEYSC	RTDMAC(2)	CMT2	CMT0
IPRGS	TMU0 0	TMU 0 1	TMU02	TSIF1
IPRHS	TTI20	—	VEU	BEU
IPRIS	—	MSIOF	TSIF0	IIC0
IPRJS	—	3DG	—	—
IPRKS	2DG	ASA	LMB	PEP
IPRLS	IPMMU	—	—	HQE
IPRMS	IIC2	—	—	RWDT0
IPRAS3	RTDMAC2(1)	—	—	—
IPRBS3	RTDMAC2(2)	—	—	—
IPRCS3	—	—	—	—
IPRDS3	—	—	—	—
IPRES3	—	—	—	—
IPRFS3	—	—	—	—
IPRGS3	—	—	—	—
IPRHS3	—	—	—	—
IPRIS3	—	ISP	—	—
IPRJS3	LCDC1	CSIRX	DSITX	—

Register name	IPR0nS	IPR1nS	IPR2nS	IPR3nS
IPRKS3	SPU2	—	FSI	FMSI
IPRLS3	—	—	—	HDMI
IPRMS3	TMU1	—	—	—
IPRNS3	CMT4	DSITX1_0	DSITX1_1	—
IPROS3	MFIS2	CPORTS2R	CEC_1	CEC_2
IPRPS3	JPU6E			

Note: —: Reserved. An undefined value will be read. Writing is ignored.

(18) Interrupt Source Register 00S (INTREQ00S)

INTREQ00S is a register that indicates interrupt requests from external input pins IRQ7 to IRQ0. This register value is not affected by the INTPRI00S setting or the interrupt masks specified with INTMSK00S.

When edge-detection mode is set for an IRQ pin (ICR0S.IRQnSS = B'00 or B'01), an interrupt request is cleared by writing 0 to the corresponding IRQnS bit after reading IRQnS = 1; write 1 to the other bits.

Bit:	7	6	5	4	3	2	1	0
	IRQ0S	IRQ1S	IRQ2S	IRQ3S	IRQ4S	IRQ5S	IRQ6S	IRQ7S
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	IRQ0S	0	R/W	IRQn Interrupt Request
6	IRQ1S	0	R/W	Indicates whether there is an interrupt request input to the IRQn pin.
5	IRQ2S	0	R/W	
4	IRQ3S	0	R/W	[When edge-detection mode is selected (ICR0S.IRQnSS = B'00 or B'01)]
3	IRQ4S	0	R/W	When reading:
2	IRQ5S	0	R/W	0: No interrupt request has been detected
1	IRQ6S	0	R/W	1: An interrupt request has been detected
0	IRQ7S	0	R/W	When writing:
				0: Each bit is cleared by writing 0 after reading 1
				1: Writing 1 is ignored
				[When level-detection mode is selected (ICR0S.IRQnSS = B'10 or B'11)]
				When reading:
				0: The corresponding interrupt pin has not been asserted
				1: The corresponding interrupt pin has been asserted
				When writing:
				Writing 0 or 1 is ignored.

[Legend]
n = 0 to 7

(19) Interrupt Source Register 10S (INTREQ10S)

INTREQ10S is a register that indicates interrupt requests from external input pins IRQ15 to IRQ8. This register value is not affected by the INTPRI10S setting or the interrupt masks specified with the INTMSK10S.

When edge-detection mode is set for an IRQ pin (ICR1S.IRQnSS = B'00 or B'01), an interrupt request is cleared by writing 0 to the corresponding IRQnS bit after reading IRQnS = 1; write 1 to the other bits.

Bit:	7	6	5	4	3	2	1	0
	IRQ 8S	IRQ 9S	IRQ 10S	IRQ 11S	IRQ 12S	IRQ 13S	IRQ 14S	IRQ 15S
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

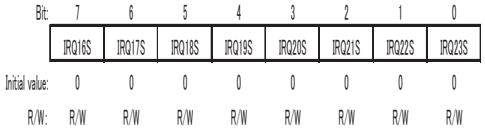
Bit	Bit Name	Initial Value	R/W	Description
7	IRQ8S	0	R/W	IRQn Interrupt Request
6	IRQ9S	0	R/W	Indicates whether there is an interrupt request input to the IRQn pin.
5	IRQ10S	0	R/W	[When edge-detection mode is selected (ICR1S.IRQnSS = B'00 or B'01)]
4	IRQ11S	0	R/W	When reading:
3	IRQ12S	0	R/W	0: No interrupt request has been detected
2	IRQ13S	0	R/W	1: An interrupt request has been detected
1	IRQ14S	0	R/W	When writing:
0	IRQ15S	0	R/W	0: Each bit is cleared by writing 0 after reading 1
				1: Writing 1 is ignored
				[When level-detection mode is selected (ICR1S.IRQnSS = B'10 or B'11)]
				When reading:
				0: The corresponding interrupt pin has not been asserted
				1: The corresponding interrupt pin has been asserted
				When writing:
				Writing 0 or 1 is ignored.

[Legend]
n = 8 to 15

(20) Interrupt Source Register 20S (INTREQ20S)

INTREQ20S is a register that indicates interrupt requests from external input pins IRQ23 to IRQ16. This register value is not affected by the INTPRI20S setting or the interrupt masks specified with the INTMSK20S.

When edge-detection mode is set for an IRQ pin (ICR2S.IRQnSS = B'00 or B'01), an interrupt request is cleared by writing 0 to the corresponding IRQnS bit after reading IRQnS = 1; write 1 to the other bits.



Bit:	7	6	5	4	3	2	1	0
	IRQ16S	IRQ17S	IRQ18S	IRQ19S	IRQ20S	IRQ21S	IRQ22S	IRQ23S
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	IRQ16S	0	R/W	IRQn Interrupt Request
6	IRQ17S	0	R/W	Indicates whether there is an interrupt request input to the IRQn pin.
5	IRQ18S	0	R/W	[When edge-detection mode is selected (ICR2S.IRQnSS = B'00 or B'01)]
4	IRQ19S	0	R/W	When reading:
3	IRQ20S	0	R/W	0: No interrupt request has been detected
2	IRQ21S	0	R/W	1: An interrupt request has been detected
1	IRQ22S	0	R/W	When writing:
0	IRQ23S	0	R/W	0: Each bit is cleared by writing 0 after reading 1
				1: Writing 1 is ignored
				[When level-detection mode is selected (ICR2S.IRQnSS = B'10 or B'11)]
				When reading:
				0: The corresponding interrupt pin has not been asserted
				1: The corresponding interrupt pin has been asserted
				When writing:
				Writing 0 or 1 is ignored.

[Legend]
n = 16 to 23

(21) Interrupt Source Register 30S (INTREQ30S)

INTREQ30S is a register that indicates interrupt requests from external input pins IRQ31 to IRQ24. This register value is not affected by the INTPRI30S setting or the interrupt masks specified with the INTMSK30S.

When edge-detection mode is set for an IRQ pin (ICR3S.IRQnSS = B'00 or B'01), an interrupt request is cleared by writing 0 to the corresponding IRQnS bit after reading IRQnS = 1; write 1 to the other bits.

Bit:	7	6	5	4	3	2	1	0
	IRQ24S	IRQ25S	IRQ26S	IRQ27S	IRQ28S	IRQ29S	IRQ30S	IRQ31S
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	IRQ24S	0	R/W	IRQn Interrupt Request
6	IRQ25S	0	R/W	Indicates whether there is an interrupt request input to the IRQn pin.
5	IRQ26S	0	R/W	
4	IRQ27S	0	R/W	[When edge-detection mode is selected (ICR3S.IRQnSS = B'00 or B'01)]
3	IRQ28S	0	R/W	When reading:
2	IRQ29S	0	R/W	0: No interrupt request has been detected
1	IRQ30S	0	R/W	1: An interrupt request has been detected
0	IRQ31S	0	R/W	When writing:
				0: Each bit is cleared by writing 0 after reading 1
				1: Writing 1 is ignored
				[When level-detection mode is selected (ICR3S.IRQnSS = B'10 or B'11)]
				When reading:
				0: The corresponding interrupt pin has not been asserted
				1: The corresponding interrupt pin has been asserted
				When writing:
				Writing 0 or 1 is ignored.

[Legend]
n = 31 to 24

(22) Interrupt Mask Register 00S (INTMSK00S)

INTMSK00S is a register that masks interrupt requests from external interrupt input pins IRQ7 to IRQ0.

To clear an interrupt mask, write 1 to the corresponding bit in INTMSKCLR00S. Writing 0 to the corresponding bit in INTMSK00S does not affect the bit value.

Bit:	7	6	5	4	3	2	1	0
	IRQ0S	IRQ1S	IRQ2S	IRQ3S	IRQ4S	IRQ5S	IRQ6S	IRQ7S
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	IRQ0S	0	R/W	IRQn Interrupt Mask
6	IRQ1S	0	R/W	0: The corresponding interrupt is not masked
5	IRQ2S	0	R/W	1: The corresponding interrupt is masked
4	IRQ3S	0	R/W	
3	IRQ4S	0	R/W	
2	IRQ5S	0	R/W	
1	IRQ6S	0	R/W	
0	IRQ7S	0	R/W	

[Legend]
n = 0 to 7

(23) Interrupt Mask Register 10S (INTMSK10S)

INTMSK10S is a register that masks interrupt requests from external interrupt input pins IRQ15 to IRQ8.

To clear an interrupt mask, write 1 to the corresponding bit in INTMSKCLR10S. Writing 0 to the corresponding bit in INTMSK10S does not affect the bit value.

Bit:	7	6	5	4	3	2	1	0
	IRQ8S	IRQ9S	IRQ10S	IRQ11S	IRQ12S	IRQ13S	IRQ14S	IRQ15S
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	IRQ8S	0	R/W	IRQn Interrupt Mask
6	IRQ9S	0	R/W	0: The corresponding interrupt is not masked
5	IRQ10S	0	R/W	1: The corresponding interrupt is masked
4	IRQ11S	0	R/W	
3	IRQ12S	0	R/W	
2	IRQ13S	0	R/W	
1	IRQ14S	0	R/W	
0	IRQ15S	0	R/W	

[Legend]
n = 8 to 15

(24) Interrupt Mask Register 20S (INTMSK20S)

INTMSK20S is a register that masks interrupt requests from external interrupt input pins IRQ23 to IRQ16.

To clear an interrupt mask, write 1 to the corresponding bit in INTMSKCLR20S. Writing 0 to the corresponding bit in INTMSK20S does not affect the bit value.

Bit:	7	6	5	4	3	2	1	0
	IRQ16S	IRQ17S	IRQ18S	IRQ19S	IRQ20S	IRQ21S	IRQ22S	IRQ23S
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	IRQ16S	0	R/W	IRQn Interrupt Mask
6	IRQ17S	0	R/W	0: The corresponding interrupt is not masked
5	IRQ18S	0	R/W	1: The corresponding interrupt is masked
4	IRQ19S	0	R/W	
3	IRQ20S	0	R/W	
2	IRQ21S	0	R/W	
1	IRQ22S	0	R/W	
0	IRQ23S	0	R/W	

[Legend]
n = 16 to 23

(25) Interrupt Mask Register 30S (INTMS30S)

INTMSK30S is a register that masks interrupt requests from external interrupt input pins IRQ31 to IRQ24.

To clear an interrupt mask, write 1 to the corresponding bit in INTMSKCLR30S. Writing 0 to the corresponding bit in INTMSK30S does not affect the bit value.

Bit:	7	6	5	4	3	2	1	0
	IRQ24S	IRQ25S	IRQ26S	IRQ27S	IRQ28S	IRQ29S	IRQ30S	IRQ31S
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	IRQ24S	0	R/W	IRQn Interrupt Mask
6	IRQ25S	0	R/W	0: The corresponding interrupt is not masked
5	IRQ26S	0	R/W	1: The corresponding interrupt is masked
4	IRQ27S	0	R/W	
3	IRQ28S	0	R/W	
2	IRQ29S	0	R/W	
1	IRQ30S	0	R/W	
0	IRQ31S	0	R/W	

[Legend]
n = 24 to 31

(26) Interrupt Mask Clear Register 00S (INTMSKCLR00S)

INTMSKCLR00S is a write-only register that clears the mask settings for interrupts from external interrupt input pins IRQ7 to IRQ0.

Bit:	7	6	5	4	3	2	1	0
	IRQ0S	IRQ1S	IRQ2S	IRQ3S	IRQ4S	IRQ5S	IRQ6S	IRQ7S
Initial value:	-	-	-	-	-	-	-	-
R/W:	W	W	W	W	W	W	W	W

Bit	Bit Name	Initial Value	R/W	Description
7	IRQ0S	—	W	IRQnS Interrupt Mask Clear
6	IRQ1S	—	W	0: Writing 0 is ignored
5	IRQ2S	—	W	1: Clears the corresponding interrupt mask
4	IRQ3S	—	W	When reading:
3	IRQ4S	—	W	An undefined value will be read.
2	IRQ5S	—	W	
1	IRQ6S	—	W	
0	IRQ7S	—	W	

[Legend]
n = 0 to 7

(27) Interrupt Mask Clear Register 10S (INTMSKCLR10S)

INTMSKCLR10S is a write-only register that clears the mask settings for interrupts from external interrupt input pins IRQ15 to IRQ8.

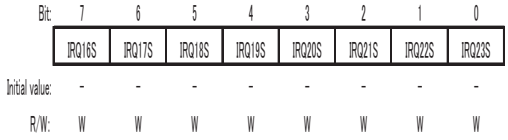
Bit:	7	6	5	4	3	2	1	0
	IRQ 8S	IRQ 9S	IRQ 10S	IRQ 11S	IRQ 12S	IRQ 13S	IRQ 14S	IRQ 15S
Initial value:	-	-	-	-	-	-	-	-
R/W:	W	W	W	W	W	W	W	W

Bit	Bit Name	Initial Value	R/W	Description
7	IRQ8S	—	W	IRQnS Interrupt Mask Clear
6	IRQ9S	—	W	0: Writing 0 is ignored
5	IRQ10S	—	W	1: Clears the corresponding interrupt mask
4	IRQ11S	—	W	When reading:
3	IRQ12S	—	W	An undefined value will be read.
2	IRQ13S	—	W	
1	IRQ14S	—	W	
0	IRQ15S	—	W	

[Legend]
n = 8 to 15

(28) Interrupt Mask Clear Register 20S (INTMSKCLR20S)

INTMSKCLR20S is a write-only register that clears the mask settings for interrupts from external interrupt input pins IRQ23 to IRQ16.



Bit	Bit Name	Initial Value	R/W	Description
7	IRQ16S	—	W	IRQnS Interrupt Mask Clear
6	IRQ17S	—	W	0: Writing 0 is ignored
5	IRQ18S	—	W	1: Clears the corresponding interrupt mask
4	IRQ19S	—	W	When reading:
3	IRQ20S	—	W	An undefined value will be read.
2	IRQ21S	—	W	
1	IRQ22S	—	W	
0	IRQ23S	—	W	

[Legend]
n = 16 to 23

(29) Interrupt Mask Clear Register 30S (INTMSKCLR30S)

INTMSKCLR30S is a write-only register that clears the mask settings for interrupts from external interrupt input pins IRQ31 to IRQ24.

Bit:	7	6	5	4	3	2	1	0
	IRQ24S	IRQ25S	IRQ26S	IRQ27S	IRQ28S	IRQ29S	IRQ30S	IRQ31S
Initial value:	-	-	-	-	-	-	-	-
R/W:	W	W	W	W	W	W	W	W

Bit	Bit Name	Initial Value	R/W	Description
7	IRQ24S	—	W	IRQnS Interrupt Mask Clear
6	IRQ25S	—	W	0: Writing 0 is ignored
5	IRQ26S	—	W	1: Clears the corresponding interrupt mask
4	IRQ27S	—	W	When reading:
3	IRQ28S	—	W	An undefined value will be read.
2	IRQ29S	—	W	
1	IRQ30S	—	W	
0	IRQ31S	—	W	

[Legend]
n = 24 to 31

(30) Peripheral Interrupt Mask Registers 0S to 12S,0S3 to 7S3 (IMR0S to IMR12S,IMR0S3 to IMR7S3)

IMR0S to IMR12S and IMR0S3 to IMR7S3 are registers that mask on-chip peripheral module interrupts. To mask an interrupt, write 1 to the corresponding bit in IMR0S to IMR12S and IMR0S3 to IMR7S3. Peripheral module interrupts not used should be masked.

To clear an interrupt mask, write 1 to the corresponding bit in IMCR0S to IMCR12S and IMR0S3 to IMR7S3. Writing 0 to the corresponding bit in IMR0S to IMR12S and IMR0S3 to IMR7S3 does not affect the bit value.

Table 5.9 shows the correspondence between the bits in IMR0S to IMR12S and IMR0S3 to IMR7S3 and the interrupt sources.

IMR0S to IMR12S:

Bit:	7	6	5	4	3	2	1	0
	IMRn 0S	IMRn 1S	IMRn 2S	IMRn 3S	IMRn 4S	IMRn 5S	IMRn 6S	IMRn 7S
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

IMR0S3 to IMR7S3:

Bit:	7	6	5	4	3	2	1	0
	IMRm 0S3	IMRm 1S3	IMRm 2S3	IMRm 3S3	IMRm 4S3	IMRm 5S3	IMRm 6S3	IMRm 7S3
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

IMR0S to IMR12S:

Bit	Bit Name	Initial Value	R/W	Description
7	IMRn0S	0	R/W	Interrupt Mask
6	IMRn1S	0	R/W	Masks the interrupt request corresponding to each bit. See table 5.9 for the correspondence between IMR and each interrupt source.
5	IMRn2S	0	R/W	
4	IMRn3S	0	R/W	When writing:
3	IMRn4S	0	R/W	0: Writing 0 is ignored
2	IMRn5S	0	R/W	1: Masks the corresponding interrupt request
1	IMRn6S	0	R/W	When reading:
0	IMRn7S	0	R/W	0: The corresponding interrupt request is accepted
				1: The corresponding interrupt request is masked

[Legend]
n = 0 to 12

IMR0S3 to IMR7S3:

Bit	Bit Name	Initial Value	R/W	Description
7	IMRm0S3	0	R/W	Interrupt Mask
6	IMRm1S3	0	R/W	Masks the interrupt request corresponding to each bit. See table 5.9 for the correspondence between IMR and each interrupt source.
5	IMRm2S3	0	R/W	
4	IMRm3S3	0	R/W	When writing:
3	IMRm4S3	0	R/W	0: Writing 0 is ignored
2	IMRm5S3	0	R/W	1: Masks the corresponding interrupt request
1	IMRm6S3	0	R/W	When reading:
0	IMRm7S3	0	R/W	0: The corresponding interrupt request is accepted
				1: The corresponding interrupt request is masked

[Legend]
m = 0 to 7

(31) Peripheral Interrupt Mask Clear Registers 0S to 12S,0S3 to 7S3(IMCR0S to IMCR12S,IMCR0S3 to IMCR7S3)

IMCR0S to IMCR12S and IMCR0S3 to IMCR7S3 are write-only registers that clear the mask settings for the on-chip peripheral module interrupts. Table 5.9 shows the correspondence between the bits in IMCR0S to IMCR12S and IMCR0S3 to IMCR7S3 and the interrupt sources.

IMCR0S to IMCR12S:

Bit:	7	6	5	4	3	2	1	0
	IMCRn0S	IMCRn1S	IMCRn2S	IMCRn3S	IMCRn4S	IMCRn5S	IMCRn6S	IMCRn7S
Initial value:	-	-	-	-	-	-	-	-
R/W:	W	W	W	W	W	W	W	W

IMCR0S3 to IMCR7S3:

Bit:	7	6	5	4	3	2	1	0
	IMCRm0S3	IMCRm1S3	IMCRm2S3	IMCRm3S3	IMCRm4S3	IMCRm5S3	IMCRm6S3	IMCRm7S3
Initial value:	-	-	-	-	-	-	-	-
R/W:	W	W	W	W	W	W	W	W

IMCR0S to IMCR12S:

Bit	Bit Name	Initial Value	R/W	Description
7	IMCRn0S	—	W	Interrupt Mask Clear
6	IMCRn1S	—	W	Clears the mask setting for the interrupt corresponding to each bit. See table 5.9 for the correspondence between IMCR and each interrupt source.
5	IMCRn2S	—	W	
4	IMCRn3S	—	W	When writing:
3	IMCRn4S	—	W	0: Writing 0 is ignored
2	IMCRn5S	—	W	1: Clears the corresponding interrupt mask
1	IMCRn6S	—	W	When reading:
0	IMCRn7S	—	W	An undefined value will be read.

[Legend]
n = 0 to 12

IMCR0S3 to IMCR7S3:

Bit	Bit Name	Initial Value	R/W	Description
7	IMCRm0S3	—	W	Interrupt Mask Clear
6	IMCRm1S3	—	W	Clears the mask setting for the interrupt corresponding to each bit. See table 5.9 for the correspondence between IMCR and each interrupt source.
5	IMCRm2S3	—	W	
4	IMCRm3S3	—	W	When writing:
3	IMCRm4S3	—	W	0: Writing 0 is ignored
2	IMCRm5S3	—	W	1: Clears the corresponding interrupt mask
1	IMCRm6S3	—	W	When reading:
0	IMCRm7S3	—	W	An undefined value will be read.

[Legend]

m = 0 to 7

(32) Peripheral Interrupt Mask Registers 0SA to 12SA,0SA3 to 7SA3 (IMR0SA to IMR12SA,IMR0SA3 to IMR7SA3)

IMR0SA to IMR12SA and IMR0SA3 to IMR7SA3 are registers that mask on-chip peripheral module interrupts to be sent to the INTCA. To mask an interrupt request, write 1 to the corresponding bit in IMR0SA to IMR12SA and IMR0SA3 to IMR7SA3. Peripheral module interrupts not used should be masked.

To clear an interrupt mask, write 1 to the corresponding bit in IMCR0SA to IMCR12SA and IMR0SA3 to IMR7SA3. Writing 0 to the corresponding bit in IMR0SA to IMR12SA and IMR0SA3 to IMR7SA3 does not affect the bit value.

Table 5.9 shows the correspondence between the bits in IMR0SA to IMR12SA and IMR0SA3 to IMR7SA3 and the interrupt sources.

IMR0SA to IMR12SA:

Bit:	7	6	5	4	3	2	1	0
	IMRn 0SA	IMRn 1SA	IMRn 2SA	IMRn 3SA	IMRn 4SA	IMRn 5SA	IMRn 6SA	IMRn 7SA
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

IMR0SA3 to IMR7SA3:

Bit:	7	6	5	4	3	2	1	0
	IMRm 0SA3	IMRm 1SA3	IMRm 2SA3	IMRm 3SA3	IMRm 4SA3	IMRm 5SA3	IMRm 6SA3	IMRm 7SA3
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

IMR0SA to IMR12SA:

Bit	Bit Name	Initial Value	R/W	Description
7	IMRn0SA	0	R/W	Interrupt Mask
6	IMRn1SA	0	R/W	Masks the interrupt request corresponding to each bit. See table 5.9 for the correspondence between IMR and each interrupt source.
5	IMRn2SA	0	R/W	
4	IMRn3SA	0	R/W	When writing:
3	IMRn4SA	0	R/W	0: Writing 0 is ignored
2	IMRn5SA	0	R/W	1: Masks the corresponding interrupt request
1	IMRn6SA	0	R/W	When reading:
0	IMRn7SA	0	R/W	0: The corresponding interrupt request is accepted
				1: The corresponding interrupt request is masked

[Legend]
n = 0 to 12

IMR0SA3 to IMR7SA3:

Bit	Bit Name	Initial Value	R/W	Description
7	IMRm0SA3	0	R/W	Interrupt Mask
6	IMRm1SA3	0	R/W	Masks the interrupt request corresponding to each bit. See table 5.9 for the correspondence between IMR and each interrupt source.
5	IMRm2SA3	0	R/W	
4	IMRm3SA3	0	R/W	When writing:
3	IMRm4SA3	0	R/W	0: Writing 0 is ignored
2	IMRm5SA3	0	R/W	1: Masks the corresponding interrupt request
1	IMRm6SA3	0	R/W	When reading:
0	IMRm7SA3	0	R/W	0: The corresponding interrupt request is accepted
				1: The corresponding interrupt request is masked

[Legend]
m = 0 to 12

(33) Peripheral Interrupt Mask Clear Registers 0SA to 12SA,0SA3 to 7SA3 (IMCR0SA to IMCR12SA,IMCR0SA3 to IMCR7SA3)

IMCR0SA to IMCR12SA and IMCR0SA3 to IMCR7SA3 are write-only registers that clear the mask settings for the on-chip peripheral module interrupts to be sent to the INTCA. Table 5.9 shows the correspondence between the bits in IMCR0SA to IMCR12SA and IMCR0SA3 to IMCR7SA3 and the interrupt sources.

IMCR0SA to IMCR12SA:

Bit:	7	6	5	4	3	2	1	0
	IMCR n0SA	IMCR n1SA	IMCR n2SA	IMCR n3SA	IMCR n4SA	IMCR n5SA	IMCR n6SA	IMCR n7SA
Initial value:	-	-	-	-	-	-	-	-
R/W:	W	W	W	W	W	W	W	W

IMCR0SA3 to IMCR7SA3:

Bit:	7	6	5	4	3	2	1	0
	IMCRm 0SA3	IMCRm 1SA3	IMCRm 2SA3	IMCRm 3SA3	IMCRm 4SA3	IMCRm 5SA3	IMCRm 6SA3	IMCRm 7SA3
Initial value:	-	-	-	-	-	-	-	-
R/W:	W	W	W	W	W	W	W	W

IMCR0SA to IMCR12SA:

Bit	Bit Name	Initial Value	R/W	Description
7	IMCRn0SA	—	W	Interrupt Mask Clear Clears the mask setting for the interrupt corresponding to each bit. See table 5.9 for the correspondence between IMCR and each interrupt source. When writing: 0: Writing 0 is ignored 1: Clears the corresponding interrupt mask When reading: An undefined value will be read.
6	IMCRn1SA	—	W	
5	IMCRn2SA	—	W	
4	IMCRn3SA	—	W	
3	IMCRn4SA	—	W	
2	IMCRn5SA	—	W	
1	IMCRn6SA	—	W	
0	IMCRn7SA	—	W	

[Legend]
n = 0 to 12

IMCR0SA3 to IMCR7SA3:

Bit	Bit Name	Initial Value	R/W	Description
7	IMCRm0SA3	—	W	Interrupt Mask Clear
6	IMCRm1SA3	—	W	Clears the mask setting for the interrupt corresponding to each bit. See table 5.9 for the correspondence between IMCR and each interrupt source.
5	IMCRm2SA3	—	W	
4	IMCRm3SA3	—	W	When writing:
3	IMCRm4SA3	—	W	0: Writing 0 is ignored
2	IMCRm5SA3	—	W	1: Clears the corresponding interrupt mask
1	IMCRm6SA3	—	W	When reading:
0	IMCRnmSA3	—	W	An undefined value will be read.

[Legend]
n = 0 to 7

Table 5.9 Correspondence between On-Chip Peripheral Module Interrupt Sources and IMR0S to IMR12S, IMR0S3 to IMR7S3, IMCR0S to IMCR12S, IMCR0S3 to IMCR7S3, IMR0SA to IMR12SA, IMR0SA3 to IMR7SA3, IMCR0SA to IMCR12SA and IMCR0SA3 to IMCR7SA3.

Register Name	Bit Name(Function Name)							
	7	6	5	4	3	2	1	0
IMR0S/IMCR0S	—	—	—	—	—	—	—	—
IMR0SA/IMCR0SA	—	—	—	—	—	—	—	—
IMR1S/IMCR1S	BEU2	BEU1	BEU0	CEU	VEU3	VEU2	VEU1	VEU0
IMR1SA/IMCR1SA	(BEU)			(CEU)	(VEU)			
IMR2S/IMCR2S	—	—	—	VPU	BBIF2	—	—	MFI
IMR2SA/IMCR2SA	—	—	—	(VPU)	(BBIF2)	—	—	(MFI)
IMR3S/IMCR3S	—	—	—	2DDM0	—	—	—	ICB
IMR3SA/IMCR3SA	(2DDMAC)				—	—	—	(ICB)
IMR4S/IMCR4S	—	—	—	CTI	JPEG	—	LCRC	LCDC
IMR4SA/IMCR4SA	—	—	—	CTI	(JPU)	—	(LCRC)	(LCDC)
IMR5S/IMCR5S	KEY	DADERR	DEI5	DEI4	DEI3	DEI2	DEI1	DEI0
IMR5SA/IMCR5SA	(KEYSC)	(RTDMAC(2))			(RTDMAC(1))			
IMR6S/IMCR6S	—	—	MSIOF	—	SGX540	—	TTI20*	—
IMR6SA/IMCR6SA	—	—	(MSIOF)	—	(3DG)	—	(TTI20)	—
IMR7S/IMCR7S	—	TUNI2	TUNI1	TUNI0	—	—	—	—

Register Name	Bit Name(Function Name)							
	7	6	5	4	3	2	1	0
IMR7SA/IMCR7SA	—	(TMU)			—	—	—	—
IMR8S/IMCR8S	—	—	—	—	—	—	—	—
IMR8SA/IMCR8SA	—	—	—	—	—	—		—)
IMR9S/IMCR9S	—	RWDT0	CMT2	CMT0	DTEI2	WAITI2	TACKI2	ALI2
IMR9SA/IMCR9SA	—	(RWDT0)	(CMT2)	(CMT0)	(IIC2)			
IMR10S/IMCR10S IMR10SA/IMCR10SA	—	—	IPMMUR2	IPMMUR	—	—	—	—
	(IPMMU)				—	—	—	—
IMR11S/IMCR11S	DTEI0	WAITI0	TACKI0	ALI0	—	TSIF1	LMB	TSIF0
IMR11SA/IMCR11SA	(IIC0)				—	(TSIF1)	(LMB)	(TSIF0)
IMR12S/IMCR12S	—	—	—	—	—	—	—	—
IMR12SA/IMCR12SA	—	—	—	—	—	—	(PINTCS)	
IMR0S3/IMCR0S3	DEI0	DEI1	DEI2	DEI3	DEI4	DEI5	DADERR	—
IMR0SA3/IMCR0SA3	RTDMAC2(1)				RTDMAC2(2)			—
IMR1S3/IMCR1S3	—	—	—	—	—	—	—	—
IMR1SA3/IMCR1SA3	—	—	—	—	—	—	—	—
IMR2S3/IMCR2S3	—	—	—	—	—	—	—	—
IMR2SA3/IMCR2SA3	—	—	—	—	—	—	—	—
IMR3S3/IMCR3S3	—	—	—	—	—	—	—	—
IMR3SA3/IMCR3SA3	—	—	—	—	—	—	—	—
IMR4S3/IMCR4S3	—	—	—	—	LCDC1	CSIRX	DSITX0[*1]	DSITX1[*2]
IMR4SA3/IMCR4SA3	—	ISP	—	—	LCDC1	CSIRX	DSITX	
IMR5S3/IMCR5S3	SPU0	SPU1	FSI	FMSI	—	—	—	HDMI
IMR5SA3/IMCR5SA3	SPU2		FSI	FMSI	—	—	—	HDMI
IMR6S3/IMCR6S3 IMR6SA3/IMCR6SA3	TUNI10	TUNI11	TUNI12	—	CMT4	DSITX1_0	DSITX1_1	—
	TMU1			—	CMT4	DSITX1		—
IMR7S3/IMCR7S3 IMR7SA3/IMCR7SA3	MFIS2	CPORTS2R	CEC_1	CEC_2	JPU6E	—	—	—
	MFIS2	CPORTS2R	CEC		JPU6E	—	—	—

Note: —: Reserved. An undefined value will be read. Writing is ignored.

* Bit 1 of IMR6AS/IMCR6AS is reserved. In the AP-System core, the TTI20 interrupt should be handled directly by the INTCA.

(34) User Interrupt Mask Level Register S (USERIMASKS)

USERIMASKS is a register that specifies the level of interrupts to be accepted. As this register is allocated to a 64-Kbyte page that differs from the area of the other INTCS registers, only USERIMASKS can be accessed in user mode by translating its address to the corresponding address in area 7 through the MMU.

When the level of an interrupt is not higher than the interrupt level specified in the UIMASKS bit, the interrupt is masked. The interrupt with a higher level than that specified in the UIMASKS bit is accepted only when the corresponding interrupt mask bit in the interrupt mask register is 0 (interrupt enabled) and the IMASK bit setting in SR is lower than the level of that interrupt. The UIMASKS value does not change even after an interrupt is accepted.

This register is initialized to H'00000000 (all interrupts enabled) by a power-on reset or a manual reset. To prevent unintentional modification, this register can only be written to with bits 31 to 24 set to H'A5.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	UIMASKS				-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R/W	Reserved These bits are always read as 0. Be sure to write H'A5 to these bits when writing to the UIMASKS bit.
23 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 4	UIMASKS	0000	R/W	User Interrupt Mask Level When the level of an interrupt is not higher than this value, the interrupt is masked.
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

(35) AP-System Core Individual Interrupt Source Register (INTEVTSA)

INTEVTSA is a read-only register that indicates the code for the source of the interrupt sent from each peripheral module assigned to the INTCS to the AP-System core.

For the interrupt source code, refer to the list of INTCS interrupt sources (table 5.13). The interrupt signals from the peripheral modules assigned to the INTCS are combined into one signal, and this signal is sent to the INTCA as a peripheral interrupt. The code for this interrupt signal is H'0F80 as shown in the list of INTCA interrupt sources (table 5.11). When the AP-System core accepts this interrupt, the AP-System core can process the peripheral interrupt assigned to the INTCS by reading this register within the AP-System interrupt handler.

The interrupt signal sent from the INTCS to the AP-System core can be masked by the INTSMASK setting.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	EVTCODESA									-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13 to 5	EVTCODESA	H'000	R/W	Interrupt Code These bits hold the interrupt code. For details, see table 5.13.
4 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

(36) NMI Flag Control Register S (NMIFCRS)

NMIFCRS is a register that has an NMI flag (NMIFL bit) that can be read and cleared by software. The NMIFL bit is automatically set to 1 by hardware when the INTCS detects an NMI. This bit can be cleared by writing 0 through software and the NMI request detected by the INTCS is also canceled.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NMIL	-	-	-	-	-	-	-	-	-	-	-	-	-	-	NMIFL
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	NMIL	0	R	NMI Input Level Indicates the level of the NMI signal set by the SFTNMI bit in SYSTBCR of the CPGA. This bit cannot be modified. 0: NMI signal is set low 1: NMI signal is set high
14 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	NMIFL	0	R/W	NMI Interrupt Request Detection Indicates whether an NMI interrupt request signal has been detected. This bit is automatically set to 1 when the INTCS detects an NMI interrupt request. Write 0 to clear the bit. Writing 1 is ignored. 0: NMI interrupt request has not been detected 1: NMI interrupt request has been detected

(37) AP-System Core Interrupt Mask Register (INTAMASK)

INTAMASK indicates whether to mask all interrupts sent to the AP-Realtime core from the peripheral modules on the INTCA side. INTAMASK is located in the INTCS and controlled by the AP-Realtime core. When the MASK bit in this register is set to 1, no interrupts are sent to the AP-Realtime core regardless of the IMCR*AS setting.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	MASK
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	MASK	0	R/W	Interrupt Mask Indicates masking of interrupt requests sent to the AP-Realtime core. When reading: 0: Interrupt requests are not masked 1: Interrupt requests are masked

(38) Pulse Interrupt Flag Register 0S (IFLG0S)

IFLG0S is a register that has a flag bit for indicating the TTI20 interrupt request to the AP-Realtime core. This bit does not change when the TTI20 interrupt is masked with IMR6S.

The interrupt request can be cleared by writing 0 to the TTI20 bit after reading TTI20 = 1.

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	TTI20
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	TTI20	0	R/W	TTI20 Interrupt Request Indicates a TTI20 interrupt request. When reading: 0: No TTI20 interrupt has been requested to the AP-Realtime core 1: A TTI20 interrupt request has been requested to the AP-Realtime core When writing: 0: Cleared to 0 only after reading 1 1: Writing 1 is ignored

(39) Pseudo-Interrupt Setting Register 0A (SIR0A)

SIR0A is a register to generate an interrupt from a source that is different from the usual one for a specific interrupt.

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	TTI20
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	TTI20	0	R/W	TTI20 Pseudo-Interrupt Setting This bit can be used to debug the TTI20 interrupt routine when the BB side is stopped. 0: TTI20 interrupt 1: RCLK is changed to a TTI20 interrupt detection signal

5.4 Interrupt Sources

There are two types of interrupt sources: IRQ pins, on-chip peripheral modules. Each interrupt has a priority level (15 to 0), with 15 the highest and 1 the lowest. Priority level 0 masks an interrupt, so the interrupt request is ignored.

5.4.1 NMI Interrupt

For the AP-Realtime core, an NMI interrupt can be set by software (SYSTBCR.SFTNMI of CPG). Interrupt request is detected by changing bit value from 1 to 0. NMI interrupt is reserved while SR.BL is 1. SR.IMASK is set automatically when CPUOPM.INTMU or AP-Realtime core is 1. SR.IMASK is not changed when CPUOPM.INTMU is 0.

5.4.2 IRQ pins Interrupts

(a) Interrupts to AP-System Core

IRQ pin interrupts are input from pins IRQ31 to IRQ0, which can be used to request wakeup from the power cutoff state. Sixteen interrupts are sent to the AP-System core separately, and a mask and a priority level can be specified for each interrupt. When level-detection mode is selected for IRQ interrupts by the IRQnSA bits (n = 0 to 7) in ICR1A, IRQnSA bits (n = 8 to 15) in ICR2A, IRQnSA bits (n = 16 to 23) in ICR3A and IRQnSA bits (n = 24 to 31) in ICR4A the pin levels must be retained until the interrupts are accepted and interrupt handling starts. Note that even when edge-detection mode is selected for IRQ pin interrupts, if an interrupt signal pulse width is less than three ZBϕ clock cycles, the interrupt may not be detected. The time it takes for the INTC to detect an interrupt and send it to the CPU is six ZBϕ clock cycles when the INTC is operating. In the case of level detection with the INTC halted, standby cancellation is requested in three RCLK cycles, and in the case of edge detection with the INTC halted, an interrupt is detected immediately by gate delay and standby cancellation is requested. When an IRQ pin is used to request wakeup from the power cutoff state, an IRQ interrupt is generated according to the INTCA register setting after power has been restored.An IRQ interrupt can also be used to request wakeup from the C5 area power cutoff state. In this case, an interrupt occurs because the source is retained.

When an IRQ pins interrupt is accepted by the AP-System core, an IRQ exception is generated in the AP-System core and the IRQ exception interrupt handler is initiated. The IRQ exception handler must first read INTFLGA, which automatically modifies the INTLVLA value to the level of the accepted interrupt and saves the previous INTLVLA value in INTLVLB. The code of the accepted interrupt is stored in INTEVTA. Note that INTFLGA must be read only once. If it is read multiple times, the interrupt flag may be cleared unexpectedly.

(b) Interrupts to AP-Realtime Core

Thirty-two IRQ pin interrupts are also sent to the AP-Realtime core separately, and a mask and a priority level can be specified for each interrupt. When level-detection mode is selected for IRQ interrupts by the IRQnSS bits (n = 0 to 7) in ICR0S , IRQnSS bits (n = 8 to 15) in ICR1S, IRQnSS bits (n = 16 to 23) in ICR2S and IRQnSS bits (n = 24 to 31) in ICR3S , the pin levels must be retained until the interrupts are accepted and interrupt handling starts. Note that even when edge-detection mode is selected for IRQ pins interrupts, if an interrupt signal pulse width is less than three Bϕ clock cycles, the interrupt may not be detected. The time it takes for the INTC to detect an interrupt and send it to the CPU is six ZBϕ clock cycles when the INTC is operating. In the case of level detection with the INTC halted, standby cancellation is requested in three RCLK cycles, and in the case of edge detection with the INTC halted, an interrupt is detected immediately by gate delay and standby cancellation is requested. When an IRQ pin is used to request wakeup from the power cutoff state, an IRQ pins interrupt is generated according to the INTCS register setting after power has been restored. An IRQ pins interrupt can also be used to request wakeup from the C5 area power cutoff state. In this case, an interrupt occurs because the source is retained.

When an IRQ pins interrupt is accepted by the AP-Realtime core, a general exception is generated in the AP-Realtime core and the exception handler is initiated.

When the INTMU bit in the CPU operating mode register (CPUOPM) is set to 1, the interrupt mask level (IMASK) in SR is automatically modified to the level of the accepted interrupt. When the INTMU bit is cleared to 0, the IMASK value in SR is not affected by the accepted interrupt.

5.4.3 On-Chip Peripheral Module Interrupts

On-chip peripheral module interrupts are generated in the peripheral modules classified into the following three groups.

1. Modules whose interrupts should be sent to both the SYS domain and RT domain
2. SYS-domain modules
3. RT-domain modules

Group 1 includes the BBIF2,MSU,SPU,FSI,FMSI,KEYSC,RWDT0,CMT2,3DG,MFIS2. For each interrupt generated in these modules, different masks and priority levels can be specified and different interrupt codes are assigned separately in the INTCA and INTCS.

For each interrupt generated in the modules in group 2, a mask and priority level can be specified in the INTCA and a unique interrupt code is assigned. The interrupts are also sent to the INTCS through one combined signal. For each of the combined interrupts, a mask can be specified

independently from the mask setting for the INTCA and the priority level specified in the INTCA is applied. The AP-Realtime core can identify the individual interrupt source by reading INTEVTAS within the interrupt handler and process the SYS-domain interrupt.

For each interrupt generated in the modules in group 3, a mask and priority level can be specified in the INTCS and a unique interrupt code is assigned. The interrupts are also sent to the INTCA through one combined signal. For each of the combined interrupts, a mask can be specified independently from the mask setting for the INTCS and the priority level specified in the INTCS is applied. The AP-System core can identify the individual interrupt source by reading INTEVTSA within the interrupt handler and process the RT-domain interrupt.

(a) Peripheral Module Interrupts in AP-System

A priority level (from 15 to 0) can be set for each module by writing to IPRAA to IPROA. Not every interrupt source is assigned a different interrupt vector. Sources are reflected in the interrupt flag register (INTFLGA) and then reflected in the interrupt event register (INTEVTA) when INTFLGA is read. It is easy to identify sources by using the value of this code as a branch offset in the exception handling routine.

When an interrupt is sent to the AP-System core, an IRQ exception is generated in the AP-System core and the IRQ exception handler is initiated. The CPU branch destination is determined by the VE bit in the CP15 register c1 of the ARM11 and VTB of the INTCA.

The IRQ exception handler must first read INTFLGA, which automatically modifies the INTLVLA value to the level of the accepted interrupt and saves the previous INTLVLA value in INTLVLB. The code of the accepted interrupt is stored in INTEVTA. Note that INTFLGA must be read only once. If it is read multiple times, the interrupt flag may be cleared unexpectedly.

Hardware determines whether an interrupt is accepted, automatically modifies the INTLVLA value to the level of the accepted interrupt, and saves the previous INTLVLA value in INTLVLB. The code of the accepted interrupt is stored in INTEVTA. The IRQ exception handler must not access INTFLGA.

(b) Peripheral Module Interrupts in AP-Realtime

A priority level (from 15 to 0) can be set for each module by writing to IPRAS to IPRMS and IPRAS3 to IPRRS3. Not every interrupt source is assigned a different interrupt vector. Sources are reflected in the interrupt event register (INTEVT). It is easy to identify sources by using the INTEVT value as a branch offset in the exception handling routine.

When the INTMU bit in CPUOPM is set to 1, the interrupt mask level (IMASK) in SR is automatically modified to the level of the accepted interrupt. When the INTMU bit in CPUOPM is cleared to 0, the IMASK value in SR is not affected by the accepted interrupt.

5.4.4 Notes on Interrupt Clearing and Interrupt Register Settings

The interrupt source flags and interrupt enable bits must be modified only while no interrupts can be accepted. To avoid accepting unintentional interrupts that should have been updated, the necessary internal timing must be ensured by inserting instructions. As shown in (1) and (2) below, read the on-chip peripheral register with the corresponding flag.

If a flag is modified while interrupts can be accepted, execution will branch to the interrupt handling routine with interrupt code = 0; interrupt handling may start depending on the timing relationship between flag updating and interrupt request detection in the LSI. In this case, operation can be continued without causing any problems by returning to the program executed before the branch.

Likewise, care must be taken when modifying the interrupt priority registers and interrupt mask registers. It is recommended to modify these registers while the corresponding interrupt cannot be accepted. After these registers have been modified, if the CPU interrupt settings (the SR register of the AP-RT core and the CPSR register of the AP-System core) are changed and if the order of the action of modifications should be observed, the necessary internal timing can be ensured by reading the modified INTC register once.

(a) ARM Accepting an Interrupt (Including Accepting via INTCS)

After the instruction for clearing an interrupt flag, read that flag register or read a register in the INTCA once. In either case, insert at least one instruction before the SUBS PC, R14, #4 instruction.

(b) SH Accepting an Interrupt (Including Accepting via INTCA)

After the instruction for clearing an interrupt flag, read that flag register twice, or read that flag register once and then read a register in the INTCS once.

Note: About “The corresponding interrupt cannot be accepted”

(1) When ARM can accept interrupt

(2) When SH can accept interrupt

5.4.5 Interrupt Exception Handling and Priority

Tables 5.10 and 5.11 show the interrupt sources, interrupt codes (codes for INTFLGA and INTEVTA), and the interrupt priority in the INTCA. Tables 5.12 and 5.13 show the interrupt sources, codes for the interrupt event register (INTEVT), and the interrupt priority in the INTCS.

The start address of the exception handling routine is common for all interrupt sources. This is why, for instance, the value of INTFLGA or INTEVT is used as an offset at the start of the exception handling routine to branch execution in order to identify the interrupt source.

The start address of the exception handling routine can be set through software using bits 31 to 2 in VTB. In addition, by setting bits 1 and 0 in VTB to 2'b01 or 2'b10 to select the offset mode, a branch can be made to the address indicated by bits 31 to 2 in VTB + (interrupt code value/8) or the address indicated by bits 31 to 2 in VTB + (interrupt code value); different address for each interrupt (vector interrupt).

On-chip peripheral module interrupt priority levels can be set freely between 15 and 0 for each module by using IPRAA to IPROA, IPRAA3 to IPRUA3, IPRAS to IPRMS and IPRAS3 to IPRPS3. A reset assigns priority level 0 to the on-chip peripheral module interrupts.

If the same priority level is assigned to two or more interrupt sources and interrupts from those sources occur simultaneously, their priority is determined according to the default priority indicated in tables 5.11 to 5.13.

Table 5.10 External Interrupt Sources and Priority (INTCA)

Interrupt Source		INTEVT Code	Interrupt Priority (Initial Value)	IPR (Bit Numbers)	Priority within IPR Setting Range	Default Priority
IRQ	IRQ0A	H'0200	15～0(0)	INTPRI00A(31～28)	–	High
	IRQ1A	H'0220	15～0(0)	INTPRI00A(27～24)	–	
	IRQ2A	H'0240	15～0(0)	INTPRI00A(23～20)	–	
	IRQ3A	H'0260	15～0(0)	INTPRI00A(19～16)	–	
	IRQ4A	H'0280	15～0(0)	INTPRI00A(15～12)	–	
	IRQ5A	H'02A0	15～0(0)	INTPRI00A(11～8)	–	
	IRQ6A	H'02C0	15～0(0)	INTPRI00A(7～4)	–	
	IRQ7A	H'02E0	15～0(0)	INTPRI00A(3～0)	–	
	IRQ8A	H'0300	15～0(0)	INTPRI10A(31～28)	–	
	IRQ9A	H'0320	15～0(0)	INTPRI10A(27～24)	–	
	IRQ10A	H'0340	15～0(0)	INTPRI10A(23～20)	–	
	IRQ11A	H'0360	15～0(0)	INTPRI10A(19～16)	–	
	IRQ12A	H'0380	15～0(0)	INTPRI10A(15～12)	–	
	IRQ13A	H'03A0	15～0(0)	INTPRI10A(11～8)	–	
	IRQ14A	H'03C0	15～0(0)	INTPRI10A(7～4)	–	
	IRQ15A	H'03E0	15～0(0)	INTPRI10A(3～0)	–	
	IRQ16A	H’3200	15～0(0)	INTPRI20A(31～28)	–	
	IRQ17A	H’3220	15～0(0)	INTPRI20A(27～24)	–	
	IRQ18A	H’3240	15～0(0)	INTPRI20A(23～20)	–	
	IRQ19A	H’3260	15～0(0)	INTPRI20A(19～16)	–	
	IRQ20A	H’3280	15～0(0)	INTPRI20A(15～12)	–	
	IRQ21A	H’32A0	15～0(0)	INTPRI20A(11～8)	–	
	IRQ22A	H’32C0	15～0(0)	INTPRI20A(7～4)	–	
	IRQ23A	H’32E0	15～0(0)	INTPRI20A(3～0)	–	
	IRQ24A	H’3300	15～0(0)	INTPRI30A(31～28)	–	
	IRQ25A	H’3320	15～0(0)	INTPRI30A(27～24)	–	
	IRQ26A	H’3340	15～0(0)	INTPRI30A(23～20)	–	
	IRQ27A	H’3360	15～0(0)	INTPRI30A(19～16)	–	
	IRQ28A	H’3380	15～0(0)	INTPRI30A(15～12)	–	
	IRQ29A	H’33A0	15～0(0)	INTPRI30A(11～8)	–	
	IRQ30A	H’33C0	15～0(0)	INTPRI30A(7～4)	–	
	IRQ31A	H’33E0	15～0(0)	INTPRI30A(3～0)	–	Low

Table 5.11 On-Chip Peripheral Module Interrupt Sources and Priority (INTCA)

Interrupt Source		INTEVT Code	Interrupt Priority (Initial Value)	IPR (Bit Numbers)	Priority within IPR Setting Range	Default Priority
INTCA	DIRC	H'0560	15～0(0)	IPROA(7～4)	–	High
Crypt*[1]	STD	H'0700	15～0(0)	IPRCA(11～8)	–	
IIC1	ALI1	H'0780	15～0(0)	IPRIA(3～0)	High	
	TACKI1	H'07A0	15～0(0)			
	WAITI1	H'07C0	15～0(0)			
	DTEI1	H'07E0	15～0(0)		Low	
AP-ARM	IRQPMU	H'0800	15～0(0)	IPRCA(3～0)	High	
	COMMTX	H'0840	15～0(0)			
	COMMRX	H'0860	15～0(0)		Low	
MFI	ACMFI1/2	H'0900	15～0(0)	IPREA(7～4)	–	
MFIS	MFIS(MFIINT)	H'0920	15～0(0)	IPREA(11～8)	–	
BBIF1	BBIF1	H'0940	15～0(0)	IPRBA(7～4)	–	
BBIF2	BBIF2	H'0960	15～0(0)	IPRBA(3～0)	–	
USBHSDMAC	USHDMI	H'0A00	15～0(0)	IPRHA(11～8)	–	
3DG	SGX540	A'0A60	15～0(0)	IPRFA(7～4)	–	
CMT1	CMT10	H'0B00	15～0(0)	IPRFA(3～0)	–	
	CMT11	H'0B20	15～0(0)	IPRCA(7～4)	–	
	CMT12	H'0B40	15～0(0)	IPRDA(7～4)	–	
	CMT13	H'0B60	15～0(0)	IPRKA(11～8)	–	
CMT2	CMT2	H'0B80	15～0(0)	IPRAA(7～4)	–	
CMT3	CMT3	H'0BA0	15～0(0)	IPRMA(11～8)	–	
KEYSC	KEY	H'0BE0	15～0(0)	IPRFA(15～12)	–	
SCIFA0	SCIFA0	H'0C00	15～0(0)	IPRGA(15～12)	–	
SCIFA1	SCIFA1	H'0C20	15～0(0)	IPRGA(11～8)	–	
SCIFA2	SCIFA2	H'0C40	15～0(0)	IPRGA(7～4)	–	
SCIFA3	SCIFA3	H'0C60	15～0(0)	IPRGA(3～0)	–	
MSIOF2	MSIOF2	H'0C80	15～0(0)	IPRHA(15～12)	–	
MSIOF1	MSIOF1	H'0D00	15～0(0)	IPRIA(15～12)	–	Low

Interrupt Source		INTEVT Code	Interrupt Priority (Initial Value)	IPR (Bit Numbers)	Priority within IPR Setting Range	Default Priority
SCIFA4	SCIFA4	H'0D20	15～0(0)	IPRIA(11～8)	–	high
SCIFA5	SCIFA5	H'0D40	15～0(0)	IPRNA(11～8)	–	
SCIFB	SCIFB	H'0D60	15～0(0)	IPRNA(15～12)	–	
FLCTL	FLSTEI	H'0D80	15～0(0)	IPRHA(7～4)	High	
	FLTENDI	H'0DA0	15～0(0)			
	FLTREQ0I	H'0DC0	15～0(0)			
	FLTREQ1I	H'0DE0	15～0(0)		Low	
SDHI0	SDHI0I0	H'0E00	15～0(0)	IPRHA(3～0)	High	
	SDHI0I1	H'0E20	15～0(0)			
	SDHI0I2	H'0E40	15～0(0)			
	SDHI0I3	H'0E60	15～0(0)		Low	
SDHI1	SDHI1I0	H'0E80	15～0(0)	IPRKA(3～0)	High	
	SDHI1I1	H'0EA0	15～0(0)			
	SDHI1I2	H'0EC0	15～0(0)		Low	
–	–	H'0F60	15～0(0)	IPRKA(7～4)	–	
IrDA	IrDA	H'0480	15～0(0)	IPRBA(15～12)	–	
TPU0	TPU0	H'04A0	15～0(0)	IPRLA(15～12)	–	
TTI20	TTI20	H'1100	15～0(0)	IPRJA(3～0)	–	
DDM	DDM	H'1140	15～0(0)	IPRNA(3～0)	–	
SDHIF2	SDHI2I0	H'1200	15～0(0)	IPROA[3:0]	High	
	SDHI2I1	H'1220	15～0(0)			
	SDHI2I2	H'1240	15～0(0)			
	SDHI2I3	H'1260	15～0(0)		Low	Low

Interrupt Source		INTEVT Code	Interrupt Priority (Initial Value)	IPR (Bit Numbers)	Priority within IPR Setting Range	Default Priority
RWDT0	RWDT0	H'1280	15～0(0)	IPRMA(3～0)	–	High
DMAC1(1)	DEI0	H'2000	15～0(0)	IPREA(15～12)	High	
	DEI1	H'2020	15～0(0)			
	DEI2	H'2040	15～0(0)			
	DEI3	H'2060	15～0(0)		Low	
DMAC1(2)	DEI4	H'2080	15～0(0)	IPRFA(11～8)	High	
	DEI5	H'20A0	15～0(0)			
	DADERR	H'20C0	15～0(0)		Low	
DMAC2(1)	DEI0	H'2100	15～0(0)	IPRJA(15～12)	High	
	DEI1	H'2120	15～0(0)			
	DEI2	H'2140	15～0(0)			
	DEI3	H'2160	15～0(0)		Low	
DMAC2(2)	DEI4	H'2180	15～0(0)	IPRJA(11～8)	High	
	DEI5	H'21A0	15～0(0)			
	DADERR	H'21C0	15～0(0)		Low	
DMAC3(1)	DEI0	H'2200	15～0(0)	IPRAA(15～12)	High	
	DEI1	H'2220	15～0(0)			
	DEI2	H'2240	15～0(0)			
	DEI3	H'2260	15～0(0)		Low	
DMAC3(2)	DEI4	H'2280	15～0(0)	IPRAA(11～8)	High	
	DEI5	H'22A0	15～0(0)			
	DADERR	H'22C0	15～0(0)		Low	
SHWYSTAT	SHWYSTAT(RT)	H'1300	15～0(0)	IPRAA3(15～12)	High	
	SHWYSTAT(HS)	H'1320	15～0(0)			
	SHWYSTAT(Com)	H'1340	15～0(0)		Low	
HDMI	HDMI	H'17E0	15～0(0)	IPRJA3(3～0)	–	
SPU2	SPU0	H'1800	15～0(0)	IPRKA3(15～12)	High	
	SPU1	H'1820	15～0(0)		Low	
FSI	FSI	H'1840	15～0(0)	IPRKA3(7～4)	–	
FMSI	FMSI	H'1860	15～0(0)	IPRKA3(3～0)	–	
MIPI-HSI	MIPI-HSI	H'18E0	15～0(0)	IPRLA3(3～0)	–	Low

Interrupt Source		INTEVT Code	Interrupt Priority (Initial Value)	IPR (Bit Numbers)	Priority within IPR Setting Range	Default Priority
IPMMU	IPMMUD	H'1920	15～0(0)	IPRMA3(15～12)	–	High
CEC	CEC_1	H'1940	15～0(0)	IPRMA3(7～4)	High	
	CEC_2	H'1960	15～0(0)	IPRMA3(3～0)	Low	
AP-ARM	CTIIRQ	H'1980	15～0(0)	IPRNA3(15～12)	High	
	DMAEXTERRIRQ	H'19A0	15～0(0)			
	DMAIRQ	H'19C0	15～0(0)			
	DMASIRQ	H'19E0	15～0(0)		Low	
MFIS2	MFIS2	H'1A00	15～0(0)	IPROA3(15～12)	–	
CPORTR2S	CPORTR2S	H'1A20	15～0(0)	IPROA3(11～8)	–	
CMT14	CMT14	H'1A40	15～0(0)	IPROA3(7～4)	–	
CMT15	CMT15	H'1A60	15～0(0)	IPROA3(3～0)	–	
MMC	MMC_ERR	H'1AC0		IPRPA3(7～4)	High	
	MMC_NOR	H'1AE0		IPRPA3(3～0)	Low	
I2C(4)	ALI4	H'1B00	15～0(0)	IPRQA3(15～12)	High	
	TACKI4	H'1B20		IPRQA3(11～8)		
	WAITI4	H'1B40		IPRQA3(7～4)		
	DTEI4	H'1B60		IPRQA3(3～0)	Low	
I2C(3)	ALI3	H'1B80	15～0(0)	IPRRA3(15～12)	High	
	TACKI3	H'1BA0		IPRRA3(11～8)		
	WAITI3	H'1BC0		IPRRA3(7～4)		
	DTEI3	H'1BE0		IPRRA3(3～0)	Low	
USB0	USBI1 (ch0)	H'1C80	15～0(0)	IPRTA3(15～12)	High	
	USBI0 (ch0)	H'1CA0		IPRTA3(11～8)	Low	
USB1	USBI1 (ch1)	H'1CC0	15～0(0)	IPRTA3(7～4)	High	
	USBI0 (ch1)	H'1CE0		IPRTA3(3～0)	Low	
USBHSDMAC1	USHDMI	H'1D00	15～0(0)	IPRUA3(15～12)	–	
INTCS	INTCS	H'0F80	15～0(0)	–	–	Low

*1 in case CC5INT bit of LIFEC_SEC_SRC is 0

Table 5.12 External Interrupt Sources and Priority (INTCS)

Interrupt Source		INTEVT Code	Interrupt Priority (Initial Value)	IPR (Bit Numbers)	Priority within IPR Setting Range	Default Priority
NMI*		H'01C0	16		–	–
IRQ	IRQ0S	H'0200	15～0(0)	INTPRI00S(31～28)	–	High
	IRQ1S	H'0220	15～0(0)	INTPRI00S(27～24)	–	
	IRQ2S	H'0240	15～0(0)	INTPRI00S(23～20)	–	
	IRQ3S	H'0260	15～0(0)	INTPRI00S(19～16)	–	
	IRQ4S	H'0280	15～0(0)	INTPRI00S(15～12)	–	
	IRQ5S	H'02A0	15～0(0)	INTPRI00S(11～8)	–	
	IRQ6S	H'02C0	15～0(0)	INTPRI00S(7～4)	–	
	IRQ7S	H'02E0	15～0(0)	INTPRI00S(3～0)	–	
	IRQ8S	H'0300	15～0(0)	INTPRI10S(31～28)	–	
	IRQ9S	H'0320	15～0(0)	INTPRI10S(27～24)	–	
	IRQ10S	H'0340	15～0(0)	INTPRI10S(23～20)	–	
	IRQ11S	H'0360	15～0(0)	INTPRI10S(19～16)	–	
	IRQ12S	H'0380	15～0(0)	INTPRI10S(15～12)	–	
	IRQ13S	H'03A0	15～0(0)	INTPRI10S(11～8)	–	
	IRQ14S	H'03C0	15～0(0)	INTPRI10S(7～4)	–	
	IRQ15S	H'03E0	15～0(0)	INTPRI10S(3～0)	–	
	IRQ16S	H'3200	15～0(0)	INTPRI20S(31～28)	–	
	IRQ17S	H'3220	15～0(0)	INTPRI20S(27～24)	–	
	IRQ18S	H'3240	15～0(0)	INTPRI20S(23～20)	–	
	IRQ19S	H'3260	15～0(0)	INTPRI20S(19～16)	–	
	IRQ20S	H'3280	15～0(0)	INTPRI20S(15～12)	–	
	IRQ21S	H'32A0	15～0(0)	INTPRI20S(11～8)	–	
	IRQ22S	H'32C0	15～0(0)	INTPRI20S(7～4)	–	
	IRQ23S	H'32E0	15～0(0)	INTPRI20S(3～0)	–	
	IRQ24S	H'3300	15～0(0)	INTPRI30S(31～28)	–	
	IRQ25S	H'3320	15～0(0)	INTPRI30S(27～24)	–	
	IRQ26S	H'3340	15～0(0)	INTPRI30S(23～20)	–	
	IRQ27S	H'3360	15～0(0)	INTPRI30S(19～16)	–	
	IRQ28S	H'3380	15～0(0)	INTPRI30S(15～12)	–	
	IRQ29S	H'33A0	15～0(0)	INTPRI30S(11～8)	–	
	IRQ30S	H'33C0	15～0(0)	INTPRI30S(7～4)	–	Low

Interrupt Source		INTEVT Code	Interrupt Priority (Initial Value)	IPR (Bit Numbers)	Priority within IPR Setting Range	Default Priority
	IRQ31S	H'33E0	15～0(0)	INTPRI30S(3～0)	–	Low

*depend on CPGA.SYSTBCR.SFTNMI

Table 5.13 On-Chip Peripheral Module Interrupt Sources and Priority (INTCS)

Interrupt Source		INTEVT Code	Interrupt Priority (Initial Value)	IPR (Bit Numbers)	Priority within IPR Setting Range	Default Priority
VEU	VEU0	H'0700	15～0(0)	IPRHS(7～4)	High	High
	VEU1	H'0720	15～0(0)		↕	↕
	VEU2	H'0740	15～0(0)		↕	↕
	VEU3	H'0760	15～0(0)		Low	↕
—	—	—	—	—	—	↕
RTDMAC(1)	DEI0	H'0800	15～0(0)	IPRES(15～12)	High	↕
	DEI1	H'0820	15～0(0)		↕	↕
	DEI2	H'0840	15～0(0)		↕	↕
	DEI3	H'0860	15～0(0)		Low	↕
CEU	CEU	H'0880	15～0(0)	IPRES(11～8)	—	↕
BEU	BEU0	H'08A0	15～0(0)	IPRHS(3～0)	High	↕
	BEU1	H'08C0	15～0(0)		↕	↕
	BEU2	H'08E0	15～0(0)		Low	↕
MFI	MFI	H'0900	15～0(0)	IPRES(7～4)	—	↕
BBIF2	BBIF2	H'0960	15～0(0)	IPRCS(15～12)	—	↕
VPU	VPU	H'0980	15～0(0)	IPRES(3～0)	—	↕
TSIF1	TSIF1	H'09A0	15～0(0)	IPRGS(3～0)	—	↕
3DG	SGX540	H'09E0	15～0(0)	IPRJS(11～8)	—	↕
2DDMAC	2DDMAC	H'0A00	15～0(0)	IPRAS(7～4)	High	↕
	—	—	—		↕	↕
	—	—	—		↕	↕
	—	—	—		Low	↕
IIC2	ALI2	H'0A80	15～0(0)	IPRMS(15～12)	High	↕
	TACKI2	H'0AA0	15～0(0)		↕	↕
	WAITI2	H'0AC0	15～0(0)		↕	↕
	DTEI2	H'0AE0	15～0(0)		Low	↕
IPMMU	IPMMUR	H'0B00	15～0(0)	IPRLS(15～12)	High	↕
	IPMMUR2	H'0B20	15～0(0)		↕	↕
					Low	↕
RTDMAC(2)	DEI4	H'0B80	15～0(0)	IPRFS(11～8)	High	↕
	DEI5	H'0BA0	15～0(0)		↕	↕
	DADERR	H'0BC0	15～0(0)		Low	Low

Interrupt Source		INTEVT Code	Interrupt Priority (Initial Value)	IPR (Bit Numbers)	Priority within IPR Setting Range	Default Priority
KEYSC	KEY	H'0BE0	15～0(0)	IPRFS(15～12)	—	Low

Interrupt Source		INTEVT Code	Interrupt Priority (Initial Value)	IPR (Bit Numbers)	Priority within IPR Setting Range	Default Priority
TTI20	TTI20	H'0C80	15～0(0)	IPRHS(15～12)	–	High
MSIOF	MSIOF	H'0D20	15～0(0)	IPRIS(11～8)	–	
IIC0	ALI0	H'0E00	15～0(0)	IPRIS(3～0)	高	
	TACKI0	H'0E20	15～0(0)			
	WAITI0	H'0E40	15～0(0)			
	DTEI0	H'0E60	15～0(0)		低	
TMU	TUNI0	H'0E80	15～0(0)	IPRGS(15～12)	–	
	TUNI1	H'0EA0	15～0(0)	IPRGS(11～8)	–	
	TUNI2	H'0EC0	15～0(0)	IPRGS(7～4)	–	
CMT0	CMT0	H'0F00	15～0(0)	IPRFS(3～0)	–	
TSIF0	TSIF0	H'0F20	15～0(0)	IPRIS(7～4)	–	
CMT2	CMT2	H'0F40	15～0(0)	IPRFS(7～4)	–	
LMB	LMB	H'0F60	15～0(0)	IPRKS(7～4)	–	
CTI	CTI	H’0400	15～0(0)	IPRAS(15～12)	–	
RWDT0	RWDT0	H'0440	15～0(0)	IPRMS(3～0)	–	
ICB	ICB	H'0480	15～0(0)	IPRAS(3～0)	–	
JPU	JPEG	H'0560	15～0(0)	IPRBS(15～12)	–	
LCDC	LCDC	H'0580	15～0(0)	IPRBS(11～8)	–	
LCRC	LCRC	H'05A0	15～0(0)	IPRBS(3～0)	–	
RTDMAC2(1)	DEI0	H'1300	15～0(0)	IPRAS3(15～12)	High	
	DEI1	H'1320	15～0(0)			
	DEI2	H'1340	15～0(0)			
	DEI3	H'1360	15～0(0)		Low	
RTDMAC2 (2)	DEI4	H'1380	15～0(0)	IPRBS3(15～12)	High	
	DEI5	H'13A0	15～0(0)			
	DADERR	H'13C0	15～0(0)		Low	
ISP	ISP	H'1720	15～0(0)	IPRIS3(11～8)	–	
LCDC1	LCDC1	H’1780	15～0(0)	IPRJS3(15～12)	–	
CSIRX	CSIRX	H’17A0	15～0(0)	IPRJS3(11～8)	–	
DSITX	DSITX0*1	H’17C0	15～0(0)	IPRJS3(7～4)	High	
	DSITX1*2	H’17E0	15～0(0)		Low	
SPU2	SPU0	H’1800	15～0(0)	IPRKS3(15～12)	High	Low

Interrupt Source		INTEVT Code	Interrupt Priority (Initial Value)	IPR (Bit Numbers)	Priority within IPR Setting Range	Default Priority
	SPU1	H'1820	15～0(0)		Low	High
FSI	FSI	H'1840	15～0(0)	IPRKS3(7～4)	–	
FMSI	FMSI	H'1860	15～0(0)	IPRKS3(3～0)	–	
HDMI	HDMI	H'18E0	15～0(0)	IPRLS3(3～0)	–	
TMU1	TUNI10	H'1900	15～0(0)	IPRMS3(15～12)	High	
	TUNI11	H'1920	15～0(0)			
	TUNI12	H'1940	15～0(0)		Low	
CMT4	CMt4	H'1980	15～0(0)	IPRNS3(15～12)	–	
DSITX1	DSITX1_0	H'19A0	15～0(0)	IPRNS3(11～8)	High	
	DSITX1_1	H'19C0		IPRNS3(7～4)	Low	
MFIS2	MFIS2	H'1A00	15～0(0)	IPROS3(15～12)	–	
CPORTS2R	CPORTS2R	H'1A20	15～0(0)	IPROS3(11～8)	–	
CEC	CEC_1	H'1A40	15～0(0)	IPROS3(7～4)	High	
	CEC_2	H'1A60		IPROS3(3～0)	Low	
JPU6E	JPU6E	H'1A80	15～0(0)	IPRPS3(15～12)	–	
INTCA	INTCA	H'FE0	–	–	–	Low

*1 DSITX0 : DSI-L-Bridge interrupt
*2 DSITX1 : DSI-LINK interrupt

5.5 Operation

5.5.1 INTCA Interrupt Sequence

The sequence of interrupt operations is described below.

1. The interrupt request sources send interrupt request signals to the INTCA.
2. The INTCA selects the highest-priority interrupt from the sent interrupt requests according to the interrupt priority registers. Lower-priority interrupts are held pending. If two of these interrupts have the same priority level or if multiple interrupts occur within a single module, the interrupt with the highest priority is selected according to tables 5.10 and 5.11.
3. The priority level of the selected interrupt is compared with the INTLVLA value. If the priority level is higher than the INTLVLA value, the INTCA accepts the interrupt and sends an interrupt request signal to the AP-System core.
4. The AP-System core accepts an interrupt at a break in instructions.
5. The interrupts are disabled after that, and the program counter (PC) is set to the IRQ exception interrupt handler address.

5.5.2 INTCS Interrupt Sequence

The sequence of interrupt operations is described below.

1. The interrupt request sources send interrupt request signals to the INTCS.
2. The INTCS selects the highest-priority interrupt from the sent interrupt requests according to the interrupt priority registers. Lower-priority interrupts are held pending. If two of these interrupts have the same priority level or if multiple interrupts occur within a single module, the interrupt with the highest priority is selected according to tables 5.12 and 5.13.
3. The priority level of the selected interrupt is compared with the interrupt mask level (IMASK) set in SR of the AP-Realtime core. If the priority level is higher than the level set in IMASK, the INTCS accepts the interrupt and sends an interrupt request signal to the AP-Realtime core.
4. The AP-Realtime core accepts an interrupt at a break in instructions.
5. The interrupt source code is set in the interrupt event register (INTEVT).
6. SR and program counter (PC) are saved in SSR and SPC, respectively. R15 is saved in SGR at this time.
7. The BL, MD, and RB bits in SR are set to 1.
8. Execution jumps to the start address of the interrupt exception handling routine (the sum of the value set in the vector base register (VBR) and H'00000600).

9. In the exception handling routine, execution branches with the INTEVT value used, for example, as its offset in order to identify the interrupt source. This enables execution to branch to the routine for handling the individual interrupt source.

Note: When the INTMU bit in the CPU operating mode register (CPUOPM) is set to 1, the interrupt mask level (IMASK) in SR is automatically set to the level of the accepted interrupt. When the INTMU bit is cleared to 0, the IMASK value in SR is not affected by the accepted interrupt.

5.5.3 INTCA Interrupt Handler

The following shows an example of INTCA handler processing when multiple interrupts are not handled.

(1) Interrupt Handler

1. Save the necessary user register contents in the stack.
2. Read INTFLGA once in the IRQ exception handing routine to identify the interrupt source. If it is read multiple times, the interrupt flag may be cleared unexpectedly.
3. Branch with the INTFLGA value used as an offset.
4. Clear the interrupt source in the interrupt handling routine. Perform necessary interrupt processing.
5. Restore the register contents from the stack. INTLVLA has been set to the level of the interrupt accepted by hardware; read INTLVLB and set the contents in INTLVLA.
6. Restore the PC value from the link register (R14), that is, execute the SUBS PC, R14, #4 instruction.

5.5.4 INTCA Interrupt Handler for Handling Multiple Interrupts

When handling multiple interrupts, an interrupt handling routine should include the following procedures.

1. Save the link register (R14), SPSR, and necessary user register contents in the stack.
2. Read INTFLGA to identify the interrupt source.
3. Save the INTLVLB contents in the stack.
4. Branch to a specific interrupt handling routine for the interrupt source with the INTFLGA value used as an offset.
5. Clear the interrupt source in the interrupt handling routine.

6. Enable interrupts. At this time, INTLVLA is automatically modified to the level of the accepted interrupt.
7. Perform necessary interrupt processing. Interrupts can be nested during this processing.
8. Disable interrupts.
9. Set INTLVLA to the INTLVLB value saved in the stack. Restore the user register contents from the stack. After that, restore the link register and SPSR and return to the program executed before the interrupt.

When these procedures are followed in order, an interrupt of higher priority than the one being handled can be accepted if multiple interrupts occur immediately after step 6. This reduces the interrupt response time for urgent processing.

5.5.5 INTCS Interrupt Handler for Handling Multiple Interrupts

When handling multiple interrupts, an interrupt handling routine should include the following procedures.

1. To identify the interrupt source, branch to a specific interrupt handling routine for the interrupt source with the INTEVT code used as an offset.
2. Clear the interrupt source in the interrupt handling routine.
3. Save the SSR and SPC contents in the stack.
4. Clear the BL bit in SR. When the INTMU bit in CPUOPM is set to 1, the interrupt mask level (IMASK) in SR is automatically modified to the level of the accepted interrupt. When the INTMU bit in CPUOPM is cleared to 0, set the IMASK bit in SR by software to the accepted interrupt level.
5. Perform necessary interrupt processing.
6. Set the BL bit in SR to 1.
7. Restore the SSR and SPC contents from memory.
8. Execute the RTE instruction.

When these procedures are followed in order, an interrupt of higher priority than the one being handled can be accepted if multiple interrupts occur immediately after step 4. This reduces the interrupt response time for urgent processing.

5.5.6 Interrupt Disabling Function in User Mode

Setting the interrupt mask level in USERIMASKA or USERIMASKS disables interrupts having an equal or lower priority level than the specified mask level. This function can disable less-urgent interrupts in a task (such as device driver) operating in user mode to accelerate urgent processing.

USERIMASKA and USERIMASKS are allocated to a 4-Kbyte page that is different from the area of the other INTCA and INTCS registers. When accessing USERIMASKA or USERIMASKS in user mode, translate the address through the MMU. In the system that uses a multitasking OS, processes that can access USERIMASKA or USERIMASKS must be controlled by using memory protection functions of the MMU. When terminating the task or switching to another task, be sure to clear USERIMASKA or USERIMASKS to 0 before quitting the task. If the UIMASKA or UIMASKS bits are left set to a non-zero value, interrupts which are not higher in priority than the UIMASKA or UIMASKS level are held disabled, and correct operation may not be performed (for example, the OS cannot switch tasks).

A sample sequence of user-mode interrupt disabling operation is described below.

1. Classify interrupts into A and B shown below, and assign higher interrupt levels to A than B.
   A. Interrupts that should be accepted in the device driver
      (interrupts used by the OS, such as timer interrupts)
   B. Interrupts that should be disabled in the device driver
2. Make the MMU settings so that the address space including USERIMASKA or USERIMASKS can only be accessed by the device driver in which interrupts should be disabled.
3. Branch to the device driver.
4. Specify the UIMASKA or UIMASKS bits so that interrupts B are masked in the device driver operating in user mode.
5. Perform urgent processing in the device driver.
6. Clear the UIMASKA or UIMASKS bits to 0 to return from the device driver processing.

5.5.7 IRQ Chattering Removal

For signals entering at the IRQ31 to IRQ0 pins, chattering can be removed by setting interrupt control registers 3 to 10(ICR3 to 10). Figure 5.2 shows the timing of a chattering removal circuit for a single IRQ.

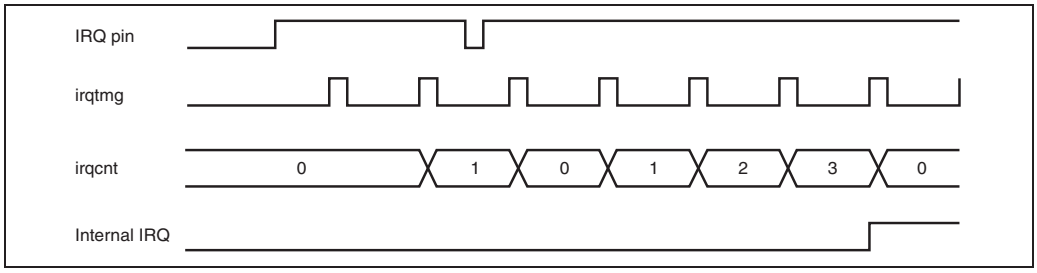


Figure 5.2 Timing of IRQ Chattering Removal Circuit

The operation is entirely based on the EXTALR clock.

The chattering circuit is started when the IRQnSTS2 bits (n = 0 to 31) in interrupt control registers 3 to 10 become something other than H'00. The irqtmg signal, which follows the irqcnt count-up timing, is generated at 1-ms to 8-ms intervals according to IRQnSTS1.

The irqcnt signal inverts all the initial values in the results of the signal detection carried out at EXTALR intervals in the irqtmg period and then counts up when the irqtmg is asserted. In signal detection at EXTALR intervals, if the same value as the initial value is detected within the irqtmg, the irqcnt signal returns to count 0 when the next irqtmg is asserted. When the irqcnt has a value of IRQnSTS2 - 1 and when the irqtmg is asserted, the internal IRQ signal is asserted.

After this, the same operation is repeated with the initial value inverted.

5.6 LSI Internal Communication Interrupts and Wakeup Function (Request to AP Block)

A specified event in the internal connections of the LSI can be used to send a request to the AP-System core for wakeup from the power cutoff state or an interrupt.

A wakeup request is used to start power supply or generate clocks when the power to the AP-System core or INTCA is stopped or when interrupts cannot be accepted because the clock to the AP-System core or INTCA is stopped. When a wakeup request is used to start power supply, execution branches to the reset vector; otherwise, usual interrupt processing is done.

This request is sent together with the interrupt from the MFI to the AP-System core.

5.6.1 LSI Internal Communication Interrupt/Wakeup Function (Request to AP Block) Register Configuration

Table 5.14 shows the LSI internal communication interrupt/wakeup function (request to AP block) register configuration. Table 5.15 shows the register states in each operating mode.

Table 5.14 Register Configuration

Register Name	Abbreviation	R/W	Address	Access Size
AP block LSI internal communication interrupt/wakeup function register	CCOMIFAP	R/W	H'E605 8000	32
AP block LSI internal communication interrupt/wakeup source register	CCOMIEAP	R	H'E605 8004	32
AP block LSI internal communication interrupt/wakeup source clear register	CCOMICAP	W	H'E605 8008	32

Table 5.15 Register States in Each Operating Mode

Abbreviation	Reset *	Module Standby
CCOMIFAP	Initialized	Retained
CCOMIEAP	Initialized	Retained
CCOMICAP	Initialized	Retained

Note: * For details, refer to section 1-D Overview of reset.

5.6.2 AP Block LSI Internal Communication Interrupt/Wakeup Function Register (CCOMIFAP)

CCOMIFAP specifies the conditions for interrupt/wakeup requests to the AP-System core, which are caused by specific events in the internal connections of the LSI. This register is in power supply area C5. A wakeup request can be issued even when power is stopped up to power supply area A4R/A4S.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IFM	IFV0	IFR	IFB	IFV1	–	–	–	–	–	–	–	–	–	–	–
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	W	W	W	W	W	W	W	W	W	W	W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	IFA1	IFB1	IFC1	IFA0	IFB0	IFC0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	W	W	W	W	W	W	W	W	W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	IFM	0	R/W	0: Disables an MFI interrupt/wakeup request to the AP block 1: Enables an MFI interrupt/wakeup request to the AP block
30	IFV0	0	R/W	0: Disables a VBUS0_0 interrupt/wakeup request to the AP block 1: Enables an interrupt/wakeup request to the AP block at the rising edge of VBUS0_0
29	IFR	0	R/W	0: Disables an SCIFA3_CTS interrupt/wakeup request to the AP block 1: Enables an interrupt/wakeup request to the AP block at the falling edge of SCIFA3_CTS
28	IFB	0	R/W	0: Disables a BBIF1_RSCK interrupt/wakeup request to the AP block 1: Enables an interrupt/wakeup request to the AP block at the rising edge of BBIF1_RSCK
27	IFV1	0	R/W	0: Disables a VBUS0_1 interrupt/wakeup request to the AP block 1: Enables an interrupt/wakeup request to the AP block at the rising edge of VBUS0_1
26 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	IFA1			Specifies the change in the GPIn signal as an interrupt/wakeup request condition.
4	IFB1			
3	IFC1			
2	IFA0			
1	IFB0			

IFAn	IFBn	IFCn	(n: 1 to 0)
0	0	0	Disables an interrupt/wakeup request

0	IFC0		0	0	1	Enables an interrupt/wakeup request at the falling edge
			0	1	0	Enables an interrupt/wakeup request at the rising edge
			0	1	1	Enables an interrupt/wakeup request at either edge
			1	x	0	Enables an interrupt/wakeup request at a low level
			1	x	1	Enables an interrupt/wakeup request at a high level

[Legend]

x: Don't care

5.6.3 AP Block LSI Internal Communication Interrupt/Wakeup Source Register (CCOMIEAP)

CCOMIEAP is a read-only register that indicates the source of the interrupt/wakeup request issued from CCOMIFAP. The initial value of this register is H'00000000. When level detection is specified and an interrupt is asserted, the corresponding bit among the IE1 to IE0 bits is set to 1.

Bits 31 to 24	IEM	IEV0	IER	IEB	IEV1	0	0	0
Bits 23 to 16	0	0	0	0	0	0	0	0
Bits 15 to 8	0	0	0	0	0	0	0	0
Bits 1 to 0	0	0	0	0	0	0	IE1	IE0

5.6.4 AP Block LSI Internal Communication Interrupt/Wakeup Source Clear Register (CCOMICAP)

CCOMICAP is a write-only register. Writing 1 to a bit clears the corresponding source of the interrupt/wakeup request issued from CCOMIFAP. Before writing to CCOMICAP, be sure to read from CCOMIEAP. The MFI source is retained until the MFI register that issued the request is cleared. When level detection is specified, a write to the IC1 to IC0 bits is ignored.

Bits 31 to 24	0	ICV0	ICR	ICB	ICV1	0	0	0
Bits 23 to 16	0	0	0	0	0	0	0	0
Bits 15 to 8	0	0	0	0	0	0	0	0
Bits 7 to 0	0	0	0	0	0	0	IC1	IC0

5.6.5 Usage Notes When Changing CCOMxxAP

Modify CCOMIFAP, CCOMICAP, and CCOMIEAP using the following procedures in order to guarantee the time until the write operation actually takes effect.

(a) CCOMIFAP

After changing CCOMIFAP, perform a dummy read of CCOMIFAP.

When changing the IFAn, IFBn, or IFCn bit setting, clear the detected source with the procedure below because there is a possibility of detecting a GPIn interrupt.

1. Mask the ACMFI1/2 interrupt using IMR2A[0] of the INTCA.
2. Change the IFAn, IFBn, or IFCn bit setting.
3. Perform dummy read of CCOMIFAP.
4. Write 1 to the relevant bit in CCOMICAP to clear the detected source of GPIn.
5. Perform dummy read of CCOMICAP.
6. Clear masking of the ACMFI1/2 interrupt using IMCR2A[0] of the INTCA.

However, if the IFAn, IFBn, or IFCn bit setting is level detection before and after the change (change from low-level detection to high-level detection or change from high-level detection to low-level detection), this procedure is unnecessary because there is no possibility of detecting a GPIn interrupt.

(b) CCOMICAP

After writing 1 to a bit in CCOMICAP, perform a dummy read of CCOMICAP.

(c) CCOMIEAP

After power-on, a value of 1 may be set due to erroneous detection. Therefore, clear all sources before setting the priority of the ACMFI1/2 interrupt of the INTCA.

5.7 LSI Internal Communication Interrupts and Wakeup Function (Request to SYS from RT)

A specified event in the internal connections of the LSI can be used to send a request to the AP-System core for wakeup from the power cutoff state or an interrupt.

A wakeup request is used to start power supply or generate clocks when the power to the AP-System core or INTCA is stopped or when interrupts cannot be accepted because the clock to the AP-System core or INTCA is stopped. When a wakeup request is used to start power supply, execution branches to the reset vector; otherwise, usual interrupt processing is done.

This request is sent together with the interrupt from the MFI to the AP-System core.

5.7.1 LSI Internal Communication Interrupt/Wakeup Function (Request to SYS) Register Configuration

Table 5.16 shows the LSI internal communication interrupt/wakeup function (request to SYS) register configuration. Table 5.17 shows the register states in each operating mode.

Table 5.16 Register Configuration

Register Name	Abbreviation	R/W	Address	Access Size
SYS domain LSI internal communication interrupt/wakeup function register	CCOMIFR2S	R/W	H'E605 8060	32
SYS domain LSI internal communication interrupt/wakeup source register	CCOMIER2S	R	H'E605 8064	32
SYS domain LSI internal communication interrupt/wakeup source clear register	CCOMICR2S	W	H'E605 8068	32

Table 5.17 Register States in Each Operating Mode

Abbreviation	Reset *	Module Standby
CCOMIFR2S	Initialized	Retained
CCOMIER2S	Initialized	Retained
CCOMICR2S	Initialized	Retained

Note: * For details, refer to section 1-D Overview of reset.

5.7.2 LSI Internal Communication Interrupts and Wakeup Function(CCOMIFR2S)

CCOMIFR2S specifies the conditions for interrupt/wakeup requests to the AP-System core, which are caused by specific events in the internal connections of the LSI. This register is in power supply area C5. A wakeup request can be issued even when power is stopped up to power supply area A4R/A4S.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	IFA7	IFB7	IFC7	-	IFA6	IFB6	IFC6	-	IFA5	IFB5	IFC5	-	IFA4	IFB4	IFC4
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	IFA3	IFB3	IFC3	-	IFA2	IFB2	IFC2	-	IFA1	IFB1	IFC1	-	IFA0	IFB0	IFC0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit		Initial Value	R/W	Description
31	—	0	R	
30	IFA7	000	R/W	
29	IFB7	000	R/W	Specifies the change in the GPOR2Sn pins as an interrupt/wakeup request condition.
28	IFC7	000	R/W	
27	—	0	R	
26	IFA6	000	R/W	
25	IFA6	000	R/W	
24	IFA6	000	R/W	
23	—	0	R	
22	IFA5	000	R/W	
21	IFA5	000	R/W	
20	IFA5	000	R/W	
19	—	0	R	
18	IFA4	000	R/W	
17	IFA4	000	R/W	
16	IFA4	000	R/W	
15	—	0	R	
14	IFA3	000	R/W	
13	IFA3	000	R/W	
12	IFA3	000	R/W	
11	—	0	R	
10	IFA2	000	R/W	
9	IFA2	000	R/W	
8	IFA2	000	R/W	
7	—	0	R	
6	IFA1	000	R/W	
5	IFA1	000	R/W	
4	IFA1	000	R/W	
3	—	0	R	
2	IFA0	000	R/W	
1	IFA0	000	R/W	
0	IFA0	000	R/W	

IFAn	IFBn	IFCn	(n: 7 to 0)
0	0	0	Disables an interrupt/wakeup request
0	0	1	Enables an interrupt/wakeup request at the falling edge
0	1	0	Enables an interrupt/wakeup request at the rising edge
0	1	1	Enables an interrupt/wakeup request at both edge
1	x	0	Enables an interrupt/wakeup request at a low level
1	x	1	Enables an interrupt/wakeup request at a high level

[Legend]

x: Don't care

5.7.3 AP Block LSI Internal Communication Interrupt/Wakeup Source Register (CCOMIER2S)

CCOMIER2S is a read-only register that indicates the source of the interrupt/wakeup request issued from CCOMIFR2S. The initial value of this register is H'00000000. When level detection is specified and an interrupt is asserted, the corresponding bit among the IE7 to IE0 bits is set to 1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	IE7	IE6	IE5	IE4	IE3	IE2	IE1	IE0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

5.7.4 AP Block LSI Internal Communication Interrupt/Wakeup Source Clear Register (CCOMICR2S)

CCOMICR2S is a write-only register. Writing 1 to a bit clears the corresponding source of the interrupt/wakeup request issued from CCOMIFR2S. Before writing to CCOMICR2S, be sure to read from CCOMIER2S. The MFI source is retained until the MFI register that issued the request is cleared. When level detection is specified, a write to the IC7 to IC0 bits is ignored.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	IC7	IC6	IC5	IC4	IC3	IC2	IC1	IC0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

5.7.5 Usage Notes When Changing CCOMxxR2S

Modify CCOMIFR2S, CCOMICR2S, and CCOMIER2S using the following procedures in order to guarantee the time until the write operation actually takes effect.

(a) CCOMIFR2S

After changing CCOMIFR2S, perform a dummy read of CCOMIFR2S.

When changing the IFAn, IFBn, or IFCn bit setting, clear the detected source with the procedure below because there is a possibility of detecting a GPIn interrupt.

1. Mask the CPORTR2S interrupt using IMR7A3[6] of the INTCA.
2. Change the IFAn, IFBn, or IFCn bit setting.
3. Perform dummy read of CCOMIFR2S.
4. Write 1 to the relevant bit in CCOMICR2S to clear the detected source of GPIn.
5. Perform dummy read of CCOMICR2S.
6. Clear masking of the CPORTR2S interrupt using IMCR7A3[6] of the INTCA.

However, if the IFAn, IFBn, or IFCn bit setting is level detection before and after the change (change from low-level detection to high-level detection or change from high-level detection to low-level detection), this procedure is unnecessary because there is no possibility of detecting a GPIn interrupt.

(b) CCOMICR2S

After writing 1 to a bit in CCOMICAP, perform a dummy read of CCOMICR2S.

(c) CCOMIER2S

After power-on, a value of 1 may be set due to erroneous detection. Therefore, clear all sources before setting the priority of the CPORTR2S interrupt of the INTCA.

5.8 LSI Internal Communication Interrupts and Wakeup Function (Request to RT from SYS)

A specified event in the internal connections of the LSI can be used to send a request to the AP-Realtime core for wakeup from the power cutoff state or an interrupt.

A wakeup request is used to start power supply or generate clocks when the power to the AP-Realtime core or INTCS is stopped or when interrupts cannot be accepted because the clock to the AP- Realtime core or INTCS is stopped. When a wakeup request is used to start power supply, execution branches to the reset vector; otherwise, usual interrupt processing is done.

This request is sent together with the interrupt from the MFI to the AP- Realtime core.

5.8.1 LSI Internal Communication Interrupt/Wakeup Function (Request to RT) Register Configuration

Table 5.18 shows the LSI internal communication interrupt/wakeup function (request to RT) register configuration. Table 5.19 shows the register states in each operating mode.

Table 5.18 Register Configuration

Register Name	Abbreviation	R/W	Address	Access Size
RT domain LSI internal communication interrupt/wakeup function register	CCOMIFS2R	R/W	H'E605 8070	32
RT domain LSI internal communication interrupt/wakeup source register	CCOMIES2R	R	H'E605 8074	32
RT domain LSI internal communication interrupt/wakeup source clear register	CCOMICS2R	W	H'E605 8078	32

Table 5.19 Register States in Each Operating Mode

Abbreviation	Power-On Reset	Software Standby (A4R/A4S Area Power Cutoff)	Module Standby	Sleep
CCOMIFS2R	Initialized	Retained	Retained	Retained
CCOMIES2R	Initialized	Retained	Retained	Retained
CCOMICS2R	Initialized	Retained	Retained	Retained

5.8.2 LSI Internal Communication Interrupts and Wakeup Function(CCOMIFS2R)

CCOMIFS2R specifies the conditions for interrupt/wakeup requests to the AP-Realtime core, which are caused by specific events in the internal connections of the LSI. This register is in power supply area C5. A wakeup request can be issued even when power is stopped up to power supply area A4R/A4S.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	IFA7	IFB7	IFC7	-	IFA6	IFB6	IFC6	-	IFA5	IFB5	IFC5	-	IFA4	IFB4	IFC4
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	IFA3	IFB3	IFC3	-	IFA2	IFB2	IFC2	-	IFA1	IFB1	IFC1	-	IFA0	IFB0	IFC0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit		Initial Value	R/W	Description
31	—	0	R	
30	IFA7	000	R/W	
29	IFB7	000	R/W	Specifies the change in the GPOS2Rn pins as an interrupt/wakeup request condition.
28	IFC7	000	R/W	
27	—	0	R	
26	IFA6	000	R/W	
25	IFA6	000	R/W	
24	IFA6	000	R/W	
23	—	0	R	
22	IFA5	000	R/W	
21	IFA5	000	R/W	
20	IFA5	000	R/W	
19	—	0	R	
18	IFA4	000	R/W	
17	IFA4	000	R/W	
16	IFA4	000	R/W	
15	—	0	R	
14	IFA3	000	R/W	
13	IFA3	000	R/W	
12	IFA3	000	R/W	
11	—	0	R	
10	IFA2	000	R/W	
9	IFA2	000	R/W	
8	IFA2	000	R/W	
7	—	0	R	
6	IFA1	000	R/W	
5	IFA1	000	R/W	
4	IFA1	000	R/W	
3	—	0	R	
2	IFA0	000	R/W	
1	IFA0	000	R/W	
0	IFA0	000	R/W	

IFAn	IFBn	IFCn	(n: 7 to 0)
0	0	0	Disables an interrupt/wakeup request
0	0	1	Enables an interrupt/wakeup request at the falling edge
0	1	0	Enables an interrupt/wakeup request at the rising edge
0	1	1	Enables an interrupt/wakeup request at both edge
1	x	0	Enables an interrupt/wakeup request at a low level
1	x	1	Enables an interrupt/wakeup request at a high level

[Legend]

x: Don't care

5.8.3 AP Block LSI Internal Communication Interrupt/Wakeup Source Register (CCOMIES2R)

CCOMIES2R is a read-only register that indicates the source of the interrupt/wakeup request issued from CCOMIFS2R. The initial value of this register is H'00000000. When level detection is specified and an interrupt is asserted, the corresponding bit among the IE7 to IE0 bits is set to 1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	IE7	IE6	IE5	IE4	IE3	IE2	IE1	IE0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

5.8.4 AP Block LSI Internal Communication Interrupt/Wakeup Source Clear Register (CCOMICS2R)

CCOMICS2R is a write-only register. Writing 1 to a bit clears the corresponding source of the interrupt/wakeup request issued from CCOMIFS2R. Before writing to CCOMICS2R, be sure to read from CCOMIES2R. The MFI source is retained until the MFI register that issued the request is cleared. When level detection is specified, a write to the IC7 to IC0 bits is ignored.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	IC7	IC6	IC5	IC4	IC3	IC2	IC1	IC0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

5.8.5 Usage Notes When Changing CCOMxxS2R

Modify CCOMIFS2R, CCOMICS2R, and CCOMIES2R using the following procedures in order to guarantee the time until the write operation actually takes effect.

(a) CCOMIFS2R

After changing CCOMIFS2R, perform a dummy read of CCOMIFS2R.

When changing the IFAn, IFBn, or IFCn bit setting, clear the detected source with the procedure below because there is a possibility of detecting a GPIn interrupt.

1. Mask the CPORTS2R interrupt using IMR7S3[6] of the INTCS.
2. Change the IFAn, IFBn, or IFCn bit setting.
3. Perform dummy read of CCOMIFS2R.
4. Write 1 to the relevant bit in CCOMICS2R to clear the detected source of GPIn.
5. Perform dummy read of CCOMICS2R.
6. Clear masking of the CPORTS2R interrupt using IMCR7S3[6] of the INTCS.

However, if the IFAn, IFBn, or IFCn bit setting is level detection before and after the change (change from low-level detection to high-level detection or change from high-level detection to low-level detection), this procedure is unnecessary because there is no possibility of detecting a GPIn interrupt.

(b) CCOMICS2R

After writing 1 to a bit in CCOMICS2R, perform a dummy read of CCOMICS2R.

(c) CCOMIES2R

After power-on, a value of 1 may be set due to erroneous detection. Therefore, clear all sources before setting the priority of the CPORTS2R interrupt of the INTCS.

Section 6 Bus State Controller (BSC)

The bus state controller (BSC) outputs control signals for various types of memory and external devices that are connected to the external address space. The BSC functions enable this LSI to connect directly with SRAM and other memory storage devices, and external devices.

6.1 Features

The BSC has the following features:

- External address space
  128 Mbytes for each of CS0 and CS2, 64 Mbytes for CS4, and 32 Mbytes for each of CS5A, CS5B, and CS6A (total of 416 Mbytes which is divided into six partial spaces).
  Address spaces CS0 and CS2 can be merged into a 256-Mbyte address space that can be accessed. Address spaces CS5A and CS5B can be merged into 64-Mbyte address spaces that can be accessed.
  Can specify the normal space interface, SRAM interface with byte selection, or burst ROM for each address space
  Can select the data bus width (8 or 16 bits) for each address space
  Controls insertion of wait cycle for each address space
  Controls insertion of wait cycle for each read access and write access
  Can set independent idle cycles in the continuous access for five cases: read-write (in same space/different spaces), read-read (in same space/different spaces), the first cycle is a write access
- Normal space interface
  Supports the interface that can be connected directly to SRAM
  Supports the AD-MUX interface (CS0, CS2, and CS4)
- Burst ROM interface
  High-speed access to the memory having a page-mode function
  High-speed access to the memory having a clock-synchronous burst mode function
  Supports a clock-synchronous burst ROM interface
  Supports the AD-MUX interface (CS0, CS2, and CS4)

- SRAM interface with byte selection
  Supports the interface that can be connected directly to SRAM with byte selection
  Supports Write Enable(WEn_N) control writing
  Supports page mode
  Supports the AD-MUX interface (CS0, CS2, CS4, CS5A, CS5B, and CS6A)
- CKO output stop function
- The BSC operating frequency ZBϕ can be set to 99.6 (= 199.3/2) MHz, 66.4 (= 199.3/3) MHz, 49.8 (= 199.3/4) MHz by changing the common frequency control register (CMFRQCR) in the CPGA.
- Memory protection function
  Can set permissions for reading and writing from the AP module, in 64-Mbit increments, of a 2-Gbit area starting at the initial address of area 0.

A block diagram of the BSC is shown in figure 6.1.

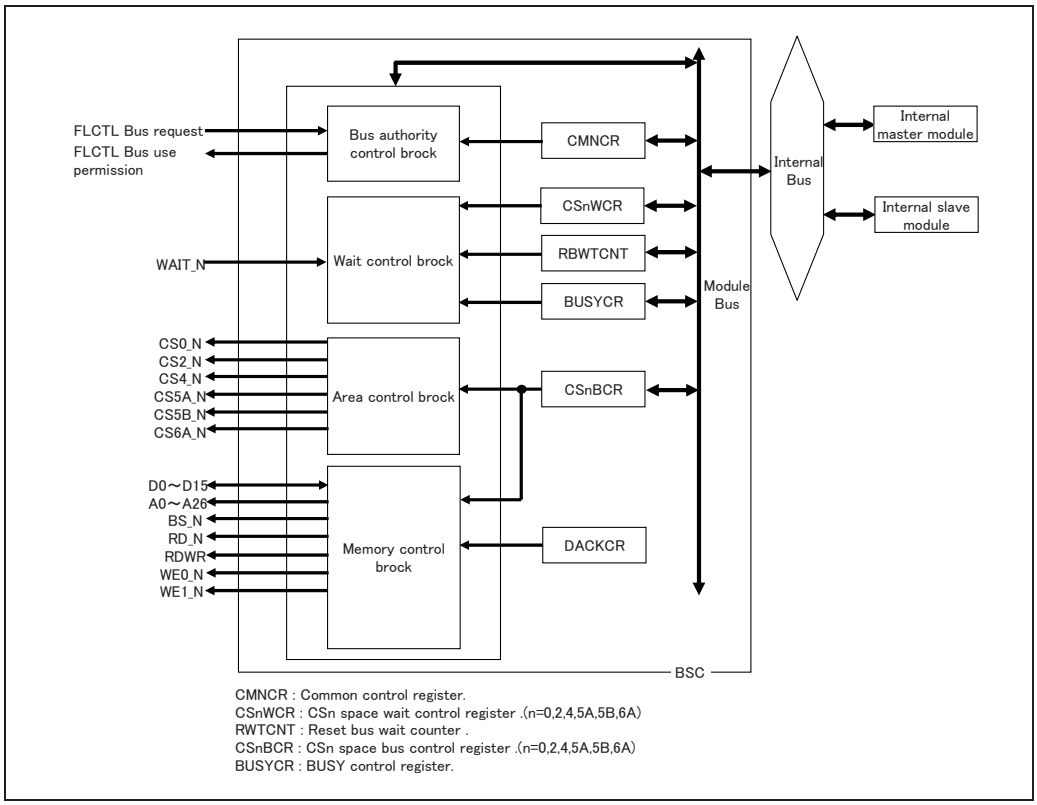


Figure 6.1 Block Diagram of BSC

6.2 Input/Output Pins

Table 6.1 Pin Configuration

Name	Function	I/O	Description
CKO	Bus clock	Output	Bus clock output
A26 to A0	Address bus	Output	Address output
D15 to D0	Data bus	I/O	16-bit bidirectional bus
BS_N	Bus start	Output	Bus start signal This signal is asserted at the start of the bus cycle. This signal is connected to the address valid pin of the memory having the Sync Burst function. In this LSI, this pin is multiplexed with the A0 pin. For burst ROM interface, the wait cycles can be changed.
CS0_N CS2_N CS4_N CS5A_N CS5B_N CS6A_N	Chip select CS0, CS 2, CS 4, CS 5A, CS 5B, CS 6A	Output	Chip select signal for external memory or device. CS5A_N and CS6A_N are active only when the MAP bit in CMNCR is set to 0 and the address map 1 or 3 is selected. When the MAP bit in CMNCR is set to 1 and the address map 2 or 4 is selected, CA5B_N become the chip select signals for the area 5 .CS2_N becomes active only when the EXTEND bit in CMNCR is set to 0 and address map 1 or 2 is selected. When the EXTEND bit in CMNCR is set to 1 and address map 3 or 4 is selected, CS2_N always becomes inactive.
RD_N	Read	Output	Indicates that data is read from an external device.

Name	Function	I/O	Description
RDWR	Read/write	Output	Read/write signal pin
WE1_N	Write to upper byte	Output	Indicates that bits 15 to 8 of external memory or device data are being written to.
WE0_N	Write to lower byte	Output	Indicates that bits 7 to 0 of external memory or device data are being written to.
WAIT_N	External wait input	Input	Inserts a wait cycle between bus cycles for accessing the external space.
BSCMD	CS0 memory type select	Input	Sets the initial value of the CS0 memory type. 0: Normal memory The initial value of pins A26 to A13 is an address. 1: AD-MUX The initial value of pin A0 is BS_N.

6.3 Area Overview

6.3.1 Area Division

In the architecture, this LSI has 32-bit address spaces. In the AP-Realtime core, the address area is classified into P0 to P4 by the upper three bits of the 32-bit address, and each area represents the cache access method. For details, see section 3, AP-Realtime Core. The remaining 29 bits are used for division of the space into six areas (address map 1) or four areas (address map 2) according to the setting of the MAP bit in CMNCR. The BSC performs control for this 29-bit space.

As listed in tables 6.2 to 6.5, this LSI can connect six to four physical areas to each type of memory, and it outputs chip select signals (CS0_N, CS2_N, CS4_N, CS5A_N, CS5B_N, and CS6A_N) for each of them. CS0_N is asserted during area CS 0 access. During area CS 5A access, CS5A_N is asserted when address map 1 is selected, and CS5B_N is asserted when address map 2 is selected.

6.3.2 Shadow Area

Areas CS 0, CS 2, CS 4, CS 5A, CS 5B, and CS 6A are decoded by physical addresses A28 to A25, which correspond to areas B'000 to B'110. Addresses A31 to A29 are ignored. This means that the range of area 0 addresses, for example, is H'0000 0000 to H'07FF FFFF, and its corresponding shadow space is the address space obtained by adding to it H'2000 0000 × n (n = 1 to 6).

6.3.3 Address Map

The external address space has a capacity of 416 Mbytes and is divided into six partial spaces, (address map 1) four partial spaces (address map 2), five partial spaces (address map 3), or three partial spaces (address map 4). The type of memory to be connected and the data bus width are specified for each partial space. The address map for the external address space is listed in tables 6.2 to 6.5.

Table 6.2 Address Map 1 (CMNCR.MAP = 0, CMNCR.EXTEND = 0)

Address	Area	Memory to be Connected	Capacity
H'0000 0000 to H'07FF FFFF	Area 0	Normal memory SRAM with byte selection Burst ROM	128 Mbytes
H'0800 0000 to H'0FFF FFFF	Area 2	Normal memory SRAM with byte selection Burst ROM	128 Mbytes
H'1000 0000 to H'13FF FFFF	Area 4	Normal memory SRAM with byte selection Burst ROM	64 Mbytes
H'1400 0000 to H'15FF FFFF	Area 5A	Normal memory SRAM with byte selection	32 Mbytes
H'1600 0000 to H'17FF FFFF	Area 5B	Normal memory SRAM with byte selection	32 Mbytes
H'1800 0000 to H'19FF FFFF	Area 6A	Normal memory SRAM with byte selection	32 Mbytes
H'1A00 0000 to H'1FFF FFFF	—	Reserved space*	96 Mbytes

Note: * Do not access reserved space. If reserved space is accessed, the operation of this LSI is not guaranteed.

Table 6.3 Address Map 2 (CMNCR.MAP = 1, CMNCR.EXTEND = 0)

Address	Area	Memory to be Connected	Capacity
H'0000 0000 to H'07FF FFFF	Area 0	Normal memory SRAM with byte selection Burst ROM	128 Mbytes
H'0800 0000 to H'0FFF FFFF	Area 2	Normal memory SRAM with byte selection Burst ROM	128 Mbytes
H'1000 0000 to H'13FF FFFF	Area 4	Normal memory SRAM with byte selection Burst ROM (asynchronous)	64 Mbytes
H'1400 0000 to H'17FF FFFF	Area 5*1	Normal memory SRAM with byte selection	64 Mbytes
H'1800 0000 to H'1FFF FFFF	—	Reserved space*2	128 Mbytes

Note: 1. For area 5, CS5BBCR and CS5BWCR are valid.
2. Do not access reserved space. If reserved space is accessed, the operation of this LSI is not guaranteed.

Table 6.4 Address Map 3 (CMNCR.MAP= 0, CMNCR.EXTEND = 1)

Address	Area	Memory to be Connected	Capacity
H'0000 0000 to H'0FFF FFFF	Area 0	Normal memory SRAM with byte selection Burst ROM	256 Mbytes
H'1000 0000 to H'13FF FFFF	Area 4	Normal memory SRAM with byte selection Burst ROM	64 Mbytes
H'1400 0000 to H'15FF FFFF	Area 5A	Normal memory SRAM with byte selection	32 Mbytes
H'1600 0000 to H'17FF FFFF	Area 5B	Normal memory SRAM with byte selection	32 Mbytes
H'1800 0000 to H'19FF FFFF	Area 6A	Normal memory SRAM with byte selection	32 Mbytes
H'1A00 0000 to H'1FFF FFFF	—	Reserved space*	96 Mbytes

Note: * Do not access reserved space. If reserved space is accessed, the operation of this LSI is not guaranteed.

Table 6.5 Address Map 4 (CMNCR.MAP = 1, CMNCR.EXTEND = 1)

Address	Area	Memory to be Connected	Capacity
H'0000 0000 to H'0FFF FFFF	Area 0	Normal memory SRAM with byte selection Burst ROM	256 Mbytes
H'1000 0000 to H'13FF FFFF	Area 4	Normal memory SRAM with byte selection Burst ROM (asynchronous)	64 Mbytes
H'1400 0000 to H'17FF FFFF	Area 5*1	Normal memory SRAM with byte selection	64 Mbytes
H'1800 0000 to H'1FFF FFFF	—	Reserved space*2	128 Mbytes

Note: 1. For area 5, CS5BBCR and CS5BWCR are valid.
2. Do not access reserved space. If reserved space is accessed, the operation of this LSI is not guaranteed.

6.3.4 Memory Bus Width

The memory bus width in this LSI can be set as 8 bits or 16 bits for each area by setting the BSZ bits in CSnBCR (n = 2, 4, 5A, 5B, 6A).

Note that the memory bus width in area 0 is fixed to 16 bits.

6.3.5 Data Alignment

This LSI supports the little endian method for data alignment.

6.4 Register Descriptions

Table 6.6 shows the BSC register configuration. Table 6.7 shows the register states in each operating mode.

Do not access spaces other than CS0 until the completion of the memory interface setting.

Table 6.6 Register Configuration

Register	Abbreviation	R/W	Address	Access Size
Common control register	CMNCR	R/W	H'FEC10000	32
CS0 space bus control register	CS0BCR	R/W	H'FEC10004	32
CS2 space bus control register	CS2BCR	R/W	H'FEC10008	32
CS4 space bus control register	CS4BCR	R/W	H'FEC10010	32
CS5A space bus control register	CS5ABCR	R/W	H'FEC10014	32
CS6A space bus control register	CS6ABCR	R/W	H'FEC1001C	32
CS0 space wait control register	CS0WCR	R/W	H'FEC10024	32
CS2 space wait control register	CS2WCR	R/W	H'FEC10028	32
CS4 space wait control register	CS4WCR	R/W	H'FEC10030	32
CS5A space wait control register	CS5AWCR	R/W	H'FEC10034	32
CS6A space wait control register	CS6AWCR	R/W	H'FEC1003C	32
Reset bus wait counter	RBWTCNT	—	H'FEC10054	32
Busy control register	BUSYCR	R/W	H'FEC10058	32
Burst ROM timing control register	BROMTIMCR	R/W	H'FEC1 0070	32
Memory protection area settings register 00	BPTCR00	R/W	H'FEC1 0090	32
Memory protection area settings register 01	BPTCR01	R/W	H'FEC1 0094	32
Memory protection area settings register 02	BPTCR02	R/W	H'FEC1 0098	32
Memory protection area settings register 03	BPTCR03	R/W	H'FEC1 009C	32
Memory protection area settings register 04	BPTCR04	R/W	H'FEC1 00A0	32
Memory protection area settings register 05	BPTCR05	R/W	H'FEC1 00A4	32
Memory protection area settings register 06	BPTCR06	R/W	H'FEC1 00A8	32
Memory protection area settings register 07	BPTCR07	R/W	H'FEC1 00AC	32
Memory protection area settings register 08	BPTCR08	R/W	H'FEC1 00B0	32
Memory protection area settings register 09	BPTCR09	R/W	H'FEC1 00B4	32
Memory protection area settings register 10	BPTCR10	R/W	H'FEC1 00B8	32
Memory protection area settings register 11	BPTCR11	R/W	H'FEC1 00BC	32

Register	Abbreviation	R/W	Address	Access Size
Memory protection area settings register 12	BPTCR12	R/W	H'FEC1 00C0	32
Memory protection area settings register 13	BPTCR13	R/W	H'FEC1 00C4	32
Memory protection area settings register 14	BPTCR14	R/W	H'FEC1 00C8	32
Memory protection area settings register 15	BPTCR15	R/W	H'FEC1 00CC	32
Memory protection area settings register 16	BPTCR16	R/W	H'FEC1 00D0	32
Memory protection area settings register 17	BPTCR17	R/W	H'FEC1 00D4	32
Memory protection area settings register 18	BPTCR18	R/W	H'FEC1 00D8	32
Memory protection area settings register 19	BPTCR19	R/W	H'FEC1 00DC	32
Memory protection area settings register 20	BPTCR20	R/W	H'FEC1 00E0	32
Memory protection area settings register 21	BPTCR21	R/W	H'FEC1 00E4	32
Memory protection area settings register 22	BPTCR22	R/W	H'FEC1 00E8	32
Memory protection area settings register 23	BPTCR23	R/W	H'FEC1 00EC	32
Memory protection area settings register 24	BPTCR24	R/W	H'FEC1 00F0	32
Memory protection area settings register 25	BPTCR25	R/W	H'FEC1 00F4	32
Memory protection area settings register 26	BPTCR26	R/W	H'FEC1 00F8	32
Memory protection area settings register 27	BPTCR27	R/W	H'FEC1 00FC	32
Memory protection area settings register 28	BPTCR28	R/W	H'FEC1 0100	32
Memory protection area settings register 29	BPTCR29	R/W	H'FEC1 0104	32
Memory protection area settings register 30	BPTCR30	R/W	H'FEC1 0108	32
Memory protection area settings register 31	BPTCR31	R/W	H'FEC1 010C	32
BS_N assert period control register	BSWCR	R/W	H'FEC10110	32
CS0 space wait control register 2	CS0WCR2	R/W	H'FEC10224	32
CS2 space wait control register 2	CS2WCR2	R/W	H'FEC10228	32
CS4 space wait control register 2	CS4WCR2	R/W	H'FEC10230	32

Table 6.7 Register States in Each Operating Mode

Register Abbreviation	Power-On Reset	Software Standby	Module Standby	Sleep	C4 Area Power Off
CMNCR	Initialized	Retained	—	Retained	Retained
CS0BCR	Initialized	Retained	—	Retained	Retained
CS2BCR	Initialized	Retained	—	Retained	Initialized
CS4BCR	Initialized	Retained	—	Retained	Initialized
CS5ABCR	Initialized	Retained	—	Retained	Initialized
CS5BBCR	Initialized	Retained	—	Retained	Initialized
CS6ABCR	Initialized	Retained	—	Retained	Initialized
CS0WCR	Initialized	Retained	—	Retained	Retained
CS2WCR	Initialized	Retained	—	Retained	Initialized
CS4WCR	Initialized	Retained	—	Retained	Initialized
CS5AWCR	Initialized	Retained	—	Retained	Initialized
CS5BWCR	Initialized	Retained	—	Retained	Initialized
CS6AWCR	Initialized	Retained	—	Retained	Initialized
RBWTCNT	Initialized	Retained	—	Retained	Initialized
BUSYCR	Initialized	Retained	—	Retained	Initialized
BROMTIMCR	Initialized	Retained	—	Retained	Retained
BPTCR00 to 31	Initialized	Retained	—	Retained	Retained
BSWCR	Initialized	Retained	—	Retained	Retained
CS0WCR2	Initialized	Retained	—	Retained	Retained
CS2WCR2	Initialized	Retained	—	Retained	Retained
CS4WCR2	Initialized	Retained	—	Retained	Retained

6.4.1 Common Control Register (CMNCR)

CMNCR is a 32-bit register that controls the common items for each area.

CMNCR is initialized by a power-on reset. However, CMNCR is not initialized but retains the previous value in standby mode. Do not access external memory other than area 0 until the CMNCR initialization is completed.

Bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	CKOD STP	CKO STP	BROM MD1	BROM MD0	-	-	-	-	-
Initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	EXT END	-	MAP	-	-	-	-	-	-	-	-	-	A2H	-	-
Initial value :	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1
R/W :	R	R/W	R	R/W	R	R	R	R	R	R	R	R	R	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	CKODSTP	0	R/W	Clock Operation Specification in Non-Access Cycles When the BROMMD0 bit is set to 1, this bit can specify the operation in non-access cycles. 0: CKO operates in non-access cycles 1: CKO is halted in non-access cycles
23	CKOSTP	0	R/W	Clock Stop Specification 0: CKO operates 1: CKO is halted
22	BROMMD1	0	R/W	Specifies the input data when PH1RD of CSnBCR (n 0, 2, 4, 5A, 5B, 6A) is set. When this bit is set to 1, the value of the D pin is sampled on the rising edge of CKO that is output. 0: Selects direct bus from the D pin 1: Selects fetch from the feedback CKO

Bit	Bit Name	Initial Value	R/W	Description
21	BROMMD0	0	R/W	Clock Output Specification Specifies CKO output. Setting 1 to this bit assures the hold time for CKO of the control signal that is output. 0: Selects the same phase output as the operation clock ZBCK 1: Selects the inverse output of the operation clock ZBCK When inverse output is selected, CKO is halted in non-access cycles.
20 to 15	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
14	EXTEND	0	R/W	CS0/CS2 Area Size Specification 0: CS0/CS2 area is a 128-Mbyte area 1: The CS0 area is a 256-Mbyte area (The CS2 and CS0 areas are merged.)
13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	MAP	0	R/W	Space Specification Selects the address map for the external address space. The address maps to be selected are shown in tables 6.2 and 6.3. 0: Selects address map 1 or 3 1: Selects address map 2 or 4
11 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
4, 3	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.
2	A2H	0	R/W	A2 Level Specification for Accesses in Fixed Addressing Mode A2 is a normal output when the DMAC or VIO does not access in fixed addressing mode. 0: Outputs a low level signal from A2 pin 1: Outputs a high level signal from A2 pin
1,0	—	1	R	Reserved These bits are always read as 1. The write value should always be 1.

6.4.2 CSn Space Bus Control Register (CSnBCR) (n = 0, 2, 4, 5A, 5B, 6A)

CSnBCR is a 32-bit readable/writable register that specifies the function of each area, the number of idle cycles between bus cycles, and the bus width.

CSnBCR is initialized by a power-on reset. However, CSnBCR is not initialized but retains the previous value in standby mode. Do not access external memory other than area 0 until the CSnBCR initialization is completed.

Bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	IWW[1:0]		-	IWRWD[1:0]		-	IWRWS[1:0]		-	IWRRD[1:0]		-	IWRRS[1:0]	
Initial value :	0	0	1	1	0	1	1	0	1	1	0	1	1	0	1	1
R/W :	R	R	R/W	R/W	R	R/W	R/W	R	R/W	R/W	R	R/W	R/W	R	R/W	R/W

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	TYPE[2:0]			-	BSZ[1:0]		-	-	-	-	CKO STP	-	BUSY EN	PH1R D	-
Initial value :	0	0	0	0	0	1	0	0	0	0	0	0	0	0/1	0	0
R/W :	R	R/W	R/W	R/W	R	R/W	R/W	R	R	R	R	R/W	R	R/W	R/W	R

Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29, 28	IWW[1:0]	11	R/W	Specification for Idle Cycles between Write-Read/Write-Write Cycles Specify the number of idle cycles to be inserted after access to memory that is connected to the space is completed. The target cycles are write-read cycles and write-write cycles. 00: No idle cycle inserted 01: 1 idle cycle inserted 10: 2 idle cycles inserted 11: 4 idle cycles inserted Note: In actual operation, an idle cycle or cycles may be inserted by factors other than specification of these bits.

Bit	Bit Name	Initial Value	R/W	Description
27	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
26, 25	IWRWD[1:0]	11	R/W	Specification for Idle Cycles between Read-Write Cycles in Different Spaces Specify the number of idle cycles to be inserted after access to memory that is connected to the space is completed. The target cycles are read-write cycles in which continuous accesses are switched between different spaces. 00: 1 idle cycle inserted 01: 1 idle cycle inserted 10: 2 idle cycles inserted 11: 4 idle cycles inserted Note: In actual operation, an idle cycle or cycles may be inserted by factors other than specification of these bits.
24	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
23, 22	IWRWS[1:0]	11	R/W	Specification for Idle Cycles between Read-Write Cycles in the Same Space Specify the number of idle cycles to be inserted after access to memory that is connected to the space is completed. The target cycles are read-write cycles in which continuous accesses are performed for the same space. 00: 1 idle cycle inserted 01: 1 idle cycle inserted 10: 2 idle cycles inserted 11: 4 idle cycles inserted Note: In actual operation, an idle cycle or cycles may be inserted by factors other than specification of these bits.

Bit	Bit Name	Initial Value	R/W	Description
21	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
20, 19	IWRRD[1:0]	11	R/W	Specification for Idle Cycles between Read-Read Cycles in Different Spaces Specify the number of idle cycles to be inserted after access to memory that is connected to the space is completed. The target cycles are read-read cycles in which continuous accesses are switched between different spaces. 00: No idle cycle inserted 01: 1 idle cycle inserted 10: 2 idle cycles inserted 11: 4 idle cycles inserted Note: In actual operation, an idle cycle or cycles may be inserted by factors other than specification of these bits.
18	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
17, 16	IWRRS[1:0]	11	R/W	Specification for Idle Cycles between Read-Read Cycles in the Same Space Specify the number of idle cycles to be inserted after access to memory that is connected to the space is completed. The target cycles are read-read cycles in which continuous accesses are performed for the same space. 00: No idle cycle inserted 01: 1 idle cycle inserted 10: 2 idle cycles inserted 11: 4 idle cycles inserted Note: In actual operation, an idle cycle or cycles may be inserted by factors other than specification of these bits.

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14 to 12	TYPE[2:0]	000	R/W	Memory Type Specification Specify the type of memory connected to the space. 000: Normal space 001: Burst ROM 011: SRAM with byte selection Other than above: Setting prohibited Note: Burst ROM can be set in areas 0, 2, and 4 only.
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10, 9	BSZ[1:0]	10	R/W	Data Bus Size Specification Specify the data bus sizes of spaces. Either 8-bit size or 16-bit size can be specified for CS2, CS4, CS5A, CS5B, CS6A. CS0 can be specified to 16-bit size only. 00: Setting prohibited 01: 8-bit size 10: 16-bit size 11: 32-bit size
8 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	CKOSTP	0	R/W	CKO stop enable bit 0: When access a pertinent area, CKO is output. 1: When access a pertinent area, CKO is not output.
3		0	R	Reserved These bits are always read as 0. The write value should always be 0.

2	BUSYEN	0/1	R/W	Busy Wait Enable The initial value of CS0 is 1 and that of other signals are 0. 0: Access inhibition that is specified by the BUSY control register is disabled. 1: Access inhibition that is specified by the BUSY control register is enabled.
1	PH1RD	0	R/W	Data Sampling Timing Specification 0: Data is sampled on the falling edge of the operation clock ZBϕ of the BSC. The RD_N output timing is the falling edge of ZBϕ. 1: Data is sampled on the rising edge of the operation clock ZBϕ of the BSC. The RD_N output timing is the rising edge of ZBϕ.
0	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

6.4.3 CSn Space Wait Control Register (CSnWCR) (n = 0, 2, 4, 5A, 5B, 6A)

CSnWCR specifies various wait cycles for memory accesses. The bit configuration of this register varies as shown below according to the memory type specified by the TYPE bits in the CSn space bus control register (CSnBCR). Specify CSnWCR before accessing the target area. Specify CSnBCR first, then specify CSnWCR.

CSnWCR is initialized to H'0000 0540 by a power-on reset. However, CSnWCR is not initialized but retains the previous value in standby mode.

(1) Normal Space, SRAM with Byte Selection

- CS0WCR, CS4WCR, CS5AWCR, CS5BWCR, CS6AWCR

Bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-		WSHW EN	WSW[1:0]		WHW[1:0]		-	-	-	BAS	-	WW[2:0]		
Initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R	R/W	R/W	R/W

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ADRSFIX	-	-	SW[2:0]		WR[3:0]				WM	-	-	ADMUX	-	HW[1:0]	
Initial value :	0	0	0	0/1	0/1	1	0	1	0	1	0	0	0/1	0	0	0
R/W :	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28	WSHWEN	0	R/W	0: Access is made according to SW[1:0] and HW[1:0] during the write cycle. 1: Access is made according to WSW[1:0] and WHW[1:0] during the write cycle.
27, 26	WSW[1:0]	00	R/W	Number of Delay Cycles from Address, CSn_N Assertion to RD_N, WEn_N Assertion Specify the number of delay cycles from address and CSn_N assertion to RD_N and WEn_N assertion during write cycles. When the WSHWEN bit is set to 1, the setting for this bit is enabled. 00: 0.5 cycle 01: 1.5 cycles 10: 2.5 cycles 11: 3.5 cycles
25, 24	WHW[1:0]	00	R/W	Number of Delay Cycles from RD_N, WEn_N Negation to Address, CSn_N Negation Specify the number of delay cycles from RD_N and WEn_N negation to address and CSn_N negation during write cycles. When the WSHWEN bit is set to 1, the setting for this bit is enabled. 00: 0.5 cycle 01: 1.5 cycles 10: 2.5 cycles 11: 3.5 cycles

Bit	Bit Name	Initial Value	R/W	Description
23 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	BAS	0	R/W	Byte Access Selection when SRAM with Byte Selection is Used Specifies the WEn_N and RDWR signal timing when SRAM interface with byte selection is used. 0: Asserts the WEn _N signal at the read/write timing and asserts the RDWR signal during the write access cycle 1: Asserts the WEn_N signal during the read/write access cycle and asserts the RDWR signal at the write timing
19	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
18 to 16	WW[2:0]	000	R/W	Number of Wait Cycles in Write Access Specify the number of cycles necessary for write access. 000: The same cycles as WR[3:0] settings (read access wait) 001: 0 cycle 010: 1 cycle 011: 2 cycles 100: 3 cycles 101: 4 cycles 110: 5 cycles 111: 6 cycles

Bit	Bit Name	Initial Value	R/W	Description
15	ADRSFIX	0	R/W	Address Updating Inhibited (only valid for CS6A) 0: Outputs address normally 1: Inhibits address updating of the second and subsequent burst access.
14, 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12, 11	SW[1:0]	00/11*1	R/W	Number of Delay Cycles from Address, CSn_N Assertion to RD_N, WEn_N Assertion Specify the number of delay cycles from address and CSn_N assertion to RD_N and WEn_N assertion. WEn_N and RD_N in case with CSnBCR.PH1RD=0 00: 0.5 cycle 01: 1.5 cycles 10: 2.5 cycles 11: 3.5 cycles RD_N in case with CSnBCR.PH1RD=1 00: 1 cycle 01: 2 cycles 10: 3 cycles 11: 4 cycles Note: In the case with CSnBCR.PH1RD=1 and CSnWCR.ADMUX=1,RD_N assertion delay cycle becomes 3 cycle.
10 to 7	WR[3:0]	1010	R/W	Number of Access Wait Cycles Specify the number of wait cycles necessary for read/write access.

				0000: 0 cycle	1000: 10 cycles
				0001: 1 cycle	1001: 12 cycles
				0010: 2 cycles	1010: 14 cycles
				0011: 3 cycles	1011: 18 cycles
				0100: 4 cycles	1100: 24 cycles
				0101: 5 cycles	1101: 32 cycles
				0110: 6 cycles	1110: 38 cycles
				0111: 8 cycles	1111: 52 cycles
6	WM	1	R/W	External Wait Mask Specification Specifies whether or not the external wait input is valid. The specification by this bit is valid even when the number of access wait cycles is 0. 0: External wait is valid 1: External wait is ignored	
5, 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.	
3	ADMUX	0/1*	R/W	Address Data Multiplex Mode Specification 0: Normal memory 1: AD-MUX memory At BS_N assert of the AD-MUX interface, address bits A27 to A17 are output from pins A11 to A1 and address bits A16 to A1 are output from pins D15 to D0.	

Bit	Bit Name	Initial Value	R/W	Description
2	—	All 0	R	Reserved This bit is always read as 0. The write value should always be 0.
1, 0	HW[1:0]	00	R/W	Delay Cycles from RD_N, WEn_N Negation to Address, CSn_N Negation Specify the number of delay cycles from RD_N and WEn_N negation to address and CSn_N negation. WEn_N and RD_N in case with CSnBCR.PH1RD=0 00: 0.5 cycle 01: 1.5 cycles 10: 2.5 cycles 11: 3.5 cycles RD_N in case with CSnBCR.PH1RD=1 00: 0 cycle 01: 1 cycles 10: 2 cycles 11: 3 cycles

Notes: 1. The initial value of the CS0 space differs according to the setting value of the BSCMD pin. When the BSCMD level is high, the SW bits become 11.
2. The initial value of the CS0 space differs according to the setting value of the BSCMD pin. When the BSCMD level is high, the ADMUX bit becomes 1.

- CS2WCR

Bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-		WSHW EN	WSW[1:0]		WHW[1:0]		BW[1:0]		PMD	BAS	-	WW[2:0]		
Initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	SW[2:0]		WR[3:0]				WM	-	-	ADMUX	-	HW[1:0]	
Initial value :	0	0	0	0/1	0/1	1	0	1	0	1	0	0	0	0	0	0
R/W :	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28	WSHWEN	0	R/W	0: Access is made according to SW[1:0] and HW[1:0] during the write cycle. 1: Access is made according to WSW[1:0] and WHW[1:0] during the write cycle.
27, 26	WSW[1:0]	00	R/W	Number of Delay Cycles from Address, CSn_N Assertion to RD_N, WEn_N Assertion Specify the number of delay cycles from address and CSn_N assertion to RD_N and WEn_N assertion during write cycles. When the WSHWEN bit is set to 1, the setting for this bit is enabled. 00: 0.5 cycle 01: 1.5 cycles 10: 2.5 cycles 11: 3.5 cycles
25, 24	WHW[1:0]	00	R/W	Number of Delay Cycles from RD_N, WEn_N Negation to Address, CSn_N Negation Specify the number of delay cycles from RD_N and WEn_N negation to address and CSn_N negation during write cycles. When the WSHWEN bit is set to 1, the setting for this bit is enabled. 00: 0.5 cycle 01: 1.5 cycles 10: 2.5 cycles 11: 3.5 cycles
23, 22	BW[1:0]	00	R/W	Number of Burst Wait Cycles Specify the number of wait cycles to be inserted in the second and later access cycles in burst access. 00: 0 cycle 01: 1 cycle 10: 2 cycles 11: 3 cycles Note: The bit positions are different from the burst ROM.

Bit	Bit Name	Initial Value	R/W	Description
21	PMD	0	R/W	Page Mode Specification when SRAM with Byte Selection is Used Specifies the page mode of SRAM with byte selection. 0: Non-page mode access 1: Page mode access
20	BAS	0	R/W	Byte Access Selection when SRAM with Byte Selection is Used Specifies the WEn_N and RDWR signal timing when SRAM interface with byte selection is used. 0: Asserts the WEn_N signal at the read/write timing and asserts the RDWR signal during the write access cycle 1: Asserts the WEn_N signal during the read/write access cycle and asserts the RDWR signal at the write timing
19	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
18 to 16	WW[2:0]	000	R/W	Number of Wait Cycles in Write Access Specify the number of cycles necessary for write access. 000: The same cycles as WR[3:0] settings (read access wait) 001: 0 cycle 010: 1 cycle 011: 2 cycles 100: 3 cycles 101: 4 cycles 110: 5 cycles 111: 6 cycles
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
12, 11	SW[1:0]	00	R/W	Number of Delay Cycles from Address, CSn_N Assertion to RD_N, WEn_N Assertion Specify the number of delay cycles from address and CSn_N assertion to RD_N and WEn_N assertion. WEn_N and RD_N in case with CSnBCR.PH1RD=0 00: 0.5 cycle 01: 1.5 cycles 10: 2.5 cycles 11: 3.5 cycles RD_N in case with CSnBCR.PH1RD=1 00: 1 cycle 01: 2 cycles 10: 3 cycles 11: 4 cycles Note: In the case with CSnBCR.PH1RD=1 and CSnWCR.ADMUX=1,RD_N assertion delay cycle becomes 3 cycle.
10 to 7	WR[3:0]	1010	R/W	Number of Access Wait Cycles Specify the number of cycles necessary for read/write access. 0000: 0 cycle 0001: 1 cycle 0010: 2 cycles 0011: 3 cycles 0100: 4 cycles 0101: 5 cycles 0110: 6 cycles 0111: 8 cycles 1000: 10 cycles 1001: 12 cycles 1010: 14 cycles 1011: 18 cycles 1100: 24 cycles 1101: Setting prohibited 1110: Setting prohibited 1111: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Description
6	WM	1	R/W	External Wait Mask Specification Specifies whether or not the external wait input is valid. The specification by this bit is valid even when the number of access wait cycles is 0. 0: External wait input is valid 1: External wait input is ignored
5, 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3	ADMUX	0/1*	R/W	Address Data Multiplex Mode Specification 0: Normal memory 1: AD-MUX memory At BS_N assert of the AD-MUX interface, address bits A27 to A17 are output from pins A11 to A1 and address bits A16 to A1 are output from pins D15 to D0.
2	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
1, 0	HW[1:0]	00	R/W	Delay Cycles from RD_N, WEn_N Negation to Address, CSn_N Negation Specify the number of delay cycles from RD_N and WEn_N negation to address and CSn_N negation. 00: 0.5 cycle 01: 1.5 cycles 10: 2.5 cycles 11: 3.5 cycles

Note: * The initial value of the CS0 space differs according to the setting value of the BSCMD pin. When the BSCMD level is high, the ADMUX bit becomes 1.

(2) Burst ROM

- CS0WCR, CS2WCR, CS4WCR

Bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-		WSH WEN	WSW[1:0]		WHW[1:0]		BSTMD[1:0]		-	BAS	BSW[1:0]		BW[1:0]	
Initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	SW[2:0]			W[3:0]			WM	-	-	AD MUX	-	HW[1:0]	
Initial value :	0	0	0	0/1	0/1	1	0	1	0	1	0	0	0/1	0	0	0
R/W :	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28	WSHWEN	0	R/W	0: Access is made according to SW[1:0] and HW[1:0] during the write cycle. 1: Access is made according to WSW[1:0] and WHW[1:0] during the write cycle.
27, 26	WSW[1:0]	00	R/W	Number of Delay Cycles from address, CSn_N assertion to RD_N, WEn_N assertion Specify the number of delay cycles from address and CSn_N assertion to RD_N and WEn_N assertion during write cycles. When the WSHWEN bit is set to 1, the setting for this bit is enabled. 00: 0.5 cycle 01: 1.5 cycles 10: 2.5 cycles 11: 3.5 cycles

Bit	Bit Name	Initial Value	R/W	Description
25, 24	WHW[1:0]	00	R/W	Number of Delay Cycles from address, CSn_N assertion to RD_N, WEn_N assertion Specify the number of delay cycles from address and CSn_N assertion to RD_N and WEn_N assertion during write cycles. When the WSHWEN bit is set to 1, the setting for this bit is enabled. 00: 0.5 cycle 01: 1.5 cycles 10: 2.5 cycles 11: 3.5 cycles
23, 22	BSTMD[1:0]	00	R/W	Burst Mode Specification 00: 8-burst mode 01: 4-burst mode 10: 16-burst mode 11: Prohibition
21	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	BAS	0	R/W	Byte access selection of Burst ROM When Burst ROM is selected, this bit specify the timing of WEn_N and RDWR. 0: WEn_N is asserted according to the timing of reading and writing. RDWR is asserted while writing access. 1: WEn_N is asserted while writing access. RDWR is s asserted according to the timing of reading and writing.
19, 18	BSW[1:0]	00	R/W	Number of BS_N Assert Cycles Specify the number of cycles for the BS_N assert period. 00: 1 cycle 01: 2 cycles 10: 3 cycles 11: 4 cycles

Bit	Bit Name	Initial Value	R/W	Description
17, 16	BW[1:0]	00	R/W	Number of Burst Wait Cycles Specify the number of wait cycles to be inserted in the second and later access cycles in burst read access. 00: 0 cycle 01: 1 cycle 10: 2 cycles 11: 3 cycles
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12, 11	SW[1:0]	00/11*1	R/W	Number of Delay Cycles from Address, CSn_N Assertion to RD_N, WEn_N Assertion Specify the number of delay cycles from address and CSn_N assertion to RD and WEn_N assertion. WEn_N and RD_N in case with CSnBCR.PH1RD=0 00: 0.5 cycle 01: 1.5 cycles 10: 2.5 cycles 11: 3.5 cycles RD_N in case with CSnBCR.PH1RD=1 00: 1 cycle 01: 2 cycles 10: 3 cycles 11: 4 cycles Note: In the case with CSnBCR.PH1RD=1 and CSnWCR .ADMUX=1,RD_N assertion delay cycle becomes 3 cycle.
10 to 7	W[3:0]	1010	R/W	Number of Access Wait Cycles Specify the number of wait cycles to be inserted in the write and first read access cycles. 0000: 0 cycle 1000: 10 cycles 0001: 1 cycle 1001: 12 cycles 0010: 2 cycles 1010: 14 cycles 0011: 3 cycles 1011: 18 cycles 0100: 4 cycles 1100: 24 cycles 0101: 5 cycles 1101: Setting prohibited 0110: 6 cycles 1110: Setting prohibited 0111: 8 cycles 1111: Setting prohibited

6	WM	1	R/W	External Wait Mask Specification Specify whether or not the external wait input is valid. The specification by this bit is valid even when the number of access wait cycles is 0. 0: External wait input is valid 1: External wait input is ignored
5, 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3	ADMUX	0/1*2	R/W	Address Data Multiplex Mode Specification 0: Normal memory 1: AD-MUX memory At BS_N assert of the AD-MUX interface, address bits A27 to A17 are output from pins A11 to A1 and address bits A16 to A1 are output from pins D15 to D0.
2	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
1, 0	HW[1:0]	00	R/W	Delay Cycles from RD_N, WEn_N Negation to Address, CSn_N Negation Specify the number of delay cycles from RD_N and WEn _N negation to address and CSn_N negation. WEn_N and RD_N in case with CSnBCR.PH1RD=0 00: 0.5 cycle 01: 1.5 cycles 10: 2.5 cycles 11: 3.5 cycles RD_N in case with CSnBCR.PH1RD=1 00: 0 cycle 01: 1 cycles 10: 2 cycles 11: 3 cycles

Notes: 1. The initial value of the CS0 space differs according to the setting value of the BSCMD pin. When the BSCMD level is high, the SW bits become 11.
2. The initial value of the CS0 space differs according to the setting value of the BSCMD pin. When the BSCMD level is high, the ADMUX bit becomes 1.

6.4.4 Reset Bus Wait Counter (RBWTCNT)

RBWTCNT is a 7-bit counter. This counter starts to decrement in synchronization with the CKO pin after a power-on reset is cleared, and stops when the value reaches H'00. External bus access is suspended while the counter is operating. This counter is provided to assure the minimum time from clearing a reset for flash memory and the like to the first access.

6.4.5 Busy Control Register (BUSYCR)

BUSYCR specifies the time period until access is started after BUSY is negated.

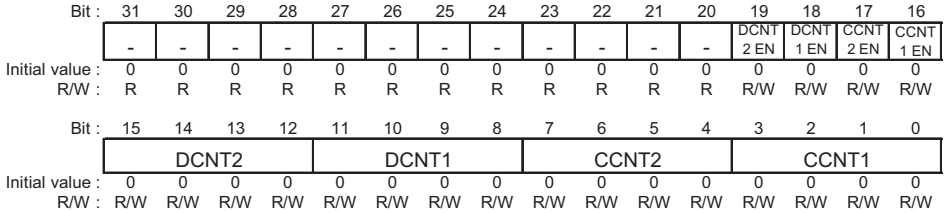
Bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	BUSY SETE	-	BUSYWAIT						
Initial value :	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0
R/W :	R	R	R	R	R	R	R	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	BUSYSETEN	1	R/W	Counts down the value that is specified by the BUSYWAIT bits after BUSY is negated. When an access to the BUSY_EN setting area of BCR occurs, an access is inhibited until counting down is completed. This bit is also used to enable the NBRST input. 0: BUSYWAIT bits are not set after BUSY is negated. NBRST input is invalid. 1: BUSYWAIT bits are set after BUSY is negated. NBRST input is valid.
7	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
6 to 0	BUSYWAIT[7:0]	H'04	R/W	Specify the wait period after BUSY is negated.

6.4.7 Burst ROM Timing Control Register (BROMTIMCR)

BROMTIMCR adjusts the data pin input timing and the CKO pin output timing.



Bit	Bit Name	Initial Value	R/W	Description
31 to 20	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
19	DCNT2EN	0	R/W	Enables the DCNT2 bit setting. In the case to set busrt write mode of CSnWCR2, and when CKO2 of CSnWCR2 is set to 1, the setting of this bit is selected. 0: Disabled 1: Enabled
18	DCNT1EN	0	R/W	Enables the DCNT1 bit setting. 0: Disabled 1: Enabled
17	CCNT2EN	0	R/W	Enables the CCNT2 bit setting. In the case to set busrt write mode of CSnWCR2, and when CKO2 of CSnWCR2 is set to 1, the setting of this bit is selected. 0: Disabled 1: Enabled
16	CCNT1EN	0	R/W	Enables the CCNT1 bit setting. 0: Disabled 1: Enabled

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	DCNT2[3:0]	0000	R/W	The timing input from the data signal pin is set. In the case to set busrt write mode of CSnWCR2, and when CKO2 of CSnWCR2 is set to 1, the setting of this bit is selected. 1111: Long delay ~ 0000: Short delay
11 to 8	DCNT1[3:0]	0000	R/W	The timing input from the data signal pin is set. 1111: Long delay ~ 0000: Short delay
7 to 4	CCNT2[3:0]	0	R/W	Sets the timing of output from the CKO pin. In the case to set busrt write mode of CSnWCR2, and when CKO2 of CSnWCR2 is set to 1, the setting of this bit is selected. 1111: Long delay ~ 0000: Short delay
3 to 0	CCNT[3:0]	0	R/W	Sets the timing of output from the CKO pin. 1111: Long delay ~ 0000: Short delay

6.4.8 Memory Protection Area Settings Register (BPTCR00 to 31)

BPTCR is a 32-bit register that configures write protection for the external memory space.

Write-protection settings can be set in 64-bit increments for a designated 2-Gbit area starting at the initial address of each supported external memory space. This register has register write protection functions that disable setting changes from CPUs that do not have access privileges.

Bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	CPUTYPE[1:0]		REG WP	-	-	-	-			RP_ RSP	WP_ RSP
Initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R/W	R/W

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	BB_ RP	AP_ RP	-	-	-	-	-	-	BB_ WP	AP_ WP
Initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 27	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
26, 25	CPUTYPE[1:0]	00	R	These bits specify the type of CPU that has the privilege to change this register's settings. When setting the privilege to change settings in this register, also write 1 to the REGWP bit. The CPU set in this register is automatically designated as the CPU that has the privilege to change settings. When B'0 is written to the REGWP bit, these bits are cleared to B'00, allowing settings to be changed from all CPUs. 00: All CPUs have the privilege to change settings. 01: Only AP-SH has the privilege to change settings. 10: Only AP-ARM has the privilege to change settings.

Bit	Bit Name	Initial Value	R/W	Description
24	REGWP	0	R/W	Privilege to Change Register Setting This bit specifies whether the CPU that specified this register's settings permits the settings value to be changed by other CPUs. After 1 is written to this bit, the bit automatically becomes 0. When this bit is set to 1, the type of CPU that set this register is specified in CPUTYPE. After the register value changes, the register is read and this bit returns to 0. Accordingly, do not start a memory area access until first checking with software that CPUTYPE has been set. Also, write operations from CPUs that do not have the privilege to change settings, as specified by CPUTYPE, are disabled. 0: Enables all CPUs to change settings. 1: Only the CPU that set this register has the privilege to change settings.
23 to 18	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
17	RP_RSP	0	R/W	This bit specifies the BSC response method when a read access to the read protection area occurs. If a CPU that does not have the privilege to change this register's settings as specified in CPUTYPE attempts to write to this bit, the operation is ignored. 0: An error response is sent. 1: No error response is sent. About error responses when this bit is set to 0 When AP-SH accesses the protected area, BSC returns an error response, but AP-SH exception handling does not occur. When AP-ARM accesses the protected area, the error is treated as a data abort condition.

Bit	Bit Name	Initial Value	R/W	Description
16	WP_RSP	0	R/W	This bit specifies the BSC response method when a write access to the read protection area occurs. If a CPU that does not have the privilege to change this register's settings as specified in CPUTYPE attempts to write to this bit, the operation is ignored. 0: An error response is sent. 1: No error response is sent. About error responses when this bit is set to 0 When AP-SH accesses the protected area, BSC returns an error response, but AP-SH exception handling does not occur. When AP-ARM accesses the protected area, the error is treated as a data abort condition.
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	BB_RP	0	R/W	Privilege to Read BB Resource* Setting If a CPU that does not have the privilege to change this register's settings as specified in CPUTYPE attempts to write to this bit, the operation is ignored. When the read protection area is read, this bit is read as 0.
8	AP_RP	0	R/W	Privilege to Read AP Resource* Setting If a CPU that does not have the privilege to change this register's settings as specified in CPUTYPE attempts to write to this bit, the operation is ignored. 0: The read privilege for the corresponding BSC area exists. 1: No read privilege for the corresponding BSC area exists. When the read protection area is read, this bit is read as 0.
7 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
1	BB_WP	0	R/W	Privilege to Write to BB Resource* Setting If a CPU that does not have the privilege to change this register's settings as specified in CPUTYPE attempts to write to this bit, the operation is ignored. 0: The read privilege for the corresponding BSC area exists. 1: No read privilege for the corresponding BSC area exists.
0	AP_WP	0	R/W	AP Resource Write Authorization Settings If a CPU that does not have the privilege to change this register's settings as specified in CPUTYPE attempts to write to this bit, the operation is ignored. 0: The write privilege for the corresponding BSC area exists. 1: No write privilege for the corresponding BSC area exists.

Note: * AP resources: AP-SH, AP-ARM, AP-DMAC (RT-DMAC, SYS-DMAC), AP-JTAG, etc. (image IP and MBXL)
BB resources: ACMFI

6.4.9 BS assert period Settings Register (BSWCR)

BSWCR is a 32-bit register that specifies the period of BS_N assert.

Bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	BSCS6A[1:0]		BSCS5B[1:0]		BSCS5A[1:0]		BSCS4[1:0]		-	-	BSCS2[1:0]		BSCS0[1:0]	
Initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
13,12	BSCS6A[1:0]	00	R/W	BS_N assert cycle number of area CS6A specifies. 00: 1 cycle 01: 2 cycle 10: 3 cycle 11: Prohibition
11,10	BSCS5B[1:0]	00	R/W	BS_N assert cycle number of area CS5B specifies. 00: 1 cycle 01: 2 cycle 10: 3 cycle 11: Prohibition
9, 8	BSCS5A[1:0]	00	R/W	BS_N assert cycle number of area CS5A specifies. 00: 1 cycle 01: 2 cycle 10: 3 cycle 11: Prohibition
7, 6	BSCS4[1:0]	00	R/W	BS_N assert cycle number of area CS4 specifies. 00: 1 cycle 01: 2 cycle 10: 3 cycle 11: Prohibition [notes] When burst ROM is selected,these bits set 00 and BS_N assert cycle number is specifies by BSW bits of CS4WCR.
5, 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3, 2	BSCS2[1:0]	00	R/W	BS_N assert cycle number of area CS2 specifies. 00: 1 cycle 01: 2 cycle 10: 3 cycle 11: Prohibition [notes] When burst ROM is selected,these bits set 00 and BS_N assert cycle number is specifies by BSW bits of CS2WCR.

Bit	Bit Name	Initial Value	R/W	Description
1, 0	BSCS0[1:0]	00	R/W	BS_N assert cycle number of area CS0 specifies. 00: 1 cycle 01: 2 cycle 10: 3 cycle 11: Prohibition [notes] When burst ROM is selected,these bits set 00 and BS_N assert cycle number is specifies by BSW bits of CS0WCR.

6.4.10 CSn Space Wait Control Register 2(CSnWCR2) (n = 0, 2, 4)

CSnWCR2 specifies various wait cycles for memory accesses. Specify CSnWCR2 before accessing the target area.

CSnWCR is initialized to H'0000 0000 by a power-on reset. However, CSnWCR is not initialized but retains the previous value in standby mode.

Bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	BST16	–	RWAIT			–	WWAIT			–	CKO2	WAITMD	BWMD
Initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	BST16	0	R/W	Burst write setting 0: 8 burst write 1: 16 burst write
11	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
10 to 8	RWAIT[2:0]	000	R/W	After WAIT_N sampling, beginning of burst read is set. 000: 1cycle 001: 2cycle 010: 3cycle 100: 0cycle
7	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
6 to 4	WWAIT[2:0]	000	R/W	After WAIT_N sampling, beginning of burst write is set. 100: 1cycle 000: 2cycle 001: 3cycle Excluding the above-mentioned : reserve
3	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	CKO2	0	R/W	In the Case of BWMD bit is 1 0: Feedback CKO is selected 1: Feedback CKO2 is selected
1	WAITMD	0	R/W	WAIT mode is set. This bit sets the method of WAIT_N sampling. 0: WAIT_N signal is not sampling by CKO. 1: WAIT_N signal is sampling by CKO.
0	BWMD	0	R/W	Burst Write mode specifies. 0: Single Write mode Write cycle is asynchronous single write. BST16 , RWAIT[1:0] and WWAIT[1:0] are invalid. 1: Burst Write mode Write cycle is burst write. BST16 , RWAIT[1:0] and WWAIT[1:0] are valid.

6.5 Operation

6.5.1 Endian/Access Size and Data Alignment

This LSI supports little endian, in which the 0 address is the least significant byte (LSByte) in the byte data. Two data bus widths (8 bits and 16 bits) are available for normal memory and SRAM with byte selection. Data alignment is performed in accordance with the data bus width of the device and endian. This also means that when longword data is read from an 8-bit width device, the read operation must be done four times. In this LSI, data alignment and conversion of the data length are performed automatically between the respective interfaces.

Tables 6.8 and 6.9 show the relationship between endian, device data width, and access unit.

Table 6.8 16-Bit External Device/Little Endian Access and Data Alignment

		Data Bus		Strobe Signals	
Operation		**D15 to D8**	**D7 to D0**	**WE1_N**	**WE0_N**
Byte access at 0		—	Data 7 to data 0	—	Assert
Byte access at 1		Data 7 to data 0	—	Assert	—
Byte access at 2		—	Data 7 to data 0	—	Assert
Byte access at 3		Data 7 to data 0	—	Assert	—
Word access at 0		Data 15 to data 8	Data 7 to data 0	Assert	Assert
Word access at 2		Data 15 to data 8	Data 7 to data 0	Assert	Assert
Longword access at 0	1st time at 0	Data 15 to data 8	Data 7 to data 0	Assert	Assert
	2nd time at 2	Data 31 to data 24	Data 23 to data 16	Assert	Assert

Table 6.9 8-Bit External Device/Little Endian Access and Data Alignment

		Data Bus		Strobe Signals	
Operation		**D15 to D8**	**D7 to D0**	**WE1_N**	**WE0_N**
Byte access at 0		—	Data 7 to data 0	—	Assert
Byte access at 1		—	Data 7 to data 0	—	Assert
Byte access at 2		—	Data 7 to data 0	—	Assert
Byte access at 3		—	Data 7 to data 0	—	Assert
Word access at 0	1st time at 0	—	Data 7 to data 0	—	Assert
	2nd time at 1	—	Data 15 to data 8	—	Assert
Word access at 2	1st time at 2	—	Data 7 to data 0	—	Assert
	2nd time at 3	—	Data 15 to data 8	—	Assert
Longword access at 0	1st time at 0	—	Data 7 to data 0	—	Assert
	2nd time at 1	—	Data 15 to data 8	—	Assert
	3rd time at 2	—	Data 23 to data 16	—	Assert
	4th time at 3	—	Data 31 to data 24	—	Assert

6.5.2 Normal Space Interface

(1) Basic Timing

For access to a normal space, this LSI uses strobe signal output in consideration of the fact that mainly SRAM without a byte-selection pin will be directly connected. When using SRAM with a byte-selection pin, see section 6.5.6, SRAM Interface with Byte Selection. Figure 6.2 shows the basic timing of normal space access. A no-wait normal access is completed in two cycles. The BS_N signal indicates that the bus cycle has started, and is asserted one clock cycle.

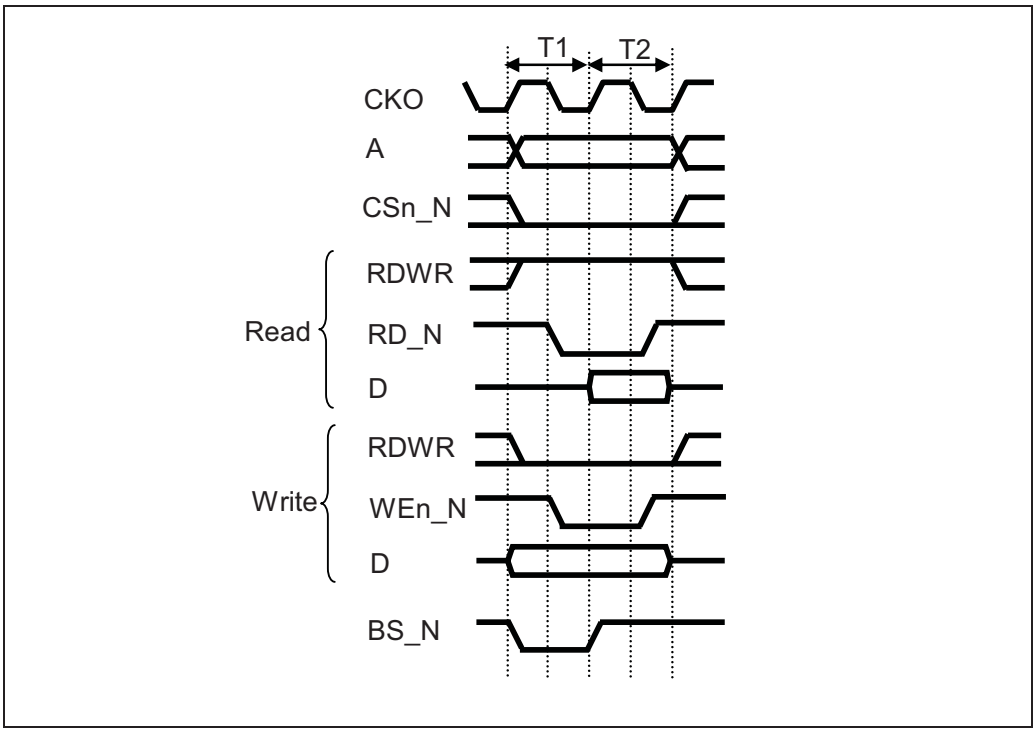


Figure 6.2 Normal Space Basic Access Timing (Access Wait = 0 (WW[2:0] = B'000, W/WR[3:0] = B'0000, SW[1:0] = B'00, HW[1:0] = B'00))

There is no access size specification when reading from the external bus. The correct access start address is output in the least significant bit of the address, but since there is no access size specification, 16 bits are always read in case of a 16-bit device. When writing, only the WEn_N signal for the byte to be written is asserted.

It is necessary to output the data that has been read using the RD_N signal when a buffer is provided in the data bus. The RDWR signal is in a read state (high output) when no access has been carried out. Therefore, care must be taken to avoid collision when controlling the external data buffer using RDWR signal.

Figures 6.3 and 6.4 show the basic timings of continuous accesses to a normal space. If the WM bit in CSnWCR is cleared to 0, a Tnop cycle is inserted to evaluate the external wait (figure 6.3). However, if the WM bit is set to 1, external waits are ignored and no Tnop cycle is inserted (figure 6.4).

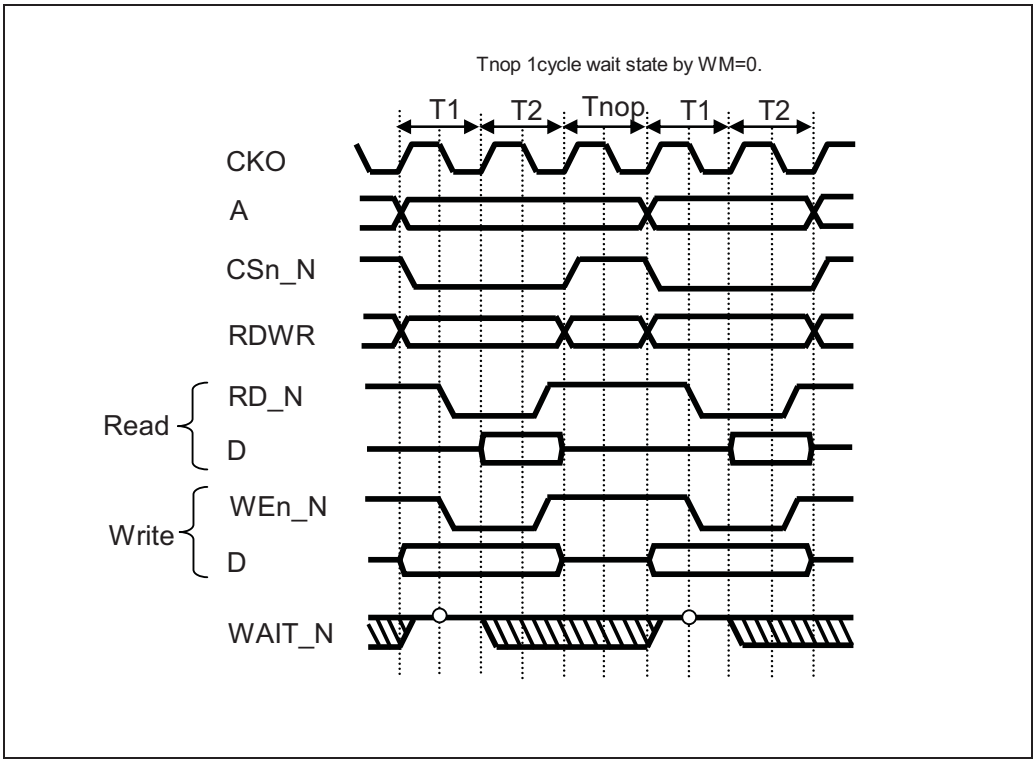


Figure 6.3 Continuous Access for Normal Space 1
Bus Width = 16 Bits, Longword Access, WM Bit in CSnWCR = 0
(Access Wait = 0 (WW[2:0] = B'000, W/WR[3:0] = B'0000, SW[1:0] = B'00,
HW[1:0] = B'00), Cycle Wait = 0 (IWW[1:0] = B'00, IWRWD[1:0] = B'00,
IWRWS[1:0] = B'00, IWRRD[1:0] = B'00, IWRRS[1:0] = B'00))

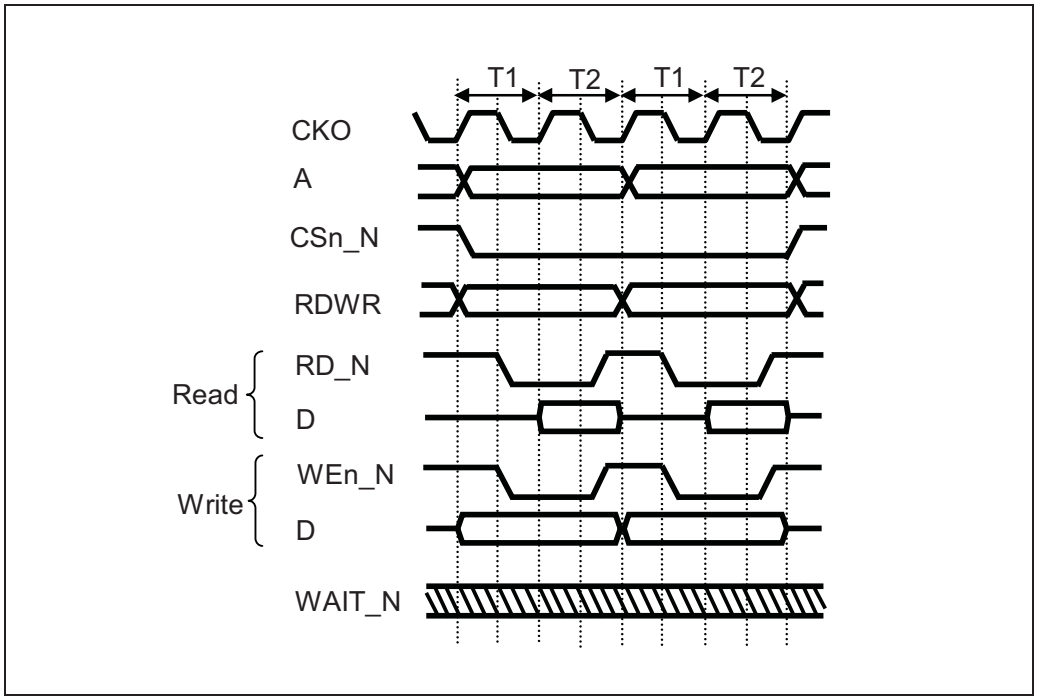


Figure 6.4 Continuous Access for Normal Space 2
Bus Width = 16 Bits, Longword Access, WM Bit in CSnWCR = 1
(Access Wait = 0 (WW[2:0] = B'000, W/WR[3:0] = B'0000, SW[1:0] = B'00, HW[1:0] = B'00), Cycle Wait = 0 (IWW[1:0] = B'00, IWRWD[1:0] = B'00, IWRWS[1:0] = B'00, IWRRD[1:0] = B'00, IWRRS[1:0] = B'00))

Figure 6.5 shows an example of connection to 16-bit data-width SRAM.

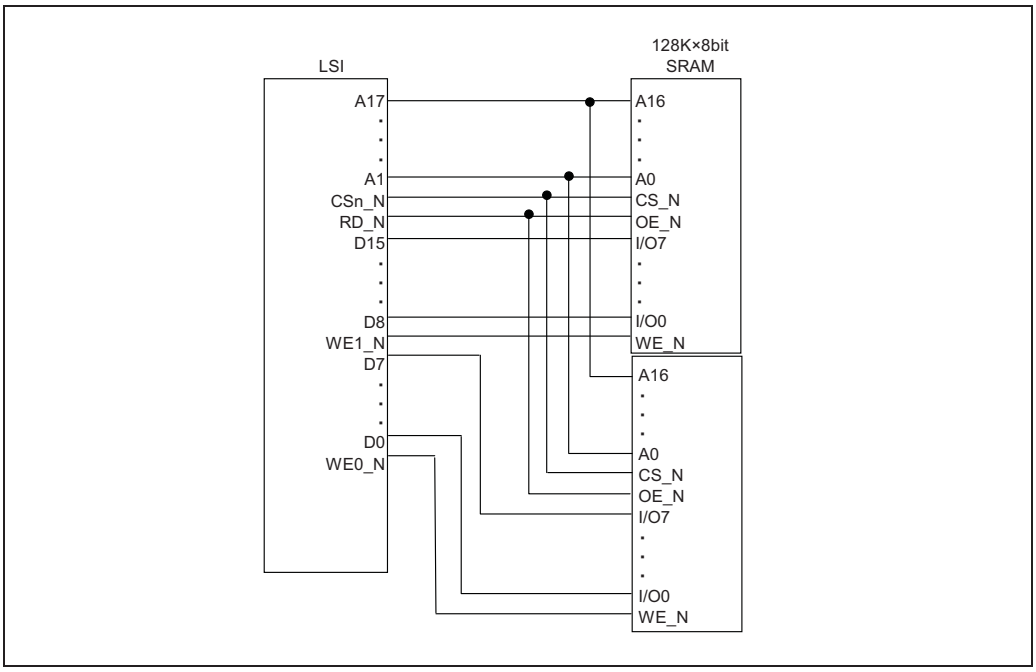


Figure 6.5 Example of 16-Bit Data-Width SRAM Connection

Figure 6.6 shows an example of connection to 8-bit data-width SRAM.

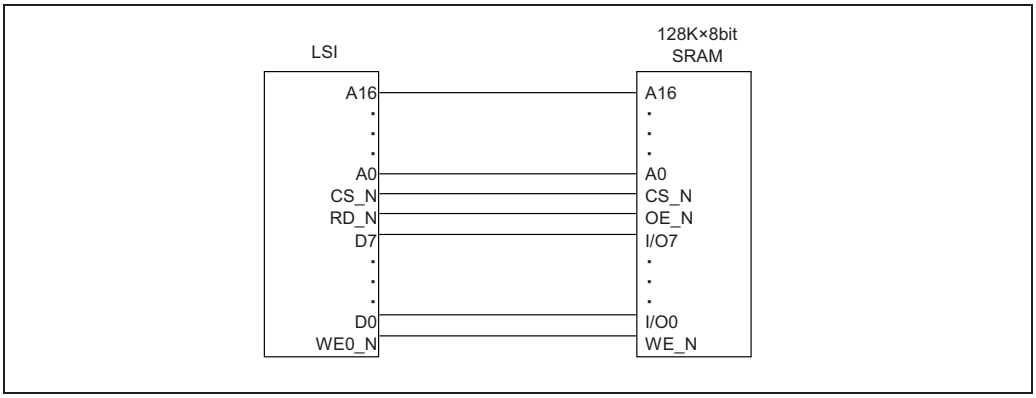


Figure 6.6 Example of 8-Bit Data-Width SRAM Connection

6.5.3 Access Wait Control

Wait cycle insertion on a normal space access can be controlled by setting the WR bits in CSnWCR. Setting the WW bits can insert wait cycles independently in read access and in write access. The specified number of Tw cycles are inserted as wait cycles in a normal space access shown in figure 6.7.

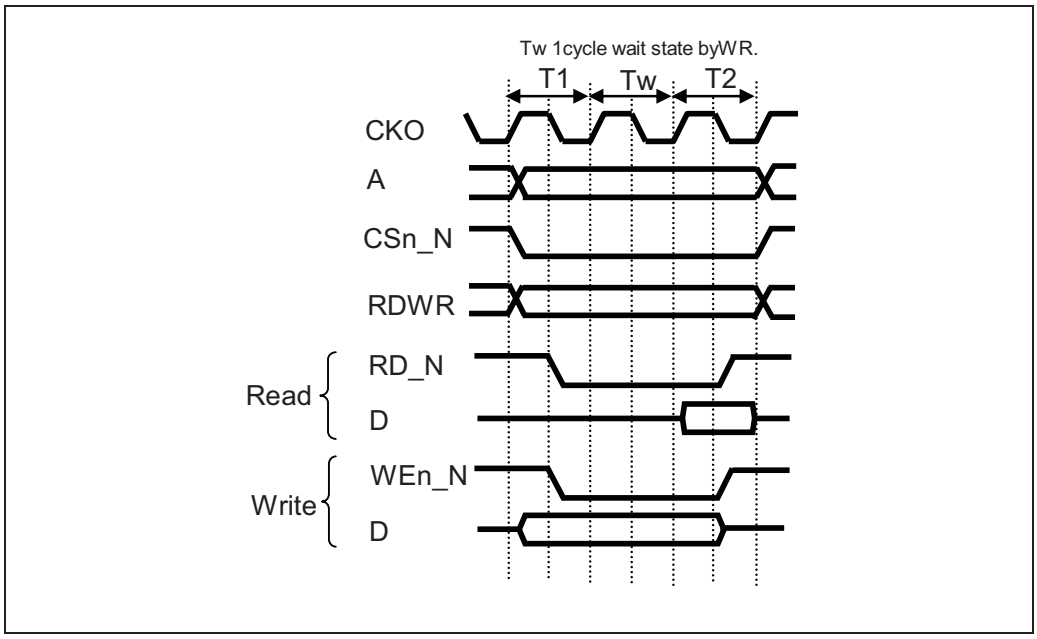


Figure 6.7 Wait Timing for Normal Space Access (Software Wait Only)
(Setting Example in Figure: Access Wait = 1 (WW[2:0] = B'000, W/WR[3:0] = B'0001, SW[1:0] = B'00, HW[1:0] = B'00))

When the WM bit in CSnWCR is cleared to 0, the external wait input WAIT_N signal is also sampled. WAIT_N pin sampling is shown in figure 6.8. A 2-cycle wait is specified as a software wait. The WAIT_N signal is sampled at the falling edge of CKO at the transition from the T1 or Tw cycle to the T2 cycle.

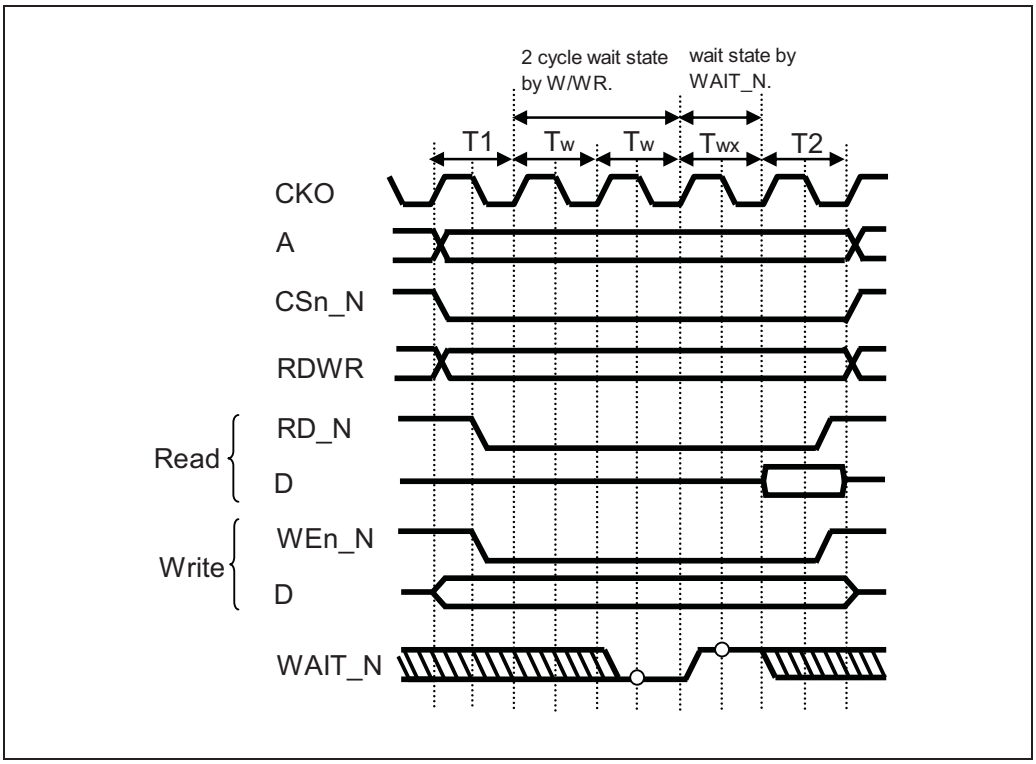


Figure 6.8 Wait Cycle Timing for Normal Space Access (Wait Cycle Insertion Using WAIT_N Signal) (Setting Example in Figure: Access Wait = 2 (WW[2:0] = B'000, W/WR[3:0] = B'0010, SW[1:0] = B'00, HW[1:0] = B'00), External Wait Valid (WM = 0))

6.5.4 CSn_N Assert Period Extension

The number of cycles from CSn_N assertion to RD_N, WEn_N assertion can be specified by setting the SW bits in CSnWCR. The number of cycles from RD_N, WEn_N negation to CSn_N negation can be specified by setting the HW bits. Therefore, a flexible interface to an external device can be obtained.

Figure 6.9 shows an example.

A Th cycle and a Tf cycle are added before and after an ordinary cycle, respectively. In these cycles, RD_N and WEn_N are not asserted, while other signals are asserted. The data output is prolonged to the Tf cycle, and this prolongation is useful for devices with slow write operations.

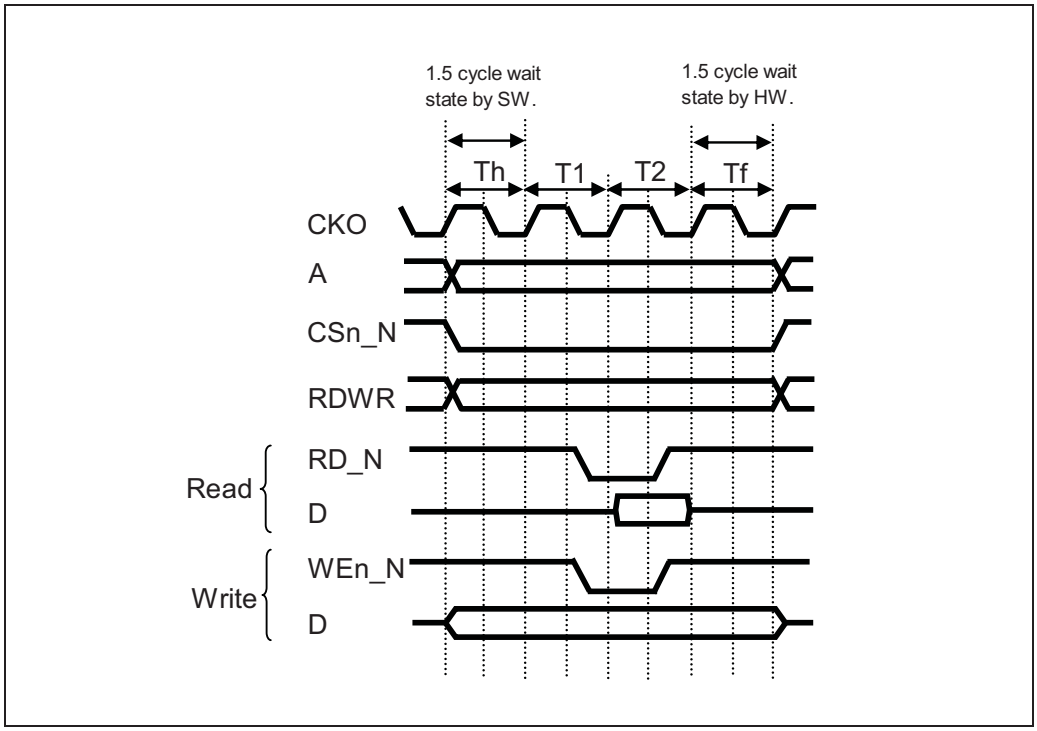


Figure 6.9 CSn_N Assert Period Extension
(Setting Example in Figure: Access Wait = 0, Setup Wait = 1, Hold Wait = 1
(WW[2:0] = B'000, W/WR[3:0] = B'0000, SW[1:0] = B'01, HW[1:0] = B'01))

6.5.5 Burst ROM Interface

(1) Page Mode

The burst ROM interface is used to access a memory with a high-speed read function using a method of address switching called burst mode or page mode. In the burst ROM interface, basically the same access as the normal space is performed, but the second and subsequent accesses are performed by changing only the address, without negating the RD_N signal at the end of the first cycle. In the second and subsequent accesses, addresses are changed at the falling edge of CKO.

For the first access cycle, the number of wait cycles specified by the W bits in CSnWCR is inserted. For the second and subsequent access cycles, the number of wait cycles specified by the BW bits in CSnWCR is inserted.

In the burst ROM access, the BS_N signal is asserted only in the first access cycle. Also, an external wait input is valid only in the first access cycle.

In the single access or write access that does not perform the burst operation in the burst ROM interface, access timing is the same as a normal space.

Table 6.10 lists a relationship between the bus width, access size, and number of bursts. Figure 6.10 shows a timing chart.

Table 6.10 Relationship between Bus Width, Access Size, and Number of Bursts

Bus Width	Access Size	Number of Bursts	Number of Accesses
8 bits	8 bits	1	1
	16 bits	2	1
	32 bits	4	1
	16 bytes	16	1
	32 bytes	16	2
16 bits 4-burst mode BSTMD = 1	8 bits	1	1
	16 bits	1	1
	32 bits	2	1
	16 bytes	4	2
	32 bytes	4	4
16 bits 8-burst mode BSTMD = 0	8 bits	1	1
	16 bits	1	1
	32 bits	2	1
	16 bytes	8	1
	32 bytes	8	2

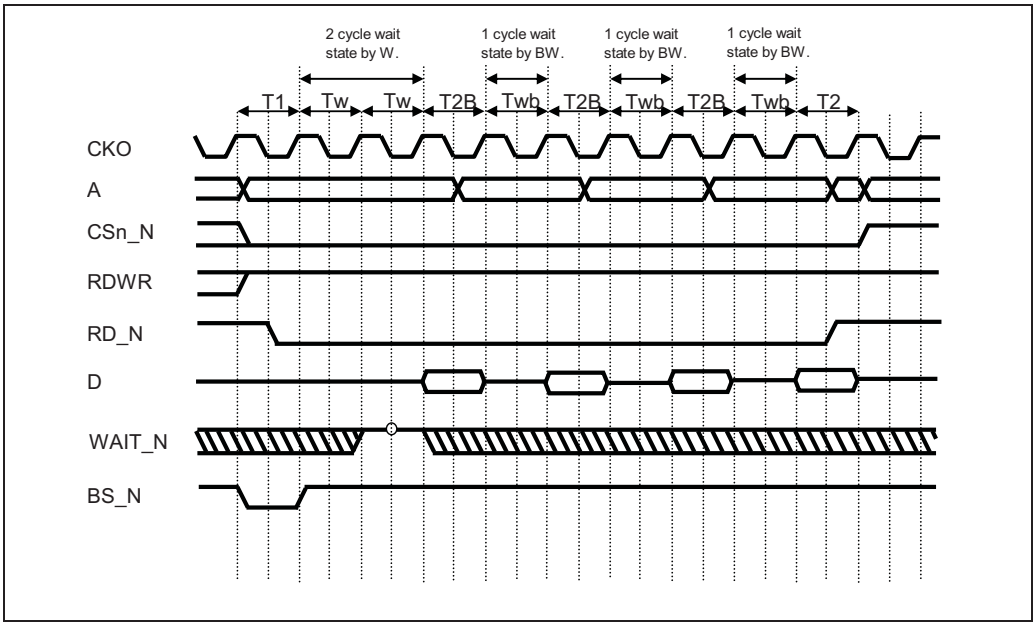


Figure 6.10 Burst ROM Access
(Bus Width = 16 Bits, 8-Byte Transfer (Number of Bursts = 4)
(Setting Example in Figure: Access Wait for 1st Time = 2, Access Wait for 2nd Time and After = 1, Setup Wait = 0, Hold Wait = 0 (BW[1:0] = B'01, W[3:0] = B'0010, SW[1:0] = B'00,
HW[1:0] = B'00, PH1RD = B'0, BROMMD = B'00))

(2) Clock Synchronous Burst Mode

This LSI can be interfaced with the memory having a clock-synchronous burst mode. To form the interface with memory of this type, connect the BS_N pin of this LSI to the address valid pin of the memory.

To assure the hold time for the clock that is supplied to the memory, set the BROMMD0 bit in CMNCR to 1. In addition, set the PH1RD bit in CSnBCR to 1 to assure the read data setup time for this LSI. Set the memory to wrap around with a burst length of 8.

Figures 6.11 and 6.12 show burst ROM (AD-MUX) access timings.

When the ADMUX bit in CSnWCR is set to 1 in the normal space interface or the burst ROM interface, the AD-MUX interface is specified for the CS0, CS2, and CS4 spaces. When the BSCMD external pin is reset to the high level, the ADMUX bit in CS0WCR is

set to its initial value of 1 and the AD-MUX interface is specified. In the AD-MUX interface, the lower 16 bits of the address, A16 to A1, are output from the data pins D15 to D0 and address bits A27 to A17 are output from address pins A11 to A1. In asynchronous mode, while BS_N is low, these outputs are loaded into memory and used as the address. In clock synchronous mode, these outputs are loaded into memory on the rising edge of CKO while BS_N is low and used as the address.

The BS_N assert period can be set by the BSW bits in CSnWCR. The access after BS_N negate is similar to an access in an interface other than the AD-MUX interface.

The WR3 to WR0 bits in CSnWCR control the wait period from negation of the RD_N signal to initial data loading. Figure 6.11 shows the timing chart when 3 cycles are specified by the WR3 to WR0 bits in CSnWCR. Initial data is loaded on the third CKO rising edge (Tck3) after the RD_N signal falls.

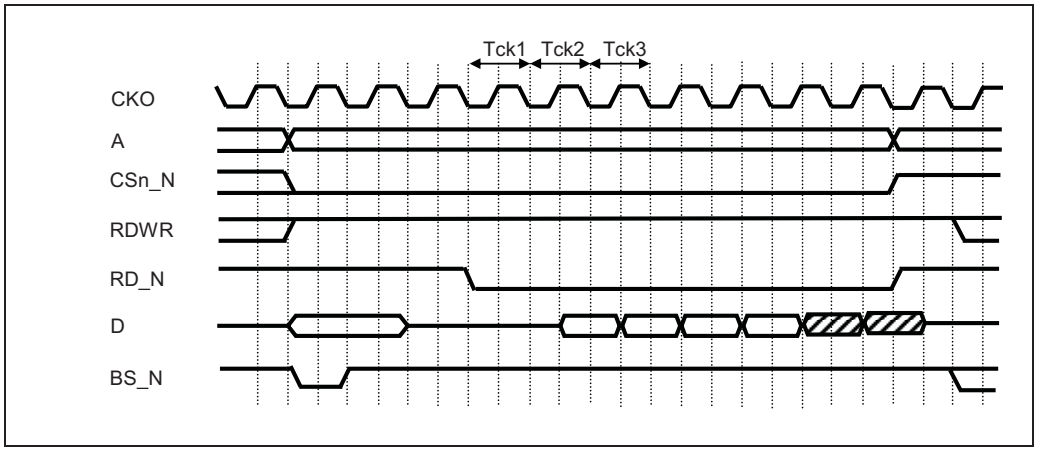


Figure 6.11 Burst ROM Access, 8-Byte Read
(Setting Example in Figure: Access Wait for 1st Time = 1, Access Wait for 2nd Time and After = 0, Setup Wait = 0, Hold Wait = 0 (BW[1:0] = B'00, W[3:0] = B'0011, SW[1:0] = B'10,
HW[1:0] = B'00), ADMUX = B'1, PH1RD = B'1, BROMMD = B'11, BSW = B'00)

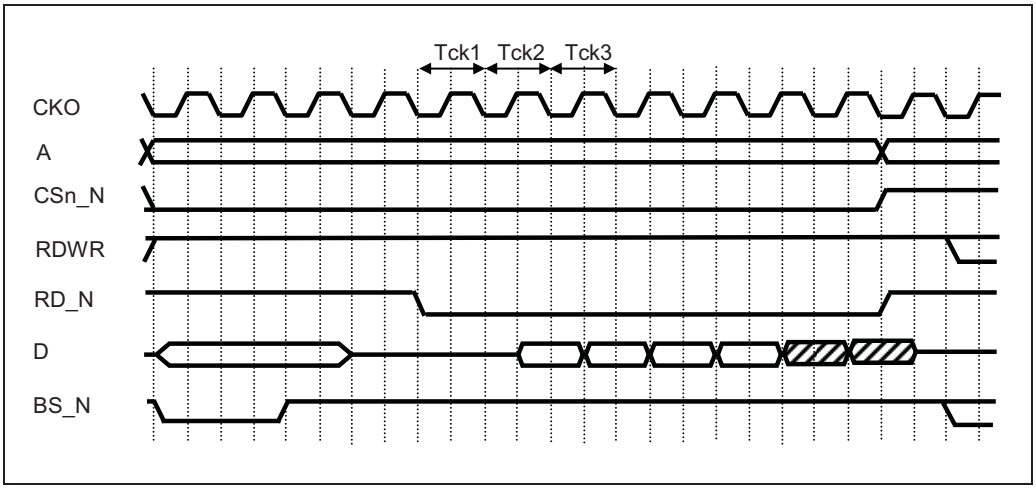


Figure 6.12 Burst ROM Access, 8-Byte Read
(ADMUX = B'1, PH1RD = B'1, BROMMD = B'11, BSW = B'01, SW = B'11)
(Setting Example in Figure: Access Wait for 1st Time = 1, Access Wait for 2nd Time and After = 0, Setup Wait = 0, Hold Wait = 0 (BW[1:0] = B'00, W[3:0] = B'0001, SW[1:0] = B'11,
HW[1:0] = B'00), ADMUX = B'1, PH1RD = B'1, BROMMD = B'11, BSW = B'01)

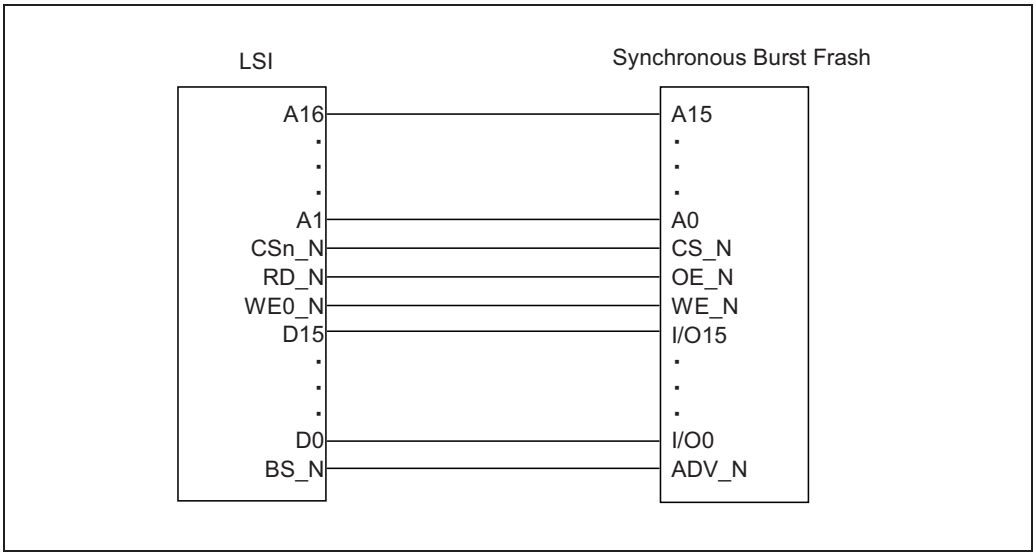


Figure 6.13 Synchronous Burst Flash Connection Example

6.5.6 SRAM Interface with Byte Selection

(1) Basic Access Timing

The SRAM interface with byte selection is a memory interface which outputs a byte-selection pin (WEn_N) in a read/write bus cycle. This interface has 16-bit data pins and accesses SRAMs having upper and lower byte-selection pins, such as UB and LB.

When the BAS bit in CSnWCR is cleared to 0 (initial value), the write access timing of the SRAM interface with byte selection is the same as that for the normal space interface. While in read access of the SRAM interface with byte selection, the byte-selection signal is output from the WEn_N pin, which is different from that for the normal space interface. The basic access timing is shown in figure 6.13. In write access, data is written to memory according to the timing of the byte-selection pin (WEn_N). For details, refer to the data sheet for the corresponding memory.

If the BAS bit is set to 1, the WEn_N pin and RDWR pin timings change. Figure 6.14 shows the basic access timing. In write access, data is written to memory according to the timing of the write enable pin (RDWR).

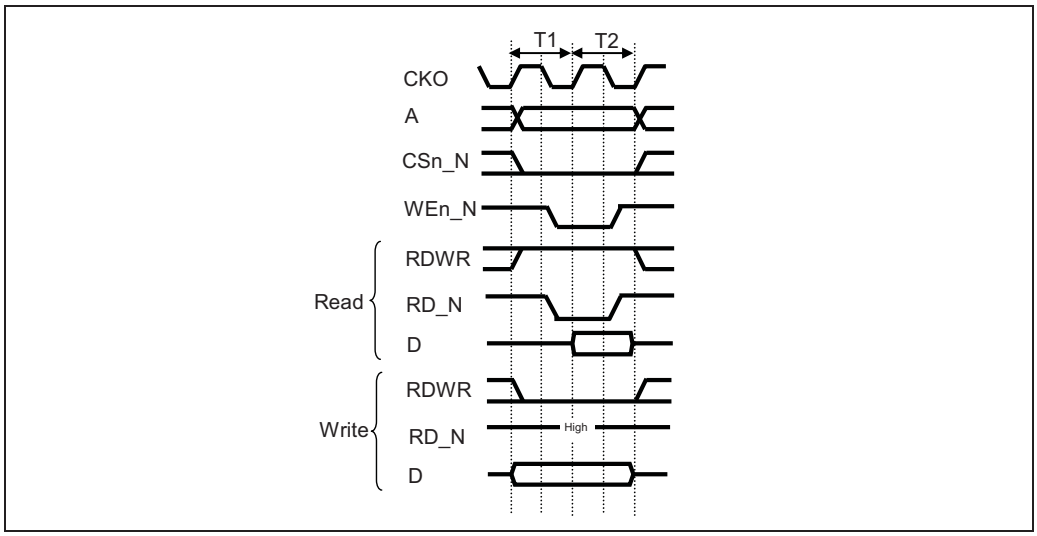


Figure 6.14 Basic Access Timing for SRAM with Byte Selection (BAS = 0) (Access Wait = 0 (WW[2:0] = B'000, W/WR[3:0] = B'0000, SW[1:0] = B'00, HW[1:0] = B'00))

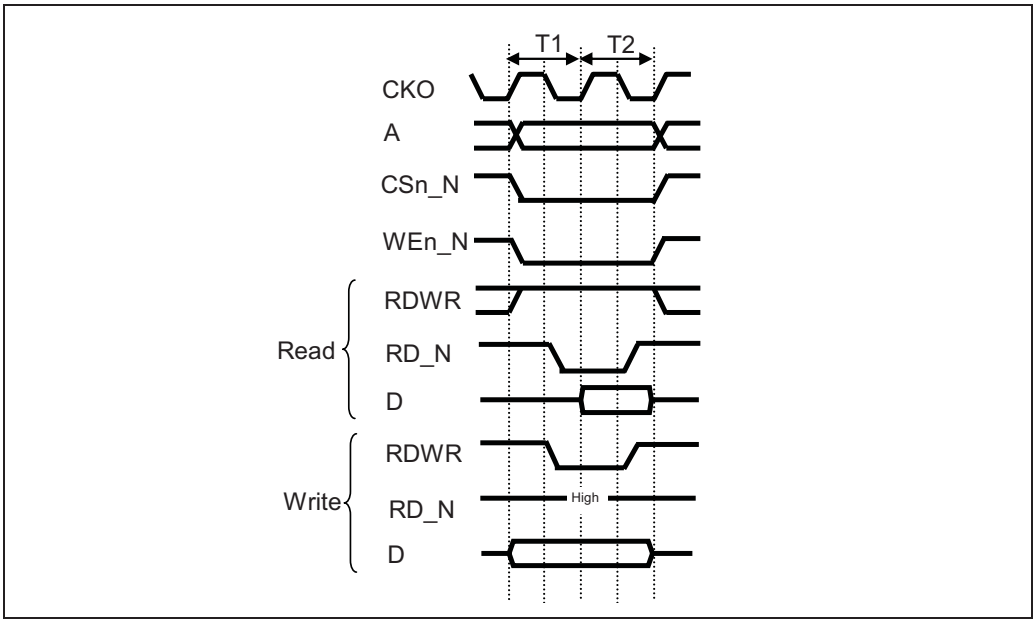


Figure 6.15 Basic Access Timing for SRAM with Byte Selection (BAS = 1) (Access Wait = 0 (WW[2:0] = B'000, W/WR[3:0] = B'0000, SW[1:0] = B'00, HW[1:0] = B'00))

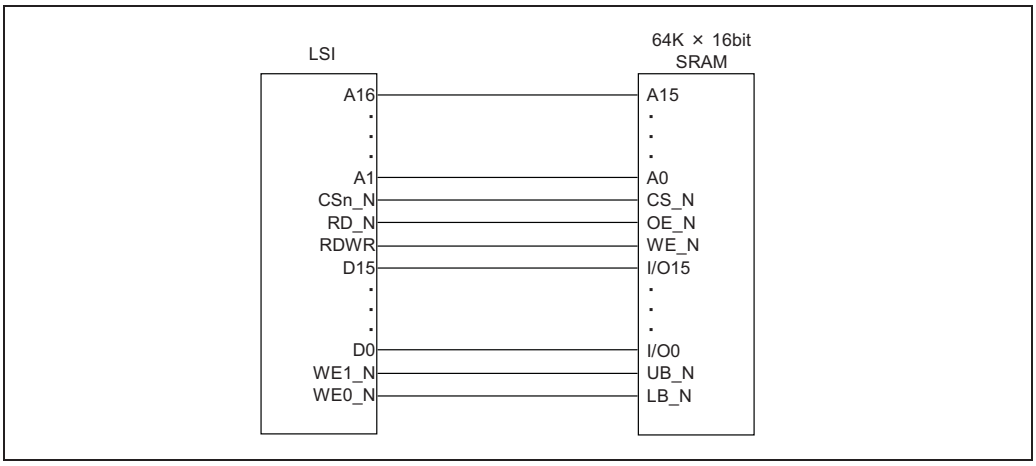


Figure 6.16 Example of Connection with SRAM with Byte Selection (16-Bit Data Bus)

(2) Page Mode of SRAM with Byte Selection

The page mode of SRAM with byte selection is used to access a memory with a high-speed read function using a method of address switching called burst mode or page mode. In page mode of SRAM with byte selection, basically the same access as the normal space is performed, but the 2nd and subsequent accesses are performed by changing only the address, without negating the RD_N signal at the end of the first cycle. In the second and subsequent accesses, addresses are changed at the falling edge of CKO*.

For the first access cycle, the number of wait cycles specified by the WR bits in CSnWCR is inserted. For the second and subsequent access cycles, the number of wait cycles specified by the BW bits in CSnWCR is inserted.

During the period of read in page mode, the BS_N signal is asserted only in the first access cycle. Also, an external wait input is valid only in the first access cycle.

The signal access or write access that does not perform the burst operation in page mode of SRAM with byte selection has the same access timing as an non-page mode access.

Table 6.11 lists a relationship between the bus width, access size, and number of bursts. Figures 6.16 and 6.17 show timing charts.

Note: * This description relates to a case where the CKO output and the BSC operation clock ZBCK are output in the same phase.

Bus Width	Access Size	Number of Bursts	Number of Accesses
8 bits	8 bits	1	1
	16 bits	2	1
	32 bits	4	1
	16 bytes	16	1
	32 bytes	16	2
16 bits	8 bits	1	1
	16 bits	1	1
	32 bits	2	1
	16 bytes	8	1
	32 bytes	8	2

Table 6.11 Relationship between Bus Width, Access Size, and Number of Bursts

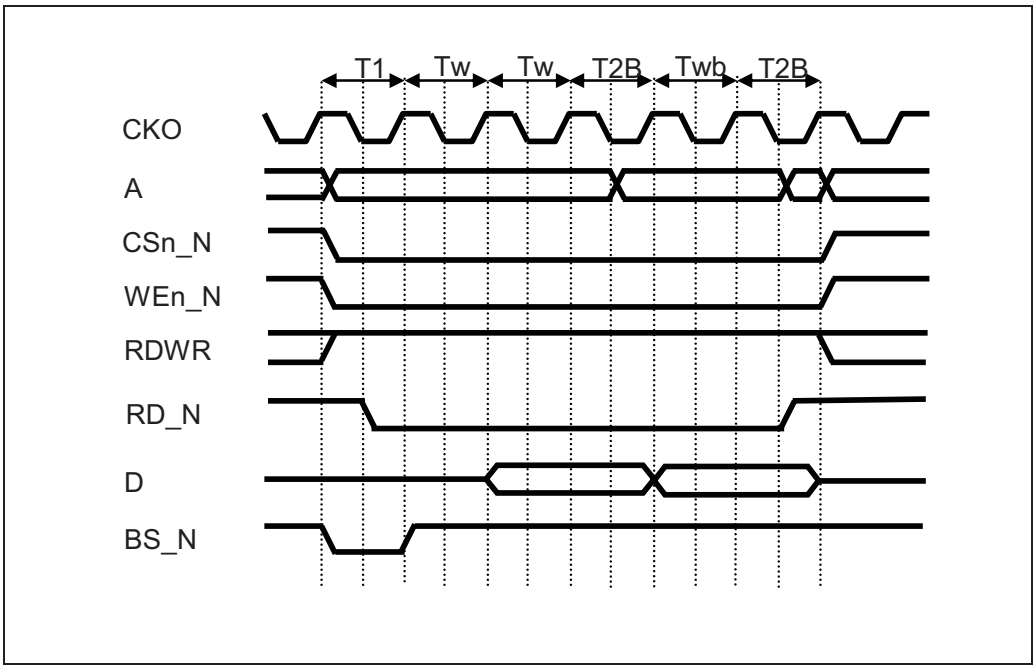


Figure 6.17 Page Mode Read for SRAM with Byte Selection (PMD = 1, BAS = 1) (Bus Width = 16 Bits, Longword Transfer (Number of Bursts = 2), Access Wait for 1st Time = 2, Access Wait for 2nd Time and After = 1) (BW[1:0] = B'01, WW[2:0] = B'000, WR[3:0] = B'0010, SW[1:0] = B'00, HW[1:0] = B'00)

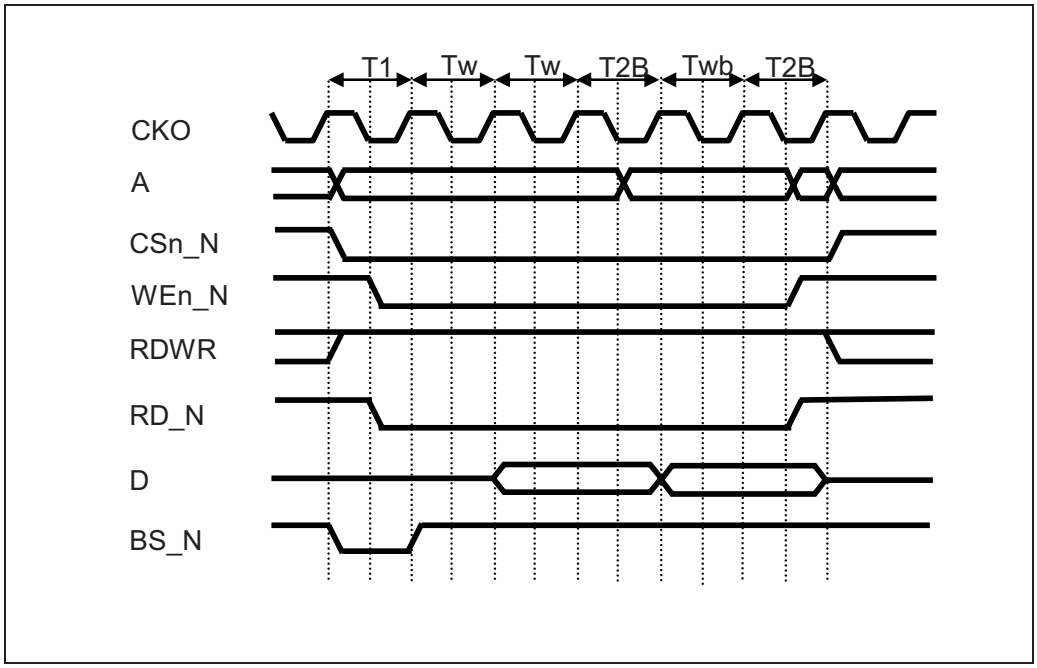


Figure 6.18 Page Mode Read for SRAM with Byte Selection (PMD = 1, BAS = 0) (Bus Width = 16 Bits, Longword Transfer (Number of Bursts = 2), Access Wait for 1st Time = 2, Access Wait for 2nd Time and After = 1) (BW[1:0] = B'01, WW[2:0] = B'000, WR[3:0] = B'0010, SW[1:0] = B'00, HW[1:0] = B'00)

6.5.7 Wait between Access Cycles

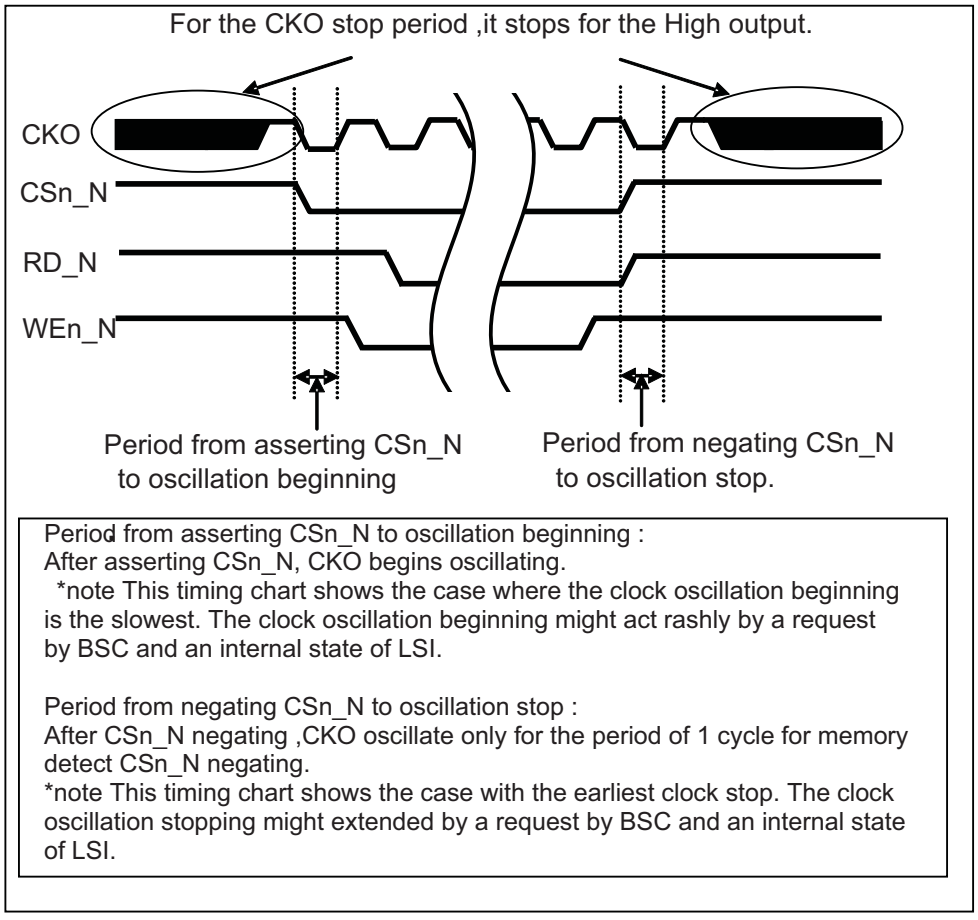
As the operating frequency of LSIs becomes higher, the off-operation of the data buffer often collides with the next data output when the data output from devices with slow access speed is completed. As a result of these collisions, the reliability of the device is low and malfunctions may occur. A function that avoids data collisions by inserting wait cycles between continuous access cycles has been newly added.

The number of wait cycles between access cycles can be set by the IWW, IWRWD, IWRWS, IWRRD, and IWRRS bits in CSnBCR. The conditions for inserting the wait cycles (idle cycles) between access cycles are shown below.

1. Continuous accesses are write-read or write-write
2. Continuous accesses are read-write for different spaces
3. Continuous accesses are read-write for the same space
4. Continuous accesses are read-read for different spaces
5. Continuous accesses are read-read for the same space

6.5.8 CKO automatic stop function in case where output is not needed.

The control of the selection of the output of CKO is added in each area. This control is controlled by CSnBCR.CKOSTP bit . When the asynchronization memory that doesn't need the CKO output is connected, the output of CKO is controlled by setting CSnBCR.CKOSTP to 1. The CKO output start and stop timing are shown.



Period from asserting CSn_N to oscillation beginning :
After asserting CSn_N, CKO begins oscillating.
*note This timing chart shows the case where the clock oscillation beginning is the slowest. The clock oscillation beginning might act rashly by a request by BSC and an internal state of LSI.

Period from negating CSn_N to oscillation stop :
After CSn_N negating ,CKO oscillate only for the period of 1 cycle for memory detect CSn_N negating.
*note This timing chart shows the case with the earliest clock stop. The clock oscillation stopping might extended by a request by BSC and an internal state of LSI.

Figure 6.19 CKO output start and stop timing

6.5.9 Burst Write mode.

Burst Write mode is used to access the memory in which the rapid access is possible and Burst Write mode function is provided. The write/read access timing without WAIT is shown in Figure 6.20.a, with WAIT is shown in Figure 6.20.b.The Write access timing with WWAIT Setting is shown in figure Figure 6.20.c. The Read access timing with RWAIT Setting is shown in figure Figure 6.20.d.

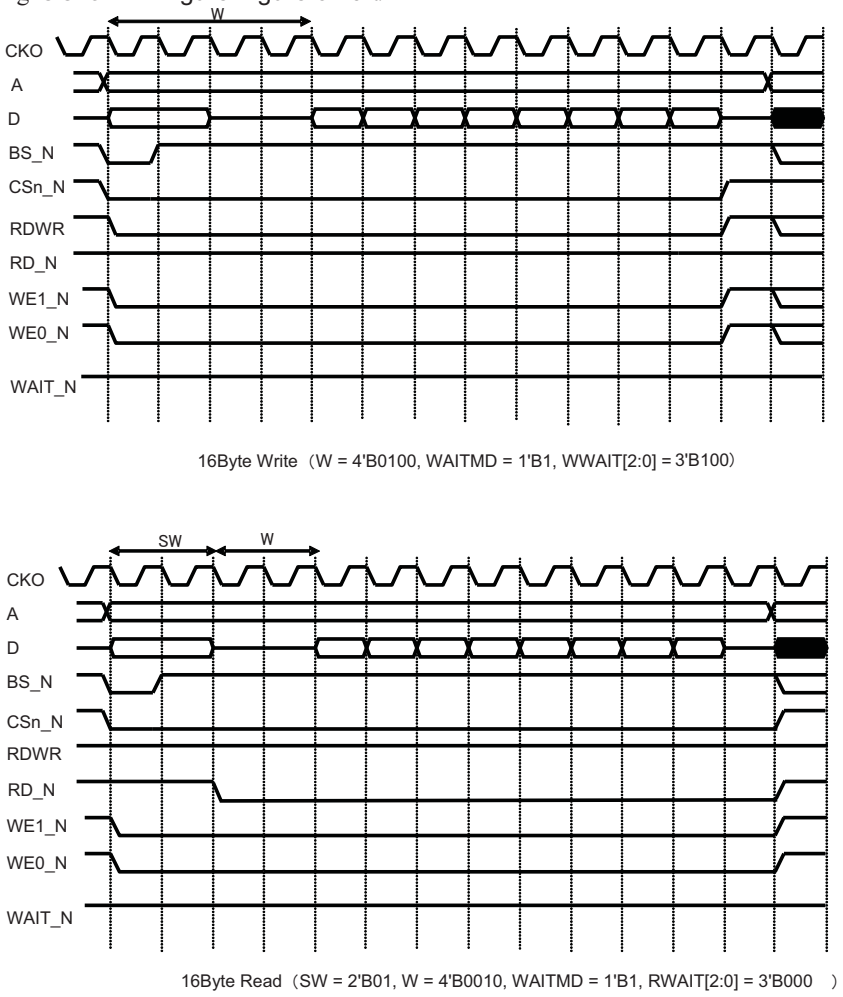
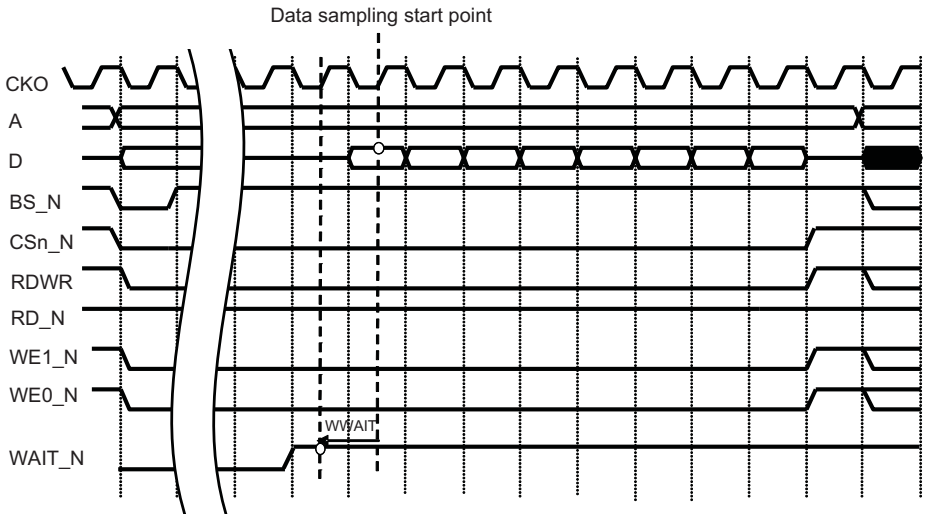
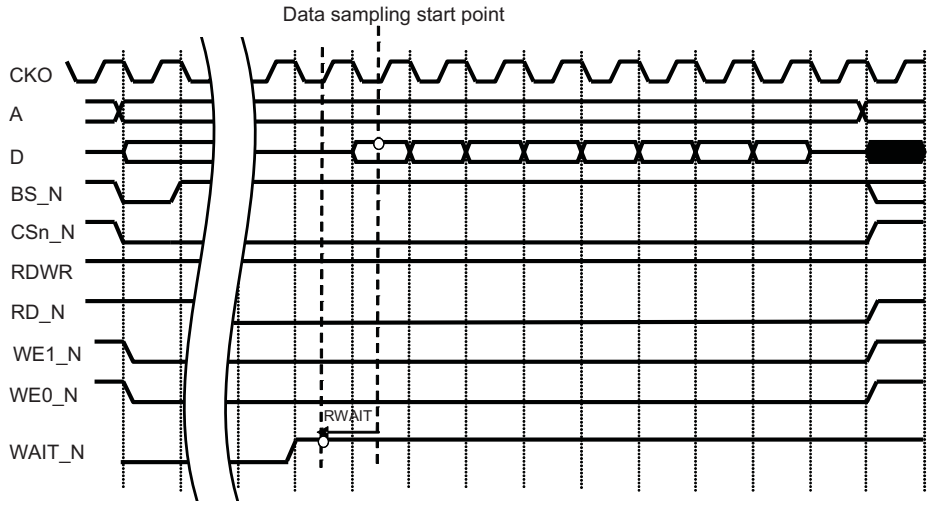


Figure 6.20.a Burst write/read timing (Without WAIT)



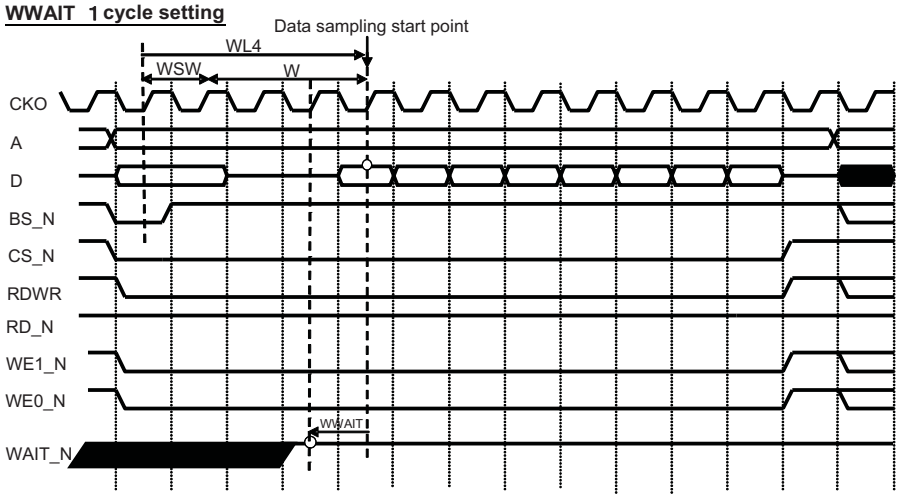
16Byte Write（WAITMD = 1'B1, WWAIT[2:0] = 3'B100）



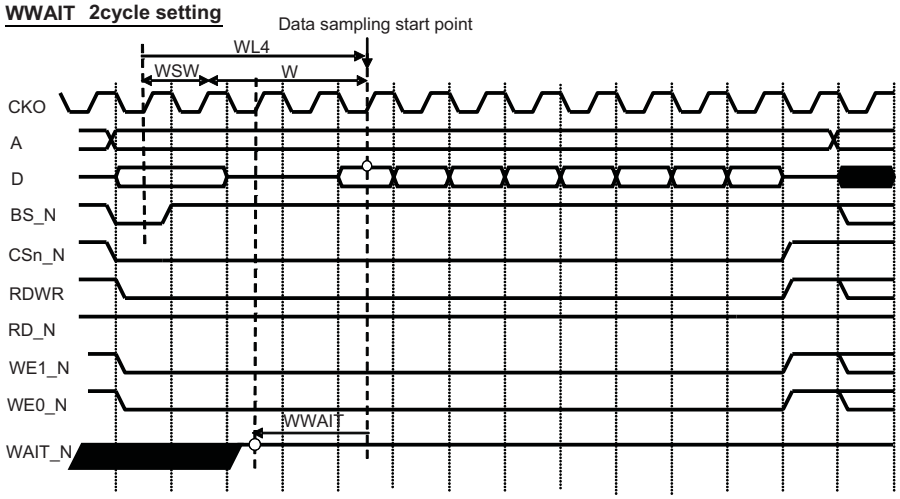
16Byte Read（WAITMD = 1'B1, RWAIT[2:0] = 3'B000）

（ADMUX= 1 'B1, BAS=1'B1, BROMMD[1:0]=2'B11, PH1RD=1'B1,HW[1:0]=2'B00,BSTMD[1:0]=2'B10,WM=1'B0）

Figure 6.20.b Burst write/read timing(With WAIT)



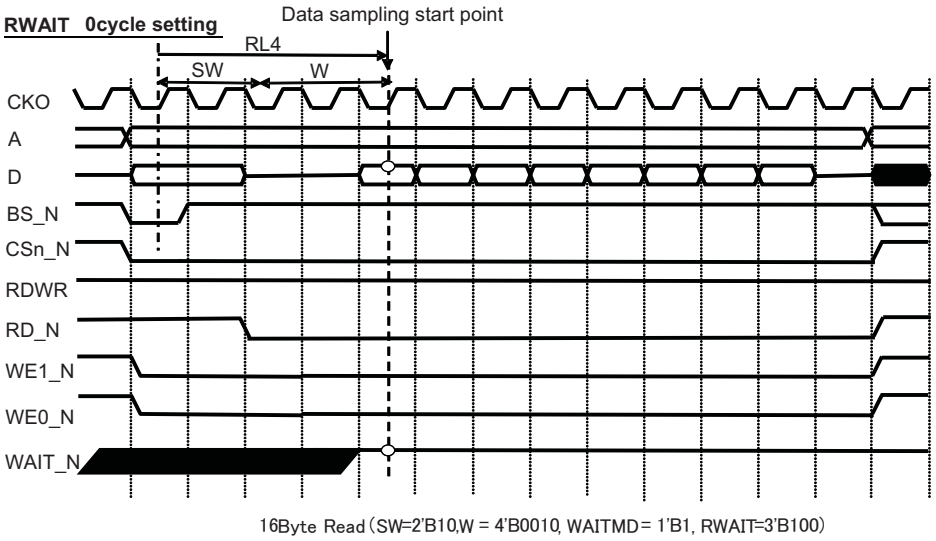
16Byte Write （WSHWEN = 1'B1, WSW = 2'b01,W = 4'B0011, WAITMD = 1'B1,WWAIT=3'B100）

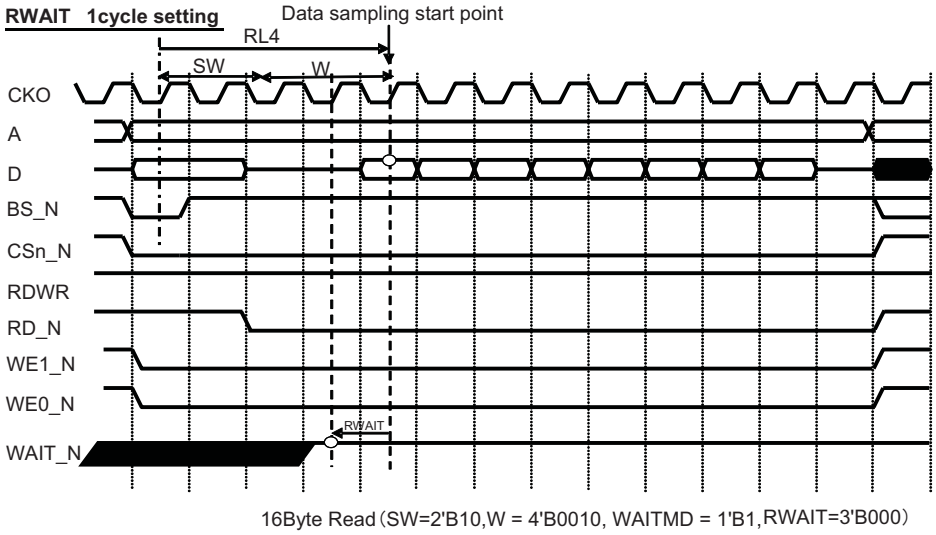


16Byte Write（WSHWEN = 1'B1, WSW = 2'b01,W = 4'B0011, WAITMD = 1'B1,WWAIT=3'B000）

（ADMUX＝１'B1, BAS=1'B1, BROMMD[1:0]=2'B11, PH1RD=1'B1,HW[1:0]=2'B00,BSTMD[1:0]＝2'B10,WM=1'B0 ）

Figure 6.20.c Burst write timing(WWAIT setting)





ADMUX＝１'B1, BAS=1'B1, BROMMD[1:0]=2'B11, PH1RD=1'B1,HW[1:0]=2'B00,BSTMD[1:0]＝2'B10,WM=1'B0 ）

Figure 6.20.c Burst read timing(RWAIT setting)

Table 6.14 : **Burst Write Register Setting**

Register Setting				WL	RL
WSHWEN	WSW[1:0]	SW[1:0]	W[1:0]		
1	10	11	0001	3*	4
1	11	11	0001	4	4
1	10	11	0010	4	5
1	10	11	0011	5	6
1	11	11	0010	5	5
1	10	11	0100	6	7
1	11	11	0100	7	7

Please do not change to the settings other than the following.

CMNCR.BROMMD = 2'b11, CMNCR.TYPE = 3'B001

CSnBCR.PH1RD = 1'B1

CSnWCR.BSTMD = 2'B10, CSnWCR.BAS = 1'B1, CSnWCR.ADMUX = 1'B1

CSnWCR.WM = 1'B0, CSnWCR.HW = 2'B00

Note: * If set WL=3 and use external WAIT, Please set CSnWCR2.WWAIT = 3'B000 or 3'B100.

6.6 Others

6.6.1 Reset

The BSC can be initialized completely only by a power-on reset. At a power-on reset, all signals are negated and output buffers are turned off immediately regardless of the bus cycle state. All control registers are initialized. When power supply is intercepted,excluding C5 area, control registers of the BSC are not initialized.

Some flash memories may specify a minimum time from reset cancel to the first access. To ensure this minimum time, the BSC supports a 7-bit counter (RBWTCNT). At a power-on reset, RBWTCNT is set to H'7F. After clearing a power-on reset, RBWTCNT is counted down synchronized with CKO and an external access will not be generated until RBWTCNT is counted up to H'00.

6.6.2 On-Chip Peripheral Module Access

To access an on-chip peripheral module register, two or more peripheral clock (Pϕ) cycles are required. Care must be taken in system design.

6.6.3 Releasing the External Bus

The external bus of this LSI is shared by the BSC and FLCTL of the AP block (see figure 6.19).

When the FLCTL requires access to the external bus, the FLCTL issues a request to the BSC, and the BSC performs arbitration. BSC access is kept waiting while there is a request from the FLCTL block.

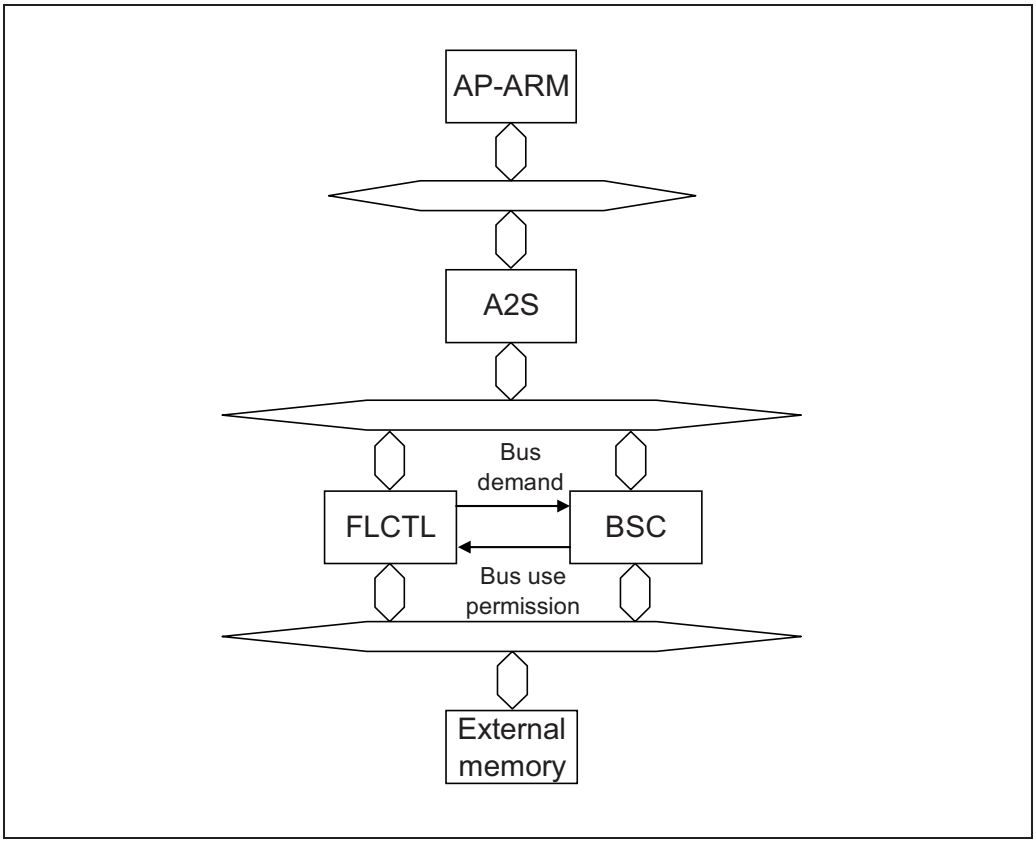


Figure 6.19 Relationship of Permissions and Bus Release Requests

6.6.4 Memory Protection Area Settings Registers and Handling of the Address Space

By setting BPTCR 00 to 31, this LSI can set write and read privileges for every 64 Mbits of the BSC area. Table 6.15 shows BPTCR 00 to 31 and the corresponding address space.

Table 6.14 Memory Protection Area Settings Registers and Handling of the Address Space

Space	Area Name	Settings Register Name	Start Address	End Address	Size

Area 0	Protection area 0	BPTCR 00	H'0000_0000	H'007F_FFFF	64 Mbits
	Protection area 1	BPTCR 01	H'0080_0000	H'00FF_FFFF	64 Mbits
	Protection area 2	BPTCR 02	H'0100_0000	H'017F_FFFF	64 Mbits
	Protection area 3	BPTCR 03	H'0180_0000	H'01FF_FFFF	64 Mbits
	Protection area 4	BPTCR 04	H'0200_0000	H'027F_FFFF	64 Mbits
	Protection area 5	BPTCR 05	H'0280_0000	H'02FF_FFFF	64 Mbits
	Protection area 6	BPTCR 06	H'0300_0000	H'037F_FFFF	64 Mbits
	Protection area 7	BPTCR 07	H'0380_0000	H'03FF_FFFF	64 Mbits
	Protection area 8	BPTCR 08	H'0400_0000	H'047F_FFFF	64 Mbits
	Protection area 9	BPTCR 09	H'0480_0000	H'04FF_FFFF	64 Mbits
	Protection area 10	BPTCR 10	H'0500_0000	H'057F_FFFF	64 Mbits
	Protection area 11	BPTCR 11	H'0580_0000	H'05FF_FFFF	64 Mbits
	Protection area 12	BPTCR 12	H'0600_0000	H'067F_FFFF	64 Mbits
	Protection area 13	BPTCR 13	H'0680_0000	H'06FF_FFFF	64 Mbits
	Protection area 14	BPTCR 14	H'0700_0000	H'077F_FFFF	64 Mbits
	Protection area 15	BPTCR 15	H'0780_0000	H'07FF_FFFF	64 Mbits
Area 2	Protection area 16	BPTCR 16	H'0800_0000	H'087F_FFFF	64 Mbits
	Protection area 17	BPTCR 17	H'0880_0000	H'08FF_FFFF	64 Mbits
	Protection area 18	BPTCR 18	H'0900_0000	H'097F_FFFF	64 Mbits
	Protection area 19	BPTCR 19	H'0980_0000	H'09FF_FFFF	64 Mbits
	Protection area 20	BPTCR 20	H'0A00_0000	H'0A7F_FFFF	64 Mbits
	Protection area 21	BPTCR 21	H'0A80_0000	H'0AFF_FFFF	64 Mbits
	Protection area 22	BPTCR 22	H'0B00_0000	H'0B7F_FFFF	64 Mbits
	Protection area 23	BPTCR 23	H'0B80_0000	H'0BFF_FFFF	64 Mbits
	Protection area 24	BPTCR 24	H'0C00_0000	H'0C7F_FFFF	64 Mbits
	Protection area 25	BPTCR 25	H'0C80_0000	H'0CFF_FFFF	64 Mbits
	Protection area 26	BPTCR 26	H'0D00_0000	H'0D7F_FFFF	64 Mbits
	Protection area 27	BPTCR 27	H'0D80_0000	H'0DFF_FFFF	64 Mbits
	Protection area 28	BPTCR 28	H'0E00_0000	H'0E7F_FFFF	64 Mbits
	Protection area 29	BPTCR 29	H'0E80_0000	H'0EFF_FFFF	64 Mbits
	Protection area 30	BPTCR 30	H'0F00_0000	H'0F7F_FFFF	64 Mbits
	Protection area 31	BPTCR 31	H'0F80_0000	H'0FFF_FFFF	64 Mbits

6.6.5 Wait Control Using External Pins

BSC uses the WAIT_N pins for wait control based on external pins. Figure 6.21 shows the control circuit from these pins to the BSC wait control block.

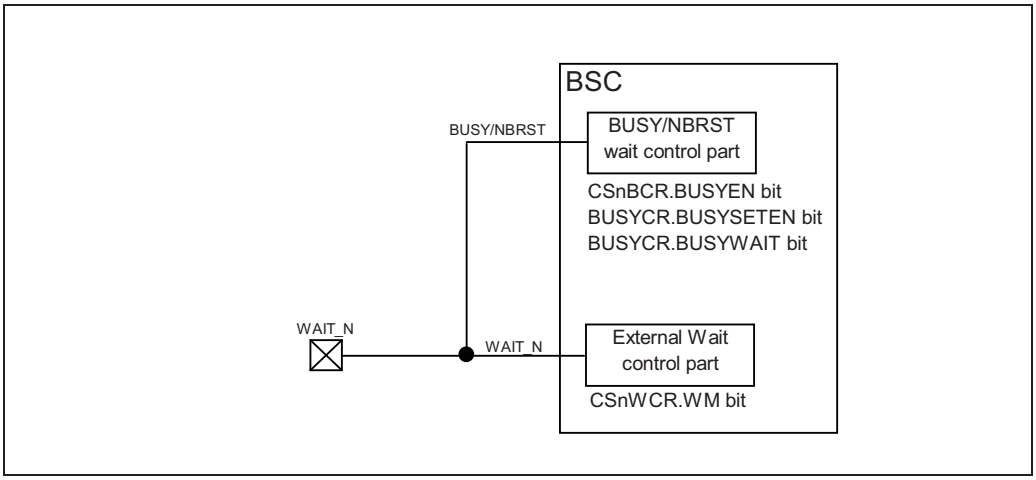


Figure 6.21 Wait Control Using External Pins

6.6.6 CKO Output, D-pin Input Control

The CKO pin and D pin of this LSI are controlled by the BSC bit and CPGA bit shown in table 16.6. These control bits must be set when clock asynchronous burst mode of the burst Rom interface is used.

Table 6.15: Relationship between Memory Protection Area Settings Registers and Address Space

Bit Name	Settings When Clock Asynchronous Burst Mode of the Burst Rom Interface Used
BSC.CSnBCR.PH1RD	Must be set to 1.
BSC.CMNCR.BROMMD0	Must be set to 1.
BSC.CMNCR.BROMMD1	Must be set to 1.
BSC.CMNCR.CKODSTP	For low power consumption, set to 1.
BSC. CMNCR.CKOSTP	Must be set to 0.
BSC.BROMTIMCR.CCNT[3:0]	Renesas will provide this information separately.
BSC.BROMTIMCR.DCNT[3:0]	Renesas will provide this information separately.
CPGA.PLLC1CR.CKODIVSTP	For low power consumption, set to 1.

Figure 6.22 shows the concept of CKO pin control and D pin control, both of which are controlled by the bits listed in the above table.

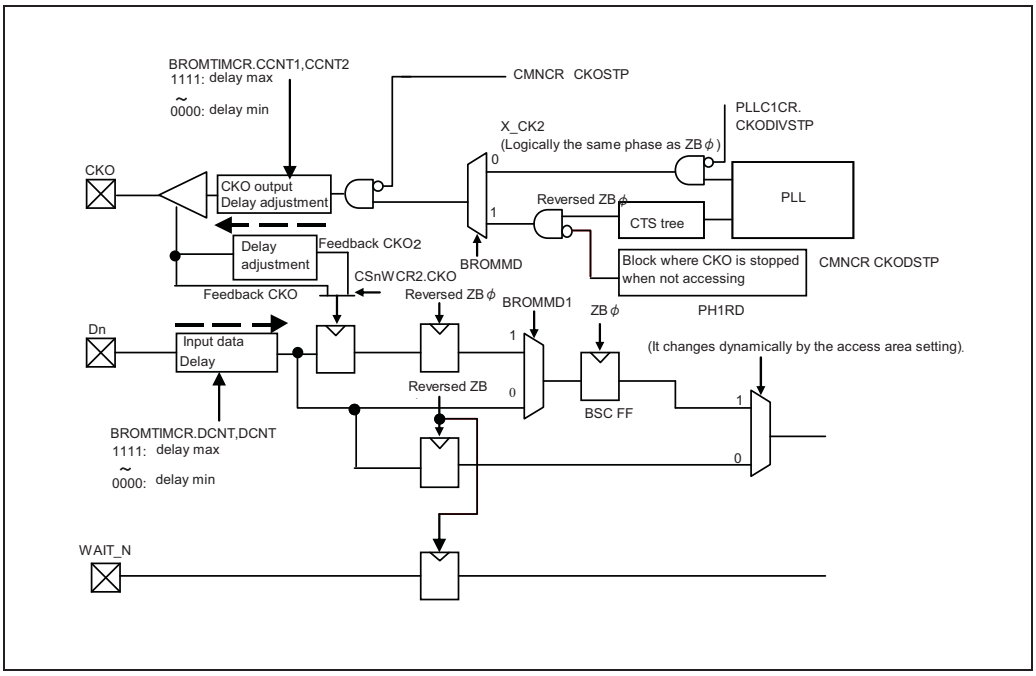


Figure 6.22 Concept of CKO Pin Control and C Pin Control

Section 7. Bus State Controller for SDRAM (SBSC)

The bus state controller for SDRAM (SBSC) outputs control signals for SDRAM that is connected to the external address space. The SBSC functions enable this LSI to connect directly with SDRAM.

7.1 Features

The SBSC has the following features:

- Module configuration
  The SBSC controls the LP bus, and has one chip select signal.

- External address space
  The SBSC has a maximum 4 Gbits of external address space.
  The SBSC controls the one area of LPCSA.

- Operational mode
  SBSC has two operational modes (DDR600, DDR400)
  (DDR600 mode and DDR400 mode are selected with CPGA.FRQCRD.ZB3D2SEL bit)
  DDR600 mode
  Frequency : 20 to 300 MHz (ZBCLK3)
  Bus Width : 32 bits
  RL/WL/BL : 5/2/4
  DDR400 mode
  Frequency : 20 to 200 MHz(ZBCLK3)
  Bus Width : 32 bits / 64 bits
  RL/WL/BL : 3/1/4

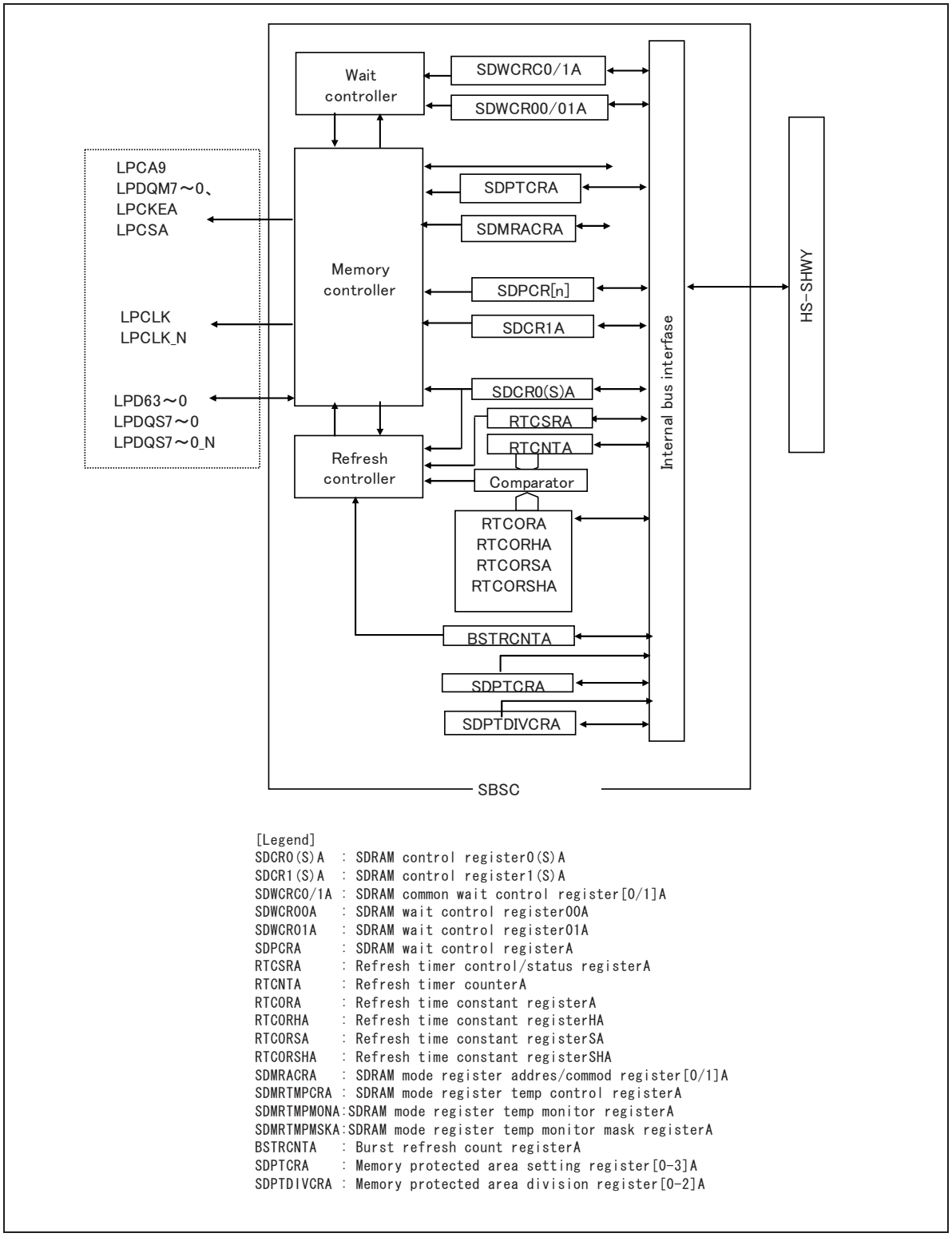
- Controllable insertion of wait cycles according to the LPDDR2-S4 specifications

- LPDDR2-S4, interface
  Multiplexed output for command/row address/column address
  High-speed access by bank-active mode.
  Supports auto-refresh and self-refresh.
  Supports a low-power function.

- Memory protection function
  Can set the privilege to write to and read from the AP module or BB module (ACMFI).
  The area is divided into four, and a minimum unit of each area is 1 Mbits.

- Refresh function
  Supports auto-refresh and self-refresh.
  Specifies the refresh interval using the refresh counter and clock selection.
  Can execute concentrated refresh by specifying the refresh count (1, 2, 4, 6, or 8).
  Has a function to automatically switch the refresh rate based on the automatic determination of the temperature sensor in LPDDR-S4 MR#4 register.

Figure 7.1 shows a block diagram of the SBSC.



[Legend]
SDCR0(S)A : SDRAM control register0(S)A
SDCR1(S)A : SDRAM control register1(S)A
SDWCRC0/1A : SDRAM common wait control register[0/1]A
SDWCR00A : SDRAM wait control register00A
SDWCR01A : SDRAM wait control register01A
SDPCRA : SDRAM wait control registerA
RTCSRA : Refresh timer control/status registerA
RTCNTA : Refresh timer counterA
RTCORA : Refresh time constant registerA
RTCORHA : Refresh time constant registerHA
RTCORSA : Refresh time constant registerSA
RTCORSHA : Refresh time constant registerSHA
SDMRACRA : SDRAM mode register addres/commod register[0/1]A
SDMRTMPCRA : SDRAM mode register temp control registerA
SDMRTMPMONA:SDRAM mode register temp monitor registerA
SDMRTMPMSKA:SDRAM mode register temp monitor mask registerA
BSTRCNTA : Burst refresh count registerA
SDPTCRA : Memory protected area setting register[0-3]A
SDPTDIVCRA : Memory protected area division register[0-2]A

Figure 7.1 Block Diagram of SBSC

7.2 Input/Output Pins

Table 7.1 lists the SBSC pin configurations.

The SBSC controls the LP bus.

Table 7.1 SBSC Pin Configuration (LP Bus)

Name	Function	I/O	Description
LPCA9 to LPCA0	Command/Address bus	Output	Command / Address output
LPD63 to LPD0	Data bus	I/O	32-bit or 64-bit bidirectional bus
LPCSA	Chip select	Output	Chip select signal for connection to memory in DRAM area 0
LPDQM7	UUU-side data mask	Output	Byte-selection signal corresponding to D63 to D55 of LPDDR2-S4 Only 64-bit bus is used
LPDQM6	UUL-side data mask	Output	Byte-selection signal corresponding to D54 to D48 of LPDDR2-S4 Only 64-bit bus is used
LPDQM5	ULU-side data mask	Output	Byte-selection signal corresponding to D47 to D40 of LPDDR2-S4 Only 64-bit bus is used
LPDQM4	ULL-side data mask	Output	Byte-selection signal corresponding to D39 to D32 of LPDDR2-S4 Only 64-bit bus is used
LPDQM3	LUU-side data mask	Output	Byte-selection signal corresponding to D31 to D24 of LPDDR2-S4.
LPDQM2	LUL-side data mask	Output	Byte-selection signal corresponding to D23 to D16 of LPDDR2-S4.
LPDQM1	LLU-side data mask	Output	Byte-selection signal corresponding to D15 to D8 of LPDDR2-S4.
LPDQM0	LLL-side data mask	Output	Byte-selection signal corresponding to D7 to D0 of LPDDR2-S4.
LPCKEA	Clock enable	Output	SDRAM clock enable signal. Connected to the CKE pin of SDRAM.
LPCLK	Synchronous clock	Output	Synchronous clock output
LPCLK_N	Synchronous clock	Output	Inverted LPCLK clock output for LPDDR2-S4
LPDQS7/ LPDQS7_N	Data strobe	I/O	Data strobe signal corresponding to D63 to D56 of LPDDR2-S4 Only 64-bit bus is used
LPDQS6/ LPDQS6_N	Data strobe	I/O	Data strobe signal corresponding to D55 to D48 of LPDDR2-S4 Only 64-bit bus is used

Name	Function	I/O	Description
LPDQS5/ LPDQS5_N	Data strobe	I/O	Data strobe signal corresponding to D47 to D40 of LPDDR2-S4 Only 64-bit bus is used
LPDQS4/ LPDQS4_N	Data strobe	I/O	Data strobe signal corresponding to D39 to D32 of LPDDR2-S4 Only 64-bit bus is used
LPDQS3/ LPDQS3_N	Data strobe	I/O	Data strobe signal corresponding to D31 to D24 of LPDDR2-S4
LPDQS2/ LPDQS2_N	Data strobe	I/O	Data strobe signal corresponding to D23 to D16 of LPDDR2-S4
LPDQS1/ LPDQS1_N	Data strobe	I/O	Data strobe signal corresponding to D15 to D8 of LPDDR2-S4
LPDQS0/ LPDQS0_N	Data strobe	I/O	Data strobe signal corresponding to D7 to D0 of LPDDR2-S4

7.3 Area Overview

7.3.1 Address Map

This LSI has 4 Gbits for the external address space only for LPDDR2-S4. The external address space is divided into up to eight partial spaces according to the maximum size of the connected memory. Among these partial spaces, the SBSC controls DRAM area 0.

Tables 7.2 show the address maps of the external address space.

Table 7.2 Address Map

Address	Area	Memory to be Connected	Capacity
H'4000 0000 to H'5FFF FFFF	DRAM area 0 (SBSC)	LPDDR2-SDRAM(S4 only)	4-Gbit
-	DRAM area 1 (SBSC)	Not support.	-

7.3.2 Memory Bus Width

The memory bus width of this LSI can be set as 32 bits or 64 bits by the SZ bit in the SDRAM control registers 0A (SDCR0A).

7.3.3 Data Alignment

This LSI supports only the little endian method for data alignment.

7.4 Register Descriptions of SBSC1

Table 7.3 shows the SBSC1 register configuration. Table 7.4 shows the register states in each operating mode. Do not access DRAM area 0 or DRAM area 1 until the memory interface settings have been made.

Table 7.3 SBSC1 Register Configuration

Register	Abbreviation	R/W	Address	Access Size
SDRAM control register 0A	SDCR0A	R/W	H'FE40 0008	32
SDRAM control register 1A	SDCR1A	R/W	H'FE40 000C	32
SDRAM control register 0SA	SDCR0SA	R/W	H'FE40 0018	32
SDRAM Common wait control register0A	SDWCRC0A	R/W	H'FE40 0040	32
SDRAM Common wait control register1A	SDWCRC1A	R/W	H'FE40 0044	32
SDRAM Common wait control register2A	SDWCRC2A	R/W	H'FE40 0064	32
SDRAM wait control register00A	SDWCR00A	R/W	H'FE40 0048	32
SDRAM wait control register01A	SDWCR01A	R/W	H'FE40 004C	32
Power-down control register 0A	SDPDCR0A	R/W	H'FE40 0058	32
Extend bank mode registerA	EBMCRA	R/W	H'FE40 0014	32
SDRAM pin control register A	SDPCRA	R/W	H'FE40 0010	32
Refresh timer control/status register A	RTCSRA	R/W	H'FE40 0020	32*1
Refresh timer counter A	RTCNTA	R/W	H'FE40 0024	32*1
Refresh time constant register A	RTCORA	R/W	H'FE40 0028	32*1
Refresh time constant register HA	RTCORHA	R/W	H'FE40 002C	32*1
Refresh time constant registerSA	RTCORSA	R/W	H'FE40 0030	32*1
Refresh time constant registerSHA	RTCORSHA	R/W	H'FE40 0034	32*1
Refresh count register A	RFCRA	R/W	H'FE40 0038	32*1
Burst refresh count register A	BSTRCNTA	R/W	H'FE40 003C	32
SDRAM mode register A*[2]	SDMRA	R/W	H'FE5x xxxx	8/32
SDRAM mode register addres/commod register0A	SDMRACR0A	R/W	H'FE40 0084	32
SDRAM mode register addres/commod register1A	SDMRACR1A	R/W	H'FE40 0088	32
SDRAM mode register temp control registerA	SDMRTMPCRA	R/W	H'FE40 008C	32
SDRAM mode register temp monitor registerA	SDMRTMPMONA	R/W	H'FE40 0090	32
SDRAM mode register temp monitor mask registerA	SDMRTMPMSKA	R/W	H'FE40 0094	32
SDRAM General-purpose down counter down counterA	SDGENCNTA	R/W	H'FE40 009C	32
SDRAM drivability control register 0A	SDDRVCR0A	R/W	H'FE40 00B4	32
SDRAM drivability control register 1A	SDDRVCR1A	R/W	H'FE40 00B8	32
Memory protected area division register0A	SDPTDIVCR0A	R/W	H'FE40 00F0	32
Memory protected area division register1A	SDPTDIVCR1A	R/W	H'FE40 00F4	32
Memory protected area division register2A	SDPTDIVCR2A	R/W	H'FE40 00F8	32
Memory protected area setting register0A	SDPTCR0A	R/W	H'FE40 0100	32
Memory protected area setting register1A	SDPTCR1A	R/W	H'FE40 0104	32
Memory protected area setting register2A	SDPTCR2A	R/W	H'FE40 0108	32

Register	Abbreviation	R/W	Address	Access Size
Memory protected area setting register3A	SDPTCR3A	R/W	H'FE40 010C	32
DLL control register0A	DLLCNT0A	R/W	H'FE40 0354	32
SBSC monitor register0A	SBSCMON0A	R	H'FE40 0358	32

Notes: 1. To prevent the erroneous writing, 32-bit write operations only are performed when the upper 16 bits of the write data are H'A55A. Otherwise, write operations are not performed. The upper 16 bits of the data are read as H'0000.

2. The entity of this register is in SDRAM. Data is written to the register in the SDRAM by accessing the register space for it. For details, refer to section 7.6.2 (3),LPDDR2-S4 internal register access function.

Table 7.4 Register States in Each Operating Mode

Register Abbreviation	Power-On Reset	System Reset	A4S Area Power Cutoff	C5 Area Power Cutoff
SDCR0A	Initialized	Retained	Retained	Initialized
SDCR1A	Initialized	Retained	Retained	Initialized
SDCR0SA	Initialized	Retained	Retained	Initialized
SDCR1SA	Initialized	Retained	Retained	Initialized
SDWCRC0A	Initialized	Retained	Retained	Initialized
SDWCRC1A	Initialized	Retained	Retained	Initialized
SDWCR00A	Initialized	Retained	Retained	Initialized
SDWCR01A	Initialized	Retained	Retained	Initialized
SDWCR10A	Initialized	Retained	Retained	Initialized
SDWCR11A	Initialized	Retained	Retained	Initialized
SDPDCR0A	Initialized	Retained	Retained	Initialized
EBMCRA	Initialized	Retained	Retained	Initialized
SDPCRA	Initialized	Retained	Retained	Initialized
RTCSRA	Initialized	Retained *1	Retained *1	Initialized
RTCNTA	Initialized	Initialized	Initialized	Initialized
RTCORA	Initialized	Retained	Retained	Initialized
RTCORHA	Initialized	Retained	Retained	Initialized
RTCORSA	Initialized	Retained	Retained	Initialized
RTCORSHA	Initialized	Retained	Retained	Initialized
RFCRA	Initialized	Initialized	Initialized	Initialized
BSTRCNTA	Initialized	Retained	Retained	Initialized
SDMRA	-	-	-	-
SDMRACR0A	Initialized	Retained	Retained	Initialized
SDMRACR1A	Initialized	Retained	Retained	Initialized
SDMRTMPCRA	Initialized	Retained	Retained	Initialized
SDMRTMPMONA	Initialized	Retained	Retained	Initialized
SDMRTMPMSKA	Initialized	Retained	Retained	Initialized
SDGENCNTA	Initialized	Initialized	Initialized	Initialized
SDDRVCR0A	Initialized	Retained	Retained	Initialized
SDDRVCR1A	Initialized	Retained	Retained	Initialized
SDPTDIVCR0 to 2A	Initialized	Retained	Retained	Initialized
SDPTCR0 to 3A	Initialized	Retained	Retained	Initialized
DLLCNT0A	Initialized	Retained	Retained	Initialized
SBSCMON0A	Initialized	Initialized	Initialized	Initialized

Notes: 1. Bits OVF and CMF in RTCSRA are not retained.

7.4.1 SDRAM Control Register 0 A (SDCR0A)

SDCR0A specifies the method to refresh and access SDRAM connected to DRAM area 0, and the types and bus width of SDRAM to be connected.

SDCR0A is initialized to H'B0CA0109 by a power-on reset, but is not initialized and retains the contents in standby mode. Bits other than PDSELF, SRF_PRE, RFSH, RMODE, PDOWN, and DEEP should be set before accessing SDRAM connected to DRAM area 0, and should not be modified during SDRAM access. When writing to the PDSELF, SRF_PRE, RFSH, RMODE, PDOWN, and DEEP bits, the same value should be written to the other bits so that they remain unchanged.

bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	SDSZ[1:0]		PDSELF	PLLCNT	–	–	MEMTYPE[1:0]		–	–	BL	SRF_PRE	SZ[1:0]	
Initial value	1	0	1	1	0	0	0	0	1	1	0	0	1	0	1	0
R/W:	R	R	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W	R/W	R/W

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PDOWN1	PDOWN0	DEEP	–	RFSH	RMODE	–	BACTV	–	BANK	ROW[2:0]			–	COL[1:0]	
Initial value	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	1
R/W:	R/W	R/W	R/W	R	R/W	R/W	R	R/W	R	R/W	R/W	R/W	R/W	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
30	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
29, 28	—	11	R	Reserved This bit is always read as 1. The write value should always be 1.
27	PDSELF	0	R/W	Selects whether to transit to self-refresh mode when the ZBCK3 frequency has been changed and SBSC power (A4S) is turned off. 0: Does not enter self-refresh mode 1: Enters self-refresh mode Note: The DEEP bit in SDCR0A must be cleared to 0 when this bit is set to 1. Even though partial refreshing has been specified when setting MR10 of the SDRAM, care is required for using this bit because memory contents cannot be saved in some areas. When a frequency is changed, this bit must be set to 1 in order to avoid refresh shortage.
26	PLLCNT	0	R/W	DRAM control at PLLC1 off period is specified. 0:SDRAM in the SBSC1 area in off PLLC1 continues an auto refreshing. 1:SDRAM in the SBSC1 area in off PLLC1 is assumed to be self-refresh. For details of settings, refer refer to "7.6.2(5) (f) Control of Automatic Transition to Self-Refresh Mode while PLLC1 is Off"

Bit	Bit Name	Initial Value	R/W	Description
25 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23,22	MEMTYPE	11	R/W	Memory Type Select 11:LPDDR2-S4 is connected to DRAM area 0. Others: Setting prohibited
21 to 20	—	All 0	R	Reserved This bit is always read as 0. The write value should always be 0.
19	BL	1	R/W	Burst Length Select When selecting the burst length of 4, the BACTV bit should be set to 1 to select bank active mode. 1: Burst length is 4 for LPDDR2-S4 access Others: Setting prohibited
18	SRF_PRE	0	R/W	All Bank Precharge Select Selects whether to issue the all-bank precharge command (PALL) before the burst refreshing that is performed on clearing of self-refresh mode. This bit is valid only when the SRFCNT bits in the BSTRCNTA register are set to a value greater than or equal to 1. 0: PALL is not issued before the burst refreshing is started 1: PALL is issued before the burst refreshing is started
17 to 16	SZ	10	R/W	Data Bus Width Specifies the data bus width of SDRAM. 01: 32 bits 10:64 bits Others: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Description
15, 14	PDOWN1 PDOWN0	All 0	R/W	These bits select the power-down mode. When the PDOWNSEL bit in SDPDCR0A is 1, the setting of these bits is compared with the power-down mode set by the PDOWN bits in SDCRA1, and the power-down mode with the smaller access latency is selected. 00: Normal operation 10: Power-down mode 1 If there is no access to the SBSC during the ZB3ϕ cycles specified by the PDWAIT bits in SDPDCR0A, the LPCKEA and LPCKEB pins are pulled to low and the SDRAM is placed in power-down mode. 01: Power-down mode 2 If there is no access to the SBSC during the ZB3ϕ cycles specified by the PDWAIT bits in SDPDCR0A, the LPCKEA and LPCKEB pins are pulled to low and the SDRAM is placed in power-down mode. At this time, the clock to the internal bus interface block in the SBSC is stopped. If there is a new access to the SBSC, a latency of one ZSϕ clock cycle is added compared to power-down mode 1 to start clock supply to the internal bus interface block. 11: Power-down mode 3 If there is no access to the SBSC during the ZB3ϕ cycles specified by the PDWAIT bits in SDPDCR0A, the self-refresh command is issued for the SDRAM and the SDRAM is placed in self-refresh mode. At this time, the clock (ZSϕ) to the internal bus interface block in the SBSC and the SBSC operation clock (ZB3ϕ) are stopped. If there is a new access to the SBSC, a latency of three ZSϕ clock cycles is added compared to power-down mode 1 to start clock supply.

Bit	Bit Name	Initial Value	R/W	Description
13	DEEP	0	R/W	Deep Power-Down Mode This bit is valid only for low-power SDRAM. If the RFSH and RMODE bits in SDCR0A are both set to 1 when the DEEPSEL0 bit in SDPDCR0A is 0 and this bit is set to 1, the deep power-down entry command is issued for the low-power SDRAM connected to DRAM area 0 and the low-power SDRAM enters deep power-down mode. When the DEEPSEL0 bit in SDPDCR0A is 1, whether to enter self-refresh mode or deep power-down mode is determined by ANDing this bit and the DEEP bit in SDCRA0S. Transition to self-refresh mode or deep power-down mode occurs at the timing specified when the RFSH bit in SDCR0 A is 1 and the RMODE bit in SDCR0(S) A is 1. The target mode is determined by the following setting. • When the DEEPSEL0 bit in SDPDCR0A is 0 0: DRAM area 0 enters self-refresh mode 1: DRAM area 0 enters deep power-down mode When the DEEPSEL0 bit in SDPDCR0A is 1 SDCR0A DEEP / SDCRA0S DEEP / Description 0 / 0 / DRAM area 0 enters self-refresh mode 1 / 0 / DRAM area 0 enters self-refresh mode 0 / 1 / DRAM area 0 enters self-refresh mode 1 / 1 / DRAM area 0 enters deep power-down mode
12	-	0	R	Reserved This bit is always read as 0. The write value should always be 0.
11	RFSH	0	R/W	Refresh Control Specifies whether or not the refresh operation of SDRAM is performed. 0: No refresh 1: Refresh

Bit	Bit Name	Initial Value	R/W	Description
10	RMODE	0	R/W	Refresh Mode Specifies whether to perform auto-refresh or self-refresh for the low-power SDRAM connected to DRAM area 0 when the RFSH bit in SDCRA0 is 1. When the RFSH bit is 1 and this bit is 1, self-refresh starts immediately. When the RFSH bit is 1 and this bit is 0, auto-refresh starts according to the settings in RTCSRA, RTCNTA, and RTCORA. When the RMODESEL0 bit in SDPDCR0A is 0, auto-refresh or self-refresh is selected by only this bit. However, when the RMODESEL0 bit in SDPDCR0A is 1, auto-refresh or self-refresh is determined by ANDing this bit and the RMODE bit in SDCRA0S. • When the RMODESEL0 bit in SDPDCR0A is 0 0: Auto-refresh is performed 1: Self-refresh is performed • When the RMODESEL0 bit in SDPDCR0A is 1 SDCR0A .RMODE / SDCR0SA .RMODE / Description 0 / 0 / DRAM area 0 enters auto-refresh mode 1 / 0 / DRAM area 0 enters auto-refresh mode 0 / 1 / DRAM area 0 enters auto-refresh mode 1 / 1 / DRAM area 0 enters self-refresh mode
9	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
8	BACTV	1	R/W	Bank Active Mode Specifies whether to access in auto-precharge mode (using READA and WRITA commands) or in bank active mode (using READ and WRIT commands). 0: Auto-precharge mode (using READA and WRITA commands) 1: Bank active mode (using READ and WRIT commands)
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6	BANK	0	R/W	Number of Bits of Bank Address These bits specify the number of bits of bank address for DRAM area 0. 0: 2 bits (4-banks) 1: 3 bits (8-banks)

Bit	Bit Name	Initial Value	R/W	Description
5 to 3	ROW[2:0]	011	R/W	Number of Bits of Row Address These bits specify the number of bits of row address for DRAM area 0. 000: 11 bits 001: 12 bits 010: 13 bits 011: 14 bits 100: 15 bits Others: Setting prohibited
2	-	0	R	Reserved This bit is always read as 0. The write value should always be 0.
1, 0	COL[1:0]	00	R/W	Number of Bits of Column Address These bits specify the number of bits of column address for DRAM area 0. 00: 8 bits 01: 9 bits 10: 10 bits 11: Setting prohibited

7.4.2 SDRAM Control Register 1 A (SDCR1A)

SDCR1A specifies the method to refresh and access SDRAM connected to DRAM area 0, and the types and bus width of SDRAM to be connected.

SDCR1A is initialized to H'00020409 by a power-on reset, but is not initialized and retains the contents in standby mode.

bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PDOWN1	PDOWN0	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value:	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	1

Bit	Bit Name	Initial Value	R/W	Description
31 to 18	—	All 0	R	Reserved This bit is always read as 1. The write value should always be 1.
17	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
16	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
15, 14	PDOWN1 PDOWN0	All 0	R/W	These bits select the power-down mode. These bits are valid only when the PDOWNSEL bit in SDPDCR0A is 1. When the PDOWNSEL bit in SDPDCR0A is 1, the setting of these bits is compared with the power-down mode set by the PDOWN bits in SDCR0A, and the power-down mode with the smaller access latency is selected. 00: Normal operation 10: Power-down mode 1 01: Power-down mode 2 11: Power-down mode 3 Note:The latency order is as follows: Normal operation < Power-down mode 1 < Power-down mode 2 < Power-down mode 3
13 to 11	—	All 0	R	Reserved This bit is always read as 0. The write value should always be 0.
10	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
9 to 4	—	All 0	R	Reserved This bit is always read as 0. The write value should always be 0.
3	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
2 ,1	—	All 0	R	Reserved This bit is always read as 0. The write value should always be 0.
2	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

7.4.3 SDRAM Control Register 0S A (SDCR0SA)

SDCR0SA specifies power-down control for the SDRAM connected to DRAM area 0. SDCR0SA is initialized to H'0000 0000 by a power-on reset, but is not initialized and retains the contents in standby mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	DEEP	—	—	RMODE	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R	R	R/W	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13	DEEP	0	R/W	Deep Power-Down Mode This bit is valid only when the DEEPSEL0 bit in SDPDCR0A is 1. When the DEEPSEL0 bit in SDPDCR0A is 1, whether DRAM area 0 enters self-refresh mode or deep power-down mode is determined by ANDing this bit and the DEEP bit in SDCRA0. For details about transition to self-refresh mode or deep power-down mode, see the bit description for the DEEP bit in SDCRA0. • When the DEEPSEL0 bit in SDPDCR0A is 0 0: Invalid setting 1: Invalid setting When the DEEPSEL0 bit in SDPDCR0A is 1 SDCRA0. DEEP / SDCRA0S DEEP / Description 0 / 0 / DRAM area 0 enters self-refresh mode 1 / 0 / DRAM area 0 enters self-refresh mode 0 / 1 / DRAM area 0 enters self-refresh mode 1 / 1 / DRAM area 0 enters deep power-down mode

Bit	Bit Name	Initial Value	R/W	Description
12, 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10	RMODE	0	R/W	Refresh Mode This bit is valid only when the RMODESEL0 bit in SDPDCR0A is 1. When the RMODESEL0 bit in SDPDCR0A is 1, auto-refresh or self-refresh is determined for the SDRAM connected to DRAM area 0 by ANDing this bit and the RMODE bit in SDCRA0. • When the RMODESEL0 bit in SDPDCR0A is 0 0: Invalid setting 1: Invalid setting When the RMODESEL0 bit in SDPDCR0A is 1 SDCRA1. SDCRA1S. RMODE RMODE Description 0 0 DRAM area 0 enters auto-refresh mode 1 0 DRAM area 0 enters auto-refresh mode 0 1 DRAM area 0 enters auto-refresh mode 1 1 DRAM area 0 enters self-refresh mode
9 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

7.4.4 SDRAM Common Wait Control Register C0A(SDWCRC0A)

SDWCRC0A specifies various wait cycles for SDRAM access. Set SDWCRC0A before accessing SDRAM.SDWCRC0A is initialized to H'20562111 by a power-on reset, but is not initialized and retains the contents in standby mode. The bits should be set before accessing SDRAM, and should not be modified during SDRAM access.

bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	RL[2:0]			–	–	WL[1:0]		–	TWTR[2:0]			–	TRTW[2:0]		
Initial value	0	0	1	0	0	0	0	0	0	1	0	1	0	1	1	0
R/W:	R	R/W	R/W	R/W	R	R	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	TMRW[1:0]			–	–	TMRR[1:0]		–	–	TCKE[1:0]		–	TCKESR[2:0]		
Initial value	0	0	1	0	0	0	0	1	0	0	0	1	0	0	0	1
R/W:	R	R/W	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	-	0	R	Reserved This bit is always read as 0. The write value should always be 0.
30 to 28	RL[2:0]	010	R/W	RL(Read laytency) 010:3cycles 100:5cycles Other than aboe: Setting prohibited
27 to 26	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25, 24	WL[1:0]	All 0	R/W	WL (Write laytency) 00: 1 cycle 01: 2 cycles Other than above: Setting prohibited
23	-	0	R	Reserved This bit is always read as 0. The write value should always be 0.
22 to 20	TWTR[2:0]	101	R/W	tWTR , Write to Read Time These bits specify the minimum number of cycles from issuing of an WRIT(A) command to to issuing of the READ(A) command. The specification of cycle number becomes this bit setting value +1. 000: 1 cycle 001: 2 cycles : 111: 8 cycles

Bit	Bit Name	Initial Value	R/W	Description
19	-	0	R	Reserved This bit is always read as 0. The write value should always be 0.
18 to 16	TRTW[2:0]	110	R/W	tRTW , Read to Write Time These bits specify the minimum number of cycles from issuing of an READ(A) command to to issuing of the WRIT(A) commond. The specification of cycle number becomes this bit setting value +1. 000: 1 cycle 001: 2 cycles : 111: 8 cycles
15	-	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14 to 12	TMRW[2:0]	010	R/W	tMRW These bits specify the minimum number of cycles from issuing of an MRW(Mode Register Write) command to to issuing of the any command. 000: 1 cycle 001: 2 cycles : 111: 8 cycles
11, 10	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9, 8	TMRR[2:0]	01	R/W	tMRR These bits specify the minimum number of cycles from issuing of an MRR(Mode Register Read) command to to issuing of the any command. 00: 1 cycle 01: 2 cycles 10: 3 cycles 11: 4 cycles
7, 6	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5, 4	TCKE[1:0]	01	R/W	tCKE These bits specify the minimum number of CKE pulse width during power-down mode. 00: 2 cycles 01: 3 cycles 10: 4 cycles 11: 5 cycles

Bit	Bit Name	Initial Value	R/W	Description
3	-	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2 to 0	TCKESR [2:0]	001	R/W	tCKESR These bits specify the minimum number of CKE pulse width during Self-refresh or Deep power-down mode. The specification of cycle number becomes this bit setting value +2. 000: 2 cycles 001: 3 cycles : 111: 9 cycles

7.4.5 SDRAM Common Wait Control Register C1A(SDWCRC1A)

SDWCRC1A specifies various wait cycles for SDRAM access. Set SDWCRC1A before accessing SDRAM.SDWCRC0A is initialized to H'20090120 by a power-on reset, but is not initialized and retains the contents in standby mode. The bits should be set before accessing SDRAM, and should not be modified during SDRAM access.

bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	TRFC[5:0]						–	–	–	TRCAB[4:0]				
Initial value	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	1
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TFAW[3:0]				TXR[3:0]				–	–	TSREX[5:0]					
Initial value	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31, 30	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29 to 24	TRFC[5:0]	100000	R/W	tRFC These bits specify the minimum number of cycles from issuing of the REF command to issuing of the next REF command, the minimum number of cycles from issuing of the REF command to issuing of the ACTV command. The specification of cycle number becomes this bit setting value +1. 000000: 1 cycles 000001: 2 cycles : 111111: 64 cycles
23 to 21	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20 to 16	TRCAB[4:0]	01001	R/W	tRC(AB) These bits specify the minimum number of cycles from issuing of the ACTV command to issuing of the (REF/SELF/DEEP) command. The specification of cycle number becomes this bit setting value +1. 00000: 1 cycles 00001: 2 cycles : 11111: 32 cycles

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	TFAW	All 0	R/W	tFAW These bits specify four Bank Active window(tFAW) The specification of cycle number becomes this bit setting value +1. 0000: 1 cycles 0001: 2 cycles : 1111: 16 cycles
11 to 8	TXP[3:0]	0001	R/W	tXR These bits specify the minimum number of cycles from exit power-down to next valid command. The specification of cycle number becomes this bit setting value +1. 0000: 1 cycles 0001: 2 cycles : 1111: 16 cycles
7,6	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5 to 0	TSREX[5:0]	100000	R/W	tSREX(tXSR) These bits specify the minimum number of cycles from exit self-refresh to next valid command. The specification of cycle number becomes this bit setting value +1. 000000: 1 cycles 000001: 2 cycles : 111111: 64 cycles

7.4.6 SDRAM Wait Control Register 00A(SDWCR00A)

SDWCR00A specifies various wait cycles for SDRAM access. Set SDWCR00A before accessing SDRAM.SDWCR00A is initialized to H'10608203 by a power-on reset, but is not initialized and retains the contents in standby mode. The bits should be set before accessing SDRAM, and should not be modified during SDRAM access.

bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	TRRD[2:0]			–	–	–	TRAS[4:0]					–	–	TPRAB[3:2]	
Initial value	0	0	0	1	0	0	0	0	0	1	1	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TPRAB[1:0]		–	–	TPRPB[3:0]				–	–	TRCD[5:0]					
Initial value	1	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1
R/W:	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	-	0	R	Reserved This bit is always read as 0. The write value should always be 0.
30 to 28	TRRD[2:0]	001	R/W	t_{RRD}, Delay Time for RAS to RAS Assertion These bits specify the minimum number of cycles from issuing of an ACTV command to issuing of the next ACTV command for a different bank. The specification of cycle number becomes this bit setting value +1. 000: 1 cycle 001: 2 cycles : 111: 8 cycles
27 to 25	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24 to 20	TRAS[4:0]	00110	R/W	t_{RAS}, RAS Active Time These bits specify the minimum number of cycles from issuing of an ACTV command to issuing of the PRE command for the same bank. The specification of cycle number becomes this bit setting value +1. 00000 : 1cycles 00001 : 2 cycles : 11111 : 32 cycles
19,18	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
17 to 14	TPRAB[3:0]	0010	R/W	$t_{RP(Ab)}$, Delay Time for All Bank Precharge to ACTV Command These bits specify the minimum number of cycles from issuing of the PALL command to issuing of the ACTV command. The specification of cycle number becomes this bit setting value +1. 0000 : 1 cycle 0001 : 2 cycles : 1111 : 16 cycles
13,12	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
11 to 8	TPRPB[3:0]	0010	R/W	$t_{RP(PB)}$, Delay Time for Precharge to ACTV Command These bits specify the minimum number of cycles from the start of auto-precharge or issuing of the PRE command to issuing of the ACTV command for the same bank. The specification of cycle number becomes this bit setting value +1. 0000 : 1 cycle 0001 : 2 cycles : 1111 : 16 cycles
7,6	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5 to 0	TRCD[5:0]	000011	R/W	tRCD, Number of Cycles from ACTV Command to READ(A)/WRIT(A) Command These bits specify the minimum number of cycles from issuing of the ACTV command to issuing of the READ(A)/WRIT(A) command. The specification of cycle number becomes this bit setting value +1. 000000 : 1 cycle 000001 : 2 cycles : 111111 : 64 cycles

7.4.7 SDRAM Wait Control Register 01A(SDWCR01A)

SDWCR01A specifies various wait cycles for SDRAM access. Set SDWCR01A before accessing SDRAM. SDWCR01A is initialized to H'00090106 by a power-on reset, but is not initialized and retains the contents in standby mode. The bits should be set before accessing SDRAM, and should not be modified during SDRAM access.

bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	TRCPB[4:0]				
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R/W	R/W	R/W

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	TRTP[2:0]			–	–	–	–	TWTP[3:0]			
Initial value	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20 to 16	TRCPB[4:0]	01001	R/W	t_{RC} Number of t_{RC}, RAS Cycles These bits specify the minimum number of cycles the from issuing of the ACTV command to issuing of the REF command or ACTV command for the same bank. The specification of cycle number becomes this bit setting value +1. 00000 : 1cycles 00001 : 2 cycles : 11111 : 32 cycles
15 to 11	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 8	TRTP[2:0]	001	R/W	tRTP Number of Cycles from READ(A) Command to PALL / PRE Command These bits specify the minimum number of cycles the from issuing of the READ(A) command to issuing of the PALL command or PRE command for the same bank. The specification of cycle number becomes this bit setting value +1. 000 : 1cycles 001 : 2 cycles : 111 : 8 cycles
7 to 4	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	TWTP[3:0]	0110	R/W	tWTP, Number of Cycles from WRIT(A) Command to PALL / PRE Command These bits specify the minimum number of cycles the from issuing of the WRIT(A) command to issuing of the PALL command or PRE command for the same bank. The specification of cycle number becomes this bit setting value +1. 0000 : 1cycles 0001 : 2 cycles : 1111 : 16 cycles

7.4.8 SDRAM Pin Control Register A (SDPCRA)

SDPCRA specifies the SDRAM pin states in standby mode. Set SDPCRA before accessing SDRAM. SDPCRA is initialized to H'0030 0087 by a power-on reset, but is not initialized and retains the contents in standby mode. Before changing the LPCLKFIX, CKEFIXA, and CKEFIXB bit values, confirm that the SDRAM is not being accessed.

bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	LPCLKFIX	–	–	MONCKEA	MONCKEB	–	–	CKEFIXA	CKEFIXB
Initial value	0	0	0	0	0	0	0	0	0	0	*	*	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	CKELV	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	*	0	0	0	0	1	1	1
R/W:	R	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	LPCLKFIX	0	R/W	LPCLK/LPCLK_N Pin Control bit 0: Normal oscillation for LPCLK and LPCLK_N after entering self-refresh mode or deep power-down mode (automatically stops when power-down mode is selected) 1: Fixed low-level output from LPCLK and LPCLK_N
23, 22	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
21	MONCKEA	1	R	LPCKEA Status Monitor 0: External pin LPCKEA is low 1: External pin LPCKEA is high
20	MONCKEB	1	R	LPCKEB Status Monitor 0: External pin LPCKEB is low 1: External pin LPCKEB is high
19, 18	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
17	CKEFIXA	0	R/W	LPCKEA Pin Fixed Output 0: Normal operation 1: External pin LPCKEA is fixed to low
16	CKEFIXB	0	R/W	LPCKEB Pin Fixed Output 0: Normal operation 1: External pin LPCKEB is fixed to low
15 to 8	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
7	CKELV	*	R/W	LPCKEA/LPCKEB Pin Level Control at Reset In a power-on reset or A4S area reset, the value of the CKEMD10 bit in reset control register 2 (RESCNT2) of the SYSC is sampled and set in this bit. If the chip is started with the CKEMD10 bit cleared to 0, the LPCKEA/LPCKEB pin will initially be at the low level. The LPCKEA/LPCKEB pin can then be driven high by writing 1 to this bit. This bit is automatically cleared when self-refresh mode is entered with both the RFSH and RMODE bits in the SDCRA0 register set to 1. This bit is readable and writable, but the only valid value for writing is 1. When the chip has been started up with the CKEMD10 bit cleared to 0, drive the LPCKEA/LPCKEB pin back to the high level by writing 1 to this bit. 0: The CKEMD10 bit, which sets the initial level of LPCKEA/LPCKEB, was 0 at the time of a power-on reset or A4S area reset, so the LPCKEA/LPCKEB pin is at the low level during the power-on reset or A4S area reset and after the reset has been canceled. 1: The CKEMD10 bit, which sets the initial level of LPCKEA/LPCKEB, was 1 at the time of a power-on reset or A4S area reset, so the LPCKEA/LPCKEB pin is at the high level during the power-on reset or A4S area reset and after the reset has been canceled.
6 to 3	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2 to 0	-	111	R	Reserved These bits are always read as 1. The write value should always be 1.

Note: * At a power-on reset or A4S area reset, the value of the CKEMD10 bit in reset control register 2 of the SYSC, which sets the initial level of LPCKEA/LPCKEB, is sampled and set in the CKELV bit.

7.4.9 Power-Down Control Register (SDPDCR0A)

SDPDCR0A is used to make settings related to power-down modes.

SDPDCR0A is initialized to H'08000000 by a power-on reset, but is not initialized and retains the contents in standby mode. The values of the bits should not be modified during SDRAM access.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PDWAIT								—	PDOWNSEL	—	—	—	—	—	—
Initial value:	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	RMODESEL0	RMODESEL1	—	DEEPSEL0	DEEPSEL1	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R/W	R/W	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	PDWAIT	H'08	R/W	These bits specify the number of cycles (ZBCK3) it takes to enter power-down mode. When power-down mode 0 or 1 is selected by the PDWON bits in SDCRA0/SDCRA1, the number of cycles between issuance of the last command to the SDRAM and the CKE pin pulled down to low is specified. When power-down mode 2 is selected by the PDWON bits in SDCRA0/SDCRA1, the number of cycles between issuance of the last command to the SDRAM and issuance of the self-refresh command is specified. H'00 to H'07: Setting prohibited H'08 to H'FF: Enters power-down mode after the specified number of cycles (ZBCK3) has passed
23	-	0	R	Reserved This bit is always read as 0. The write value should always be 0.
22	PDOWNSEL	0	R/W	Specifies the condition for entering power-down mode. 0: Selects the power-down mode specified by the PDWON bits in SDCRA0 1: Compares the power-down mode specified by the PDWON bits in SDCRA0 with the power-down mode specified by the PDWON bits in SDCRA1, and selects the power-down mode with the smaller access latency
21 to 14	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13	RMODESEL0	0	R/W	RMODE Select Bit 0 Specifies the condition for making the SDRAM connected to DRAM area 0 enter self-refresh mode. Whether to AND the RMODE bit in SDCRA0 and the RMODE bit in SDCRA0S is specified. 0: Self-refresh mode is controlled only by the RMODE bit in SDCRA0 1: Self-refresh mode is controlled by ANDing the RMODE bit in SDCRA0 and the RMODE bit in SDCRA0S (self-refresh mode is entered only when both bits are 1)
12	RMODESEL1	0	R/W	RMODE Select Bit 1 Specifies the condition for making the SDRAM connected to DRAM area 1 enter self-refresh mode. Whether to AND the RMODE bit in SDCRA1 and the RMODE bit in SDCRA1S is specified. 0: Self-refresh mode is controlled only by the RMODE bit in SDCRA1 1: Self-refresh mode is controlled by ANDing the RMODE bit in SDCRA1 and the RMODE bit in SDCRA1S (self-refresh mode is entered only when both bits are 1)
11	-	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
10	DEEPSEL0	0	R/W	DEEP Select Bit 0 Specifies the condition for making the SDRAM connected to DRAM area 0 enter deep power-down mode. Whether to AND the DEEP bit in SDCRA0 and the DEEP bit in SDCRA0S is specified. 0: Deep power-down mode is controlled only by the DEEP bit in SDCRA0 1: Deep power-down mode is controlled by ANDing the DEEP bit in SDCRA0 and the DEEP bit in SDCRA0S (deep power-down mode is entered only when both bits are 1)
9	DEEPSEL1	0	R/W	DEEP Select Bit 1 Specifies the condition for making the SDRAM connected to DRAM area 1 enter deep power-down mode. Whether to AND the DEEP bit in SDCRA1 and the DEEP bit in SDCRA1S is specified. 0: Deep power-down mode is controlled only by the DEEP bit in SDCRA1 1: Deep power-down mode is controlled by ANDing the DEEP bit in SDCRA1 and the DEEP bit in SDCRA1S (deep power-down mode is entered only when both bits are 1)
8 to 0	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

7.4.10 Extend bank mode Register (EBMCRA)

EBMCRA is a register that controls the bank address.

EBMCRA is initialized to H'00000000 by a power-on reset, but is not initialized and retains the contents in standby mode.

The values of the bits should not be modified during SDRAM access.

bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

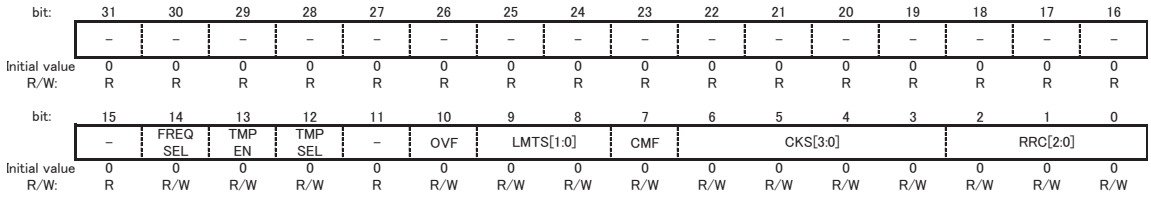
bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	BAA[1:0]	
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1 to 0	BAA[1:0]	00	R/W	Bank adders control(DRAM0) BANK(BA2 to 0), ROW, and the COL address position of the memory connected with the DRAM0 area are controlled. 00: BA2,BA1,BA0,ROW,COL 01: BA2,BA1, ROW, BA0,COL 10: BA2, ROW, BA1,BA0,COL 11: ROW, BA2,BA1,BA0,COL [notes] The high rank of an internal address doesn't correspond to the memory bank address when this bit is set excluding 00. Therefore, the bank position in which the memory by partial self-refresh is maintained doesn't become linear. When the BANK bit of SDCR0A is 0(four banks memory), this bit cannot be set to 11.

7.4.11 Refresh Timer Control/Status Register A (RTCSRA)

RTCSRA specifies various items about refresh for SDRAM.

When setting RTCSRA, write H'A55A to the upper 16 bits and the data to be written to the lower 16 bits in longwords.



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	-	All 0	R	Reserved These bits are always read as 0. The write value should always be H'A55A.
15	-	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14	FRQSEL	0	R/W	Frequency(ZBCK3) synchronization control bit of auto refreshing 0:OFF 1:ON
13	TMPEN	0	R/W	Temperature Sensor Refresh Control Enable 0: Disabled 1: Enabled
12	TMPSEL	0	R/W	Temperature Sensor Signal Polarity Select 0: Normal temperature when the temperature control signal is 0 and high temperature when it is 1 1: Normal temperature when the temperature control signal is 1 and high temperature when it is 0
11	OVF	0	R/W	Refresh Count Overflow Flag 0: Clearing condition: When 0 is written to the OVF bit after reading out RTCSRA during OVF = 1. 1: Setting condition: When the RFCRA counter overflows, that is, exceeds the count limit value indicated by bits LMTS[1:0].
10	-	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
9, 8	LMTS[1:0]	00	R/W	Refresh Count Overflow Limit Indicate the count limit value to be compared with the refresh count indicated by the RFCRA counter. When the RFCRA counter exceeds the value shown by these bits and overflows, the OVF flag is set. 00: Count limit value is 2048 01: Count limit value is 4096 10: Count limit value is 8192 11: Setting prohibited
7	CMF	0	R/W	Compare Match Flag 0: Clearing condition: When 0 is written to the CMF bit after reading out RTCSRA during CMF = 1. 1: Setting condition: When the condition RTCNTA = RTCORA is satisfied.
6 to 3	CKS[3:0]	0000	R/W	Clock Select Select the clock input to count up RTCNTA. 0000: Stop the counting-up 0001: ZB3ϕ/4 0010: ZB3ϕ/16 0011: ZB3ϕ/64 0100: ZB3ϕ/256 0101: ZB3ϕ/1024 0110: ZB3ϕ/2048 1001: EXTAL1ϕ/2 Other: Setting prohibited
2 to 0	RRC[2:0]	000	R/W	Refresh Count Specify the number of continuous refresh cycles, when the refresh request occurs after the coincidence of the values of RTCNTA and RTCORA. These bits can make the period of occurrence of refresh long. 000: Once 001: Twice 010: 4 times 011: 6 times 100: 8 times 101: Setting prohibited 110: Setting prohibited 111: Setting prohibited

7.4.12 Refresh Timer Counter A (RTCNTA)

RTCNTA is an 8-bit counter that increments using the clock selected by the CKS bits in RTCSRA. When RTCNTA matches RTCORA, RTCNTA is cleared to 0. The value in RTCNTA returns to 0 after counting up to 255.

When setting RTCNTA , write H'A55A00 to the upper 24 bits and the data to be written to the lower eight bits in longwords.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—								
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	-	All 0	R	Reserved These bits are always read as 0. The write value should always be H'A55A00.
7 to 0		H'00	R/W	8-Bit Counter

7.4.13 Refresh Time Constant Register A (RTCORA)

RTCORA is referenced when the TMPEN bit in RTCSRA is 0 or 1 with the SDRAM temperature sensor indicating normal temperature. When the RTCORA value matches the RTCNTA value, the CMF bit in RTCSRA is set to 1 and RTCNTA is cleared to 0.

When the RFSH bit in SDCRA0 is set to 1, a refresh request is issued by this matching signal. This refresh request is retained until the refresh operation is performed. If the refresh request is not processed when the next matching occurs, the previous refresh request is ignored.

When setting RTCORA, write H'A55A00 to the upper 24 bits and the data to be written to the lower eight bits in longwords

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—								
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	-	All 0	R	Reserved These bits are always read as 0. The write value should always be H'A55A00.
7 to 0	-	H'00	R/W	Counter Upper Limit Value

7.4.14 Refresh Time Constant Register HA (RTCORHA)

RTCORHA is referenced instead of RTCORA when the TMPEN bit in RTCSRA is 1 with the SDRAM temperature sensor indicating high temperature. When the RTCORHA value matches the RTCNTA value, the CMF bit in RTCSRA is set to 1 and RTCNTA is cleared to 0.

When the RFSH bit in SDCRA0 is set to 1, a refresh request is issued by this matching signal. This refresh request is retained until the refresh operation is performed. If the refresh request is not processed when the next matching occurs, the previous refresh request is ignored.

When setting RTCORHA, write H'A55A00 to the upper 24 bits and the data to be written to the lower eight bits in longwords.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—								
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	-	All 0	R	Reserved These bits are always read as 0. The write value should always be H'A55A00.
7 to 0	-	H'00	R/W	Counter Upper Limit Value

7.4.15 Refresh Time Constant Register SA (RTCORSA)

RTCORSA is referenced when the FREQSEL bit in RTCSRA is 1 with ZBCLK3 is slow frequency and when the TMPEN bit in RTCSRA is 0 or 1 with the SDRAM temperature sensor indicating normal temperature. When the RTCORSA value matches the RTCNTA value, the CMF bit in RTCSRA is set to 1 and RTCNTA is cleared to 0.

When the RFSH bit in SDCRA0 is set to 1, a refresh request is issued by this matching signal. This refresh request is retained until the refresh operation is performed. If the refresh request is not processed when the next matching occurs, the previous refresh request is ignored.

When setting RTCORSA, write H'A55A00 to the upper 24 bits and the data to be written to the lower eight bits in longwords

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—								
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	-	All 0	R	Reserved These bits are always read as 0. The write value should always be H'A55A00.
7 to 0	-	H'00	R/W	Counter Upper Limit Value

7.4.16 Refresh Time Constant Register SHA (RTCORSHA)

RTCORSHA is referenced when the FREQSEL bit in RTCSRA is 1 with ZBCLK3 is high frequency and when the TMPEN bit in RTCSRA is 0 or 1 with the SDRAM temperature sensor indicating normal temperature. When the RTCORSHA value matches the RTCNTA value, the CMF bit in RTCSRA is set to 1 and RTCNTA is cleared to 0.

When the RFSH bit in SDCRA0 is set to 1, a refresh request is issued by this matching signal. This refresh request is retained until the refresh operation is performed. If the refresh request is not processed when the next matching occurs, the previous refresh request is ignored.

When setting RTCORSHA, write H'A55A00 to the upper 24 bits and the data to be written to the lower eight bits in longwords

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—								
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	-	All 0	R	Reserved These bits are always read as 0. The write value should always be H'A55A00.
7 to 0	-	H'00	R/W	Counter Upper Limit Value

7.4.17 Refresh Count Register A (RFCRA)

RFCRA is a readable/writable 13-bit counter that counts the number of refreshing. The count is incremented each time RTCORA and RTCNTA match. When the count exceeds the count limit value specified by the LMTS bit in RTCSRA, the OVF flag in RTCSRA is set and RFCRA is cleared.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

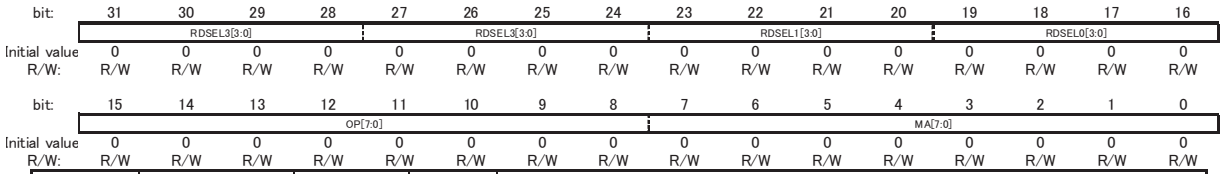
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—													
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 13	-	All 0	R	Reserved These bits are always read as 0. The write value of bits 31 to 16 should always be H'A55A.
12 to 0	-	H'0000	R/W	13-Bit Counter

7.4.18 SDRAM Mode Register Addres/Commod Register0/1A (SDMRACR0/1A)

SDMRACR0/1A is 32-bit registers that control the mode register access. SDMRACR0/1A is initialized to H'00000000 by a power-on reset, but is not initialized and retains the contents in standby mode.

SDMRACCR0A is referred to when SDMR.REGSEL=0 and SDMRACCR1A is referred to when SDMR.REGSEL=1.



Bit	Bit Name	Initial Value	R/W	Description
31 to 28	RDSEL3[3:0]	All 0	R/W	These bits controls the position where the data read by the MRR command is stored. (R[31:24] of CPU). 1xxx : 8'h00 is returned to R[31:24] of CPU 0000 : LPD[7:0] is returned to R[31:24] of CPU 0001 : LPD[15:8] is returned to R[31:24] of CPU 0010 : LPD[23:16] is returned to R[31:24] of CPU 0011 : LPD[31:24] is returned to R[31:24] of CPU. 0100 : LPD[39:32] is returned to R[31:24] of CPU 0101 : LPD[47:40] is returned to R[31:24] of CPU 0110 : LPD[55:48] is returned to R[31:24] of CPU 0111 : LPD[63:56] is returned to R[31:24] of CPU A set value of this bit depends on the connection of this LSI and LPDDR2-SDRAM.

Bit	Bit Name	Initial Value	R/W	Description
27 to 24	RDSEL2[3:0]	0000	R/W	These bits controls the position where the data read by the MRR command is stored. (R[23:16] of CPU). 1xxx : 8'h00 is returned to R[23:16] of CPU 0000 : LPD[7:0] is returned to R[23:16] of CPU 0001 : LPD[15:8] is returned to R[23:16] of CPU 0010 : LPD[23:16] is returned to R[23:16] of CPU 0011 : LPD[31:24] is returned to R[23:16] of CPU. 0100 : LPD[39:32] is returned to R[23:16] of CPU 0101 : LPD[47:40] is returned to R[23:16] of CPU 0110 : LPD[55:48] is returned to R[23:16] of CPU 0111 : LPD[63:56] is returned to R[23:16] of CPU A set value of this bit depends on the connection of this LSI and LPDDR2-SDRAM.
23 to 20	RDSEL1[3:0]	0000	R/W	These bits controls the position where the data read by the MRR command is stored. (R[15:8] of CPU). 1xxx : 8'h00 is returned to R[15:8] of CPU 0000 : LPD[7:0] is returned to R[15:8] of CPU 0001 : LPD[15:8] is returned to R[15:8] of CPU 0010 : LPD[23:16] is returned to R[15:8] of CPU 0011 : LPD[31:24] is returned to R[15:8] of CPU. 0100 : LPD[39:32] is returned to R[15:8] of CPU 0101 : LPD[47:40] is returned to R[15:8] of CPU 0110 : LPD[55:48] is returned to R[15:8] of CPU 0111 : LPD[63:56] is returned to R[15:8] of CPU A set value of this bit depends on the connection of this LSI and LPDDR2-SDRAM.
19 to 16	RDSEL0[3:0]	0000	R/W	These bits controls the position where the data read by the MRR command is stored. (R[7:0] of CPU). 1xxx : 8'h00 is returned to R[7:0] of CPU 0000 : LPD[7:0] is returned to R[7:0] of CPU 0001 : LPD[15:8] is returned to R[7:0] of CPU 0010 : LPD[23:16] is returned to R[7:0] of CPU 0011 : LPD[31:24] is returned to R[7:0] of CPU. 0100 : LPD[39:32] is returned to R[7:0] of CPU 0101 : LPD[47:40] is returned to R[7:0] of CPU 0110 : LPD[55:48] is returned to R[7:0] of CPU 0111 : LPD[63:56] is returned to R[7:0] of CPU A set value of this bit depends on the connection of this LSI and LPDDR2-SDRAM.

Bit	Bit Name	Initial Value	R/W	Description
15 to 8	OP[7:0]	All 0	R/W	Specifies value set in mode register (OP).
7 to 0	MA[7:0]	All 0	R/W	Specifies mode register address (MA).

7.4.19 SDRAM Mode Register Temp Control RegisterA (SDMRTMPCRA)

SDMRTMPCRA controls the automatic refresh rate switch function. SDMRTMPCRA is initialized to H'00000000 by a power-on reset, but is not initialized and retains the contents in standby mode.

bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	RDSEL1[3:0]				RDSEL0[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	MA[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 20	RDSEL1[3:0]	0000	R/W	When automatic refresh rate switch function is used, the reading data from mode register specified in the MA bit of this register is stored in SDMRTMPMONA. These bits controls the position where the data read by the MRR command is stored. (SDMRTMPMONA[15:8]). These bits controls the reading value from the memory connected with DRAM area 0. 1xxx : 0 is returned to SDMRTMPMONA[15:8]. 0000 : LPD[7:0] is returned to SDMRTMPMONA[15:8] 0001 : LPD[15:8] is returned to SDMRTMPMONA[15:8] 0010 : LPD[23:16] is returned to SDMRTMPMONA[15:8] 0011 : LPD[31:24] is returned to SDMRTMPMONA[15:8] 0100 : LPD[39:32] is returned to SDMRTMPMONA[15:8] 0101 : LPD[47:40] is returned to SDMRTMPMONA[15:8] 0110 : LPD[55:48] is returned to SDMRTMPMONA[15:8] 0111 : LPD[63:56] is returned to SDMRTMPMONA[15:8] A set value of this bit depends on the connection of this LSI and LPDDR2-SDRAM.

Bit	Bit Name	Initial Value	R/W	Description
19 to 16	RDSEL0 [3:0]	0000	R/W	When automatic refresh rate switch function is used, the reading data from mode register specified in the MA bit of this register is stored in SDMRTMPMONA. These bits controls the position where the data read by the MRR command is stored. (SDMRTMPMONA[7:0]). These bits controls the reading value from the memory connected with DRAM area 0. 1xxx : 0 is returned to SDMRTMPMONA[7:0]. 0000 : LPD[7:0] is returned to SDMRTMPMONA[7:0] 0001 : LPD[15:8] is returned to SDMRTMPMONA[7:0] 0010 : LPD[23:16] is returned to SDMRTMPMONA[7:0] 0011 : LPD[31:24] is returned to SDMRTMPMONA[7:0] 0100 : LPD[39:32] is returned to SDMRTMPMONA[7:0] 0101 : LPD[47:40] is returned to SDMRTMPMONA[7:0] 0110 : LPD[55:48] is returned to SDMRTMPMONA[7:0] 0111 : LPD[63:56] is returned to SDMRTMPMONA[7:0] A set value of this bit depends on the connection of this LSI and LPDDR2-SDRAM.
15 to 8	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	MA[7:0]	All 0	R/W	Specifies mode register address (MA).

7.4.20 SDRAM Mode Register Temp Monitor Mask RegisterA (SDMRTMPMONA)

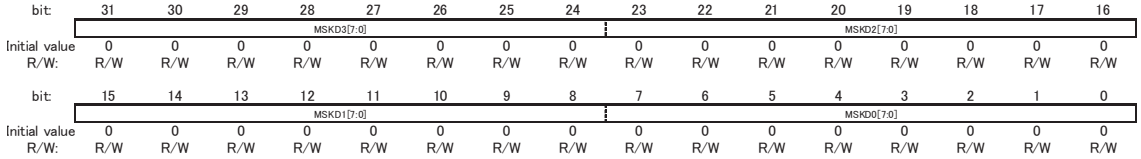
SDMRTMPMONA is a register that stores the reading value from a memory internal register when the automatic refresh rate switch function is used. SDMRTMPMONA is initialized to H'00000000 by a power-on reset, but is not initialized and retains the contents in standby mode.

bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MOND3[7:0]								MOND2[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MOND1[7:0]								MOND0[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7.4.21 SDRAM Mode Register Temp Monitor Mask RegisterA (SDMRTMPMSKA)

SDMRTMPMSKA selects the bit value used from the reading value taken into the SDMRTMPMONA for high temperature/normal temperature judgment, when the automatic refresh rate switch function is used.

SDMRTMPMSKA is initialized to H'00000000 by a power-on reset, but is not initialized and retains the contents in standby mode.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	MOND3[7:0]	All 0	R/W	The data read according to the setting of the MA bit and the RDSEL3 bit of the SDMRTMPCRA is stored.
23 to 16	MOND2[7:0]	All 0	R/W	The data read according to the setting of the MA bit and the RDSEL2 bit of the SDMRTMPCRA is stored.
15 to 8	MOND1[7:0]	All 0	R/W	The data read according to the setting of the MA bit and the RDSEL1 bit of the SDMRTMPCRA is stored.
7 to 0	MOND0[7:0]	All 0	R/W	The data read according to the setting of the MA bit and the RDSEL0 bit of the SDMRTMPCRA is stored.

7.4.22 SDRAM General-purpose Down Counter A (SDGENCNTA)

SDGENCNTA is a general-purpose down counter. SDGENCNTA can be used when waiting for a fixed time as execute the initialization sequence of the memory. The countdown begins immediately when the value of 1 or more is written in this register. And, it stops when becoming 0. SDGENCNTA is a 32-bit counter that decrements using ZB3D2CLK.

SDGENCNTA is initialized to H'00000000 by a power-on reset.

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	CNT[31:0]	All 0	R/W	These bits set the count value. The countdown begins immediately when the value of 1 or more is written in this register. And, it stops when becoming 0 [note] There is a possibility that the SBSC internal clock stops when Power-down mode3 has been selected. Therefore, this counter operation stops, too.

7.4.23 Burst Refresh Count Register A (BSTRCNTA)

BSTRCNTA specifies the number of refresh operations in burst refreshing performed after the SDRAM has been taken out of self-refresh mode. This function should be used when the SDRAM in use requires a specified number of auto-refresh operations after leaving self-refresh mode.

BSTRCNTA is initialized to H'00000000 by a power-on reset, but is not initialized and retains its contents when the chip enters standby mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SREFCNT[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 0	SREFCNT [15:0]	H'0000	R/W	Specifies the number of refresh commands (REF) to be inserted after self-refresh mode is exited. The refresh command will be issued the number of times specified in this part of the register.*

Note: * With this register set to 0, burst refreshing will not be performed after self-refresh mode is exited.

7.4.24 Memory Protected Area Division Register 0 to 2 A (SDPTDIVCR0 to 2A)

SDPTDIVCRA is a 32-bit register that sets the division in the protection location of the external memory space. This register has the register write protection function.

These registers which have the register write protect function cannot be changed by a CPU that does not have the privilege to access.

bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	CPUTYPE[2:0]			REGWP	REGWP2	-	-	-	-	-	-	-
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R	R

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DIVADDR[14:0]															-
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R

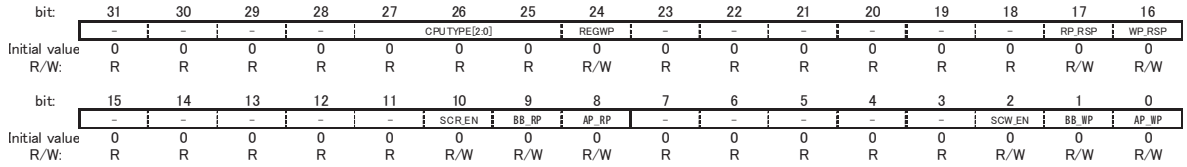
Bit	Bit Name	Initial Value	R/W	Description
31 to 28	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
27 to 25	CPUTYPE[2:0]	000	R	These bits indicate the CPU that has the privilege to change this register setting. When specifying the CPU that will have the privilege to change this register setting, write 1 to the REGWP bit or the REGWP2 at the same time. When REGWP2 is set 1, no CPUs have the privilege to change this register setting. When REGWP2 is set 0 and REGWP is set 1, the CPU that has written to this register is automatically set as the CPU with the privilege to change this register setting. When B'0 is written to the REGWP bit, these bits are cleared to B'000 and all CPUs are allowed to change this register setting. 000: All CPUs have the privilege to change this register setting 001: Only AP-SH has the privilege to change this register setting 010: Only AP-ARM (non-secure mode) has the privilege to change this register setting 110: Only AP-ARM (secure mode) has the privilege to change this register setting 111: No CPUs has the privilege to change this register setting No values other than the above can be read.
24	REGWP	0	R/W	Register Write Privilege Setting Specifies whether the CPU that has set this register allows other CPUs to change the register setting. After 1 is written to this bit, this bit is automatically cleared to 0. When this bit is set to 1, the CPU that has set this register is set to the CPUTYPE bits. After this register value has been changed, read from this register to confirm through software that this bit has returned to 0 and the CPUTYPE bit setting has been updated. After that, start access to the memory area. A write to this register from a CPU that does not have the privilege to change this register setting as shown by the CPUTYPE bits is invalidated. 0: All CPUs can change this register setting 1: Only the CPU that has set this register has the privilege to change this register setting

Bit	Bit Name	Initial Value	R/W	Description
23	REGWP2	0	R/W	Register Write Privilege Setting2 Specifies whether to prohibit the setting change of this register since this register was set. After 1 is written to this bit, this bit is automatically cleared to 0. When this bit is set to 1, the CPU that has set this register is set to the CPUTYPE bits. When REGWP2 is set to 1, 3'b111 is set to CPUTYPE. After this register value has been changed, read from this register to confirm through software that this bit has returned to 0 and the CPUTYPE bit setting has been updated. After that, start access to the memory area. A write to this register from a CPU that does not have the privilege to change this register setting as shown by the CPUTYPE bits is invalidated. 0: The privilege that changes this register setting depends on the REGWP bit. 1: No CPU have the privilege that changes this register setting even in power-on reset.
23 to 16	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 1	DIVADR	All 0	R/W	The memory protection division address is set. The physical address[31:17] of this LSI is set. [note] SDPTCR0A to 3A register is not set until this register is set. A set value of the DIVADR bit should fill the relation between the following. (SBSC top address (0x40000000) >> 17) < SDPTDIVCR0.DIVADR < SDPTDIVCR1.DIVADR < SDPTDIVCR2.DIVADR < (SBSC top address (0x5FFFFFFF) >> 17) Operation when violating it is outside the guarantee as for the restriction.
0	-	0	R	Reserved This bit is always read as 0. The write value should always be 0.

7.4.25 Memory Protected Area Setting Registers 0A to 3A (SDPTCR0A to SDPTCR3A)

The SDPTCRA registers are 32-bit registers that specify write protection for the external memory spaces.
Protection can be set within 4 Gbits from the start address of each supported external memory space, and the access inhibit to four each area divided by the SDPTDIVCR0Ato2A register is set.
These registers which have the register write protect function cannot be changed by a CPU that does not have the privilege to access.



bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	CPUTYPE[2:0]			REGWP	–	–	–	–	–	–	RP_RSP	WP_RSP
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R/W	R/W

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	SCR_EN	BB_RP	AP_RP	–	–	–	–	–	SCW_EN	BB_WP	AP_WP
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
27 to 25	CPUTYPE [2:0]	000	R	These bits indicate the CPU that has the privilege to change this register setting. When specifying the CPU that will have the privilege to change this register setting, write 1 to the REGWP bit at the same time. The CPU that has written to this register is automatically set as the CPU with the privilege to change this register setting. When B'0 is written to the REGWP bit, these bits are cleared to B'000 and all CPUs are allowed to change this register setting. 000: All CPUs have the privilege to change this register setting 001: Only AP-SH has the privilege to change this register setting 010: Only AP-ARM (non-secure mode) has the privilege to change this register setting 110: Only AP-ARM (secure mode) has the privilege to change this register setting Nothing other than the above will be read.
24	REGWP	0	R/W	Register Write Privilege Setting Specifies whether the CPU that has set this register allows other CPUs to change the register setting. After 1 is written to this bit, this bit is automatically cleared to 0. When this bit is set to 1, the CPU that has set this register is set to the CPUTYPE bits. After this register value has been changed, read from this register to confirm through software that this bit has returned to 0 and the CPUTYPE bit setting has been updated. After that, start access to the memory area. A write to this register from a CPU that does not have the privilege to change this register setting as shown by the CPUTYPE bits is invalidated. 0: All CPUs can change this register setting 1: Only the CPU that has set this register has the privilege to change this register setting
23 to 18	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
17	RP_RSP	0	R/W	Specifies the SBSC1 response method used when a read-protected area was accessed for read. A write to this register from a CPU that does not have the privilege to change this register setting as shown by the CPUTYPE bits is invalidated. 0: Error response 1: No error response Note:Error response when this bit is 0: When the AP-SH accesses a write-protected area, the SBSC returns an error response but the AP-SH does not initiate exception handling. When the AP-ARM accesses a write-protected area, data is aborted.
16	WP_RSP	0	R/W	Specifies the SBSC1 response method when a write-protected area was accessed for write. A write to this register from a CPU that does not have the privilege to change this register setting as shown by the CPUTYPE bits is invalidated. 0: Error response 1: No error response Note:Error response when this bit is 0: When the AP-SH accesses a write-protected area, the SBSC returns an error response but the AP-SH does not initiate exception handling. When the AP-ARM accesses a write-protected area, data is aborted.
15 to 11	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10	SCR_EN	0	R/W	Secure area specification. (Read Privilege Setting) A write to this register from a CPU that does not have the privilege to change this register setting as shown by the CPUTYPE bits is invalidated . 0: The relevant SBSC area is Non-Secure area 1: The relevant SBSC area is Secure area When this bit is set to1, only the initiator of the secure mode can be read, and it doesn't depend on the setting of the BB_RP/AP_RP bit . When reading from initiators other than the secure mode , all 0 is read.
9	BB_RP	0	R/W	BB Resource* Read Privilege Setting A write to this register from a CPU that does not have the privilege to change this register setting as shown by the CPUTYPE bits is invalidated. 0: Has the privilege to read the appropriate SBSC area 1: Does not have the privilege to read the appropriate SBSC area A value read from a read-protected area is always 0.

Bit	Bit Name	Initial Value	R/W	Description
8	AP_RP	0	R/W	AP Resource* Read Privilege Setting A write to this register from a CPU that does not have the privilege to change this register setting as shown by the CPUTYPE bits is invalidated. 0: Has the privilege to read the appropriate SBSC area 1: Does not have the privilege to read the appropriate SBSC area A value read from a read-protected area is always 0.
7 to 3	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	SCW_EN	0	R/W	Secure area specification. (Write Privilege Setting) A write to this register from a CPU that does not have the privilege to change this register setting as shown by the CPUTYPE bits is invalidated . 0: The relevant SBSC area is Non-Secure area 1: The relevant SBSC area is Secure area When this bit is set to1, Only the initiator of the secure mode can be write, and it doesn't depend on the setting of the BB_WP/AP_WP bits .
1	BB_WP	0	R/W	BB Resource* Write Privilege Setting A write to this register from a CPU that does not have the privilege to change this register setting as shown by the CPUTYPE bits is invalidated. 0: Has the privilege to write to the relevant SBSC area 1: Does not have the privilege to write to the relevant SBSC area
0	AP_WP	0	R/W	AP Resource* Write Privilege Setting A write to this register from a CPU that does not have the privilege to change this register setting as shown by the CPUTYPE bits is invalidated. 0: Has the privilege to write to the relevant SBSC area 1: Does not have the privilege to write to the relevant SBSC area

Note: * AP resources: AP-SH, AP-ARM, AP-DMAC (RT-DMAC, SYS-DMAC), AP-JTAG, and others (image IP, USBDMAC)
BB resources: ACMFI

7.4.26 SDRAM Drivability Control Register 0A (SDDRVCR0A)

SDDRVCR0A controls the drivability of the LP bus. SDDRVCR0A is initialized to H'0FFFFFFF at a power-on reset. In standby mode, however, SDDRVCR0A is not initialized and retains its content. Do not change the value of any bit during access to SDRAM.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	LPCMD_DRV [1:0]		LPD3_DRV [1:0]		LPD2_DRV [1:0]		LPD1_DRV [1:0]		LPD0_DRV [1:0]		LPDQM3_DRV [1:0]	
Initial value:	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LPDQM2_DRV [1:0]		LPDQM1_DRV [1:0]		LPDQM0_DRV [1:0]		LPDQS3_DRV [1:0]		LPDQS2_DRV [1:0]		LPDQS1_DRV [1:0]		LPDQS0_DRV [1:0]		LPCLK_DRV [1:0]	
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
27, 26	LPCMD_DRV [1:0]	11	R/W	These bits control the drivability of the LPCSA, LPCSB, LPCKEA, LPCKEB and LPCA9-0 pins. 00: Small drive 01: ↑ 10: ↓ 11: Large drive
25, 24	LPD3_DRV [1:0]	11	R/W	These bits control the drivability of the LPD31 to LPD24 pins during output. 00: Small drive 01: ↑ 10: ↓ 11: Large drive
23, 22	LPD2_DRV [1:0]	11	R/W	These bits control the drivability of the LPD23 to LPD16 pins during output. 00: Small drive 01: ↑ 10: ↓ 11: Large drive
21, 20	LPD1_DRV [1:0]	11	R/W	These bits control the drivability of the LPD15 to LPD8 pins during output. 00: Small drive 01: ↑ 10: ↓ 11: Large drive

Bit	Bit Name	Initial Value	R/W	Description
19, 18	LPD0_DRV [1:0]	11	R/W	These bits control the drivability of the LPD7 to LPD0 pins during output. 00: Small drive 01: ↑ 10: ↓ 11: Large drive
17, 16	LPDQM3_DRV [1:0]	11	R/W	These bits control the drivability of the LPDQM3 pin. 00: Small drive 01: ↑ 10: ↓ 11: Large drive
15, 14	LPDQM2_DRV [1:0]	11	R/W	These bits control the drivability of the LPDQM2 pin. 00: Small drive 01: ↑ 10: ↓ 11: Large drive
13, 12	LPDQM 1_DRV [1:0]	11	R/W	These bits control the drivability of the LPDQM1 pin. 00: Small drive 01: ↑ 10: ↓ 11: Large drive
11, 10	LPDQM 0_DRV [1:0]	11	R/W	These bits control the drivability of the LPDQM0 pin. 00: Small drive 01: ↑ 10: ↓ 11: Large drive
9, 8	LPDQS3_DRV [1:0]	11	R/W	These bits control the drivability of the LPDQS3 and LPDQS3_N pins during output. 00: Small drive 01: ↑ 10: ↓ 11: Large drive
7, 6	LPDQS2_DRV [1:0]	11	R/W	These bits control the drivability of the LPDQS2 and LPDQS2_N pins during output. 00: Small drive 01: ↑ 10: ↓ 11: Large drive

Bit	Bit Name	Initial Value	R/W	Description
5, 4	LPDQS 1_DRV [1:0]	11	R/W	These bits control the drivability of the LPDQS1 and LPDQS1_N pins during output. 00: Small drive 01: ↑ 10: ↓ 11: Large drive
3, 2	LPDQS 0_DRV [1:0]	11	R/W	These bits control the drivability of the LPDQS0 and LPDQS0_N pins during output. 00: Small drive 01: ↑ 10: ↓ 11: Large drive
1, 0	LPCLK_DRV [1:0]	11	R/W	These bits set the drivability of the LPCLK and LPCLK_N pins. 00: Small drive 01: ↑ 10: ↓ 11: Large drive

7.4.27 SDRAM Drivability Control Register 1A (SDDRVCR1A)

SDDRVCR1A controls the drivability of the LP bus. SDDRVCR1A is initialized to H'03FFFFFC at a power-on reset. In standby mode, however, SDDRVCR1A is not initialized and retains its content. Do not change the value of any bit during access to SDRAM

bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	LPD7_DRV[1:0]		LPD6_DRV[1:0]		LPD5_DRV[1:0]		LPD4_DRV[1:0]		LPDQM7_DRV[1:0]	
Initial value	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LPDQM6_DRV[1:0]		LPDQM5_DRV[1:0]		LPDQM4_DRV[1:0]		LPDQS7_DRV[1:0]		LPDQS6_DRV[1:0]		LPDQS5_DRV[1:0]		LPDQS4_DRV[1:0]		-	-
Initial value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 26	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25, 24	LPD7_DRV [1:0]	11	R/W	These bits control the drivability of the LPD63 to LPD56 pins during output. 00: Small drive 01: ↑ 10: ↓ 11: Large drive

Bit	Bit Name	Initial Value	R/W	Description
23, 22	LPD6_DRV [1:0]	11	R/W	These bits control the drivability of the LPD55 to LPD48 pins during output. 00: Small drive 01: ↑ 10: ↓ 11: Large drive
21, 20	LPD5_DRV [1:0]	11	R/W	These bits control the drivability of the LPD47 to LPD40 pins during output. 00: Small drive 01: ↑ 10: ↓ 11: Large drive
19, 18	LPD4_DRV [1:0]	11	R/W	These bits control the drivability of the LPD39 to LPD32 pins during output. 00: Small drive 01: ↑ 10: ↓ 11: Large drive
17, 16	LPDQM7_DRV [1:0]	11	R/W	These bits control the drivability of the LPDQM7 pin. 00: Small drive 01: ↑ 10: ↓ 11: Large drive
15, 14	LPDQM6_DRV [1:0]	11	R/W	These bits control the drivability of the LPDQM6 pin. 00: Small drive 01: ↑ 10: ↓ 11: Large drive
13, 12	LPDQM 5_DRV [1:0]	11	R/W	These bits control the drivability of the LPDQM5 pin. 00: Small drive 01: ↑ 10: ↓ 11: Large drive
11, 10	LPDQM 4_DRV [1:0]	11	R/W	These bits control the drivability of the LPDQM4 pin. 00: Small drive 01: ↑ 10: ↓ 11: Large drive

Bit	Bit Name	Initial Value	R/W	Description
9, 8	LPDQS7_DRV [1:0]	11	R/W	These bits control the drivability of the LPDQS7 and LPDQS7_N pins during output. 00: Small drive 01: ↑ 10: ↓ 11: Large drive
7, 6	LPDQS6_DRV [1:0]	11	R/W	These bits control the drivability of the LPDQS6 and LPDQS6_N pins during output. 00: Small drive 01: ↑ 10: ↓ 11: Large drive
5, 4	LPDQS 5_DRV [1:0]	11	R/W	These bits control the drivability of the LPDQS5 and LPDQS5_N pins during output. 00: Small drive 01: ↑ 10: ↓ 11: Large drive
3, 2	LPDQS 4_DRV [1:0]	11	R/W	These bits control the drivability of the LPDQS4 and LPDQS4_N pins during output. 00: Small drive 01: ↑ 10: ↓ 11: Large drive
1,0	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

7.4.28 DLL control register0A (DLLCNT0A)

DLLCNT0A controls the DLL of the DDR-Phy in This LSI. bus. DLLCNT0A is initialized to H'27100000 at a power-on reset. In standby mode, however, DLLCNT0A is not initialized and retains its content.

bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DLLCYC[15:0]															
Initial value	0	0	1	0	0	1	1	1	0	0	0	1	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	DLLMODE[1:0]	
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	DLLCYC	H'2710	R/W	Specification at DLL oscillation steady waiting cycle. The value that satisfies the following condition is set to DLLCYC. DLLCYC > 33 us * EXTAL1 / 2 ex) Case : EXTAL1 = 26MHz DLLCYC > 33 * 26 / 2 = 0x01AD
15	D2MSTP	0	R/W	Clock control bit for DDR PHY (LPD63-LPD32 0;clock enable (64 bit bus width) 1:clock stop (32 bit bus width)
14 to 2	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1,0	DLLMODE[1:0]	All 0	R/W	DLL mode selection 00 : DLL oscillation Off 01 : DLL oscillation On (Always) 10 : DLL oscillation On (synchronizes with the power management) Other than aboe: Setting prohibited

7.4.29 SBSC Monitor Register 0A (SBSCMON0A)

SBSCMON0A This register is a register that monitors an internal state of SBSC and this LSI.

SBSCMON0A is Read only register.

bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DLLMON	-	-	-	-	-	-	-	-	-	-	PLLC1MON	-	-	-	DDRMODE
Initial value	0	0	0	0	0	0	0	0	0	0	0	1	0	x	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	-	All 0	R	Reserved
16	-	x	R	Reserved The reading value of this bit is not decided.
15	DLLMON	0	R	The state of DLL oscillation 0: DLL oscillation is not steady. 1: DLL oscillation is steady.
14 to 5	-	All 0	R	Reserved These bits are always read as 0.

Bit	Bit Name	Initial Value	R/W	Description
4	PLLC1MON	1	R	The state of PLLC1. SDCR0A.PLLCNT is 0 : This bit is always read as 1. SDCR0A.PLLCNT is 1 : 0 : PLLC1 OFF 1 : PLLC1 ON
3	-	0		Reserved These bits are always read as 0.
2	-	x	R	Reserved The reading value of this bit is not decided.
1		0		Reserved These bits are always read as 0.
0	DDRMODE	0	R	The state of CPGA.FRQCRD.ZB3D2SEL 0: ZB3D2SEL = 0 (DDR400 mode is selected) 1: ZB3D2SEL = 1 (DDR600 mode is selected)

7.5 Operation

This section describes the SBSC1 operation.

Replace the register names and pin names shown below when reading if not specified otherwise.

- Register names to be replaced when reading

  SBSC1: XXXXA → Notation in section 7.5: XXXX

  Example: SDCR0A (SDRAM control register 0A of SBSC1) → Notation in section 7.5: SDCR0

This LSI supports only 32-bits / 64-bits width SDRAM.

7.5.1 Access Size and Data Alignment

This LSI supports little endian, in which address 0 is the least significant byte (LSByte) in the byte data. Two data bus widths are available; 32 bits and 64 bits in the SBSC1. Data alignment is performed in accordance with the data bus width. This also means that when longword data is read from a 16-bit width SDRAM, the read operation must be done twice. In this LSI, data alignment and conversion of the data length are performed automatically through the interface with SDRAM.

Tables 7.5 to 7.7 show the relationship between the SDRAM data width and access unit.

Table 7.5 16-Bit External Bus Access and Data Alignment

Operation		Data bus				Strobe Signals			
		LPD31 to LPD24	LPD23 to LPD16	LPD15 to LPD8	LPD7 to LPD0	LPDQM3	LPDQM2	LPDQM1	LPDQM0
Byte access at 4n + 0		-	-	-	Data 7 to 0	-	-	-	Assert
Byte access at 4n + 1		-	-	Data 7 to 0	-	-	-	Assert	-
Byte access at 4n + 2		-	-	-	Data 7 to 0	-	-	-	-
Byte access at 4n + 3		-	-	Data 7 to 0	-	-	-	-	-
Word access at 4n + 0		-	-	Data 15 to 8	Data 7 to 0	-	-	Assert	Assert
Word access at 4n + 2		-	-	Data 15 to 8	Data 7 to 0	-	-	-	-
Longword access at 4n	1st time at 0	-	-	Data 15 to 8	Data 7 to 0	-	-	Assert	Assert
	1st time at 2	-	-	Data 31 to 24	Data 23 to 16	-	-	Assert	Assert

Table 7.6 32-Bit External Bus Access and Data Alignment

Operation	Data bus				Strobe Signals			
	LPD31 to LPD24	LPD23 to LPD16	LPD15 to LPD8	LPD7 to LPD0	LPDQM3	LPDQM2	LPDQM1	LPDQM0
Byte access at 4n + 0	-	-	-	Data 7 to 0	-	-	-	Assert
Byte access at 4n + 1	-	-	Data 7 to 0	-	-	-	Assert	-
Byte access at 4n + 2	-	Data 7 to 0	-	-	-	Assert	-	-
Byte access at 4n + 3	Data 7 to 0	-	-	-	Assert	-	-	-
Word access at 4n + 0	-	-	Data 15 to 8	Data 7 to 0	-	-	Assert	Assert
Word access at 4n + 2	Data 15 to 8	Data 7 to 0	-	-	Assert	Assert	-	-
Longword access at 4n	Data 31 to 24	Data 23 to 16	Data 15 to 8	Data 7 to 0	Assert	Assert	Assert	Assert

Table 7.7 64-Bit External Bus Access and Data Alignment

	Data Bus								Strobe Signals							
Operation	LPD63 to LPD56	LPD55 to LPD48	LPD47 to LPD40	LPD39 to LPD32	LPD31 to LPD24	LPD23 to LPD16	LPD15 to LPD8	LPD7 to LPD0	LPDQM 7	LPDQM 6	LPDQM 5	LPDQM 4	LPDQM 3	LPDQM 2	LPDQM 1	LPDQM 0
Byte access at 8n + 0	-	-	-	-	-	-	-	Data 7 to 0	-	-	-	-	-	-	-	Assert
Byte access at 8n + 1	-	-	-	-	-	-	Data 7 to 0	-	-	-	-	-	-	-	Assert	-
Byte access at 8n + 2	-	-	-	-	-	Data 7 to 0	-	-	-	-	-	-	-	Assert	-	-
Byte access at 8n + 3	-	-	-	-	Data 7 to 0	-	-	-	-	-	-	-	Assert	-	-	-
Byte access at 8n + 4	-	-	-	Data 7 to 0	-	-	-	-	-	-	-	Assert	-	-	-	-
Byte access at 8n + 5	-	-	Data 7 to 0	-	-	-	-	-	-	-	Assert	-	-	-	-	-
Byte access at 8n + 6	-	Data 7 to 0	-	-	-	-	-	-	-	Assert	-	-	-	-	-	-
Byte access at 8n + 7	Data 7 to 0	-	-	-	-	-	-	-	Assert	-	-	-	-	-	-	-
Word access at 8n + 0	-	-	Data 15 to 8	Data 7 to 0	-	-	Data 15 to 8	Data 7 to 0	-	-	-	-	-	-	Assert	Assert
Word access at 8n + 2	Data 15 to 8	Data 7 to 0	-	-	Data 15 to 8	Data 7 to 0	-	-	-	-	-	-	Assert	Assert	-	-
Word access at 8n + 4	-	-	-	-	-	-	-	-	-	-	Assert	Assert	-	-	-	-
Word access at 8n + 6	-	-	-	-	-	-	-	-	Assert	Assert	-	-	-	-	-	-
Longword access at 8n + 0	-	-	-	-	Data 31 to 24	Data 23 to 16	Data 15 to 8	Data 7 to 0	-	-	-	-	Assert	Assert	Assert	Assert
Longword access at 8n + 4	Data 31 to 24	Data 23 to 16	Data 15 to 8	Data 7 to 0	-	-	-	-	Assert	Assert	Assert	Assert	-	-	-	-

7.5.2 LPDDR2-SDRAM (S4 Standard) Interface

(1) LPDDR2-SDRAM (S4 Standard) Interface

The LPDDR2-S4 device that can be connected to this LSI is a product that has 11/12/13/14/15 bits of row address, 8/9/10/11 bits of column address, and 4/8 banks, and conforms to the JEDEC standard.

The control signals for direct connection of LPDDR2-S4 are LPCLK, /LPCLK, $\overline{\text{LPCSA}}$, LPCA, LPCKEA, and LPCKEB. Signals, except for LPCKEA and LPCKEB, are only valid while $\overline{\text{LPCSA}}$ or $\overline{\text{LPCSB}}$ is asserted. The data bus width of the area that is connected to LPDDR2-S4 can be set as 16 bits, 32 bits, or 64 bits. Depending on the data bus width, part of or all of LPDQM7 to LPDQM0, LPDQS7 to LPDQS0, /LPDQS7 to /LPDQS0, and LPD64 to LPD0 are used.

Commands for LPDDR2-S4 can be specified by the LPCA, LPCKEA, and LPCKEB signals. This LSI issues the following commands to the LPDDR2-S4.

No operation (NOP)

All banks auto-refresh (REFAB)

Self-refresh (SELF)

Deep power-down (DEEP)

All banks precharge (PALL)

Specified bank precharge (PRE)

Bank active (ACTV)

Read (READ)

Read with precharge (READA)

Write (WRIT)

Write with precharge (WRITA)

Write to mode register (MRW)

Read from mode register (MRR)

Table 7.8 Commands for LPDDR2-S4

Command	Description	LPCKE[n]		LPCS[n]	LPCA0	LPCA1	LPCA2	LPCA3	LPCA4	LPCA5	LPCA6	LPCA7	LPCA8	LPCA9	LPCLK EDGE
		PCLK(n-1)	LPCLK(n)												
MRW	Write to mode register	H	H	L	L	L	L	L	MA0	MA1	MA2	MA3	MA4	MA5	↑
					MA6	MA7	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	↓
MRR	Read from mode register	H	H	L	L	L	L	H	MA0	MA1	MA2	MA3	MA4	MA5	↑
					MA6	MA7	X	X	X	X	X	X	X	X	↓
REFA	All banks refresh	H	H	L	L	L	H	H	X	X	X	X	X	X	↑
					X	X	X	X	X	X	X	X	X	X	↓
SELF	Self-refresh	H	L	L	L	L	H	X	X	X	X	X	X	X	↑
					X	X	X	X	X	X	X	X	X	X	↓
ACTV	Active	H	H	L	L	H	R8	R9	R10	R11	R12	BA0	BA1	BA2	↑
					R0	R1	R2	R3	R4	R5	R6	R7	R13	R14	↓
WRIT	Write	H	H	L	H	L	L	L	L	C1	C2	BA0	BA1	BA2	↑
					AP	C3	C4	C5	C6	C7	C8	C9	C10	C11	↓
READ	Read	H	H	L	H	L	H	L	L	C1	C2	BA0	BA1	BA2	↑
					AP	C3	C4	C5	C6	C7	C8	C9	C10	C11	↓
PALL	All banks prechrage	H	H	L	H	H	L	H	H	X	X	X	X	X	↑
					X	X	X	X	X	X	X	X	X	X	↓
PRE	Specified bank precharge	H	H	L	H	H	L	H	L	X	X	BA0	BA1	BA2	↑
					X	X	X	X	X	X	X	X	X	X	↓
DEEP	Deep power-down entry	H	L	L	H	H	L	X	X	X	X	X	X	X	↑
					X	X	X	X	X	X	X	X	X	X	↓
NOP	No operation	H	H	L	H	H	H	X	X	X	X	X	X	X	↑
					X	X	X	X	X	X	X	X	X	X	↓
SELF/DEEP /PD retain	SELF/DEEP /PD retain	L	L	X	H	H	H	X	X	X	X	X	X	X	↑
					X	X	X	X	X	X	X	X	X	X	↓
PDEN	Power-down entry	H	L	H	X	X	X	X	X	X	X	X	X	X	↑
					X	X	X	X	X	X	X	X	X	X	↓
SELF/DEEP /PD EXIT	SELF/DEEP /PD exit	L	H	H	X	X	X	X	X	X	X	X	X	X	↑
					X	X	X	X	X	X	X	X	X	X	↓

The byte to be accessed is specified by LPDQM7 to LPDQM0. Read or write access is performed for a byte whose corresponding LPDQMn is low. For details on the relationship between LPDQM7 to LPDQM0 and the byte to be accessed, refer to section 7.5.1, Access Size and Data Alignment.

Figures 7.2 to 74 show connection examples through the 16-bit, 32-bit, and 64-bit buses, respectively.

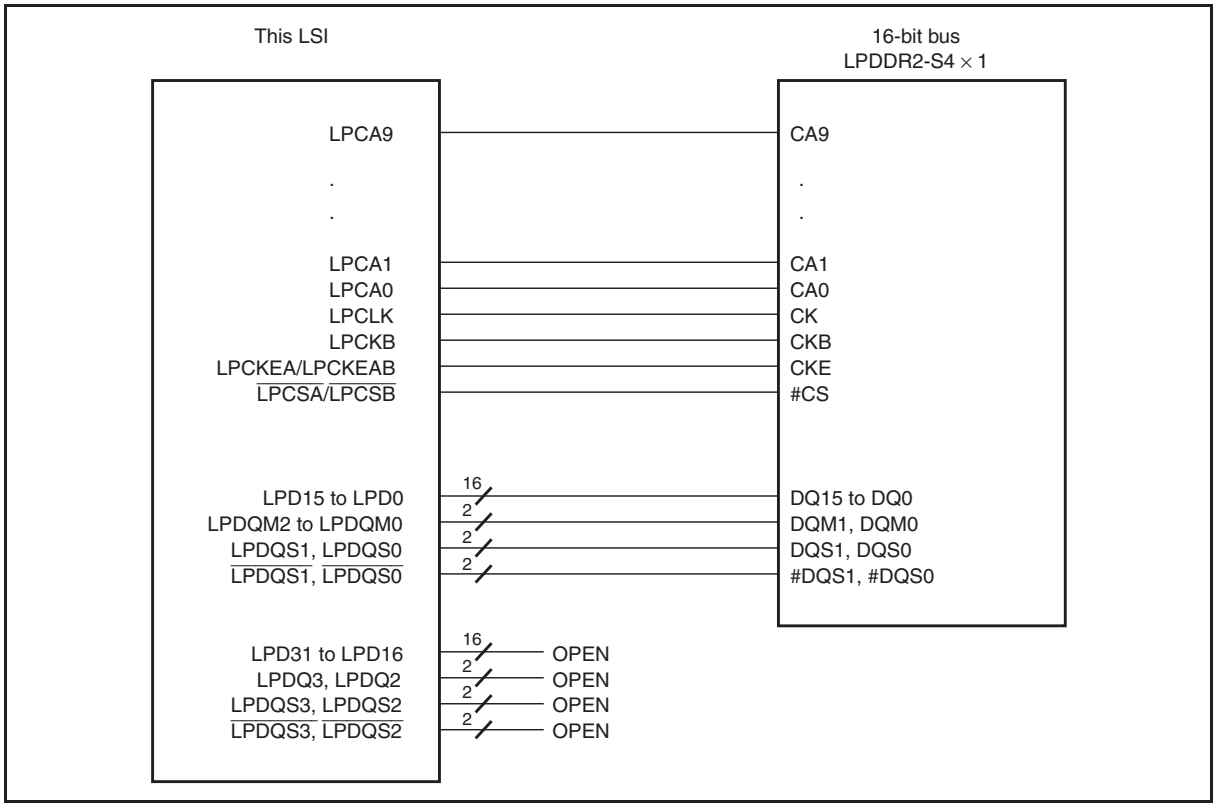


Figure 7.2 Example of Connection with LPDDR2-S4 (16-Bit Data Bus)

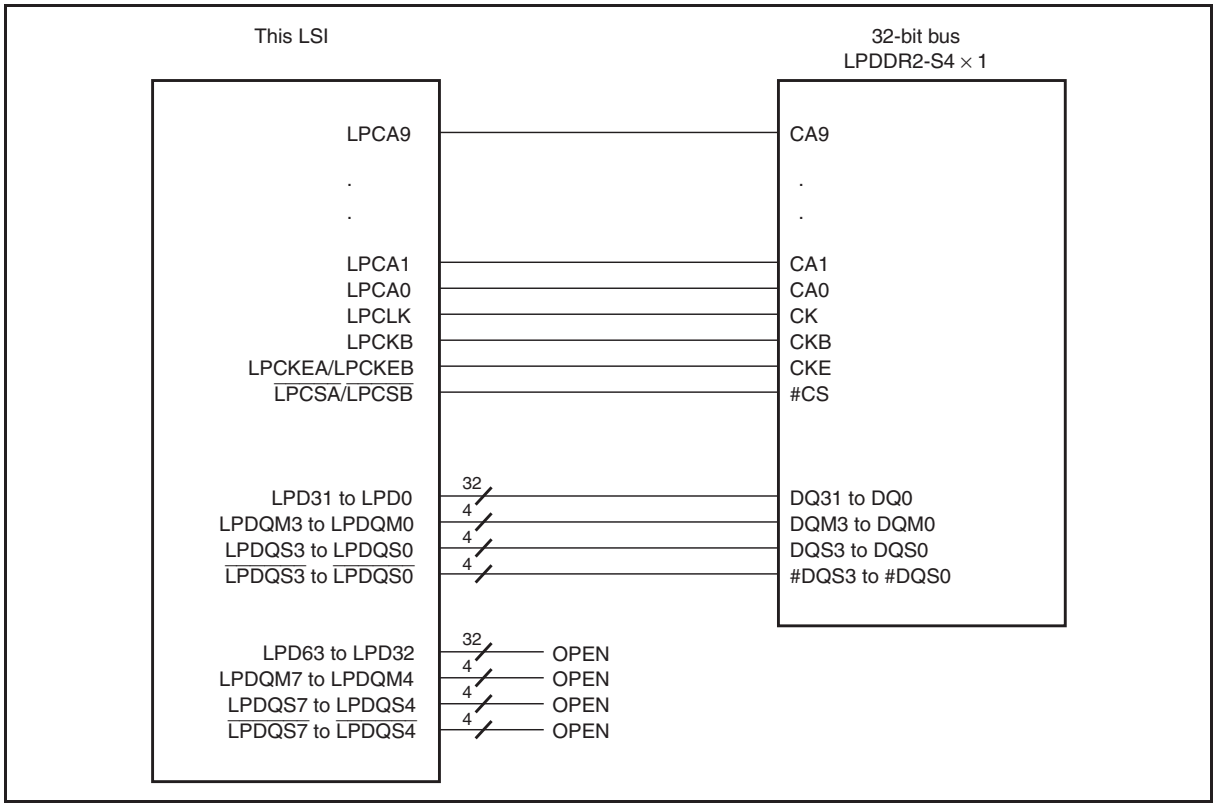


Figure 7.3 Example of Connection with LPDDR2-S4 (32-Bit Data Bus)

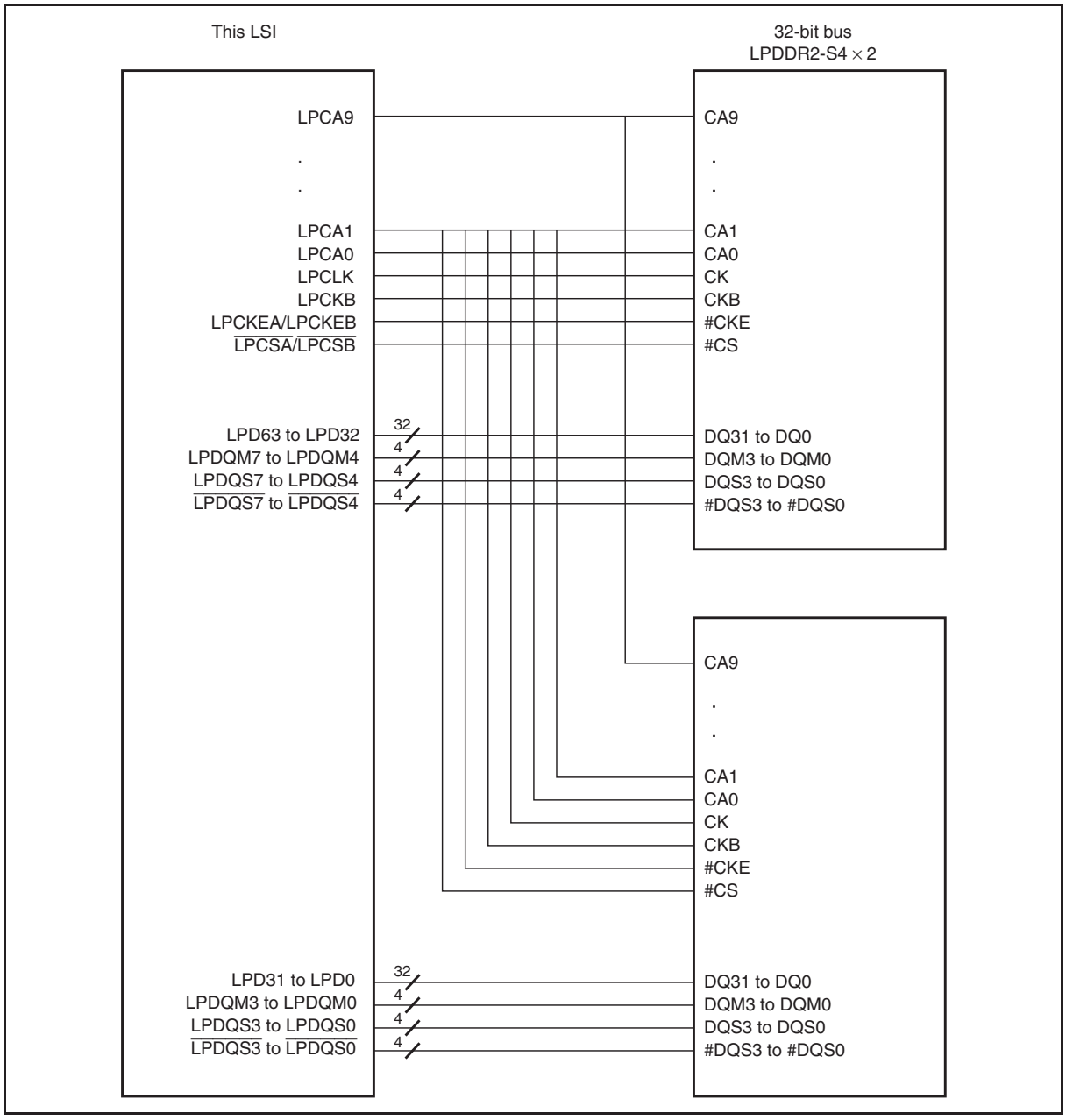


Figure 7.4 Example of Connection with LPDDR2-S4 (64-Bit Data Bus)

(2) Address Multiplexing

Address multiplexing is specified so that the LPDDR2-S4 device can be connected without external address multiplexing circuitry according to the settings of the SZ, BANK, ROW, and COL bits in SDCR0 and SDCR1 and the BAA bits in EBMCR. Tables 7.16 to 7.19 show the relationship between the settings of the SZ, BANK, ROW, COL and BAA bits, the LPDDR2-S4 memory address, and the physical address (Ax) in this LSI.

Connect the CA0 pin of the LPDDR2-S4 to the LPCA0 pin of this LSI, then the CA1 pin to the LPCA1 pin, and so on,

regardless of the data bus width.

Table 7.9 Relationship between SZ, BANK, ROW, COL, and BAA Bits and Address Multiplex Output (1)

SZ = 01 (32 bits)		BANK = 0 (4 banks)		ROW = 13 bits		COL = 9 bits			
BAA = 2'b00		BAA = 2'b01		BAA = 2'b10		BAA = 2'b11		LPDDR2-S4 Function	
Row Address Output Cycle	Column Address Output Cycle	Row Address Output Cycle	Column Address Output Cycle	Row Address Output Cycle	Column Address Output Cycle	Row Address Output Cycle	Column Address Output Cycle	Row Address Output Cycle	Column Address Output Cycle
0	0	0	0	0	0	-	-	BA2	BA2
A25	A25	A25	A25	A12	A12	-	-	BA1	BA1
A24	A24	A11	A11	A11	A11	-	-	BA0	BA0
-	-	-	-	-	-	-	-	R14	-
-	-	-	-	-	-	-	-	R13	-
A23	-	A24	-	A25	-	-	-	R12	-
A22	-	A23	-	A24	-	-	-	R11	C11
A21	-	A22	-	A23	-	-	-	R10	C10
A20	-	A21	-	A22	-	-	-	R9	C9
A19	A10	A20	A10	A21	A10	-	-	R8	C8
A18	A9	A19	A9	A20	A9	-	-	R7	C7
A17	A8	A18	A8	A19	A8	-	-	R6	C6
A16	A7	A17	A7	A18	A7	-	-	R5	C5
A15	A6	A16	A6	A17	A6	-	-	R4	C4
A14	A5	A15	A5	A16	A5	-	-	R3	C3
A13	A4	A14	A4	A15	A4	-	-	R2	C2
A12	A3	A13	A3	A14	A3	-	-	R1	C1
A11	A2	A12	A2	A13	A2	-	-	R0	C0
-	H/L	-	H/L	-	H/L	-	-	-	AP
Connected memory example: 512-Mbit product (4 Mwords x 32 bits x 4 banks, column 9 bits product): 1									

Table 7.10 Relationship between SZ, BANK, ROW, COL, and BAA Bits and Address Multiplex Output (2)

SZ = 00 (16 bits)		BANK = 0 (4 banks)		ROW = 13 bits		COL = 9 bits			
BAA = 2'b00		BAA = 2'b01		BAA = 2'b10		BAA = 2'b11		LPDDR2-S4 Function	
Row Address Output Cycle	Column Address Output Cycle	Row Address Output Cycle	Column Address Output Cycle	Row Address Output Cycle	Column Address Output Cycle	Row Address Output Cycle	Column Address Output Cycle	Row Address Output Cycle	Column Address Output
0	0	0	0	0	0	-	-	BA2	BA2
A24	A24	A24	A24	A11	A11	-	-	BA1	BA1
A23	A23	A10	A10	A10	A10	-	-	BA0	BA0
-	-	-	-	-	-	-	-	R14	-
-	-	-	-	-	-	-	-	R13	-
A22	-	A23	-	A24	-	-	-	R12	-
A21	-	A22	-	A23	-	-	-	R11	C11
A20	-	A21	-	A22	-	-	-	R10	C10
A19	-	A20	-	A21	-	-	-	R9	C9
A18	A9	A19	A9	A20	A9	-	-	R8	C8
A17	A8	A18	A8	A19	A8	-	-	R7	C7
A16	A7	A17	A7	A18	A7	-	-	R6	C6
A15	A6	A16	A6	A17	A6	-	-	R5	C5
A14	A5	A15	A5	A16	A5	-	-	R4	C4
A13	A4	A14	A4	A15	A4	-	-	R3	C3
A12	A3	A13	A3	A14	A3	-	-	R2	C2
A11	A2	A12	A2	A13	A2	-	-	R1	C1
A10	A1	A11	A1	A12	A1	-	-	R0	C0
-	H/L	-	H/L	-	H/L	-	-	-	AP
Connected memory example: 256-Mbit product (4 Mwords x 16 bits x 4 banks, column 9 bits product): 1									

Table 7.11 Relationship between SZ, BANK, ROW, COL, and BAA Bits and Address Multiplex Output (3)

SZ = 01 (32 bits)		BANK = 1 (8 banks)		ROW = 13 bits		COL = 9 bits			
BAA = 2'b00		BAA = 2'b01		BAA = 2'b10		BAA = 2'b11		LPDDR2-S4 Function	
Row Address Output Cycle	Column Address Output Cycle	Row Address Output Cycle	Column Address Output Cycle	Row Address Output Cycle	Column Address Output Cycle	Row Address Output Cycle	Column Address Output Cycle	Row Address Output Cycle	Column Address Output
A26	A26	A26	A26	A26	A26	A13	A13	BA2	BA2
A25	A25	A25	A25	A12	A12	A12	A12	BA1	BA1
A24	A24	A11	A11	A11	A11	A11	A11	BA0	BA0
-	-	-	-	-	-	-	-	R14	-
-	-	-	-	-	-	-	-	R13	-
A23	-	A24	-	A25	-	A26	-	R12	-
A22	-	A23	-	A24	-	A25	-	R11	C11
A21	-	A22	-	A23	-	A24	-	R10	C10
A20	-	A21	-	A22	-	A23	-	R9	C9
A19	A10	A20	A10	A21	A10	A22	A10	R8	C8
A18	A9	A19	A9	A20	A9	A21	A9	R7	C7
A17	A8	A18	A8	A19	A8	A20	A8	R6	C6
A16	A7	A17	A7	A18	A7	A19	A7	R5	C5
A15	A6	A16	A6	A17	A6	A18	A6	R4	C4
A14	A5	A15	A5	A16	A5	A17	A5	R3	C3
A13	A4	A14	A4	A15	A4	A16	A4	R2	C2
A12	A3	A13	A3	A14	A3	A15	A3	R1	C1
A11	A2	A12	A2	A13	A2	A14	A2	R0	C0
-	H/L	-	H/L	-	H/L	-	H/L	-	AP
Connected memory example: 1-Gbit product (8 Mwords x 32 bits x 4 banks, column 9 bits product): 1									

Table 7.12 Relationship between SZ, BANK, ROW, COL, and BAA Bits and Address Multiplex Output (4)

SZ = 10 (64 bits)		BANK = 1 (8 banks)		ROW = 13 bits		COL = 9 bits			
BAA = 2'b00		BAA = 2'b01		BAA = 2'b10		BAA = 2'b11		LPDDR2-S4 Function	
Row Address Output Cycle	Column Address Output Cycle	Row Address Output Cycle	Column Address Output Cycle	Row Address Output Cycle	Column Address Output Cycle	Row Address Output Cycle	Column Address Output Cycle	Row Address Output Cycle	Column Address Output Cycle
A27	A27	A27	A27	A27	A27	A14	A14	BA2	BA2
A26	A26	A26	A26	A13	A13	A13	A13	BA1	BA1
A25	A25	A12	A12	A12	A12	A12	A12	BA0	BA0
-	-	-	-	-	-	-	-	R14	-
-	-	-	-	-	-	-	-	R13	-
A24	-	A25	-	A26	-	A27	-	R12	-
A23	-	A24	-	A25	-	A26	-	R11	C11
A22	-	A23	-	A24	-	A25	-	R10	C10
A21	-	A22	-	A23	-	A24	-	R9	C9
A20	A11	A21	A11	A22	A11	A23	A11	R8	C8
A19	A10	A20	A10	A21	A10	A22	A10	R7	C7
A18	A9	A19	A9	A20	A9	A21	A9	R6	C6
A17	A8	A18	A8	A19	A8	A20	A8	R5	C5
A16	A7	A17	A7	A18	A7	A19	A7	R4	C4
A15	A6	A16	A6	A17	A6	A18	A6	R3	C3
A14	A5	A15	A5	A16	A5	A17	A5	R2	C2
A13	A4	A14	A4	A15	A4	A16	A4	R1	C1
A12	A3	A13	A3	A14	A3	A15	A3	R0	C0
-	H/L	-	H/L	-	H/L	-	H/L	-	AP
Connected memory example: 1-Gbit product (8 Mwords x 32 bits x 4 banks, column 9 bits product): 2									

(3) LPDDR2-S4 Internal Register Access Function

The LPDDR2-S4 device has registers (MR registers) in memory. The SBSC provides an interface for accessing these MR registers. Use the SDMR access function to access the MR registers.

a) Writing to MR Registers

An MR register can be written to through longword or byte write to the 32-bit address (32 {MRSKET11 to MRSKET0, REF_SEL, PADINI, AREASELEN, AREASEL, PALLMSK, 4'b0, TMRWSEL, 8'b0}} shown in table 7.20. According to each bit setting through the write access, an MRW command is issued to the LPDDR2-S4 device and the MR register is written to. The MR register address (MA) and setting data (OP) should be written to SDMRACR0 or SDMRACR1 in advance.

Table 7.13 Writing to MR Register

Bit	Bit Name	Bit Count	Description
31 to 20	MRSKET11 to MRSKET0	12	When setting SBSC1: H'FE5
19	REF_SEL	1	0: Refreshing is not inserted between the PALL and MRW/MRR commands 1: Refreshing is inserted between the PALL and MRW/MRR commands (two times)
18	PADINI	1	Specifies whether to initialize the PAD. 0: An MR register write (MRW) command is issued 1: PAD is initialized When SDMR is written to with this bit set to 1, the MRW command is not issued. To perform a dummy read from the LPDDR2-S4 device to initialize the PAD, the LPDDR2-S4 device should be reset in advance. The PAD should be initialized only after step 9) described in section 7.5.2 (4), Power-On Sequence.
17	AREASELEN	1	MRW Command Issue Area Select Enable For SBSC1: 0: MRW command is issued for both DRAM areas 0 and 1 1: MRW command is issued for the DRAM area selected through the AREASEL bit
16	AREASEL	1	MRW Command Issue Area Select For SBSC1: 0: MRW command is issued for DRAM area 0 1: MRW command is issued for DRAM area 1

Bit	Bit Name	Bit Count	Description
15	REGSEL	1	Specifies the address (MA) and data (OP) for the MRW command to be issued. 0: MA and OP of SDMRACR0 are specified 1: MA and OP of SDMRACR1 are specified
14	PALLMSK	1	PALL Command Issue Select before MRW Command 0: Before the MRW command is issued, the PALL command is issued (PALL -> MRW) 1: Only the MRW command is issued Note: When issuing a RESET command to initialize the LPDDR2, set this bit to 1. In other cases, clear this bit to 0. When setting this bit to 1, be sure to clear the REF_SEL and PADINI bits to 0.
13 to 10	—	2	Reserved These bits should always be 0.
9 to 8	TMRWSEL	2	TMRW Specification Setting These bits should be used only when selecting the tMRW bits that specify the minimum number of cycles between an MRW command for writing to an MR register and the next valid command. These bits are provided assuming the case where the ZQ calibration function of the LPDDR2 memory is used. A different wait cycle setting should be specified in each of the tMRW1 to tMRW3 bits separately for each ZQ calibration type and the register bits to be referenced should be switched through these TMRWSEL bits according to the target ZQ calibration type. 00: tMRW bits in SDWCRC0 are referenced 01: tMRW1 bits in SDWCRC2 are referenced 10: tMRW2 bits in SDWCRC2 are referenced 11: tMRW3 bits in SDWCRC2 are referenced
7 to 0	—	1	Reserved These bits should always be 0.

The following shows some examples of command processing.

To issue a reset command for the LPDDR2-S4 device in DRAM areas 0 and 1 (no PALL command):

1) Write 8'h3F to the MA bits in SDMRACR0.
2) Execute a byte or longword write to address 0xFE500000 (REF_SEL = 0, PADINI = 0, AREASELEN = 0, AREASEL = x, REFSEL = 0, ALLMSK = 1).

To write 0x42 to MR1 of the LPDDR2-S4 device in DRAM area 3
(no refreshing is inserted between PALL and MRW commands and the PAD is not initialized):

1) Write 0x01 to the MA bits and 0x42 to the OP bits in SDMRACR1.
2) Execute a byte or longword write to address 0xFB538000 (REF_SEL = 0, PADINI = 0, AREASELEN = 1, AREASEL = 1, REFSEL = 1, PALLMSK = 0).

To write 0x03 to MR2 of the LPDDR2-S4 device in DRAM areas 2 and 3
(refreshing is inserted between PALL and MRW commands and the PAD is initialized at the same time):

1) Write 0x02 to the MA bits and 0x03 to the OP bits in SDMRACR1.
2) Execute a byte or longword write to address 0xFB5C8000 (REF_SEL = 1, PADINI = 1, AREASELEN = 0, AREASEL = 0, REFSEL = 1, PALLMSK = 0).

When an MRW issue request is generated, the SBSC waits for the end of precharging that is in progress in any bank, and then issues a PALL command to move all banks from active state to precharged state. After that, the SBSC inserts a wait for the number of cycles specified through the TRPAB bits and then issues an MRW command or an REFA command. When the REF_SEL bit is 1, the wait cycles specified through the TRFC bits are inserted after the last REFA command and then an MRW command is issued. The period between the MRW command and the next valid command is determined by the TMRW bit setting.

Figure 7.5 is a waveform when REF_SEL = 0 and PALLMSK = 0, figure 7.6 is a waveform when REF_SEL = 1 and PALLMSK = 0, and figure 7.7 is a waveform when REF_SEL = 0 and PALLMSK = 1.

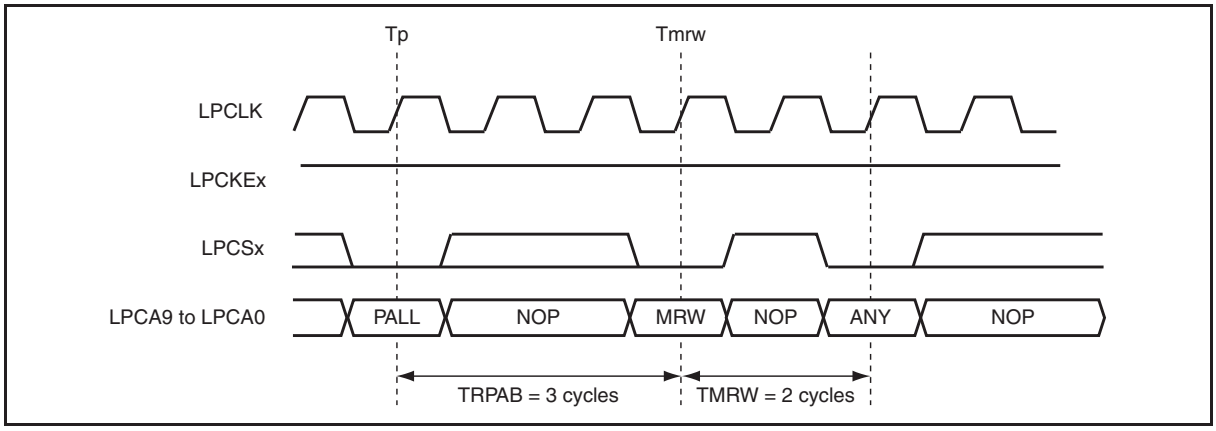


Figure 7.5 Timing Chart of MRW Command Issuing (REF_SEL = 0 and PALLMSK = 0)

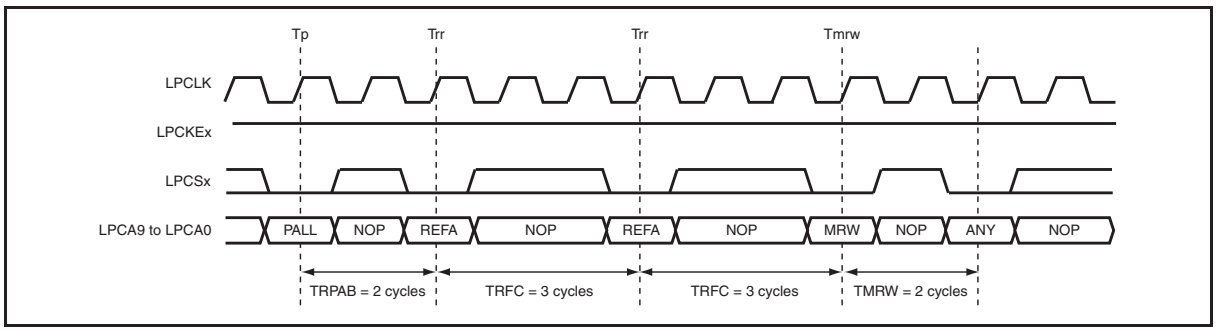


Figure 7.6 Timing Chart of MRW Command Issuing (REF_SEL = 1 and PALLMSK = 0)

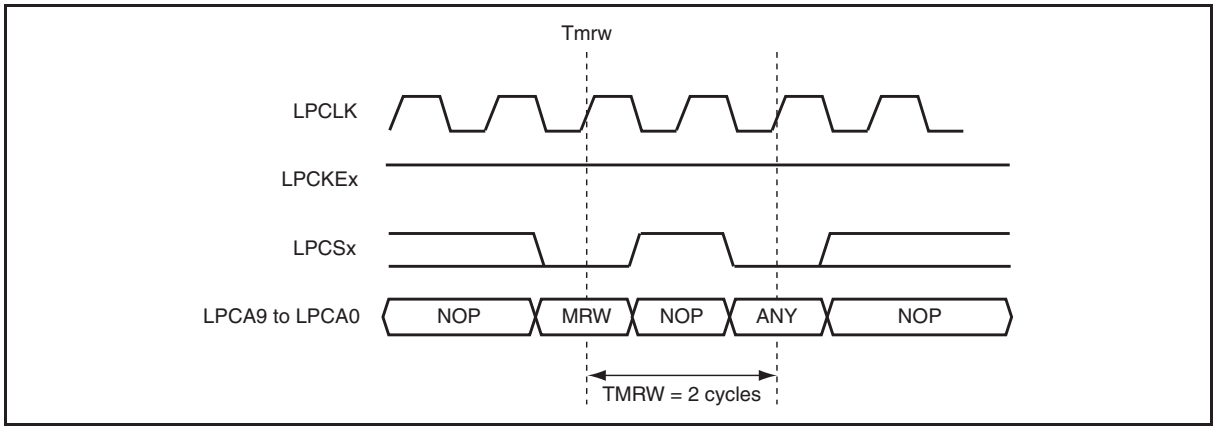


Figure 7.7 Timing Chart of MRW Command Issuing (REF_SEL = 0 and PALLMSK = 1)

b) Reading from MR Registers

An MR register can be read through longword read from the 32-bit address (32{MRSKET11 to MRSKET0, 3'b000, AREASEL, REGSEL, 15'b0}) shown in table 7.14. According to each bit setting through the read access, an

MRR command is issued to the MR register in the LPDDR2-S4 device. The MR register address (MA) and setting data (OP) should be written to SDMRACR0 or SDMRACR1 in advance.

Table 7.14 Reading from MR Register

Bit	Bit Name	Bit Count	Description
31 to 20	MRSKET11 to MRSKET0	12	When setting SBSC1: H'FE5
19 to 17	—	3	These bits should be 0 when the MR register is read.
16	AREASEL	1	MRR Command Issue Area Select For SBSC1: 0: MRR command is issued for DRAM area 0 to read the MR register 1: MRR command is issued for DRAM area 1 to read the MR register
15	REGSEL	1	Specifies the address (MA) and data (OP) for MRW command to be issued. 0: MA and OP of SDMRACR0 are specified 1: MA and OP of SDMRACR1 are specified
14 to 0	—	15	Reserved These bits should always be 0.

Figure 7.8 shows a timing chart of MRR command issuing. When an MRR command issue request is generated, the SBSC waits for the end of precharging that is in progress in any bank, and then issues a PALL command to move all banks from active state to precharged state. After that, the SBSC inserts a wait for the number of cycles specified through the TRPAB bits and then issues an MRR command. The period between the MRR command and data reading from the LPD bus is determined by the RL bit setting. The period between the MRR command and the next valid command is determined by the TMRR bit setting.

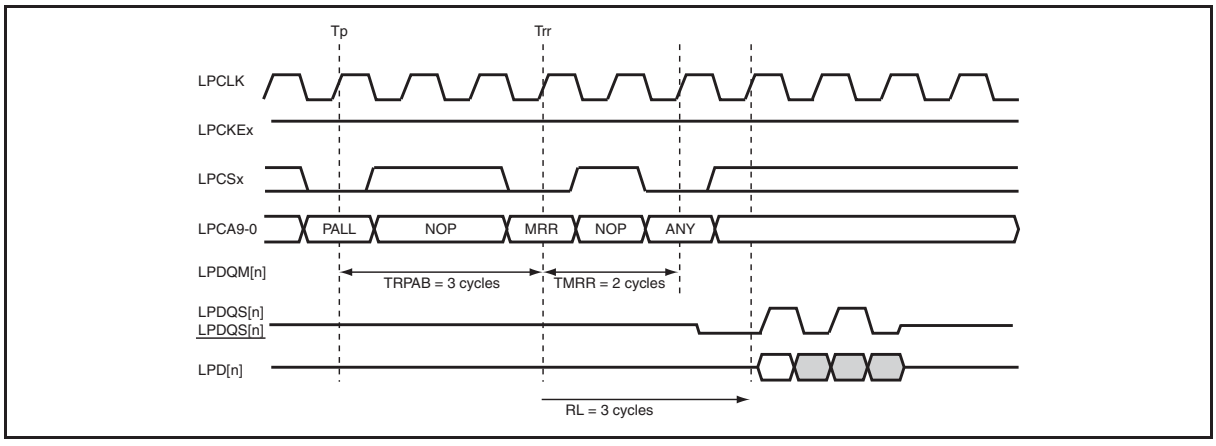


Figure 7.8 Timing Chart of MRR Command Issuing

The LPDDR2-S4 device outputs data read from a register to DQ7 to DQ0. When two x32-bit LPDDR2-S4 devices are

used with 64-bit bus width, data is read from the first LPDDR2-S4 device through LPD7 to LPD0 and from the second LPDDR2-S4 device through LPD39 to LPD32. As the bit position on the LPD bus to be read depends on the memory configuration, the correspondence between the LPD bus bits and the 32-bit read value is specified through the RDSEL3 to RDSEL0 bits in SDMRACR0 or SDMRACR1.

For example, to store 0 in general register bits R[31:16] in the CPU, the value read from the first LPDDR2-S4 device (lower data) in R[7:0], and the value read from the second LPDDR2-S4 device (upper data) in R[15:8], specify RDSEL3 = 0x8, RDSEL2 = 0x8, RDSEL1 = 0x4, and RDSEL0 =0x0 in SDMRACR0 or SDMRACR1. Figure 7.9 shows a schematic diagram of this example.

Table 7.15 shows the correspondence between the SBSC bus width, SDMRACR setting for each memory configuration, and the value read from the CPU when the connected memory provides an MR register read function conforming to the JEDEC LPDDR2-S4 device standard.

Table 7.15 SDMRACR Setting and Value Read from CPU

Memory Configuration			SDMRACR					Value Read from CPU			
Bus Width	DRAM0	DRAM1	RDSEL0	RDSEL1	RDSEL2	RDSEL3	Register Value	R[31:24]	R[23:16]	R[15:8]	R[7:0]
64	64 bits x 1	None	0x0	0x8	0x8	0x8	0x8880XXXX	0x00	0x00	0x00	Valid
	None	64 bits x 1	0x0	0x8	0x8	0x8	0x8880XXXX	0x00	0x00	0x00	Valid
	32 bits x 2	None	0x0	0x4	0x8	0x8	0x8840XXXX	0x00	0x00	Valid	Valid
	None	32 bits x 2	0x0	0x4	0x8	0x8	0x8840XXXX	0x00	0x00	Valid	Valid
32	32 bits x 1	32 bits x 1	0x0	0x8	0x8	0x8	0x8880XXXX	0x00	0x00	0x00	Valid
	32 bits x 1	None	0x0	0x8	0x8	0x8	0x8880XXXX	0x00	0x00	0x00	Valid
	None	32 bits x 1	0x0	0x8	0x8	0x8	0x8880XXXX	0x00	0x00	0x00	Valid
	16 bits x 2	16 bits x 2	0x0	0x2	0x8	0x8	0x8820XXXX	0x00	0x00	Valid	Valid
	16 bits x 2	None	0x0	0x2	0x8	0x8	0x8820XXXX	0x00	0x00	Valid	Valid
	None	16 bits x 2	0x0	0x2	0x8	0x8	0x8820XXXX	0x00	0x00	Valid	Valid
16	16 bits x 1	16 bits x 1	0x0	0x8	0x8	0x8	0x8880XXXX	0x00	0x00	0x00	Valid
	16 bits x 1	None	0x0	0x8	0x8	0x8	0x8880XXXX	0x00	0x00	0x00	Valid
	None	16 bits x 1	0x0	0x8	0x8	0x8	0x8880XXXX	0x00	0x00	0x00	Valid

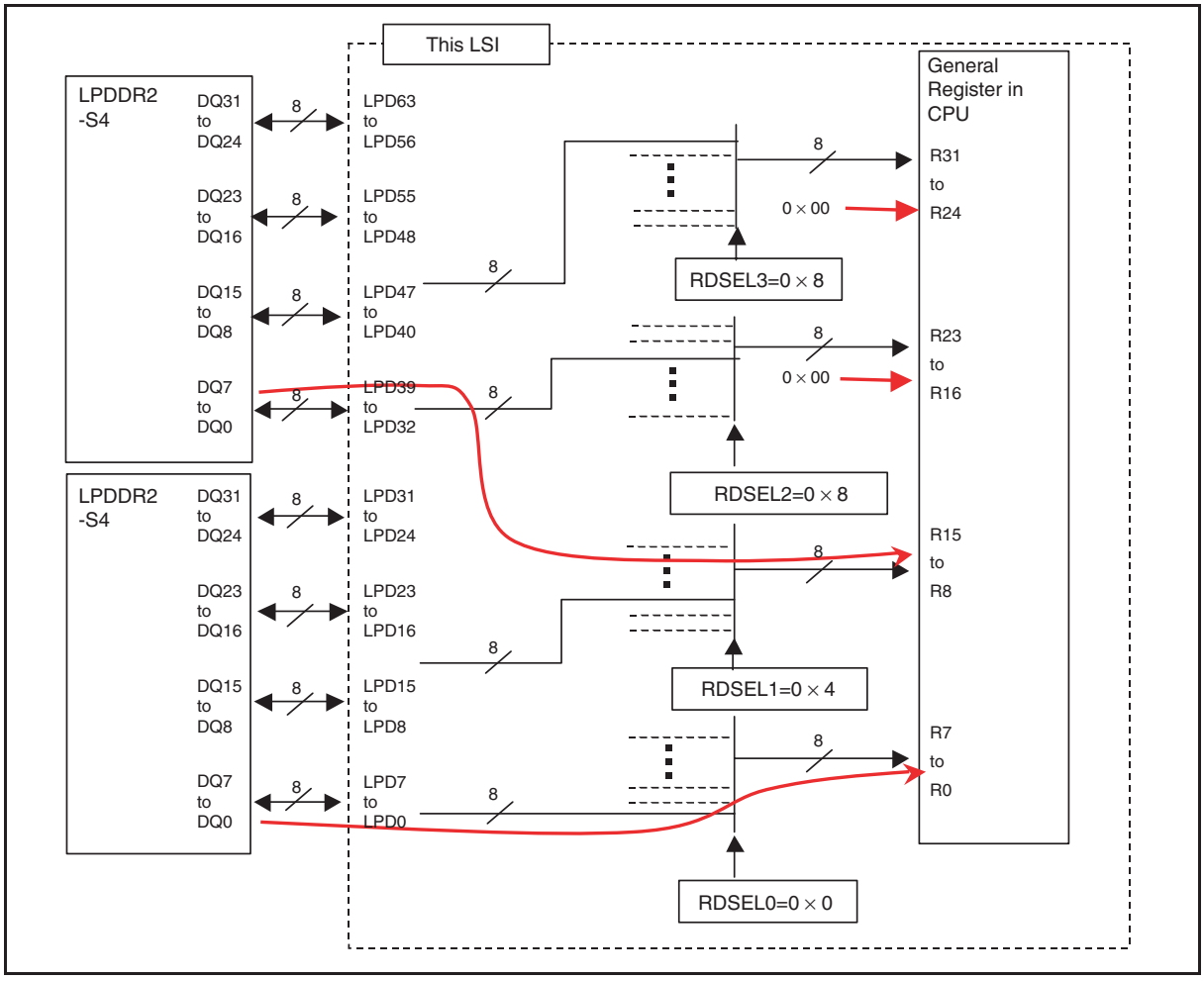


Figure 7.9 Read by MRR when RDSEL3 = 0x8, RDSEL2 = 0x8, RDSEL1 = 0x4, and RDSEL0 = 0x0 in SDMRACR0 or SDMRACR1

(4) Power-On Sequence

To use the LPDDR2-S4 device, reset and mode setting must first be done for the LPDDR2-S4 device after powering on. The following shows an example of this procedure. For details of settings, refer to the data sheet of the target LPDDR2-S4 device.

1) Keep CKE low until power is supplied to all LPDDR2 devices.
   (Refer to the power-supply sequence in the data sheet of the LPDDR2-S4 device.)
2) Set the SBSC1 operating frequency (ZB3ϕ) to a value from 10 MHz to 55 MHz.
3) Enable DLL oscillation in the DDRPHY.
   This setting is unnecessary, if only DDR400 mode is used.
   3.1) Set the DLL operating frequency (DDRPCLKϕ) to a value 300MHz.
   3.2) Set the DLLCYC bit in DLLCNT0A to 0x01AD.
   3.3) Set the DLLMODE[1:0] bit in DLLCNT0A to b01 (DLL oscillation ON always).

4) After specifying the frequency, wait at least 100 ns.
   Insert wait cycles by software, or write the number of cycles corresponding to 100 ns at ZB3ϕ to SDGENCNT and wait until this number becomes 0.
5) Make necessary settings in SBSC1 control registers according to the target LPDDR2 device. Do not specify auto-refreshing, power-down mode, or self-refreshing at this time.
   Note: When the LPDDR2 device to be connected may be changed:
   - Among the memory parameters set in SDCR, the SDSZ, BANK, ROW, and COL bit settings do not need to match the actually-connected memory for a correct power-on sequence.
   - For each wait parameter, the longest wait cycles among the memory devices that may be connected should be specified.
6) Set the CKELV bit in SDPCR to 1 to drive CKE high.
   Before proceeding to the next step, read the CKELV bit to confirm that the bit is set to 1.
7) Wait at least 200 μs by software.
   Insert wait cycles by software, or write the number of cycles corresponding to 200 μs at ZB3ϕ or ZB3Sϕ to SDGENCNT and wait until this number becomes 0.
8) Issue a RESET command to the LPDDR2 device; that is,
   8.1) Write SDMRACRA0 = 0x0000003F.
   8.2) Access SDMR (byte or longword write to address 0xFE500000 consisting of REF_SEL = 0, PADINI = 0, AREALSEEN = 0, AREASEL = 0, REGSEL = 0, and PALLMSK = 1).
9) Wait at least 10 μs(tINIT5) after the end of step 8) before proceeding to step 10).
   Insert wait cycles by software, or write the number of cycles corresponding to 1 μs at ZB3ϕ to SDGENCNT and wait until this number becomes 0.
10) An MRW ZS lnitialzation Calibration commond is issued to the LPDDR2.
   10.1) Write SDMRACRA0 = 0x0000FF0A.
   10.2) Access SDMR (byte or longword write to address 0xFE500000 consisting of REF_SEL = 0, PADINI = 0, AREALSEEN = 0, AREASEL = 0, REGSEL = 0, and PALLMSK = 1).
11) Wait at least 1 μs(tZQINIT) after the end of step 10) before proceeding to step 12).
   Insert wait cycles by software, or write the number of cycles corresponding to 1 μs at ZB3ϕ to SDGENCNT and wait until this number becomes 0.
12) Specify the operating mode through MR registers in the LPDDR2. The following shows an example of MR1/2 setting.
   12.1) Write SDMRACRA0 = 0x00002201 (nWR = 3'b001, WC = 1'b0, BT = 1'b0, and BL = 3'b010)
   12.2) Access SDMR (byte or longword write to address 0xFE500000 consisting of REF_SEL = 0, PADINI = 0, AREALSEEN = 0, AREASEL = x, REGSEL = 0, and PALLMSK = 0).
   12.3) Write SDMRACRA0 = 0x00000302(DDR600mode) or 0x00000102(DDR400mode).
   (RL&WL=RL3/WL1(DDR400mode)orRL5/WL2(DDR600mode)
   12.4) Access SDMR (byte or longword write to address 0xFE500000 consisting of REF_SEL = 0, PADINI = 0, AREALSEEN = 0, AREASEL = x, REGSEL = 0, and PALLMSK = 0).
13) Initialize the DDR I/F section of this LSI.
   Access SDMR (byte or longword write to address 0xFE5C0000 consisting of REF_SEL = 1, PADINI = 1, AREALSEEN = 0, AREASEL = x, REGSEL = 0, and PALLMSK = 0).
14) Initialization of the LPDDR2 device is completed.
15) Specify the following through SBSC registers.
   15.1) Temperature sensor control
   15.2) Auto-refreshing control
   15.3) Memory protection settings
   15.4) Power-down mode control

16) Select DLL mode.
This setting is unnecessary, if only DDR400 mode is used.

17) Set the SBSC1 operating frequency to a desired value.

(5) Refreshing

The SBSC has a function for controlling LPDDR2-S4 refreshing. Auto-refreshing can be performed by clearing the RMODE bit to 0 and setting the RFSH bit to 1 in SDCR0. A continuous refreshing can be performed by setting the RRC bits in RTCSR. If SDR-SDRAM is not accessed for a long period, self-refresh mode, in which power consumption is low, can be activated by setting both the RMODE bit and RFSH bit to 1.

(a) Auto-Refreshing

The number of times of refreshing set by the RRC bits in RTCSR is performed at intervals determined by the input clock selected by the CKS bits in RTCSR and the value set in RTCOR. Register settings should be made so as to satisfy the refresh interval stipulation for the LPDDR2-S4 used. First make the settings for RTCOR, RTCNT, and the RMODE and RFSH bits in SDCR0, then make the settings for the CKS and RRC bits in RTCSR. When the input clock is selected by the CKS bits, RTCNT starts counting up from the value at that time. The RTCNT value is constantly compared with the RTCOR value, and when the two values become the same, a refresh request is generated and auto-refreshing is performed for the number of times specified by the RRC bits. At the same time, RTCNT is cleared to 0 and restarts count-up.

Figure 7.10 shows the auto-refresh cycle timing. After starting auto-refreshing, the PALL command is issued in the Tp cycle to move all banks from the active state to the precharged state after completion of precharging that is in progress in any bank. The REFA command is then issued in the Trr cycle after inserting idle cycles of which number is specified by the TRP bits. A new command is not issued for the duration of the number of cycles specified by the TRFC bits after the Trr cycle. The TRFC bits must be set so as to satisfy the LPDDR2-S4 refreshing cycle time stipulation (t_{RFC}). An NOP cycle is inserted between the Tp cycle and Trr cycle when the value set in the TRP bits is two or more cycles.

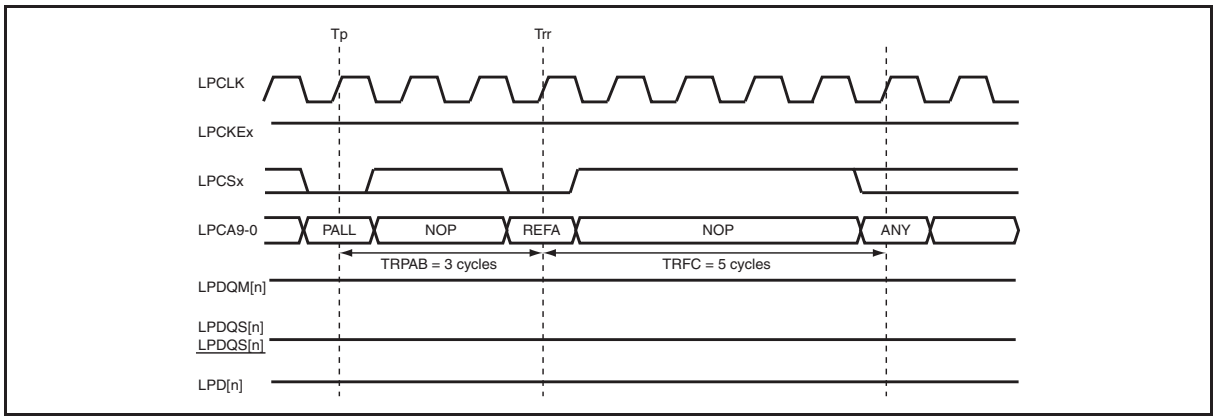


Figure 7.10 Auto-Refresh Timing (SDCR0.RMODE = 0, RFSH = 1, TRPAB= 2 (3 cycles), TRFC = 4 (5 cycles))

(b) Automatic Switching of Auto-Refresh Rate

The SBSC has a function for selecting one of four RTCORx registers to be referenced to determine the refresh rate

according to the SBSC operation clock frequency (ZB3φ) and the LPDDR2-S4 internal temperature. Four RTCOR registers are used for the following purposes.

RTCOR: Referenced when the SBSC clock is set to high-speed clock mode and the temperature sensor indicates a normal temperature

RTCORH: Referenced when the SBSC clock is set to high-speed clock mode and the temperature sensor indicates a high temperature

RTCOSR: Referenced when the SBSC clock is set to low-speed clock mode and the temperature sensor indicates a normal temperature

RTCOSRH: Referenced when the SBSC clock is set to low-speed clock mode and the temperature sensor indicates a high temperature

The frequency synchronization control function is enabled by setting the FRQSEL bit to 1 in RTCSR. There are two clock modes, high-speed mode and low-speed clock mode, and the mode is determined by the division ratio of the SBSC operation clock frequency specified in the CPG and the PLLC1 status. Table 7.16 shows the clock mode conditions. When FRQSEL = 0, RTCOR or RTCORH (selected according to the temperature) is referenced. When FRQSEL = 1, RTCOR or RTCORH (selected according to the temperature) is referenced in high-speed clock mode, and RTCORS or RTCORSH (selected according to the temperature) is referenced in low-speed clock mode.

Table 7.16 SBSC Operation Clock Modes

SBSC1	Mode	Condition
SBSC1	High-speed clock mode	ZB3φ = 1/6 division (or higher) and PLLC1 is enabled
	Low-speed clock mode	ZB3φ = 1/8 division (or lower) or PLLC1 is disabled

The following describes the refresh rate switching control function according to the LPDDR2-S4 internal temperature.

This function is enabled by setting the TMPEN bit to 1 in RTCSR. When TMPEN = 0, RTCOR or RTCORS (selected according to the operation clock mode) is referenced. When TMPEN = 1, RTCORH or RTCORSH (selected according to the operation clock mode) is referenced at a high temperature, and RTCOR or RTCORS (selected according to the operation clock mode) is referenced at a normal temperature.

The LPDDR2-S4 internal temperature is indicated in the Device Temperature register (MR4) in the LPDDR2-S4. The SBSC reads the temperature from MR4 with the same timing as auto-refreshing. The SBSC then stores the read data in SDMRTMPMON, masks the data with the value specified in SDMRTMPMSK in bit units, and ORs all bits of the obtained data into a value to determine whether the LPDDR2-S4 internal temperature is normal (all-ORed value is 0) or high (all-ORed value is 1).

The temperature synchronization control function should be specified as follows.

1) Specify in the MA bits in SDMRTMPCR the address of the register that indicates the LPDDR2-S4 internal temperature.
2) Specify in the RDSEL0 and RDSEL1 bits in SDMRTMPCR the LPD bus bits where the MR register value read from the LPDDR2-S4 connected to DRAM area 0 or 2 is output. When no LPDDR2-S4 is connected to DRAM area 0 or 2, set both RDSEL0 and RDSEL1 to 0x8, or when only one memory is connected to either DRAM area 0 or 2, set RDSEL1 to 0x8, so that 0x00 is always stored in the corresponding bits.
3) Likewise, specify in the RDSEL2 and RDSEL3 bits in SDMRTMPCR the LPD bus bits where the MR register value read from the LPDDR2-S4 connected to DRAM area 1 or 3 is output. When no LPDDR2-S4 is connected to DRAM area 1 or 3, set both RDSEL2 and RDSEL3 to 0x8, or when only one memory is connected to either DRAM area 1 or 3, set RDSEL1 to 0x8, so that 0x00 is always stored in the corresponding bits. SDMRTMPMSK is a register that selects the bits used to determine whether the temperature is high or normal. Only the bits used for judgment should be set to 1.

Figure 7.11 gives an overview of sample setting and operation when an LPDDR2-S4 device with a 32-bit bus width is connected to DRAM area 2 through the LPB bus and an LPDDR2-S4 device with a 32-bit bus width is connected to DRAM area 3.

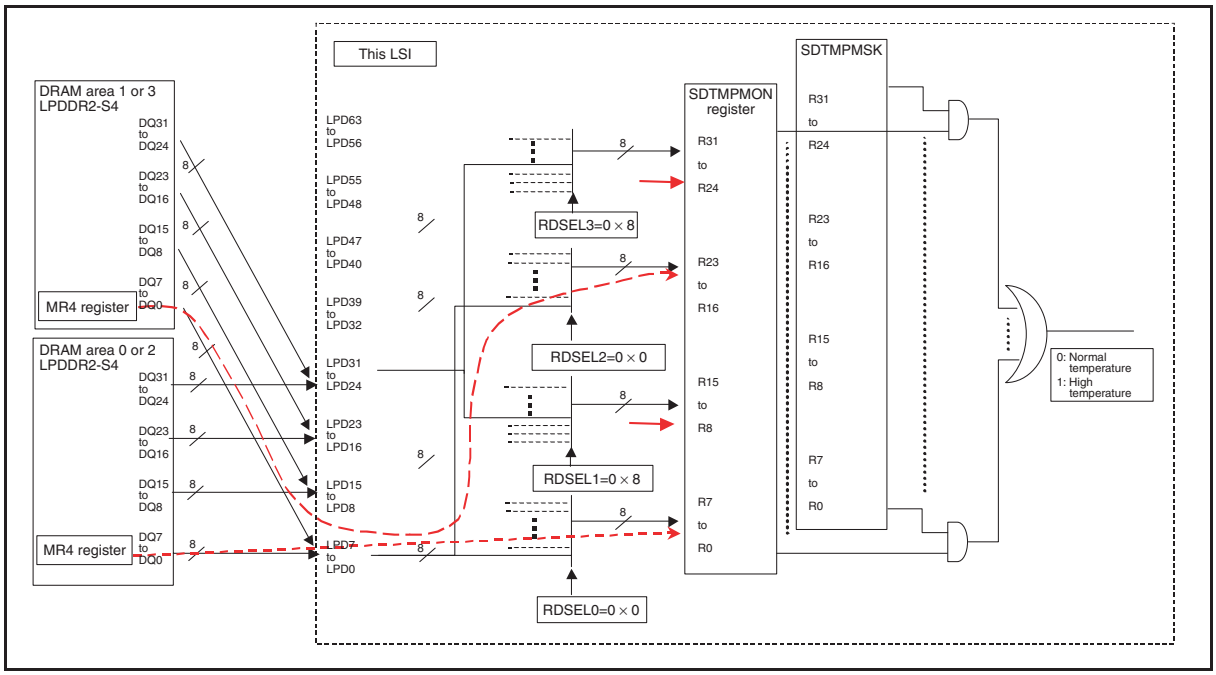


Figure 7.11 Temperature Control Operation Overview

Table 7.24 shows examples of SDTMPCR and SDTMPMSK register settings corresponding to the SBSC bus width and

memory configuration for the Device Temperature register (MR4) conforming to the JEDEC LPDDR2-S4 device standard.

Table 7.17 SDTMPCR and SDTMPMSK Setting Examples

Memory Configuration			SDMRTMPCR						SDMRTMPMSK
Bus Width	DRAM0	DRAM1	MA	RDSEL0	RDSEL1	RDSEL2	RDSEL3	Register Value	Register Value
64	64 bits x 1	None	0x04	0x0	0x8	0x8	0x8	0x88800004	0x00000004
	None	64 bits x 1	0x04	0x8	0x8	0x0	0x8	0x80880004	0x00040000
	32 bits x 2	None	0x04	0x0	0x4	0x8	0x8	0x88400004	0x00000404
	None	32 bits x 2	0x04	0x8	0x8	0x0	0x4	0x40880004	0x04040000
32	32 bits x 1	32 bits x 1	0x04	0x0	0x8	0x0	0x8	0x80800004	0x00040004
	32 bits x 1	None	0x04	0x0	0x8	0x8	0x8	0x88800004	0x00000004
	None	32 bits x 1	0x04	0x8	0x8	0x0	0x8	0x80880004	0x00040000
	16 bits x 2	16 bits x 2	0x04	0x0	0x2	0x0	0x2	0x20200004	0x04040404
	16 bits x 2	None	0x04	0x0	0x2	0x8	0x8	0x88200004	0x00000404
	None	16 bits x 2	0x04	0x8	0x8	0x0	0x2	0x20880004	0x04040000
16	16 bits x 1	16 bits x 1	0x04	0x0	0x8	0x0	0x8	0x80800004	0x00040004
	16 bits x 1	None	0x04	0x0	0x8	0x8	0x8	0x88800004	0x00000004
	None	16 bits x 1	0x04	0x8	0x8	0x0	0x8	0x80880004	0x00040000

(c) Self-Refreshing

Self-refresh mode is a kind of standby mode in which the refresh timing and refresh addresses are generated within the LPDDR2-S4. Self-refreshing is activated by setting both the RMODE bit and RFSH bit in SDCR0 to 1. After starting self-refreshing, the PALL command is issued in the Tp cycle after completion of precharging that is in progress in any bank. The SELF command is then issued in the Tsr cycle after inserting idle cycles of which number is specified by the TRPAB bits. The LPDDR2-S4 cannot be accessed in the self-refresh state. Self-refresh mode is canceled by clearing the RMODE bit to 0. After self-refresh mode has been canceled, command issuance is disabled for the number of cycles specified by the TSREX bits.

Self-refresh timing is shown in figure 7.12. After self-refreshing is canceled, settings must be made so that auto-refreshing is performed immediately at the correct intervals. When self-refreshing is activated from the state in which auto-refreshing is set, auto-refreshing is restarted if the RFSH bit is set to 1 and the RMODE bit is cleared to 0 when self-refresh mode is cleared. If the transition from clearing of self-refresh mode to the start of auto-refreshing takes time, making the RTCNT value 1 less than the RTCOR value will enable auto-refreshing to be started immediately.

The SBSC stops LPCLK and /LPCLK in self-refresh mode to reduce the I/O current of this LSI. The stop timing is one clock cycle after the SELF command is issued (Tsr) and the start timing is five clock cycles before self-refresh mode is cleared (Tsrexit).

After self-refreshing has been set, the self-refresh state continues even if this LSI enters the standby state and is maintained even after wakeup from standby state due to an interrupt. After a power-on reset, the LPCKEA and LPCKEB pins need to be driven low to continue self-refreshing (see section 7.5.2 (10), Initial Value of LPCKEA/LPCKEB Pin Level).

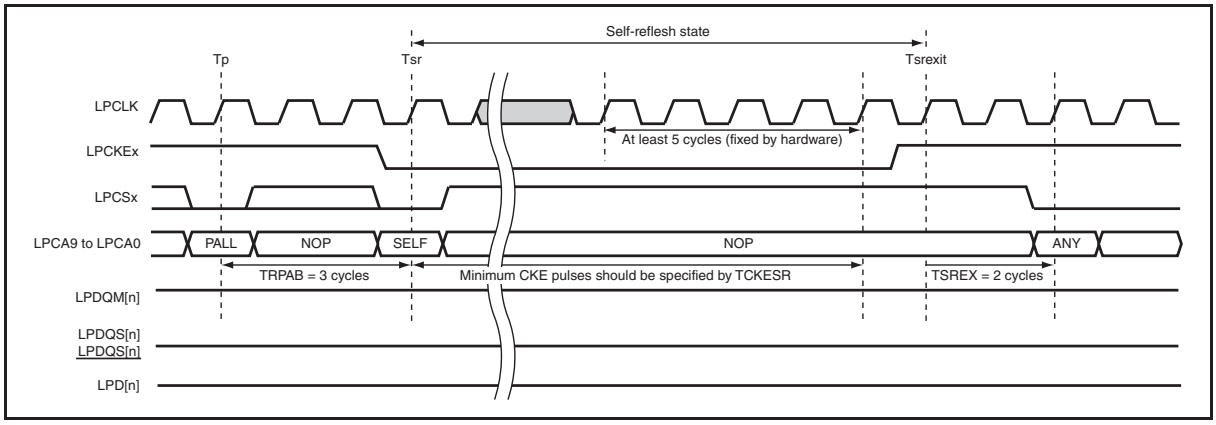


Figure 7.12 Self-Refresh Timing
(SDCR0.RMODE = 1, RFSH = 1, TRPAB = 2 (3 cycles), TSREX = 1 (2 cycles))

(d) Burst-Refreshing after Exit from Self-Refreshing

Some LPDDR2-S4 devices require that auto-refreshing be performed a specified number of times after they are taken out of self-refresh mode. To support such devices, this LSI has a function for issuing a specified number of consecutive refresh commands after the LPDDR2-S4 has been taken out of self-refresh mode. This is called "burst refreshing". No other commands are issued while burst refreshing is in progress.

Setting SREFCNT to 1 or a greater value before the LPDDR2-S4 is placed in self-refresh mode selects auto-refreshing the specified number of times after the LPDDR2-S4 is taken out of self-refresh mode. Furthermore, setting the SREF_PRE bit in SDCR0 to 1 selects issuing of the precharge command (PALL) before the issuance of REF commands the number of times set in SREFCNT.

Figure 7.13 shows the timing when the LPDDR2-S4 is taken out of self-refresh mode when SREFCNT has been set to a value greater than or equal to 1 and the SREF_PRE bit has been cleared to 0. Figure 7.14 shows the timing when the LPDDR2-S4 is taken out of self-refresh mode when SREFCNT has been set to a value greater than or equal to 1 and the SREF_PRE bit has been set to 1. Note that no refresh commands will be issued if SREFCNT is set to 0. For the operation in this case, see section 7.5.2 (5) (c), Self-Refreshing.

With the SREF_PRE bit cleared to 0, the LPDDR2-S4 leaves self-refresh mode in the Tsrexit cycle where LPCKEA/LPCKEB is driven high. After that, the number of idle cycles specified by the TSREX bits are inserted, and the first REFA command is issued in the Trr cycle. The number of idle cycles specified by the TRFC bits are then inserted before all subsequently issued REFA commands. After the last REFA command has been issued, no further commands are issued for the number of cycles specified by the TRFC bits. With the SREF_PRE bit set to 1, the LPDDR2-S4 leaves self-refresh mode in the Tsrexit cycle, the number of idle cycles specified by the TSREX bits are inserted, and the all-bank precharge command (PALL) is issued in the Tp cycle. After that, the number of idle cycles specified by the TRFC bits are inserted, and the first REFA command is issued in the Trr cycle. The number of idle cycles specified by the TRFC bits are then inserted before all subsequently issued REFA commands. After the last REFA command has been issued, no further commands are issued for the number of cycles specified by the TRFC bits.

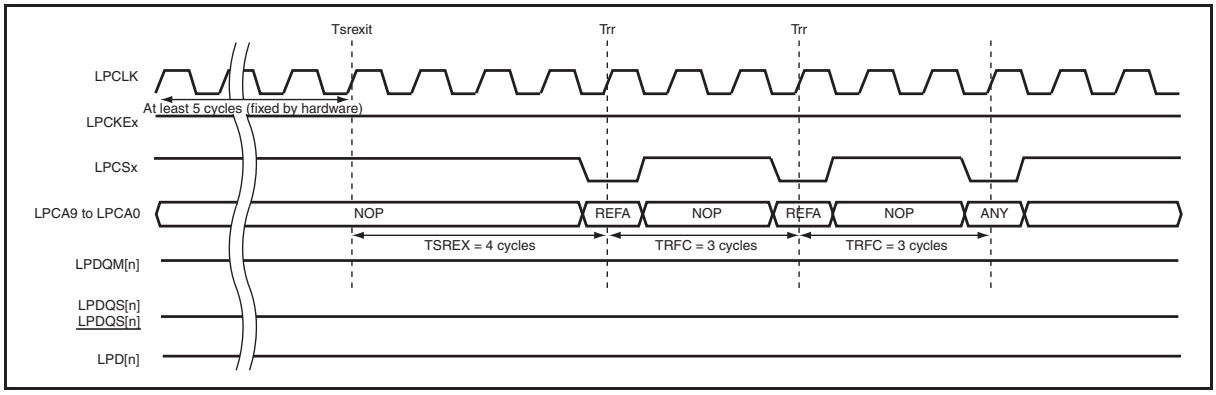


Figure 7.13 Burst-Refreshing after Exit from Self-Refresh Mode (1)
(SREFCNT = 2 (twice), SDCR0.SREF_PRE = 0, TSREX = 3 (4 cycles), TRFC = 2 (3 cycles))

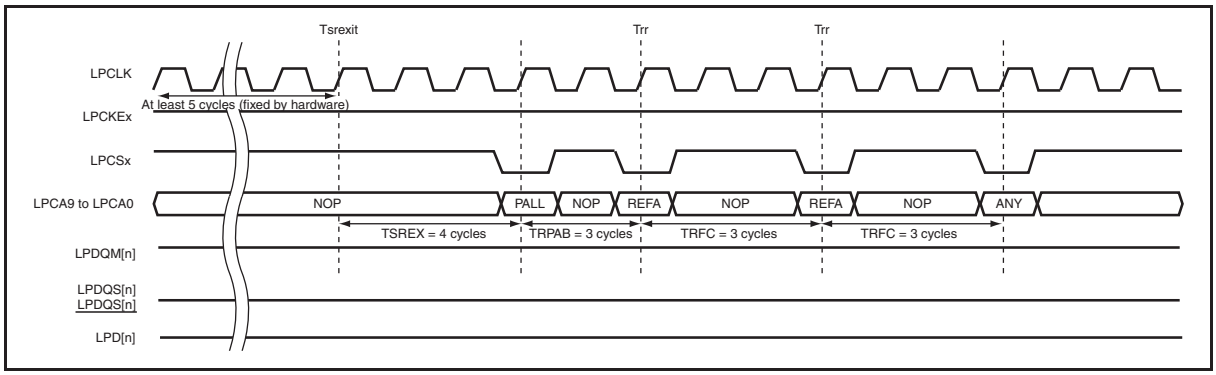


Figure 7.14 Burst-Refreshing after Exit from Self-Refresh Mode (2)
(SREFCNT = 2 (twice), SDCR0.SREF_PRE = 1, TSREX = 3 (4 cycles), TRPAB = 1 (2 cycles), TRFC = 2 (3 cycles))

Precautions:

1. Settings of SREFCNT and the SREF_PRE bit in SDCR0 should be made before the LPDDR2-S4 is placed in self-refresh mode.
2. The LPDDR2-S4 can be taken out of self-refresh mode by writing 1 to the RMODE bit in SDCR0. When writing to this bit, be careful not to change the value of bit SREF_PRE.

(e) Procedures for Controlling Transition to or Exit from Self-Refresh Mode

The following gives restrictions and notes on control of the SBSC and connected LPDDR2-S4 at transition to or exit from self-refresh mode. Use the control procedures given below. When stopping the clock supply (stopping the source clock) to the SBSC after transition to self-refresh mode, specify self-refreshing through the RMODE bit in SDCR0 or cut the power supply to the SBSC area by setting PDSEFL = 1 and RFSH = 1 in SDCR0 so that the LPDDR2-S4 is in self-refresh state. This section describes the procedures for using the RMODE bit in SDCRx for self-refresh control.

- Procedure for controlling transition to self-refresh mode
  1. Stop access to the LPDDR2-S4 in the target memory space to be set to self-refresh mode. This must be controlled by software. If an access is made to the memory space that is in self-refresh mode, the SBSC will return an error.
  2. Write 1 to the RMODE and RFSH bits in SDCR0 that controls the target memory space to set it to self-refresh mode.

     Note: If 1 is written to the DEEP bit before or at the same time as 1 is written to the RMODE bit, the LPDDR2-S4 in the corresponding memory space is moved to deep power-down mode.

     To specify partial self-refreshing of the LPDDR2-S4, use the registers in the LPDDR2-S4. For details, refer to the data sheet of the LPDDR2-S4 device.

- Procedure for controlling exit from self-refresh mode
  1. Check that the power is turned on in the SBSC power-supply area (SBSC1: A4S).
  2. Write 0 to the RMODE bit in SDCRx that controls the target memory space to clear self-refresh mode for the memory space.
  3. Restart access to the LPDDR2-S4.

(f) Control of Automatic Transition to Self-Refresh Mode while PLLC1 is Off

While the PLLC1 in this LSI is turned off, the frequency of the SBSC clock (ZB3ϕ or ZB3Sϕ) is low (the frequency depends on the input clock and frequency division ratio) and auto-refreshing is not performed at the necessary rate. To avoid this, self-refresh mode should be specified through the RMODE bit in SDCRx, but in some systems self-refreshing cannot be correctly controlled by software. Assuming such a case, the SBSC provides a function for controlling self-refreshing in synchronization with the PLLC1 status (on or off). This function is enabled by setting the PLLCNT bit to 1 in SDCR0.

- Operation when PLLCNT == 0:

  Auto-refreshing continues while the PLLC1 is turned off. During the period in which the PLLC1 might be turned off, the memory should be placed in self-refresh mode through the RMODE bit setting in SDCRx to avoid data loss due to an insufficient refreshing rate.

- Operation when PLLCNT==1:

  The SDRAM is placed in self-refresh mode while the PLLC1 is turned off. Upon detecting the processing that turns off the PLLC1, the SBSC automatically moves the SDRAM to self-refresh mode. Upon detecting the processing that turns on the PLLC1, the SBSC automatically releases the SDRAM from self-refresh mode.

  Note that when the SDRAM has been moved to self-refresh mode through the RMODE bit setting in SDCRx, self-refreshing continues regardless of PLLC1 transition to the on or off state.

If the SBSC memory space is accessed (including the registers in the SDRAM) while this automatic transition function is enabled and the PLLC1 is off, the SBSC will return an access error and an abort is generated in the CPU.

Figure 7.15 shows the relationship between PLLC1 state transition (on or off) and self-refreshing when PLLCNT = 1.

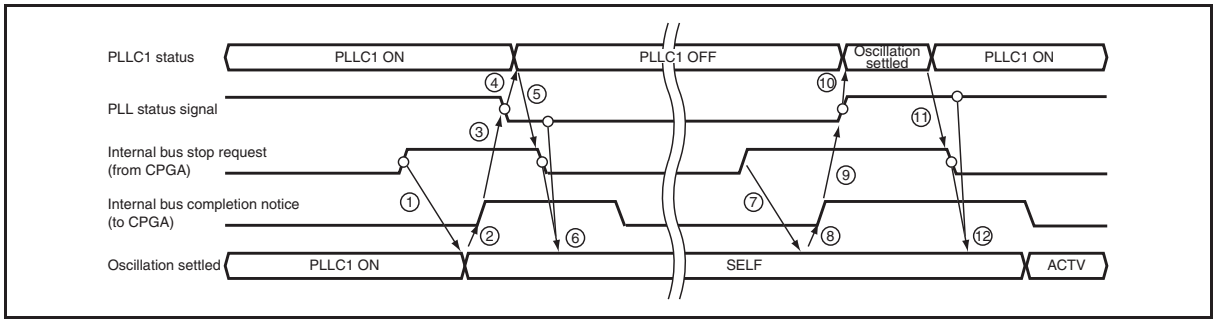


Figure 7.15 Relationship between PLLC1 State Transition (On or Off) and Self-Refreshing

Description:

1. Upon detecting a turn-off request for the PLLC1, the CPGA sends an internal bus stop request to each module.
2. Upon receiving the internal bus stop request from the CPGA, the SBSC moves to self-refresh mode. After completion of transition to self-refresh mode, the SBSC returns an internal bus stop completion notice to the CPGA.
3. After all modules have returned an internal bus stop completion notice, the CPGA instructs the PLLC1 to stop oscillation.
4. Upon receiving the instruction, the PLLC1 stops oscillation.
5. After the PLLC1 has stopped, the CPGA negates the internal bus stop request to each module.
6. When the internal bus stop request is negated, the SBSC checks the PLL status signal. Here, the PLLC1 status signal indicates the off state and the SBSC continues self-refreshing.
7. Upon detecting a turn-on request for the PLLC1, the CPGA sends an internal bus stop request to each module.
8. Upon receiving the internal bus stop request form the CPGA, the SBSC checks its state. When the SBSC state is self-refresh mode, the SBSC returns an internal bus stop completion notice to the CPGA immediately.
9. After all modules have returned an internal bus stop completion notice, the CPGA instructs the PLLC1 to start oscillation.
10. Upon receiving the instruction, the PLLC1 starts oscillation.
11. After checking that the PLLC1 has started oscillation, the CPGA negates the internal bus stop request to each module.
12. When the internal bus stop request is negated, the SBSC checks the PLL status signal. Here, the PLL status signal indicates the on state, and the SBSC clears self-refreshing mode.

(6) Relationship between Refresh Requests and Bus Cycles

If a refresh request occurs during bus cycle execution, the refresh cycle must wait for the bus cycle to be completed.

If a new refresh request occurs while waiting for the previous refresh request, the previous refresh request is deleted. To perform refreshing correctly, a bus cycle longer than the refresh interval or the bus mastership occupation must be prevented from occurring.

(7) Power-Down Modes

This LSI has three types of power-down modes that can be selected by the PDOWN bits in SDCR0. When the PDOWNSEL bit in SDPDCR0 is set to 1, the PDOWN bit setting of SDCR0 is compared with the PDOWN bit setting of SDCR1, and the power-down mode with the smaller access latency is selected.

The access latency order for power-down modes is as follows:

Normal operation < Power-down mode 1 < Power-down mode 2 < Power-down mode 3

Power-down mode 3 has the largest access latency.

Refer to section 7.5.2 (9), Power-Down Control Using LPCKEA/LPCKEB Pin, for operation with the PDOWNSEL bit in SDPDCR0 set to 1.

The SBSC stops the LPCLK and /LPCLK clock output in power-down mode or self-refresh mode to reduce the current flowing in the I/O section of the SBSC. The earliest oscillation stop timing is one clock cycle after transition to power-down mode or self-refresh mode (CKE is driven low) and the latest oscillation start timing is five clock cycles before power-down mode or self-refresh mode is cleared (CKE is driven high).

Note on Power-Down Mode Switching:

When the connected SDRAM is set to self-refresh mode through the RMODE and RFSH bit settings in SDCRx, do not change power-down mode through the PDMODE bit (when the SDRAM is not actually in self-refresh state, the power-down mode can be switched because of register arbitration).

When only one of DRAM areas 0 and 1 in the SBSC1 is in self-refresh state, the power-down mode can be switched.

(a) Power-Down Mode 1

If the PDOWN1 and PDOWN0 bits in SDCR0 are set to B'10, the LPDDR2-S4 is placed in power-down mode by setting the LPCKEA/LPCKEB signal to the low level in a non-access cycle. The period it takes to enter power-down mode is specified by the PDWAIT bits in SDPDCR0. After issuance of the last command to the LPDDR2-S4, if there is no new transfer request during the period of ZB3ϕ cycles specified by the PDWAIT bits, the LPDDR2-S4 enters power-down mode. This power-down mode can effectively lower power consumption in non-access cycles. However, note that if an access occurs in power-down mode, one cycle for driving LPCKEA/LPCKEB high to cancel LPDDR2-S4 power-down mode and wait cycles to satisfy the tXR specification of the LPDDR2-S4 are inserted. Figure 7.17 shows the access timing in power-down mode 1.

(b) Power-Down Mode 2

If the PDOWN1 and PDOWN0 bits in SDCR0 are set to B'01, the LPDDR2-S4 is placed in power-down mode by setting the LPCKEA/LPCKEB signal to the low level in a non-access cycle. At this time, the clock (ZSϕ for SBSC1) to the internal

bus interface block in the SBSC is stopped. The period it takes to enter power-down mode is specified by the PDWAIT bits in SDPDCR0. After issuance of the last command to the LPDDR2-S4, if there is no new transfer request during the period of ZB3ϕ cycles specified by the PDWAIT bits, the LPDDR2-S4 enters power-down mode. This power-down mode can effectively lower power consumption in non-access cycles. However, note that if an access occurs in power-down mode, one cycle for supplying the clock to the internal bus I/F section, one cycle driving the LPCKEA/LPCKEB signal high to cancel LPDDR2-S4 power-down mode, and wait cycles to satisfy the tXR specification of the LPDDR2-S4 are inserted. Figure 7.16 shows the access timing in power-down mode 2.

(c) Power-Down Mode 3

If the PDOWN1 and PDOWN0 bits in SDCR0 are set to B'11, the LPDDR2-S4 is placed in self-refresh mode by issuing the self-refresh command for the LPDDR2-S4 in a non-access cycle. At this time, the clock (ZSϕ for SBSC1) to the internal bus interface block in the SBSC and the SBSC operation clock (ZB3ϕ) are stopped. The period it takes to issue the self-refresh command is specified by the PDWAIT bits in SDPDCR0. After issuance of the last command to the LPDDR2-S4, if there is no new transfer request during the period of ZB3ϕ cycles specified by the PDWAIT bits, the LPDDR2-S4 enters self-refresh mode. This power-down mode can effectively lower power consumption in non-access cycles. However, note that if an access occurs in self-refresh mode, an overhead equal to the number of wait cycles occurring between SDR-SDRAM self-refresh mode cancellation and ACTV command issuance occurs in order to cancel LPDDR2-S4 self-refresh mode. Figure 7.16 shows the access timing in power-down mode 3.

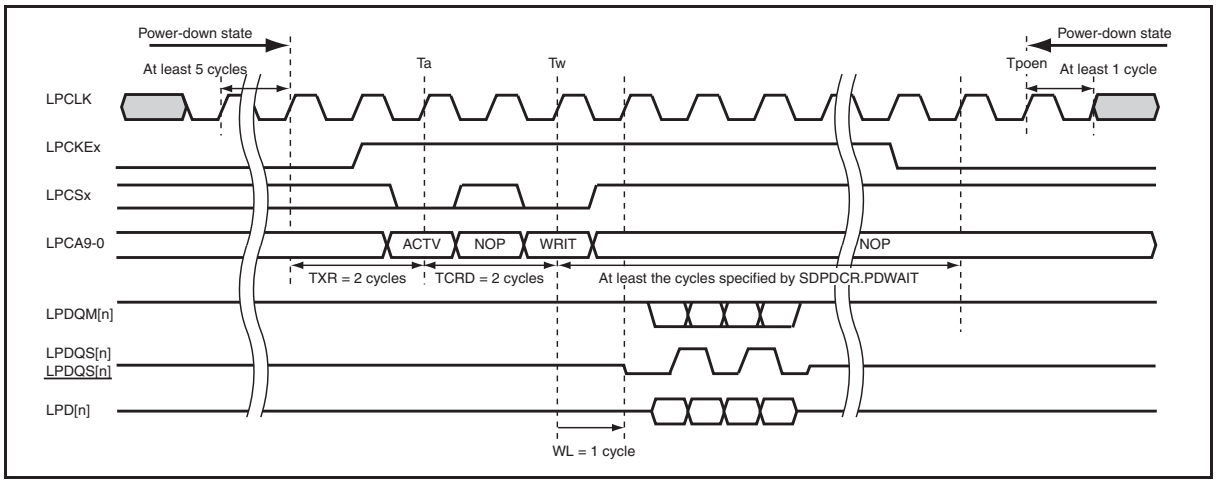


Figure 7.16 Access Timing in Power Down Mode 1 or 2 (SDCR0.PDOWN10 = 10/01, TXR = 1 (2 cycles), TRCD = 1 (2 cycles))

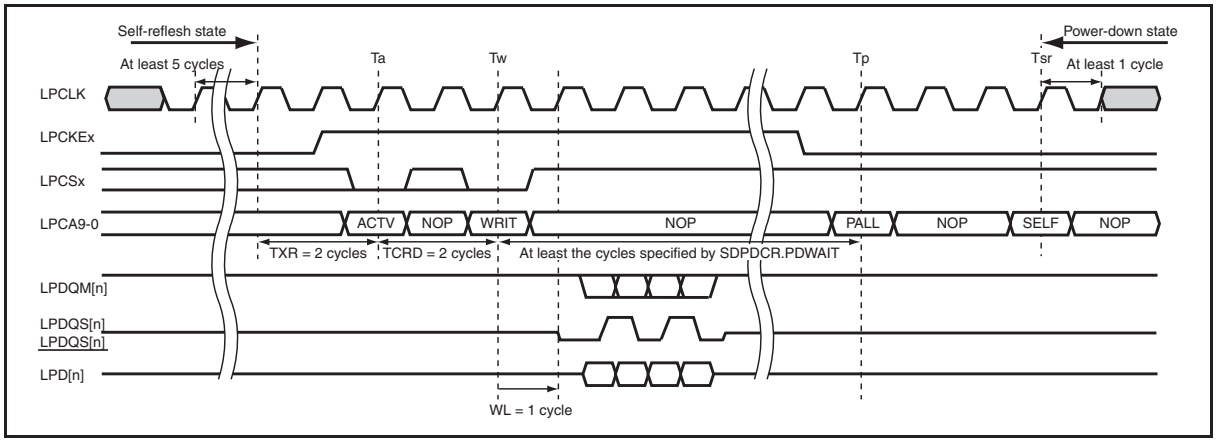


Figure 7.17 Access Timing in Power Down Mode 3
(SDCR0.PDOWN10 = 10/01, TSREX = 1 (2 cycles), TRCD = 1 (2 cycles), TRPAB = 2 (3 cycles))

(8) Deep Power-Down Mode

The LPDDR2-S4 supporting the low-power function provides deep power-down mode as a power-down mode.

With the partial self-refresh function, self-refreshing is performed on a specific area. In deep power-down mode, self-refreshing will not be performed on any memory area. This mode is effective in systems where all of the system memory areas are used as work areas.

If the value of 1 is written to the RMODE bit while the DEEP bit in SDCR0/SDCR1 and the RFSH bit are both set to 1, the LPDDR2-S4 supporting the low-power function enters deep power-down mode. If the RMODE bit is cleared to 0, the LPCKEA/LPCKEB signal is pulled high to cancel deep power-down mode. Before executing an access after canceling deep power-down mode, the power-on sequence must be re-executed.

Note that some LPDDR2-S4 devices require specific cycles of idle time after cancellation of deep power-down mode. For information on this idle time, see the manual of the LPDDR2-S4 to be used.

When shifting the LPDDR2-S4 from self-refresh state to deep power-down mode, write 0 to the RMODE bit to clear self-refresh mode before setting deep power-down mode. Likewise, when shifting from deep power-down mode to self-refresh mode, clear deep power-down mode before setting self-refresh mode.

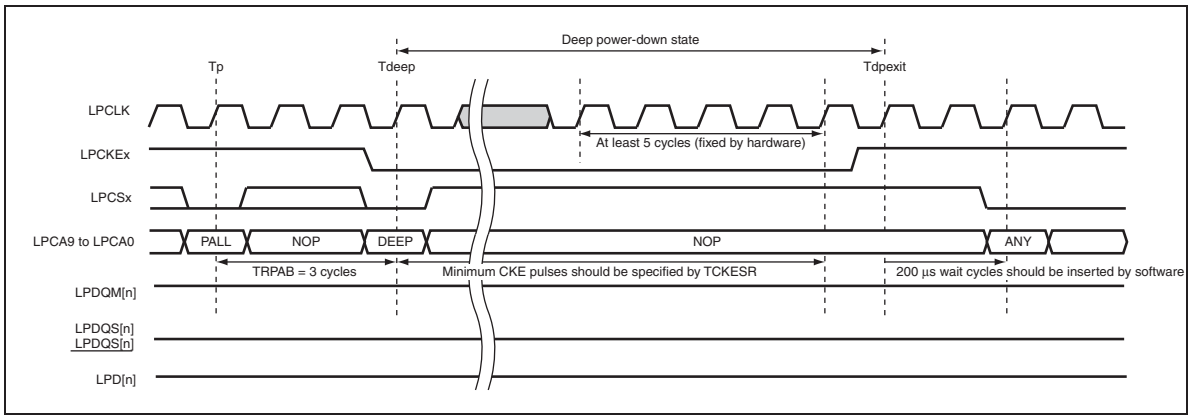


Figure 7.18 Deep Power-Down Mode Transition Timing (SDCR0.DEEP = 1, RMODE = 1, RFSH = 1, SDWCR0/1.TRP = 2)

(9) Power-Down Control Using LPCKEA/LPCKEB Pin

In this LSI, a different CKE pin can be connected to each LPDDR2-S4. This enables power-down modes, such as self-refresh mode and deep power-down mode, to be selected separately for each LPDDR2-S4 to reduce power consumption. In power-down mode 1, 2, or 3, only the DRAM area that is accessed is activated.

(10) Initial Value of LPCKEA/LPCKEB Pin Level

In this LSI, the initial value of the LPACKEA/LPACKEB pin during a power-on reset and after cancellation of a reset can be selected with the CKEMD10 (SBSC1) bit in reset control register 2 (RESCNT2) of the SYSC. The correspondence between the CKEMD10 bit and the LPACKEA/LPACKEB pin level is shown in table 7.18.

If the low level is selected as the initial value of the LPACKEA/LPACKEB pin, drive the LPACKEA/LPACKEB pin back to the high level by writing 1 to the CKELV bit in SDPCR before access to LPDDR2-S4 is restarted.

Table 7.18 Correspondence between CKEMD10 Bit in Reset Control Register 2 of SYSC and LPACKEA/LPACKEB Pin Level

CKEMD10 Bit in Reset Control Register 2	Description
0	LPACKEA/LPACKEB pin outputs low level as initial state
1	LPACKEA/LPACKEB pin outputs high level as initial state

(11) Control during Power Cutoff

The SBSC is allocated in the area where the power cutoff function works.

SBSC1: Power-supply area A4S

The SBSC has a function for register backup during power cutoff; after power-supply is restarted, the register contents can be restored to the state before power cutoff. (For the registers whose contents are saved, refer to table 7.3, SBSC1 Register States in Each Operating Mode.)

The following shows the procedures for SBSC power cutoff.

a) Power Cutoff while the SBSC is in Self-Refresh Mode

a-1) Stop memory access to the SBSC. It should be guaranteed by software that the SBSC area is never accessed during power cutoff. If the memory space or register space in the SBSC is accessed while the power to the SBSC is stopped, the SHWY module returns an error.

a-2) Set the SBSC to self-refresh mode through the RMODE bit in SDCRx.

a-3) Turn off the power to the corresponding power-supply area. *

a-4) Power cutoff state *

a-5) Turn on the power to the corresponding power-supply area. *

a-6) Check the status bit that indicates the power-supply state to confirm that the power has been turned on. *

a-7) Clear self-refresh mode. (Write 1 to the RMODE bit in SDCRx.)

a-8) Read the RMODE bit to confirm that 1 has been written to it.

a-9) Restart memory access.

Note: * For details of power control, refer to the section describing the SYSC.

b) Power Cutoff while the SBSC is in Auto-Refresh Mode

When power is cut off while the SBSC is in auto-refresh mode without being shifted to self-refresh mode, the SBSC detects the power cutoff sequence and automatically moves to self-refresh mode. Therefore, correct memory contents are retained after the power supply is stopped and then restarted.

b-1) Stop memory access to the SBSC. It should be guaranteed by software that the SBSC area is never accessed

during power cutoff. If the memory space or register space in the SBSC is accessed while the power to the SBSC is stopped, the SHWY module returns an error.

b-2) Turn off the power to the corresponding power-supply area. *

b-3) Power cutoff state *

(When PDSELF = 1 and RFSH = 1 in SDCR0, the SBSC sets the LPDDR2-S4 to self-refresh state in synchronization with power cutoff in the SBSC area.)

b-4) Turn on the power to the corresponding power-supply area. *

Upon detecting the power-on sequence, the SBSC clears self-refresh mode and restarts auto-refreshing (if self-refresh mode was specified through the RMODE bit before power cutoff, the SBSC continues self-refresh mode).

b-5) Check the status bit that indicates the power-supply state to confirm that the power has been turned on. *

b-6) Restart memory access.

Note: * For details of power control, refer to the section describing the SYSC.

(12) Memory Protected Area Function

In this LSI, each SBSC area is divided into four areas through the setting in the memory protected area division register and an access privilege can be assigned for each area. The memory protection function of this LSI has the following features.

a) Ability to specify a privilege to change the memory protected area setting register (SDPTCR)

Once a CPU writes to SDPTCR with the REGWP bit set to 1, only that CPU subsequently has the privilege to change the SDPTCR setting.

The BB-CPU, AP-CPU, AP secure CPU, and RT-CPU can have this privilege.

b) Ability to specify a privilege to access (change) the memory protected area division register (SDPTDIVCR)

Once a CPU writes to SDPTDIVCR with the REGWP bit set to 1, only that CPU subsequently has the privilege to change the SDPTDIVCR setting. The BB-CPU, AP-CPU, AP secure CPU, and RT-CPU can have this privilege. In addition, once a CPU writes to SDPTDIVCR with the REGWP2 bit set to 1, no CPU can subsequently change the SDPTDIVCR setting. In this case, the SDPTDIVCR setting cannot be modified until a power-on reset is applied.

c) Ability to specify secure-mode areas

Writing 1 to the SCR_EN or SRW_EN bit in SDPTDIVCR specifies the corresponding area as a secure-mode area; that is, the area can be accessed only from a secure initiator. When SCR_EN = 1, the area can be read only from a secure initiator, and when SCR_EN = 1, the area can be written to only from a secure initiator. The AP-ARM, BB-ARM, CC5, or CoreSight in secure mode can be a secure initiator.

d) Ability to specify a privilege of access from the BB and AP to an area set to non-secure mode

For an area that is used in non-secure mode, the privilege of access from the AP-domain modules and BB-domain modules can be specified separately for read access and write access.

Figure 7.19 gives an overview of the SBSC memory protection function.

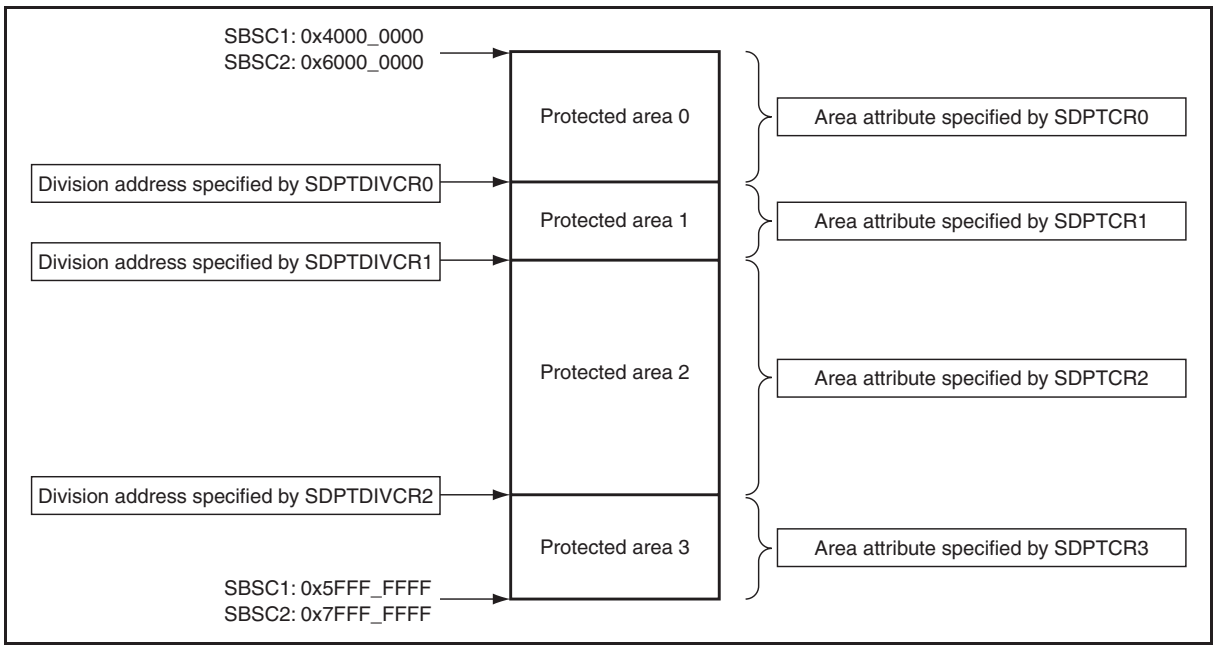


Figure 7.19 Overview of SBSC Memory Protection Function

Use the following procedure for memory protection setting.

1) Specify area division addresses through SDPTDIVCR0 to SDPTDIVCR2 to satisfy the following restrictions.

   Restrictions on SBSC1 memory protection setting

   Bits 31 to 17 of SBSC1 start address (0x40000000)

   < SDPTDIVCR0A.DIVADR < SDPTDIVCR1A.DIVADR < SDPTDIVCR2A.DIVADR

   < Bits 31 to 17 of SBSC1 end address (0x5FFFFFFF)

2) Check that desired values are read from the CPUTYPE bits in SDPTDIVCR0 to SDPTDIVCR2 and both the REGWP and REGWP2 bits are cleared to 0.

3) Make necessary memory protection settings for each area through SDPTCR0 to SDPTCR3.

4) Check that desired values are read from the CPUTYPE bits in SDPTCR0 to SDPTCR3 and the REGWP bit is cleared to 0.

Notes:

1) The SDPTDIVCR0 to SDPTDIVCR2 values must satisfy the above restrictions. Until SDPTDIVCR settings are completed and satisfy the above restrictions, do not make memory protection settings for each area through SDPTCR0 to SDPTCR3; otherwise, the memory protection function will work unexpectedly.

2) SDPTDIVCR0 to SDPTDIVCR2 and SDPTCR0 to SDPTCR3 can be modified from a program in the SBSC external memory space including the target area of a memory protection setting modification, but make sure that the area does not become the target of access protection during or after setting modification.

7.6 Others

7.6.1 Reset

The SBSC1 can be initialized completely only by a power-on reset. At a power-on reset, all signals are negated and output buffers are turned off immediately regardless of the bus cycle state. All control registers are initialized.

The SBSC1 has a function to retain the control register values when the power to the power supply area (A4S) where the SBSC1 is allocated is cut off. The control registers whose values are to be retained are shown in tables 7.9 and 7.11. The backup registers for retaining control register values are allocated in area C5. Control register values will not be retained if the power to area C5 is cut off.

7.6.2 Access Error

The SBSC may return an access error according to its state.

When the SBSC returns an access error, a prefetch abort or a data abort occurs in the CPU.

In cases 1) to 7) below, the SBSC returns an access error.

1) After a power-on reset is canceled, memory is accessed while the CKELV bit in SDPTCR is 0.
2) Access is done for a memory area that has been set to self-refresh or deep power-down state through the RMODE bit setting in SDCRx.
3) A memory area is accessed by a CPU that is not assigned a privilege of access to that memory area through the memory protection function.
4) Access is done for a DRAM area whose memory parameter setting exceeds the memory capacity specified through the SDSZ bits (memory space per DRAM area) in SDCR0.

   Example: Case 4) applies to when DRAM area 0 is accessed while the SDCRA0.SDSZ bits are set to 2'b00 (512 Mbits per area) and parameters for 1-Gbit memory (SZ = 2'b01, BANK = 0 (4-bank configuration), ROW = 3'b100 (15 bits), and COL = 2'b00 (8 bits)) are specified in SDCR0.
5) Access is done at an address exceeding the memory capacity in the DRAM area whose memory parameter setting does not reach the memory capacity specified through the SDSZ bits (memory space per DRAM area) in SDCR0.

   Example: When the SDCRA0.SDSZ bits are set to 2'b01 (1 Gbits per area) and parameters for 512-Mbit memory are specified in SDCR0:

   DRAM area 0: 1 G bits from 0x50000000 to 0x57FFFFFF

   Memory parameter setting: 512 Mbits from 0x50000000 to 0x53FFFFFF

   Case 5) applies to access to an address from 0x54000000 to 0x57FFFFFF under the above conditions.
6) An SBSC register or memory area is accessed while the power-supply area where the SBSC is allocated is turned off.
7) The memory area (including the registers in the memory) is accessed while the PLLCNT bit in SDCR0 is 1 and the PLLC1 is turned off.

7.6.3 SBSC1 Performance Monitor

This LSI has an SBSC access monitor function. For details, refer to the section describing the TDBG.

The module stop setting through the CPGA is applied to this monitor block. In the initial state, this block is in module stop state; to use the monitor function, cancel module stop state.

When the SBSC1 performance monitor function is used, signals are output in the mobileDDR (single data rate) protocol for each output command because if the LPDDR2 protocol is used instead, addresses and commands are output at double data rate and cannot be monitored correctly from outside.

Table 7.20 shows the correspondence between the LPDDR-S4 protocol and monitor output protocol.

Table 7.20 Correspondence between LPDDR-S4 Protocol and Monitor Output Protocol

LPDDR2-S4 Command		Monitor Output									
Command	Command Description	CKE		CS	RAS	CAS	RDWR	AP (ADR10)	BA 2 to 0	ADR 14 to 0	Remarks
		CLK(n-1)	CLK(n)								
MRW	Write to mode register	H	H	L	L	L	L	X	X	X	Cannot distinguish between MRW and MRR
MRR	Read from mode register	H	H	L	L	L	L	X	X	X	
REFA	All banks refresh	H	H	L	L	L	H	X	X	X	
SELF	Self-refresh entry	H	L	L	L	L	H	X	X	L	
ACTV	Active	H	H	L	L	H	H	Target row address	Target bank	Target row address	
WRIT	Write	H	H	L	H	L	L	AP	Target bank	Target column address	
READ	Read	H	H	L	H	L	H	AP	Target bank	Target column address	
PALL	All banks precharge	H	H	L	L	H	L	H	X	X	
PRE	Specified bank precharge	H	H	L	L	H	L	L	Target bank	X	
DEEP	Deep power-down entry	H	L	L	H	H	L	X	X	X	
NOP	No operation	H	H	L	H	H	H	X	X	X	
SELF/DEEP /PD retain	SELF/DEEP /PD retain	L	L	X	X	X	X	X	X	X	
PDEN	Power-down entry	H	L	H	X	X	X	X	X	X	
SELF/DEEP /PD EXIT	SELF/DEEP /PD exit	L	H	H	X	X	X	X	X	X	

Section 8 Direct Memory Access Controller (DMAC)

This LSI includes three sets of direct memory access controllers (DMAC1, DMAC2 and DMAC3 which are collectively called the DMAC).

The DMAC can be used in place of the CPU to perform high-speed transfers between external memory, on-chip memory, memory-mapped external devices, and on-chip peripheral modules.

8.1 Features

- Six channels
- 4-Gbyte physical address space
- Data transfer unit is selectable: Byte, word (2 bytes), longword (4 bytes), 8 bytes, 16 bytes, 32 bytes, and 64 bytes
- Maximum transfer count: 16,777,216 transfers
- Address mode: Dual address mode
- Transfer requests:

  On-chip peripheral module request, or auto request can be selected.

  The following modules can issue an on-chip peripheral module request.

  — CMT1, SCIFA0/1/2/3/4/5, SCIFB, MSIOF0/1/2, BBIF1/2, IIC0/1/2/3/4, FLCTL0/1, FSI, SDHI0/1/2, TPU0, TSIF0/1, IRDA, DSI0/1, HSI, MFI, MMC, SHWYSTAT
- Bus mode: Cycle steal mode (normal mode and intermittent mode)
- Selectable channel priority levels:

  The channel priority levels are selectable between fixed mode and round-robin mode.
- Interrupt request: An interrupt request can be generated to the CPU after half of the transfers ended, all transfers ended, or an address error occurred.
- Gathering buffer function: Transfer data of 256 bytes or less can be collectively transmitted.

Figure 8.1 shows the block diagram of the DMAC.

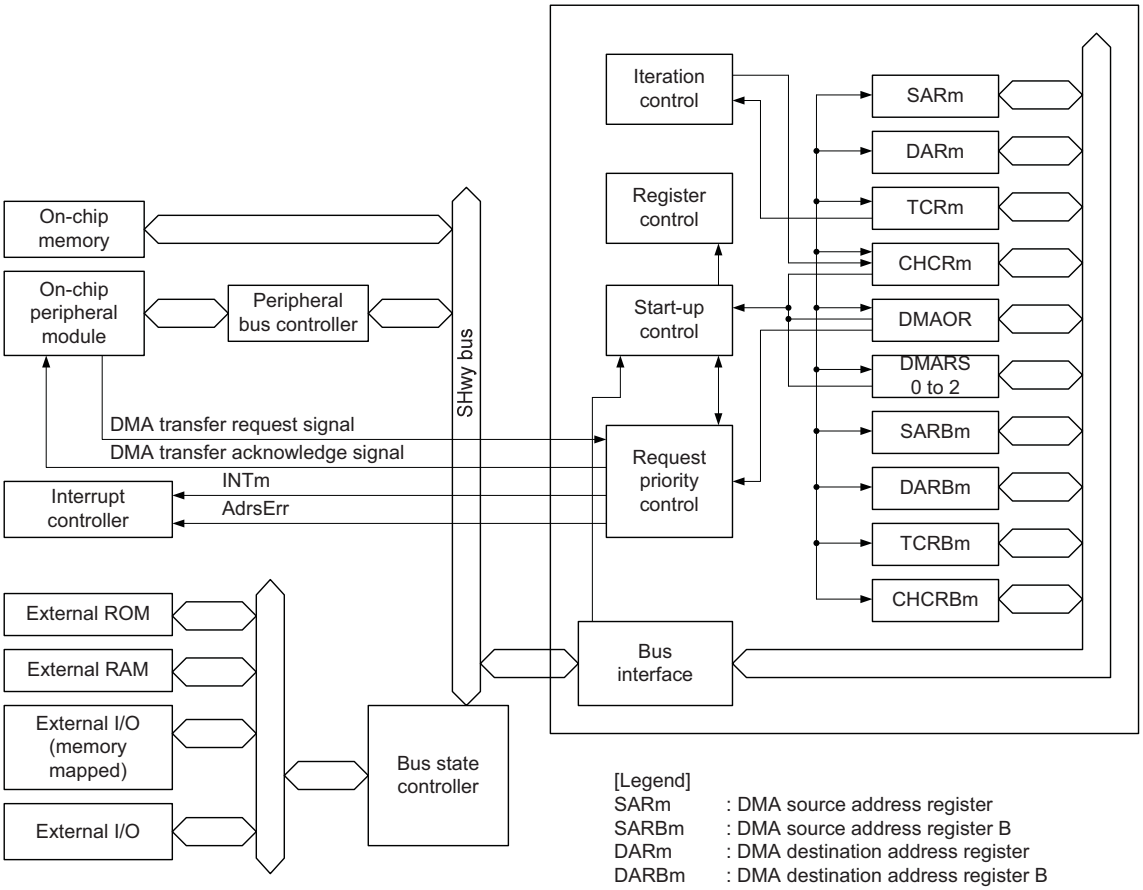


Figure 8.1 Block Diagram of DMAC

8.2 Input/Output Pins

There are no external pins relevant to the DMAC.

8.3 Register Descriptions

Table 8.1, Table 8.3, and Table 8.5 show the configuration of registers of the DMAC1, DMAC2, and DMAC3, respectively. Table 8.2, Table 8.4, and Table 8.6 show the state of the registers in each processing mode.

The DMASAR for channel 0 in the DMAC1 is expressed as DMA1SAR_0 and the DMAOR for channel 2 in the DMAC2 is expressed as DMA2OR.

Table 8.1 Register Configuration of DMAC1

Name	Abbreviation	R/W	Address	Access Size
DMA1 source address register_0	DMA1SAR_0	R/W	H'FE00 8020	32
DMA1 destination address register_0	DMA1DAR_0	R/W	H'FE00 8024	32
DMA1 transfer count register_0	DMA1TCR_0	R/W	H'FE00 8028	32
DMA1 channel control register_0	DMA1CHCR_0	R/W	H'FE00 802C	32
DMA1 source address register_1	DMA1SAR_1	R/W	H'FE00 8030	32
DMA1 destination address register_1	DMA1DAR_1	R/W	H'FE00 8034	32
DMA1 transfer count register_1	DMA1TCR_1	R/W	H'FE00 8038	32
DMA1 channel control register_1	DMA1CHCR_1	R/W	H'FE00 803C	32
DMA1 source address register_2	DMA1SAR_2	R/W	H'FE00 8040	32
DMA1 destination address register_2	DMA1DAR_2	R/W	H'FE00 8044	32
DMA1 transfer count register_2	DMA1TCR_2	R/W	H'FE00 8048	32
DMA1 channel control register_2	DMA1CHCR_2	R/W	H'FE00 804C	32
DMA1 source address register_3	DMA1SAR_3	R/W	H'FE00 8050	32
DMA1 destination address register_3	DMA1DAR_3	R/W	H'FE00 8054	32
DMA1 transfer count register_3	DMA1TCR_3	R/W	H'FE00 8058	32
DMA1 channel control register_3	DMA1CHCR_3	R/W	H'FE00 805C	32
DMA1 operation register	DMA1OR	R/W	H'FE00 8060	16
DMA1 source address register_4	DMA1SAR_4	R/W	H'FE00 8070	32
DMA1 destination address register_4	DMA1DAR_4	R/W	H'FE00 8074	32
DMA1 transfer count register_4	DMA1TCR_4	R/W	H'FE00 8078	32
DMA1 channel control register_4	DMA1CHCR_4	R/W	H'FE00 807C	32
DMA1 source address register_5	DMA1SAR_5	R/W	H'FE00 8080	32
DMA1 destination address register_5	DMA1DAR_5	R/W	H'FE00 8084	32
DMA1 transfer count register_5	DMA1TCR_5	R/W	H'FE00 8088	32
DMA1 channel control register_5	DMA1CHCR_5	R/W	H'FE00 808C	32
DMA1 source address register B_0	DMA1SARB_0	R/W	H'FE00 8120	32
DMA1 destination address register B_0	DMA1DARB_0	R/W	H'FE00 8124	32
DMA1 transfer count register B_0	DMA1TCRB_0	R/W	H'FE00 8128	32
DMA1 channel control register B_0	DMA1CHCRB_0	R/W	H'FE00 812C	32
DMA1 source address register B_1	DMA1SARB_1	R/W	H'FE00 8130	32
DMA1 destination address register B_1	DMA1DARB_1	R/W	H'FE00 8134	32
DMA1 transfer count register B_1	DMA1TCRB_1	R/W	H'FE00 8138	32
DMA1 channel control register B_1	DMA1CHCRB_1	R/W	H'FE00 813C	32
DMA1 source address register B_2	DMA1SARB_2	R/W	H'FE00 8140	32

Name	Abbreviation	R/W	Address	Access Size
DMA1 destination address register B_2	DMA1DARB_2	R/W	H'FE00 8144	32
DMA1 transfer count register B_2	DMA1TCRB_2	R/W	H'FE00 8148	32
DMA1 channel control register B_2	DMA1CHCRB_2	R/W	H'FE00 814C	32
DMA1 source address register B_3	DMA1SARB_3	R/W	H'FE00 8150	32
DMA1 destination address register B_3	DMA1DARB_3	R/W	H'FE00 8154	32
DMA1 transfer count register B_3	DMA1TCRB_3	R/W	H'FE00 8158	32
DMA1 channel control register B_3	DMA1CHCRB_3	R/W	H'FE00 815C	32
DMA1 source address register B_4	DMA1SARB_4	R/W	H'FE00 8170	32
DMA1 destination address register B_4	DMA1DARB_4	R/W	H'FE00 8174	32
DMA1 transfer count register B_4	DMA1TCRB_4	R/W	H'FE00 8178	32
DMA1 channel control register B_4	DMA1CHCRB_4	R/W	H'FE00 817C	32
DMA1 source address register B_5	DMA1SARB_5	R/W	H'FE00 8180	32
DMA1 destination address register B_5	DMA1DARB_5	R/W	H'FE00 8184	32
DMA1 transfer count register B_5	DMA1TCRB_5	R/W	H'FE00 8188	32
DMA1 channel control register B_5	DMA1CHCRB_5	R/W	H'FE00 818C	32
DMA1 channel clear register_0	DMA1CHCLR_0	R/W	H'FE00 8220	32
DMA1 channel clear register_1	DMA1CHCLR_1	R/W	H'FE00 8230	32
DMA1 channel clear register_2	DMA1CHCLR_2	R/W	H'FE00 8240	32
DMA1 channel clear register_3	DMA1CHCLR_3	R/W	H'FE00 8250	32
DMA1 channel clear register_4	DMA1CHCLR_4	R/W	H'FE00 8270	32
DMA1 channel clear register_5	DMA1CHCLR_5	R/W	H'FE00 8280	32
DMA1 extended resource selector_0	DMA1RS_0	R/W	H'FE00 9000	16
DMA1 extended resource selector_1	DMA1RS_1	R/W	H'FE00 9004	16
DMA1 extended resource selector_2	DMA1RS_2	R/W	H'FE00 9008	16

Table 8.2 State of DMAC1 Registers in Each Operating Mode

Abbreviation	Reset*	Module Standby
DMA1SAR_0 to DMA1SAR_5	Initialized	Retained
DMA1DAR_0 to DMA1DAR_5	Initialized	Retained
DMA1TCR_0 to DMA1TCR_5	Initialized	Retained
DMA1CHCR_0 to DMA1CHCR_5	Initialized	Retained
DMA1OR	Initialized	Retained
DMA1SARB_0 to DMA1SARB_5	Initialized	Retained
DMA1DARB_0 to DMA1DARB_5	Initialized	Retained
DMA1TCRB_0 to DMA1TCRB_5	Initialized	Retained
DMA1CHCRB_0 to DMA1CHCRB_5	Initialized	Retained
DMA1CHCLR_0 to DMA1CHCLR_5	Initialized	Retained
DMA1RS_0 to DMA1RS_2	Initialized	Retained

* For details, refer to section 1-D Overview of reset.

Table 8.3 Register Configuration of DMAC2

Name	Abbreviation	R/W	Address	Access Size
DMA2 source address register_0	DMA2SAR_0	R/W	H'FE01 8020	32
DMA2 destination address register_0	DMA2DAR_0	R/W	H'FE01 8024	32
DMA2 transfer count register_0	DMA2TCR_0	R/W	H'FE01 8028	32
DMA2 channel control register_0	DMA2CHCR_0	R/W	H'FE01 802C	32
DMA2 source address register_1	DMA2SAR_1	R/W	H'FE01 8030	32
DMA2 destination address register_1	DMA2DAR_1	R/W	H'FE01 8034	32
DMA2 transfer count register_1	DMA2TCR_1	R/W	H'FE01 8038	32
DMA2 channel control register_1	DMA2CHCR_1	R/W	H'FE01 803C	32
DMA2 source address register_2	DMA2SAR_2	R/W	H'FE01 8040	32
DMA2 destination address register_2	DMA2DAR_2	R/W	H'FE01 8044	32
DMA2 transfer count register_2	DMA2TCR_2	R/W	H'FE01 8048	32
DMA2 channel control register_2	DMA2CHCR_2	R/W	H'FE01 804C	32
DMA2 source address register_3	DMA2SAR_3	R/W	H'FE01 8050	32
DMA2 destination address register_3	DMA2DAR_3	R/W	H'FE01 8054	32
DMA2 transfer count register_3	DMA2TCR_3	R/W	H'FE01 8058	32
DMA2 channel control register_3	DMA2CHCR_3	R/W	H'FE01 805C	32
DMA2 operation register	DMA2OR	R/W	H'FE01 8060	16
DMA2 source address register_4	DMA2SAR_4	R/W	H'FE01 8070	32
DMA2 destination address register_4	DMA2DAR_4	R/W	H'FE01 8074	32
DMA2 transfer count register_4	DMA2TCR_4	R/W	H'FE01 8078	32
DMA2 channel control register_4	DMA2CHCR_4	R/W	H'FE01 807C	32
DMA2 source address register_5	DMA2SAR_5	R/W	H'FE01 8080	32
DMA2 destination address register_5	DMA2DAR_5	R/W	H'FE01 8084	32
DMA2 transfer count register_5	DMA2TCR_5	R/W	H'FE01 8088	32
DMA2 channel control register_5	DMA2CHCR_5	R/W	H'FE01 808C	32
DMA2 source address register B_0	DMA2SARB_0	R/W	H'FE01 8120	32
DMA2 destination address register B_0	DMA2DARB_0	R/W	H'FE01 8124	32
DMA2 transfer count register B_0	DMA2TCRB_0	R/W	H'FE01 8128	32
DMA2 channel control register B_0	DMA2CHCRB_0	R/W	H'FE01 812C	32
DMA2 source address register B_1	DMA2SARB_1	R/W	H'FE01 8130	32
DMA2 destination address register B_1	DMA2DARB_1	R/W	H'FE01 8134	32
DMA2 transfer count register B_1	DMA2TCRB_1	R/W	H'FE01 8138	32
DMA2 channel control register B_1	DMA2CHCRB_1	R/W	H'FE01 813C	32
DMA2 source address register B_2	DMA2SARB_2	R/W	H'FE01 8140	32
DMA2 destination address register B_2	DMA2DARB_2	R/W	H'FE01 8144	32
DMA2 transfer count register B_2	DMA2TCRB_2	R/W	H'FE01 8148	32
DMA2 channel control register B_2	DMA2CHCRB_2	R/W	H'FE01 814C	32
DMA2 source address register B_3	DMA2SARB_3	R/W	H'FE01 8150	32
DMA2 destination address register B_3	DMA2DARB_3	R/W	H'FE01 8154	32
DMA2 transfer count register B_3	DMA2TCRB_3	R/W	H'FE01 8158	32
DMA2 channel control register B_3	DMA2CHCRB_3	R/W	H'FE01 815C	32

Name	Abbreviation	R/W	Address	Access Size
DMA2 source address register B_4	DMA2SARB_4	R/W	H'FE01 8170	32
DMA2 destination address register B_4	DMA2DARB_4	R/W	H'FE01 8174	32
DMA2 transfer count register B_4	DMA2TCRB_4	R/W	H'FE01 8178	32
DMA2 channel control register B_4	DMA2CHCRB_4	R/W	H'FE01 817C	32
DMA2 source address register B_5	DMA2SARB_5	R/W	H'FE01 8180	32
DMA2 destination address register B_5	DMA2DARB_5	R/W	H'FE01 8184	32
DMA2 transfer count register B_5	DMA2TCRB_5	R/W	H'FE01 8188	32
DMA2 channel control register B_5	DMA2CHCRB_5	R/W	H'FE01 818C	32
DMA2 channel clear register_0	DMA2CHCLR_0	R/W	H'FE01 8220	32
DMA2 channel clear register_1	DMA2CHCLR_1	R/W	H'FE01 8230	32
DMA2 channel clear register_2	DMA2CHCLR_2	R/W	H'FE01 8240	32
DMA2 channel clear register_3	DMA2CHCLR_3	R/W	H'FE01 8250	32
DMA2 channel clear register_4	DMA2CHCLR_4	R/W	H'FE01 8270	32
DMA2 channel clear register_5	DMA2CHCLR_5	R/W	H'FE01 8280	32
DMA2 extended resource selector_0	DMA2RS_0	R/W	H'FE01 9000	16
DMA2 extended resource selector_1	DMA2RS_1	R/W	H'FE01 9004	16
DMA2 extended resource selector_2	DMA2RS_2	R/W	H'FE01 9008	16

Table 8.4 State of DMAC2 Registers in Each Operating Mode

Abbreviation	Reset*	Module Standby
DMA2SAR_0 to DMA2SAR_5	Initialized	Retained
DMA2DAR_0 to DMA2DAR_5	Initialized	Retained
DMA2TCR_0 to DMA2TCR_5	Initialized	Retained
DMA2CHCR_0 to DMA2CHCR_5	Initialized	Retained
DMA2OR	Initialized	Retained
DMA2SARB_0 to DMA2SARB_5	Initialized	Retained
DMA2DARB_0 to DMA2DARB_5	Initialized	Retained
DMA2TCRB_0 to DMA2TCRB_5	Initialized	Retained
DMA2CHCRB_0 to DMA2CHCRB_5	Initialized	Retained
DMA2CHCLR_0 to DMA2CHCLR_5	Initialized	Retained
DMA2RS_0 to DMA2RS_2	Initialized	Retained

* For details, refer to section 1-D Overview of reset.

Table 8.5 Register Configuration of DMAC3

Name	Abbreviation	R/W	Address	Access Size
DMA3 source address register_0	DMA3SAR_0	R/W	H'FE02 8020	32
DMA3 destination address register_0	DMA3DAR_0	R/W	H'FE02 8024	32
DMA3 transfer count register_0	DMA3TCR_0	R/W	H'FE02 8028	32
DMA3 channel control register_0	DMA3CHCR_0	R/W	H'FE02 802C	32
DMA3 source address register_1	DMA3SAR_1	R/W	H'FE02 8030	32
DMA3 destination address register_1	DMA3DAR_1	R/W	H'FE02 8034	32
DMA3 transfer count register_1	DMA3TCR_1	R/W	H'FE02 8038	32
DMA3 channel control register_1	DMA3CHCR_1	R/W	H'FE02 803C	32
DMA3 source address register_2	DMA3SAR_2	R/W	H'FE02 8040	32
DMA3 destination address register_2	DMA3DAR_2	R/W	H'FE02 8044	32
DMA3 transfer count register_2	DMA3TCR_2	R/W	H'FE02 8048	32
DMA3 channel control register_2	DMA3CHCR_2	R/W	H'FE02 804C	32
DMA3 source address register_3	DMA3SAR_3	R/W	H'FE02 8050	32
DMA3 destination address register_3	DMA3DAR_3	R/W	H'FE02 8054	32
DMA3 transfer count register_3	DMA3TCR_3	R/W	H'FE02 8058	32
DMA3 channel control register_3	DMA3CHCR_3	R/W	H'FE02 805C	32
DMA3 operation register	DMA3OR	R/W	H'FE02 8060	16
DMA3 source address register_4	DMA3SAR_4	R/W	H'FE02 8070	32
DMA3 destination address register_4	DMA3DAR_4	R/W	H'FE02 8074	32
DMA3 transfer count register_4	DMA3TCR_4	R/W	H'FE02 8078	32
DMA3 channel control register_4	DMA3CHCR_4	R/W	H'FE02 807C	32
DMA3 source address register_5	DMA3SAR_5	R/W	H'FE02 8080	32
DMA3 destination address register_5	DMA3DAR_5	R/W	H'FE02 8084	32
DMA3 transfer count register_5	DMA3TCR_5	R/W	H'FE02 8088	32
DMA3 channel control register_5	DMA3CHCR_5	R/W	H'FE02 808C	32
DMA3 source address register B_0	DMA3SARB_0	R/W	H'FE02 8120	32
DMA3 destination address register B_0	DMA3DARB_0	R/W	H'FE02 8124	32
DMA3 transfer count register B_0	DMA3TCRB_0	R/W	H'FE02 8128	32
DMA3 channel control register B_0	DMA3CHCRB_0	R/W	H'FE02 812C	32
DMA3 source address register B_1	DMA3SARB_1	R/W	H'FE02 8130	32
DMA3 destination address register B_1	DMA3DARB_1	R/W	H'FE02 8134	32
DMA3 transfer count register B_1	DMA3TCRB_1	R/W	H'FE02 8138	32
DMA3 channel control register B_1	DMA3CHCRB_1	R/W	H'FE02 813C	32
DMA3 source address register B_2	DMA3SARB_2	R/W	H'FE02 8140	32
DMA3 destination address register B_2	DMA3DARB_2	R/W	H'FE02 8144	32
DMA3 transfer count register B_2	DMA3TCRB_2	R/W	H'FE02 8148	32
DMA3 channel control register B_2	DMA3CHCRB_2	R/W	H'FE02 814C	32
DMA3 source address register B_3	DMA3SARB_3	R/W	H'FE02 8150	32
DMA3 destination address register B_3	DMA3DARB_3	R/W	H'FE02 8154	32
DMA3 transfer count register B_3	DMA3TCRB_3	R/W	H'FE02 8158	32
DMA3 channel control register B_3	DMA3CHCRB_3	R/W	H'FE02 815C	32

Name	Abbreviation	R/W	Address	Access Size
DMA3 source address register B_4	DMA3SARB_4	R/W	H'FE02 8170	32
DMA3 destination address register B_4	DMA3DARB_4	R/W	H'FE02 8174	32
DMA3 transfer count register B_4	DMA3TCRB_4	R/W	H'FE02 8178	32
DMA3 channel control register B_4	DMA3CHCRB_4	R/W	H'FE02 817C	32
DMA3 source address register B_5	DMA3SARB_5	R/W	H'FE02 8180	32
DMA3 destination address register B_5	DMA3DARB_5	R/W	H'FE02 8184	32
DMA3 transfer count register B_5	DMA3TCRB_5	R/W	H'FE02 8188	32
DMA3 channel control register B_5	DMA3CHCRB_5	R/W	H'FE02 818C	32
DMA3 channel clear register_0	DMA3CHCLR_0	R/W	H’FE02 8220	32
DMA3 channel clear register_1	DMA3CHCLR_1	R/W	H’FE02 8230	32
DMA3 channel clear register_2	DMA3CHCLR_2	R/W	H’FE02 8240	32
DMA3 channel clear register_3	DMA3CHCLR_3	R/W	H’FE02 8250	32
DMA3 channel clear register_4	DMA3CHCLR_4	R/W	H’FE02 8270	32
DMA3 channel clear register_5	DMA3CHCLR_5	R/W	H’FE02 8280	32
DMA3 extended resource selector_0	DMA3RS_0	R/W	H'FE02 9000	16
DMA3 extended resource selector_1	DMA3RS_1	R/W	H'FE02 9004	16
DMA3 extended resource selector_2	DMA3RS_2	R/W	H'FE02 9008	16

Table 8.6 State of DMAC3 Registers in Each Operating Mode

Abbreviation	Reset*	Module Standby
DMA3SAR_0 to DMA3SAR_5	Initialized	Retained
DMA3DAR_0 to DMA3DAR_5	Initialized	Retained
DMA3TCR_0 to DMA3TCR_5	Initialized	Retained
DMA3CHCR_0 to DMA3CHCR_5	Initialized	Retained
DMA3OR	Initialized	Retained
DMA3SARB_0 to DMA3SARB_5	Initialized	Retained
DMA3DARB_0 to DMA3DARB_5	Initialized	Retained
DMA3TCRB_0 to DMA3TCRB_5	Initialized	Retained
DMA3CHCRB_0 to DMA3CHCRB_5	Initialized	Retained
DMA3CHCLR_0 to DMA3CHCLR_5	Initialized	Retained
DMA3RS_0 to DMA3RS_2	Initialized	Retained

* For details, refer to section 1-D Overview of reset.

8.3.1 DMA Source Address Registers 0 to 5 (DMASAR_0 to DMASAR_5)

The DMASAR registers are 32-bit readable/writable registers that specify the source address of a DMA transfer. During a DMA transfer, these registers indicate the next source address.

To transfer data in word or in longword units, specify a word or longword boundary address. When transferring data in 8-byte, 16-byte, 32-byte, or 64-byte units, an 8-byte, 16-byte, 32-byte, or 64-byte boundary must be set for the source address value. However, if the address mode in the DMA channel control register is set as fixed (SM[1:0] = B'11) even when transferring data in 32-byte or 64-byte, a value can be specified in 16-byte boundary.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SAR															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SAR															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

8.3.2 DMA Source Address Registers B_0 to 5 (DMASARB_0 to DMASARB_5)

The DMASARB registers are 32-bit readable/writable registers that specify the source address of a DMA transfer that is to be set in DMASAR in repeat/reload mode. Data to be written from the CPU to DMASAR is also written to DMASARB. To set a DMASARB address that differs from the DMASAR address, write data to DMASARB after DMASAR.

To transfer data in word or in longword units, specify a word or longword boundary address. When transferring data in 8-byte, 16-byte, 32-byte, or 64-byte units, an 8-byte, 16-byte, 32-byte, or 64-byte boundary must be set for the source address value. However, if the address mode in the DMA channel control register is set as fixed (SM[1:0] = B'11) even when transferring data in 32-byte or 64-byte, a value can be specified in 16-byte boundary.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SARB															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SARB															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

8.3.3 DMA Destination Address Registers 0 to 5 (DMADAR_0 to DMADAR_5)

The DMADAR registers are 32-bit readable/writable registers that specify the destination address of a DMA transfer. During a DMA transfer, these registers indicate the next destination address.

To transfer data in word or in longword units, specify a word or longword boundary address. When transferring data in 8-byte, 16-byte, 32-byte, or 64-byte units, an 8-byte, 16-byte, 32-byte, or 64-byte boundary must be set for the destination address value. However, if the address mode in the DMA channel control register is set as fixed (SM[1:0] = B'11) even when transferring data in 32-byte or 64-byte, a value can be specified in 16-byte boundary.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DAR															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DAR															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

8.3.4 DMA Destination Address Registers B_0 to 5 (DMADARB_0 to DMADARB_5)

The DMADARB registers are 32-bit readable/writable registers that specify the destination address of a DMA transfer that is to be set in DMADAR in repeat/reload mode. Data to be written from the CPU to DMADAR is also written to DMADARB. To set a DMADARB address that differs from the DMADAR address, write data to DMADARB after DMADAR.

To transfer data in word or in longword units, specify a word or longword boundary address. When transferring data in 8-byte, 16-byte, 32-byte, or 64-byte units, an 8-byte, 16-byte, 32-byte, or 64-byte boundary must be set for the destination address value. However, if the address mode in the DMA channel control register is set as fixed (SM[1:0] = B'11) even when transferring data in 32-byte or 64-byte, a value can be specified in 16-byte boundary.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DARB															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DARB															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

8.3.5 DMA Transfer Count Registers 0 to 5 (DMATCR_0 to DMATCR_5)

The DMATCR registers are 32-bit readable/writable registers that specify the DMA transfer count. The number of transfers is 1 when the setting is H'00000001, 16,777,215 when H'00FFFFFF is set, and 16,777,216 (the maximum) when H'00000000 is set. During a DMA transfer, these registers indicate the remaining transfer count.

The upper eight bits of DMATCR are always read as 0, and the write value should always be 0.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TCR															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TCR															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

8.3.6 DMA Transfer Count Registers B_0 to 5 (DMATCRB_0 to DMATCRB_5)

The DMATCRB registers are 32-bit readable/writable registers. Data to be written from the CPU to DMATCR is also written to DMATCRB. To set a DMATCRB address that differs from the DMATCR address, write data to DMATCRB after DMATCR. While the HE function is used, DMATCRB is used to hold the initial value for detecting HE. DMATCRB specifies the number of DMA transfers which are set in DMATCR in repeat mode. DMATCRB specifies the number of DMA transfers and are used as a transfer counter in reload mode.

In reload mode, the lower 16 bits operate as a transfer counter; the values of DMASAR and DMADAR are updated after the value of the lower 16 bits became 0, and the value of the upper 16 bits of DMATCRB is loaded to the lower 16 bits. In the upper 16 bits, set the number of transfers that should be executed before the transfer count is reloaded. In reload mode, the same number of transfers should be set in both upper and lower 16 bits. In addition, set the HIE bit in DMACHCR to 0 and do not use the HE function.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TCRB															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TCRB															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

8.3.7 DMA Channel Control Registers 0 to 5 (DMACHCR_0 to DMACHCR_5)

The DMACHCR registers are 32-bit readable/writable registers that control the DMA transfer mode.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CAE	CAIE	HEE[1:0]		RPT[2:0]			-	-	-	TS[3:2]		HE	HIE	-	–
Initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/(W)*	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/(W)*	R/W	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DM[1:0]		SM[1:0]		RS[3:0]				-	-	-	TS[1:0]		IE	TE	DE
Initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/(W)*	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31	CAE	0	R/(W)*	Address Error Flag Indicates that an address error interrupt occurred during DMA transfer. This bit is set under following conditions: • The value set in DMASAR or DMADAR does not match the transfer size boundary. • The transfer source or transfer destination is invalid space. • The transfer source or transfer destination is in module stop mode If this bit is set, DMA transfer is not enabled for the channel even if the DE bit is set to 1. To clear the CAE bit, write 0 to the CAE bit after reading 1 from the bit or clear the AE bit in DMAOR. (Clearing the AE bit clears the channel address errors for all channels.) 0: No DMAC address error interrupt [Clearing condition] Writing CAE = 0 after reading CAE = 1 1: DMAC address error interrupt occurs during DMA transfer
30	CAIE	0	R/W	Channel Address Error Interrupt Enable Specifies whether to request the CPU of an interrupt when an address error occurs. If the CAIE bit is set to 1, setting the CAE bit requests the CPU of an interrupt (DEI0 to DEI 5) for each channel. Note: An address error interrupt (DADERR) is asserted simultaneously. For interrupts, see section 5, Interrupt Controller (INTC). 0: Interrupt request disabled 1: Interrupt request enabled

Bit	Bit Name	Initial Value	R/W	Descriptions
29, 28	HEE[1:0]	00	R/W	HE Interrupt Function Extension This bit is meaningful only when the HIE bit is set to 1. 00: HE interrupt occurs when the transfer count reaches about a half of DMATCR which is set before transfer (same as before). 01: HE interrupt occurs every time the transfer count reaches about n/4 (n=1, 2, or 3) of DMATCR which is set before transfer. 10: HE interrupt occurs every time the transfer count reaches about n/8 (n=1 to 7) of DMATCR which is set before transfer. 11: HE interrupt occurs every time the transfer count reaches about n/16 (n=1 to 15) of DMATCR which is set before transfer.
27 to 25	RPT[2:0]	000	R/W	DMA Setting Renewal Specify 000: Normal mode (DMAC operation) 001: Repeat mode DMASAR/DMADAR used as repeat area 010: Repeat mode DMADAR used as repeat area 011: Repeat mode DMASAR used as repeat area 100: Setting prohibited 101: Reload mode DMASAR/DMADAR used as reload area 110: Reload mode DMADAR used as reload area 111: Reload mode DMASAR used as reload area
24 to 22	—	000	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
21, 20	TS[3:2]	00	R/W	DMA Transfer Size Specify With TS[1:0], these bits specify the DMA transfer size. When the transfer source or transfer destination is a register of an on-chip peripheral module with a transfer size set, a proper transfer size for the register should be set. In 2-division transfer mode, 16/32-byte data is halved and transferred in two operations. For the transfer source or destination address specified by DMASAR or DMADAR, an appropriate boundary address should be set according to the transfer data size. TS[3:2] + TS[1:0] 0000: Byte units transfer 0001: Word (2-byte) units transfer 0010: Longword (4-byte) units transfer 0011: 16-byte units transfer 0100: 32-byte units transfer 0101: 64-byte units transfer 0111: 8-byte units transfer Other than above: Setting prohibited
19	HE	0	R/(W)*	Half End Flag After HIE (bit 18) is set to 1 and the number of transfers become half of DMATCR (1 bit shift to right) which is set before transfer starts, HE becomes 1. The HE bit is not set when transfers are ended by an address error or by clearing the DE bit and the DME bit in DMAOR before the number of transfers is decreased to half of the DMATCR value set preceding the transfer. The HE bit is kept set when the transfer ends by an address error, or clearing the DE bit (bit 0) or the DME bit in DMAOR after the HE bit is set to 1. To clear the HE bit, write 0 after reading 1 in the HE bit. 0: During the DMA transfer or DMA transfer has been interrupted DMATCR > (DMATCR set before transfer)/2 [Clearing condition] Writing 0 after reading HE = 1. 1: DMATCR ≤ (DMATCR set before transfer)/2
18	HIE	0	R/W	Half End Interrupt Enable Specifies whether an interrupt request is generated to the CPU when the number of transfers is decreased to half of the DMATCR value set preceding the transfer. When the HIE bit is set to 1 and the HE bit is set, an interrupt request is generated to the CPU. Set this bit to 0 while reload mode is set. 0: Interrupt request is disabled when DMATCR = (DMATCR set before transfer)/2 1: Interrupt request is enabled when DMATCR = (DMATCR set before transfer)/2
17, 16	—	000	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
15, 14	DM[1:0]	00	R/W	Destination Address Mode Specify whether the DMA destination address is incremented, decremented, or left fixed. 00: Fixed destination address 01: Destination address is incremented +1 in byte units transfer +2 in word units transfer +4 in longword units transfer +8 in 8-byte units transfer +16 in 16-byte units transfer +32 in 32-byte units transfer +64 in 64-byte units transfer 10: Destination address is decremented –1 in byte units transfer –2 in word units transfer –4 in longword units transfer Setting prohibited in 8/16/32-byte units transfer 11: Fixed destination address Set to prevent an address from being changed in the objective modules. Example: When specifying FIFOs in the peripheral modules.
13, 12	SM[1:0]	00	R/W	Source Address Mode Specify whether the DMA source address is incremented, decremented, or left fixed. 00: Fixed source address 01: Source address is incremented +1 in byte units transfer +2 in word units transfer +4 in longword units transfer +8 in 8-byte units transfer +16 in 16-byte units transfer +32 in 32-byte units transfer +64 in 64-byte units transfer 10: Source address is decremented –1 in byte units transfer –2 in word units transfer –4 in longword units transfer Setting prohibited in 8/16/32-byte units transfer 11: Fixed source address Set to prevent an address from being changed in the objective modules. Example: When specifying FIFOs in the peripheral modules.
11 to 8	RS[3:0]	0000	R/W	Resource Select Specify which transfer requests will be sent to the DMAC. The changing of transfer request source should be done in the state that the DMA enable bit (DE) is set to 0. 0100: Auto request 1000: Selected by DMA extended resource selector Other than above: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Descriptions
7 to 5	—	000	R	Reserved This bit is always read as 0. The write value should always be 0.
4, 3	TS[1:0]	00	R/W	DMA Transfer Size Specify See the description of TS[3:2] (bits 21 and 20).
2	IE	0	R/W	Interrupt Enable Specifies whether or not an interrupt request is generated to the CPU at the end of the DMA transfer. Setting this bit to 1 generates an interrupt request (DEI) to the CPU when the TE bit is set to 1. 0: Interrupt request is disabled. 1: Interrupt request is enabled.
1	TE	0	R/(W)*	Transfer End Flag The TE bit is set to 1 when data transfer ends when DMATCR becomes 0. The TE bit is not set to 1 in the following cases. • DMA transfer ends due to a DMA address error before DMATCR becomes 0. • DMA transfer is ended by clearing the DE bit and DME bit in DMAOR. To clear the TE bit, the TE bit should be written to 0 after reading 1. Even if the DE bit is set to 1 while this bit is set to 1, transfer is not enabled. 0: During the DMA transfer or DMA transfer has been interrupted [Clearing condition] Writing 0 after reading TE = 1 1: DMA transfer ends by the specified count (TCR = 0)
0	DE	0	R/W	DMA Enable Enables or disables the DMA transfer. In auto request mode, DMA transfer starts by setting the DE bit and DME bit in DMAOR to 1. At this time, both of the AE bit in DMAOR and the TE bit must be 0. In an peripheral module request, DMA transfer starts if DMA transfer request is generated by the devices or peripheral modules after setting the DE and DME bits to 1. In this case, however, both of the TE and AE bits must be 0, which is the same as in the case of auto request mode. Clearing the DE bit to 0 can terminate the DMA transfer. 0: DMA transfer disabled 1: DMA transfer enabled

Note: * Writing 0 is possible to clear the flag.

8.3.8 DMA Channel Control Register B_0 to 5 (DMACHCRB_0 to DMACHCRB_5)

The DMACHCRB registers are 32-bit readable/writable registers that control the DMA transfer mode.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	GS	GL	GCNT[3:0]				-	-	-	-	-	-	-	–
Initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	PRI[3:0]			
Initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31, 30	—	00	R	Reserved These bits are always read as 0. The write value should always be 0.
29	GS	0	R/W	Gathering Buffer Enable (Writing side) Data is transmitted collectively to the transfer destination. 0: disabled 1: enabled
28	GL	0	R/W	Gathering Buffer Enable (Reading side) Data is received collectively from the transfer source. 0: disabled 1: enabled
27 to 24	GCNT[3:0]	0000	R/W	Number of data gathering ability in gathering buffer Specify the number of data collectively transmitted with GCNT+1. The number of data transmits the transfer unit specified for the TS bits in DMACHCR. However, when the transfer size exceeds 256 bytes, the transfer size becomes 256 bytes.
31 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	PRI[3:0]	0000	R/W	Bus Request Priority Setting These bits set the priority of the bus request that is output by the DMAC. 1111: Highest priority : 0000: Lowest priority Note: For details of the PRI signal, see section 1-F Bus Functions.

8.3.9 DMA Operation Register (DMAOR)

DMAOR is a 16-bit readable/writable register that specifies the priority level of channels for the DMA transfer. This register also shows the DMA transfer status.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMS[3:0]				-	-	PR[1:0]		PPRI	-	-	-	-	AE	-	DME
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R	R	R	R	R/(W)*	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	CMS[3:0]	0000	R/W	Cycle Steal Mode Select Select either normal mode or intermittent mode in cycle steal mode. It is necessary that all channel's bus modes are set to cycle steal mode to make valid intermittent mode. 0000: Normal mode 0010: Intermittent mode 16 Executes one DMA transfer in each of 16 cycles of the external bus clock. 0011: Intermittent mode 64 Executes one DMA transfer in each of 64 cycles of the external bus clock. 0100: Intermittent mode 256 Executes one DMA transfer in each of 256 cycles of the external bus clock. Other than above: Setting prohibited
11, 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9, 8	PR[1:0]	00	R/W	Priority Mode Select the priority level between channels when there are transfer requests for multiple channels simultaneously. 00: CH0 > CH1 > CH2 > CH3 > CH4 > CH5 01: CH0 > CH2 > CH3 > CH1 > CH4 > CH5 10: Round-robin mode with top priority placed on CH0 11: Round-robin mode
7	PPRI	0	R/W	Bus Request Priority Push out Assigns the highest DMA bus request priority setting for channels performing DMA transfer as the value of bus request priority being currently output to the SHWY. 0: Normal mode 1: Bus request priority push out
6 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

2	AE	0	R/(W)*	Address Error Flag Indicates that an address error interrupt occurred during DMA transfer. This bit is set under following conditions: • The value set in DMASAR or DMADAR does not match the transfer size boundary. • The transfer source or transfer destination is invalid space. • The transfer source or transfer destination is in module stop mode If this bit is set, DMA transfer is not enabled for the channel even if the DE bit is set to 1. To clear the AE bit, write 0 to the AE bit after reading 1 from the bit or clear the CAE bit for each channel. (Clearing the AE bit clears the channel address errors for all channels.) 0: No DMAC address error interrupt [Clearing condition] Writing CAE = 0 after reading CAE = 1 1: DMAC address error interrupt occurs during DMA transfer
1	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
0	DME	0	R/W	DMA Master Enable Enables or disables DMA transfers on all channels. If the DME bit and the DE bit in DMACHCR are set to 1, DMA transfer is enabled. At this time, the TE bits in DMACHCR and the AE bits in DMAOR must be all 0. If this bit is cleared during transfer, transfers in all channels are terminated. 0: Disables DMA transfers on all channels 1: Enables DMA transfers on all channels

Note: * Writing 0 is possible to clear the flag.

8.3.10 DMA Channel Clear Register 0 to 5 (CHCLR_0 to CHCLR_5)

The CHCLR registers are 32-bit readable/writable registers that clear the buffer of each channel.

Bit	:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value	:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		—	—	—	—	—	—	—	RP[4:0]					—	—	—	CLR
Initial value	:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	W

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8 to 4	RP[4:0]	All 0	R	Number of data in buffer of channel The number of data that remains in the buffer of the channel is read. Units of the number of data are the DMA transfer size.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	CLR	0	W	Channel Clear Bit When writing 0 to the bit, the buffer of channel to be cleared. Writing is prohibited during DMA operating.

8.3.11 DMA Extended Resource Selectors 0 to 2 (DMARS_0 to DMARS_2)

The DMARS registers are 16-bit readable/writable registers that specify the peripheral module as the source of the DMA transfer request for each channel. DMARS_0 specifies for channels 0 and 1, DMARS_1 specifies for channels 2 and 3, and DMARS_2 specifies for channels 4 and 5.

When MID/RID is set to a value other than the values listed in Table 8.7, the operation of this LSI is not guaranteed. The transfer request from DMARS is valid only when the resource select bits (RS[3:0]) have been set to B'1000 for DMACHCR_0 to DMACHCR_5. Otherwise, even if DMARS has been set, transfer request source is not accepted.

DMARS_0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	C1MID[5:0]						C1RID[1:0]		C0MID[5:0]						C0RID[1:0]	
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	C1MID[5:0]	000000	R/W	Transfer request module ID5 to ID0 for DMA channel 1 (MID) See Table 8.7.
9, 8	C1RID[1:0]	00	R/W	Transfer request register ID1 and ID0 for DMA channel 1 (RID) See Table 8.7.
7 to 2	C0MID[5:0]	000000	R/W	Transfer request module ID5 to ID0 for DMA channel 0 (MID) See Table 8.7.
1, 0	C0RID[1:0]	00	R/W	Transfer request register ID1 and ID0 for DMA channel 0 (RID) See Table 8.7.

DMARS_1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	C3MID[5:0]						C3RID[1:0]		C2MID[5:0]						C2RID[1:0]	
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	C3MID[5:0]	000000	R/W	Transfer request module ID5 to ID0 for DMA channel 3 (MID) See Table 8.7.
9, 8	C3RID[1:0]	00	R/W	Transfer request register ID1 and ID0 for DMA channel 3 (RID) See Table 8.7.
7 to 2	C2MID[5:0]	000000	R/W	Transfer request module ID5 to ID0 for DMA channel 2 (MID) See Table 8.7.
1, 0	C2RID[1:0]	00	R/W	Transfer request register ID1 and ID0 for DMA channel 2 (RID) See Table 8.7.

DMARS_2

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	C5MID[5:0]						C5RID[1:0]		C4MID[5:0]						C4RID[1:0]	
Initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	C5MID[5:0]	000000	R/W	Transfer request module ID5 to ID0 for DMA channel 5 (MID) See Table 8.7.
9, 8	C5RID[1:0]	00	R/W	Transfer request register ID1 and ID0 for DMA channel 5 (RID) See Table 8.7.
7 to 2	C4MID[5:0]	000000	R/W	Transfer request module ID5 to ID0 for DMA channel 4 (MID) See Table 8.7.
1, 0	C4RID[1:0]	00	R/W	Transfer request register ID1 and ID0 for DMA channel 4 (RID) See Table 8.7.

Table 8.7 Transfer Request Sources

Peripheral Module	Setting Value for One Channel (MID + RID)	MID	RID	Function
BBIF1	H'5A	B'010110	B'10	Receive
BBIF1	H'59	B'010110	B'01	Transmit
BBIF2	H'5E	B'010111	B'10	Receive
BBIF2	H'5D	B'010111	B'01	Transmit
CMT1	H'07	B'000001	B'11	Transmit and receive
FLCTL0	H'83	B'100000	B'11	Transmit and receive the data part
FLCTL1	H'87	B'100001	B'11	Transmit and receive the control code part
IIC0	H'62	B'011000	B'10	Receive
IIC0	H'61	B'011000	B'01	Transmit
IIC1	H'66	B'011001	B'10	Receive
IIC1	H'65	B'011001	B'01	Transmit
IIC2	H'6A	B'011010	B'10	Receive
IIC2	H'69	B'011010	B'01	Transmit
IIC3	H'6E	B'011011	B'10	Receive
IIC3	H'6D	B'011011	B'01	Transmit
IIC4	H'72	B'011100	B'10	Receive
IIC4	H'71	B'011100	B'01	Transmit
MSIOF0	H'52	B'010100	B'10	Receive
MSIOF0	H'51	B'010100	B'01	Transmit
MSIOF1	H'56	B'010101	B'10	Receive
MSIOF1	H'55	B'010101	B'01	Transmit
MSIOF2	H'42	B'010000	B'10	Receive
MSIOF2	H'41	B'010000	B'01	Transmit
SCIFA0	H'22	B'001000	B'10	Receive
SCIFA0	H'21	B'001000	B'01	Transmit
SCIFA1	H'26	B'001001	B'10	Receive
SCIFA1	H'25	B'001001	B'01	Transmit
SCIFA2	H'2A	B'001010	B'10	Receive
SCIFA2	H'29	B'001010	B'01	Transmit
SCIFA3	H'2E	B'001011	B'10	Receive
SCIFA3	H'2D	B'001011	B'01	Transmit
SCIFA4	H'3A	B'001110	B'10	Receive
SCIFA4	H'39	B'001110	B'01	Transmit
SCIFA5	H'36	B’001101	B'10	Receive
SCIFA5	H'35	B’001101	B'01	Transmit
SCIFB	H'3E	B'001111	B'10	Receive
SCIFB	H'3D	B'001111	B'01	Transmit
SDHI0	H'C2	B'110000	B'10	Receive

Peripheral Module	Setting Value for One Channel (MID + RID)	MID	RID	Function
SDHI0	H'C1	B'110000	B'01	Transmit
SDHI0	H'C6	B'110001	B'10	Receive
SDHI0	H'C5	B'110001	B'01	Transmit
SDHI1	H'CA	B'110010	B'10	Receive
SDHI1	H'C9	B'110010	B'01	Transmit
SDHI2	H'CE	B'110011	B'10	Receive
SDHI2	H'CD	B'110011	B'01	Transmit
FSIA	H’B2	B’101100	B’10	Receive
FSIA	H’B1	B’101100	B’01	Transmit
FSIB	H’B5	B’101101	B’01	Transmit
TPU0	H'F1	B'111100	B'01	Transmit
TSIF0	H'EA	B'111010	B'10	Receive
TSIF1	H'EE	B'111011	B'10	Receive
IRDA	H'32	B'001100	B'10	Receive
DSI0	H’92	B’100100	B’10	Receive
DSI1	H’96	B’100101	B’10	Receive
HSI0	H’0A	B’000010	B’10	Receive
HSI0	H’09	B’000010	B’01	Transmit
HSI1	H’0E	B’000011	B’10	Receive
HSI1	H’0D	B’000011	B’01	Transmit
HSI2	H’12	B’000100	B’10	Receive
HSI2	H’11	B’000100	B’01	Transmit
HSI3	H’16	B’000101	B’10	Receive
HSI3	H’15	B’000101	B’01	Transmit
MMC	H’D2	B’110100	B’10	Receive
MMC	H’D1	B’110100	B’01	Transmit
MFI	H’E7	B’111001	B’11	Receive
MFI	H’E3	B’111000	B’11	Transmit
SHWYSTATR	H’A6	B’101001	B’10	Receive
SHWYSTATH	H’9E	B’100111	B’10	Receive
SHWYSTATC	H’AA	B’101010	B’10	Receive

8.4 Operation

When there is a DMA transfer request, the DMAC starts the transfer according to the predetermined channel priority; when the transfer end conditions are satisfied, it ends the transfer. Transfers can be requested in two modes: auto request, and on-chip peripheral module request. As bus mode, cycle steal mode (normal mode and intermittent mode) is used.

8.4.1 DMA Transfer Requests

DMA transfer requests are basically generated in either the data transfer source or destination, but they can also be generated by on-chip peripheral modules that are neither the source nor the destination. Transfers can be requested in two modes: auto request, and on-chip peripheral module request. The request mode is selected for each channel in the RS[3:0] bits in DMACHCR, DMARS0 to DMARS2.

(1) Auto-Request Mode

When there is no transfer request signal from an external source, as in a memory-to-memory transfer or a transfer between memory and an on-chip peripheral module unable to request a transfer, auto-request mode allows the DMAC to automatically generate a transfer request signal internally. When the DE bit in DMACHCR and the DME bit in DMAOR are set to 1 for the target channel, the transfer begins so long as the CAE bit in DMACHCRR is 0.

(2) On-Chip Peripheral Module Request Mode

In this mode, a transfer is performed at the transfer request signal of an on-chip peripheral module. The source (peripheral module) of the DMA transfer request is specified by the DMARS_0/1/2 register.

When this mode is selected, if the DMA transfer is enabled (DE = 1, DME = 1, TE = 0, CAE = 0), a transfer is performed upon the input of a transfer request signal.

When a transmit data empty transfer request of the SCIF is set as the transfer request, the transfer destination must be the SCIF's transmit data register. Likewise, when receive data full transfer request of the SCIF is set as the transfer request, the transfer source must be the SCIF's receive data register. These conditions also apply to the other on-chip peripheral modules.

The number of the receive FIFO triggers can be set as a transfer request depending on an on-chip peripheral module. Data needs to be read after the DMA transfer is ended, because data may be left in the receive FIFO when the receive FIFO trigger condition is not satisfied.

Table 8.8 Selecting On-Chip Peripheral Module Request Modes with Bits RS3 to RS0 (T.B.D.)

CHCR	DMARS		DMA Transfer Request Source	DMA Transfer Request Signal	Source	Destination	Bus Mode
RS[3:0]	MID	RID					
1000	000001	11	CMT1	Transmit and receive request	Any	Any	Cycle steal
	001000	01	SCIFA0 transmitter	TXI (Transmit FIFO data empty)	Any	SCAFTDR0	Cycle steal
		10	SCIFA0 receiver	RXI (Receive FIFO data full)	SCAFRDR0	Any	Cycle steal
	001001	01	SCIFA1 transmitter	TXI (Transmit FIFO data empty)	Any	SCAFTDR1	Cycle steal
		10	SCIFA1 receiver	RXI (Receive FIFO data full)	SCAFRDR11	Any	Cycle steal
	001010	01	SCIFA2 transmitter	TXI (Transmit FIFO data empty)	Any	SCAFTDR2	Cycle steal
		10	SCIFA2 receiver	RXI (Receive FIFO data full)	SCAFRDR2	Any	Cycle steal
	001011	01	SCIFA3 transmitter	TXI (Transmit FIFO data empty)	Any	SCAFTDR3	Cycle steal
		10	SCIFA3 receiver	RXI (Receive FIFO data full)	SCAFRDR3	Any	Cycle steal
	001110	01	SCIFA4 transmitter	TXI (Transmit FIFO data empty)	Any	SCAFTDR4	Cycle steal
		10	SCIFA4 receiver	RXI (Receive FIFO data full)	SCAFRDR4	Any	Cycle steal
	001101	01	SCIFA5 transmitter	TXI (Transmit FIFO data empty)	Any	SCAFTDR5	Cycle steal
		10	SCIFA5 receiver	RXI (Receive FIFO data full)	SCAFRDR5	Any	Cycle steal
	001110	01	SCIFB transmitter	TXI (Transmit FIFO data empty)	Any	SCBFTDR	Cycle steal
		10	SCIFB receiver	RXI (Receive FIFO data full)	SCBFRDR	Any	Cycle steal
	010100	01	MSIOF0 transmitter	TXI (Transmit data request)	Any	SITDR	Cycle steal
		10	MSIOF0 receiver	RXI (Receive data request)	SIRDR	Any	Cycle steal
	010101	01	MSIOF1 transmitter	TXI (Transmit data request)	Any	SITDR	Cycle steal
		10	MSIOF1 receiver	RXI (Receive data request)	SIRDR	Any	Cycle steal
	010000	01	MSIOF2 transmitter	TXI (Transmit data request)	Any	SITDR	Cycle steal
		10	MSIOF2 receiver	RXI (Receive data request)	SIRDR	Any	Cycle steal
	010110	01	BBIF1 transmitter	TXI (Transmit data request)	Any	SITFDR	Cycle steal
		10	BBIF1 receiver	RXI (Receive data request)	SIRFDR	Any	Cycle steal

CHCR	DMARS		DMA Transfer Request Source	DMA Transfer Request Signal	Source	Destination	Bus Mode
RS[3:0]	MID	RID					
	010111	01	BBIF2 transmitter	TXI (Transmit data request)	Any	SITFDR	Cycle steal
		10	BBIF2 receiver	RXI (Receive data request)	SIRFDR	Any	Cycle steal
	011000	01	IIC0	Transmit empty transfer request	Any	Data register	Cycle steal
		10		Receive full transfer request	Data register	Any	Cycle steal
	011001	01	IIC1	Transmit empty transfer request	Any	Data register	Cycle steal
		10		Receive full transfer request	Data register	Any	Cycle steal
	011010	01	IIC2	Transmit empty transfer request	Any	Data register	Cycle steal
		10		Receive full transfer request	Data register	Any	Cycle steal
	011011	01	IIC3	Transmit empty transfer request	Any	Data register	Cycle steal
		10		Receive full transfer request	Data register	Any	Cycle steal
	011100	01	IIC4	Transmit empty transfer request	Any	Data register	Cycle steal
		10		Receive full transfer request	Data register	Any	Cycle steal
	100000	11	FLCTL data part transmit	Transmit FIFO data empty request	Any	FLDTFIFO	Cycle steal
			FLCTL data part receive	Receive FIFO data full request	FLDTFIFO	Any	Cycle steal
	100001	11	FLCTL control code part transmit	Transmit FIFO data empty request	Any	FLECFIFO	Cycle steal
			FLCTL control code part receive	Receive FIFO data full request	FLECFIFO	Any	Cycle steal
	101100	01	FSIA	Transmit empty transfer request (port A)	Any	A_DODT	Cycle steal
		10		Receive full transfer request (port A)	A_DIDT	Any	Cycle steal
	101101	01	FSIB	Transmit empty transfer request (port B)	Any	B_DODT	Cycle steal
	110000	01	SDHI0 channel 0	Transmit empty transfer request	Any	Data register	Cycle steal
		10	SDHI0 channel 1	Receive full transfer request	Data register	Any	Cycle steal
	110001	01	SDHI0 channel 2	Transmit empty transfer request	Any	Data register	Cycle steal
		10	SDHI0 channel 3	Receive full transfer request	Data register	Any	Cycle steal
	110010	01	SDHI1 channel 0	Transmit empty transfer request	Any	Data register	Cycle steal

CHCR	DMARS		DMA Transfer Request Source	DMA Transfer Request Signal	Source	Destination	Bus Mode
RS[3:0]	MID	RID					
		10	SDHI1 channel 1	Receive full transfer request	Data register	Any	Cycle steal
	110011	01	SDHI2 channel 0	Transmit empty transfer request	Any	Data register	Cycle steal
		10	SDHI2 channel 1	Receive full transfer request	Data register	Any	Cycle steal
	111100	01	TPU0	Transmit empty transfer request	Any	Data register	Cycle steal
	111010	10	TSIF0	Receive full transfer request	TSTSDR	Any	Cycle steal
	111011	10	TSIF1	Receive full transfer request	TSTSDR	Any	Cycle steal
	001100	10	IRDA	Receive transfer request	IrDA buffer RAM	Any	Cycle steal
	100100	10	DSI0	RXI (Receive data request)	Data register	Any	Cycle steal
	100101	10	DSI1	RXI (Receive data request)	Data register	Any	Cycle steal
	000010	01	HSI0	TXI (Transmit data request)	Any	Data register	Cycle steal
	000010	10		RXI (Receive data request)	Data register	Any	Cycle steal
	000011	01	HSI1	TXI (Transmit data request)	Any	Data register	Cycle steal
	000011	10		RXI (Receive data request)	Data register	Any	Cycle steal
	000100	01	HSI2	TXI (Transmit data request)	Any	Data register	Cycle steal
	000100	10		RXI (Receive data request)	Data register	Any	Cycle steal
	000101	01	HSI3	TXI (Transmit data request)	Any	Data register	Cycle steal
	000101	10		RXI (Receive data request)	Data register	Any	Cycle steal
	110100	01	MMC	TXI (Transmit data request)	Any	Data register	Cycle steal
	110100	10		RXI (Receive data request)	Data register	Any	Cycle steal
	111000	11	MFI	TXI (Transmit data request)	Any	Data register	Cycle steal
	111001	11		RXI (Receive data request)	Data register	Any	Cycle steal
	101001	10	SHWYSTATR	RXI (Receive data request)	Data register	Any	Cycle steal
	100111	10	SHWYSTATH	RXI (Receive data request)	Data register	Any	Cycle steal
	101010	10	SHWYSTATC	RXI (Receive data request)	Data register	Any	Cycle steal

8.4.2 Channel Priority

When the DMAC receives simultaneous transfer requests on two or more channels, it transfers data according to a predetermined priority. Two modes (fixed mode and round-robin mode) are selected by the PR[1:0] bits in DMAOR.

(1) Fixed Mode

In this mode, the priority levels among the channels remain fixed. There are two kinds of fixed modes as follows:

- CH0 > CH1 > CH2 > CH3 > CH4 > CH5
- CH0 > CH2 > CH3 > CH1 > CH4 > CH5

These are selected by the PR[1:0] bits in DMAOR.

(2) Round-Robin Mode

In round-robin mode each time data of one transfer unit (byte, word, longword, 8-byte, 16-byte, or 32-byte unit) is transferred on one channel, the priority is rotated. The channel on which the transfer was just finished rotates to the bottom of the priority. The round-robin mode operation is shown in Figure 8.2. The priority of round-robin mode is CH0 > CH1 > CH2 > CH3 > CH4 > CH5 immediately after reset.

(3) CH0 Top Priority Round-Robin Mode

In this mode, the round-robin mode function is enabled for the channels from CH1 to CH5, with CH0 being always transferred at top priority. Once the transfer of CH0 is completed, the priority order will be the same as that applicable before the transfer.

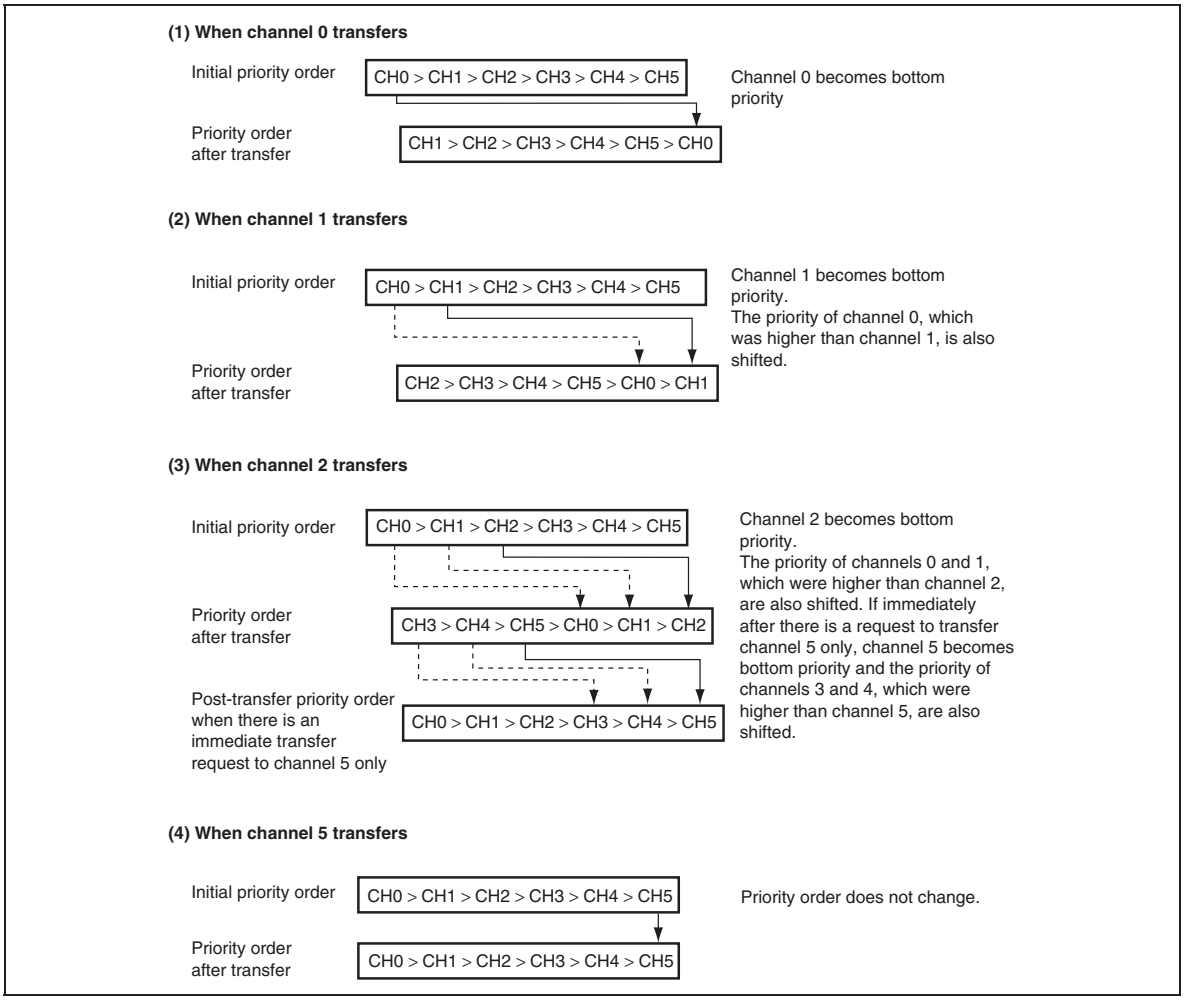


Figure 8.2 Round-Robin Mode

Figure 8.3 shows how the priority changes when channel 0 and channel 3 transfers are requested simultaneously and a channel 1 transfer is requested during the channel 0 transfer. The DMAC operates as follows:

1. Transfer requests are generated simultaneously to channels 0 and 3.
2. Channel 0 has a higher priority, so the channel 0 transfer begins first (channel 3 waits for transfer).
3. A channel 1 transfer request occurs during the channel 0 transfer (channels 1 and 3 are both waiting)
4. When the channel 0 transfer ends, channel 0 becomes lowest priority.
5. At this point, channel 1 has a higher priority than channel 3, so the channel 1 transfer begins (channel 3 waits for transfer).
6. When the channel 1 transfer ends, channel 1 becomes lowest priority.
7. The channel 3 transfer begins.
8. When the channel 3 transfer ends, channels 3 and 2 shift downward in priority so that channel 3 becomes the lowest priority.

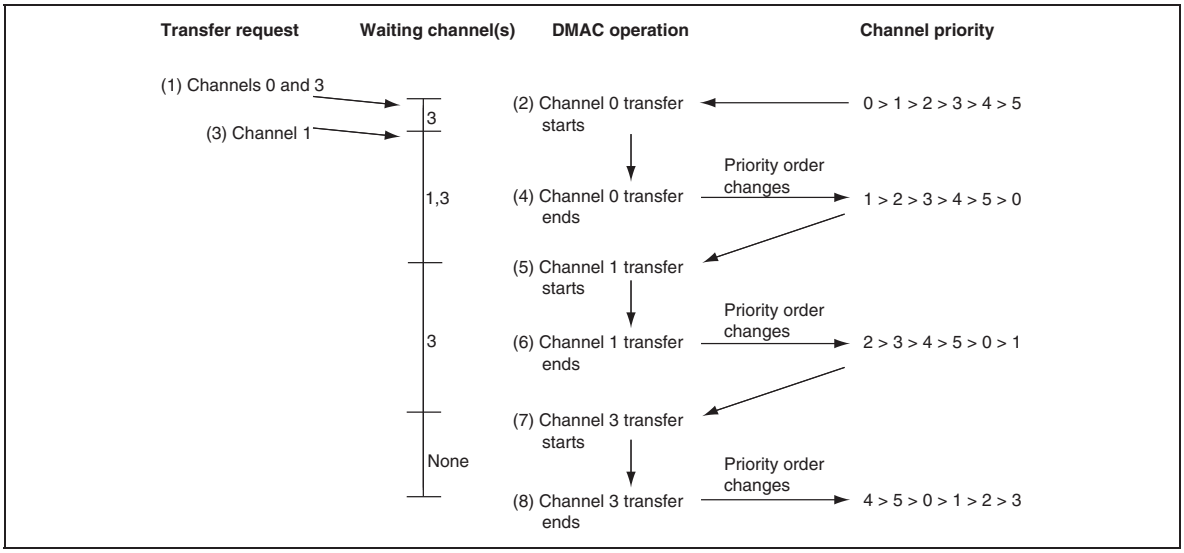


Figure 8.3 Changes in Channel Priority in Round-Robin Mode

8.4.3 Bus Request Priority Push out

The bus request priority push out is a function that assigns the highest value of the bus request priority setting bit in the DMA channel control register B among the output-enabled channels (channels in auto-request mode or channels that accepted a request) as the value of bus request priority being currently output to the SHWY.

Enabling this function prevents the processing of channels with higher bus request priority from being delayed by the presence of channels with lower bus request priority.

Figure 8.4 shows an example in which the bus request priority push out function is enabled.

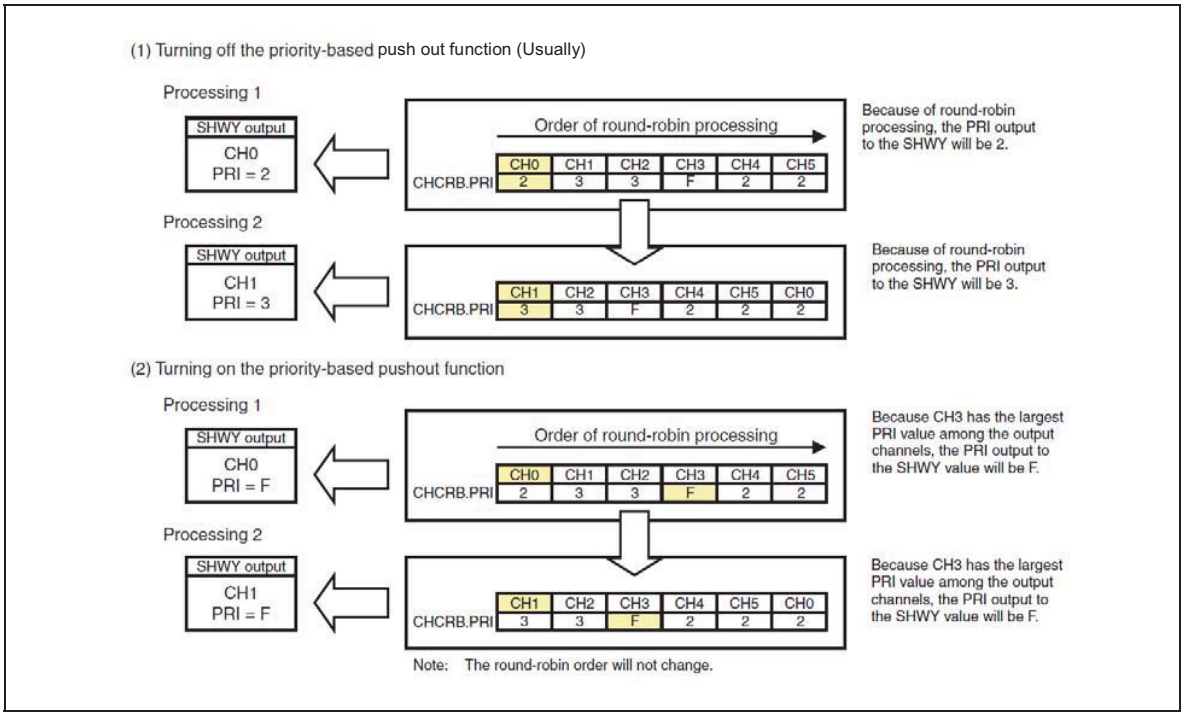


Figure 8.4 Example of Using the Bus Request Priority Push out Function

Note: For details of the PRI signal, see section 1-F Bus Functions.

8.4.4 DMA Transfer Types

DMA transfer is done in dual address mode. As bus mode, cycle steal mode (normal mode and intermittent mode) is used. The DMAC supports the transfers shown in Table 8.9.

Table 8.9 Supported DMA Transfers

	Destination			
Source	**External Memory**	**Memory-Mapped External Device**	**On-Chip Peripheral Module**	**X/Y Memory**
External device with DACK	Dual	Dual	Not available	Not available
External memory	Dual	Dual	Dual	Dual
Memory-mapped external device	Dual	Dual	Dual	Dual
On-chip peripheral module	Dual	Dual	Dual	Dual
X/Y memory	Dual	Dual	Dual	Dual

Note: 1. Dual: Dual address mode

(1) Address Mode

(a) Dual Address Mode

In dual address mode, both the transfer source and destination are accessed by addresses. The source and destination can be located externally or internally.

DMA transfer requires two bus cycles because data is read from the transfer source in a data read cycle and written to the transfer destination in a data write cycle. At this time, transfer data is temporarily stored in the DMAC. In the transfer between external memories as shown in Figure 8.5, data is read to the DMAC from one external memory in a data read cycle, and then that data is written to the other external memory in a write cycle.

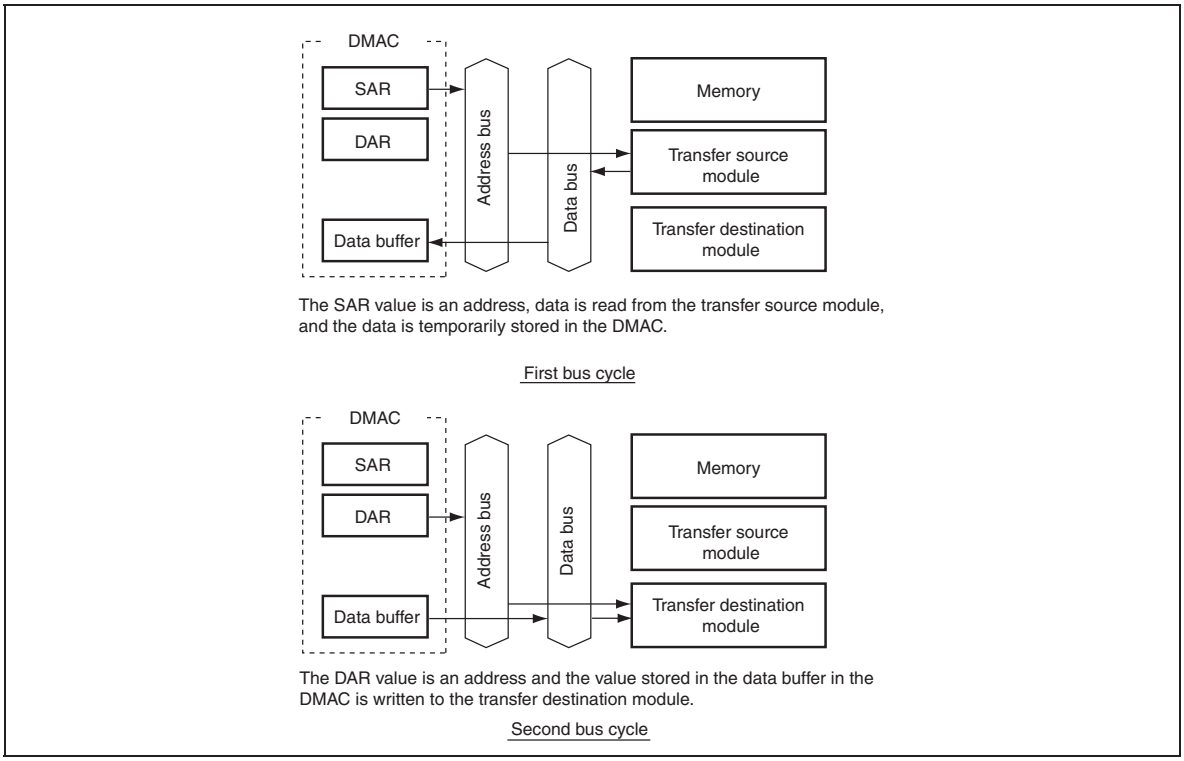


Figure 8.5 Data Flow of Dual Address Mode

Auto request, and on-chip peripheral module request are available for the transfer request.

(2) Bus Modes

Cycle steal mode is used as bus mode.

(a) Cycle-Steal Mode

- Normal mode

  In cycle-steal normal mode, the DMAC gives the bus mastership to another bus master every time a unit of transfer (byte, word, longword, 8-byte, 16-byte, 32-byte, or 64-byte unit) is complete. When another transfer request occurs after that, the DMAC gets the bus mastership from the other bus master and performs a transfer for one transfer unit. When that transfer ends, the DMAC returns the bus mastership to the other bus master. This is repeated until the transfer end conditions are satisfied.

  In cycle-steal normal mode, all transfer areas are available for the transfer request source, transfer source, and transfer destination.

  Figure 8.6 shows an example of DMA transfer timing in cycle-steal normal mode. Transfer conditions shown in the figure are:

  — Condition 1: Dual address mode

  — Condition 2: DREQ low level detection

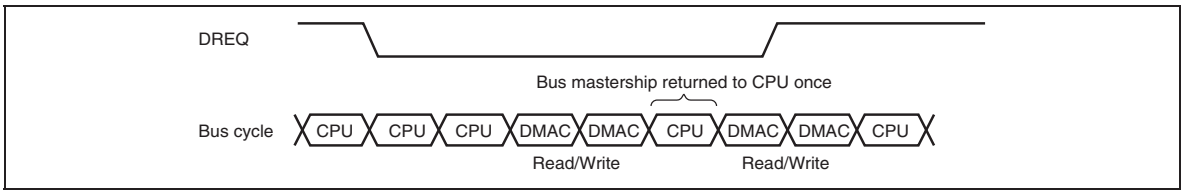


Figure 8.6 DMA Transfer Example in Cycle-Steal Normal Mode (Dual Address, DREQ Low Level Detection)

- Intermittent mode

  In intermittent mode of cycle steal, the DMAC gives the bus mastership to another bus master every time a unit of transfer (byte, word, longword, 8-byte, 16-byte, 32-byte or 64-byte unit) is complete. When another transfer request occurs after that, the DMAC gets the bus mastership from the other bus master after waiting for 16, 64, or 256 clock cycles in ZSϕ count. The DMAC then transfers data of one unit and returns the bus mastership to the other bus master. This is repeated until the transfer end conditions are satisfied. It is thus possible to make lower the ratio of bus occupation by DMA transfer than cycle-steal normal mode.

  When the DMAC gets again the bus mastership, DMA transfer can be postponed in case of entry updating due to cache miss.

  In intermittent mode, all transfer areas are available for the transfer request source, transfer source, and transfer destination. The bus modes, however, must be cycle steal mode in all channels.

  Figure 8.7 shows an example of DMA transfer timing in cycle steal intermittent mode. Transfer conditions shown in the figure are:

  — Condition 1: Dual address mode

  — Condition 2: DREQ low level detection

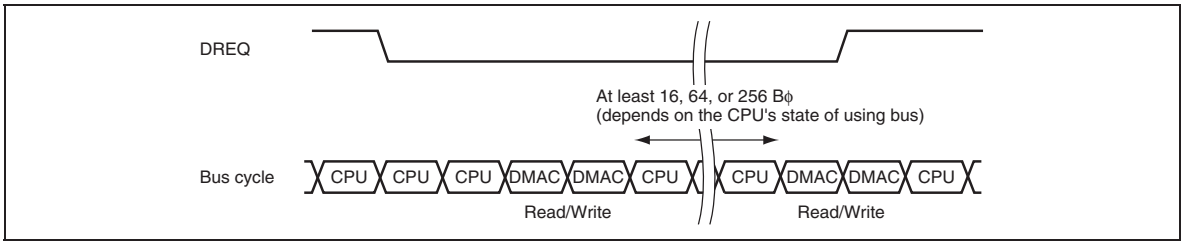


Figure 8.7 Example of DMA Transfer in Cycle Steal Intermittent Mode (Dual Address, DREQ Low Level Detection)

(3) Relationship between Request Modes and Bus Modes by DMA Transfer Category

Table 8.10 shows the relationship between request modes and bus modes by DMA transfer category.

Table 8.10 Relationship between Request Modes and Bus Modes by DMA Transfer Category

Address Mode	Transfer Category	Request Mode	Bus Mode	Transfer Size (Bits)	Usable Channels
Dual	External memory and external memory	External, auto	C	1/2/4/8/16/32/64	0 to 5
	External memory and memory-mapped external device	External, auto	C	1/2/4/8/16/32/64	0 to 5
	Memory-mapped external device and memory-mapped external device	External, auto	C	1/2/4/8/16/32/64	0 to 5
	External memory and on-chip peripheral module	All*[1]	C	1/2/4/8/16/32/64*[2]	0 to 5
	Memory-mapped external device and on-chip peripheral module	All*[1]	C	1/2/4/8/16/32/64*[2]	0 to 5
	On-chip peripheral module and on-chip peripheral module	All*[1]	C	1/2/4/8/16/32/64*[2]	0 to 5
	X/Y memory and X/Y memory	External, auto	C	1/2/4/8/16/32/64	0 to 5
	X/Y memory and memory-mapped external device	External, auto	C	1/2/4/8/16/32/64	0 to 5
	X/Y memory and on-chip peripheral module	All*[1]	C	1/2/4/8/16/32/64*[2]	0 to 5
	X/Y memory and external memory	External, auto	C	1/2/4/8/16/32/64	0 to 5

[Legend]

C: Cycle steal mode

Notes: 1. Auto requests, and on-chip peripheral module requests are all available. However the request source register must be designated as the transfer source or the transfer destination.

2. Access size permitted for the on-chip peripheral module register functioning as the transfer source or transfer destination.

Table 8.11 DMA transfer size according to module

Module	1 byte	2 byte	4 byte	16 byte	32 byte	DREQPAK
BBIF1/2	O	O	O			O
CMT1*						
FLCTL			O	O		
IIC 0/1/2/3/4		O				
MSIOF0/1/2	O	O	O			O
SCIF0/1/2/3/4/5,SCIFB	O					O
SDHI0/1/2		O		O	O	
FSI			O			
TPU0		O				
TSIF0/1			O			O
IRDA					O	
DSI0/1			O			
HSI			O			O
MMC			O			
MFI				O		
SHWYSTAT			O		O	

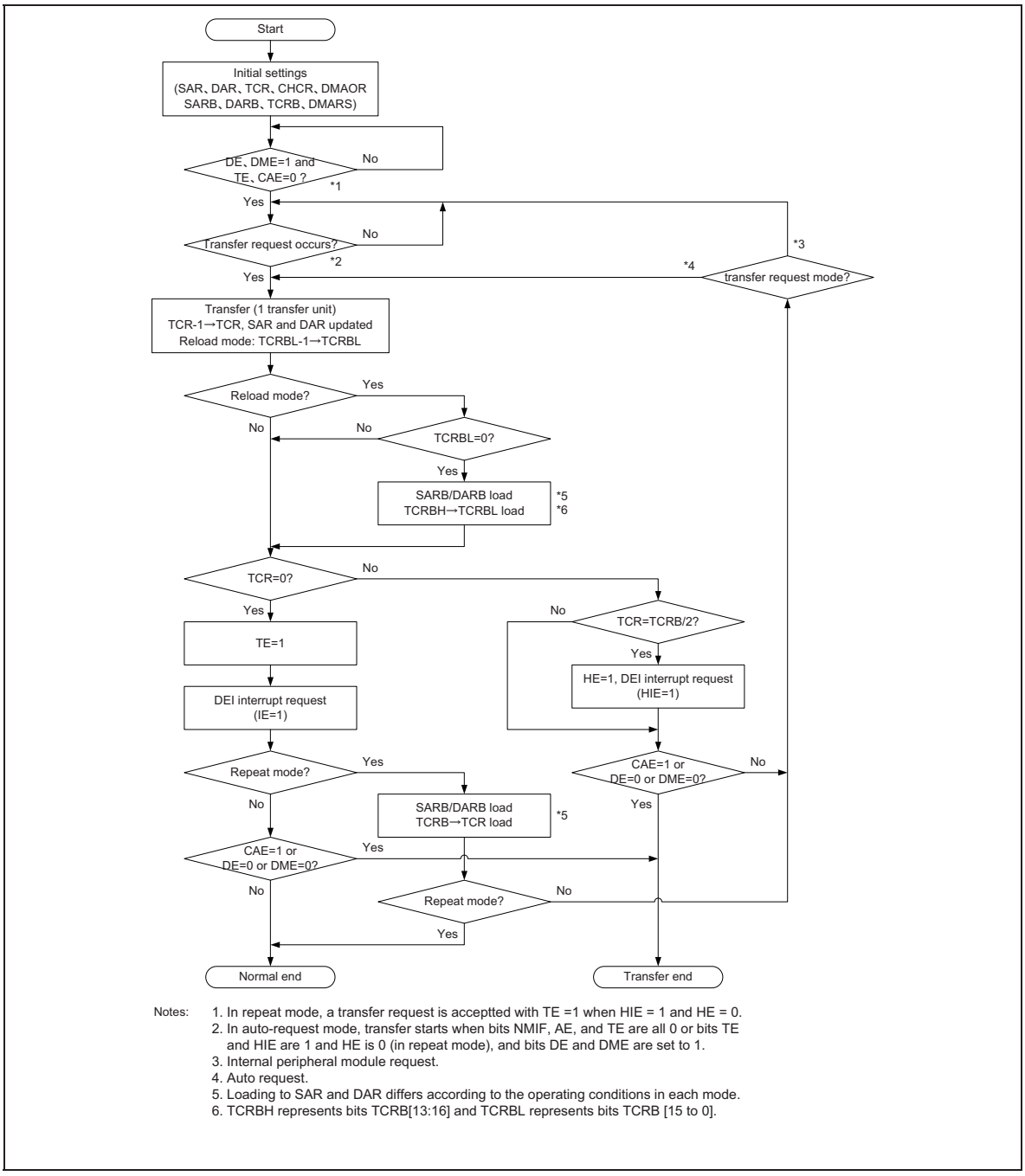
notes : * Never transmits directly to CMT1.

8.4.5 DMA Transfer Flow

After the DMA source address registers (DMASAR), DMA destination address registers (DMADAR), DMA transfer count registers (DMATCR), DMA channel control registers (DMACHCR), DMA operation register (DMAOR), and DMA extended resource selectors (DMARS) are set, the DMAC transfers data according to the following procedure:

1. Checks to see if transfer is enabled (DE = 1, DME = 1, TE = 0, CAE = 0)
2. When a transfer request occurs while transfer is enabled, the DMAC transfers one transfer unit of data (depending on the setting of the TS3 to TS0 bits). In auto request mode, the transfer begins automatically when the DE bit and DME bit are set to 1. The DMATCR value will be decremented for each transfer. The actual transfer flows vary by address mode and bus mode.
3. When the specified number of transfers have been completed (when DMATCR reaches 0), the transfer ends normally. If the IE bit in DMACHCR is set to 1 at this time, a DEI interrupt is sent to the CPU.
4. When an address error is generated, the transfer is aborted. Transfers are also aborted when the DE bit in DMACHCR or the DME bit in DMAOR is changed to 0.

Figure 8.8 shows a flowchart of this procedure.



Notes:
1. In repeat mode, a transfer request is acceptted with TE =1 when HIE = 1 and HE = 0.
2. In auto-request mode, transfer starts when bits NMIF, AE, and TE are all 0 or bits TE and HIE are 1 and HE is 0 (in repeat mode), and bits DE and DME are set to 1.
3. Internal peripheral module request.
4. Auto request.
5. Loading to SAR and DAR differs according to the operating conditions in each mode.
6. TCRBH represents bits TCRB[13:16] and TCRBL represents bits TCRB [15 to 0].

Figure 8.8 DMA Transfer Flowchart

8.4.6 Repeat Mode Transfer

In a repeat mode transfer, a DMA transfer is repeated without making the transfer settings every time before executing a transfer.

Using a repeat mode transfer with the half end function allows a double buffer transfer executed virtually. The following procedures can be executed effectively by using a repeat mode transfer. As an example, operation of receiving voice data from the VOICE CODEC and compressing it is explained.

In the following example, processing of compressing 40-word voice data for every data reception is explained. In this case, it is assumed that voice data is received by means of MSIOF.

1. DMAC settings
- Set address of the MSIOF receive data register in DMASAR
- Set address of an internal memory data store area in DMADAR
- Set DMATCR to 80 (H'50)
- Make the following settings of DMACHCR
  Bits RPT[2:0] = B'010: Repeat mode (use DAR as a repeat area)
  Bit HIE = B'1: TCR/2 interrupt generated
  Bits DM[1:0] = B'01: DAR incremented
  Bits SM[1:0] = B'00: SAR fixed
  Bit IE = B'1: Interrupt enabled
  Bit DE = B'1: DMA transfer enabled
- Set such as bits TB and TS[2:0] according to use conditions
- Set bits CMS[3:0] and PR[1:0] in DMAOR according to use conditions and set the DME bit to B'1

2. Voice data is received and then transferred by MSIOF/DMAC
3. DMATCR is decreased to half of its initial value and an interrupt is generated
   Read DMACHCR to confirm that the HE bit is set to 1 by an interrupt processing, and compress 40-word voice data from the address set in DMADAR.
4. DMATCR is cleared to 0 and an interrupt is generated
   Read DMACHCR to confirm that the TE bit is set to 1 by an interrupt processing, and compress 40-word voice data from the address set in DMADAR + 40. After this operation, the value of DMADARB is copied to DMADAR in DMAC and initialized, and the value of DMATCRB is copied to DMATCR and initialized to 80.
5. Hereafter, steps 2 and 3 are repeated until bit DME or DE is set to B'0.

As explained above, a repeat mode transfer enables sequential voice compression by switching a buffer for storing data received consequentially and a data buffer for processing signals alternately.

8.4.7 Reload Mode Transfer

In a reload mode transfer, according to the settings of bits RPT[2:0] in DMACHCR, the value set in DMASARB/DMADARB is set to DMASAR/DMADAR and the value of bits DMATCRB[31:16] is set in bits DMATCRB[15:0] every time the number of transfers specified in the DMATCRB[15:0] bits are completed, and the transfer is repeated until DMATCR becomes 0 without specifying the transfer settings again. A reload mode transfer is effective when repeating data transfer with specific areas. Figure 8.9 shows the operation of reload mode transfer.

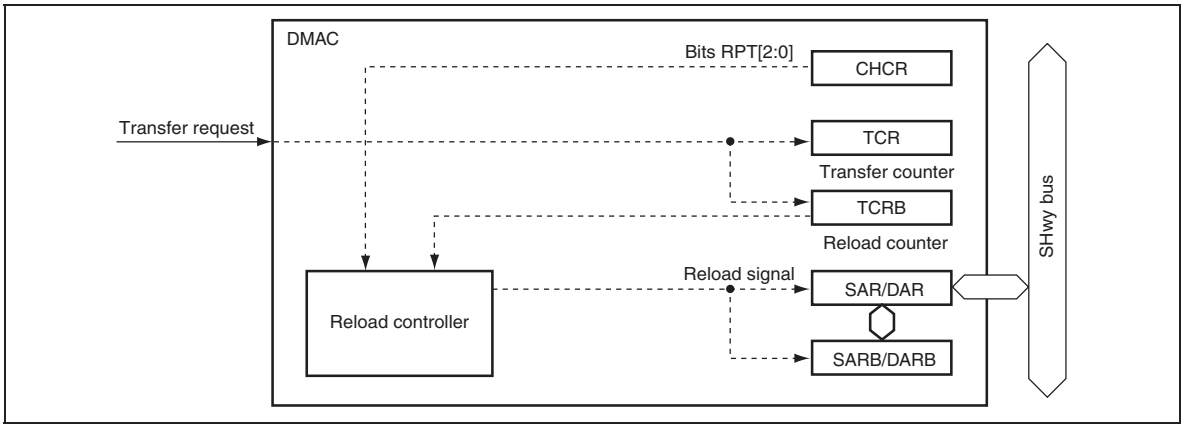


Figure 8.9 Reload Mode Transfer

When a reload mode transfer is executed, DMATCRB is used as a reload counter. Set DMATCRB as described in section 8.3.7, DMA Transfer Count Registers B_0 to 5 (DMATCRB_0 to DMATCRB_5).

8.4.8 Gathering Buffer Function

When the gathering buffer function is made effective, receive data or the transmission data is transmitted collectively in 256 bytes or less. The penalty by the row address mistake of a different bank is reduced to SDRAM by collectively transmitting, and the performance of the transmission improves.

Write 0 to the GL bits in DMACHCRB when you make this function effective on the receiving side. Write 0 to the GS bits in DMACHCRB when you make this function effective at the transmitting side. And, set the GCNT bits in DMACHCRB. After, begin the DMA transfer. This function transmits the size specified for the TS bits in DMACHCR data GCNT+1 collectively. However, when the transfer size exceeds 256 bytes, the transfer size becomes 256 bytes.

When the RS bits in DMACHCR is DMA Extended Resource Selector (B'1000), On-chip peripheral module side can not enable the gathering buffer function.

When the RS bits in DMACHCR is DMA Extended Resource Selector (B'1000), the data that remains in the buffer is output to the memory when writing 0 to the DE bit in DMACHCR while receive data is being collected from the On-chip peripheral module.

The number of packets that remains in the buffer can be confirmed by reading RP bits in DMACHCLR.

Figure 8.10 shows the example of timing when the gathering buffer function is used.

Table 8.12 shows the correspondence table of the gathering buffer function.

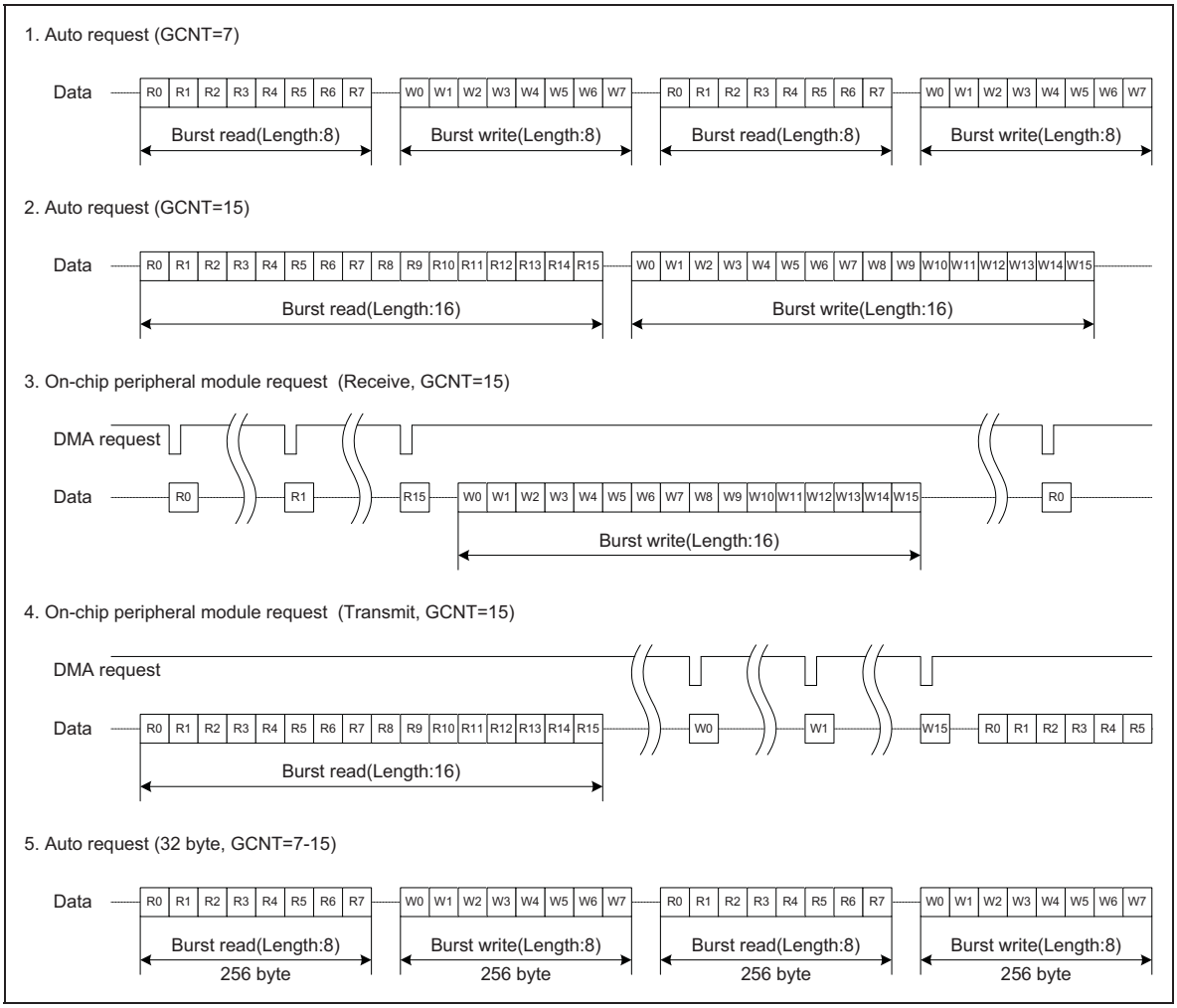


Figure 8.10 Example of Timing when the Gathering Buffer Function is Used

Table 8.12 The Correspondence Table of the Gathering Buffer Function.

Module	Function	Source	Destination
Memory-to-memory	—	Yes	Yes
External device	Transmit and receive	No	No
BBIF1/2	Transmit	Yes	No
	Receive	No	Yes
CMT1	Transmit and receive	No	No
FLCTL	Transmit and receive	No	No
IIC 0/1/2/3/4	Transmit	Yes	No
	Receive	No	Yes
MSIOF0/1/2	Transmit	Yes	No
	Receive	No	Yes
SCIF0/1/2/3/4/5,SCIFB	Transmit	Yes	No
	Receive	No	Yes
SDHI0/1/2	Transmit	Yes	No
	Receive	No	Yes
FSI	Transmit	Yes	No
	Receive	No	Yes
TPU0	Transmit	Yes	No
TSIF0/1	Receive	No	Yes
IRDA	Receive	No	Yes
DSI0/1	Receive	No	Yes
HSI	Transmit	Yes	No
	Receive	No	Yes
MMC	Transmit	Yes	No
	Receive	No	Yes
MFI	Transmit and receive	No	No
SHWYSTAT	Receive	No	Yes

notes : As for the transfer to on-chip peripheral module side, the gathering buffer function is compulsorily invalidated.

8.5 Usage Notes

Pay attentions to the following notes when the DMAC is used.

(1) DMA Transfer for Peripheral Modules

When executing a DMA transfer for peripheral modules, an appropriate boundary address should be set for the transfer source or destination address according to the transfer data size. Otherwise, an address error may occur.

(2) Module Stop

While the DMAC is in operation, the DMAC should not be stopped by the module stop register (MSTPCR0) setting. When the DMAC is stopped, transfer contents cannot be guaranteed.

(3) Address Error

Clear the buffer by writing 0 to the CLR bit in DMA channel clear register (DMACHCLR) when the DMA address error occurs. When a DMA address error is generated, set the register of the error-ridden channel again and then start a transfer.

(4) DMA Transfer Stop

Wait for the RP bits in CHCLR to become 0 after writing 0 to the DE bit in CHCR about the stop of the DMA transfer.

(5) DMA Transfer Interruption

When make the DMA transfer interrupted, the interruption disable should be set and set the DE bit in DMA channel control register (DMACHCR) as the DMA transfer disable. If the TE is generated during the DMA transfer interruption, the TE should be initialized. The generation timing after the transfer interruption for an asynchronous assumed following three cases.

1. A case that after setting for the interruption disable, TE is changed to 1 before the CHCR initialization. The TE is initialized by the processing DMA transfer initialization.
2. A case that after setting for the interruption disable, the TE is changed to 1 by ignoring the transfer interruption. After the DMA transfer initialization and the CHCR dummy read, check the TE bit. If the TE bit is 1, the DMA transfer initialization process should be performed.
3. A case that after setting for the interruption disable, the TE is not changed to 0 even though the transfer interruption is occurred.
   After the DMA transfer interruption, the TE is not generated because the transfer data is still remained.

Note: In a case that the DMA transfer initialization is performed while the last transfer is executing, causes TE generation delay. So the dummy read should be performed.

Figure 8.11 shows the processing example when DMA transfer interruption (Data is guaranteed).

Figure 8.12 shows the processing example when DMA transfer interruption (Compulsion interruption).

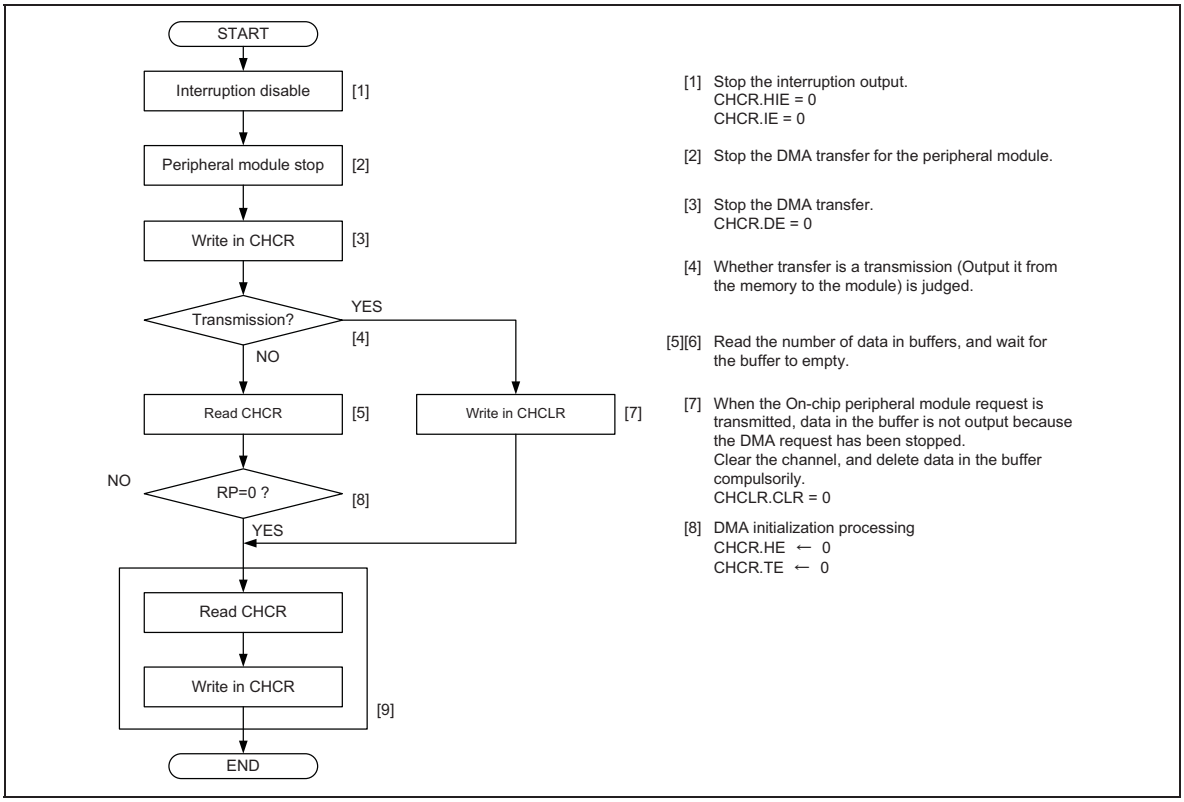


Figure 8.11 Example of DMAC Transfer Interruption Processing (Data is Guaranteed)

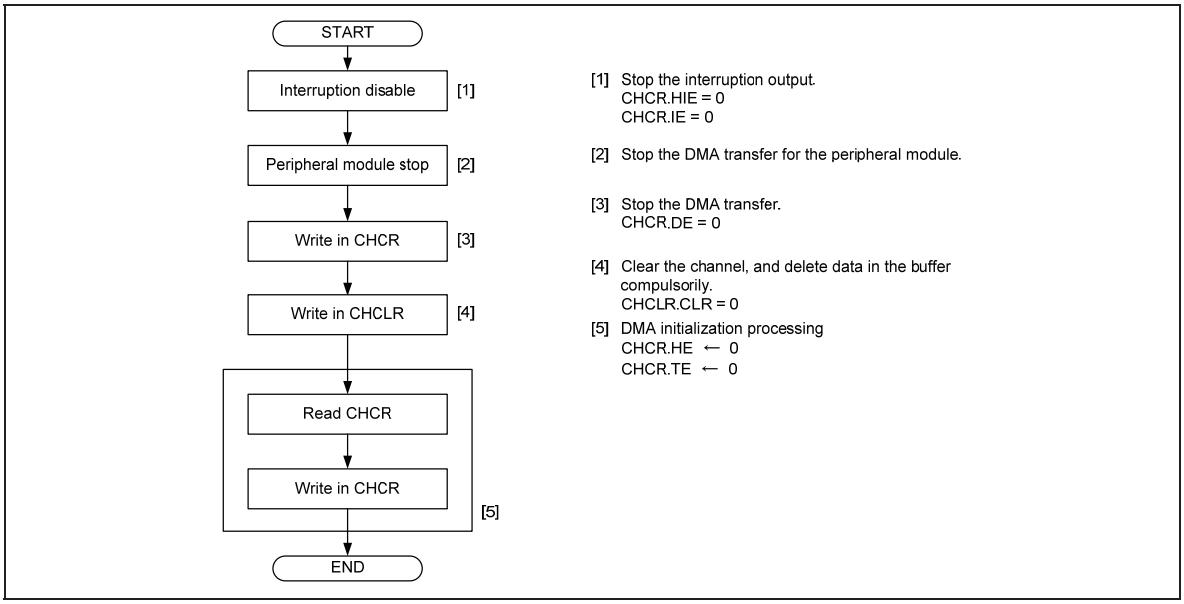


Figure 8.12 Example of DMAC Transfer Interruption Processing (Compulsion Interruption)

Section 9 Realtime Direct Memory Access Controller (RTDMAC)

This LSI includes three sets of direct memory access controllers (RTDMAC1 and RTDMAC2 which are collectively called the RTDMAC).

The RTDMAC can be used in place of the CPU to perform high-speed transfers between external memory, on-chip memory, memory-mapped external devices, and on-chip peripheral modules.

9.1 Features

- Six channels
- 4-Gbyte physical address space
- Data transfer unit is selectable: Byte, word (2 bytes), longword (4 bytes), 8 bytes, 16 bytes, 32 bytes, and 64 bytes
- Maximum transfer count: 16,777,216 transfers
- Address mode: Dual address mode
- Transfer requests:

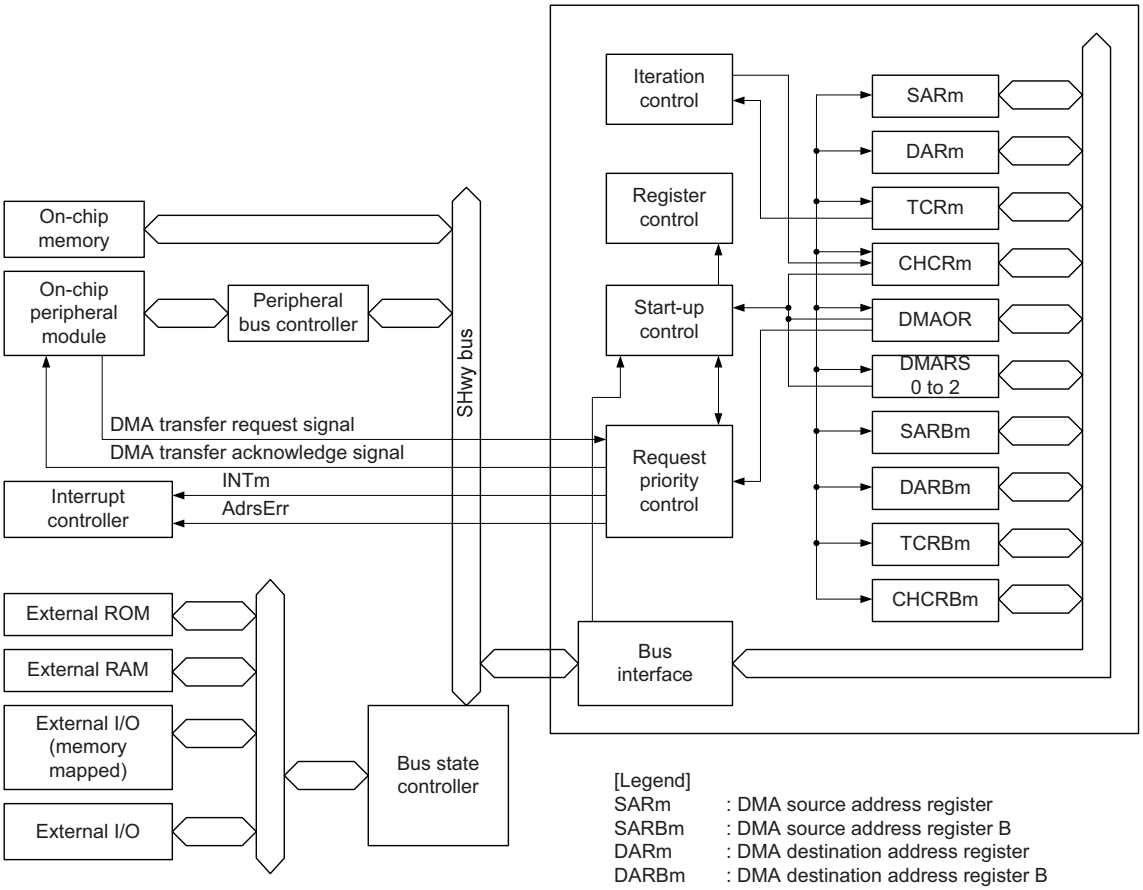
  On-chip peripheral module request, or auto request can be selected.

  The following modules can issue an on-chip peripheral module request.

  — CMT1, SCIFA0/1/2/3/4/5, SCIFB, MSIOF0/1/2, BBIF1/2, IIC0/1/2/3/4, FLCTL0/1, FSI, SDHI0/1/2, TPU0, TSIF0/1, IRDA, DSI0/1, HSI, MFI, MMC, SHWYSTAT
- Bus mode: Cycle steal mode (normal mode and intermittent mode)
- Selectable channel priority levels:

  The channel priority levels are selectable between fixed mode and round-robin mode.
- Interrupt request: An interrupt request can be generated to the CPU after half of the transfers ended, all transfers ended, or an address error occurred.
- Gathering buffer function: Transfer data of 256 bytes or less can be collectively transmitted.

Figure 9.1 shows the block diagram of the RTDMAC.



[Legend]
SARm : DMA source address register
SARBm : DMA source address register B
DARm : DMA destination address register
DARBm : DMA destination address register B
TCRm : DMA transfer count register
TCRBm : DMA transfer count register B
CHCRm : DMA channel control register
CHCRBm : DMA channel control register B
DMAOR : DMA operation register
DMARS0 to DMARS2 : DMA extended resource selectors 0 to 2
INTm : DMA transfer end/half-end interrupt request
AdrsErr : Address error interrupt request
m : 0,1,2,3,4,5

Figure 9.1 Block Diagram of RTDMAC

9.2 Input/Output Pins

There are no external pins relevant to the RTDMAC.

9.3 Register Descriptions

Table 9.1, and Table 9.3 show the configuration of registers of the RTDMAC, and RTDMAC2 respectively. Table 9.2, and Table 9.4 show the state of the registers in each processing mode.

The DMASAR for channel 0 in the RTDMAC is expressed as RDM1SAR_0 and the DMAOR for channel 2 in the RTDMAC2 is expressed as RDM2OR.

Table 9.1 Register Configuration of RTDMAC

Name	Abbreviation	R/W	Address	Access Size
RTDMAC source address register_0	RDM1SAR_0	R/W	H'FFC1 8020	32
RTDMAC destination address register_0	RDM1DAR_0	R/W	H'FFC1 8024	32
RTDMAC transfer count register_0	RDM1TCR_0	R/W	H'FFC1 8028	32
RTDMAC channel control register_0	RDM1CHCR_0	R/W	H'FFC1 802C	32
RTDMAC source address register_1	RDM1SAR_1	R/W	H'FFC1 8030	32
RTDMAC destination address register_1	RDM1DAR_1	R/W	H'FFC1 8034	32
RTDMAC transfer count register_1	RDM1TCR_1	R/W	H'FFC1 8038	32
RTDMAC channel control register_1	RDM1CHCR_1	R/W	H'FFC1 803C	32
RTDMAC source address register_2	RDM1SAR_2	R/W	H'FFC1 8040	32
RTDMAC destination address register_2	RDM1DAR_2	R/W	H'FFC1 8044	32
RTDMAC transfer count register_2	RDM1TCR_2	R/W	H'FFC1 8048	32
RTDMAC channel control register_2	RDM1CHCR_2	R/W	H'FFC1 804C	32
RTDMAC source address register_3	RDM1SAR_3	R/W	H'FFC1 8050	32
RTDMAC destination address register_3	RDM1DAR_3	R/W	H'FFC1 8054	32
RTDMAC transfer count register_3	RDM1TCR_3	R/W	H'FFC1 8058	32
RTDMAC channel control register_3	RDM1CHCR_3	R/W	H'FFC1 805C	32
RTDMAC operation register	RDM1OR	R/W	H'FFC1 8060	16
RTDMAC source address register_4	RDM1SAR_4	R/W	H'FFC1 8070	32
RTDMAC destination address register_4	RDM1DAR_4	R/W	H'FFC1 8074	32
RTDMAC transfer count register_4	RDM1TCR_4	R/W	H'FFC1 8078	32
RTDMAC channel control register_4	RDM1CHCR_4	R/W	H'FFC1 807C	32
RTDMAC source address register_5	RDM1SAR_5	R/W	H'FFC1 8080	32
RTDMAC destination address register_5	RDM1DAR_5	R/W	H'FFC1 8084	32
RTDMAC transfer count register_5	RDM1TCR_5	R/W	H'FFC1 8088	32
RTDMAC channel control register_5	RDM1CHCR_5	R/W	H'FFC1 808C	32
RTDMAC source address register B_0	RDM1SARB_0	R/W	H'FFC1 8120	32
RTDMAC destination address register B_0	RDM1DARB_0	R/W	H'FFC1 8124	32
RTDMAC transfer count register B_0	RDM1TCRB_0	R/W	H'FFC1 8128	32
RTDMAC channel control register B_0	RDM1CHCRB_0	R/W	H'FFC1 812C	32
RTDMAC source address register B_1	RDM1SARB_1	R/W	H'FFC1 8130	32
RTDMAC destination address register B_1	RDM1DARB_1	R/W	H'FFC1 8134	32
RTDMAC transfer count register B_1	RDM1TCRB_1	R/W	H'FFC1 8138	32
RTDMAC channel control register B_1	RDM1CHCRB_1	R/W	H'FFC1 813C	32
RTDMAC source address register B_2	RDM1SARB_2	R/W	H'FFC1 8140	32

Name	Abbreviation	R/W	Address	Access Size
RTDMAC destination address register B_2	RDM1DARB_2	R/W	H'FFC1 8144	32
RTDMAC transfer count register B_2	RDM1TCRB_2	R/W	H'FFC1 8148	32
RTDMAC channel control register B_2	RDM1CHCRB_2	R/W	H'FFC1 814C	32
RTDMAC source address register B_3	RDM1SARB_3	R/W	H'FFC1 8150	32
RTDMAC destination address register B_3	RDM1DARB_3	R/W	H'FFC1 8154	32
RTDMAC transfer count register B_3	RDM1TCRB_3	R/W	H'FFC1 8158	32
RTDMAC channel control register B_3	RDM1CHCRB_3	R/W	H'FFC1 815C	32
RTDMAC source address register B_4	RDM1SARB_4	R/W	H'FFC1 8170	32
RTDMAC destination address register B_4	RDM1DARB_4	R/W	H'FFC1 8174	32
RTDMAC transfer count register B_4	RDM1TCRB_4	R/W	H'FFC1 8178	32
RTDMAC channel control register B_4	RDM1CHCRB_4	R/W	H'FFC1 817C	32
RTDMAC source address register B_5	RDM1SARB_5	R/W	H'FFC1 8180	32
RTDMAC destination address register B_5	RDM1DARB_5	R/W	H'FFC1 8184	32
RTDMAC transfer count register B_5	RDM1TCRB_5	R/W	H'FFC1 8188	32
RTDMAC channel control register B_5	RDM1CHCRB_5	R/W	H'FFC1 818C	32
RTDMAC channel clear register_0	RDM1CHCLR_0	R/W	H'FFC1 8220	32
RTDMAC channel clear register_1	RDM1CHCLR_1	R/W	H'FFC1 8230	32
RTDMAC channel clear register_2	RDM1CHCLR_2	R/W	H'FFC1 8240	32
RTDMAC channel clear register_3	RDM1CHCLR_3	R/W	H'FFC1 8250	32
RTDMAC channel clear register_4	RDM1CHCLR_4	R/W	H'FFC1 8270	32
RTDMAC channel clear register_5	RDM1CHCLR_5	R/W	H'FFC1 8280	32
RTDMAC extended resource selector_0	RDM1RS_0	R/W	H'FFC1 9000	16
RTDMAC extended resource selector_1	RDM1RS_1	R/W	H'FFC1 9004	16
RTDMAC extended resource selector_2	RDM1RS_2	R/W	H'FFC1 9008	16

Table 9.2 State of DMAC1 Registers in Each Operating Mode

Abbreviation	Power-on Reset	Module Standby
RDM1SAR_0 to RDM1SAR_5	Initialized	Retained
RDM1DAR_0 to RDM1DAR_5	Initialized	Retained
RDM1TCR_0 to RDM1TCR_5	Initialized	Retained
RDM1CHCR_0 to RDM1CHCR_5	Initialized	Retained
RDM1OR	Initialized	Retained
RDM1SARB_0 to RDM1SARB_5	Initialized	Retained
RDM1DARB_0 to RDM1DARB_5	Initialized	Retained
RDM1TCRB_0 to RDM1TCRB_5	Initialized	Retained
RDM1CHCRB_0 to RDM1CHCRB_5	Initialized	Retained
RDM1CHCLR_0 to RDM1CHCLR_5	Initialized	Retained
RDM1RS_0 to RDM1RS_2	Initialized	Retained

* For details, refer to section 1-D Overview of reset.

Table 9.3 Register Configuration of RTDMAC2

Name	Abbreviation	R/W	Address	Access Size
RTDMAC2 transfer count register_0	RDM2TCR_0	R/W	H'FFC2 8028	32
RTDMAC2 channel control register_0	RDM2CHCR_0	R/W	H'FFC2 802C	32
RTDMAC2 source address register_1	RDM2SAR_1	R/W	H'FFC2 8030	32
RTDMAC2 destination address register_1	RDM2DAR_1	R/W	H'FFC2 8034	32
RTDMAC2 transfer count register_1	RDM2TCR_1	R/W	H'FFC2 8038	32
RTDMAC2 channel control register_1	RDM2CHCR_1	R/W	H'FFC2 803C	32
RTDMAC2 source address register_2	RDM2SAR_2	R/W	H'FFC2 8040	32
RTDMAC2 destination address register_2	RDM2DAR_2	R/W	H'FFC2 8044	32
RTDMAC2 transfer count register_2	RDM2TCR_2	R/W	H'FFC2 8048	32
RTDMAC2 channel control register_2	RDM2CHCR_2	R/W	H'FFC2 804C	32
RTDMAC2 source address register_3	RDM2SAR_3	R/W	H'FFC2 8050	32
RTDMAC2 destination address register_3	RDM2DAR_3	R/W	H'FFC2 8054	32
RTDMAC2 transfer count register_3	RDM2TCR_3	R/W	H'FFC2 8058	32
RTDMAC2 channel control register_3	RDM2CHCR_3	R/W	H'FFC2 805C	32
RTDMAC2 operation register	RDM2OR	R/W	H'FFC2 8060	16
RTDMAC2 source address register_4	RDM2SAR_4	R/W	H'FFC2 8070	32
RTDMAC2 destination address register_4	RDM2DAR_4	R/W	H'FFC2 8074	32
RTDMAC2 transfer count register_4	RDM2TCR_4	R/W	H'FFC2 8078	32
RTDMAC2 channel control register_4	RDM2CHCR_4	R/W	H'FFC2 807C	32
RTDMAC2 source address register_5	RDM2SAR_5	R/W	H'FFC2 8080	32
RTDMAC2 destination address register_5	RDM2DAR_5	R/W	H'FFC2 8084	32
RTDMAC2 transfer count register_5	RDM2TCR_5	R/W	H'FFC2 8088	32
RTDMAC2 channel control register_5	RDM2CHCR_5	R/W	H'FFC2 808C	32
RTDMAC2 source address register B_0	RDM2SARB_0	R/W	H'FFC2 8120	32
RTDMAC2 destination address register B_0	RDM2DARB_0	R/W	H'FFC2 8124	32
RTDMAC2 transfer count register B_0	RDM2TCRB_0	R/W	H'FFC2 8128	32
RTDMAC2 channel control register B_0	RDM2CHCRB_0	R/W	H'FFC2 812C	32
RTDMAC2 source address register B_1	RDM2SARB_1	R/W	H'FFC2 8130	32
RTDMAC2 destination address register B_1	RDM2DARB_1	R/W	H'FFC2 8134	32
RTDMAC2 transfer count register B_1	RDM2TCRB_1	R/W	H'FFC2 8138	32
RTDMAC2 channel control register B_1	RDM2CHCRB_1	R/W	H'FFC2 813C	32
RTDMAC2 source address register B_2	RDM2SARB_2	R/W	H'FFC2 8140	32
RTDMAC2 destination address register B_2	RDM2DARB_2	R/W	H'FFC2 8144	32
RTDMAC2 transfer count register B_2	RDM2TCRB_2	R/W	H'FFC2 8148	32
RTDMAC2 channel control register B_2	RDM2CHCRB_2	R/W	H'FFC2 814C	32
RTDMAC2 source address register B_3	RDM2SARB_3	R/W	H'FFC2 8150	32
RTDMAC2 destination address register B_3	RDM2DARB_3	R/W	H'FFC2 8154	32
RTDMAC2 transfer count register B_3	RDM2TCRB_3	R/W	H'FFC2 8158	32
RTDMAC2 channel control register B_3	RDM2CHCRB_3	R/W	H'FFC2 815C	32
RTDMAC2 source address register B_4	RDM2SARB_4	R/W	H'FFC2 8170	32
RTDMAC2 destination address register B_4	RDM2DARB_4	R/W	H'FFC2 8174	32

Name	Abbreviation	R/W	Address	Access Size
RTDMAC2 transfer count register B_4	RDM2TCRB_4	R/W	H'FFC2 8178	32
RTDMAC2 channel control register B_4	RDM2CHCRB_4	R/W	H'FFC2 817C	32
RTDMAC2 source address register B_5	RDM2SARB_5	R/W	H'FFC2 8180	32
RTDMAC2 destination address register B_5	RDM2DARB_5	R/W	H'FFC2 8184	32
RTDMAC2 transfer count register B_5	RDM2TCRB_5	R/W	H'FFC2 8188	32
RTDMAC2 channel control register B_5	RDM2CHCRB_5	R/W	H'FFC2 818C	32
RTDMAC2 channel clear register_0	RDM2CHCLR_0	R/W	H'FFC2 8220	32
RTDMAC2 channel clear register_1	RDM2CHCLR_1	R/W	H'FFC2 8230	32
RTDMAC2 channel clear register_2	RDM2CHCLR_2	R/W	H'FFC2 8240	32
RTDMAC2 channel clear register_3	RDM2CHCLR_3	R/W	H'FFC2 8250	32
RTDMAC2 channel clear register_4	RDM2CHCLR_4	R/W	H'FFC2 8270	32
RTDMAC2 channel clear register_5	RDM2CHCLR_5	R/W	H'FFC2 8280	32
RTDMAC2 extended resource selector_0	RDM2RS_0	R/W	H'FFC2 9000	16
RTDMAC2 extended resource selector_1	RDM2RS_1	R/W	H'FFC2 9004	16
RTDMAC2 extended resource selector_2	RDM2RS_2	R/W	H'FFC2 9008	16

Table 9.4 State of RTDMAC2 Registers in Each Operating Mode

Abbreviation	Reset*	Module Standby
RDM2SAR_0 to RDM2SAR_5	Initialized	Retained
RDM2DAR_0 to RDM2DAR_5	Initialized	Retained
RDM2TCR_0 to RDM2TCR_5	Initialized	Retained
RDM2CHCR_0 to RDM2CHCR_5	Initialized	Retained
RDM2OR	Initialized	Retained
RDM2SARB_0 to RDM2SARB_5	Initialized	Retained
RDM2DARB_0 to RDM2DARB_5	Initialized	Retained
RDM2TCRB_0 to RDM2TCRB_5	Initialized	Retained
RDM2CHCRB_0 to RDM2CHCRB_5	Initialized	Retained
RDM2CHCLR_0 to RDM2CHCLR_5	Initialized	Retained
RDM2RS_0 to RDM2RS_2	Initialized	Retained

* For details, refer to section 1-D Overview of reset.

9.3.1 DMA Source Address Registers 0 to 5 (DMASAR_0 to DMASAR_5)

The DMASAR registers are 32-bit readable/writable registers that specify the source address of a DMA transfer. During a DMA transfer, these registers indicate the next source address.

To transfer data in word or in longword units, specify a word or longword boundary address. When transferring data in 8-byte, 16-byte, 32-byte, or 64-byte units, an 8-byte, 16-byte, 32-byte, or 64-byte boundary must be set for the source address value. However, if the address mode in the DMA channel control register is set as fixed (SM[1:0] = B'11) even when transferring data in 32-byte or 64-byte, a value can be specified in 16-byte boundary.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SAR															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SAR															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

9.3.2 DMA Source Address Registers B_0 to 5 (DMASARB_0 to DMASARB_5)

The DMASARB registers are 32-bit readable/writable registers that specify the source address of a DMA transfer that is to be set in DMASAR in repeat/reload mode. Data to be written from the CPU to DMASAR is also written to DMASARB. To set a DMASARB address that differs from the DMASAR address, write data to DMASARB after DMASAR.

To transfer data in word or in longword units, specify a word or longword boundary address. When transferring data in 8-byte, 16-byte, 32-byte, or 64-byte units, an 8-byte, 16-byte, 32-byte, or 64-byte boundary must be set for the source address value. However, if the address mode in the DMA channel control register is set as fixed (SM[1:0] = B'11) even when transferring data in 32-byte or 64-byte, a value can be specified in 16-byte boundary.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SARB															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SARB															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

9.3.3 DMA Destination Address Registers 0 to 5 (DMADAR_0 to DMADAR_5)

The DMADAR registers are 32-bit readable/writable registers that specify the destination address of a DMA transfer. During a DMA transfer, these registers indicate the next destination address.

To transfer data in word or in longword units, specify a word or longword boundary address. When transferring data in 8-byte, 16-byte, 32-byte, or 64-byte units, an 8-byte, 16-byte, 32-byte, or 64-byte boundary must be set for the destination address value. However, if the address mode in the DMA channel control register is set as fixed (SM[1:0] = B'11) even when transferring data in 32-byte or 64-byte, a value can be specified in 16-byte boundary.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DAR															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DAR															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

9.3.4 DMA Destination Address Registers B_0 to 5 (DMADARB_0 to DMADARB_5)

The DMADARB registers are 32-bit readable/writable registers that specify the destination address of a DMA transfer that is to be set in DMADAR in repeat/reload mode. Data to be written from the CPU to DMADAR is also written to DMADARB. To set a DMADARB address that differs from the DMADAR address, write data to DMADARB after DMADAR.

To transfer data in word or in longword units, specify a word or longword boundary address. When transferring data in 8-byte, 16-byte, 32-byte, or 64-byte units, an 8-byte, 16-byte, 32-byte, or 64-byte boundary must be set for the destination address value. However, if the address mode in the DMA channel control register is set as fixed (SM[1:0] = B'11) even when transferring data in 32-byte or 64-byte, a value can be specified in 16-byte boundary.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DARB															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DARB															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

9.3.5 DMA Transfer Count Registers 0 to 5 (DMATCR_0 to DMATCR_5)

The DMATCR registers are 32-bit readable/writable registers that specify the DMA transfer count. The number of transfers is 1 when the setting is H'00000001, 16,777,215 when H'00FFFFFF is set, and 16,777,216 (the maximum) when H'00000000 is set. During a DMA transfer, these registers indicate the remaining transfer count.

The upper eight bits of DMATCR are always read as 0, and the write value should always be 0.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TCR															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TCR															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

9.3.6 DMA Transfer Count Registers B_0 to 5 (DMATCRB_0 to DMATCRB_5)

The DMATCRB registers are 32-bit readable/writable registers. Data to be written from the CPU to DMATCR is also written to DMATCRB. To set a DMATCRB address that differs from the DMATCR address, write data to DMATCRB after DMATCR. While the HE function is used, DMATCRB is used to hold the initial value for detecting HE. DMATCRB specifies the number of DMA transfers which are set in DMATCR in repeat mode. DMATCRB specifies the number of DMA transfers and are used as a transfer counter in reload mode.

In reload mode, the lower 16 bits operate as a transfer counter; the values of DMASAR and DMADAR are updated after the value of the lower 16 bits became 0, and the value of the upper 16 bits of DMATCRB is loaded to the lower 16 bits. In the upper 16 bits, set the number of transfers that should be executed before the transfer count is reloaded. In reload mode, the same number of transfers should be set in both upper and lower 16 bits. In addition, set the HIE bit in DMACHCR to 0 and do not use the HE function.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TCRB															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TCRB															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

9.3.7 DMA Channel Control Registers 0 to 5 (DMACHCR_0 to DMACHCR_5)

The DMACHCR registers are 32-bit readable/writable registers that control the DMA transfer mode.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CAE	CAIE	HEE[1:0]		RPT[2:0]			-	-	-	TS[3:2]		HE	HIE	-	–
Initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/(W)*	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/(W)*	R/W	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DM[1:0]		SM[1:0]		RS[3:0]				-	-	-	TS[1:0]		IE	TE	DE
Initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/(W)*	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31	CAE	0	R/(W)*	Address Error Flag Indicates that an address error interrupt occurred during DMA transfer. This bit is set under following conditions: • The value set in DMASAR or DMADAR does not match the transfer size boundary. • The transfer source or transfer destination is invalid space. • The transfer source or transfer destination is in module stop mode If this bit is set, DMA transfer is not enabled for the channel even if the DE bit is set to 1. To clear the CAE bit, write 0 to the CAE bit after reading 1 from the bit or clear the AE bit in DMAOR. (Clearing the AE bit clears the channel address errors for all channels.) 0: No RTDMAC address error interrupt [Clearing condition] Writing CAE = 0 after reading CAE = 1 1: RTDMAC address error interrupt occurs during DMA transfer
30	CAIE	0	R/W	Channel Address Error Interrupt Enable Specifies whether to request the CPU of an interrupt when an address error occurs. If the CAIE bit is set to 1, setting the CAE bit requests the CPU of an interrupt (DEI0 to DEI 5) for each channel. Note: An address error interrupt (DADERR) is asserted simultaneously. For interrupts, see section 5, Interrupt Controller (INTC). 0: Interrupt request disabled 1: Interrupt request enabled

Bit	Bit Name	Initial Value	R/W	Descriptions
29, 28	HEE[1:0]	00	R/W	HE Interrupt Function Extension This bit is meaningful only when the HIE bit is set to 1. 00: HE interrupt occurs when the transfer count reaches about a half of DMATCR which is set before transfer (same as before). 01: HE interrupt occurs every time the transfer count reaches about n/4 (n=1, 2, or 3) of DMATCR which is set before transfer. 10: HE interrupt occurs every time the transfer count reaches about n/8 (n=1 to 7) of DMATCR which is set before transfer. 11: HE interrupt occurs every time the transfer count reaches about n/16 (n=1 to 15) of DMATCR which is set before transfer.
27 to 25	RPT[2:0]	000	R/W	DMA Setting Renewal Specify 000: Normal mode (RTDMAC operation) 001: Repeat mode DMASAR/DMADAR used as repeat area 010: Repeat mode DMADAR used as repeat area 011: Repeat mode DMASAR used as repeat area 100: Setting prohibited 101: Reload mode DMASAR/DMADAR used as reload area 110: Reload mode DMADAR used as reload area 111: Reload mode DMASAR used as reload area
24 to 22	—	000	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
21, 20	TS[3:2]	00	R/W	DMA Transfer Size Specify With TS[1:0], these bits specify the DMA transfer size. When the transfer source or transfer destination is a register of an on-chip peripheral module with a transfer size set, a proper transfer size for the register should be set. In 2-division transfer mode, 16/32-byte data is halved and transferred in two operations. For the transfer source or destination address specified by DMASAR or DMADAR, an appropriate boundary address should be set according to the transfer data size. TS[3:2] + TS[1:0] 0000: Byte units transfer 0001: Word (2-byte) units transfer 0010: Longword (4-byte) units transfer 0011: 16-byte units transfer 0100: 32-byte units transfer 0101: 64-byte units transfer 0111: 8-byte units transfer Other than above: Setting prohibited
19	HE	0	R/(W)*	Half End Flag After HIE (bit 18) is set to 1 and the number of transfers become half of DMATCR (1 bit shift to right) which is set before transfer starts, HE becomes 1. The HE bit is not set when transfers are ended by an address error or by clearing the DE bit and the DME bit in DMAOR before the number of transfers is decreased to half of the DMATCR value set preceding the transfer. The HE bit is kept set when the transfer ends by an address error, or clearing the DE bit (bit 0) or the DME bit in DMAOR after the HE bit is set to 1. To clear the HE bit, write 0 after reading 1 in the HE bit. 0: During the DMA transfer or DMA transfer has been interrupted DMATCR > (DMATCR set before transfer)/2 [Clearing condition] Writing 0 after reading HE = 1. 1: DMATCR ≤ (DMATCR set before transfer)/2
18	HIE	0	R/W	Half End Interrupt Enable Specifies whether an interrupt request is generated to the CPU when the number of transfers is decreased to half of the DMATCR value set preceding the transfer. When the HIE bit is set to 1 and the HE bit is set, an interrupt request is generated to the CPU. Set this bit to 0 while reload mode is set. 0: Interrupt request is disabled when DMATCR = (DMATCR set before transfer)/2 1: Interrupt request is enabled when DMATCR = (DMATCR set before transfer)/2
17, 16	—	000	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
15, 14	DM[1:0]	00	R/W	Destination Address Mode Specify whether the DMA destination address is incremented, decremented, or left fixed. 00: Fixed destination address 01: Destination address is incremented +1 in byte units transfer +2 in word units transfer +4 in longword units transfer +8 in 8-byte units transfer +16 in 16-byte units transfer +32 in 32-byte units transfer +64 in 64-byte units transfer 10: Destination address is decremented –1 in byte units transfer –2 in word units transfer –4 in longword units transfer Setting prohibited in 8/16/32-byte units transfer 11: Fixed destination address Set to prevent an address from being changed in the objective modules. Example: When specifying FIFOs in the peripheral modules.
13, 12	SM[1:0]	00	R/W	Source Address Mode Specify whether the DMA source address is incremented, decremented, or left fixed. 00: Fixed source address 01: Source address is incremented +1 in byte units transfer +2 in word units transfer +4 in longword units transfer +8 in 8-byte units transfer +16 in 16-byte units transfer +32 in 32-byte units transfer +64 in 64-byte units transfer 10: Source address is decremented –1 in byte units transfer –2 in word units transfer –4 in longword units transfer Setting prohibited in 8/16/32-byte units transfer 11: Fixed source address Set to prevent an address from being changed in the objective modules. Example: When specifying FIFOs in the peripheral modules.
11 to 8	RS[3:0]	0000	R/W	Resource Select Specify which transfer requests will be sent to the RTDMAC. The changing of transfer request source should be done in the state that the DMA enable bit (DE) is set to 0. 0100: Auto request 1000: Selected by DMA extended resource selector Other than above: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Descriptions
7 to 5	—	000	R	Reserved This bit is always read as 0. The write value should always be 0.
4, 3	TS[1:0]	00	R/W	DMA Transfer Size Specify See the description of TS[3:2] (bits 21 and 20).
2	IE	0	R/W	Interrupt Enable Specifies whether or not an interrupt request is generated to the CPU at the end of the DMA transfer. Setting this bit to 1 generates an interrupt request (DEI) to the CPU when the TE bit is set to 1. 0: Interrupt request is disabled. 1: Interrupt request is enabled.
1	TE	0	R/(W)*	Transfer End Flag The TE bit is set to 1 when data transfer ends when DMATCR becomes 0. The TE bit is not set to 1 in the following cases. • DMA transfer ends due to a DMA address error before DMATCR becomes 0. • DMA transfer is ended by clearing the DE bit and DME bit in DMAOR. To clear the TE bit, the TE bit should be written to 0 after reading 1. Even if the DE bit is set to 1 while this bit is set to 1, transfer is not enabled. 0: During the DMA transfer or DMA transfer has been interrupted [Clearing condition] Writing 0 after reading TE = 1 1: DMA transfer ends by the specified count (TCR = 0)
0	DE	0	R/W	DMA Enable Enables or disables the DMA transfer. In auto request mode, DMA transfer starts by setting the DE bit and DME bit in DMAOR to 1. At this time, both of the AE bit in DMAOR and the TE bit must be 0. In an peripheral module request, DMA transfer starts if DMA transfer request is generated by the devices or peripheral modules after setting the DE and DME bits to 1. In this case, however, both of the TE and AE bits must be 0, which is the same as in the case of auto request mode. Clearing the DE bit to 0 can terminate the DMA transfer. 0: DMA transfer disabled 1: DMA transfer enabled

Note: * Writing 0 is possible to clear the flag.

9.3.8 DMA Channel Control Register B_0 to 5 (DMACHCRB_0 to DMACHCRB_5)

The DMACHCRB registers are 32-bit readable/writable registers that control the DMA transfer mode.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	GS	GL	GCNT[3:0]				-	-	-	-	-	-	-	–
Initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	PRI[3:0]			
Initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31, 30	—	00	R	Reserved These bits are always read as 0. The write value should always be 0.
29	GS	0	R/W	Gathering Buffer Enable (Writing side) Data is transmitted collectively to the transfer destination. 0: disabled 1: enabled
28	GL	0	R/W	Gathering Buffer Enable (Reading side) Data is received collectively from the transfer source. 0: disabled 1: enabled
27 to 24	GCNT[3:0]	0000	R/W	Number of data gathering ability in gathering buffer Specify the number of data collectively transmitted with GCNT+1. The number of data transmits the transfer unit specified for the TS bits in DMACHCR. However, when the transfer size exceeds 256 bytes, the transfer size becomes 256 bytes.
31 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	PRI[3:0]	0000	R/W	Bus Request Priority Setting These bits set the priority of the bus request that is output by the RTDMAC. 1111: Highest priority : 0000: Lowest priority Note: For details of the PRI signal, see section 1-F Bus Functions.

9.3.9 DMA Operation Register (DMAOR)

DMAOR is a 16-bit readable/writable register that specifies the priority level of channels for the DMA transfer. This register also shows the DMA transfer status.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMS[3:0]				-	-	PR[1:0]		PPRI	-	-	-	-	AE	-	DME
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R	R	R	R	R/(W)*	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	CMS[3:0]	0000	R/W	Cycle Steal Mode Select Select either normal mode or intermittent mode in cycle steal mode. It is necessary that all channel's bus modes are set to cycle steal mode to make valid intermittent mode. 0000: Normal mode 0010: Intermittent mode 16 Executes one DMA transfer in each of 16 cycles of the external bus clock. 0011: Intermittent mode 64 Executes one DMA transfer in each of 64 cycles of the external bus clock. 0100: Intermittent mode 256 Executes one DMA transfer in each of 256 cycles of the external bus clock. Other than above: Setting prohibited
11, 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9, 8	PR[1:0]	00	R/W	Priority Mode Select the priority level between channels when there are transfer requests for multiple channels simultaneously. 00: CH0 > CH1 > CH2 > CH3 > CH4 > CH5 01: CH0 > CH2 > CH3 > CH1 > CH4 > CH5 10: Round-robin mode with top priority placed on CH0 11: Round-robin mode
7	PPRI	0	R/W	Bus Request Priority Push out Assigns the highest DMA bus request priority setting for channels performing DMA transfer as the value of bus request priority being currently output to the SHWY. 0: Normal mode 1: Bus request priority push out
6 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

2	AE	0	R/(W)*	Address Error Flag Indicates that an address error interrupt occurred during DMA transfer. This bit is set under following conditions: • The value set in DMASAR or DMADAR does not match the transfer size boundary. • The transfer source or transfer destination is invalid space. • The transfer source or transfer destination is in module stop mode If this bit is set, DMA transfer is not enabled for the channel even if the DE bit is set to 1. To clear the AE bit, write 0 to the AE bit after reading 1 from the bit or clear the CAE bit for each channel. (Clearing the AE bit clears the channel address errors for all channels.) 0: No RTDMAC address error interrupt [Clearing condition] Writing CAE = 0 after reading CAE = 1 1: RTDMAC address error interrupt occurs during DMA transfer
1	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
0	DME	0	R/W	DMA Master Enable Enables or disables DMA transfers on all channels. If the DME bit and the DE bit in DMACHCR are set to 1, DMA transfer is enabled. At this time, the TE bits in DMACHCR and the AE bits in DMAOR must be all 0. If this bit is cleared during transfer, transfers in all channels are terminated. 0: Disables DMA transfers on all channels 1: Enables DMA transfers on all channels

Note: * Writing 0 is possible to clear the flag.

9.3.10 DMA Channel Clear Register 0 to 5 (CHCLR_0 to CHCLR_5)

The CHCLR registers are 32-bit readable/writable registers that clear the buffer of each channel.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	RP[4:0]					—	—	—	CLR
Initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	W

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8 to 4	RP[4:0]	All 0	R	Number of data in buffer of channel The number of data that remains in the buffer of the channel is read. Units of the number of data are the DMA transfer size.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	CLR	0	W	Channel Clear Bit When writing 0 to the bit, the buffer of channel to be cleared. Writing is prohibited during DMA operating.

9.3.11 DMA Extended Resource Selectors 0 to 2 (DMARS_0 to DMARS_2)

The DMARS registers are 16-bit readable/writable registers that specify the peripheral module as the source of the DMA transfer request for each channel. DMARS_0 specifies for channels 0 and 1, DMARS_1 specifies for channels 2 and 3, and DMARS_2 specifies for channels 4 and 5.

When MID/RID is set to a value other than the values listed in Table 9.5, the operation of this LSI is not guaranteed. The transfer request from DMARS is valid only when the resource select bits (RS[3:0]) have been set to B'1000 for DMACHCR_0 to DMACHCR_5. Otherwise, even if DMARS has been set, transfer request source is not accepted.

DMARS_0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	C1MID[5:0]						C1RID[1:0]		C0MID[5:0]						C0RID[1:0]	
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	C1MID[5:0]	000000	R/W	Transfer request module ID5 to ID0 for DMA channel 1 (MID) See Table 9.5.
9, 8	C1RID[1:0]	00	R/W	Transfer request register ID1 and ID0 for DMA channel 1 (RID) See Table 9.5.
7 to 2	C0MID[5:0]	000000	R/W	Transfer request module ID5 to ID0 for DMA channel 0 (MID) See Table 9.5.
1, 0	C0RID[1:0]	00	R/W	Transfer request register ID1 and ID0 for DMA channel 0 (RID) See Table 9.5.

DMARS_1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	C3MID[5:0]						C3RID[1:0]		C2MID[5:0]						C2RID[1:0]	
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	C3MID[5:0]	000000	R/W	Transfer request module ID5 to ID0 for DMA channel 3 (MID) See Table 9.5.
9, 8	C3RID[1:0]	00	R/W	Transfer request register ID1 and ID0 for DMA channel 3 (RID) See Table 9.5.
7 to 2	C2MID[5:0]	000000	R/W	Transfer request module ID5 to ID0 for DMA channel 2 (MID) See Table 9.5.
1, 0	C2RID[1:0]	00	R/W	Transfer request register ID1 and ID0 for DMA channel 2 (RID) See Table 9.5.

DMARS_2

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	C5MID[5:0]						C5RID[1:0]		C4MID[5:0]						C4RID[1:0]	
Initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	C5MID[5:0]	000000	R/W	Transfer request module ID5 to ID0 for DMA channel 5 (MID) See Table 9.5.
9, 8	C5RID[1:0]	00	R/W	Transfer request register ID1 and ID0 for DMA channel 5 (RID) See Table 9.5.
7 to 2	C4MID[5:0]	000000	R/W	Transfer request module ID5 to ID0 for DMA channel 4 (MID) See Table 9.5.
1, 0	C4RID[1:0]	00	R/W	Transfer request register ID1 and ID0 for DMA channel 4 (RID) See Table 9.5.

Table 9.5 Transfer Request Sources

Peripheral Module	Setting Value for One Channel (MID + RID)	MID	RID	Function
BBIF1	H'5A	B'010110	B'10	Receive
BBIF1	H'59	B'010110	B'01	Transmit
BBIF2	H'5E	B'010111	B'10	Receive
BBIF2	H'5D	B'010111	B'01	Transmit
CMT1	H'07	B'000001	B'11	Transmit and receive
FLCTL0	H'83	B'100000	B'11	Transmit and receive the data part
FLCTL1	H'87	B'100001	B'11	Transmit and receive the control code part
IIC0	H'62	B'011000	B'10	Receive
IIC0	H'61	B'011000	B'01	Transmit
IIC1	H'66	B'011001	B'10	Receive
IIC1	H'65	B'011001	B'01	Transmit
IIC2	H'6A	B'011010	B'10	Receive
IIC2	H'69	B'011010	B'01	Transmit
IIC3	H'6E	B'011011	B'10	Receive
IIC3	H'6D	B'011011	B'01	Transmit
IIC4	H'72	B'011100	B'10	Receive
IIC4	H'71	B'011100	B'01	Transmit
MSIOF0	H'52	B'010100	B'10	Receive
MSIOF0	H'51	B'010100	B'01	Transmit
MSIOF1	H'56	B'010101	B'10	Receive
MSIOF1	H'55	B'010101	B'01	Transmit
MSIOF2	H'42	B'010000	B'10	Receive
MSIOF2	H'41	B'010000	B'01	Transmit
SCIFA0	H'22	B'001000	B'10	Receive
SCIFA0	H'21	B'001000	B'01	Transmit
SCIFA1	H'26	B'001001	B'10	Receive
SCIFA1	H'25	B'001001	B'01	Transmit
SCIFA2	H'2A	B'001010	B'10	Receive
SCIFA2	H'29	B'001010	B'01	Transmit
SCIFA3	H'2E	B'001011	B'10	Receive
SCIFA3	H'2D	B'001011	B'01	Transmit
SCIFA4	H'3A	B'001110	B'10	Receive
SCIFA4	H'39	B'001110	B'01	Transmit
SCIFA5	H'36	B’001101	B'10	Receive
SCIFA5	H'35	B’001101	B'01	Transmit
SCIFB	H'3E	B'001111	B'10	Receive
SCIFB	H'3D	B'001111	B'01	Transmit
SDHI0	H'C2	B'110000	B'10	Receive

Peripheral Module	Setting Value for One Channel (MID + RID)	MID	RID	Function
SDHI0	H'C1	B'110000	B'01	Transmit
SDHI0	H'C6	B'110001	B'10	Receive
SDHI0	H'C5	B'110001	B'01	Transmit
SDHI1	H'CA	B'110010	B'10	Receive
SDHI1	H'C9	B'110010	B'01	Transmit
SDHI2	H'CE	B'110011	B'10	Receive
SDHI2	H'CD	B'110011	B'01	Transmit
FSIA	H’B2	B’101100	B’10	Receive
FSIA	H’B1	B’101100	B’01	Transmit
FSIB	H’B5	B’101101	B’01	Transmit
TPU0	H'F1	B'111100	B'01	Transmit
TSIF0	H'EA	B'111010	B'10	Receive
TSIF1	H'EE	B'111011	B'10	Receive
IRDA	H'32	B'001100	B'10	Receive
DSI0	H’92	B’100100	B’10	Receive
DSI1	H’96	B’100101	B’10	Receive
HSI0	H’0A	B’000010	B’10	Receive
HSI0	H’09	B’000010	B’01	Transmit
HSI1	H’0E	B’000011	B’10	Receive
HSI1	H’0D	B’000011	B’01	Transmit
HSI2	H’12	B’000100	B’10	Receive
HSI2	H’11	B’000100	B’01	Transmit
HSI3	H’16	B’000101	B’10	Receive
HSI3	H’15	B’000101	B’01	Transmit
MMC	H’D2	B’110100	B’10	Receive
MMC	H’D1	B’110100	B’01	Transmit
MFI	H’E7	B’111001	B’11	Receive
MFI	H’E3	B’111000	B’11	Transmit
SHWYSTATR	H’A6	B’101001	B’10	Receive
SHWYSTATH	H’9E	B’100111	B’10	Receive
SHWYSTATC	H’AA	B’101010	B’10	Receive

9.4 Operation

When there is a DMA transfer request, the RTDMAC starts the transfer according to the predetermined channel priority; when the transfer end conditions are satisfied, it ends the transfer. Transfers can be requested in two modes: auto request, and on-chip peripheral module request. As bus mode, cycle steal mode (normal mode and intermittent mode) is used.

9.4.1 DMA Transfer Requests

DMA transfer requests are basically generated in either the data transfer source or destination, but they can also be generated by on-chip peripheral modules that are neither the source nor the destination. Transfers can be requested in two modes: auto request, and on-chip peripheral module request. The request mode is selected for each channel in the RS[3:0] bits in DMACHCR, DMARS0 to DMARS2.

(1) Auto-Request Mode

When there is no transfer request signal from an external source, as in a memory-to-memory transfer or a transfer between memory and an on-chip peripheral module unable to request a transfer, auto-request mode allows the RTDMAC to automatically generate a transfer request signal internally. When the DE bit in DMACHCR and the DME bit in DMAOR are set to 1 for the target channel, the transfer begins so long as the CAE bit in DMACHCRR is 0.

(2) On-Chip Peripheral Module Request Mode

In this mode, a transfer is performed at the transfer request signal of an on-chip peripheral module. The source (peripheral module) of the DMA transfer request is specified by the DMARS_0/1/2 register.

When this mode is selected, if the DMA transfer is enabled (DE = 1, DME = 1, TE = 0, CAE = 0), a transfer is performed upon the input of a transfer request signal.

When a transmit data empty transfer request of the SCIF is set as the transfer request, the transfer destination must be the SCIF's transmit data register. Likewise, when receive data full transfer request of the SCIF is set as the transfer request, the transfer source must be the SCIF's receive data register. These conditions also apply to the other on-chip peripheral modules.

The number of the receive FIFO triggers can be set as a transfer request depending on an on-chip peripheral module. Data needs to be read after the DMA transfer is ended, because data may be left in the receive FIFO when the receive FIFO trigger condition is not satisfied.

Table 9.6 Selecting On-Chip Peripheral Module Request Modes with Bits RS3 to RS0 (T.B.D.)

CHCR	DMARS		DMA Transfer Request Source	DMA Transfer Request Signal	Source	Destination	Bus Mode
RS[3:0]	MID	RID					
1000	000001	11	CMT1	Transmit and receive request	Any	Any	Cycle steal
	001000	01	SCIFA0 transmitter	TXI (Transmit FIFO data empty)	Any	SCAFTDR0	Cycle steal
		10	SCIFA0 receiver	RXI (Receive FIFO data full)	SCAFRDR0	Any	Cycle steal
	001001	01	SCIFA1 transmitter	TXI (Transmit FIFO data empty)	Any	SCAFTDR1	Cycle steal
		10	SCIFA1 receiver	RXI (Receive FIFO data full)	SCAFRDR11	Any	Cycle steal
	001010	01	SCIFA2 transmitter	TXI (Transmit FIFO data empty)	Any	SCAFTDR2	Cycle steal
		10	SCIFA2 receiver	RXI (Receive FIFO data full)	SCAFRDR2	Any	Cycle steal
	001011	01	SCIFA3 transmitter	TXI (Transmit FIFO data empty)	Any	SCAFTDR3	Cycle steal
		10	SCIFA3 receiver	RXI (Receive FIFO data full)	SCAFRDR3	Any	Cycle steal
	001110	01	SCIFA4 transmitter	TXI (Transmit FIFO data empty)	Any	SCAFTDR4	Cycle steal
		10	SCIFA4 receiver	RXI (Receive FIFO data full)	SCAFRDR4	Any	Cycle steal
	001101	01	SCIFA5 transmitter	TXI (Transmit FIFO data empty)	Any	SCAFTDR5	Cycle steal
		10	SCIFA5 receiver	RXI (Receive FIFO data full)	SCAFRDR5	Any	Cycle steal
	001110	01	SCIFB transmitter	TXI (Transmit FIFO data empty)	Any	SCBFTDR	Cycle steal
		10	SCIFB receiver	RXI (Receive FIFO data full)	SCBFRDR	Any	Cycle steal
	010100	01	MSIOF0 transmitter	TXI (Transmit data request)	Any	SITDR	Cycle steal
		10	MSIOF0 receiver	RXI (Receive data request)	SIRDR	Any	Cycle steal
	010101	01	MSIOF1 transmitter	TXI (Transmit data request)	Any	SITDR	Cycle steal
		10	MSIOF1 receiver	RXI (Receive data request)	SIRDR	Any	Cycle steal
	010000	01	MSIOF2 transmitter	TXI (Transmit data request)	Any	SITDR	Cycle steal
		10	MSIOF2 receiver	RXI (Receive data request)	SIRDR	Any	Cycle steal
	010110	01	BBIF1 transmitter	TXI (Transmit data request)	Any	SITFDR	Cycle steal
		10	BBIF1 receiver	RXI (Receive data request)	SIRFDR	Any	Cycle steal

CHCR	DMARS		DMA Transfer Request Source	DMA Transfer Request Signal	Source	Destination	Bus Mode
RS[3:0]	MID	RID					
	010111	01	BBIF2 transmitter	TXI (Transmit data request)	Any	SITFDR	Cycle steal
		10	BBIF2 receiver	RXI (Receive data request)	SIRFDR	Any	Cycle steal
	011000	01	IIC0	Transmit empty transfer request	Any	Data register	Cycle steal
		10		Receive full transfer request	Data register	Any	Cycle steal
	011001	01	IIC1	Transmit empty transfer request	Any	Data register	Cycle steal
		10		Receive full transfer request	Data register	Any	Cycle steal
	011010	01	IIC2	Transmit empty transfer request	Any	Data register	Cycle steal
		10		Receive full transfer request	Data register	Any	Cycle steal
	011011	01	IIC3	Transmit empty transfer request	Any	Data register	Cycle steal
		10		Receive full transfer request	Data register	Any	Cycle steal
	011100	01	IIC4	Transmit empty transfer request	Any	Data register	Cycle steal
		10		Receive full transfer request	Data register	Any	Cycle steal
	100000	11	FLCTL data part transmit	Transmit FIFO data empty request	Any	FLDTFIFO	Cycle steal
			FLCTL data part receive	Receive FIFO data full request	FLDTFIFO	Any	Cycle steal
	100001	11	FLCTL control code part transmit	Transmit FIFO data empty request	Any	FLECFIFO	Cycle steal
			FLCTL control code part receive	Receive FIFO data full request	FLECFIFO	Any	Cycle steal
	101100	01	FSIA	Transmit empty transfer request (port A)	Any	A_DODT	Cycle steal
		10		Receive full transfer request (port A)	A_DIDT	Any	Cycle steal
	101101	01	FSIB	Transmit empty transfer request (port B)	Any	B_DODT	Cycle steal
	110000	01	SDHI0 channel 0	Transmit empty transfer request	Any	Data register	Cycle steal
		10	SDHI0 channel 1	Receive full transfer request	Data register	Any	Cycle steal
	110001	01	SDHI0 channel 2	Transmit empty transfer request	Any	Data register	Cycle steal
		10	SDHI0 channel 3	Receive full transfer request	Data register	Any	Cycle steal
	110010	01	SDHI1 channel 0	Transmit empty transfer request	Any	Data register	Cycle steal

CHCR	DMARS		DMA Transfer Request	DMA Transfer			
RS[3:0]	MID	RID	Source	Request Signal	Source	Destination	Bus Mode
		10	SDHI1 channel 1	Receive full transfer request	Data register	Any	Cycle steal
	110011	01	SDHI2 channel 0	Transmit empty transfer request	Any	Data register	Cycle steal
		10	SDHI2 channel 1	Receive full transfer request	Data register	Any	Cycle steal
	111100	01	TPU0	Transmit empty transfer request	Any	Data register	Cycle steal
	111010	10	TSIF0	Receive full transfer request	TSTSDR	Any	Cycle steal
	111011	10	TSIF1	Receive full transfer request	TSTSDR	Any	Cycle steal
	001100	10	IRDA	Receive transfer request	IrDA buffer RAM	Any	Cycle steal
	100100	10	DSI0	RXI (Receive data request)	Data register	Any	Cycle steal
	100101	10	DSI1	RXI (Receive data request)	Data register	Any	Cycle steal
	000010	01	HSI0	TXI (Transmit data request)	Any	Data register	Cycle steal
	000010	10		RXI (Receive data request)	Data register	Any	Cycle steal
	000011	01	HSI1	TXI (Transmit data request)	Any	Data register	Cycle steal
	000011	10		RXI (Receive data request)	Data register	Any	Cycle steal
	000100	01	HSI2	TXI (Transmit data request)	Any	Data register	Cycle steal
	000100	10		RXI (Receive data request)	Data register	Any	Cycle steal
	000101	01	HSI3	TXI (Transmit data request)	Any	Data register	Cycle steal
	000101	10		RXI (Receive data request)	Data register	Any	Cycle steal
	110100	01	MMC	TXI (Transmit data request)	Any	Data register	Cycle steal
	110100	10		RXI (Receive data request)	Data register	Any	Cycle steal
	111000	11	MFI	TXI (Transmit data request)	Any	Data register	Cycle steal
	111001	11		RXI (Receive data request)	Data register	Any	Cycle steal
	101001	10	SHWYSTATR	RXI (Receive data request)	Data register	Any	Cycle steal
	100111	10	SHWYSTATH	RXI (Receive data request)	Data register	Any	Cycle steal
	101010	10	SHWYSTATC	RXI (Receive data request)	Data register	Any	Cycle steal

9.4.2 Channel Priority

When the RTDMAC receives simultaneous transfer requests on two or more channels, it transfers data according to a predetermined priority. Two modes (fixed mode and round-robin mode) are selected by the PR[1:0] bits in DMAOR.

(1) Fixed Mode

In this mode, the priority levels among the channels remain fixed. There are two kinds of fixed modes as follows:

- CH0 > CH1 > CH2 > CH3 > CH4 > CH5
- CH0 > CH2 > CH3 > CH1 > CH4 > CH5

These are selected by the PR[1:0] bits in DMAOR.

(2) Round-Robin Mode

In round-robin mode each time data of one transfer unit (byte, word, longword, 8-byte, 16-byte, or 32-byte unit) is transferred on one channel, the priority is rotated. The channel on which the transfer was just finished rotates to the bottom of the priority. The round-robin mode operation is shown in Figure 9.2. The priority of round-robin mode is CH0 > CH1 > CH2 > CH3 > CH4 > CH5 immediately after reset.

(3) CH0 Top Priority Round-Robin Mode

In this mode, the round-robin mode function is enabled for the channels from CH1 to CH5, with CH0 being always transferred at top priority. Once the transfer of CH0 is completed, the priority order will be the same as that applicable before the transfer.

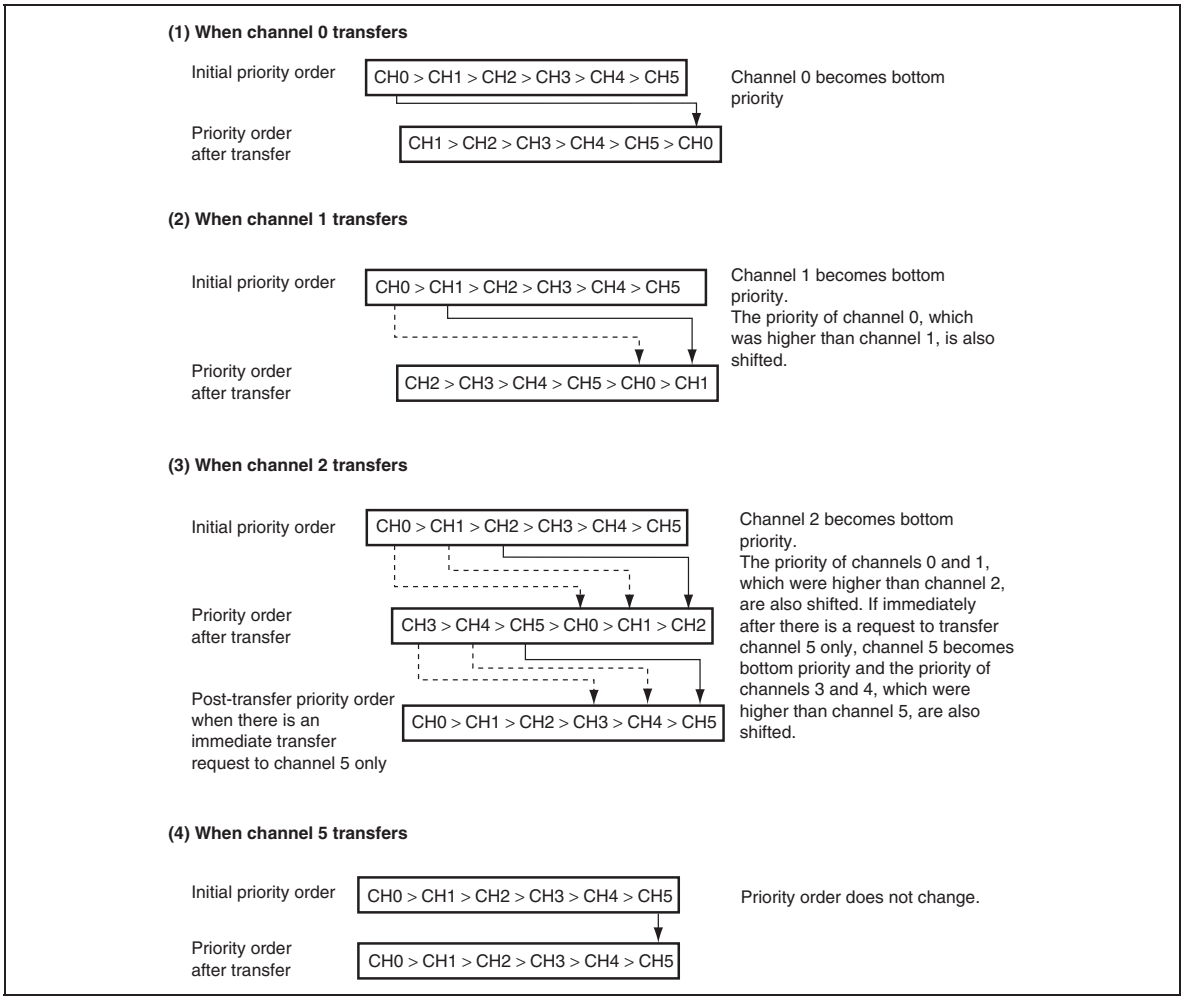


Figure 9.2 Round-Robin Mode

Figure 9.3 shows how the priority changes when channel 0 and channel 3 transfers are requested simultaneously and a channel 1 transfer is requested during the channel 0 transfer. The RTDMAC operates as follows:

1. Transfer requests are generated simultaneously to channels 0 and 3.
2. Channel 0 has a higher priority, so the channel 0 transfer begins first (channel 3 waits for transfer).
3. A channel 1 transfer request occurs during the channel 0 transfer (channels 1 and 3 are both waiting)
4. When the channel 0 transfer ends, channel 0 becomes lowest priority.
5. At this point, channel 1 has a higher priority than channel 3, so the channel 1 transfer begins (channel 3 waits for transfer).
6. When the channel 1 transfer ends, channel 1 becomes lowest priority.
7. The channel 3 transfer begins.
8. When the channel 3 transfer ends, channels 3 and 2 shift downward in priority so that channel 3 becomes the lowest priority.

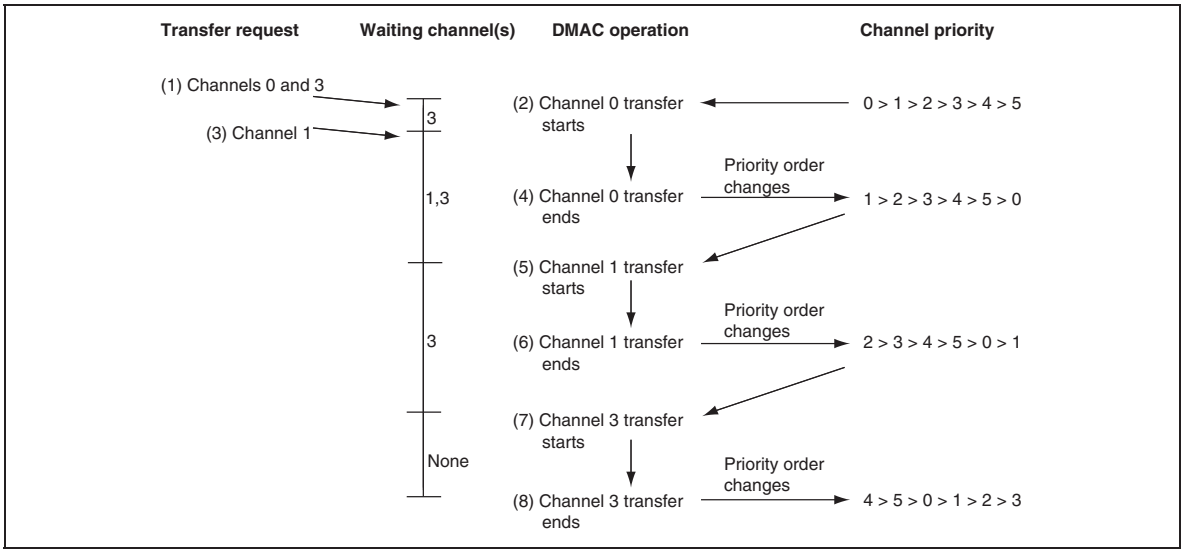


Figure 9.3 Changes in Channel Priority in Round-Robin Mode

9.4.3 Bus Request Priority Push out

The bus request priority push out is a function that assigns the highest value of the bus request priority setting bit in the DMA channel control register B among the output-enabled channels (channels in auto-request mode or channels that accepted a request) as the value of bus request priority being currently output to the SHWY.

Enabling this function prevents the processing of channels with higher bus request priority from being delayed by the presence of channels with lower bus request priority.

Figure 9.4 shows an example in which the bus request priority push out function is enabled.

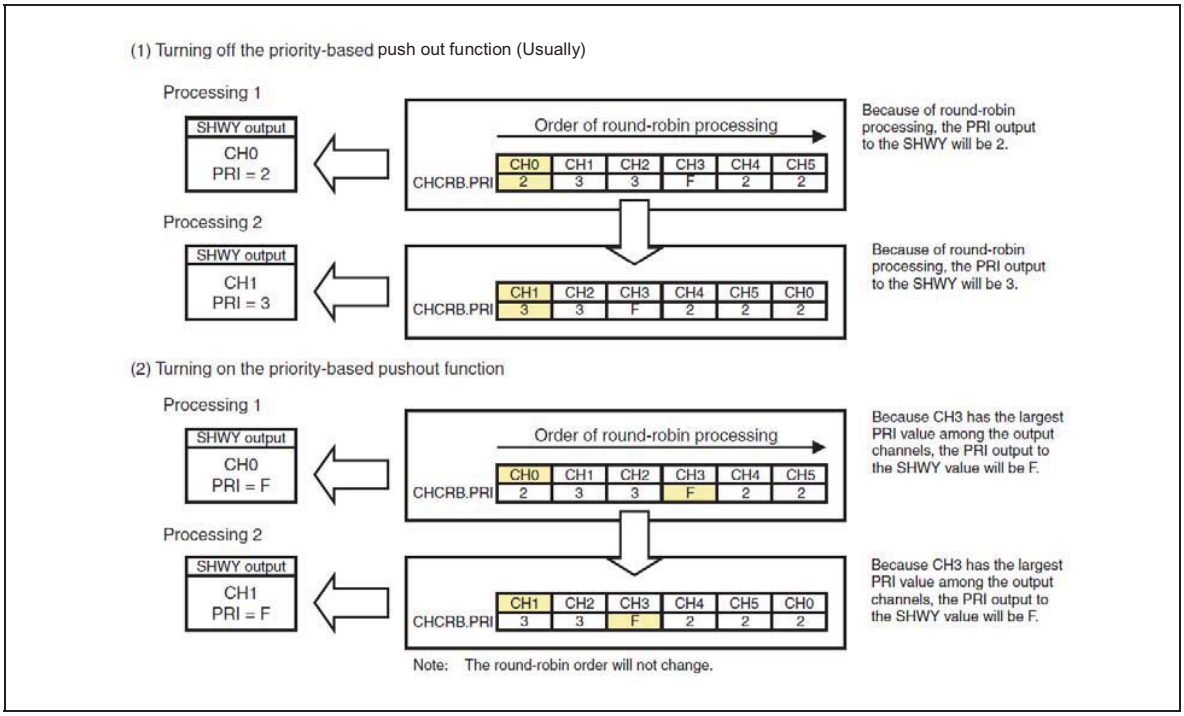


Figure 9.4 Example of Using the Bus Request Priority Push out Function

Note: For details of the PRI signal, see section 1-F Bus Functions.

9.4.4 DMA Transfer Types

DMA transfer is done in dual address mode. As bus mode, cycle steal mode (normal mode and intermittent mode) is used. The RTDMAC supports the transfers shown in Table 9.7.

Table 9.7 Supported DMA Transfers

	Destination			
Source	**External Memory**	**Memory-Mapped External Device**	**On-Chip Peripheral Module**	**X/Y Memory**
External device with DACK	Dual	Dual	Not available	Not available
External memory	Dual	Dual	Dual	Dual
Memory-mapped external device	Dual	Dual	Dual	Dual
On-chip peripheral module	Dual	Dual	Dual	Dual
X/Y memory	Dual	Dual	Dual	Dual

Note: 1. Dual: Dual address mode

(1) Address Mode

(a) Dual Address Mode

In dual address mode, both the transfer source and destination are accessed by addresses. The source and destination can be located externally or internally.

DMA transfer requires two bus cycles because data is read from the transfer source in a data read cycle and written to the transfer destination in a data write cycle. At this time, transfer data is temporarily stored in the RTDMAC. In the transfer between external memories as shown in Figure 9.5, data is read to the RTDMAC from one external memory in a data read cycle, and then that data is written to the other external memory in a write cycle.

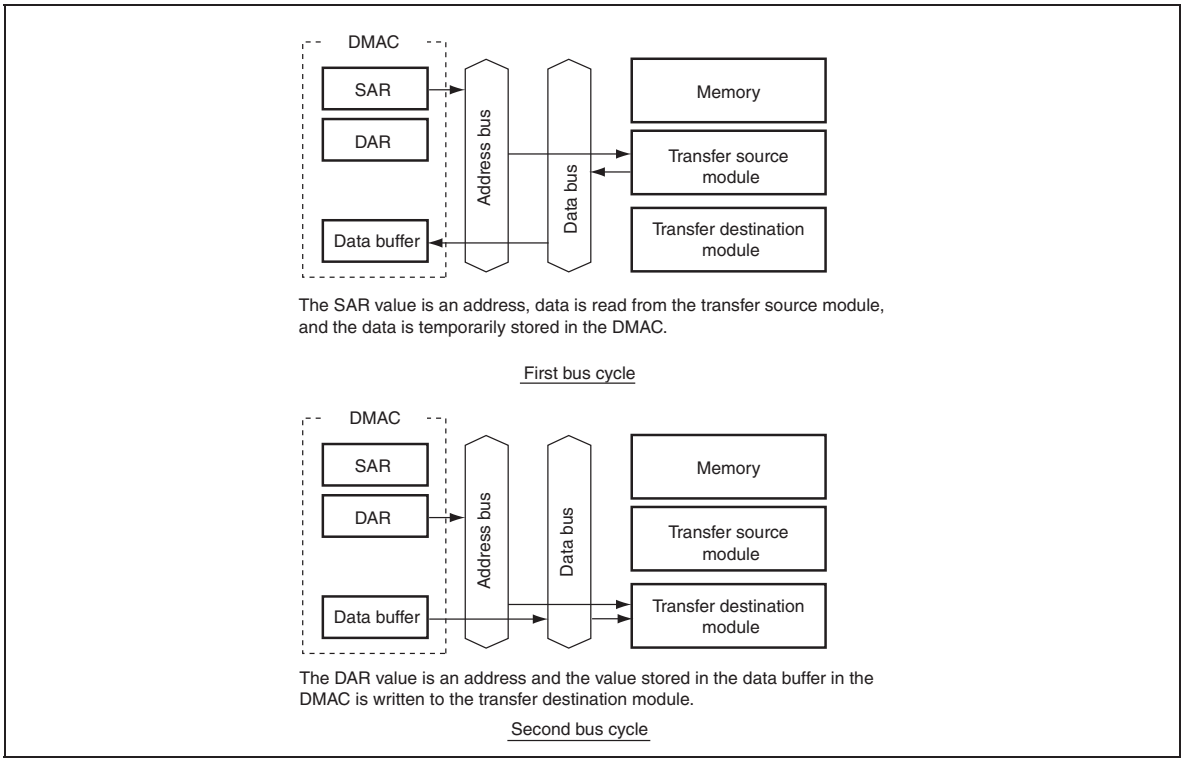


Figure 9.5 Data Flow of Dual Address Mode

Auto request, and on-chip peripheral module request are available for the transfer request.

(2) Bus Modes

Cycle steal mode is used as bus mode.

(a) Cycle-Steal Mode

- Normal mode

  In cycle-steal normal mode, the RTDMAC gives the bus mastership to another bus master every time a unit of transfer (byte, word, longword, 8-byte, 16-byte, 32-byte, or 64-byte unit) is complete. When another transfer request occurs after that, the RTDMAC gets the bus mastership from the other bus master and performs a transfer for one transfer unit. When that transfer ends, the RTDMAC returns the bus mastership to the other bus master. This is repeated until the transfer end conditions are satisfied.

  In cycle-steal normal mode, all transfer areas are available for the transfer request source, transfer source, and transfer destination.

  Figure 9.6 shows an example of DMA transfer timing in cycle-steal normal mode. Transfer conditions shown in the figure are:

  — Condition 1: Dual address mode

  — Condition 2: DREQ low level detection

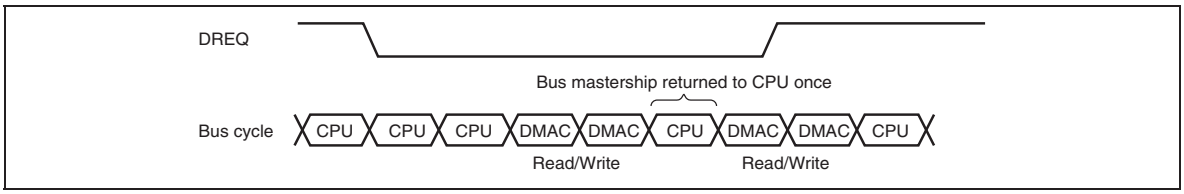


Figure 9.6 DMA Transfer Example in Cycle-Steal Normal Mode (Dual Address, DREQ Low Level Detection)

- Intermittent mode

  In intermittent mode of cycle steal, the RTDMAC gives the bus mastership to another bus master every time a unit of transfer (byte, word, longword, 8-byte, 16-byte, 32-byte or 64-byte unit) is complete. When another transfer request occurs after that, the RTDMAC gets the bus mastership from the other bus master after waiting for 16, 64, or 256 clock cycles in ZSϕ count. The RTDMAC then transfers data of one unit and returns the bus mastership to the other bus master. This is repeated until the transfer end conditions are satisfied. It is thus possible to make lower the ratio of bus occupation by DMA transfer than cycle-steal normal mode.

  When the RTDMAC gets again the bus mastership, DMA transfer can be postponed in case of entry updating due to cache miss.

  In intermittent mode, all transfer areas are available for the transfer request source, transfer source, and transfer destination. The bus modes, however, must be cycle steal mode in all channels.

  Figure 9.7 shows an example of DMA transfer timing in cycle steal intermittent mode. Transfer conditions shown in the figure are:

  — Condition 1: Dual address mode

  — Condition 2: DREQ low level detection

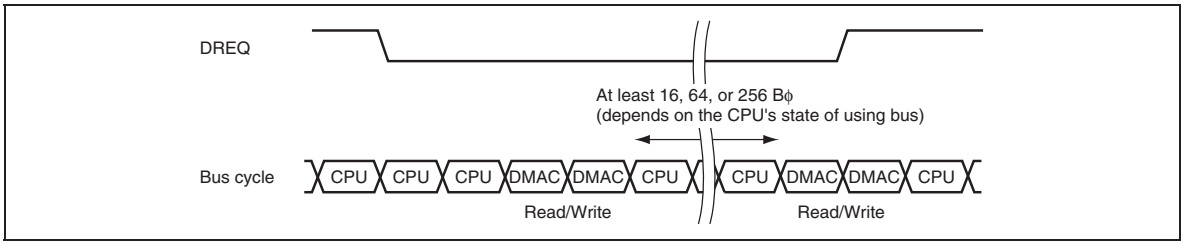


Figure 9.7 Example of DMA Transfer in Cycle Steal Intermittent Mode (Dual Address, DREQ Low Level Detection)

(3) Relationship between Request Modes and Bus Modes by DMA Transfer Category

Table 9.8 shows the relationship between request modes and bus modes by DMA transfer category.

Table 9.8 Relationship between Request Modes and Bus Modes by DMA Transfer Category

Address Mode	Transfer Category	Request Mode	Bus Mode	Transfer Size (Bits)	Usable Channels
Dual	External memory and external memory	External, auto	C	1/2/4/8/16/32/64	0 to 5
	External memory and memory-mapped external device	External, auto	C	1/2/4/8/16/32/64	0 to 5
	Memory-mapped external device and memory-mapped external device	External, auto	C	1/2/4/8/16/32/64	0 to 5
	External memory and on-chip peripheral module	All*[1]	C	1/2/4/8/16/32/64*[2]	0 to 5
	Memory-mapped external device and on-chip peripheral module	All*[1]	C	1/2/4/8/16/32/64*[2]	0 to 5
	On-chip peripheral module and on-chip peripheral module	All*[1]	C	1/2/4/8/16/32/64*[2]	0 to 5
	X/Y memory and X/Y memory	External, auto	C	1/2/4/8/16/32/64	0 to 5
	X/Y memory and memory-mapped external device	External, auto	C	1/2/4/8/16/32/64	0 to 5
	X/Y memory and on-chip peripheral module	All*[1]	C	1/2/4/8/16/32/64*[2]	0 to 5
	X/Y memory and external memory	External, auto	C	1/2/4/8/16/32/64	0 to 5

[Legend]

C: Cycle steal mode

Notes: 1. Auto requests, and on-chip peripheral module requests are all available. However the request source register must be designated as the transfer source or the transfer destination.

2. Access size permitted for the on-chip peripheral module register functioning as the transfer source or transfer destination.

Table 9.9 DMA transfer size according to module

Module	1 byte	2 byte	4 byte	16 byte	32 byte	DREQPAK
BBIF1/2	O	O	O			O
CMT1*						
FLCTL			O	O		
IIC 0/1/2/3/4		O				
MSIOF0/1/2	O	O	O			O
SCIF0/1/2/3/4/5,SCIFB	O					O
SDHI0/1/2		O		O	O	
FSI			O			
TPU0		O				
TSIF0/1			O			O
IRDA					O	
DSI0/1			O			
HSI			O			O
MMC			O			
MFI				O		
SHWYSTAT			O		O	

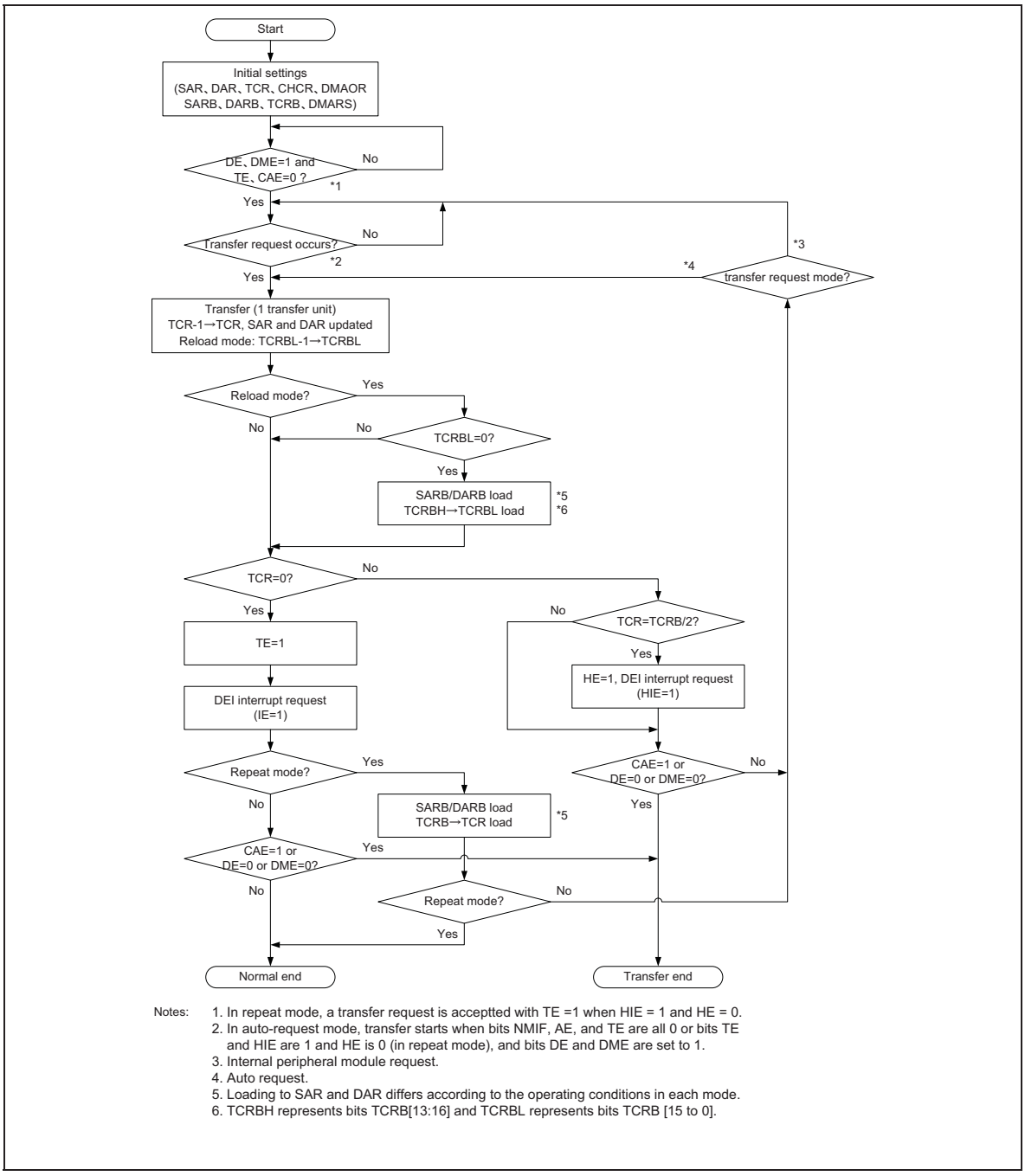
notes : * Never transmits directly to CMT1.

9.4.5 DMA Transfer Flow

After the DMA source address registers (DMASAR), DMA destination address registers (DMADAR), DMA transfer count registers (DMATCR), DMA channel control registers (DMACHCR), DMA operation register (DMAOR), and DMA extended resource selectors (DMARS) are set, the RTDMAC transfers data according to the following procedure:

1. Checks to see if transfer is enabled (DE = 1, DME = 1, TE = 0, CAE = 0)
2. When a transfer request occurs while transfer is enabled, the RTDMAC transfers one transfer unit of data (depending on the setting of the TS3 to TS0 bits). In auto request mode, the transfer begins automatically when the DE bit and DME bit are set to 1. The DMATCR value will be decremented for each transfer. The actual transfer flows vary by address mode and bus mode.
3. When the specified number of transfers have been completed (when DMATCR reaches 0), the transfer ends normally. If the IE bit in DMACHCR is set to 1 at this time, a DEI interrupt is sent to the CPU.
4. When an address error is generated, the transfer is aborted. Transfers are also aborted when the DE bit in DMACHCR or the DME bit in DMAOR is changed to 0.

Figure 9.8 shows a flowchart of this procedure.



Notes:
1. In repeat mode, a transfer request is acceptted with TE =1 when HIE = 1 and HE = 0.
2. In auto-request mode, transfer starts when bits NMIF, AE, and TE are all 0 or bits TE and HIE are 1 and HE is 0 (in repeat mode), and bits DE and DME are set to 1.
3. Internal peripheral module request.
4. Auto request.
5. Loading to SAR and DAR differs according to the operating conditions in each mode.
6. TCRBH represents bits TCRB[13:16] and TCRBL represents bits TCRB [15 to 0].

Figure 9.8 DMA Transfer Flowchart

9.4.6 Repeat Mode Transfer

In a repeat mode transfer, a DMA transfer is repeated without making the transfer settings every time before executing a transfer.

Using a repeat mode transfer with the half end function allows a double buffer transfer executed virtually. The following procedures can be executed effectively by using a repeat mode transfer. As an example, operation of receiving voice data from the VOICE CODEC and compressing it is explained.

In the following example, processing of compressing 40-word voice data for every data reception is explained. In this case, it is assumed that voice data is received by means of MSIOF.

1. RTDMAC settings
- Set address of the MSIOF receive data register in DMASAR
- Set address of an internal memory data store area in DMADAR
- Set DMATCR to 80 (H'50)
- Make the following settings of DMACHCR
  Bits RPT[2:0] = B'010: Repeat mode (use DAR as a repeat area)
  Bit HIE = B'1: TCR/2 interrupt generated
  Bits DM[1:0] = B'01: DAR incremented
  Bits SM[1:0] = B'00: SAR fixed
  Bit IE = B'1: Interrupt enabled
  Bit DE = B'1: DMA transfer enabled
- Set such as bits TB and TS[2:0] according to use conditions
- Set bits CMS[3:0] and PR[1:0] in DMAOR according to use conditions and set the DME bit to B'1

2. Voice data is received and then transferred by MSIOF/RTDMAC
3. DMATCR is decreased to half of its initial value and an interrupt is generated
   Read DMACHCR to confirm that the HE bit is set to 1 by an interrupt processing, and compress 40-word voice data from the address set in DMADAR.
4. DMATCR is cleared to 0 and an interrupt is generated
   Read DMACHCR to confirm that the TE bit is set to 1 by an interrupt processing, and compress 40-word voice data from the address set in DMADAR + 40. After this operation, the value of DMADARB is copied to DMADAR in RTDMAC and initialized, and the value of DMATCRB is copied to DMATCR and initialized to 80.
5. Hereafter, steps 2 and 3 are repeated until bit DME or DE is set to B'0.

As explained above, a repeat mode transfer enables sequential voice compression by switching a buffer for storing data received consequentially and a data buffer for processing signals alternately.

9.4.7 Reload Mode Transfer

In a reload mode transfer, according to the settings of bits RPT[2:0] in DMACHCR, the value set in DMASARB/DMADARB is set to DMASAR/DMADAR and the value of bits DMATCRB[31:16] is set in bits DMATCRB[15:0] every time the number of transfers specified in the DMATCRB[15:0] bits are completed, and the transfer is repeated until DMATCR becomes 0 without specifying the transfer settings again. A reload mode transfer is effective when repeating data transfer with specific areas. Figure 9.9 shows the operation of reload mode transfer.

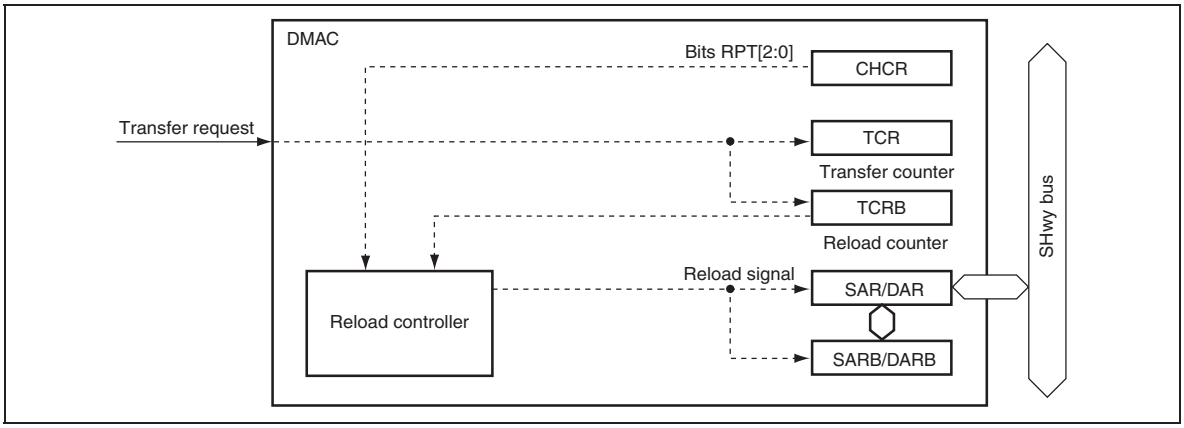


Figure 9.9 Reload Mode Transfer

When a reload mode transfer is executed, DMATCRB is used as a reload counter. Set DMATCRB as described in section 8.3.7, DMA Transfer Count Registers B_0 to 5 (DMATCRB_0 to DMATCRB_5).

9.4.8 Gathering Buffer Function

When the gathering buffer function is made effective, receive data or the transmission data is transmitted collectively in 256 bytes or less. The penalty by the row address mistake of a different bank is reduced to SDRAM by collectively transmitting, and the performance of the transmission improves.

Write 0 to the GL bits in DMACHCRB when you make this function effective on the receiving side. Write 0 to the GS bits in DMACHCRB when you make this function effective at the transmitting side. And, set the GCNT bits in DMACHCRB. After, begin the DMA transfer. This function transmits the size specified for the TS bits in DMACHCR data GCNT+1 collectively. However, when the transfer size exceeds 256 bytes, the transfer size becomes 256 bytes.

When the RS bits in DMACHCR is DMA Extended Resource Selector (B'1000), On-chip peripheral module side can not enable the gathering buffer function.

When the RS bits in DMACHCR is DMA Extended Resource Selector (B'1000), the data that remains in the buffer is output to the memory when writing 0 to the DE bit in DMACHCR while receive data is being collected from the On-chip peripheral module.

The number of packets that remains in the buffer can be confirmed by reading RP bits in DMACHCLR.

Figure 9.10 shows the example of timing when the gathering buffer function is used.

Table 9.10 shows the correspondence table of the gathering buffer function.

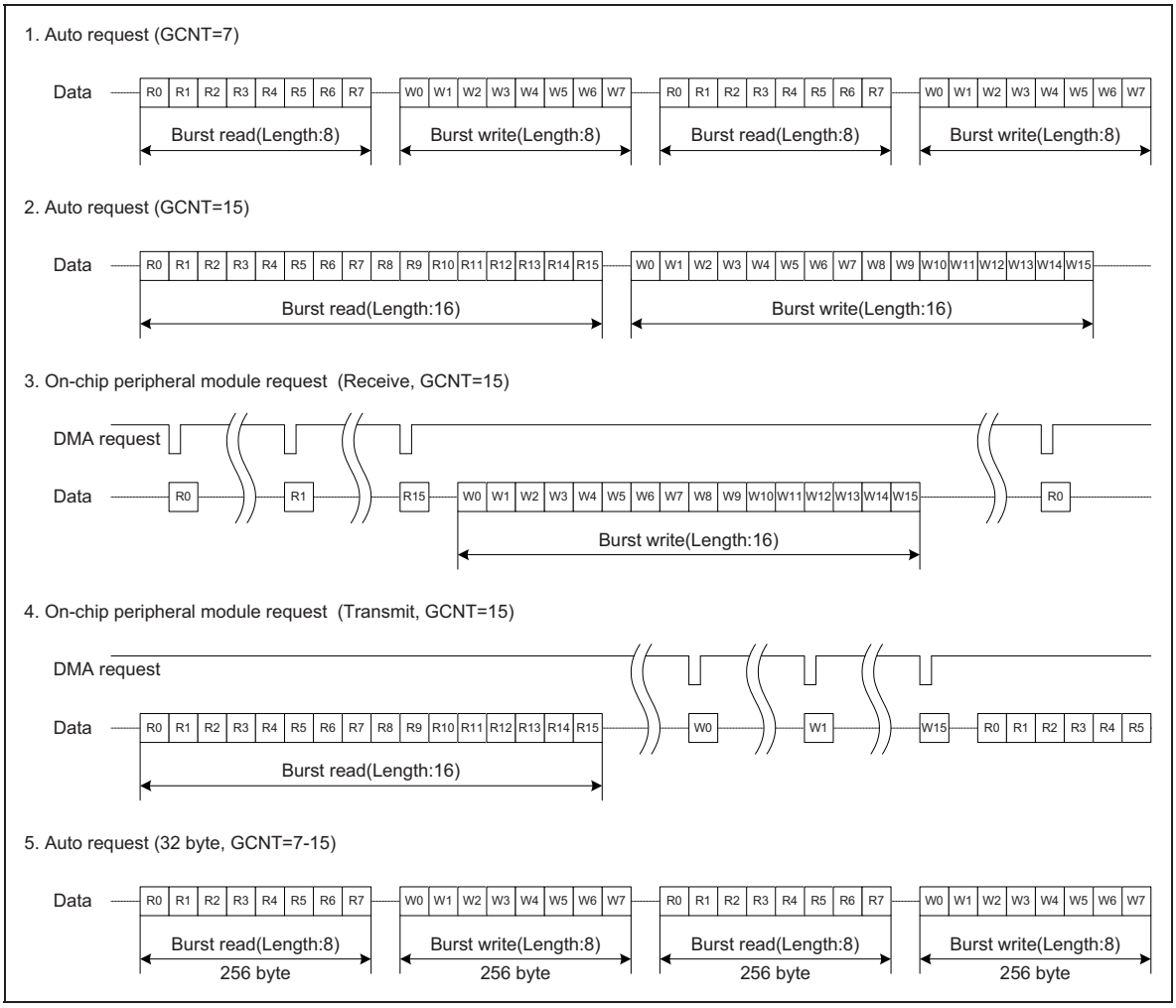


Figure 9.10 Example of Timing when the Gathering Buffer Function is Used

Table 9.10 The Correspondence Table of the Gathering Buffer Function.

Module	Function	Source	Destination
Memory-to-memory	—	Yes	Yes
External device	Transmit and receive	No	No
BBIF1/2	Transmit	Yes	No
	Receive	No	Yes
CMT1	Transmit and receive	No	No
FLCTL	Transmit and receive	No	No
IIC 0/1/2/3/4	Transmit	Yes	No
	Receive	No	Yes
MSIOF0/1/2	Transmit	Yes	No
	Receive	No	Yes
SCIF0/1/2/3/4/5,SCIFB	Transmit	Yes	No
	Receive	No	Yes
SDHI0/1/2	Transmit	Yes	No
	Receive	No	Yes
FSI	Transmit	Yes	No
	Receive	No	Yes
TPU0	Transmit	Yes	No
TSIF0/1	Receive	No	Yes
IRDA	Receive	No	Yes
DSI0/1	Receive	No	Yes
HSI	Transmit	Yes	No
	Receive	No	Yes
MMC	Transmit	Yes	No
	Receive	No	Yes
MFI	Transmit and receive	No	No
SHWYSTAT	Receive	No	Yes

notes : As for the transfer to on-chip peripheral module side, the gathering buffer function is compulsorily invalidated.

9.5 Usage Notes

Pay attentions to the following notes when the RTDMAC is used.

(1) DMA Transfer for Peripheral Modules

When executing a DMA transfer for peripheral modules, an appropriate boundary address should be set for the transfer source or destination address according to the transfer data size. Otherwise, an address error may occur.

(2) Module Stop

While the RTDMAC is in operation, the RTDMAC should not be stopped by the module stop register (MSTPCR0) setting. When the RTDMAC is stopped, transfer contents cannot be guaranteed.

(3) Address Error

Clear the buffer by writing 0 to the CLR bit in DMA channel clear register (DMACHCLR) when the DMA address error occurs. When a DMA address error is generated, set the register of the error-ridden channel again and then start a transfer.

(4) DMA Transfer Stop

Wait for the RP bits in CHCLR to become 0 after writing 0 to the DE bit in CHCR about the stop of the DMA transfer.

(5) DMA Transfer Interruption

When make the DMA transfer interrupted, the interruption disable should be set and set the DE bit in DMA channel control register (DMACHCR) as the DMA transfer disable. If the TE is generated during the DMA transfer interruption, the TE should be initialized. The generation timing after the transfer interruption for an asynchronous assumed following three cases.

1. A case that after setting for the interruption disable, TE is changed to 1 before the CHCR initialization. The TE is initialized by the processing DMA transfer initialization.
2. A case that after setting for the interruption disable, the TE is changed to 1 by ignoring the transfer interruption. After the DMA transfer initialization and the CHCR dummy read, check the TE bit. If the TE bit is 1, the DMA transfer initialization process should be performed.
3. A case that after setting for the interruption disable, the TE is not changed to 0 even though the transfer interruption is occurred.
   After the DMA transfer interruption, the TE is not generated because the transfer data is still remained.

Note: In a case that the DMA transfer initialization is performed while the last transfer is executing, causes TE generation delay. So the dummy read should be performed.

Figure 9.11 shows the processing example when DMA transfer interruption (Data is guaranteed).

Figure 9.12 shows the processing example when DMA transfer interruption (Compulsion interruption).

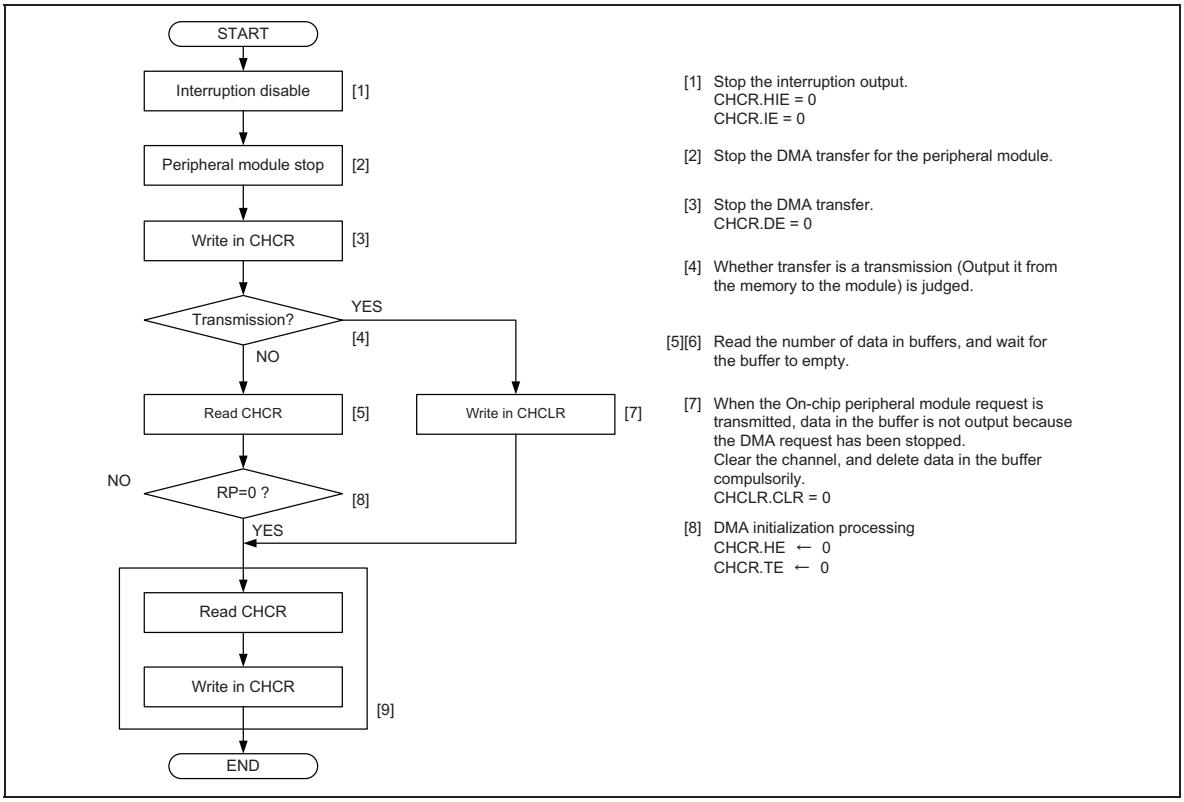


Figure 9.11 Example of RTDMAC Transfer Interruption Processing (Data is Guaranteed)

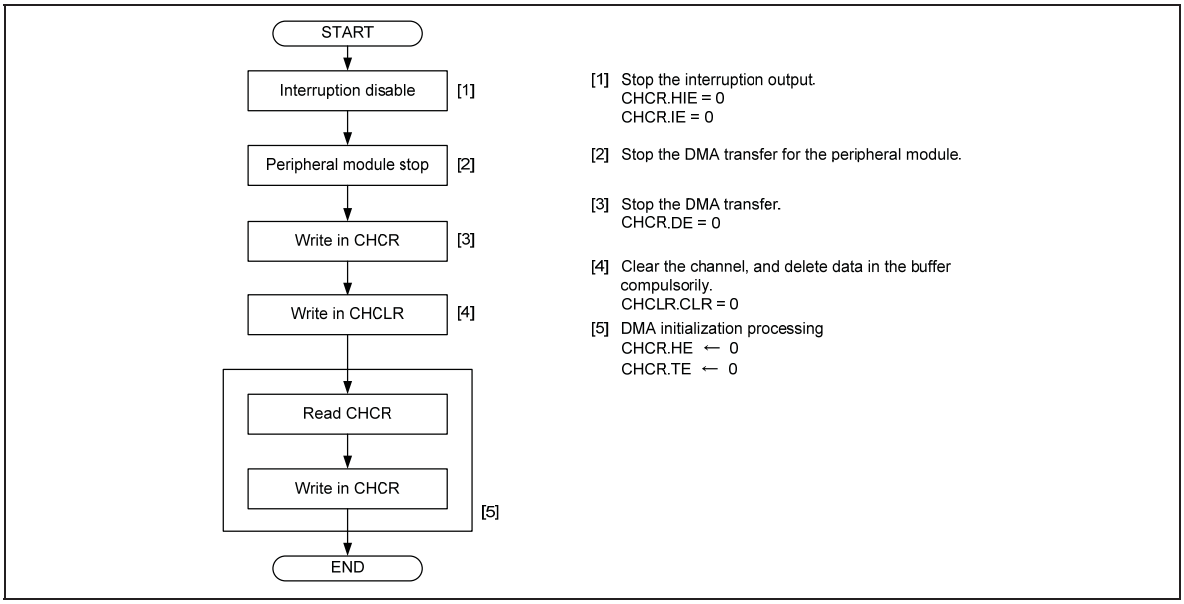


Figure 9.12 Example of RTDMAC Transfer Interruption Processing (Compulsion Interruption)

Section 10 DMAC Auxiliary Functions

10.1 DREQPAK

DREQPAK is a module that enables multiple pieces of DMA single data to be packed and transferred in burst mode to modules (e.g., SCIFA) that can select only small DMA transfer sizes such as bytes and words.

10.1.1 Overview

- Buffers send and receive 32 bytes. DMAC accesses the pack data register in address fixed mode.
- If the 32-byte transfer size contains a fraction, data is transferred in a 32-byte unit with garbage data.
- On the DMAC side, the transfer size is 32 bytes. The value obtained by dividing the transfer size by 32 and rounding up the result is set in the transfer count register. The total size of actual data is set in bytes in DRQPAK.
- Buffers are a ring buffer configuration that is one stage larger than the transfer size in consideration of occurrence of a DREQ from a peripheral module when data is transferred on the DMAC side. The next DREQ is output when near full or near empty is detected.

The following 15 modules are applicable.

SCIFA0, SCIFA1, SCIFA2, SCIFA3, SCIFA4, SCIFA5, SCIFB, MSIOF0, MSIOF1, MSIOF2, BBIF1, BBIF2, HSI, TSIF0, TSIF1

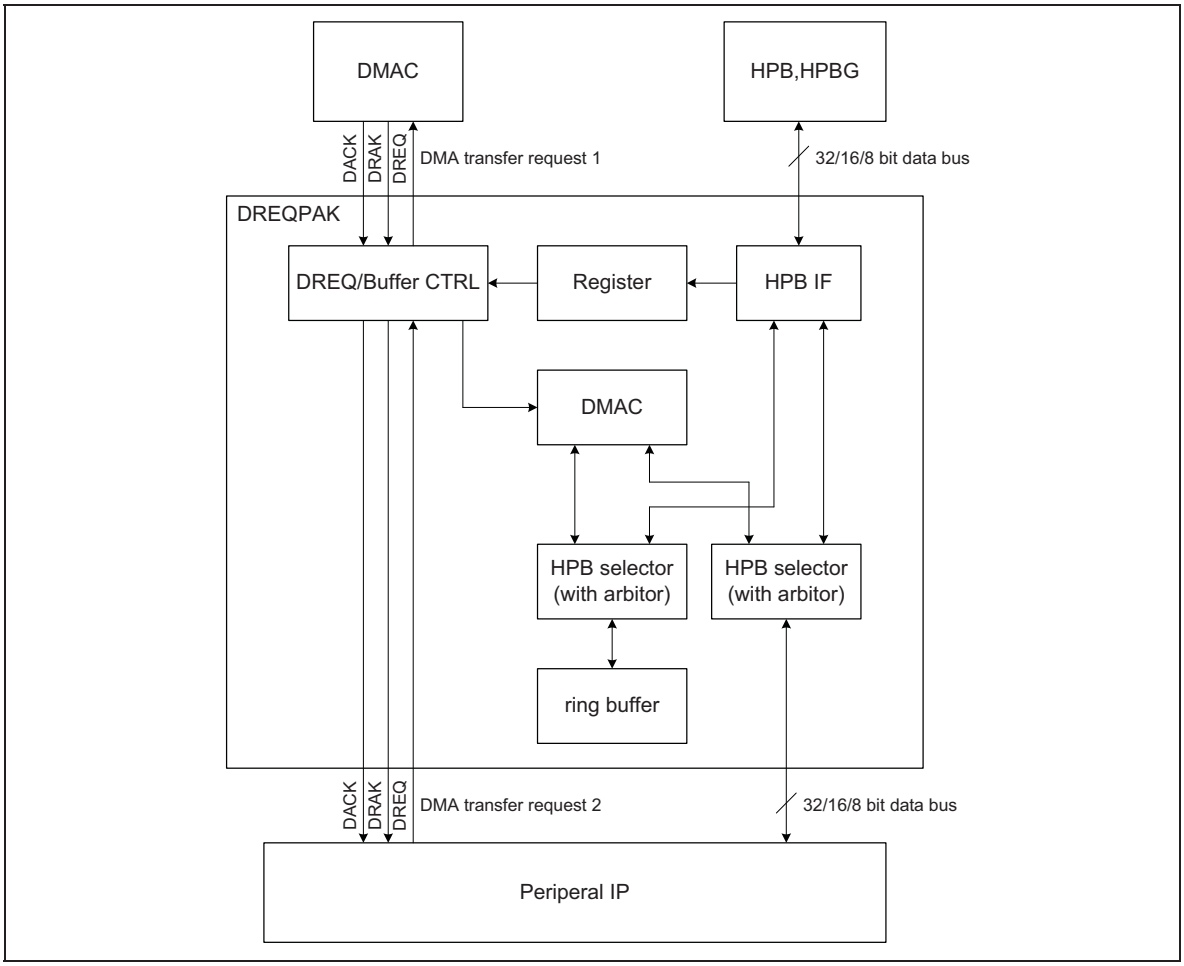


Figure 10.1 DREQPAK Internal Configuration

No access occurs in the upstream SHwy bus even if you use a peripheral module by using DREQPAK. This eliminates troublesome passes of accesses in small data units to the upstream SHwy bus.

An access latency occurs in a bus bridge but the total access time is shortened because the bus bridge reciprocation count becomes less.

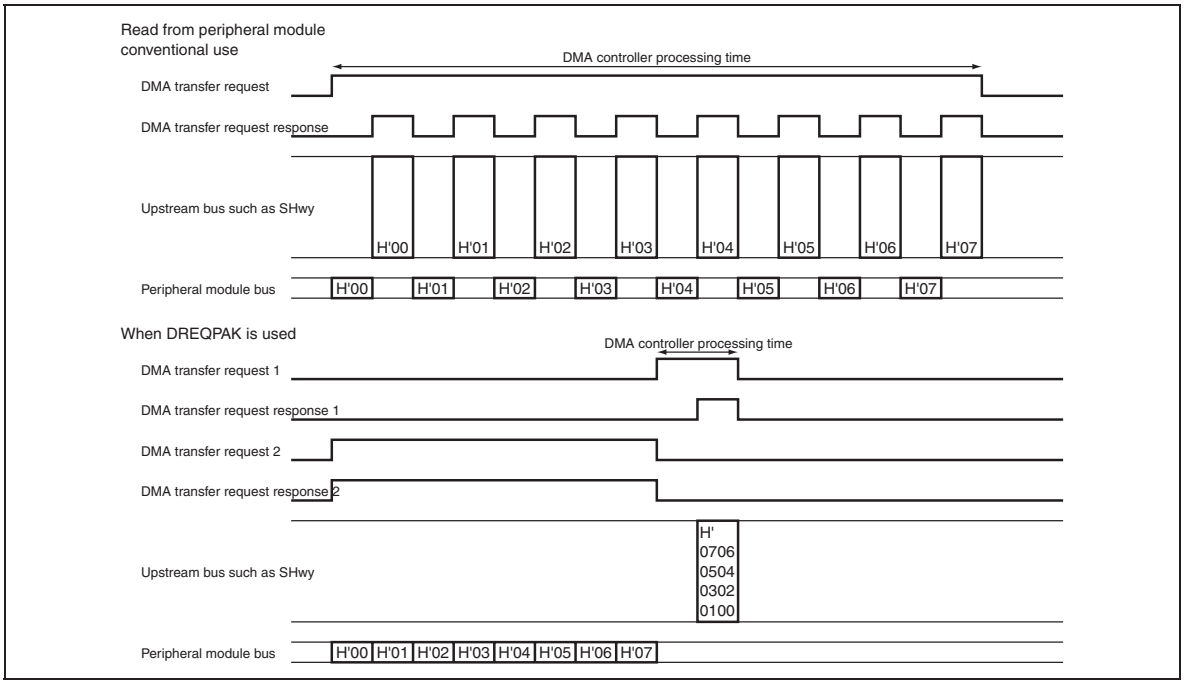


Figure 10.2 DMA Transfer Image When DREQPAK Is Used

10.1.2 DREQPAK Register Descriptions

Table 10.1 shows the DREQPAK register configuration. Table 10.2 shows the register states in each operating mode.

Table 10.1 DREQPAK Control Registers

Name	Register Abbreviation	R/W	Initial Value	Address	Access Size (Bits)	Target DMA Request (Extended Link Selector MID+RID)
SCIFB pack target address register 0	SCBPKTADR0	R/W	H'0000	H'E6C38000	16	SCIFB transmission H'3D
SCIFB pack total size register 0L	SCBPKTSIZER0L	R/W	H'0000	H'E6C38002	16	
SCIFB pack total size register 0H	SCBPKTSIZER0H	R/W	H'0000	H'E6C38004	16	
SCIFB pack control register 0	SCBPKCTLR0	R/W	H'0000	H'E6C38006	16	
SCIFB pack status register 0L	SCBPKSTATR0L	R/W	H'0000	H'E6C38008	16	
SCIFB pack status register 0H	SCBPKSTATR0H	R/W	H'0000	H'E6C3800A	16	
SCIFB pack data register 0	SCBPKDATAR0	R/W	Undefined	H'E6C39000	16	
SCIFB pack target address register 1	SCBPKTADR1	R/W	H'0000	H'E6C3800C	16	SCIFB reception H'3E
SCIFB pack total size register 1L	SCBPKTSIZER1	R/W	H'0000	H'E6C3800E	16	
SCIFB pack total size register 1H	SCBPKTSIZER1	R/W	H'0000	H'E6C38010	16	
SCIFB pack control register 1	SCBPKCTLR1	R/W	H'0000	H'E6C38012	16	
SCIFB pack status register 1L	SCBPKSTATR1	R/W	H'0000	H'E6C38014	16	
SCIFB pack status register 1H	SCBPKSTATR1	R/W	H'0000	H'E6C38016	16	
SCIFB pack data register 1	SCBPKDATAR1	R/W	Undefined	H'E6C3A000	16	
SCIFA0 pack target address register 0	SC0PKTADR0	R/W	H'0000	H'E6C48000	16	SCIFA0 transmission H'21
SCIFA0 pack total size register 0L	SC0PKTSIZER0L	R/W	H'0000	H'E6C48002	16	
SCIFA0 pack total size register 0H	SC0PKTSIZER0H	R/W	H'0000	H'E6C48004	16	
SCIFA0 pack control register 0	SC0PKCTLR0	R/W	H'0000	H'E6C48006	16	
SCIFA0 pack status register 0L	SC0PKSTATR0L	R/W	H'0000	H'E6C48008	16	
SCIFA0 pack status register 0H	SC0PKSTATR0H	R/W	H'0000	H'E6C4800A	16	
SCIFA0 pack data register 0	SC0PKDATAR0	R/W	Undefined	H'E6C49000	16	
SCIFA0 pack target address register 1	SC0PKTADR1	R/W	H'0000	H'E6C4800C	16	SCIFA0 reception H'22
SCIFA0 pack total size register 1L	SC0PKTSIZER1	R/W	H'0000	H'E6C4800E	16	
SCIFA0 pack total size register 1H	SC0PKTSIZER1	R/W	H'0000	H'E6C48010	16	
SCIFA0 pack control register 1	SC0PKCTLR1	R/W	H'0000	H'E6C48012	16	
SCIFA0 pack status register 1L	SC0PKSTATR1	R/W	H'0000	H'E6C48014	16	
SCIFA0 pack status register 1H	SC0PKSTATR1	R/W	H'0000	H'E6C48016	16	
SCIFA0 pack data register 1	SC0PKDATAR1	R/W	Undefined	H'E6C4A000	16	
SCIFA1 pack target address register 0	SC1PKTADR0	R/W	H'0000	H'E6C58000	16	SCIFA1 transmission H'25
SCIFA1 pack total size register 0L	SC1PKTSIZER0L	R/W	H'0000	H'E6C58002	16	

Name	Register Abbreviation	R/W	Initial Value	Address	Access Size (Bits)	Target DMA Request (Extended Link Selector MID+RID)
SCIFA1 pack total size register 0H	SC1PKTSIZER0H	R/W	H'0000	H'E6C58004	16	
SCIFA1 pack control register 0	SC1PKCTLR0	R/W	H'0000	H'E6C58006	16	
SCIFA1 pack status register 0L	SC1PKSTATR0L	R/W	H'0000	H'E6C58008	16	SCIFA1 transmission H'25
SCIFA1 pack status register 0H	SC1PKSTATR0H	R/W	H'0000	H'E6C5800A	16	
SCIFA1 pack data register 0	SC1PKDATAR0	R/W	Undefined	H'E6C59000	16	
SCIFA1 pack target address register 1	SC1PKTADR1	R/W	H'0000	H'E6C5800C	16	
SCIFA1 pack total size register 1L	SC1PKTSIZER1	R/W	H'0000	H'E6C5800E	16	SCIFA1 reception H'26
SCIFA1 pack total size register 1H	SC1PKTSIZER1	R/W	H'0000	H'E6C58010	16	
SCIFA1 pack control register 1	SC1PKCTLR1	R/W	H'0000	H'E6C58012	16	
SCIFA1 pack status register 1L	SC1PKSTATR1	R/W	H'0000	H'E6C58014	16	
SCIFA1 pack status register 1H	SC1PKSTATR1	R/W	H'0000	H'E6C58016	16	
SCIFA1 pack data register 1	SC1PKDATAR1	R/W	Undefined	H'E6C5A000	16	
SCIFA2 pack target address register 0	SC2PKTADR0	R/W	H'0000	H'E6C68000	16	SCIFA2 transmission H'29
SCIFA2 pack total size register 0L	SC2PKTSIZER0L	R/W	H'0000	H'E6C68002	16	
SCIFA2 pack total size register 0H	SC2PKTSIZER0H	R/W	H'0000	H'E6C68004	16	
SCIFA2 pack control register 0	SC2PKCTLR0	R/W	H'0000	H'E6C68006	16	
SCIFA2 pack status register 0L	SC2PKSTATR0L	R/W	H'0000	H'E6C68008	16	
SCIFA2 pack status register 0H	SC2PKSTATR0H	R/W	H'0000	H'E6C6800A	16	
SCIFA2 pack data register 0	SC2PKDATAR0	R/W	Undefined	H'E6C69000	16	
SCIFA2 pack target address register 1	SC2PKTADR1	R/W	H'0000	H'E6C6800C	16	SCIFA2 reception H'2A
SCIFA2 pack total size register 1L	SC2PKTSIZER1	R/W	H'0000	H'E6C6800E	16	
SCIFA2 pack total size register 1H	SC2PKTSIZER1	R/W	H'0000	H'E6C68010	16	
SCIFA2 pack control register 1	SC2PKCTLR1	R/W	H'0000	H'E6C68012	16	
SCIFA2 pack status register 1L	SC2PKSTATR1	R/W	H'0000	H'E6C68014	16	
SCIFA2 pack status register 1H	SC2PKSTATR1	R/W	H'0000	H'E6C68016	16	
SCIFA2 pack data register 1	SC2PKDATAR1	R/W	Undefined	H'E6C6A000	16	
SCIFA3 pack target address register 0	SC3PKTADR0	R/W	H'0000	H'E6C78000	16	SCIFA3 transmission H'2D
SCIFA3 pack total size register 0L	SC3PKTSIZER0L	R/W	H'0000	H'E6C78002	16	
SCIFA3 pack total size register 0H	SC3PKTSIZER0H	R/W	H'0000	H'E6C78004	16	
SCIFA3 pack control register 0	SC3PKCTLR0	R/W	H'0000	H'E6C78006	16	
SCIFA3 pack status register 0L	SC3PKSTATR0L	R/W	H'0000	H'E6C78008	16	
SCIFA3 pack status register 0H	SC3PKSTATR0H	R/W	H'0000	H'E6C7800A	16	
SCIFA3 pack data register 0	SC3PKDATAR0	R/W	Undefined	H'E6C79000	16	
SCIFA3 pack target address register 1	SC3PKTADR1	R/W	H'0000	H'E6C7800C	16	SCIFA3 reception H'2E

Name	Register Abbreviation	R/W	Initial Value	Address	Access Size (Bits)	Target DMA Request (Extended Link Selector MID+RID)
SCIFA3 pack total size register 1L	SC3PKTSIZER1	R/W	H'0000	H'E6C7800E	16	
SCIFA3 pack total size register 1H	SC3PKTSIZER1	R/W	H'0000	H'E6C78010	16	
SCIFA3 pack control register 1	SC3PKCTLR1	R/W	H'0000	H'E6C78012	16	
SCIFA3 pack status register 1L	SC3PKSTATR1	R/W	H'0000	H'E6C78014	16	
SCIFA3 pack status register 1H	SC3PKSTATR1	R/W	H'0000	H'E6C78016	16	
SCIFA3 pack data register 1	SC3PKDATAR1	R/W	Undefined	H'E6C7A000	16	
SCIFA4 pack target address register 0	SC4PKTADR0	R/W	H'0000	H'E6C88000	16	SCIFA4 transmission H'39
SCIFA4 pack total size register 0L	SC4PKTSIZER0L	R/W	H'0000	H'E6C88002	16	
SCIFA4 pack total size register 0H	SC4PKTSIZER0H	R/W	H'0000	H'E6C88004	16	
SCIFA4 pack control register 0	SC4PKCTLR0	R/W	H'0000	H'E6C88006	16	
SCIFA4 pack status register 0L	SC4PKSTATR0L	R/W	H'0000	H'E6C88008	16	
SCIFA4 pack status register 0H	SC4PKSTATR0H	R/W	H'0000	H'E6C8800A	16	
SCIFA4 pack data register 0	SC4PKDATAR0	R/W	Undefined	H'E6C89000	16	
SCIFA4 pack target address register 1	SC4PKTADR1	R/W	H'0000	H'E6C8800C	16	SCIFA4 reception H'3A
SCIFA4 pack total size register 1L	SC4PKTSIZER1	R/W	H'0000	H'E6C8800E	16	
SCIFA4 pack total size register 1H	SC4PKTSIZER1	R/W	H'0000	H'E6C88010	16	
SCIFA4 pack control register 1	SC4PKCTLR1	R/W	H'0000	H'E6C88012	16	
SCIFA4 pack status register 1L	SC4PKSTATR1	R/W	H'0000	H'E6C88014	16	
SCIFA4 pack status register 1H	SC4PKSTATR1	R/W	H'0000	H'E6C88016	16	
SCIFA4 pack data register 1	SC4PKDATAR1	R/W	Undefined	H'E6C8A000	16	
SCIFA5 pack target address register 0	SC5PKTADR0	R/W	H'0000	H'E6CB8000	16	SCIFA5 transmission H'35
SCIFA5 pack total size register 0L	SC5PKTSIZER0L	R/W	H'0000	H'E6CB8002	16	
SCIFA5 pack total size register 0H	SC5PKTSIZER0H	R/W	H'0000	H'E6CB8004	16	
SCIFA5 pack control register 0	SC5PKCTLR0	R/W	H'0000	H'E6CB8006	16	
SCIFA5 pack status register 0L	SC5PKSTATR0L	R/W	H'0000	H'E6CB8008	16	
SCIFA5 pack status register 0H	SC5PKSTATR0H	R/W	H'0000	H'E6CB800A	16	
SCIFA5 pack data register 0	SC5PKDATAR0	R/W	Undefined	H'E6CB9000	16	
SCIFA5 pack target address register 1	SC5PKTADR1	R/W	H'0000	H'E6CB800C	16	SCIFA5 reception H'36
SCIFA5 pack total size register 1L	SC5PKTSIZER1	R/W	H'0000	H'E6CB800E	16	
SCIFA5 pack total size register 1H	SC5PKTSIZER1	R/W	H'0000	H'E6CB8010	16	
SCIFA5 pack control register 1	SC5PKCTLR1	R/W	H'0000	H'E6CB8012	16	
SCIFA5 pack status register 1L	SC5PKSTATR1	R/W	H'0000	H'E6CB8014	16	
SCIFA5 pack status register 1H	SC5PKSTATR1	R/W	H'0000	H'E6CB8016	16	
SCIFA5 pack data register 1	SC5PKDATAR1	R/W	Undefined	H'E6CBA000	16	

Name	Register Abbreviation	R/W	Initial Value	Address	Access Size (Bits)	Target DMA Request (Extended Link Selector MID+RID)
BBIF1 pack target address register 0	BB1PKTADR0	R/W	H'0000 0000	H'E6C98000	32	BBIF1 transmission H'59
BBIF1 pack total size register 0	BB1PKTSIZER0	R/W	H'0000 0000	H'E6C98004	32	
BBIF1 pack control register 0	BB1PKCTLR0	R/W	H'0000 0000	H'E6C98008	32	
BBIF1 pack status register 0	BB1PKSTATR0	R/W	H'0000 0000	H'E6C9800C	32	
BBIF1 pack data register 0	BB1PKDATAR0	R/W	Undefined	H'E6C99000	32	
BBIF1 pack target address register 1	BB1PKTADR1	R/W	H'0000 0000	H'E6C98010	32	BBIF1 reception H'5A
BBIF1 pack total size register 1	BB1PKTSIZER1	R/W	H'0000 0000	H'E6C98014	32	
BBIF1 pack control register 1	BB1PKCTLR1	R/W	H'0000 0000	H'E6C98018	32	
BBIF1 pack status register 1	BB1PKSTATR1	R/W	H'0000 0000	H'E6C9801C	32	
BBIF1 pack data register 1	BB1PKDATAR1	R/W	Undefined	H'E6C9A000	32	
BBIF2 pack target address register 0	BB2PKTADR0	R/W	H'0000 0000	H'E6CA8000 H'FFFA8000	32	BBIF2 transmission H'5D
BBIF2 pack total size register 0	BB2PKTSIZER0	R/W	H'0000 0000	H'E6CA8004 H'FFFA8004	32	
BBIF2 pack control register 0	BB2PKCTLR0	R/W	H'0000 0000	H'E6CA8008 H'FFFA8008	32	
BBIF2 pack status register 0	BB2PKSTATR0	R/W	H'0000 0000	H'E6CA800C H'FFFA800C	32	
BBIF2 pack data register 0	BB2PKDATAR0	R/W	Undefined	H'E6CA9000 H'FFFA9000	32	
BBIF2 pack target address register 1	BB2PKTADR1	R/W	H'0000 0000	H'E6CA8010 H'FFFA8010	32	BBIF2 reception H'5E
BBIF2 pack total size register 1	BB2PKTSIZER1	R/W	H'0000 0000	H'E6CA8014 H'FFFA8014	32	
BBIF2 pack control register 1	BB2PKCTLR1	R/W	H'0000 0000	H'E6CA8018 H'FFFA8018	32	
BBIF2 pack status register 1	BB2PKSTATR1	R/W	H'0000 0000	H'E6CA801C H'FFFA801C	32	
BBIF2 pack data register 1	BB2PKDATAR1	R/W	Undefined	H'E6CAA000 H'FFFAA000	32	
MSIOF0 pack target address register 0	MS0PKTADR0	R/W	H'0000 0000	H'FFF18000	32	MSIOF0 transmission H'51
MSIOF0 pack total size register 0	MS0PKTSIZER0	R/W	H'0000 0000	H'FFF18004	32	
MSIOF0 pack control register 0	MS0PKCTLR0	R/W	H'0000 0000	H'FFF18008	32	
MSIOF0 pack status register 0	MS0PKSTATR0	R/W	H'0000 0000	H'FFF1800C	32	
MSIOF0 pack data register 0	MS0PKDATAR0	R/W	Undefined	H'FFF19000	32	
MSIOF0 pack target address register 1	MS0PKTADR1	R/W	H'0000 0000	H'FFF18010	32	MSIOF0 reception H'52
MSIOF0 pack total size register 1	MS0PKTSIZER1	R/W	H'0000 0000	H'FFF18014	32	
MSIOF0 pack control register 1	MS0PKCTLR1	R/W	H'0000 0000	H'FFF18018	32	
MSIOF0 pack status register 1	MS0PKSTATR1	R/W	H'0000 0000	H'FFF1801C	32	
MSIOF0 pack data register 1	MS0PKDATAR1	R/W	Undefined	H'FFF1A000	32	
MSIOF1 pack target address register 0	MS1PKTADR0	R/W	H'0000 0000	H'E6E18000	32	MSIOF1 transmission H'55

Name	Register Abbreviation	R/W	Initial Value	Address	Access Size (Bits)	Target DMA Request (Extended Link Selector MID+RID)
MSIOF1 pack total size register 0	MS1PKTSIZER0	R/W	H'0000 0000	H'E6E18004	32	
MSIOF1 pack control register 0	MS1PKCTLR0	R/W	H'0000 0000	H'E6E18008	32	
MSIOF1 pack status register 0	MS1PKSTATR0	R/W	H'0000 0000	H'E6E1800C	32	
MSIOF1 pack data register 0	MS1PKDATAR0	R/W	H'0000 0000	H'E6E19000	32	
MSIOF1 pack target address register 1	MS1PKTADR1	R/W	H'0000 0000	H'E6E18010	32	MSIOF1 reception H'56
MSIOF1 pack total size register 1	MS1PKTSIZER1	R/W	H'0000 0000	H'E6E18014	32	
MSIOF1 pack control register 1	MS1PKCTLR1	R/W	H'0000 0000	H'E6E18018	32	
MSIOF1 pack status register 1	MS1PKSTATR1	R/W	H'0000 0000	H'E6E1801C	32	
MSIOF1 pack data register 1	MS1PKDATAR1	R/W	Undefined	H'E6E1A000	32	
MSIOF2 pack target address register 0	MS2PKTADR0	R/W	H'0000 0000	H'E6E08000	32	MSIOF2 transmission H'41
MSIOF2 pack total size register 0	MS2PKTSIZER0	R/W	H'0000 0000	H'E6E08004	32	
MSIOF2 pack control register 0	MS2PKCTLR0	R/W	H'0000 0000	H'E6E08008	32	
MSIOF2 pack status register 0	MS2PKSTATR0	R/W	H'0000 0000	H'E6E0800C	32	
MSIOF2 pack data register 0	MS2PKDATAR0	R/W	H'0000 0000	H'E6E09000	32	
MSIOF2 pack target address register 1	MS2PKTADR1	R/W	H'0000 0000	H'E6E08010	32	MSIOF2 reception H'42
MSIOF2 pack total size register 1	MS2PKTSIZER1	R/W	H'0000 0000	H'E6E08014	32	
MSIOF2 pack control register 1	MS2PKCTLR1	R/W	H'0000 0000	H'E6E08018	32	
MSIOF2 pack status register 1	MS2PKSTATR1	R/W	H'0000 0000	H'E6E0801C	32	
MSIOF2 pack data register 1	MS2PKDATAR1	R/W	Undefined	H'E6E0A000	32	
HSI pack target address register 0	HSIPKTADR0	R/W	H'0000 0000	H'E6A48000	32	HSI transmission H'09
HSI pack total size register 0	HSIPKTSIZER0	R/W	H'0000 0000	H’E6A48004	32	
HSI pack control register 0	HSIPKCTLR0	R/W	H'0000 0000	H’E6A48008	32	
HSI pack status register 0	HSIPKSTATR0	R/W	H'0000 0000	H’E6A4800C	32	
HSI pack data register 0	HSIPKDATAR0	R/W	Undefined	H’E6A49000	32	
HSI pack target address register 1	HSIPKTADR1	R/W	H'0000 0000	H’E6A48010	32	HSI reception H'0A
HSI pack total size register 1	HSIPKTSIZER1	R/W	H'0000 0000	H’E6A48014	32	
HSI pack control register 1	HSIPKCTLR1	R/W	H'0000 0000	H’E6A48018	32	
HSI pack status register 1	HSIPKSTATR1	R/W	H'0000 0000	H’E6A4801C	32	
HSI pack data register 1	HSIPKDATAR1	R/W	Undefined	H’E6A49010	32	
HSI pack target address register 2	HSIPKTADR2	R/W	H'0000 0000	H’E6A48020	32	HSI transmission H'0D
HSI pack total size register 2	HSIPKTSIZER2	R/W	H'0000 0000	H’E6A48024	32	
HSI pack control register 2	HSIPKCTLR2	R/W	H'0000 0000	H’E6A48028	32	
HSI pack status register 2	HSIPKSTATR2	R/W	H'0000 0000	H’E6A4802C	32	
HSI pack data register 2	HSIPKDATAR2	R/W	Undefined	H’E6A49020	32	
HSI pack target address register 3	HSIPKTADR3	R/W	H'0000 0000	H’E6A48030	32	HSI reception H'0E
HSI pack total size register 3	HSIPKTSIZER3	R/W	H'0000 0000	H’E6A48034	32	
HSI pack control register 3	HSIPKCTLR3	R/W	H'0000 0000	H’E6A48038	32	
HSI pack status register 3	HSIPKSTATR3	R/W	H'0000 0000	H’E6A4803C	32	
HSI pack data register 3	HSIPKDATAR3	R/W	Undefined	H’E6A49030	32	

Name	Register Abbreviation	R/W	Initial Value	Address	Access Size (Bits)	Target DMA Request (Extended Link Selector MID+RID)
HSI pack target address register 4	HSIPKTADR4	R/W	H'0000 0000	H'E6A48040	32	HSI transmission H'11
HSI pack total size register 4	HSIPKTSIZER4	R/W	H'0000 0000	H'E6A48044	32	
HSI pack control register 4	HSIPKCTLR4	R/W	H'0000 0000	H'E6A48048	32	
HSI pack status register 4	HSIPKSTATR4	R/W	H'0000 0000	H'E6A4804C	32	
HSI pack data register 4	HSIPKDATAR4	R/W	Undefined	H'E6A49040	32	
HSI pack target address register 5	HSIPKTADR5	R/W	H'0000 0000	H'E6A48050	32	HSI reception H'12
HSI pack total size register 5	HSIPKTSIZER5	R/W	H'0000 0000	H'E6A48054	32	
HSI pack control register 5	HSIPKCTLR5	R/W	H'0000 0000	H'E6A48058	32	
HSI pack status register 5	HSIPKSTATR5	R/W	H'0000 0000	H'E6A4805C	32	
HSI pack data register 5	HSIPKDATAR5	R/W	Undefined	H'E6A49050	32	
HSI pack target address register 6	HSIPKTADR6	R/W	H'0000 0000	H'E6A48060	32	HSI transmission H'15
HSI pack total size register 6	HSIPKTSIZER6	R/W	H'0000 0000	H'E6A48064	32	
HSI pack control register 6	HSIPKCTLR6	R/W	H'0000 0000	H'E6A48068	32	
HSI pack status register 6	HSIPKSTATR6	R/W	H'0000 0000	H'E6A4806C	32	
HSI pack data register 6	HSIPKDATAR6	R/W	Undefined	H'E6A49060	32	
HSI pack target address register 7	HSIPKTADR7	R/W	H'0000 0000	H'E6A48070	32	HSI reception H'16
HSI pack total size register 7	HSIPKTSIZER7	R/W	H'0000 0000	H'E6A48074	32	
HSI pack control register 7	HSIPKCTLR7	R/W	H'0000 0000	H'E6A48078	32	
HSI pack status register 7	HSIPKSTATR7	R/W	H'0000 0000	H'E6A4807C	32	
HSI pack data register 7	HSIPKDATAR7	R/W	Undefined	H'E6A49070	32	
TSIF0 pack target address register 0	TS0PKTADR0	R/W	H'0000	H'FFE88000	32	TSIF0 reception H'EA
TSIF0 pack total size register 0	TS0PKTSIZER0L	R/W	H'0000	H'FFE88004	32	
TSIF0 pack control register 0	TS0PKCTLR0	R/W	H'0000	H'FFE88008	32	
TSIF0 pack status register 0	TS0PKSTATR0H	R/W	H'0000	H'FFE8800C	32	
TSIF0 pack data register 0	TS0PKDATAR0	R/W	Undefined	H'FFE89000	32	
TSIF1 pack target address register 0	TS1PKTADR0	R/W	H'0000	H'FFE98000	32	TSIF0 reception H'EE
TSIF1 pack total size register 0	TS1PKTSIZER0L	R/W	H'0000	H'FFE98004	32	
TSIF1 pack control register 0	TS1PKCTLR0	R/W	H'0000	H'FFE98008	32	
TSIF1 pack status register 0	TS1PKSTATR0H	R/W	H'0000	H'FFE9800C	32	
TSIF1 pack data register 0	TS1PKDATAR0	R/W	Undefined	H'FFE99000	32	

Table 10.2 Register States in Each Operating Mode

Abbreviation	Reset*	Module Standby
SCBPKTADR0	Initialized	Retained
SCBPKTSIZER0L	Initialized	Retained
SCBPKTSIZER0H	Initialized	Retained
SCBPKCTLR0	Initialized	Retained
SCBPKSTATR0L	Initialized	Retained

Abbreviation	Reset*	Module Standby
SCBPKSTATR0H	Initialized	Retained
SCBPKDATAR0	Initialized	Retained
SCBPKTADR1	Initialized	Retained
SCBPKTSIZER1	Initialized	Retained
SCBPKTSIZER1	Initialized	Retained
SCBPKCTLR1	Initialized	Retained
SCBPKSTATR1	Initialized	Retained
SCBPKSTATR1	Initialized	Retained
SCBPKDATAR1	Initialized	Retained
SC0PKTADR0	Initialized	Retained
SC0PKTSIZER0L	Initialized	Retained
SC0PKTSIZER0H	Initialized	Retained
SC0PKCTLR0	Initialized	Retained
SC0PKSTATR0L	Initialized	Retained
SC0PKSTATR0H	Initialized	Retained
SC0PKDATAR0	Initialized	Retained
SC0PKTADR1	Initialized	Retained
SC0PKTSIZER1	Initialized	Retained
SC0PKTSIZER1	Initialized	Retained
SC0PKCTLR1	Initialized	Retained
SC0PKSTATR1	Initialized	Retained
SC0PKSTATR1	Initialized	Retained
SC0PKDATAR1	Initialized	Retained
SC1PKTADR0	Initialized	Retained
SC1PKTSIZER0L	Initialized	Retained
SC1PKTSIZER0H	Initialized	Retained
SC1PKCTLR0	Initialized	Retained
SC1PKSTATR0L	Initialized	Retained
SC1PKSTATR0H	Initialized	Retained
SC1PKDATAR0	Initialized	Retained
SC1PKTADR1	Initialized	Retained
SC1PKTSIZER1	Initialized	Retained
SC1PKTSIZER1	Initialized	Retained
SC1PKCTLR1	Initialized	Retained
SC1PKSTATR1	Initialized	Retained
SC1PKSTATR1	Initialized	Retained
SC1PKDATAR1	Initialized	Retained
SC2PKTADR0	Initialized	Retained
SC2PKTSIZER0L	Initialized	Retained
SC2PKTSIZER0H	Initialized	Retained
SC2PKCTLR0	Initialized	Retained
SC2PKSTATR0L	Initialized	Retained

Abbreviation	Reset*	Module Standby
SC2PKSTATR0H	Initialized	Retained
SC2PKDATAR0	Initialized	Retained
SC2PKTADR1	Initialized	Retained
SC2PKTSIZER1	Initialized	Retained
SC2PKTSIZER1	Initialized	Retained
SC2PKCTLR1	Initialized	Retained
SC2PKSTATR1	Initialized	Retained
SC2PKSTATR1	Initialized	Retained
SC2PKDATAR1	Initialized	Retained
SC3PKTADR0	Initialized	Retained
SC3PKTSIZER0L	Initialized	Retained
SC3PKTSIZER0H	Initialized	Retained
SC3PKCTLR0	Initialized	Retained
SC3PKSTATR0L	Initialized	Retained
SC3PKSTATR0H	Initialized	Retained
SC3PKDATAR0	Initialized	Retained
SC3PKTADR1	Initialized	Retained
SC3PKTSIZER1	Initialized	Retained
SC3PKTSIZER1	Initialized	Retained
SC3PKCTLR1	Initialized	Retained
SC3PKSTATR1	Initialized	Retained
SC3PKSTATR1	Initialized	Retained
SC3PKDATAR1	Initialized	Retained
SC4PKTADR0	Initialized	Retained
SC4PKTSIZER0L	Initialized	Retained
SC4PKTSIZER0H	Initialized	Retained
SC4PKCTLR0	Initialized	Retained
SC4PKSTATR0L	Initialized	Retained
SC4PKSTATR0H	Initialized	Retained
SC4PKDATAR0	Initialized	Retained
SC4PKTADR1	Initialized	Retained
SC4PKTSIZER1	Initialized	Retained
SC4PKTSIZER1	Initialized	Retained
SC4PKCTLR1	Initialized	Retained
SC4PKSTATR1	Initialized	Retained
SC4PKSTATR1	Initialized	Retained
SC4PKDATAR1	Initialized	Retained
SC5PKTADR0	Initialized	Retained
SC5PKTSIZER0L	Initialized	Retained
SC5PKTSIZER0H	Initialized	Retained
SC5PKCTLR0	Initialized	Retained
SC5PKSTATR0L	Initialized	Retained

Abbreviation	Reset*	Module Standby
SC5PKSTATR0H	Initialized	Retained
SC5PKDATAR0	Initialized	Retained
SC5PKTADR1	Initialized	Retained
SC5PKTSIZER1	Initialized	Retained
SC5PKTSIZER1	Initialized	Retained
SC5PKCTLR1	Initialized	Retained
SC5PKSTATR1	Initialized	Retained
SC5PKSTATR1	Initialized	Retained
SC5PKDATAR1	Initialized	Retained
BB1PKTADR0	Initialized	Retained
BB1PKTSIZER0	Initialized	Retained
BB1PKCTLR0	Initialized	Retained
BB1PKSTATR0	Initialized	Retained
BB1PKDATAR0	Initialized	Retained
BB1PKTADR1	Initialized	Retained
BB1PKTSIZER1	Initialized	Retained
BB1PKCTLR1	Initialized	Retained
BB1PKSTATR1	Initialized	Retained
BB1PKDATAR1	Initialized	Retained
BB2PKTADR0	Initialized	Retained
BB2PKTSIZER0	Initialized	Retained
BB2PKCTLR0	Initialized	Retained
BB2PKSTATR0	Initialized	Retained
BB2PKDATAR0	Initialized	Retained
BB2PKTADR1	Initialized	Retained
BB2PKTSIZER1	Initialized	Retained
BB2PKCTLR1	Initialized	Retained
BB2PKSTATR1	Initialized	Retained
BB2PKDATAR1	Initialized	Retained
MS0PKTADR0	Initialized	Retained
MS0PKTSIZER0	Initialized	Retained
MS0PKCTLR0	Initialized	Retained
MS0PKSTATR0	Initialized	Retained
MS0PKDATAR0	Initialized	Retained
MS0PKTADR1	Initialized	Retained
MS0PKTSIZER1	Initialized	Retained
MS0PKCTLR1	Initialized	Retained
MS0PKSTATR1	Initialized	Retained
MS0PKDATAR1	Initialized	Retained
MS1PKTADR0	Initialized	Retained
MS1PKTSIZER0	Initialized	Retained
MS1PKCTLR0	Initialized	Retained

Abbreviation	Reset*	Module Standby
MS1PKSTATR0	Initialized	Retained
MS1PKDATAR0	Initialized	Retained
MS1PKTADR1	Initialized	Retained
MS1PKTSIZER1	Initialized	Retained
MS1PKCTLR1	Initialized	Retained
MS1PKSTATR1	Initialized	Retained
MS1PKDATAR1	Initialized	Retained
MS2PKTADR0	Initialized	Retained
MS2PKTSIZER0	Initialized	Retained
MS2PKCTLR0	Initialized	Retained
MS2PKSTATR0	Initialized	Retained
MS2PKDATAR0	Initialized	Retained
MS2PKTADR1	Initialized	Retained
MS2PKTSIZER1	Initialized	Retained
MS2PKCTLR1	Initialized	Retained
MS2PKSTATR1	Initialized	Retained
MS2PKDATAR1	Initialized	Retained
HSIPKTADR0	Initialized	Retained
HSIPKTSIZER0	Initialized	Retained
HSIPKCTLR0	Initialized	Retained
HSIPKSTATR0	Initialized	Retained
HSIPKDATAR0	Initialized	Retained
HSIPKTADR1	Initialized	Retained
HSIPKTSIZER1	Initialized	Retained
HSIPKCTLR1	Initialized	Retained
HSIPKSTATR1	Initialized	Retained
HSIPKDATAR1	Initialized	Retained
HSIPKTADR2	Initialized	Retained
HSIPKTSIZER2	Initialized	Retained
HSIPKCTLR2	Initialized	Retained
HSIPKSTATR2	Initialized	Retained
HSIPKDATAR2	Initialized	Retained
HSIPKTADR3	Initialized	Retained
HSIPKTSIZER3	Initialized	Retained
HSIPKCTLR3	Initialized	Retained
HSIPKSTATR3	Initialized	Retained
HSIPKDATAR3	Initialized	Retained
HSIPKTADR4	Initialized	Retained
HSIPKTSIZER4	Initialized	Retained
HSIPKCTLR4	Initialized	Retained
HSIPKSTATR4	Initialized	Retained
HSIPKDATAR4	Initialized	Retained

Abbreviation	Reset*	Module Standby
HSIPKTADR5	Initialized	Retained
HSIPKTSIZER5	Initialized	Retained
HSIPKCTLR5	Initialized	Retained
HSIPKSTATR5	Initialized	Retained
HSIPKDATAR5	Initialized	Retained
HSIPKTADR6	Initialized	Retained
HSIPKTSIZER6	Initialized	Retained
HSIPKCTLR6	Initialized	Retained
HSIPKSTATR6	Initialized	Retained
HSIPKDATAR6	Initialized	Retained
HSIPKTADR7	Initialized	Retained
HSIPKTSIZER7	Initialized	Retained
HSIPKCTLR7	Initialized	Retained
HSIPKSTATR7	Initialized	Retained
HSIPKDATAR7	Initialized	Retained
TS0PKTADR0	Initialized	Retained
TS0PKTSIZER0L	Initialized	Retained
TS0PKCTLR0	Initialized	Retained
TS0PKSTATR0H	Initialized	Retained
TS0PKDATAR0	Initialized	Retained
TS1PKTADR0	Initialized	Retained
TS1PKTSIZER0L	Initialized	Retained
TS1PKCTLR0	Initialized	Retained
TS1PKSTATR0H	Initialized	Retained
TS1PKDATAR0	Initialized	Retained

* For details, refer to section 1-D Overview of reset.

(Bit assignment is common to XXXX (SCIFA0, SCIFA1, SCIFA2, SCIFA3, SCIFA4, SCIFA5, SCIFB, TSIF0, and TSIF1) and YYYY (MSIOF0, MSIOF1, MSIOF2, BBIF0, BBIF1, and HSI).)

10.1.3 XXXX Target Address Register 0(,1)

XXXX Target Address Register 0(,1) specifies the lower 16-bit address of the register to be packed.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TGTADR[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
15 to 0	TGTADR15 to TGTADR0	H'0000	R/W	Specify the lower 16-bit address of the XXXX register to be packed.

10.1.4 XXXX Pack Total Size Register 0L(,1L)

XXXX Pack Total Size Register 0L(,1L) specifies, in bytes, the total size (lower) of data to be transferred in a single DMAC start.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TOTALSIZE[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
15 to 0	TOTALSIZE15 to TOTALSIZE0	H'0000	R/W	Specify, in bytes, the total size of data to be transferred in a single DMAC start.

10.1.5 XXXX Pack Total Size Register 0H(,1H)

XXXX Pack Total Size Register 0H(,1H) specifies, in bytes, the total size (upper) of data to be transferred in a single DMAC start. For transmission, specify the total size with a multiple of 2.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TOTALSIZE[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
15 to 0	TOTALSIZE31 to TOTALSIZE16	H'0000	R/W	Specify, in bytes, the total size of data to be transferred in a single DMAC start.

10.1.6 XXXX Pack Control Register 0(,1)

XXXX Pack Control Register 0(,1) specifies whether to use the DREQPAK function and settings when the function is used.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	FREE RUN	RW SIZE	—	RW SEL	RST	PKEN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
15 to 6	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	FREERUN	0	R/W	Free Run Mode Setting 0: Normal mode 1: Free run mode
4	RWSIZE	0	R/W	Register Access Size Set in Target Address Register 0: Words 1: Bytes

3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2	RWSEL	0	R/W	DMA Transfer Direction Select. Set this bit tailored to the target DMA request. 0: XXXX is the DMA transfer source. 1: XXXX is the DMA transfer destination.
1	RST	0	R/W	Buffer Reset 0: The buffer is not cleared. 1: The buffer is cleared.
0	PKEN	0	R/W	DREQPAK Use/Nonuse Select. This bit is cleared to 0 after data transfer is completed. 0: DREQPAK is not used. DMA transfer is performed in a single byte or word. 1: DREQPAK is used.

10.1.7 XXXX Pack Status Register 0L(,1L)

XXXX Pack Status Register 0L(,1L) indicates the status when the pack function is used.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TRANSDCOUNT[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
15 to 0	TRANSDCOUNT15 to TRANSDCOUNT0	H'0000	R	Indicate, in bytes, the amount of remaining DMA transfer data.

10.1.8 XXXX Pack Status Register 0H(,1H)

XXXX Pack Status Register 0H(,1H) indicates the status when the pack function is used.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ERR FLG	TRANSDCOUNT[30:16]														
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
15 to 0	ERRFLG	0	R/W	Flag indicating that a transfer error occurred. This bit is cleared to 0 when written. If SCIFA0 to SCIFA5, SCIFB, TSIF0, or TSIF1 issues a DMA request, a transfer error occurs even if the value set in the total size register is exceeded. 0: No transfer error occurred. 1: A transfer error occurred.
14 to 0	TRANSDCOUNT30 to TRANSDCOUNT16	H'0000_0000	R	Indicate, in bytes, the amount of remaining DMA transfer data.

10.1.9 XXXX Pack Data Register 0(,1)

XXXX Pack Data Register 0(,1) is accessed by DMAC as the source or destination when the DREQPAK function is used. This register cannot be accessed from the CPU.

Bit:	15	14	13	12	11	11	9	8	7	6	5	4	3	2	1	0
	PACKDATA[15:0]															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
15 to 0	PACKDATA31 to PACKDATA0	Undefined	R/W	Packed data

10.1.10 YYYY Target Address Register 0(,1)

YYYY Target Address Register 0(,1) specifies the lower 16-bit address of the register to be packed.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TGTADR[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 16	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 0	TGTADR15 to TGTADR0	H'0000	R/W	Specify the lower 16-bit address of the YYYY register to be packed.

10.1.11 YYYY Pack Total Size Register 0(,1)

YYYY Pack Total Size Register 0(,1) specifies, in bytes, the total size of data to be transferred in a single DMAC start. For transmission, specify the total size in a multiple of 4.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TOTALSIZE[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TOTALSIZE[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 0	TOTALSIZE31 to TOTALSIZE0	H'0000_0000	R/W	Specify, in bytes, the total size of data to be transferred in a single DMAC start.

10.1.12 YYYY Pack Control Register 0(,1)

YYYY Pack Control Register 0(,1) specifies whether to use the DREQPAK function and settings when the function is used.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	DREQMASK[2:0]			—	—	—	—	—	—	FREE RUN	RWSIZE[1:0]		RW SEL	RST	PKEN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 15	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
14 to 12	DREQMASK	0	R/W	Module DREQ Control Function. This function is valid when the PKEN bit is 0. 0: Normal 1: The next DREQ is masked till DMAACK arrives once. 2: The next DREQ is masked till DMAACK arrives twice. 3: The next DREQ is masked till DMAACK arrives four times. 4: The next DREQ is masked till DMAACK arrives eight times. 7: Unconditional mask
11 to 6	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	FREERUN	0	R/W	Free Run Mode Setting 0: Normal mode 1: Free run mode
4, 3	RWSIZE1 and RWSIZE0	00	R/W	Register Access Size Set in Target Address Register 00: Longwords 01: Words 10: Bytes 11: Prohibited

Bit	Bit Name	Initial Value	R/W	Descriptions
2	RWSEL	0	R/W	DMA Transfer Direction Select. Set this bit tailored to the target DMA request. 0: YYYY is the DMA transfer source. 1: YYYY is the DMA transfer destination.
1	RST	0	R/W	Buffer Reset 0: The buffer is not cleared. 1: The buffer is cleared.
0	PKEN	0	R/W	DREQPAK Use/Nonuse Select. This bit is cleared to 0 after data transfer is completed. 0: DREQPAK is not used. DMA transfer is performed in a single byte or word. 1: DREQPAK is used.

10.1.13 YYYY Pack Status Register 0(,1)

YYYY Pack Status Register 0(,1) indicates the status when the pack function is used.

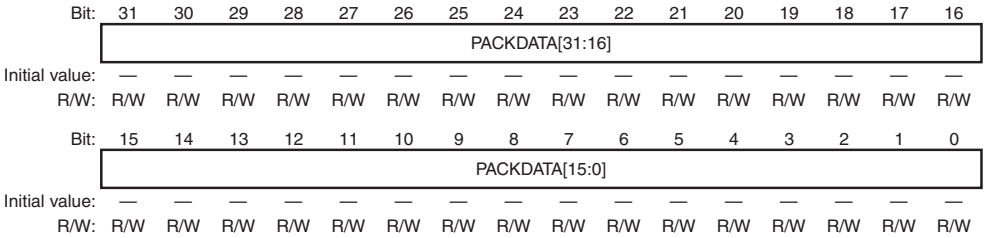
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ERR FLG	TRANSDCOUNT[30:16]														
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TRANSDCOUNT[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31	ERRFLG	0	R/W	Flag indicating that a transfer error occurred. This bit is cleared to 0 when write-accessed. If HSI, MSIOF0/1, or BBIF1/2 issues a DMA request, a transfer error occurs even if the value set in the total size register is exceeded. 0: No transfer error occurred. 1: A transfer error occurred.
30 to 0	TRANSDCOUNT30 to TRANSDCOUNT0	H'0000_0000	R	Indicate, in bytes, the amount of remaining DMA transfer data.

10.1.14 YYYY Pack Data Register 0(,1)

YYYY Pack Data Register 0(,1) is accessed by DMAC as the source or destination when the DREQPAK function is used. This register cannot be accessed from the CPU.



Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 0	PACKDATA31 to PACKDATA0	Undefined	R/W	Packed data

10.1.15 Principles of Operation

To perform DMA transfer between a peripheral module and memory by using DREQPAK, use the following procedure:

1. Setting DMAC
2. Setting DREQPAK
3. Setting the peripheral module
4. <Starting DMA transfer>
5. <Ending DMA transfer>
6. Setting the peripheral module
7. Setting DREQPAK
8. Setting DMAC

The following describes the above procedure by transmission and reception.

(1) Transfer from the peripheral module to memory (reception)

1. Setting DMAC

Set necessary settings in DMAC. DMAC setting when DREQPAK is used differs from when DREQPAK is not used in the following points:

- Set the address of the DREQPAK pack data register in the source address register.
- Specify 32 bytes as the transfer size of the channel control register.
- If 32 bytes is specified as the transfer size, the total transfer data amount (a number represented by n times a multiple of 32) is set in the transfer count register. If the amount of data you want to transfer does not become a multiple of 32, set the transfer amount rounded up to a multiple of 32 as the value to be set in the transfer count register. For example, if you want to use 66-byte transfer, set 3 as the transfer count.

Set the DMA Enable (DE) bit of DMAC to 1 to start data transfer.

2. Setting DREQPAK

Make the following settings:

- Set the register to store the source data of the peripheral module as the target address register.
- Set, in bytes, the amount of data you want to transfer to the pack total size register. You need not round up the amount of data to a multiple of 32.
- Set reception in the pack control register. Set the access size of the register to store source data as the access size. Set the RWSEL bit to 0 and the RST and PKEN bits to 1.

3. Setting the peripheral module

Enable reception DMA transfer request output.

4. <Starting DMA transfer>
5. <Ending DMA transfer>
6. Setting the peripheral module

Disable reception DMA transfer request output.

7. Setting DREQPAK

Check error occurrence, etc., in the status register as required.

8. Setting DMAC

Clear the interrupt mask and status as required.

(2) Transfer from memory to peripheral module (transmission)

1. Setting DMAC

Set necessary settings in DMAC. DMAC setting when DREQPAK is used differs from when DREQPAK is not used in the following points:

- Set the address of the DREQPAK pack data register in the destination address register.
- Specify 32 bytes as the transfer size of the channel control register.
- If 32 bytes is specified as the transfer size, the total transfer data amount (a number represented by n times a multiple of 32) is set in the transfer count register. If the amount of data you want to transfer does not become a multiple of 32, set the transfer amount rounded up to a multiple of 32 as the value to be set in the transfer count register. For example, if you want to use 66-byte transfer, set 3 as the transfer count.

Set the DMA Enable (DE) bit of DMAC to 1 to start data transfer.

2. Setting DREQPAK

Make the following settings:

- Set the register to store peripheral module data as the target address register.
- Set, in bytes, the amount of data you want to transfer to the pack total size register. You need not round up the amount of data to a multiple of 32.
- Set transmission in the pack control register. Set the access size of the register to store source data as the access size. Set the RWSEL bit to 1 and the RST and PKEN bits to 1.

3. Setting the peripheral module

Enable transmission DMA transfer request output.

4. <Starting DMA transfer>
5. <Ending DMA transfer>
6. Setting the peripheral module

Disable transmission DMA transfer request output.

7. Setting DREQPAK

Check error occurrence, etc., in the status register as required.

8. Setting DMAC

Clear the interrupt mask and status as required.

10.1.16 About free run mode

Setting the free run bit (bit 5) of the pack control register to 1 continues operation without reference to the values set in the pack total size register and enables data transfer beyond the number of bytes set in the pack total size register. This mode assumes use with DMAC repeat mode.

In free run mode, the transfer size is a multiple of 32 bytes. Factions less than a multiple of 32 are not processed.

When using free run mode, set 32(H'20) in the pack total size register.

10.1.17 About the module DREQ control function

The module DREQ control function is a support function that provides direct multibyte access between DMAC modules without DREQPAK. Multibyte transfer that uses this function can be used by the following modules that output DMAREQ and can control the FIFO threshold:

MSIOF0, MSIOF1, MSIOF2, BBIF1, BBIF2, TSIF

Example of use:

To perform 32-byte transfer via BBIF1:

1. Set 32 bytes as the DMAC transfer size.
2. Set the DREQMASK bits of DREQPAK to 8 (= 32 ÷ 4 (FIFO register size of BBIF)).

3. Set the FIFO water mark of the BBIF1 FIFO control register to "empty" or "valid eight-stage data" (x4 = 32 bytes. For transmission, set TFWM to 101. For reception, set RFWM to 010).

Note: When the DREQMASK bits (bits 14 to 12) are set to 7 (unconditional mask)

When data transfer is completed, DREQPAK automatically returns to normal mode (the PKEN bit of the pack control register is 0). If DMAC operation is continued in repeat mode and a finite size is set in DREQPAK, the module side may issue a DMA request after the data transfer of the size set in DREQPAK is completed. In this case, the DMA transfer request will directly arrive at DMAC because DREQPAK setting returns to nonuse. Setting the unconditional mask here enables data transfer to be stopped because the DMA transfer request is blocked after data transfer by DREQPAK is completed. Unconditional mask setting can be used in the following modules:

MSIOF0, MSIOF1, MSIOF2, BBIF1, BBIF2, SIU, TSIF

10.1.18 Notes on specifications

In some modules (e.g., SCIF) that do not manage the DMA transfer count on the module side, DMA requests are always asserted without reference to operation on the DMAC side as long as DMA request output setting is enabled. In such modules, the error flag of the pack status register is set to 1 even if data transfer is successfully completed. For this reason, ignore the error.

10.2 DDM (Descriptor DMAC)

The DDM is a module that reconfigures the DMAC. The OS on the main CPU is highly sophisticated and the overhead from interrupt notification to reconfiguration increases. To solve this problem, the DDM reconfigures the DMAC in a fast response time on behalf of the CPU.

Figure 10.3 shows the relationship diagram of DDM DMAC connection.

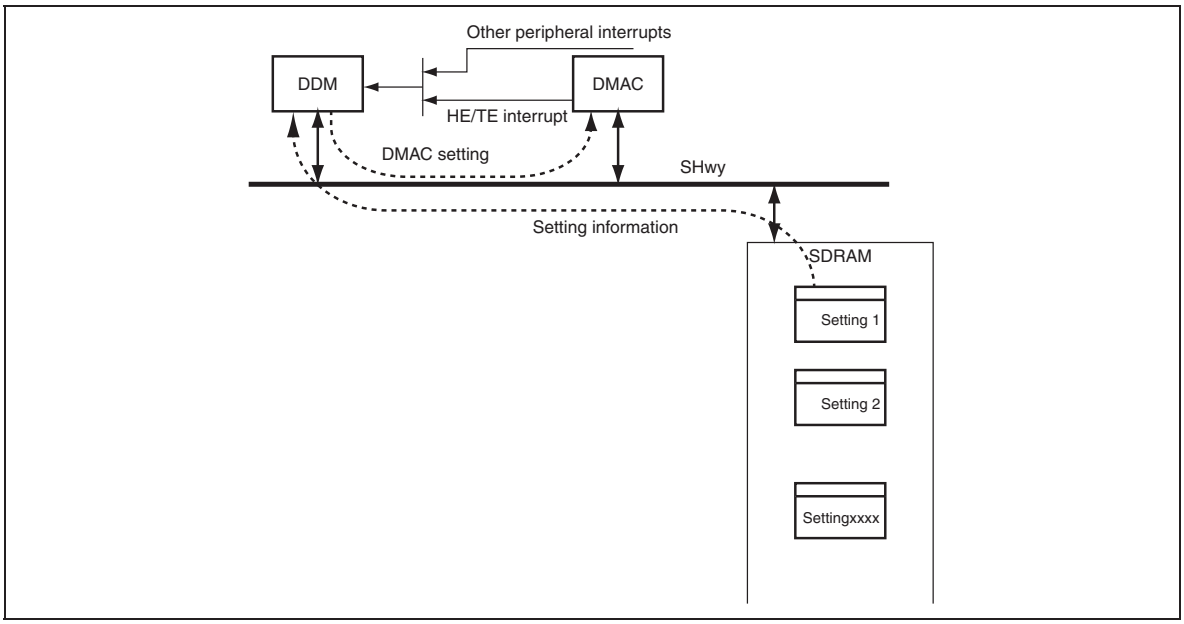


Figure 10.3 Relationship Diagram of DDM Connection

10.2.1 DDM Register Descriptions

Table 10.3 shows the DDM register configuration. Table 10.4 shows the register states in each operating mode.

Table 10.3 DDM Control Registers

Name	Register Abbreviation	R/W	Initial Value	Address	Access Size (Bits)
DDM interrupt source mask register	DDIREQMSK	R/W	H'00000000	H'FE080008	32
DDM interrupt source register	DDIREQSTA	R	H'00000000	H'FE08000C	32
DDM start source polarity reversal register 1	DDINTINV1	R/W	H'00000000	H'FE080010	32
DDM start source polarity reversal register 2	DDINTINV2	R/W	H'00000000	H'FE080014	32
DDM CH1 start source mask register 1	DDINTMSK11	R/W	H'00000000	H'FE080030	32
DDM CH1 start source mask register 2	DDINTMSK12	R/W	H'00000000	H'FE080034	32
DDM CH1 start source mask register 3	DDINTMSK13	R/W	H'00000000	H'FE080038	32
DDM CH1 start source mask register 4	DDINTMSK14	R/W	H'00000000	H'FE08003C	32
DDM CH1 start source mask register 5	DDINTMSK15	R/W	H'00000000	H'FE080040	32
DDM CH1 descriptor pointer	DDPTR1	R/W	H'00000000	H'FE080050	32
DDM CH1 control register	DDCTRL1	R/W	H'80000000	H'FE080054	32
DDM CH2 start source mask register 1	DDINTMSK21	R/W	H'00000000	H'FE080060	32
DDM CH2 start source mask register 2	DDINTMSK22	R/W	H'00000000	H'FE080064	32
DDM CH2 start source mask register 3	DDINTMSK23	R/W	H'00000000	H'FE080068	32
DDM CH2 start source mask register 4	DDINTMSK24	R/W	H'00000000	H'FE08006C	32
DDM CH2 start source mask register 5	DDINTMSK25	R/W	H'00000000	H'FE080070	32
DDM CH2 descriptor pointer	DDPTR2	R/W	H'00000000	H'FE080080	32
DDM CH2 control register	DDCTRL2	R/W	H'80000000	H'FE080084	32
DDM CH3 start source mask register 1	DDINTMSK31	R/W	H'00000000	H'FE080090	32
DDM CH3 start source mask register 2	DDINTMSK32	R/W	H'00000000	H'FE080094	32
DDM CH3 start source mask register 3	DDINTMSK33	R/W	H'00000000	H'FE080098	32
DDM CH3 start source mask register 4	DDINTMSK34	R/W	H'00000000	H'FE08009C	32
DDM CH3 start source mask register 5	DDINTMSK35	R/W	H'00000000	H'FE0800A0	32
DDM CH3 descriptor pointer	DDPTR3	R/W	H'00000000	H'FE0800B0	32
DDM CH3 control register	DDCTRL3	R/W	H'80000000	H'FE0800B4	32
DDM CH4 start source mask register 1	DDINTMSK41	R/W	H'00000000	H'FE0800C0	32
DDM CH4 start source mask register 2	DDINTMSK42	R/W	H'00000000	H'FE0800C4	32
DDM CH4 start source mask register 3	DDINTMSK43	R/W	H'00000000	H'FE0800C8	32
DDM CH4 start source mask register 4	DDINTMSK44	R/W	H'00000000	H'FE0800CC	32
DDM CH4 start source mask register 5	DDINTMSK45	R/W	H'00000000	H'FE0800D0	32
DDM CH4 descriptor pointer	DDPTR4	R/W	H'00000000	H'FE0800E0	32
DDM CH4 control register	DDCTRL4	R/W	H'80000000	H'FE0800E4	32
DDM CH5 start source mask register 1	DDINTMSK51	R/W	H'00000000	H'FE0800F0	32
DDM CH5 start source mask register 2	DDINTMSK52	R/W	H'00000000	H'FE0800F4	32
DDM CH5 start source mask register 3	DDINTMSK53	R/W	H'00000000	H'FE0800F8	32

DDM CH5 start source mask register 4	DDINTMSK54	R/W	H'00000000	H'FE0800FC	32
DDM CH5 start source mask register 5	DDINTMSK55	R/W	H'00000000	H'FE080100	32
DDM CH5 descriptor pointer	DDPTR5	R/W	H'00000000	H'FE080110	32
DDM CH5 control register	DDCTRL5	R/W	H'80000000	H'FE080114	32
DDM CH6 start source mask register 1	DDINTMSK61	R/W	H'00000000	H'FE080120	32
DDM CH6 start source mask register 2	DDINTMSK62	R/W	H'00000000	H'FE080124	32
DDM CH6 start source mask register 3	DDINTMSK63	R/W	H'00000000	H'FE080128	32
DDM CH6 start source mask register 4	DDINTMSK64	R/W	H'00000000	H'FE08012C	32
DDM CH6 start source mask register 5	DDINTMSK65	R/W	H'00000000	H'FE080130	32
DDM CH6 descriptor pointer	DDPTR6	R/W	H'00000000	H'FE080140	32
DDM CH6 control register	DDCTRL6	R/W	H'80000000	H'FE080144	32
DDM CH7 start source mask register 1	DDINTMSK71	R/W	H'00000000	H'FE080150	32
DDM CH7 start source mask register 2	DDINTMSK72	R/W	H'00000000	H'FE080154	32
DDM CH7 start source mask register 3	DDINTMSK73	R/W	H'00000000	H'FE080158	32
DDM CH7 start source mask register 4	DDINTMSK74	R/W	H'00000000	H'FE08015C	32
DDM CH7 start source mask register 5	DDINTMSK75	R/W	H'00000000	H'FE080160	32
DDM CH7 descriptor pointer	DDPTR7	R/W	H'00000000	H'FE080170	32
DDM CH7 control register	DDCTRL7	R/W	H'80000000	H'FE080174	32
DDM CH8 start source mask register 1	DDINTMSK81	R/W	H'00000000	H'FE080180	32
DDM CH8 start source mask register 2	DDINTMSK82	R/W	H'00000000	H'FE080184	32
DDM CH8 start source mask register 3	DDINTMSK83	R/W	H'00000000	H'FE080188	32
DDM CH8 start source mask register 4	DDINTMSK84	R/W	H'00000000	H'FE08018C	32
DDM CH8 start source mask register 5	DDINTMSK85	R/W	H'00000000	H'FE080190	32
DDM CH8 descriptor pointer	DDPTR8	R/W	H'00000000	H'FE0801A0	32
DDM CH8 control register	DDCTRL8	R/W	H'80000000	H'FE0801A4	32

Table 10.4 Register States in Each Operating Mode

Abbreviation	Reset*	Module Standby
DDIREQMSK	Initialized	Retained
DDIREQSTA	Initialized	Retained
DDINTINV1	Initialized	Retained
DDINTINV2	Initialized	Retained
DDINTMSK11	Initialized	Retained
DDINTMSK12	Initialized	Retained
DDINTMSK13	Initialized	Retained
DDINTMSK14	Initialized	Retained
DDINTMSK15	Initialized	Retained
DDPTR1	Initialized	Retained
DDCTRL1	Initialized	Retained
DDINTMSK21	Initialized	Retained
DDINTMSK22	Initialized	Retained
DDINTMSK23	Initialized	Retained
DDINTMSK24	Initialized	Retained

Abbreviation	Reset*	Module Standby
DDINTMSK25	Initialized	Retained
DDPTR2	Initialized	Retained
DDCTRL2	Initialized	Retained
DDINTMSK31	Initialized	Retained
DDINTMSK32	Initialized	Retained
DDINTMSK33	Initialized	Retained
DDINTMSK34	Initialized	Retained
DDINTMSK35	Initialized	Retained
DDPTR3	Initialized	Retained
DDCTRL3	Initialized	Retained
DDINTMSK41	Initialized	Retained
DDINTMSK42	Initialized	Retained
DDINTMSK43	Initialized	Retained
DDINTMSK44	Initialized	Retained
DDINTMSK45	Initialized	Retained
DDPTR4	Initialized	Retained
DDCTRL4	Initialized	Retained
DDINTMSK51	Initialized	Retained
DDINTMSK52	Initialized	Retained
DDINTMSK53	Initialized	Retained
DDINTMSK54	Initialized	Retained
DDINTMSK55	Initialized	Retained
DDPTR5	Initialized	Retained
DDCTRL5	Initialized	Retained
DDINTMSK61	Initialized	Retained
DDINTMSK62	Initialized	Retained
DDINTMSK63	Initialized	Retained
DDINTMSK64	Initialized	Retained
DDINTMSK65	Initialized	Retained
DDPTR6	Initialized	Retained
DDCTRL6	Initialized	Retained
DDINTMSK71	Initialized	Retained
DDINTMSK72	Initialized	Retained
DDINTMSK73	Initialized	Retained
DDINTMSK74	Initialized	Retained
DDINTMSK75	Initialized	Retained
DDPTR7	Initialized	Retained
DDCTRL7	Initialized	Retained
DDINTMSK81	Initialized	Retained
DDINTMSK82	Initialized	Retained
DDINTMSK83	Initialized	Retained
DDINTMSK84	Initialized	Retained

Abbreviation	Reset*	Module Standby
DDINTMSK85	Initialized	Retained
DDPTR8	Initialized	Retained
DDCTRL8	Initialized	Retained

* For details, refer to section 1-D Overview of reset.

10.2.2 DDM Interrupt Source Mask Register

The DDM Interrupt Source Mask Register enables and disables interrupt sources from the DDM.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ERR8	END8	ERR7	END7	ERR6	END6	ERR5	END5	ERR4	END4	ERR3	END3	ERR2	END2	ERR1	END1
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 16	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	ERR8	0	R/W	Interrupt Output by CH8 DDM_ERR 0: Disables interrupt output. 1: Enables interrupt output.
14	END8	0	R/W	Interrupt Output by CH8 DDM_END 0: Disables interrupt output. 1: Enables interrupt output.
13	ERR7	0	R/W	Interrupt Output by CH7 DDM_ERR 0: Disables interrupt output. 1: Enables interrupt output.
12	END7	0	R/W	Interrupt Output by CH7 DDM_END 0: Disables interrupt output. 1: Enables interrupt output.
11	ERR6	0	R/W	Interrupt Output by CH6 DDM_ERR 0: Disables interrupt output. 1: Enables interrupt output.
10	END6	0	R/W	Interrupt Output by CH6 DDM_END 0: Disables interrupt output. 1: Enables interrupt output.
9	ERR5	0	R/W	Interrupt Output by CH5 DDM_ERR 0: Disables interrupt output. 1: Enables interrupt output.
8	END5	0	R/W	Interrupt Output by CH5 DDM_END 0: Disables interrupt output. 1: Enables interrupt output.

Bit	Bit Name	Initial Value	R/W	Descriptions
7	ERR4	0	R/W	Interrupt Output by CH4 DDM_ERR 0: Disables interrupt output. 1: Enables interrupt output.
6	END4	0	R/W	Interrupt Output by CH4 DDM_END 0: Disables interrupt output. 1: Enables interrupt output.
5	ERR3	0	R/W	Interrupt Output by CH3 DDM_ERR 0: Disables interrupt output. 1: Enables interrupt output.
4	END3	0	R/W	Interrupt Output by CH3 DDM_END 0: Disables interrupt output. 1: Enables interrupt output.
3	ERR2	0	R/W	Interrupt Output by CH2 DDM_ERR 0: Disables interrupt output. 1: Enables interrupt output.
2	END2	0	R/W	Interrupt Output by CH2 DDM_END 0: Disables interrupt output. 1: Enables interrupt output.
1	ERR1	0	R/W	Interrupt Output by CH1 DDM_ERR 0: Disables interrupt output. 1: Enables interrupt output.
0	END1	0	R/W	Interrupt Output by CH1 DDM_END 0: Disables interrupt output. 1: Enables interrupt output.

10.2.3 DDM Interrupt Source Register

The DDM Interrupt Source Register indicates the currently output interrupt source. This register is read-only. You cannot clear the interrupt source in this register. Clear the interrupt source by using the control register of each channel.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ERR8	END8	ERR7	END7	ERR6	END6	ERR5	END5	ERR4	END4	ERR3	END3	ERR2	END2	ERR1	END1
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 16	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	ERR8	0	R	Interrupt output by CH8 DDM_ERR 0: The interrupt is not output. 1: The interrupt is output.
14	END8	0	R	Interrupt output by CH8 DDM_END 0: The interrupt is not output. 1: The interrupt is output.
13	ERR7	0	R	Interrupt output by CH7 DDM_ERR 0: The interrupt is not output. 1: The interrupt is output.
12	END7	0	R	Interrupt output by CH7 DDM_END 0: The interrupt is not output. 1: The interrupt is output.
11	ERR6	0	R	Interrupt output by CH6 DDM_ERR 0: The interrupt is not output. 1: The interrupt is output.
10	END6	0	R	Interrupt output by CH6 DDM_END 0: The interrupt is not output. 1: The interrupt is output.
9	ERR5	0	R	Interrupt output by CH5 DDM_ERR 0: The interrupt is not output. 1: The interrupt is output.
8	END5	0	R	Interrupt output by CH5 DDM_END 0: The interrupt is not output. 1: The interrupt is output.
7	ERR4	0	R	Interrupt output by CH4 DDM_ERR 0: The interrupt is not output. 1: The interrupt is output.

Bit	Bit Name	Initial Value	R/W	Descriptions
6	END4	0	R	Interrupt output by CH4 DDM_END 0: The interrupt is not output. 1: The interrupt is output.
5	ERR3	0	R	Interrupt output by CH3 DDM_ERR 0: The interrupt is not output. 1: The interrupt is output.
4	END3	0	R	Interrupt output by CH3 DDM_END 0: The interrupt is not output. 1: The interrupt is output.
3	ERR2	0	R	Interrupt output by CH2 DDM_ERR 0: The interrupt is not output. 1: The interrupt is output.
2	END2	0	R	Interrupt output by CH2 DDM_END 0: The interrupt is not output. 1: The interrupt is output.
1	ERR1	0	R	Interrupt output by CH1 DDM_ERR 0: The interrupt is not output. 1: The interrupt is output.
0	END1	0	R	Interrupt output by CH1 DDM_END 0: The interrupt is not output. 1: The interrupt is output.

10.2.4 DDM Start Source Polarity Reversal Registers 1 and 2

DDM Start Source Polarity Reversal Registers 1 and 2 reverse the start source input polarity to the DDM.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DDINTINV[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DDINTINV[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 0	DDINTINV31 to DDINTINV0	H'0000_0000	R/W	Reverse the DDM start source polarity.

DDM CHn Start Source Mask Registers 1 and 2

DDM CHn Start Source Mask Registers 1 and 2 mask DDM start sources.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DDINTMSK[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DDINTMSK[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 0	DDINTMSK31 to DDINTMSK0	H'0000_0000	R/W	Start Source Mask 0: Does not mask the start source. 1: Masks the start source.

The current source assignment is as follows:

Bit Name	Bit	Assigned Start Source
DDINTMSK5	31 to 4	Reserved
	3	RTDMAC2 CH5 CHCR HE bit
	2	RTDMAC2 CH4 CHCR HE bit
	1	RTDMAC2 CH3 CHCR HE bit
	0	RTDMAC2 CH2 CHCR HE bit
DDINTMSK4	31	RTDMAC2 CH1 CHCR HE bit
	30	RTDMAC2 CH0 CHCR HE bit
	29	RTDMAC2 CH5 CHCR TE bit
	28	RTDMAC2 CH4 CHCR TE bit
	27	RTDMAC2 CH3 CHCR TE bit
	26	RTDMAC2 CH2 CHCR TE bit
	25	RTDMAC2 CH1 CHCR TE bit
	24	RTDMAC2 CH0 CHCR TE bit
	23 to 0	Reserved
DDINTMSK3	31 to 0	Reserved
DDINTMSK2	31 to 16	Reserved
	15	RTDMAC CH5 CHCR HE bit
	14	RTDMAC CH4 CHCR HE bit
	13	RTDMAC CH3 CHCR HE bit
	12	RTDMAC CH2 CHCR HE bit
	11	RTDMAC CH1 CHCR HE bit
	10	RTDMAC CH0 CHCR HE bit
	9	DMAC1 CH5 CHCR HE bit
	8	DMAC1 CH4 CHCR HE bit
	7	DMAC1 CH3 CHCR HE bit
	6	DMAC1 CH2 CHCR HE bit
	5	DMAC1 CH1 CHCR HE bit
	4	DMAC1 CH0 CHCR HE bit
	3	DMAC2 CH5 CHCR HE bit

Bit Name	Bit	Assigned Start Source
	2	DMAC2 CH4 CHCR HE bit
	1	DMAC2 CH3 CHCR HE bit
	0	DMAC2 CH2 CHCR HE bit
DDINTMSK1	31	DMAC2 CH1 CHCR HE bit
	30	DMAC2 CH0 CHCR HE bit
	29	DMAC3 CH5 CHCR HE bit
	28	DMAC3 CH4 CHCR HE bit
	27	DMAC3 CH3 CHCR HE bit
	26	DMAC3 CH2 CHCR HE bit
	25	DMAC3 CH1 CHCR HE bit
	24	DMAC3 CH0 CHCR HE bit
	23	RTDMAC CH5 CHCR TE bit
	22	RTDMAC CH4 CHCR TE bit
	21	RTDMAC CH3 CHCR TE bit
	20	RTDMAC CH2 CHCR TE bit
	19	RTDMAC CH1 CHCR TE bit
	18	RTDMAC CH0 CHCR TE bit
	17	DMAC1 CH5 CHCR TE bit
	16	DMAC1 CH4 CHCR TE bit
	15	DMAC1 CH3 CHCR TE bit
	14	DMAC1 CH2 CHCR TE bit
	13	DMAC1 CH1 CHCR TE bit
	12	DMAC1 CH0 CHCR TE bit
	11	DMAC2 CH5 CHCR TE bit
	10	DMAC2 CH4 CHCR TE bit
	9	DMAC2 CH3 CHCR TE bit
	8	DMAC2 CH2 CHCR TE bit
	7	DMAC2 CH1 CHCR TE bit
	6	DMAC2 CH0 CHCR TE bit
	5	DMAC3 CH5 CHCR TE bit
	4	DMAC3 CH4 CHCR TE bit
	3	DMAC3 CH3 CHCR TE bit
	2	DMAC3 CH2 CHCR TE bit
	1	DMAC3 CH1 CHCR TE bit
	0	DMAC3 CH0 CHCR TE bit

10.2.5 DDM CHn Descriptor Pointer

The DDM CHn Descriptor Pointer indicates the start address of setting code allocated onto memory.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DDPTR[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DDPTR[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 0	DDPTR31 to DDPTR0	H'0000_0000	R/W	Descriptor pointer.

10.2.6 DDM CHn Control Register

The DDM CHn Control Register controls start and stop of DDM.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PRI[3:0]				—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	STOP	KICK	DDM_ERR	DDM_END	DDE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 28	PRI3 to PRI0	H'0	R/W	PRI value on the SHwy bus.
27 to 5	—	H'000_000	R	Reserved
4	STOP	0	R/W	Forced Stop Function 0: Does not perform forced stop. 1: Performs forced stop.
3	KICK	0	R/W	Forced Start Function without Start Source 0: Does not perform forced start. 1: Performs forced start. This bit is automatically cleared to 0 after 1 is written.
2	DDM_ERR	0	R	Error Occurrence. The error is cleared by setting the DDE bit to 0. 0: No error occurred. 1: An error occurred.
1	DDM_END	0	R	DDM End. DDM end is cleared by setting the DDE bit to 0. 0: The DDM did not end. 1: The DDM ended.

Bit	Bit Name	Initial Value	R/W	Descriptions
0	DDE	0	R/W	Start Enable 0: Does not enable DDM start. 1: Enables DDM start according to the start source.

10.2.7 Principles of Operation

To reconfigure the DMAC by using the DDM, use the following procedure:

1. Describing setting codes
2. Starting and ending the DDM

(1) Describing setting codes

(a) Data structure

A setting code is fixed-length data consisting of four longwords.

Setting code data consists of the following fields, starting from the beginning:

Field	bit
Operation field	32bit
Address field	32bit
Data field	32bit
Bit mask field	32bit

Note: Arrange a setting code in 16 byte boundary.

The following describes the operation field.

(b) Operation field

The structure of the operation field is as follows:

Bit	Bit Name	Descriptions
31 to 16	HEADER	Indicates DDM setting data. H'DDDD: Normal DDM setting code Usually, set this value. H'EEEE: DDM end code Set this value when ending the channel without starting the DDM the next time. If the HEADER bits have other values, an error occurs. The channel of the DDM stops immediately.
15 to 8	—	Reserved
7 to 4	SIZE	Specify the data access size to be set. 0000: Bytes 0001: Words 0010: Longwords
3	ENDFLG	End Flag of Setting Processing Based on This Start Source 0: Continuation 1: Setting end. The DDM waits for the next start source.

Bit	Bit Name	Descriptions
2 to 0	OPC	Operation Code 000: read (cmp/eq) (read) 001: write (write) 010: rmodw (read modify write) 011: add (addition) 100: jmp/eq (branch)

The address field, data field, and bit mask field each consist of 32 bits. The data field and bit mask field use the LSB side for word- and byte-size access.

(c) read (cmp/eq)

The read (cmp/eq) code reads the target address and compares the address with the expected values written in the data field and bit mask field.

When the comparison result becomes true, the TFLG internal variable is set to 1. TFLG is cleared to 0 when jmp/eq is executed or operation with ENDFLG is performed.

Description example:

The read (cmp/eq) code in this example reads the H'FE00802C address in longwords and checks if bit 1 is set to 1.

H'DDDD0020
H'FE00802C
H'00000002
H'00000002

(d) write

The write code writes data to the target address.

Description example:

The write code in this example accesses the H'FE00802C address in longwords and writes H'00105400.

H'DDDD0021
H'FE00802C
H'00105400
H'FFFFFFFF (don't care)

(e) rmodw

The rmodw code reads the target address and performs modify-write according to the values of the bit mask field.

Description example:

The rmodw code in this example reads the H'FE00802C address in longwords and applies H'54 modify-write to bits 11 to 4.

H'DDDD0022
H'FE00802C
H'00000540
H'00000FF0

(f) add

The add code reads the target address and performs add-modify-write according to the values of the bit mask field.

Description example:

The add code in this example reads the H'FE00802C address in longwords and applies H'200 add-modify-write to bits 11 to 0.

H'DDDD0023
H'FE00802C
H'00000200
H'00000FFF

Use 0 as the addition data corresponding to the area where the bit mask is 0.

(g) jmp/eq

If TFLG is set to 1 by the cmp/eq code, jmp/eq changes the descriptor pointer to the values of the data field. Descriptor pointer change by jmp/eq is not reflected in execution based on the next start source. Changing the descriptor pointer for the next start requires that the CHn descriptor pointer be reconfigured.

Description example:

The jmp/eq code in this example changes the descriptor pointer when TFLG is 1 to H' E558000E.

H'DDDD0024
H'00000000 (don't care)
H'E558000E
H'00000000 (don't care)

(h) Settings description order

Describe settings in the following order:

(1) Clearing the start source (source output side, not the DDM start source mask register)
(2) Changing the DDM source mask setting as required
(3) Reconfiguring registers such as DMAC
(4) Reconfiguring the next descriptor pointer

If several start sources are set, the last write may be unable to catch up with the next start. In such a case, end next descriptor pointer setting in (4) in read after write (do not end it in write).

(i) Example of setting DMAC restart

Use DDM CH1. The following shows an example of describing setting codes for reconfiguration when the TE bit of the DMAC1 CH0 channel control register is HI.

//TE bit read
H'DDDD0020
H'FE00802C
H'00000002
H'00000002
//TE bit clear
H'DDDD0021

H'FE00802C
H'00105400
H'FFFFFFFF
//SAR setting
H'DDDD0021
H'FE008020
H'58000000
H'FFFFFFFF
//DAR setting
H'DDDD0021
H'FE008024
H'00000000
H'FFFFFFFF
//TCR setting
H'DDDD0021
H'FE008028
H'00000010
H'FFFFFFFF
//DE bit write. DMA start
H'DDDD0021
H'FE00802C
H'00105401
H'FFFFFFFF
//Next descriptor pointer write. Setting end by this start.
H'DDDD0029
H'FE080050
H'580002D0
H'FFFFFFFF

(2) Start and end

(a) Starting the DDM

Make necessary settings in the DDM.

- Enabling interrupt output as required
- Setting a DDM start source
- Setting a descriptor pointer

After setting the above, set the DDM Enable bit of the DDM control register to 1 to enable DDM start.

Setting example:
Enable the interrupt by DDM CH1 end.
Address: H'FE080008 Write data: H'00000001
Enable DDM CH1 start when the DMAC1 TE bit is changed.
Address: H'FE080030 Write data: H'00001000
Set the DDM CH1 descriptor pointer to H'58000210.
Address: H'FE080050 Write data: H'58000210

Enable DDM CH1 start.

Address: H'FE080054 Write data: H'00000001

Set the KICK bit to forced start after setting the DDM Enable bit to 1. Do not set these bits at the same time.

(b) Ending the DDM

When the DDM ends, the DDM_END bit is set to 1. DDM end is cleared by setting the DDE bit to 0. To restart the DDM, you must clear the DDM_END bit by setting the DDE bit to 0.

Procedure for stopping the DDM by the STOP bit

Set the STOP bit to 1. Keep the DDE bit at 1.

Check that the DDM_END bit is 1.

Set the DDE bit to 0.

Section 11 Clock Pulse Generator (CPGA)

This LSI has a clock pulse generator (CPGA).

The CPGA generates the system domain clocks in the AP block: the system CPU clock (Zϕ and ZXϕ), system CPU debug trace clock (ZTϕ), SGX clock (ZGϕ), and high-speed peripheral clock (HPϕ).

The CPGA also generates the realtime domain clocks in the AP block: the realtime CPU clock (Iϕ), media clock (Bϕ), VPU clock (M1ϕ), CSI2 RX clock (CSIRϕ), ISP byte clock (ISPBϕ), and high-speed peripheral clock (HPϕ).

In addition, the CPGA generates the common domain clocks: the SHwy clock (Sϕ, ZSϕ), common peripheral clock (CPϕ), SDRAM clock for SBSC1 (ZB3ϕ), DDRP clock (DDRPϕ), and bus clock (ZBϕ).

The CPGA consists of an oscillator, PLL circuits C0, C1 and C2, and dividers.

11.1 Features

- Various clocks generated for LSI internal operation

  In the realtime domain of the AP block, the realtime CPU clock (Iϕ) used by the realtime CPU (CPU, DSP, cache, and TLB), media clock (Bϕ) used by the RTDMAC and media-related modules, VPU clock (M1ϕ) used by VPU, CSI2 RX clock (CSIRϕ) used by CSIR2 RX, ISP byte clock (ISPBϕ) used by ISP, and high-speed peripheral clock (HPϕ) used by the high-speed peripheral modules can be generated independently.

  The following clocks can be generated independently: (1) those in the system domain of the AP block: the system CPU clock (Zϕ and ZXϕ) used by the system CPU (CPU, cache, and TLB), the system CPU debug trace clock (ZTRϕ) and system CPU debug trace bus clock (ZTϕ), used by the system CPU for debugging, SGX clock (ZGϕ) used by the SGX540, and the high-speed peripheral clock (HPϕ) used by the high-speed peripheral modules; and (2) those in the common block: the common peripheral clock (CPϕ) used by the common peripheral modules, the SHwy clock (ZSϕ) used by the SHwy, the SDRAM clock for SBSC1 (ZB3ϕ) used by the SBSC1, the DLL clock (DDRPϕ) for SDRAM interface PHI and the bus clock (ZBϕ) used by the external bus interface.

  As other generated clocks : Video clock 1 (VCK1ϕ), Video clock 2 (VCK2ϕ), Video clock 3 (VCK3ϕ), FMSI input port clock (FMSIϕ), FMSO output port clock (FMSOϕ), FSIA clock (FSIAϕ), FSIB clock (FSIBϕ), SUB clock (SUBϕ), SUP clock (SUPϕ), VOU clock (VOUϕ), HDMI clock (HSMIϕ), DSI TX Link clock (DSITϕ), DSI0 TX PHY clock (DSIPϕ), DSI1 TX PHY clock (DSI1Pϕ)

- Frequency change function

  The frequencies of the system CPU clock can be changed independently using PLL circuit C0 or dividers in the CPG. Other frequencies of the realtime CPU clock, RT-SHway clock, media clock, VPU clock, ISP clock, CSI2 RX clock, CPU debug trace bus clock, CPU debug trace clock, SGX clock, SHwy clock, bus clock, SDRAM clock for SBSC1, DLL clock for SDRAM interface PHI , high-speed peripheral clock, and common peripheral clock can be changed independently using PLL circuit C1 or dividers in the CPG. Frequencies are changed by software using the frequency control register A (FRQCRA), frequency control register B (FRQCRB), frequency control register (FRQCRC) or frequency control register D (FRQCRD) settings.
- Power-down mode control

  The clock can be stopped for sleep mode, and specific modules can be stopped using the power cutoff mode, core standby mode, and module standby function.
- Music player mode

  Power supply on/off of the A4S4 area, PLLC0, PLLC1, and source oscillation on/off are controlled automatically for the power consumption reduction in music player mode.
- Clock source

  The AP / common domain block operates with the external clock input through the EXTAL1 pin.

A block diagram of the CPGA is shown in figure 11.1.

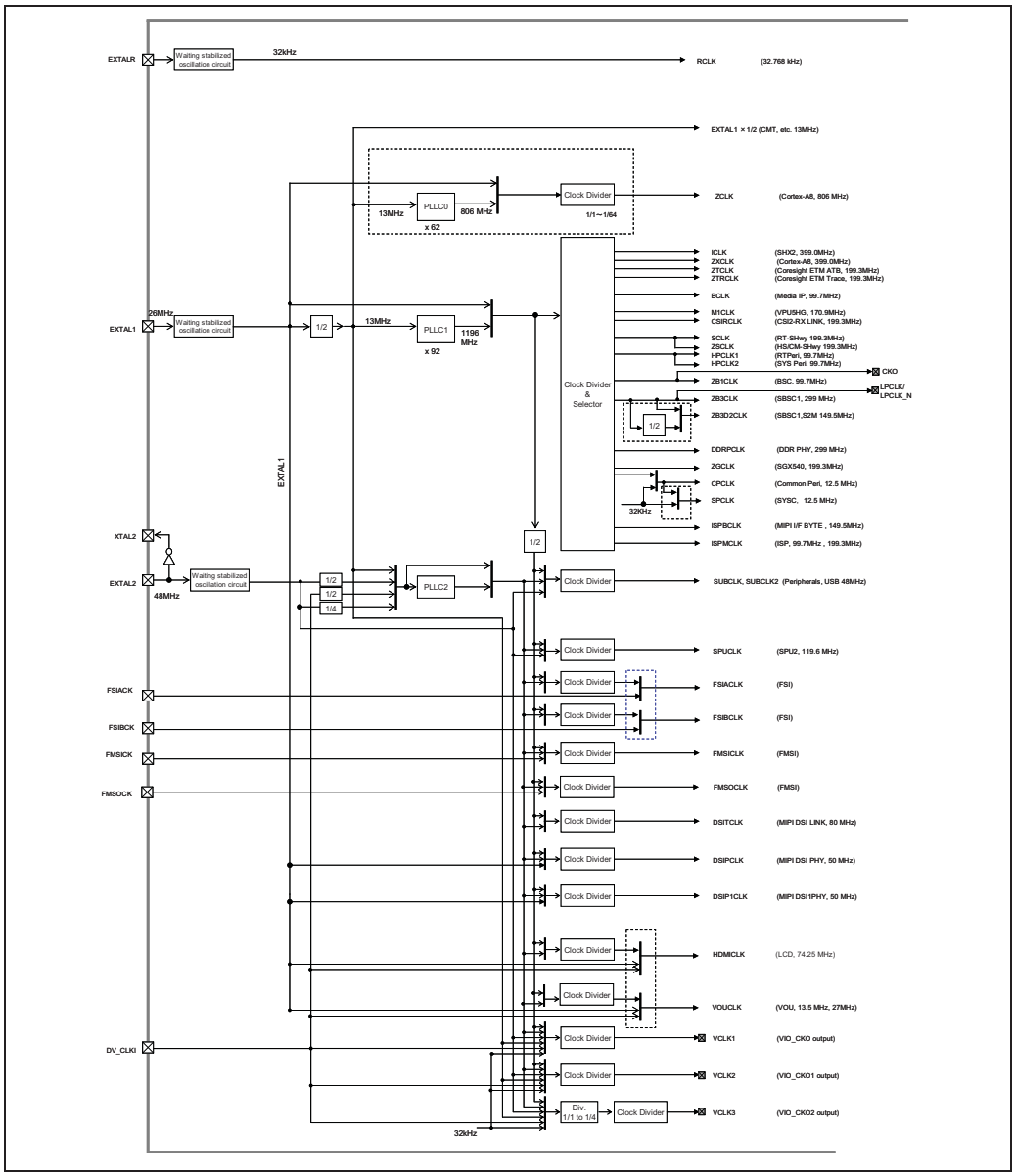


Figure 11.1 Block Diagram of CPGA

Each block of the CPGA in the AP block functions as follows:

(1) PLL Circuit C0

PLL circuit C0 multiplies the clock frequency input from the AP / Common domain main clock by the ratio of ×40 to ×92. The multiplication ratio is set by the frequency control register B (FRQCRB). Turning on and off PLL circuit C0 is set by the PLLC0 control register (PLLC01CR).

(2) Divider C0

The dividers (C0) generate the system CPU clock. The division ratio is set by each frequency control register.

(3) PLL Circuit C1

PLL circuit C1 multiplies the clock frequency input from the AP / Common domain main clock by the ratio of ×40 to ×92. The multiplication ratio is set by the frequency control register C (FRQCRC). Turning on and off PLL circuit C1 is set by the PLLC1 control register (PLLC01CR).

(4) PLL Circuit C2

PLL circuit C2 multiplies the frequency of the clock input from the AP / Common domain main clock, the clock input from the EXTAL2 pin being divided by 2, the clock input from the EXTAL2 pin being divided by 4, or the clock input from the DV_CKI pin being divided by 2 by the ratio of ×40 to ×92 as an input clock. Turning on and off PLL circuit C2 is set by the PLLC2 control register (PLLC2CR).

(5) Divider C1

The dividers (C1) generate the realtime CPU clock, media clock, VPU clock , ISP clock, CSI2 RX clock, ZG clock, high-speed peripheral clock, , system CPU debug trace clock, system CPU debug trace bus clock, SHwy clock, bus clock, SDRAM clock for SBSC1, DLL clock for SDRM interface PHY , and common peripheral clock. The division ratio is set by each frequency control register.

(6) Clock Frequency Control Circuit

The clock frequency control circuit controls the clock frequency according to the settings of the frequency control register A (FRQCRA), frequency control register B (FRQCRB), frequency control register C (FRQCRC), and frequency control register D (FRQCRD).

(7) Standby Control Circuit

The standby control circuit controls the state of the on-chip oscillation circuit and other modules during clock switching and in sleep mode or core standby mode.

(8) Frequency Control Register A (FRQCRA)

The frequency control register has bits for setting the multiplication ratio of PLL circuit C1, and the frequency division ratios of the realtime CPU clock, ZG clock , and media clock.

(9) Frequency Control Register B (FRQCRB)

The frequency control register has bits for setting the frequency division ratios of the system CPU clock for debugging and trace, system CPU clock debug trace clock, system CPU clock, and high-speed peripheral clock.

(10) Frequency Control Register C (FRQCRC)

The frequency control register has bits for setting the frequency division ratios of the SHwy clock, bus clock, SDRAM clock for SBSC1, and common peripheral clock.

(11) Frequency Control Register D (FRQCRD)

The frequency control register has bits for setting the frequency division ratios of the DLL clock for SDRAM interface PHI .

(12) Realtime Standby Control Register (RTSTBCR)

The realtime standby control register has bits for controlling the power-down modes.

(13) System Standby Control Register (SYSTBCR)

The system standby control register has bits for controlling the power-down modes.

(14) PLLC0,1 Control Register (PLLC01CR)

The PLLC0,1 control register has control bits assigned for turning on or off PLL circuit C0, C1.

(15) PLLC2 Control Register (PLLC2CR)

The PLLC2 control register has control bits assigned for turning on or off PLL circuit C2, and setting the multiplication ratio.

11.2 Input/Output Pins

Table 11.1 lists the CPGA pin configuration in the AP block.

Table 11.1 Pin Configuration and Functions of CPGA

Pin Name	Function	I/O	Description
XTAL2	Clock input pins	Output	Outputs amplified negative feedback of EXTAL2.
EXTAL2		Input	Used as an external clock input pin (e.g. 48 MHz).
EXTALR		Input	Connects the RTC clock.*
EXTAL1		Input	Used as an external clock input pin (26 MHz).*
CKO	Clock output pin	Output	Used as an external clock output pin.
LPCLK / LPCLK_N	Main pin of the SDRAM clock for SBSC1	Output	Used as the clock output pin for SBSC1.
VIO_CKO	Video clock output pin	Output	Used as a pin for video clock output 1.
VIO_CKO1	Video clock output pin	Output	Used as a pin for video clock output 2.
VIO_CKO2	Video clock output pin	Output	Used as a pin for video clock output 3.
DV_CLKI	Video clock input	Input	Used as the external clock input pin. This input signal can be used as a clock source of VCK1ϕ, VCK2ϕ, VCK3ϕ, HDMIϕ, and VOUϕ, and can be used as a reference of PLLC2.
FSIACK	Clock input for FSI port A	Input	Used as an external input clock for FSI clock A.
FSIBCK	Clock input for FSI port B	Input	Used as an external input clock for FSI clock B.
FMSICK	Clock input for FMSI input port	Input	Used as an external input clock of FMSI input clock.
FMSOCK	Clock input for FSMI output port	Input	Used as an external input clock of FSMI output clock.

Note: * Always input the RTC clock and EXTAL1 clock in this LSI.

11.3 Clock Operating Modes

Table 11.2 shows the initial clock settings.

PLL circuit C0, PLL circuit C1 and PLL circuit C2 are started in the PLL-OFF state during booting. After booting, set the PLLC01CR and PLLC2C to oscillate PLL circuit C0, oscillate PLL circuit C1 and PLL circuit C2.

Table 11.2 Clock Operating Modes

PLL Circuit C0	PLL Circuit C1	PLL Circuit C2	PLL Circuit C0 Multiplication Rate Setting	PLL Circuit C1 Multiplication Rate Setting
OFF	OFF	OFF	x40	x40

I	ZG	B	M1	CSIR	M1	ZTR	ZT	Z	HP	ZS	ZB3	ZB	CP	HP	CP
1/2	1/2	1/2	1/2	1/2	1/2	1/2	1/2	1	1/2	1/2	1/4	1/2	1/2	1/2	1/2

11.4 Clock Assignment to Modules

Table 11.3 shows the clocks assigned to each module.

Table 11.3 Clock Assignment to Modules

		Clock										Others
Domain	Module	R	I	B	Z	ZX	S, ZS	HP	CP	SUB	SUB2	
RT	Realtime CPU	–	○	–	–	–	○	○	–	–	–	
RT	HUDI	–	–	–	–	–	○	○	–	–	–	TCK
RT	DBGP	–	–	–	–	–	○	○	–	–	–	
RT	ASERAM	–	–	_	–	–	–	○	–	–	–	
RT	SUBC	–	–	–	–	–	○	○	–	–	–	
RT	PINTS	–	–	–	–	–	–	○	–	–	–	
RT	INTCS	–	–	–	–	–	–	○	–	–	–	
RT	INTCS2	○	–	–	–	–	–	○	–	–	–	
RT	INTCS3	–	–	–	–	–	–	○	–	–	–	
CM	WUCS	○	–	–	–	–	–	–	–	–	–	
RT	RT-SHwy	–	–	–	–	–	○	–	–	–	–	
RT	RTDMAC1	–	–	○	–	–	○	–	–	–	–	
RT	RTDMAC2	–	–	○	–	–	○	–	–	–	–	
RT	IPMMUR	–	–	○	–	–	○	–	–	–	–	
RT	IPMMUR2	–	–	○	–	–	○	–	–	–	–	
RT	CEU	–	–	○	–	–	–	–	–	–	–	
RT	VEU0	–	–	○	–	–	–	–	–	–	–	
RT	VEU1	–	–	○	–	–	–	–	–	–	–	
RT	VEU2	–	–	○	–	–	–	–	–	–	–	
RT	VEU3	–	–	○	–	–	–	–	–	–	–	
RT	BEU0	–	–	○	–	–	–	–	–	–	–	
RT	BEU1	–	–	○	–	–	–	–	–	–	–	
RT	BEU2	–	–	○	–	–	–	–	–	–	–	
RT	VPU	–	–	–	–	–	–	–	–	–	–	M1ϕ
RT	2DDMAC	–	–	○	–	–	○	–	–	–	–	
CM	MERAM	–	–	○	–	–	○	–	–	–	–	
RT	ICB	–	–	○	–	–	○	–	–	–	–	
RT	LCDC0	–	–	○	–	–	–	–	○	–	–	
RT	LCDC1	–	–	○	–	–	–	–	○	–	–	HDMIϕ

Domain	Module	Clock										Others
		R	I	B	Z	ZX	S, ZS	HP	CP	SUB	SUB2	
RT	CSI2	–	–	○	–	–	○	–	–	–	–	CSIRϕ
RT	DSI	–	–	○	–	–	–	–	–	–	–	DSITϕ
RT	JPU	–	–	○	–	–	–	–	–	–	–	
RT	TMU	–	–	–	–	–	–	–	–	○	–	
RT	CMT0	○	–	○	–	–	–	–	–	–	–	
RT	MSIOF0	–	–	–	–	–	–	–	–	○	–	
RT	IIC0	–	–	–	–	–	–	–	–	○	–	
SY	IIC1	–	–	–	–	–	–	–	–	○	–	
RT	IIC2	–	–	–	–	–	–	–	–	○	–	
SY	IIC3	–	–	_	–	–	–	–	–	○	–	
SY	IIC4	–	–	–	–	–	–	–	–	○	–	
SY	MFIS	–	–	–	–	–	–	○	–	–	–	
RT	TSIF0	–	–	–	–	–	–	○	–	–	–	
RT	TSIF1	–	–	–	–	–	–	○	–	–	–	
CM	VCR	–	–	–	–	–	–	–	–	–	–	
SY	System CPU	–	–	–	○	○	○	–	–	–	–	ZTϕ
SY	System-CPU- HS-SHwy Bridge	–	–	–	–	–	○	–	–	–	–	
SY	HS-SHwy	–	–	–	–	–	○	–	–	–	–	
SY	PINTA	–	–	–	–	–	–	○	–	–	–	
SY	INTCA	–	–	–	–	–	–	○	–	–	–	
SY	INTCA2	○	–	–	–	–	–	○	–	–	–	
SY	INTCA3	○	–	–	–	–	–	○	–	–	–	
CM	WUCA	○	–	–	–	–	–	–	–	–	–	
SY	SBSC1	–	–	–	–	–	○	–	–	–	–	ZB3ϕ, ZB3D2ϕ
SY	DMAC0	–	–	–	–	–	○	○	–	–	–	
SY	DMAC1	–	–	–	–	–	○	○	–	–	–	
SY	DMAC2	–	–	–	–	–	○	○	–	–	–	
SY	DDM	–	–	_	–	–	○	–	–	–	–	
SY	SGX540	–	–	–	–	–	○	–	–	–	–	ZGϕ
SY	TPU0	–	–	–	–	–	–	–	○	–	–	
SY	SCIFA0	–	–	–	–	–	–	–	–	○	–	
SY	SCIFA1	–	–	–	–	–	–	–	–	○	–	
SY	SCIFA2	–	–	–	–	–	–	–	–	○	–	
SY	SCIFA3	–	–	–	–	–	–	–	–	○	–	

Domain	Module	Clock										Others
		R	I	B	Z	ZX	S, ZS	HP	CP	SUB	SUB2	
SY	SCIFA4	–	–	–	–	–	–	–	–	○	–	
SY	SCIFA5	–	–	–	–	–	–	–	–	○	–	
SY	SCIFB	–	–	–	–	–	–	–	–	○	–	
SY	MSIOF1	–	–	–	–	–	–	–	–	○	–	
SY	MSIOF2	–	–	–	–	–	–	–	–	○	–	
SY	BBIF1	–	–	–	–	–	–	–	–	○	–	
CM	BBIF2	–	–	–	–	–	–	–	–	–	○	FSIϕ, FMSOϕ
SY	FLCTL	–	–	–	–	–	–	○	–	–	–	
SY	SDHFI0	–	–	–	–	–	–	○	–	–	–	
SY	SDHFI1	–	–	–	–	–	–	○	–	–	–	
SY	SDHFI2	–	–	_	–	–	–	○	–	–	–	
SY	IrDA	–	–	–	–	–	–	–	–	○	–	
CM	FSI2	–	–	–	–	–	○	○	–	–	–	SPUϕ, FSIAϕ, FSIBϕ
CM	FMSI	–	–	–	–	–	–	–	–	–	○	SPUϕ, FMSIϕ, FMSOϕ
CM	SPU2	–	–	–	–	–	○	–	–	–	–	SPUϕ
SY	USB0 HS	–	–	–	–	–	–	○	–	○	–	
SY	USB0 HS DMAC	–	–	–	–	–	○	○	–	○	–	
SY	USB1 HS	–	–	–	–	–	–	○	–	○	–	
SY	USB1 HS DMAC	–	–	–	–	–	○	○	–	○	–	
SY	Crypt Cell	–	–	–	–	–	○	○	–	–	–	
SY	Common-SHwy	–	–	–	–	–	○	–	–	–	–	
CM/SY/ RT	SHWYSTAT	–	–	–	–	–	–	○	–	–	–	
SY	BSC	–	–	–	–	–	–	○	–	–	–	ZBϕ
CM	MFIM	–	–	–	–	–	–	○	–	–	–	
CM	MFROM	–	–	–	–	–	–	○	–	–	–	
CM	ACMFI1	–	–	–	–	–	–	○	–	–	–	
CM	ACMFI2	–	–	_	–	–	–	○	–	–	–	
CM	MFRAM	○	–	–	–	–	–	–	○	–	–	
CM	CMT1	○	–	–	–	–	–	–	○	–	–	AP / Common domain main clock x 1/2
CM	CMT2	○	–	–	–	–	–	–	○	–	–	
CM	CMT3	○	–	–	–	–	–	–	○	–	–	
CM	CMT4	○	–	–	–	–	–	–	○	–	–	
CM	RWDT0	○	–	–	–	–	–	–	○	–	–	

Domain	Module	Clock										Others
		R	I	B	Z	ZX	S, ZS	HP	CP	SUB	SUB2	
CM	KEYSC	○	–	–	–	–	–	–	○	–	–	
CM	GPIO	–	–	–	–	–	–	–	○	–	–	
CM	PAD	–	–	–	–	–	–	–	–	–	–	
CM	CPGA	○	–	–	–	–	–	–	○	–	–	EXTAL2 source , AP / Common domain main clock x 1/2
CM	SYSC	○	–	–	–	–	–	–	○	–	–	SPϕ
CM	WUC (SYSC)	○	–	–	–	–	–	–	○	–	–	
CM	Coresight Debug	○	–	–	–	–	○	○	–	–	–	ZTRϕ, ZTϕ
SY	DBG	○	–	–	–	–	–	–	–	–	–	
SY	LIFEC	–	–	–	–	–	–	–	○	–	–	
RT	Camera-ISP	–	–	–	–	–	○	–	–	–	–	
RT	CAMIF	–	–	○	–	–	○	–	–	–	–	ISPBϕ
RT	CMOS-IF	–	–	–	–	–	○	–	–	–	–	ISPBϕ, CSIRϕ
RT	ISP-PERI	–	–	–	–	–	○	–	–	–	–	ISPBϕ
SY	HDMI	–	–	–	–	–	–	○	–	–	–	HDMIϕ, FSIBϕ
SY	CEC	○	–	–	–	–	–	○	–	–	–	
CM	VideoDAC	–	–	–	–	–	–	–	–	–	–	
CM	SDENC	–	–	○	–	–	–	–	–	–	–	
SY	MMCIF	–	–	–	–	–	–	○	–	–	–	
SY	HSI	–	–	–	–	–	–	○	–	–	–	
RT	JPU	–	–	○	–	–	–	–	–	–	–	
RT	VOSYNC	–	–	–	–	–	–	–	–	○	–	

11.5 Register Descriptions

Table 11.4 shows the CPGA register configuration in the AP block. Table 11.5 shows the register states in each operating mode.

Table 11.4 Register Configuration

Register Name	Abbreviation	R/W	Address	Access Size
frequency control register A	FRQCRA	R/W	H'E615 0000	32
frequency control register B	FRQCRB	R/W	H'E615 0004	32
frequency control register C	FRQCRC	R/W	H'E615 00E0	32
frequency control register D	FRQCRD	R/W	H'E615 00E4	32
Video clock frequency control register 1	VCLKCR1	R/W	H'E615 0008	32
Video clock frequency control register 2	VCLKCR2	R/W	H'E615 000C	32
Video clock frequency control register 3	VCLKCR3	R/W	H'E615 001C	32
FMSI clock frequency control register	FMSICKCR	R/W	H'E615 0010	32
FMSO clock frequency control register	FMSOCKCR	R/W	H'E615 0014	32
FSIA clock frequency control register	FSIACKCR	R/W	H'E615 0018	32
FSIB clock frequency control register	FSIBCKCR	R/W	H'E615 0090	32
SUB clock frequency control register	SUBCKCR	R/W	H'E615 0080	32
SPU clock frequency control register	SPUCKCR	R/W	H'E615 0084	32
VOU clock frequency control register	VOUCKCR	R/W	H'E615 0088	32
HDMI clock frequency control register	HDMICKCR	R/W	H'E615 0094	32
MIPI DSI TX Link clock frequency control register	DSITCKCR	R/W	H'E615 0060	32
MIPI DSI PHY0 clock frequency control register	DSI0PCKCR	R/W	H'E615 0064	32
MIPI DSI PHY1 clock frequency control register	DSI1PCKCR	R/W	H'E615 0098	32
Music player mode register	MPMODE	R/W	H'E615 00CC	32
Realtime standby control register	RTSTBCR	R/W	H'E615 0020	32
System standby control register	SYSTBCR	R/W	H'E615 0024	32
PLLC0 and PLLC1 control register	PLLC01CR	R/W	H'E615 0028	32

Register Name	Abbreviation	R/W	Address	Access Size
PLLC0 and PLLC1 stop condition register	PLLC01STPCR	R/W	H'E61500C8	32
PLLC2 control register	PLLC2CR	R/W	H'E615 002C	32
Module stop status register 0	MSTPSR0	R	H'E615 0030	32
Module stop status register 1	MSTPSR1	R	H'E615 0038	32
Module stop status register 2	MSTPSR2	R	H'E615 0040	32
Module stop status register 3	MSTPSR3	R	H'E615 0048	32
Module stop status register 4	MSTPSR4	R	H'E615 004C	32
Realtime module stop control register 0	RMSTPCR0 *2	R/W	H'E615 0110	32
Realtime module stop control register 1	RMSTPCR1 *2	R/W	H'E615 0114	32
Realtime module stop control register 2	RMSTPCR2 *2	R/W	H'E615 0118	32
Realtime module stop control register 3	RMSTPCR3 *2	R/W	H'E615 011C	32
Realtime module stop control register 4	RMSTPCR4 *2	R/W	H'E615 0120	32
System module stop control register 0	SMSTPCR0 *2	R/W	H'E615 0130	32
System module stop control register 1	SMSTPCR1 *2	R/W	H'E615 0134	32
System module stop control register 2	SMSTPCR2 *2	R/W	H'E615 0138	32
System module stop control register 3	SMSTPCR3 *2	R/W	H'E615 013C	32
System module stop control register 4	SMSTPCR4 *2	R/W	H'E615 0140	32
Software reset register 0	SRCR0	R/W	H'E615 80A0 *1	32
Software reset register 1	SRCR1	R/W	H'E615 80A8 *1	32
Software reset register 2	SRCR2	R/W	H'E615 80B0 *1	32
Software reset register 3	SRCR3	R/W	H'E615 80B8 *1	32
Software reset register 4	SRCR4	R/W	H'E615 80BC *1	32
Status register	ASTAT	R	H'E615 0054	32
Clock source control register	CKSCR	R/W	H'E615 00C0	32
VREF control register	VREFCR	R/W	H'E615 0108	32

Note: *1 Write access to a register allocated to address H'E615 8*** can be controlled through HPB semaphores. Obtain a semaphore before writing a register and release it after completing the write access.

*2 RMSTPCRn and SMSTPCRn might be collectively written as MSTPCRn.

Table 11.5 Register States in Each Operating Mode

Register Abbreviation	Power-On Reset *	System Reset *
FRQCRA	Initialized	Retained
FRQCRB	Initialized	Retained
FRQCRC	Initialized	Retained
FRQCRD	Initialized	Retained
VCLKCR1	Initialized	Retained
VCLKCR2	Initialized	Retained
VCLKCR3	Initialized	Retained
FMSICKCR	Initialized	Retained
FMSOCKCR	Initialized	Retained
FSIACKCR	Initialized	Retained
FSIBCKCR	Initialized	Retained
SUBCKCR	Initialized	Retained
SPUCKCR	Initialized	Retained
VOUCKCR	Initialized	Retained
HDMICKCR	Initialized	Retained
DSITCKCR	Initialized	Retained
DSI0PCKCR	Initialized	Retained
DSI1PCKCR	Initialized	Retained
RTSTBCR	Initialized	Retained
SYSTBCR	Initialized	Retained
PLLC01CR	Initialized	Retained
PLLC01STPCR	Initialized	Retained
PLLC2CR	Initialized	Retained
MSTPSR0	Initialized	Retained
MSTPSR1	Initialized	Retained
MSTPSR2	Initialized	Retained
MSTPSR3	Initialized	Retained
MSTPSR4	Initialized	Retained
RMSTPCR0	Initialized	Retained
RMSTPCR1	Initialized	Retained
RMSTPCR2	Initialized	Retained

Register Abbreviation	Power-On Reset *	System Reset *
RMSTPCR3	Initialized	Retained
RMSTPCR4	Initialized	Retained
SMSTPCR0	Initialized	Retained
SMSTPCR1	Initialized	Retained
SMSTPCR2	Initialized	Retained
SMSTPCR3	Initialized	Retained
SMSTPCR4	Initialized	Retained
ASTAT	Initialized	Retained
SRCR0	Initialized	Retained
SRCR1	Initialized	Retained
SRCR2	Initialized	Retained
SRCR3	Initialized	Retained
SRCR4	Initialized	Retained
MPMODE	Initialized	Retained
CKSCR	Initialized	Retained
VREFCR	Initialized	Retained

[Notes] * For details of the Reset range, see section 1-D.

11.5.1 Frequency Control Register A (FRQCRA)

FRQCRA is a 32-bit readable/writable register that specifies the frequency multiplication ratio of PLL circuit C1, and the frequency division ratios of the CPU clock (Iϕ), SGX clock (ZGϕ), CSI2 RX clock (CSIRϕ), and media clock (Bϕ). FRQCRA can be accessed only in longwords. The FRQCRA setting involves restrictions on the clock ratio as shown in table 11.6 of section 11.6 (6).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	STC[5:0]						IFC[3:0]				ZGFC[3:0]			
Initial value:	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	BFC[3:0]				M1FC[3:0]				CSIRFC[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31,30	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
29 to 24	STC[5:0]	010011	R/W	PLL circuit C1 Multiplication Ratio Multiplication is performed with a ratio of (setting + 1) × 2. 010011: ×40 : 101101: ×92 Other value : setting prohibited

Bit	Bit Name	Initial Value	R/W	Description
23 to 20	IFC[3:0]	0000	R/W	Realtime CPU Clock Frequency (Iϕ) Division Ratio 0000: ×1/2 0001: ×1/3 0010: ×1/4 0011: ×1/6 0100: ×1/8 0101: ×1/12 0110: ×1/16 0111: ×1/18 1000: ×1/24 1001: ×1/32 1010: ×1/36 1011: ×1/48 1100: Setting prohibited 1101: ×1/72 1110: ×1/96 1111: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Description
19 to 16	ZGFC[3:0]	0000	R/W	ZG Clock Frequency (ZGϕ) Division Ratio 0000: ×1/2 0001: ×1/3 0010: ×1/4 0011: ×1/6 0100: ×1/8 0101: ×1/12 0110: ×1/16 0111: ×1/18 1000: ×1/24 1001: ×1/32 1010: ×1/36 1011: ×1/48 1100: Setting prohibited 1101: ×1/72 1110: ×1/96 1111: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Description
15 to12	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 8	BFC[3:0]	0000	R/W	Media Clock Frequency (Bϕ) Division Ratio 0000: ×1/2 0001: ×1/3 0010: ×1/4 0011: ×1/6 0100: ×1/8 0101: ×1/12 0110: ×1/16 0111: ×1/18 1000: ×1/24 1001: ×1/32 1010: ×1/36 1011: ×1/48 1100: Setting prohibited 1101: ×1/72 1110: ×1/96 1111: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	M1FC[3:0]	0000	R/W	VPU Clock Frequency (M1ϕ) Division Ratio 0000: ×1/2 0001: ×1/3 0010: ×1/4 0011: ×1/6 0100: ×1/8 0101: ×1/12 0110: ×1/16 0111: ×1/18 1000: ×1/24 1001: ×1/32 1010: ×1/36 1011: ×1/48 1100: ×1/7 1101: ×1/72 1110: ×1/96 1111: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Description
3 to 0	CSIRFC [3:0]	0000	R/W	CSI2 RX Clock Frequency (CSIRϕ) Division Ratio 0000: ×1/2 0001: ×1/3 0010: ×1/4 0011: ×1/6 0100: ×1/8 0101: ×1/12 0110: ×1/16 0111: ×1/18 1000: ×1/24 1001: ×1/32 1010: ×1/36 1011: ×1/48 1100: Setting prohibited 1101: ×1/72 1110: ×1/96 1111: Setting prohibited

11.5.2 Frequency Control Register B (FRQCRB)

FRQCRB is a 32-bit readable/writable register that specifies the frequency division ratios of the system CPU clock (Zϕ and ZXϕ), system CPU clock for debugging and trace (ZTRϕ), system CPU debug and trace bus clock (ZTϕ), and high-speed peripheral clock (HPϕ). FRQCRB can be accessed only in longwords. The FRQCRB setting involves restrictions on the clock ratio as shown in table 11.6 of section 11.6 (6).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	KICK	-	ZFC[5:0]						ZTRFC[3:0]				ZTFC[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ZXFC[3:0]				-	-	-	-	HPFC[3:0]				-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	KICK	0	R/W	Kick 0: Does not activate the FRQCRA, FRQCRB, and FRQCRC settings. 1: Activates the FRQCRA, FRQCRB, and FRQCRC settings. This bit is automatically cleared to 0 when the frequency division setting is completed after 1 is written to this bit.
30	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
29 to 24	ZFC[5:0]	All 0	R/W	ZCLK frequency division ratio Divides the clock source (PLLC0 output) by (setting value + 1). 000000 : x 1/1 000001 : x 1/2 : 111111 : x 1/64
23 to 20	ZTRFC[3:0]	0000	R/W	System CPU Debugging and Trace Clock Frequency (ZTRϕ) Division Ratio 0000: ×1/2 0001: ×1/3 0010: ×1/4 0011: ×1/6 0100: ×1/8 0101: ×1/12 0110: ×1/16 0111: ×1/18 1000: ×1/24 1001: ×1/32 1010: ×1/36 1011: ×1/48 1100: Setting prohibited 1101: ×1/72 1110: ×1/96 1111: Setting prohibited ZTRϕ is supplied only in debugging mode.

Bit	Bit Name	Initial Value	R/W	Description
19 to 16	ZTFC[3:0]	0000	R/W	System CPU Debugging and Trace bus Clock Frequency (ZTϕ) Division Ratio 0000: ×1/2 0001: ×1/3 0010: ×1/4 0011: ×1/6 0100: ×1/8 0101: ×1/12 0110: ×1/16 0111: ×1/18 1000: ×1/24 1001: ×1/32 1010: ×1/36 1011: ×1/48 1100: Setting prohibited 1101: ×1/72 1110: ×1/96 1111: Setting prohibited ZTϕ is supplied only in debugging mode.

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	ZXFC[3:0]	0000	R/W	System CPU Clock Frequency (ZXϕ) Division Ratio 0000: ×1/2 0001: ×1/3 0010: ×1/4 0011: ×1/6 0100: ×1/8 0101: ×1/12 0110: ×1/16 0111: ×1/18 1000: ×1/24 1001: ×1/32 1010: ×1/36 1011: ×1/48 1100: Setting prohibited 1101: ×1/72 1110: ×1/96 1111: Setting prohibited
11 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	HPFC[3:0]	0000	R/W	High-Speed Peripheral Frequency (HPϕ) Division Ratio 0000: ×1/2 0001: ×1/3 0010: ×1/4 0011: ×1/6 0100: ×1/8 0101: ×1/12 0110: ×1/16 0111: ×1/18 1000: ×1/24 1001: ×1/32 1010: ×1/36 1011: ×1/48 1100: Setting prohibited 1101: ×1/72 1110: ×1/96 1111: Setting prohibited
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

11.5.3 Frequency Control Register C (FRQCRC)

FRQCRC is a 32-bit readable/writable register that specifies the frequency division ratios of the SHwy clock (Sϕ, ZSϕ), bus clock (ZBϕ), SDRAM clock for SBSC1 (ZB3ϕ), and common peripheral clock (CPϕ). FRQCRC can be accessed only in longwords. The FRQCRC setting involves restrictions on the clock ratio as shown in table 11.6 of section 11.6 (6).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ZB3D2 SEL	-	STC[5:0]						ISPBFC[3:0]				-			
Initial value:	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0
R/W:	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ZSFC[3:0]				ZBFC[3:0]				ZB3FC[3:0]				CPFC[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	ZB3D2SEL	0	R/W	ZB3CLK Clock Mode Select 0: DDR400 mode 1: DDR600 mode
30	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
29 to 24	STC[5:0]	010011	R/W	PLLC0 multiplication ratio Multiplication is performed with a ratio of (setting + 1) * 2 010011 : x 40 : 101101 : x 92 Other value : setting prohibited.
23 to 20	ISPBFC [3:0]	0000	R/W	Bus Clock Frequency (ISPBϕ) Division Ratio 0000: ×1/2 0001: ×1/3 0010: ×1/4 0011: ×1/6 0100: ×1/8 0101: ×1/12 0110: ×1/16 0111: ×1/18 1000: ×1/24 1001: ×1/32 1010: ×1/36 1011: ×1/48 1100: Setting prohibited 1101: ×1/72 1110: ×1/96 1111: Setting prohibited
19 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	ZSFC[3:0]	0000	R/W	Bus Clock Frequency (Sϕ and ZSϕ) Division Ratio 0000: ×1/2 0001: ×1/3 0010: ×1/4 0011: ×1/6 0100: ×1/8 0101: ×1/12 0110: ×1/16 0111: ×1/18 1000: ×1/24 1001: ×1/32 1010: ×1/36 1011: ×1/48 1100: Setting prohibited 1101: ×1/72 1110: ×1/96 1111: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Description
11 to 8	ZBFC[3:0]	0000	R/W	Bus Clock Frequency (ZBϕ) Division Ratio
				0000: ×1/2
				0001: ×1/3
				0010: ×1/4
				0011: ×1/6
				0100: ×1/8
				0101: ×1/12
				0110: ×1/16
				0111: ×1/18
				1000: ×1/24
				1001: ×1/32
				1010: ×1/36
				1011: ×1/48
				1100: Setting prohibited
				1101: ×1/72
				1110: ×1/96
				1111: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	ZB3FC[3:0]	0010	R/W	SDRAM Frequency (ZB3φ) Division Ratio for SBSC1 0000: ×1/2 0001: ×1/3 0010: ×1/4 0011: ×1/6 0100: ×1/8 0101: ×1/12 0110: ×1/16 0111: ×1/18 1000: ×1/24 1001: ×1/32 1010: ×1/36 1011: ×1/48 1100: Setting prohibited 1101: ×1/72 1110: ×1/96 1111: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Description
3 to 0	CPFC[3:0]	0000	R/W	Common Peripheral Frequency (CPϕ) Division Ratio 0000: ×1/2 0001: ×1/3 0010: ×1/4 0011: ×1/6 0100: ×1/8 0101: ×1/12 0110: ×1/16 0111: ×1/18 1000: ×1/24 1001: ×1/32 1010: ×1/36 1011: ×1/48 1100: Setting prohibited 1101: ×1/72 1110: ×1/96 1111: Setting prohibited

11.5.4 Frequency Control Register D (FRQCRD)

FRQCRD is a 32-bit readable/writable register that specifies the division ratio of the SDRAM interface PHI clock (DDRPϕ) frequency. FRQCRD can be accessed only in longwords. The FRQCRD setting involves restrictions on the clock ratio as shown in table 11.6 of section 11.6 (6).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DDRPCHG	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DDRPFC[3:0]				-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	DDRPCHG	0	R	DDRPCLK frequency change status flag 0: DDRPCLK frequency change is finished, and setting of DDRPFC[3:0] is valid. 1: DDRPCLK frequency change is started, and setting of DDRPFC[3:0] is invalid.
30 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	ZB3SFC [3:0]	0011	R/W	DDRPCLK frequency division ratio 0000 : prohibited 0001 : prohibited 0010 : x 1/4 0011 : x 1/6 0100 : x 1/8 0101 : x 1/12 0110 : x 1/16 0111 : prohibited 1000 : x 1/24 1001 : x 1/32 1011 : x 1/36 1100 : prohibited 1101 : x 1/48 1101 : x 1/72 1110 : x 1/96 1111 : prohibited
11 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

11.5.5 PLLC01 Control Register (PLLC01CR)

PLLC01CR is a 32-bit readable/writable register that turns on or off PLL circuits C0 and C1. PLLC01CR can be accessed only in longwords.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	PLL01E	-	-	-	-	-	-	-	-	-	-	-	CKO DIVSTP	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 15	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
14	PLL1E	0	R/W	PLL Circuit C0 and C1 Enable Turns PLL circuit C0 and C1 on or off. 0: PLL circuit C0 and C1 is turned off. The input to PLL circuit C0 and C1 is supplied as a clock. 1: PLL circuit C0 and C1 is turned on. The output from PLL circuit C0 and C1 is supplied as a clock
13 to 3	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	CKODIVSTP	0	R	Stop Bit of Divider for CKO* This bit sets whether the divider for CKO is to be turned on or off. 0: The divider for CKO is turned on. 1: The divider for CKO is turned off.

Bit	Bit Name	Initial Value	R/W	Description
1, 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Note: * When BROMMD0 in CMNCR of BSC is set to 1, the clock to be output to the CKO pin becomes an inverted ZB clock, making it unnecessary to output the divider for CKO. Therefore, this bit can be set to 1 to stop any unnecessary circuit in the CPG macro.

11.5.6 PLLC0 and PLLC1 Stop Condition Register (PLLC01STPCR)

PLLC01STPCR is a 32-bit readable/writable register that specifies the stop condition of PLLC0 and PLLC1 when PLLC01CR.PLLE is set to 1. PLLC01STPCR can be accessed only in longwords.

If the power supply status meets the stop condition of PLLC0 and PLLC1 specified in this register, the CPGA cancels the oscillation stop request to PLLC0 and PLLC1. PLLC0 and PLLC1 oscillate when this register is set to the initial value, meaning that the oscillation request from the application part always is enabled.

PLLC0 and PLLC1 are controlled by the same stop conditions. However as for control by the A3SM area, PLLC0 is controlled by the PLLC0STP bit when the A3SMSTP bit is cleared to 0.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	PLLC0 STP	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	A3SG STP	A3SM STP	A3SP STP	A4S STP	A3RL STP	A3RI STP	A2SL STP	A3RV STP	A4R STP	-	D4 STP	A4MP STP	A4LC STP	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28	PLLC0STP	0	R/W	PLLC0 Stop Condition by A3SM Power Status This bit is enabled only when A3SMSTP bit is cleared to 0. 0: PLLC0 does not stop when the power supply of the A3SM area is turned off. 1: PLLC0 stops when the power supply of the A3SM area is turned off.
27 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13	A3SGSTP	0	R/W	PLLC0 and PLLC1 Stop Condition by A3SG Power Status 0: PLLC0 and PLLC1 do not stop when the power supply of the A3SG area is turned off. 1: PLLC0 and PLLC1 stop when the power supply of the A3SG area is turned off.
12	A3SMSTP	0	R/W	PLLC0 and PLLC1 Stop Condition by A3SM Power Status 0: PLLC0 and PLLC1 do not stop when the power supply of the A3SM area is turned off. 1: PLLC0 and PLLC1 stop when the power supply of the A3SM area is turned off.
11	A3SPSTP	0	R/W	PLLC0 and PLLC1 Stop Condition by A3SP Power Status 0: PLLC0 and PLLC1 do not stop when the power supply of the A3SP area is turned off. 1: PLLC0 and PLLC1 stop when the power supply of the A3SP area is turned off.
10	A4SSTP	0	R/W	PLLC0 and PLLC1 Stop Condition by A4S Power Status 0: PLLC0 and PLLC1 do not stop when the power supply of the A4S area is turned off. 1: PLLC0 and PLLC1 stop when the power supply of the A4S area is turned off.

Bit	Bit Name	Initial Value	R/W	Description
9	A3RLSTP	0	R/W	PLLC0 and PLLC1 Stop Condition by A3RL Power Status 0: PLLC0 and PLLC1 do not stop when the power supply of the A3RL area is turned off. 1: PLLC0 and PLLC1 stop when the power supply of the A3RL area is turned off.
8	A3RISTP	0	R/W	PLLC0 and PLLC1 Stop Condition by A3RI Power Status 0: PLLC0 and PLLC1 do not stop when the power supply of the A3RI area is turned off. 1: PLLC0 and PLLC1 stop when the power supply of the A3RI area is turned off.
7	A2SLSTP	0	R/W	PLLC0 and PLLC1 Stop Condition by A2SL Power Status 0: PLLC0 and PLLC1 do not stop when the power supply of the A2SL area is turned off. 1: PLLC0 and PLLC1 stop when the power supply of the A2SL area is turned off.
6	A3RVSTP	0	R/W	PLLC0 and PLLC1 Stop Condition by A3RV Power Status 0: PLLC0 and PLLC1 do not stop when the power supply of the A3RV area is turned off. 1: PLLC0 and PLLC1 stop when the power supply of the A3RV area is turned off.
5	A4RSTP	0	R/W	PLLC0 and PLLC1 Stop Condition by A4R Power Status 0: PLLC0 and PLLC1 do not stop when the power supply of the A4R area is turned off. 1: PLLC0 and PLLC1 stop when the power supply of the A4R area is turned off.
4	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
3	D4STP	0	R/W	PLLC0 and PLLC1 Stop Condition by D4 Power Status 0: PLLC0 and PLLC1 do not stop when the power supply of the D4 area is turned off. 1: PLLC0 and PLLC1 stop when the power supply of the D4 area is turned off.

Bit	Bit Name	Initial Value	R/W	Description
2	A4MPSTP	0	R/W	PLLC0 and PLLC1 Stop Condition by A4MP Power Status 0: PLLC0 and PLLC1 do not stop when the power supply of the A4MP area is turned off. 1: PLLC0 and PLLC1 stop when the power supply of the A4MP area is turned off.
1	A4LCSTP	0	R/W	PLLC0 and PLLC1 Stop Condition by A3LC Power Status 0: PLLC0 and PLLC1 do not stop when the power supply of the A3LC area is turned off. 1: PLLC0 and PLLC1 stop when the power supply of the A3LC area is turned off.
0	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.

11.5.7 PLLC2 Control Register (PLLC2CR)

PLLC2CR is a 32-bit readable/writable register that controls PLLC2. PLLC2CR can be accessed only in longwords.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PLLE	-	STC[5:0]						-	-	-	-	-	-	-	-
Initial value:	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0
R/W:	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	CKSEL[1:0]		-	-	-	-	-	OE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	PLLE*[1]	0	R/W	PLLC2 Enable Turns PLL circuit C2 on or off. This bit is read as 1 after the oscillation settling time has passed. 0: PLL circuit C2 is oscillated. The output from PLL circuit C2 is supplied as a clock. 1: PLL circuit C2 is oscillated. The output from PLL circuit C2 is supplied as a clock.
30	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
29 to 24	STC[5:0]	010011	R/W	PLL Circuit C2 Multiplication Ratio PLL circuit C2 performs multiplication with a ratio of (setting + 1) × 2. 010011: × 40 : 101101: × 92
23 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 6	CKSEL [1:0]	00	R/W	PLL Circuit C2 Clock Source Select 00: EXTAL1 output ×1/2 01: EXTAL2/XTAL2 (crystal resonator) output 10: DV_CLKI output ×1/2 11: EXTAL2/XTAL2 (crystal resonator) output ×1/4 Other than above: Setting prohibited
5 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	XOE	1	R/W	XTAL2 (Crystal Resonator) Oscillation Enable 0: Enables XTAL2 oscillation 1: Stops XTAL2 oscillation

11.5.8 Video Clock Frequency Control Register 1 (VCLKCR1)

VCLKCR1 is a 32-bit readable/writable register that controls video clock frequency 1. VCLKCR1 can be accessed only in longwords.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	EXSRC[2:0]			-	-	-	CKSTP	-	-	VDIV[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
R/W:	R	R/W	R/W	R/W	R	R	R	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 15	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
14 to 12	EXSRC [2:0]	000	R/W	Clock Source Select 000: PLL circuit C1 output × 1/2 001: PLL circuit C2 output 010: DV_CLKI input 011: EXTAL2 input 100: AP / common domain clock × 1/2 101: EXTALR Other than above: Setting prohibited
11 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
8	CKSTP	0	R/W	Clock Stop 0: Supplies video clock 1 1: Stops video clock 1
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5 to 0	VDIV[5:0]	111111	R/W	Division Ratio These bits set the frequency division ratio of video clock 1. The frequency is set to the clock source specified by EXSRC[2:0] × 1 / (setting + 1).

11.5.9 Video Clock Frequency Control Register 2 (VCLKCR2)

VCLKCR2 is a 32-bit readable/writable register that controls video clock frequency 2. VCLKCR2 can be accessed only in longwords.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	EXSRC[2:0]			-	-	-	CKSTP	-	-	VDIV[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
R/W:	R	R/W	R/W	R/W	R	R	R	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 15	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
14 to 12	EXSRC[2:0]	000	R/W	Clock Source Select 000: PLL circuit C1 outpu t × 1/2 001: PLL circuit C2 output 010: DV_CLK input 011: EXTAL2 input 100: AP / common domain clock × 1/2 101: EXTALR Other than above: Setting prohibited
11 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	CKSTP	0	R/W	Clock Stop 0: Supplies video clock 2 1: Stops video clock 2
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5 to 0	VDIV[5:0]	111111	R/W	Division Ratio These bits set the frequency division ratio of video clock 2. The frequency is set to the clock source specified by EXSRC[2:0] × 1 / (setting + 1) .

11.5.10 Video Clock Frequency Control Register 3 (VCLKCR3)

VCLKCR2 is a 32-bit readable/writable register that controls video clock frequency 3. VCLKCR3 can be accessed only in longwords.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	EXSRC[2:0]			-	-	-	CKSTP	-	-	VDIV[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
R/W:	R	R/W	R/W	R/W	R	R	R	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 15	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
14 to 12	EXSRC[2:0]	000	R/W	Clock Source Select 000: PLL circuit C1 outpu t × 1/2 001: PLL circuit C2 output 010: DV_CLKI input 011: EXTAL2 input 100: AP / common domain clock × 1/2 101: EXTALR Other than above: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Description
11 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	CKSTP	0	R/W	Clock Stop 0: Supplies video clock 3 1: Stops video clock 3
7, 6	—	All 0	R	Division Ratio 00: × 1/1 01: × 1/2 10: Setting prohibited 11: × 1/4
5 to 0	VDIV[5:0]	111111	R/W	Division Ratio These bits set the frequency division ratio of video clock 2. The clock source specified by the EXSRC2 to EXSRC0 bits is set to the division ratio of PDIV1 or PDIV0 × 1 / (setting + 1).

11.5.11 FMSI Clock A Frequency Control Register (FMSICKCR)

FMSICKCR is a 32-bit readable/writable register that controls the FMS input port clock frequency. FMSICKCR can be accessed only in longwords.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	CKSTP	EXSRC[1:0]		DIV[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	CKSTP	0	R/W	Clock Stop 0: Supplies FMSI input port clock 1: Stops FMSI input port clock
7, 6	EXSRC[1:0]	00	R/W	Clock Source Select Selects the SIU clock A source. 00: PLL circuit C1 output × 1/2 01: PLL circuit C2 output 10: External input clock (pin name: FMSICK) 11: Setting prohibited
5 to 0	DIV[5:0]	111111	R/W	Division Ratio These bits set the frequency division ratio of SIU clock A. The clock source specified by EXSRC is set to the division ratio of 1 / (setting + 1).

11.5.12 MFSO Clock Frequency Control Register (FMSOCKCR)

FMSOCKCR is a 32-bit readable/writable register that controls the FMSI output port clock frequency. FMSOCKCR can be accessed only in longwords.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	CKSTP	EXSRC[1:0]		DIV[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	CKSTP	0	R/W	Clock Stop 0: Supplies FMSI output port clock B 1: Stops FMSI output port clock B
7, 6	EXSRC[1:0]	00	R/W	Clock Source Select Selects the FMSI output port source. 00: PLL circuit C1 output × 1/2 01: PLL circuit C2 output 10: External input clock (pin name: FMSOCK) 11: Setting prohibited
5 to 0	DIV[5:0]	111111	R/W	Division Ratio These bits set the frequency division ratio of SIU clock B. The clock source specified by EXSRC is set to the division ratio of 1 / (setting + 1).

11.5.13 FSIA Clock Frequency Control Register (FSIACKCR)

FSIACKCR is a 32-bit readable/writable register that controls the FSIA clock frequency. FSIACKCR can be accessed only in longwords.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	CKSTP	EXSRC[1:0]		DIV[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	CKSTP	0	R/W	Clock Stop 0: Supplies FSIA clock 1: Stops FSIA clock
7, 6	EXSRC[1:0]	00	R/W	Clock Source Select Selects the FSIA source. 00: PLL circuit C1 output × 1/2 01: PLL circuit C2 output 10: External input clock (pin name: FSIACK) 11: Setting prohibited
5 to 0	DIV[5:0]	111111	R/W	Division Ratio These bits set the frequency division ratio of SIU clock B. The clock source specified by EXSRC is set to the division ratio of 1 / (setting + 1).

11.5.14 FSIB Clock Frequency Control Register (FSIBCKCR)

FSIBCKCR is a 32-bit readable/writable register that controls the FSIB clock frequency. FSIBCKCR can be accessed only in longwords.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	CKSTP	EXSRC[1:0]		DIV[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	CKSTP	0	R/W	Clock Stop 0: Supplies FSIB clock 1: Stops FSIB clock
7, 6	EXSRC[1:0]	00	R/W	Clock Source Select Selects the FMSI output port source. 00: PLL circuit C1 output × 1/2 01: PLL circuit C2 output 10: External input clock (pin name: FSIBCK) 11: Setting prohibited
5 to 0	DIV[5:0]	111111	R/W	Division Ratio These bits set the frequency division ratio of SIU clock B. The clock source specified by EXSRC is set to the division ratio of 1 / (setting + 1).

11.5.15 SUB Clock Frequency Control Register (SUBCKCR)

SUBCKCR is a 32-bit readable/writable register that controls the SUB clock. SUBCKCR can be accessed only in longwords.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	E2MON	E2DET	-	-	-	SUBCK2 STP	SUBCK STP	-	CKSEL[1:0]		DIV[5:0]					
Initial value:	*[1]	1*[1]	0	0	0	0	0	1	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R	R	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	E2MON	*[1]	R	EXTAL2-Connected Clock Frequency Monitor 1: 36 MHz ≤ EXTAL2 0: Clock not connected or EXTAL2 < 36 MHz
14	E2DET	1*[1]	R	EXTAL2-Connected Clock Detection Period Monitor 1: Clock input to EXTAL2 is being detected. 0: Detection of clock input to EXTAL2 has ended.
13 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
10	SUBCK2STP	0	R/W	Clock Stop 0: Supplies SUBCK2 1: Stops SUBCK2
9	SUBCKSTP	0	R/W	Clock Stop 0: Supplies SUBCK 1: Stops SUBCK
8	—	1	R/W	Reserved These bits are always read as 1. The write value should always be 1.
7, 6	CKSEL [1:0]	*	R/W	Clock Select 00: PLL circuit C1 output × 1/2 01: PLL circuit C2 output 10: EXTAL2 11: Setting prohibited
5 to 0	DIV[5:0]	000000	R/W	Division Ratio These bits set the frequency division ratio of SUB clock. The clock source specified by the CKSEL1 and CKSEL0 bits is set to the division ratio of 1 / (setting + 1).

Notes: * After this LSI is booted, the E2DET bit is set to 1 (clock being detected) and the E2MON bit is cleared to 0 when one EXTALR cycle has passed. Use the E2MON value after the E2DET bit is cleared to 0.

11.5.16 SUP Clock Frequency Control Register (SUPCKCR)

SPUCKCR is a 32-bit readable/writable register that controls the SPU clock. SPUCKCR can be accessed only in longwords.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	CKSTP	EXSRC[1:0]		DIV[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	CKSTP	0	R/W	Clock Stop 0: Supplies SPU clock 1: Stops SPU clock
7	EXSRC	0	R/W	Clock Source Select 00: PLL circuit C1 output × 1/2 01: PLL circuit C2 output 10: EXTAL2 11: Setting prohibited
5 to 0	DIV[5:0]	111111	R/W	Division Ratio These bits set the frequency division ratio of SPU clock. The clock source specified by EXSRC is set to the division ratio of 1 / (setting + 1).

11.5.17 VOU Clock Frequency Control Register (VOUCKCR)

VOUCKCR is a 32-bit readable/writable register that controls the MSU clock. VOUCKCR can be accessed only in longwords.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	CKSTP	EXSRC[1:0]		DIV[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	CKSTP	0	R/W	Clock Stop 0: Supplies VOU clock 1: Stops VOU clock
7,6	EXSRC	0	R/W	Clock Source Select 00: PLL circuit C1 output × 1/2 01: PLL circuit C2 output 10: DV_CLKI 11:EXTAL1
5 to 0	DIV[5:0]	111111	R/W	Division Ratio These bits set the frequency division ratio of VOU clock. The clock source specified by EXSRC is set to the division ratio of 1 / (setting + 1).

11.5.18 HDMI Clock Frequency Control Register (HDMICKCR)

HDMICKCR is a 32-bit readable/writable register that controls the HDMI clock frequency. HDMICKCR can be accessed only in longwords.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	CKSTP	EXSRC[1:0]		DIV[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	CKSTP	0	R/W	Clock Stop 0: Supplies HDMI clock 1: Stops HDMI clock
7, 6	EXSRC[1:0]	00	R/W	Clock Source Select 00: PLL circuit C1 output × 1/2 01: PLL circuit C2 output 10: DV_CLKI 11: Setting prohibited
5 to 0	DIV[5:0]	111111	R/W	Division Ratio These bits set the frequency division ratio of HDMI clock. The clock source specified by EXSRC is set to the division ratio of 1 / (setting + 1).

11.5.19 DSI TX Link Clock Frequency Control Register (DSITCKCR)

DSITCKCR is a 32-bit readable/writable register that controls the MIPI DSI TX Link clock frequency. DSITCKCR can be accessed only in longwords.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	CKSTP	EXSRC	-	DIV[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	CKSTP	0	R/W	Clock Stop 0: Supplies DSI TX Link clock 1: Stops DSI TX Link clock
7	EXSRC	00	R/W	Clock Source Select 0: PLL circuit C1 output × 1/2 1: PLL circuit C2 output
6	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
5 to 0	DIV[5:0]	111111	R/W	Division Ratio These bits set the frequency division ratio of DSI TX Link clock. The clock source specified by EXSRC is set to the division ratio of 1 / (setting + 1).

11.5.20 DSI PHY0 Frequency Control Register (DSIPCKCR)

DSIPCKCR is a 32-bit readable/writable register that controls the frequency of MIPI VOU DSI PHY 0. DSIPCKCR can be accessed only in longwords.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	CKSTP	EXSRC[1:0]		DIV[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	CKSTP	0	R/W	Clock Stop 0: Supplies DSI PHY0 clock 1: Stops DSI PHY0 clock
7,6	EXSRC	0	R/W	Clock Source Select 00: PLL circuit C1 output × 1/2 01: PLL circuit C2 output 10: EXTAL1 11: Setting prohibited
5 to 0	DIV[5:0]	111111	R/W	Division Ratio These bits set the frequency division ratio of multi-function clock 1. The clock source specified by the EXSRC1 and EXSRC0 bits is set to the division ratio of 1 / (setting + 1).

11.5.21 DSI PHY 1 Clock Frequency Control Register (DSI1PCR)

DSI1PCR is a 32-bit readable/writable register that controls the frequency of MIPI VOU DSI PHY 1. DSI1CRCR can be accessed only in longwords.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	CKSTP	EXSRC[1:0]		DIV[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	CKSTP	0	R/W	Clock Stop 0: Supplies DSI PHY1 clock 1: Stops DSI PHY1 clock
7,6	EXSRC	0	R/W	Clock Source Select 00: PLL circuit C1 output × 1/2 01: PLL circuit C2 output 10: EXTAL1 11: Setting prohibited
5 to 0	DIV[5:0]	111111	R/W	Division Ratio These bits set the frequency division ratio of DSI PHY1 clock. The clock source specified by EXSRC1 and EXSRC0 is set to the division ratio of 1 / (setting + 1).

11.5.22 Music Play Mode Control Register (MPMODE)

MPMODE is a 32-bit readable/writable register that specifies the power management in music player mode. The power supply of the A4S area, PLLC0, PLLC1, and the clock signal input on the EXTAL1 pin are automatically controlled by the request from the SPU in music player mode. The range of automatic control of hardware is specified by setting this register.

The MPMODE register can be accessed only in longwords.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-					MPCKCFG	MPPLL	MPXTAL	MPPDWU
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3	MPCKCFG	0	R/W	MPMODE Clock Configuration Set MPCKCFG bit according to the SPU clock configuration. 0: SPU clock is EXTAL2 1: SPU clock is PLLC2 output, and PLLC2 clock source is EXTAL1 x 1/2

Bit	Bit Name	Initial Value	R/W	Description
2	MPPLL	0	R/W	MPMODE PLLC1 control 0 : Controls PLLC1 oscillation automatically when SPU request power & clock. 1 : Always request oscillation of PLLC1
1	MPXTAL	0	R/W	MPMODE XTAL1 control 0 : Controls EXTAL1 oscillation automatically when SPU request power & clock. 1 : Always request oscillation of EXTAL1
0	MPPDWU	0	R/W	MPMODE Power down/Wake Up control 0 : Controls A4S area power automatically when SPU request power & clock. 1 : Always request power on of A4S area

11.5.23 Realtime Standby Control Register (RTSTBCR)

RTSTBCR is a 32-bit readable/writable register that selects the state available when the realtime CPU core has executed the SLEEP instruction. RTSTBCR can be accessed only in longwords.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	CSYBY	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	CSTBY	0	R/W	Realtime CPU Core Standby Executing the SLEEP instruction from the SH after setting this bit makes a transition to CPU core standby mode. 0: Realtime CPU sleep 1: Realtime CPU core standby
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

11.5.24 System Standby Control Register (SYSTBCR)

SYSTBCR is a 32-bit readable/writable register that selects the state available when the system CPU has executed the "wait for interrupt" instruction and controls the software NMI. SYSTBCR can be accessed only in longwords.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	CSYBY	-	-	-	SFTNMI
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	CSTBY	0	R/W	System CPU Core Standby Executing the Wait for Interrupt instruction from the system CPU after setting this bit makes a transition to system CPU core standby mode. 0: System CPU sleep 1: System CPU core standby
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	SFTNMI	1	R/W	Software NMI 0: Drives the NMI signal to the INTCS at a low level 1: Drives the NMI signal to the INTCS at a high level

11.5.25 Module Stop Starts Register 0 (MSTPSR0)

MSTPCR0 is a 32-bit readable register that state of the module assigned to each bit.

MSTPCR0 can be accessed only in longwords.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MSTP ST031	MSTP ST030	MSTP ST029	-	-	MSTP ST026	-	-	MSTP ST023	MSTP ST022	MSTP ST022	-	MSTP ST019	MSTP ST018	MSTP ST017	MSTP ST016
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSTP ST015	-	-	-	-	-	-	-	MSTP ST007	-	-	-	-	-	MSTP ST001	MSTP ST000
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	MSTPST 031	0	R	Module Stop Status 031 Displays clock supply status of RT-CPU TLB 0: TLB operates 1: Clock supply to TLB halted
30	MSTPST 030	0	R	Module Stop Status 030 Displays clock supply status of RT-CPU Instruction Cache (IC) 0: IC operates 1: Clock supply to IC halted
29	MSTPST 029	0	R	Module Stop Status 029 Displays clock supply status of RT-CPU Operand Cache (OC) 0: OC operates 1: Clock supply to OC halted

Bit	Bit Name	Initial Value	R/W	Description
28, 27	—	All 0	R	Reserved These bits are always read as 0
26	MSTPST026	0	R	Module Stop Status 026 Displays clock supply status of RT-CPU X/Y memory 0: X/Y memory operates 1: Clock supply to X/Y memory halted
25, 24	—	All 0	R	Reserved These bits are always read as 0
23	MSTPST023	0	R	Module Stop Status 023 Displays clock supply status of RT-DMAC2 0: RT-DMAC2 operates 1: Clock supply to RT-DMAC2 halted
22	MSTPST022	0	R	Module Stop Status 022 Displays clock supply status of INTCS 0: INTCS operates 1: Clock supply to INTCS halted
21	MSTPST021	0	R	Module Stop Status 021 Displays clock supply status of RT-DMAC1 0: RT-DMAC1 operates 1: Clock supply to RT-DMAC1 halted
20	—	0	R	Reserved These bits are always read as 0
19	MSTPST019	0	R	Module Stop Status 019 Displays clock supply status of H-UDI 0: H-UDI operates 1: Clock supply to H-UDI halted
18	MSTPST018	0	R	Module Stop Status 018 Displays clock supply status of debug module 0: debug module operates 1: Clock supply to debug module halted

Bit	Bit Name	Initial Value	R/W	Description
17	MSTPST017	0	R	Module Stop Status 017 Displays clock supply status of UBC 0: UBC operates 1: Clock supply to UBC halted
16	MSTPST016	0	R	Module Stop Status 016 Displays clock supply status of debug module 0: debug module operates 1: Clock supply to debug module halted
15	MSTPST015	0	R	Module Stop Status 015 Displays clock supply status of ILRAM 0: ILRAM operates 1: Clock supply to ILRAM halted
14 to 8	—	All 0	R	Reserved These bits are always read as 0
7	MSTPST007	0	R	Module Stop Status 007 Displays clock supply status of ICB 0: ICB operates 1: Clock supply to ICB halted
6 to 3	—	All 0	R	Reserved These bits are always read as 0
2	—	1	R	Reserved These bits are always read as 1
1	MSTPST001	0	R	Module Stop Status 001 Displays clock supply status of IIC2 0: IIC2 operates 1: Clock supply to IIC2 halted
0	MSTPST000	0	R	Module Stop Status 000 Displays clock supply status of MSIOF0 0: MSIOF0 operates 1: Clock supply to MSIOF0 halted

11.5.26 Module Stop Starts Register 1 (MSTPSR1)

MSTPCR1 is a 32-bit readable register that state of the module assigned to each bit.

MSTPCR1 can be accessed only in longwords.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MSTP ST131	MSTP ST130	MSTP ST129	MSTP ST128	MSTP ST127	MSTP ST126	MSTP ST125	MSTP ST124	-	-	-	-	-	MSTP ST118	MSTP ST117	MSTP ST116
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSTP ST115	-	MSTP ST113	MSTP ST112	MSTP ST111	-	MSTP ST109	MSTP ST108	-	MSTP ST106	MSTP ST105	MSTP ST104	MSTP ST103	MSTP ST102	MSTP ST101	MSTP ST100
Initial value:	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	MSTPST 131	1	R	Module Stop Status 131 Displays clock supply status of VEU3 0: VEU3 operates 1: Clock supply to VEU3 halted
30	MSTPST 130	1	R	Module Stop Status 130 Displays clock supply status of VEU2 0: VEU2 operates 1: Clock supply to VEU2 halted
29	MSTPST 129	1	R	Module Stop Status 129 Displays clock supply status of VEU1 0: VEU1 operates 1: Clock supply to VEU1 halted

Bit	Bit Name	Initial Value	R/W	Description
28	MSTPST128	1	R	Module Stop Status 128 Displays clock supply status of VEU0 0: VEU0 operates 1: Clock supply to VEU0 halted
27	MSTPST127	1	R	Module Stop Status 127 Displays clock supply status of CEU 0: CEU operates 1: Clock supply to CEU halted
26	MSTPST126	1	R	Module Stop Status 126 Displays clock supply status of CSI2 RX 0: CSI2 RX operates 1: Clock supply to CSI2 RX halted
25	MSTPST125	1	R	Module Stop Status 125 Displays clock supply status of TMU0 0: TMU0 operates 1: Clock supply to TMU0 halted
24	MSTPST124	1	R	Module Stop Status 124 Displays clock supply status of CMT0 0: CMT0 operates 1: Clock supply to CMT0 halted
23 to 19	—	All 1	R	Reserved These bits are always read as 0
18	MSTPST118	0	R	Module Stop Status 118 Displays clock supply status of DSI TX Link 0: DSI TX Link operates 1: Clock supply to DSI TX Link halted
17	MSTPST117	0	R	Module Stop Status 117 Displays clock supply status of LCDC1 0: LCDC1 operates 1: Clock supply to LCDC1 halted

Bit	Bit Name	Initial Value	R/W	Description
16	MSTPST116	1	R	Module Stop Status 116 Displays clock supply status of IIC0 0: IIC0 operates 1: Clock supply to IIC0 halted 1: Clock supply to RT-DMAC1 halted
15	MSTPST115	1	R	Module Stop Status 115 Displays clock supply status of 2D-DMAC 0: 2D-DMAC operates 1: Clock supply to 2D-DMAC halted
14	—	1	R	Reserved These bits are always read as 1
13	MSTPST113	0	R	Module Stop Status 113 Displays clock supply status of MERAM 0: MERAM operates 1: Clock supply to MERAM halted
12	MSTPST112	1	R	Module Stop Status 112 Displays clock supply status of SGX540 0: SGX540 operates 1: Clock supply to SGX540 halted
11	MSTPST111	1	R	Module Stop Status 111 Displays clock supply status of TMU1 0: TMU1 operates 1: Clock supply to TMU1 halted
10	—	1	R	Reserved These bits are always read as 1
9	MSTPST109	1	R	Module Stop Status 109 Displays clock supply status of TSIF1 0: TSIF1 operates 1: Clock supply to TSIF1 halted

Bit	Bit Name	Initial Value	R/W	Description
8	MSTPST108	1	R	Module Stop Status 108 Displays clock supply status of TSIF0 0: TSIF0 operates 1: Clock supply to TSIF0 halted
7	—	1	R	Reserved These bits are always read as 1
6	MSTPST106	1	R	Module Stop Status 106 Displays clock supply status of JPU 0: JPU operates 1: Clock supply to JPU halted
5	MSTPST105	1	R	Module Stop Status 105 Displays clock supply status of JPU6E 0: JPU6E operates 1: Clock supply to JPU6E halted
4	MSTPST104	1	R	Module Stop Status 104 Displays clock supply status of BEU2 0: BEU2 operates 1: Clock supply to BEU2 halted
3	MSTPST103	1	R	Module Stop Status 103 Displays clock supply status of BEU1 0: BEU1 operates 1: Clock supply to BEU1 halted
2	MSTPST102	1	R	Module Stop Status 103 Displays clock supply status of BEU0 0: BEU0 operates 1: Clock supply to BEU0 halted
1	MSTPST101	1	R	Module Stop Status 102 Displays clock supply status of VPU 0: VPU operates 1: Clock supply to VPU halted

Bit	Bit Name	Initial Value	R/W	Description
0	MSTPST000	0	R	Module Stop Status 000 Displays clock supply status of MSIOF0 0: MSIOF0 operates 1: Clock supply to MSIOF0 halted

11.5.27 Module Stop Starts Register 2 (MSTPSR2)

MSTPCR2 is a 32-bit readable register that state of the module assigned to each bit.

MSTPCR2 can be accessed only in longwords.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	MSTP ST229	MSTP ST228	-	MSTP ST226	MSTP ST225	MSTP ST224	MSTP ST223	MSTP ST222	-	-	-	MSTP ST218	MSTP ST217	MSTP ST216
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSTP ST215	MSTP ST214	MSTP ST213	MSTP ST212	-	MSTP ST210	MSTP ST209	MSTP ST208	MSTP ST207	MSTP ST206	MSTP ST205	MSTP ST204	MSTP ST203	MSTP ST202	MSTP ST201	MSTP ST200
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 30	—	All 0	R	Reserved These bits are always read as 0
29	MSTPST 229	0	R	Module Stop Status 229 Displays clock supply status of INTCA 0: INTCA operates 1: Clock supply to INTCA halted

Bit	Bit Name	Initial Value	R/W	Description
28	MSTPST228	0	R	Module Stop Status 228 Displays clock supply status of Crypt 0: Crypt operates 1: Clock supply to Crypt halted
27	—	0	R	Reserved These bits are always read as 0
26	MSTPST226	0	R	Module Stop Status 226 Displays clock supply status of BBIF1 0: BBIF1 operates 1: Clock supply to BBIF1 halted
25	MSTPST225	0	R	Module Stop Status 225 Displays clock supply status of BBIF2 0: BBIF2 operates 1: Clock supply to BBIF2 halted
24	MSTPST224	0	R	Module Stop Status 224 Displays clock supply status of VOSYNC 0: VOSYNC operates 1: Clock supply to VOSYNC halted
23	MSTPST223	0	R	Module Stop Status 223 Displays clock supply status of SPU 0: SPU operates 1: Clock supply to SPU halted
22	MSTPST222	0	R	Module Stop Status 222 Displays clock supply status of MISTY 0: MISTY operates 1: Clock supply to MISTY halted
21 to 19	—	0	R	Reserved These bits are always read as 0
18	MSTPST218	0	R	Module Stop Status 218 Displays clock supply status of SY-DMAC1 0: SY-DMAC1 operates 1: Clock supply to SY-DMAC1 halted

Bit	Bit Name	Initial Value	R/W	Description
17	MSTPST217	0	R	Module Stop Status 217 Displays clock supply status of SY-DMAC2 0: SY-DMAC2 operates 1: Clock supply to SY-DMAC2 halted
16	MSTPST216	0	R	Module Stop Status 216 Displays clock supply status of SY-DMAC3 0: SY-DMAC3 operates 1: Clock supply to SY-DMAC3halted
15	MSTPST215	0	R	Module Stop Status 215 Displays clock supply status of DDM 0: DDM operates 1: Clock supply to DDM halted
14	MSTPST214	0	R	Module Stop Status 214 Displays clock supply status of USB-DMAC 0: USB-DMAC operates 1: Clock supply to USB-DMAC halted
13	MSTPST213	0	R	Module Stop Status 213 Displays clock supply status of MFIS 0: MFIS operates 1: Clock supply to MFIS halted
12	MSTPST212	0	R	Module Stop Status 212 Displays clock supply status of MFIM 0: MFIM operates 1: Clock supply to MFIM halted
11	—	0	R	Reserved These bits are always read as 0
10	MSTPST210	0	R	Module Stop Status 210 Displays clock supply status of MMFROM 0: MMFROM operates 1: Clock supply to MMFROM halted

Bit	Bit Name	Initial Value	R/W	Description
9	MSTPST209	0	R	Module Stop Status 209 Displays clock supply status of SMFRAM 0: SMFRAM operates 1: Clock supply to SMFRAM halted
8	MSTPST208	0	R	Module Stop Status 208 Displays clock supply status of MSIOF1 0: MSIOF1 operates 1: Clock supply to MSIOF1 halted
7	MSTPST207	0	R	Module Stop Status 207 Displays clock supply status of SCIFA5 0: SCIFA5 operates 1: Clock supply to SCIFA5 halted
6	MSTPST206	0	R	Module Stop Status 206 Displays clock supply status of SCIFB 0: SCIFB operates 1: Clock supply to SCIFB halted
5	MSTPST205	0	R	Module Stop Status 205 Displays clock supply status of MSIOF2 0: MSIOF2 operates 1: Clock supply to MSIOF2 halted
4	MSTPST204	0	R	Module Stop Status 204 Displays clock supply status of SCIFA0 0: SCIFA0 operates 1: Clock supply to SCIFA0 halted
3	MSTPST203	0	R	Module Stop Status 203 Displays clock supply status of SCIFA1 0: SCIFA1 operates 1: Clock supply to SCIFA1 halted
2	MSTPST202	0	R	Module Stop Status 202 Displays clock supply status of SCIFA2 0: SCIFA2 operates 1: Clock supply to SCIFA2 halted

Bit	Bit Name	Initial Value	R/W	Description
1	MSTPST201	0	R	Module Stop Status 201 Displays clock supply status of SCIFA3 0: SCIFA3 operates 1: Clock supply to SCIFA3 halted
0	MSTPST200	0	R	Module Stop Status 200 Displays clock supply status of SCIFA4 0: SCIFA4 operates 1: Clock supply to SCIFA4 halted

11.5.28 Module Stop Starts Register 3 (MSTPSR3)

MSTPCR3 is a 32-bit readable register that state of the module assigned to each bit.

MSTPCR3 can be accessed only in longwords.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	MSTP ST329	MSTP ST328	MSTP ST327	MSTP ST326	MSTP ST325	-	MSTP ST323	MSTP ST322	MSTP ST321	-	-	-	-	MSTP ST316
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSTP ST315	MSTP ST314	MSTP ST313	MSTP ST312	-	-	-	MSTP ST308	-	-	-	MSTP ST304	MSTP ST203	-	-	-
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 30	—	All 0	R	Reserved
29	MSTPST 329	1	R	Module Stop Status 329 Displays clock supply status of CMT1 0: CMT1 operates 1: Clock supply to CMT1 halted
28	MSTPST 328	1	R	Module Stop Status 328 Displays clock supply status of FSI 0: FSI operates 1: Clock supply to FSI halted

Bit	Bit Name	Initial Value	R/W	Description
27	MSTPST327	1	R	Module Stop Status 327 Displays clock supply status of FMSI 0: FMSI operates 1: Clock supply to FMSI halted
26	—	1	R	Reserved These bits are always read as 1
25	MSTPST325	1	R	Module Stop Status 325 Displays clock supply status of IrDA 0: IrDA operates 1: Clock supply to IrDA halted
24	—	1	R	Reserved These bits are always read as 1
23	MSTPST323	1	R	Module Stop Status 323 Displays clock supply status of IIC1 0: IIC1 operates 1: Clock supply to IIC1 halted
22	MSTPST322	1	R	Module Stop Status 322 Displays clock supply status of USB 0: USB operates 1: Clock supply to USB halted
21	MSTPST321	1	R	Module Stop Status 321 Displays clock supply status of SBSC1 performance monitor 0: SBSC1 performance monitor operates 1: Clock supply to SBSC1 performance monitor halted
20 to 17	—	All 1	R	Reserved These bits are always read as 1
16	MSTPST316	1	R	Module Stop Status 316 Displays clock supply status of SHWYSTAT 0: SHWYSTAT operates 1: Clock supply to SHWYSTAT halted

Bit	Bit Name	Initial Value	R/W	Description
15	MSTPST315	1	R	Module Stop Status 315 Displays clock supply status of FLCTL 0: FLCTL operates 1: Clock supply to FLCTL halted
14	MSTPST314	1	R	Module Stop Status 314 Displays clock supply status of SDHI0 0: SDHI0 operates 1: Clock supply to SDHI0 halted
13	MSTPST313	1	R	Module Stop Status 313 Displays clock supply status of SDHI1 0: SDHI1 operates 1: Clock supply to SDHI1 halted
12	MSTPST312	1	R	Module Stop Status 312 Displays clock supply status of MMC 0: MMC operates 1: Clock supply to MMC halted
11 to 9	—	All 1	R	Reserved These bits are always read as 1
8	MSTPST308	1	R	Module Stop Status 308 Displays clock supply status of MFIM MERAM Access function 0: MFIM MERAM Access function operates 1: Clock supply to MFIM MERAM Access function halted
7 to 5	—	All 1	R	Reserved These bits are always read as 1
4	MSTPST304	1	R	Module Stop Status 304 Displays clock supply status of TPU0 0: TPU0 operates 1: Clock supply to TPU0 halted
3 to 0	—	All 1	R	Reserved These bits are always read as 1

11.5.29 Module Stop Starts Register 4 (MSTPSR4)

MSTPCR4 is a 32-bit readable register that state of the module assigned to each bit.

MSTPCR4 can be accessed only in longwords.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	MSTP ST429	MSTP ST428	MSTP ST427	MSTP ST426	MSTP ST425	MSTP ST424	MSTP ST423	MSTP ST422	MSTP ST421	-	-	-	-	-
Initial value:	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSTP ST415	MSTP ST414	MSTP ST413	MSTP ST412	MSTP ST411	MSTP ST410	MSTP ST409	MSTP ST408	MSTP ST407	MSTP ST406	MSTP ST405	MSTP ST404	MSTP ST403	MSTP ST402	-	MSTP ST400
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 30	—	All 1	R	Reserved These bits are always read as 1
29	MSTPST 429	1	R	Module Stop Status 429 Displays clock supply status of SDENC DAC 0: SDENC DAC operates 1: Clock supply to SDENC DAC halted
28	MSTPST 428	1	R	Module Stop Status 428 Displays clock supply status of SDENC 0: SDENC operates 1: Clock supply to SDENC halted

Bit	Bit Name	Initial Value	R/W	Description
27	MSTPST427	1	R	Module Stop Status 427 Displays clock supply status of ISP 0: ISP operates 1: Clock supply to ISP halted
26	MSTPST426	1	R	Module Stop Status 426 Displays clock supply status of ISP (CAMIF) 0: ISP (CAMIF) operates 1: Clock supply to ISP (CAMIF) halted
25	MSTPST425	1	R	Module Stop Status 425 Displays clock supply status of ISP (CMOSIF) 0: ISP (CMOSIF) operates 1: Clock supply to ISP (CMOSIF) halted
24	MSTPST424	1	R	Module Stop Status 424 Displays clock supply status of ISP (JG) 0: ISP (JG) operates 1: Clock supply to ISP (JG) halted
23	MSTPST423	1	R	Module Stop Status 423 Displays clock supply status of DSI TX1 0: DSI TX1 Link operates 1: Clock supply to DSI TX1 Link halted
22	MSTPST422	0	R	Module Stop Status 422 Displays clock supply status of ACMFI1 0: ACMFI1 operates 1: Clock supply to ACMFI1 halted
21	MSTPST421	0	R	Module Stop Status 421 Displays clock supply status of ACMFI2 0: ACMFI2 operates 1: Clock supply to ACMFI2 halted
20 to 16	—	All 0	R	Reserved These bits are always read as 0

Bit	Bit Name	Initial Value	R/W	Description
15	MSTPST415	0	R	Module Stop Status 415 Displays clock supply status of SDHI2 0: SDHI2 operates 1: Clock supply to SDHI2 halted
14	MSTPST314	0	R	Module Stop Status 414 Displays clock supply status of MIPI-HSI 0: MIPI-HSI operates 1: Clock supply to MIPI-HSI halted
13	MSTPST413	0	R	Module Stop Status 413 Displays clock supply status of HDMI 0: HDMI operates 1: Clock supply to HDMI halted
12	MSTPST412	0	R	Module Stop Status 412 Displays clock supply status of CEC 0: CEC operates 1: Clock supply to CEC halted
11	MSTPST411	0	R	Module Stop Status 411 Displays clock supply status of IIC3 0: IIC3 operates 1: Clock supply to IIC3 halted
10	MSTPST410	0	R	Module Stop Status 410 Displays clock supply status of IIC4 0: IIC4 operates 1: Clock supply to IIC4 halted
9	MSTPST409	0	R	Module Stop Status 409 Displays clock supply status of ACMFI1/ACMFI2 RAM 0: ACMFI1/ACMFI2 RAM operates 1: Clock supply to ACMFI1/ACMFI2 RAM halted
8	MSTPST408	0	R	Module Stop Status 408 Displays clock supply status of SIB(ACMFI1/ACMFI2) 0: SIB(ACMFI1/ACMFI2) operates 1: Clock supply to SIB(ACMFI1/ACMFI2) halted

Bit	Bit Name	Initial Value	R/W	Description
7	MSTPST407	0	R	Module Stop Status 407 Displays clock supply status of USB DMAC1 0: USB DMAC1 operates 1: Clock supply to USB DMAC1 halted
6	MSTPST406	0	R	Module Stop Status 406 Displays clock supply status of USB1 0: USB1 operates 1: Clock supply to USB1 halted
5	MSTPST405	0	R	Module Stop Status 405 Displays clock supply status of CMT4 0: CMT4 operates 1: Clock supply to CMT4 halted
4	MSTPST404	0	R	Module Stop Status 404 Displays clock supply status of CMT3 0: CMT3 operates 1: Clock supply to CMT3 halted
3	MSTPST403	0	R	Module Stop Status 403 Displays clock supply status of KEYSC 0: KEYSC operates 1: Clock supply to KEYSC halted
2	MSTPST402	0	R	Module Stop Status 402 Displays clock supply status of RWDT0 0: RWDT0 operates 1: Clock supply to RWDT0 halted
1	—	0	R	Reserved These bits are always read as 0
0	MSTPST400	0	R	Module Stop Status 400 Displays clock supply status of CMT2 0: CMT2 operates 1: Clock supply to CMT2 halted

11.5.30 Module stop control register 0 (RMSTPCR0/ SMSTPCR0)

RMSTPCR0, SMSTPCR0 is a 32-bit readable/ writable register that individually starts or stops the module assigned to each bit. RMSTPCR0 and SMSTPCR0 assume the control from corresponding RT-CPU and SYS-CPU. It enters the state of the module stop when both of RMSTPCR0 and SMSTPCR0 settings are stops. The module stop is displayed in MSTPSR0. MSTPCR0 can be accessed only in longwords.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MSTP 031	MSTP 030	MSTP 029	-	-	MSTP 026	-	-	MSTP 023	MSTP 022	MSTP 022	-	MSTP 019	MSTP 018	MSTP 017	MSTP 016
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSTP 015	-	-	-	-	-	-	-	MSTP 007	-	-	-	-	-	MSTP 001	MSTP 000
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	MSTP 031	0	R/W	Module Stop bit 031 Controls clock supply to RT-CPU TLB 0: TLB operates 1: Clock supply to TLB halted
30	MSTP 030	0	R/W	Module Stop bit 030 Controls clock supply to RT-CPU Instruction Cache (IC) 0: IC operates 1: Clock supply to IC halted
29	MSTP 029	0	R/W	Module Stop bit 029 Controls clock supply to RT-CPU Operand Cache (OC) 0: OC operates 1: Clock supply to OC halted 0: OC operates 1: Clock supply to OC halted

Bit	Bit Name	Initial Value	R/W	Description
28, 27	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
26	MSTP026	0	R/W	Module Stop bit 026 Controls clock supply to RT-CPU X/Y memory 0: X/Y memory operates 1: Clock supply to X/Y memory halted
25, 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23	MSTP023	0	R/W	Module Stop bit 023 Controls clock supply to RT-DMAC2 0: RT-DMAC2 operates 1: Clock supply to RT-DMAC2 halted
22	MSTP022	0	R/W	Module Stop bit 022 Controls clock supply to INTCS 0: INTCS operates 1: Clock supply to INTCS halted
21	MSTP021	0	R/W	Module Stop bit 021 Controls clock supply to RT-DMAC1 0: RT-DMAC1 operates 1: Clock supply to RT-DMAC1 halted
20	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
19	MSTP019	0	R/W	Module Stop bit 019 Controls clock supply to H-UDI 0: H-UDI operates 1: Clock supply to H-UDI halted
18	MSTP018	0	R/W	Module Stop bit 018 Controls clock supply to debug module 0: debug module operates 1: Clock supply to debug module halted

Bit	Bit Name	Initial Value	R/W	Description
17	MSTP017	0	R/W	Module Stop bit 017 Controls clock supply to UBC 0: UBC operates 1: Clock supply to UBC halted
16	MSTP016	0	R/W	Module Stop bit 016 Controls clock supply to debug module 0: debug module operates 1: Clock supply to debug module halted
15	MSTP015	0	R/W	Module Stop bit 015 Controls clock supply to ILRAM 0: ILRAM operates 1: Clock supply to ILRAM halted
14 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	MSTP007	0	R	Module Stop bit 007 Controls clock supply to ICB 0: ICB operates 1: Clock supply to ICB halted
6 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	—	1	R	Reserved These bits are always read as 1. The write value should always be 1.
1	MSTPST001	0	R	Module Stop bit 001 Controls clock supply to ICB 0: IIC2 operates 1: Clock supply to IIC2 halted
0	MSTPST000	0	R	Module Stop bit 000 Controls clock supply to MSIOF0 0: MSIOF0 operates 1: Clock supply to MSIOF0 halted

11.5.31 Module Stop Control Register 1 (RMSTPCR1/ SMSTPCR1)

RMSTPCR1, SMSTPCR1 is a 32-bit readable/ writable register that individually starts or stops the module assigned to each bit. RMSTPCR1 and SMSTPCR1 assume the control from corresponding RT-CPU and SYS-CPU. It enters the state of the module stop when both of RMSTPCR1 and SMSTPCR1 settings are stops. The module stop is displayed in MSTPSR0. MSTPCR1 can be accessed only in longwords.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MSTP131	MSTP130	MSTP129	MSTP128	MSTP127	MSTP126	MSTP125	MSTP124	-	-	-	-	-	MSTP118	MSTP117	MSTP116
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSTP115	-	MSTP113	MSTP112	MSTP111	-	MSTP109	MSTP108	-	MSTP106	MSTP105	MSTP104	MSTP103	MSTP102	MSTP101	MSTP100
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	MSTP131	1	R/W	Module Stop bit 131 Controls clock supply to VEU3 0: VEU3 operates 1: Clock supply to VEU3 halted
30	MSTP130	1	R/W	Module Stop bit 130 Controls clock supply to VEU2 0: VEU2 operates 1: Clock supply to VEU2 halted
29	MSTP129	1	R/W	Module Stop bit 129 Controls clock supply to VEU1 0: VEU1 operates 1: Clock supply to VEU1 halted

Bit	Bit Name	Initial Value	R/W	Description
28	MSTP128	1	R/W	Module Stop bit 128 Controls clock supply to VEU0 0: VEU0 operates 1: Clock supply to VEU0 halted
27	MSTP127	1	R/W	Module Stop bit 127 Controls clock supply to CEU 0: CEU operates 1: Clock supply to CEU halted
26	MSTP126	1	R/W	Module Stop bit 126 Controls clock supply to CSI2 RX 0: CSI2 RX operates 1: Clock supply to CSI2 RX halted
25	MSTP125	1	R/W	Module Stop bit 125 Controls clock supply to TMU0 0: TMU0 operates 1: Clock supply to TMU0 halted
24	MSTP124	1	R/W	Module Stop bit 124 Controls clock supply to CMT0 0: CMT0 operates 1: Clock supply to CMT0 halted
23 to 19	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.
18	MSTP118	1	R	Module Stop bit 118 Controls clock supply to DSI TX Link 0: DSI TX Link operates 1: Clock supply to DSI TX Link halted
17	MSTP117	1	R	Module Stop bit 117 Controls clock supply to LCDC1 0: LCDC1 operates 1: Clock supply to LCDC1 halted

Bit	Bit Name	Initial Value	R/W	Description
16	MSTP116	1	R/W	Module Stop bit 116 Controls clock supply to IIC0 0: IIC0 operates 1: Clock supply to IIC0 halted
15	MSTP115	1	R/W	Module Stop bit 115 Controls clock supply to 2D-DMAC 0: 2D-DMAC operates 1: Clock supply to 2D-DMAC halted
14	—	1	R	Reserved These bits are always read as 1. The write value should always be 1.
13	MSTP113	1	R/W	Module Stop bit 113 Controls clock supply to MERAM 0: MERAM operates 1: Clock supply to MERAM halted
12	MSTP112	1	R/W	Module Stop bit 112 Controls clock supply to SGX540 0: SGX540 operates 1: Clock supply to SGX540 halted
11	MSTP111	1	R/W	Module Stop bit 111 Controls clock supply to TMU1 0: TMU1 operates 1: Clock supply to TMU1 halted
10	—	1	R	Reserved These bits are always read as 1. The write value should always be 1.
9	MSTP109	1	R/W	Module Stop bit 109 Controls clock supply to TSIF1 0: TSIF1 operates 1: Clock supply to TSIF1 halted

Bit	Bit Name	Initial Value	R/W	Description
8	MSTP108	1	R/W	Module Stop bit 108 Controls clock supply to TSIF0 0: TSIF0 operates 1: Clock supply to TSIF0 halted
7	—	1	R	Reserved These bits are always read as 1. The write value should always be 1.
6	MSTP106	1	R/W	Module Stop bit 106 Controls clock supply to JPU 0: JPU operates 1: Clock supply to JPU halted
5	MSTP105	1	R/W	Module Stop bit 105 Controls clock supply to JPU6E 0: JPU6E operates 1: Clock supply to JPU6E halted
4	MSTP104	1	R/W	Module Stop bit 104 Controls clock supply to BEU2 0: BEU2 operates 1: Clock supply to BEU2 halted
3	MSTP103	1	R/W	Module Stop bit 103 Controls clock supply to BEU1 0: BEU1 operates 1: Clock supply to BEU1 halted
2	MSTP102	1	R/W	Module Stop bit 102 Controls clock supply to BEU0 0: BEU0 operates 1: Clock supply to BEU0 halted
1	MSTP101	1	R/W	Module Stop bit 101 Controls clock supply to VPU 0: VPU operates 1: Clock supply to VPU halted

Bit	Bit Name	Initial Value	R/W	Description
0	MSTP100	1	R/W	Module Stop bit 100 Controls clock supply to LCDC0 0: LCDC0 operates 1: Clock supply to LCDC0 halted

11.5.32 Module Stop Control Register 2 (RMSTPCR2/ SMSTPCR2)

RMSTPCR2, SMSTPCR2 is a 32-bit readable/ writable register that individually starts or stops the module assigned to each bit. RMSTPCR2 and SMSTPCR2 assume the control from corresponding RT-CPU and SYS-CPU. It enters the state of the module stop when both of RMSTPCR2 and SMSTPCR2 settings are stops. The module stop is displayed in MSTPSR2. MSTPCR2 can be accessed only in longwords.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	MSTP 229	MSTP 228	-	MSTP 226	MSTP 225	MSTP 224	MSTP 223	MSTP 222	-	-	-	MSTP 218	MSTP 217	MSTP 216
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSTP 215	MSTP 214	MSTP 213	MSTP 212	-	MSTP 210	MSTP 209	MSTP 208	MSTP 207	MSTP 206	MSTP 205	MSTP 204	MSTP 203	MSTP 202	MSTP 201	MSTP 2000
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29	MSTP 229	0	R/W	Module Stop bit 229 Controls clock supply to INTCA 0: INTCA operates 1: Clock supply to INTCA halted

Bit	Bit Name	Initial Value	R/W	Description
28	MSTP228	0	R/W	Module Stop bit 228 Controls clock supply to Crypt 0: Crypt operates 1: Clock supply to Crypt halted
27	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
26	MSTP226	0	R/W	Module Stop bit 226 Controls clock supply to BBIF1 0: BBIF1 operates 1: Clock supply to BBIF1 halted
25	MSTP225	0	R/W	Module Stop bit 225 Controls clock supply to BBIF2 0: BBIF2 operates 1: Clock supply to BBIF2 halted
24	MSTP224	0	R/W	Module Stop bit 224 Controls clock supply to VOSYNC 0: VOSYNC operates 1: Clock supply to VOSYNC halted
23	MSTPST223	0	R/W	Module Stop bit 223 Controls clock supply to SPU 0: SPU operates 1: Clock supply to SPU halted
22	MSTP222	0	R/W	Module Stop bit 222 Controls clock supply to MISTY 0: MISTY operates 1: Clock supply to MISTY halted
21 to 19	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
18	MSTP218	0	R/W	Module Stop bit 218 Controls clock supply to SY-DMAC1 0: SY-DMAC1 operates 1: Clock supply to SY-DMAC1 halted
17	MSTP217	0	R/W	Module Stop bit 217 Controls clock supply to SY-DMAC2 0: SY-DMAC2 operates 1: Clock supply to SY-DMAC2 halted
16	MSTP216	0	R/W	Module Stop bit 216 Controls clock supply to SY-DMAC3 0: SY-DMAC3 operates 1: Clock supply to SY-DMAC3halted
15	MSTP215	0	R/W	Module Stop bit 215 Controls clock supply to DDM 0: DDM operates 1: Clock supply to DDM halted
14	MSTP214	0	R/W	Module Stop bit 214 Controls clock supply to USB-DMAC 0: USB-DMAC operates 1: Clock supply to USB-DMAC halted
13	MSTP213	0	R/W	Module Stop bit 213 Controls clock supply to MFIS 0: MFIS operates 1: Clock supply to MFIS halted
12	MSTP212	0	R/W	Module Stop bit 212 Controls clock supply to MFIM 0: MFIM operates 1: Clock supply to MFIM halted
11	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
10	MSTP210	0	R/W	Module Stop bit 210 Controls clock supply to MMFROM 0: MMFROM operates 1: Clock supply to MMFROM halted
9	MSTP209	0	R/W	Module Stop bit 209 Controls clock supply to SMFRAM 0: SMFRAM operates 1: Clock supply to SMFRAM halted
8	MSTP208	0	R/W	Module Stop bit 208 Controls clock supply to MSIOF1 0: MSIOF1 operates 1: Clock supply to MSIOF1 halted
7	MSTP207	0	R/W	Module Stop bit 207 Controls clock supply to SCIFA5 0: SCIFA5 operates 1: Clock supply to SCIFA5 halted
6	MSTP206	0	R/W	Module Stop bit 206 Controls clock supply to SCIFB 0: SCIFB operates 1: Clock supply to SCIFB halted
5	MSTP205	0	R/W	Module Stop bit 205 Controls clock supply to MSIOF2 0: MSIOF2 operates 1: Clock supply to MSIOF2 halted
4	MSTP204	0	R/W	Module Stop bit 204 Controls clock supply to SCIFA0 0: SCIFA0 operates 1: Clock supply to SCIFA0 halted
3	MSTP203	0	R/W	Module Stop bit 203 Controls clock supply to SCIFA1 0: SCIFA1 operates 1: Clock supply to SCIFA1 halted

Bit	Bit Name	Initial Value	R/W	Description
2	MSTP202	0	R/W	Module Stop bit 202 Controls clock supply to SCIFA2 0: SCIFA2 operates 1: Clock supply to SCIFA2 halted
1	MSTP201	0	R/W	Module Stop bit 201 Controls clock supply to SCIFA3 0: SCIFA3 operates 1: Clock supply to SCIFA3 halted
0	MSTP200	0	R/W	Module Stop bit 200 Controls clock supply to SCIFA4 0: SCIFA4 operates 1: Clock supply to SCIFA4 halted

11.5.33 Module stop control register 3 (RMSTPCR3/ SMSTPCR3)

RMSTPCR3, SMSTPCR3 is a 32-bit readable/ writable register that individually starts or stops the module assigned to each bit. RMSTPCR3 and SMSTPCR3 assume the control from corresponding RT-CPU and SYS-CPU. It enters the state of the module stop when both of RMSTPCR3 and SMSTPCR3 settings are stops. The module stop is displayed in MSTPSR2. MSTPCR3 can be accessed only in longwords.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	MSTP 329	MSTP 328	MSTP 327	MSTP 326	MSTP 325	-	MSTP 323	MSTP 322	MSTP 321	-	-	-	-	MSTP 316
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSTP 315	MSTP 314	MSTP 313	MSTP 312	-	-	-	MSTP 308	-	-	-	MSTP 304	-	-	-	-
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R	R/W	R	R/W	R	R	R	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 30	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.
29	MSTP 329	1	R/W	Module Stop bit 329 Controls clock supply to CMT1 0: CMT1 operates 1: Clock supply to CMT1 halted
28	MSTP 328	1	R/W	Module Stop bit 328 Controls clock supply to FSI 0: FSI operates 1: Clock supply to FSI halted

Bit	Bit Name	Initial Value	R/W	Description
27	MSTP327	1	R/W	Module Stop bit 327 Controls clock supply to FMSI 0: FMSI operates 1: Clock supply to FMSI halted
26	—	1	R	Reserved These bits are always read as 1. The write value should always be 1.
25	MSTP325	1	R/W	Module Stop bit 325 Controls clock supply to IrDA 0: IrDA operates 1: Clock supply to IrDA halted
24	—	1	R	Reserved These bits are always read as 1. The write value should always be 1.
23	MSTP323	1	R/W	Module Stop bit 323 Controls clock supply to IIC1 0: IIC1 operates 1: Clock supply to IIC1 halted
22	MSTP322	1	R/W	Module Stop bit 322 Controls clock supply to USB 0: USB operates 1: Clock supply to USB halted
21	MSTP321	1	R/W	Module Stop bit 321 Controls clock supply to SBSC1 performance monitor 0: SBSC1 performance monitor operates 1: Clock supply to SBSC1 performance monitor halted
20 to 17	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.

Bit	Bit Name	Initial Value	R/W	Description
16	MSTP316	1	R/W	Module Stop bit 316 Controls clock supply to SHWYSTAT 0: SHWYSTAT operates 1: Clock supply to SHWYSTAT halted
15	MSTP315	1	R/W	Module Stop bit 315 Controls clock supply to FLCTL 0: FLCTL operates 1: Clock supply to FLCTL halted
14	MSTP314	1	R/W	Module Stop Status 314 Displays clock supply status of SDHI0 0: SDHI0 operates 1: Clock supply to SDHI0 halted
13	MSTP313	1	R/W	Module Stop bit 314 Controls clock supply to SDHI0 0: SDHI0 operates 1: Clock supply to SDHI0 halted
12	MSTPST312	1	R/W	Module Stop bit 312 Controls clock supply to MMC 0: MMC operates 1: Clock supply to MMC halted
11 to 9	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.
8	MSTP308	1	R/W	Module Stop bit 308 Controls clock supply to MFIM MERAM Access function 0: MFIM MERAM Access function operates 1: Clock supply to MFIM MERAM Access function halted
7 to 5	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.

Bit	Bit Name	Initial Value	R/W	Description
4	MSTP304	1	R/W	Module Stop bit 304 Controls clock supply to TPU0 0: TPU0 operates 1: Clock supply to TPU0 halted
3 to 0	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.

11.5.34 Module stop control register 4 (RMSTPCR4/ SMSTPCR4)

RMSTPCR4, SMSTPCR4 is a 32-bit readable/ writable register that individually starts or stops the module assigned to each bit. RMSTPCR4 and SMSTPCR4 assume the control from corresponding RT-CPU and SYS-CPU. It enters the state of the module stop when both of RMSTPCR4 and SMSTPCR4 settings are stops. The module stop is displayed in MSTPSR4. MSTPCR4 can be accessed only in longwords.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	MSTP 429	MSTP 428	MSTP 427	MSTP 426	MSTP 425	MSTP 424	MSTP 423	MSTP 422	MSTP 421	-	-	-	-	-
Initial value:	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSTP 415	MSTP 414	MSTP 413	MSTP 412	MSTP 411	MSTP 410	MSTP 409	MSTP 408	MSTP 407	MSTP 406	MSTP 405	MSTP 404	MSTP 403	MSTP 402	-	MSTP 400
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 30	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.
29	MSTP 429	1	R/W	Module Stop bit 429 Controls clock supply to SDENC DAC 0: SDENC DAC operates 1: Clock supply to SDENC DAC halted
28	MSTP 428	1	R/W	Module Stop bit 428 Controls clock supply to SDENC 0: SDENC operates 1: Clock supply to SDENC halted

Bit	Bit Name	Initial Value	R/W	Description
27	MSTP427	1	R/W	Module Stop bit 427 Controls clock supply to ISP 0: ISP operates 1: Clock supply to ISP halted
26	MSTP426	1	R/W	Module Stop bit 426 Controls clock supply to ISP (CAMIF) 0: ISP (CAMIF) operates 1: Clock supply to ISP (CAMIF) halted
25	MSTP425	1	R/W	Module Stop bit 425 Controls clock supply to ISP (CMOSIF) 0: ISP (CMOSIF) operates 1: Clock supply to ISP (CMOSIF) halted
24	MSTP424	1	R/W	Module Stop bit 424 Controls clock supply to ISP (JG) 0: ISP (JG) operates 1: Clock supply to ISP (JG) halted
23	MSTP423	1	R/W	Module Stop bit 423 Controls clock supply to DSI TX1 0: DSI TX1 Link operates 1: Clock supply to DSI TX1 Link halted
22	MSTP422	0	R/W	Module Stop bit 422 Controls clock supply to ACMFI1 0: ACMFI1 operates 1: Clock supply to ACMFI1 halted
21	MSTP421	0	R/W	Module Stop bit 421 Controls clock supply to ACMFI2 0: ACMFI2 operates 1: Clock supply to ACMFI2 halted
20 to 16	—	All 0	R	Reserved

Bit	Bit Name	Initial Value	R/W	Description
15	MSTP415	0	R/W	Module Stop bit 415 Controls clock supply to SDHI2 0: SDHI2 operates 1: Clock supply to SDHI2 halted
14	MSTP314	0	R/W	Module Stop bit 414 Controls clock supply to MIPI-HSI 0: MIPI-HSI operates 1: Clock supply to MIPI-HSI halted
13	MSTP413	0	R/W	Module Stop bit 413 Controls clock supply to HDMI 0: HDMI operates 1: Clock supply to HDMI halted
12	MSTP412	0	R/W	Module Stop bit 412 Controls clock supply to CEC 0: CEC operates 1: Clock supply to CEC halted
11	MSTP411	0	R/W	Module Stop bit 411 Controls clock supply to IIC3 0: IIC3 operates 1: Clock supply to IIC3 halted
10	MSTP410	0	R/W	Module Stop bit 410 Controls clock supply to IIC4 0: IIC4 operates 1: Clock supply to IIC4 halted
9	MSTP409	0	R/W	Module Stop bit 409 Controls clock supply to ACMFI1/ACMFI2 RAM 0: ACMFI1/ACMFI2 RAM operates 1: Clock supply to ACMFI1/ACMFI2 RAM halted
8	MSTP408	0	R/W	Module Stop bit 408 Controls clock supply to SIB(ACMFI1/ACMFI2) 0: SIB(ACMFI1/ACMFI2) operates 1: Clock supply to SIB(ACMFI1/ACMFI2) halted

Bit	Bit Name	Initial Value	R/W	Description
7	MSTP407	0	R/W	Module Stop bit 407 Controls clock supply to USB DMAC1 0: USB DMAC1 operates 1: Clock supply to USB DMAC1 halted
6	MSTP406	0	R/W	Module Stop bit 406 Controls clock supply to USB1 0: USB1 operates 1: Clock supply to USB1 halted
5	MSTP405	0	R/W	Module Stop bit 405 Controls clock supply to CMT4 0: CMT4 operates 1: Clock supply to CMT4 halted
4	MSTP404	0	R/W	Module Stop bit 404 Controls clock supply to CMT3 0: CMT3 operates 1: Clock supply to CMT3 halted
3	MSTP403	0	R/W	Module Stop bit 403 Controls clock supply to KEYSC 0: KEYSC operates 1: Clock supply to KEYSC halted
2	MSTP402	0	R/W	Module Stop bit 402 Controls clock supply to RWDT0 0: RWDT0 operates 1: Clock supply to RWDT0 halted
1	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	MSTP400	0	R/W	Module Stop bit 400 Controls clock supply to CMT2 0: CMT2 operates 1: Clock supply to CMT2 halted

11.5.35 Software Reset Register 0 (SRCR0)

SRCR0 is a 32-bit readable/writable register. Each bit is assigned to a module in the system domain. Writing 1 to a bit resets the corresponding module and writing 0 cancels the reset. After writing 1 to a software reset bit in this register, wait for at least one EXTALR cycle before writing 0 to cancel the reset. Before applying a software reset to a module connected to the SHwy, be sure to stop data transfer to the module.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RTSRT	SRT030	-	-	-	-	-	-	SRT023	SRT022	SRT021	-	SRT019	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R	R	R	R	R	R/W	R/W	R/W	R	R/W	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	SRT007	-	-	-	-	-	SRT001	SRT000
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	RTSRT	0	R/W	Realtime Domain Software bit Issues the reset to RT domain (A3RV, A3RI, A4R) 0: RT domain operates 1: Issues the reset to RT domain
30	SRT030	0	R/W	Software Reset bit 030 Issues the reset to RT-CPU 0: RT-CPU operates 1: Issues the reset to RT-CPU
29 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
23	SRT023	0	R/W	Software Reset bit 023 Issues the reset to RT-DMAC2 0: RT-DMAC2 operates 1: Issues the reset to RT-DMAC2
22	SRT022	0	R/W	Software Reset bit 022 Issues the reset to INTCS 0: INTCS operates 1: Issues the reset to INTCS
21	SRT021	0	R/W	Software Reset bit 021 Issues the reset to RT-DMAC1 0: RT-DMAC1 operates 1: Issues the reset to RT-DMAC1
20	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
19	SRT019	0	R	Software Reset bit 019 Issues the reset to H-UDI 0: H-UDI operates 1: Issues the reset to H-UDI

Bit	Bit Name	Initial Value	R/W	Description
18 to 8	SRT018	0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	SRT007	0	R/W	Software Reset Bit 007 When this bit is set to 1, the ICB is reset. 0: Starts ICB operation 1: Resets ICB
6 to 2	SRT018	0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	SRT001	0	R/W	Software Reset bit 001 Issues the reset to ICB 0: IIC2 operates 1: Issues the reset to IIC2
0	SRT000	0	R/W	Software Reset bit 000 Issues the reset to MSIOF0 0: MSIOF0 operates 1: Issues the reset to MSIOF0

11.5.36 Software Reset Register 1 (SRCR1)

SRCR1 is a 32-bit readable/writable register. Each bit is assigned to a module in the system domain. Writing 1 to a bit resets the corresponding module and writing 0 cancels the reset. After writing 1 to a software reset bit in this register, wait for at least one EXTALR cycle before writing 0 to cancel the reset. Before applying a software reset to a module connected to the SHwy, be sure to stop data transfer to the module.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SRT 131	SRT 130	SRT 129	SRT 128	SRT 127	SRT 126	SRT 125	SRT 124	-	-	-	-	-	SRT 118	SRT 117	SRT 116
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SRT 115	-	SRT 113	SRT 112	SRT 111	-	SRT 109	SRT 108	-	SRT 106	SRT 105	SRT 104	SRT 103	SRT 102	SRT 101	SRT 100
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	SRT131	0	R/W	Software Reset bit 131 Issues the reset to VEU3 0: VEU3 operates 1: Issues the reset to VEU3
30	SRT130	0	R/W	Software Reset bit 130 Issues the reset to VEU2 0: VEU2 operates 1: Issues the reset to VEU2

Bit	Bit Name	Initial Value	R/W	Description
29	SRT129	0	R/W	Software Reset bit 129 Issues the reset to VEU1 0: VEU1 operates 1: Issues the reset to VEU1 0: Starts VEU1 operation 1: Stops clock supply to VEU1
28	SRT128	0	R/W	Software Reset bit 128 Issues the reset to VEU0 0: VEU0 operates 1: Issues the reset to VEU0
27	SRT127	0	R/W	Software Reset bit 127 Issues the reset to CEU 0: CEU operates 1: Issues the reset to CEU
26	SRT126	0	R/W	Software Reset bit 126 Issues the reset to CSI2 RX 0: CSI2 RX operates 1: Issues the reset to CSI2 RX
25	SRT125	0	R/W	Software Reset bit 125 Issues the reset to TMU0 0: TMU0 operates 1: Issues the reset to TMU0
24	SRT125	0	R/W	Software Reset bit 124 Issues the reset to CMT0 0: CMT0 operates 1: Issues the reset to CMT0
23 to 19	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
18	SRT118	0	R/W	Software Reset bit 118 Issues the reset to DSI TX Link 0: DSI TX Link operates 1: Issues the reset to DSI TX Link

Bit	Bit Name	Initial Value	R/W	Description
17	SRT117	0	R/W	Software Reset bit 117 Issues the reset to LCDC1 0: LCDC1 operates 1: Issues the reset to LCDC1
16	SRT116	0	R/W	Software Reset bit 116 Issues the reset to IIC0 0: IIC0 operates 1: Issues the reset to IIC0
15	SRT115	0	R/W	Software Reset bit 115 Issues the reset to 2D-DMAC 0: 2D-DMAC operates 1: Issues the reset to 2D-DMAC
14	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
13	SRT113	0	R/W	Software Reset bit 113 Issues the reset to MERAM 0: MERAM operates 1: Issues the reset to MERAM
12	SRT112	0	R/W	Software Reset bit 112 Issues the reset to SGX540 0: SGX540 operates 1: Issues the reset to SGX540
11	SRT111	0	R/W	Software Reset bit 111 Issues the reset to TMU1 0: TMU1 operates 1: Issues the reset to TMU1
10	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
9	SRT109	0	R/W	Software Reset bit 109 Issues the reset to TSIF1 0: TSIF1 operates 1: Issues the reset to TSIF1
8	SRT108	0	R/W	Software Reset bit 108 Issues the reset to TSIF0 0: TSIF0 operates 1: Issues the reset to TSIF0
7	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
6	SRT106	0	R/W	Software Reset bit 106 Issues the reset to JPU 0: JPU operates 1: Issues the reset to JPU
5	SRT105	0	R/W	Software Reset bit 105 Issues the reset to JPU6E 0: JPU6E operates 1: Issues the reset to JPU6E
4	SRT104	0	R/W	Software Reset bit 104 Issues the reset to BEU2 0: BEU2 operates 1: Issues the reset to BEU2
3	SRT103	0	R/W	Software Reset bit 103 Issues the reset to BEU1 0: BEU1 operates 1: Issues the reset to BEU1
2	SRT102	0	R/W	Software Reset bit 102 Issues the reset to BEU0 0: BEU0 operates 1: Issues the reset to BEU0

Bit	Bit Name	Initial Value	R/W	Description
1	SRT101	0	R/W	Software Reset bit 101 Issues the reset to VPU 0: VPU operates 1: Issues the reset to VPU
0	SRT100	0	R/W	Software Reset bit 100 Issues the reset to LCDC0 0: LCDC0 operates 1: Issues the reset to LCDC0

11.5.37 Software Reset Register 2 (SRCR2)

SRCR2 is a 32-bit readable/writable register. Each bit is assigned to a module in the system domain. Writing 1 to a bit resets the corresponding module and writing 0 cancels the reset. After writing 1 to a software reset bit in this register, wait for at least one EXTALR cycle before writing 0 to cancel the reset. Before applying a software reset to a module connected to the SHwy, be sure to stop data transfer to the module.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SRT 231	-	SRT 229	SRT 228	-	SRT 226	SRT 225	SRT 224	SRT 224	SRT 224	-	-	-	SRT 218	SRT 217	SRT 216
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SRT 215	SRT 213	SRT 213	SRT 212	-	-	-	SRT 208	SRT 208	SRT 206	SRT 205	SRT 204	SRT 203	SRT 202	SRT 201	SRT 200
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	SYSRT	0	R/W	System Domain Software bit Issues the reset to SY domain (A3SM, A3SG, A3SP, A4S) 0: SY domain operates 1: Issues the reset to SY domain
30	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
29	SRT229	0	R/W	Software Reset bit 229 Issues the reset to INTCA 0: INTCA operates 1: Issues the reset to INTCA

Bit	Bit Name	Initial Value	R/W	Description
28	SRT228	0	R/W	System Module Stop Bit 028 When this bit is set to 1, the clock supply to the Crypt is stopped. 0: Starts Crypt operation 1: Stops clock supply to Crypt
27	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
26	SRT226	0	R/W	System Module Stop Bit 026 When this bit is set to 1, the clock supply to the BBIF1 is stopped. 0: Starts BBIF1 operation 1: Stops clock supply to BBIF1
25	SRT225	0	R/W	System Module Stop Bit 025 When this bit is set to 1, the clock supply to the BBIF2 is stopped. 0: Starts BBIF2 operation 1: Stops clock supply to BBIF2
24	SRT224	0	R/W	Reserved These bits are always read as 0. The write value should always be 0.
23	SRT223	0	R/W	System Module Stop Bit 023 When this bit is set to 1, the clock supply to the SPU is stopped. 0: Starts SPU operation 1: Stops clock supply to SPU
22	SRT222	0	R/W	System Module Stop Bit 022 When this bit is set to 1, the clock supply to the MISTY is stopped. 0: Starts MISTY operation 1: Stops clock supply to MISTY
21 to 19	—	All 0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
18	SRT218	0	R/W	Software Reset bit 218 Issues the reset to SY-DMAC1 0: SY-DMAC1 operates 1: Issues the reset to SY-DMAC1
17	SRT217	0	R/W	Software Reset bit 217 Issues the reset to SY-DMAC2 0: SY-DMAC2 operates 1: Issues the reset to SY-DMAC2
16	SRT216	0	R/W	Software Reset bit 216 Issues the reset to SY-DMAC3 0: SY-DMAC3 operates 1: Issues the reset to SY-DMAC3
15	SRT215	0	R/W	Software Reset bit 215 Issues the reset to DDM 0: DDM operates 1: Issues the reset to DDM
14	SRT214	0	R/W	Software Reset bit 214 Issues the reset to USB-DMAC 0: USB-DMAC operates 1: Issues the reset to USB-DMAC
13	SRT213	0	R/W	Software Reset bit 213 Issues the reset to MFIS 0: MFIS operates 1: Issues the reset to MFIS
12	SRT212	0	R/W	Software Reset bit 212 Issues the reset to MFIM 0: MFIM operates 1: Issues the reset to MFIM
11 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
8	SRT208	0	R/W	Software Reset bit 208 Issues the reset to MSIOF1 0: MSIOF1 operates 1: Issues the reset to MSIOF1
7	SRT207	0	R/W	Software Reset bit 207 Issues the reset to SCIFA5 0: SCIFA5 operates 1: Issues the reset to SCIFA5
6	SRT206	0	R/W	Software Reset bit 206 Issues the reset to SCIFB 0: SCIFB operates 1: Issues the reset to SCIFB
5	SRT205	0	R/W	Software Reset bit 205 Issues the reset to MSIOF2 0: MSIOF2 operates 1: Issues the reset to MSIOF2
4	SRT204	0	R/W	Software Reset bit 204 Issues the reset to SCIFA0 0: SCIFA0 operates 1: Issues the reset to SCIFA0
3	SRT203	0	R/W	Software Reset bit 203 Issues the reset to SCIFA1 0: SCIFA1 operates 1: Issues the reset to SCIFA1
2	SRT202	0	R/W	Software Reset bit 202 Issues the reset to SCIFA2 0: SCIFA2 operates 1: Issues the reset to SCIFA2
1	SRT201	0	R/W	Software Reset bit 201 Issues the reset to SCIFA3 0: SCIFA3 operates 1: Issues the reset to SCIFA3

Bit	Bit Name	Initial Value	R/W	Description
0	SRT200	0	R/W	Software Reset bit 200 Issues the reset to SCIFA4 0: SCIFA4 operates 1: Issues the reset to SCIFA4

11.5.38 Software Reset Register 3 (SRCR3)

SRCR3 is a 32-bit readable/writable register. Each bit is assigned to a module in the system domain. Writing 1 to a bit resets the corresponding module and writing 0 cancels the reset. After writing 1 to a software reset bit in this register, wait for at least one EXTALR cycle before writing 0 to cancel the reset. Before applying a software reset to a module connected to the SHwy, be sure to stop data transfer to the module.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	SRT329	SRT328	SRT327	SRT326	SRT325	-	SRT324	SRT324	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SRT315	SRT313	SRT313	SRT312	-	-	-	-	-	-	-	SRT304	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R/W	R	R	R	R	R	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31,30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29	SRT329	0	R/W	Software Reset bit 329 Issues the reset to CMT1 0: CMT1 operates 1: Issues the reset to CMT1
28	SRT328	0	R/W	Software Reset bit 328 Issues the reset to FSI 0: FSI operates 1: Issues the reset to FSI

Bit	Bit Name	Initial Value	R/W	Description
27	SRT327	0	R/W	Software Reset bit 327 Issues the reset to FMSI 0: FMSI operates 1: Issues the reset to FMSI This bit is always read as 1. The write value should always be 1.
26	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
25	SRT325	0	R/W	Software Reset bit 325 Issues the reset to IrDA 0: IrDA operates 1: Issues the reset to IrDA
24	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
23	SRT323	0	R/W	Software Reset bit 323 Issues the reset to IIC1 0: IIC1 operates 1: Issues the reset to IIC1
22	SRT322	0	R/W	Software Reset bit 322 Issues the reset to USB 0: USB operates 1: Issues the reset to USB
21 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	SRT315	0	R/W	Software Reset bit 315 Issues the reset to FLCTL 0: FLCTL operates 1: Issues the reset to FLCTL

Bit	Bit Name	Initial Value	R/W	Description
14	SRT314	0	R/W	Software Reset bit 314 Issues the reset to SDHI0 0: SDHI0 operates 1: Issues the reset to SDHI0
13	SRT313	0	R/W	Software Reset bit 313 Issues the reset to SDHI1 0: SDHI1 operates 1: Issues the reset to SDHI1
12	SRT313	0	R/W	Software Reset bit 312 Issues the reset to MMC 0: MMC operates 1: Issues the reset to MMC
11 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	SRT304	0	R/W	Software Reset bit 304 Issues the reset to TPU0 0: TPU0 operates 1: Issues the reset to TPU0
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

11.5.39 Software Reset Register 4 (SRCR4)

SRCR4 is a 32-bit readable/writable register. Individual bits correspond to those modules in the common domain. When 1 is written, a module reset is issued. When 0 is written, the reset is canceled. When 1 has been written to the software reset bit in this register, a time equivalent to at least one cycle of EXTALR must be allowed before 0 is written to cancel the reset. If a software reset is applied to a module connected to SHwy, data transfer to the module must be stopped before the software reset.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	SRT 429	SRT 428	SRT 427	SRT 426	SRT 425	SRT 424	SRT 423	SRT 422	SRT 421	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SRT 415	SRT 413	SRT 413	SRT 412	SRT 411	SRT 410	-	SRT 408	SRT 407	SRT 406	SRT 405	SRT 404	SRT 403	SRT 402	-	SRT 400
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 , 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29	SRT429	0	R/W	Software Reset bit 429 Issues the reset to SDENC DAC 0: SDENC DAC operates 1: Issues the reset to SDENC DAC

Bit	Bit Name	Initial Value	R/W	Description
28	SRT428	0	R/W	Software Reset bit 428 Issues the reset to SDENC 0: SDENC operates 1: Issues the reset to SDENC
27	SRT427	0	R/W	Software Reset bit 427 Issues the reset to ISP 0: ISP operates 1: Issues the reset to ISP
26	SRT426	0	R/W	Software Reset bit 426 Issues the reset to ISP (CAMIF) 0: ISP (CAMIF) operates 1: Issues the reset to ISP (CAMIF)
25	SRT425	0	R/W	Software Reset bit 425 Issues the reset to ISP (CMOSIF) 0: ISP (CMOSIF) operates 1: Issues the reset to ISP (CMOSIF)
24	SRT424	0	R/W	Software Reset bit 424 Issues the reset to ISP (JG) 0: ISP (JG) operates 1: Issues the reset to ISP (JG)
23	SRT423	0	R/W	Software Reset bit 423 Issues the reset to DSI TX1 0: DSI TX1 Link operates 1: Issues the reset to DSI TX1 Link
22	SRT422	0	R/W	Software Reset bit 422 Issues the reset to ACMFI1 0: ACMFI1 operates 1: Issues the reset to ACMFI1
21	SRT421	0	R/W	Software Reset bit 421 Issues the reset to ACMFI2 0: ACMFI2 operates 1: Issues the reset to ACMFI2

Bit	Bit Name	Initial Value	R/W	Description
20 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	SRT415	0	R/W	Software Reset bit 415 Issues the reset to SDHI2 0: SDHI2 operates 1: Issues the reset to SDHI2
14	SRT414	0	R/W	Software Reset bit 414 Issues the reset to MIPI-HSI 0: MIPI-HSI operates 1: Issues the reset to MIPI-HSI
13	SRT413	0	R/W	Software Reset bit 413 Issues the reset to HDMI 0: HDMI operates 1: Issues the reset to HDMI
12	SRT412	0	R/W	Software Reset bit 412 Issues the reset to CEC 0: CEC operates 1: Issues the reset to CEC
11	SRT411	0	R/W	Software Reset bit 411 Issues the reset to IIC3 0: IIC3 operates 1: Issues the reset to IIC3
10	SRT410	0	R/W	Software Reset bit 410 Issues the reset to IIC4 0: IIC4 operates 1: Issues the reset to IIC4
9	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
8	SRT408	0	R/W	Software Reset bit 408 Issues the reset to SIB(ACMFI1/ACMFI2) 0: SIB(ACMFI1/ACMFI2) operates 1: Issues the reset to SIB(ACMFI1/ACMFI2)
7	SRT407	0	R/W	Software Reset bit 407 Issues the reset to USB DMAC1 0: USB DMAC1 operates 1: Issues the reset to USB DMAC1
6	SRT406	0	R/W	Software Reset bit 406 Issues the reset to USB1 0: USB1 operates 1: Issues the reset to USB1
5	SRT405	0	R/W	Software Reset bit 405 Issues the reset to CMT4 0: CMT4 operates 1: Issues the reset to CMT4
4	SRT404	0	R/W	Software Reset bit 404 Issues the reset to CMT3 0: CMT3 operates 1: Issues the reset to CMT3
3	SRT403	0	R/W	Software Reset bit 403 Issues the reset to KEYSC 0: KEYSC operates 1: Issues the reset to KEYSC
2	SRT402	0	R/W	Software Reset bit 402 Issues the reset to RWDT0 0: RWDT0 operates 1: Issues the reset to RWDT0
1	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
0	SRT400	0	R/W	Software Reset bit 400 Issues the reset to CMT2 0: CMT2 operates 1: Issues the reset to CMT2

11.5.40 Status Register (ASTAT)

ASTAT is a 32-bit read-only register that indicates the sleep or software standby state. ASTAT can be accessed only in longwords.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	SYCST	-	SYSLT	-	RTCST	-	RTSLP	-	-	-	-	-	-	-	-
Initial value:	-	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 15	—	Undefined	R	Reserved Undefined values are read from these bits.
14	SYCST	0	R	System Core Standby Status 0: Normal operation in the system core 1: System core standby state
13	—	0	R	Reserved This bit is always read as 0.
12	SYSLP	0	R	System Sleep Status 0: Normal operation in the system block 1: System sleep state
11	—	0	R	Reserved This bit is always read as 0.
10	RTCST	0	R	Realtime Core Standby Status 0: Normal operation in the realtime core 1: Realtime core standby state

Bit	Bit Name	Initial Value	R/W	Description
9	—	0	R	Reserved This bit is always read as 0.
8	RTSLP	0	R	Realtime Sleep Status 0: Normal operation in the realtime block 1: Realtime sleep state
7 to 0	—	Undefined	R	Reserved Undefined values are read from these bits.

11.5.41 Clock Source Control Register (CKSCR)

CKSCR is a 32-bit read-only register that controls the EXTAL2/XTAL2 input clocks. CKSCR can be accessed only in longwords.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	XTAL2	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0.
1	XTAL2	1	R/W	EXTAL2 Crystal Resonator Mode 0: EXTAL2 and XTAL2 are set to external supply mode 1: EXTAL2 and XTAL2 are set to crystal resonator mode
0	—	1	R	Reserved These bits are always read as 0.

11.5.42 VREF Control Register (VREFCR)

VREFCR is a 32-bit readable/writable register that controls the VREF1, VREF2, and VREF3. VREFCR can be accessed only in longwords.

VREFCR is a 32-bit readable/writable register.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	VREF3CR[3:0]		VREF2CR[3:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VREF1CR[3:0]		-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	1	0	1	0	0	0	1	0	1	0
R/W:	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 20	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
19,18	VREF3CR [3:0]	0	R/W	VREF3 pin control register 00 : Automatic control (High: A4S power on, Low: A4S power off) 10 : Low level 11 : High level other value: setting prohibited

Bit	Bit Name	Initial Value	R/W	Description
17,16	VREF2CR [3:0]	0	R/W	VREF2 pin control register 00 : Automatic control (High: A4S power on, Low: A4S power off) 10 : Low level 11 : High level other value: setting prohibited
15,14	VREF1CR [3:0]	0	R/W	VREF1 pin control register 00 : Automatic control (High: A4S power on, Low: A4S power off) 10 : Low level 11 : High level other value: setting prohibited
13 to 0	—	00001010001010	R	Reserved Please set read value of these bits at the time of write acccess to VREFCR.

11.6 Changing Frequency

The clock frequencies controlled by the frequency control registers can be changed either by changing the multiplication ratio of PLL circuits C0 and C1 or by changing the division ratio of the dividers. They are controlled by software through the frequency control registers. The methods are described below.

11.6.1 Changing Multiplication Ratio of PLL Circuit C0

Changing the multiplication ratio of PLL circuit 0 can be done by modifying the STC[5:0] bits in FRQCRC and writing 1 to the KICK bit in FRQCRB. The RWDT setting is not required because the PLL oscillation settling time is internally detected automatically.

11.6.2 Changing Multiplication Ratio of PLL Circuit C1

Changing the multiplication ratio of PLL circuit 1 can be done by modifying the STC[5:0] bits in FRQCRA and writing 1 to the KICK bit in FRQCR**B**. The RWDT setting is not required because the PLL oscillation settling time is internally detected automatically.

11.6.3 Changing Division Ratio

Changing the division ratio can be done by modifying each set of bits for setting the division ratio in FRQCRA, FRQCRB or FRQCRC and writing 1 to the KICK bit in FRQCRB. Before changing the division ratio, the KICK bit must be checked for 0. After 1 is written to the KICK bit in FRQCRB, 0 can be read if the setting change is completed. While the setting is being changed with the KICK bit being 1, no writing into FRQCRA, FRQCRB, or FRQCRC must be performed. When the KICK bit is 1, 0 must not be written into the KICK bit.

11.6.4 Turning On/Off of PLL Circuit C1

PLL circuits C0 and C1 can be turned on or off by modifying the PLL01E bit in PLLC01CR.

In the same way as multiplication ratio change for PLL circuits C0 andC1 or division ratio change the oscillation settling time of PLL circuits C0 and C1 is internally detected automatically.

11.6.5 Changing Multiplication Ratio of PLL Circuit C2

Change the multiplication ratio of PLL circuit C2 with the following procedure.

1. Check that the module that uses the clock is not operating.
2. Set the PLLE bit in PLLC2CR to 0 to reset PLL circuit C2.
3. Set the multiplication ratio in STC4 to STC0 in PLLC2CR.
4. Set 1 to the PLLE bit in PLLC2CR to oscillate PLL circuit C2.
5. If the oscillation of PLL circuit C2 is settled, 1 can be read into the PLLE bit in PLLC2CR. In this case, do not access the module using the clock of PLL circuit C2 until it becomes possible to read 1 into the PLLE bit in PLLC2CR.

11.6.6 Example of Activating PLL and Specifying Frequency Division and Multiplication Ratios

(1) Wait until FRQCRB bit31 (KICK bit) is cleared to 0.
(2) Set H'2D13 05C8 in FRQCRA.
(3) Set H'9E40 352E in FRQCRC.
(4) Set H'8033 1050 in FRQCRB.
(5) Wait until FRQCRB bit31 (KICK bit) is cleared to 0 (the division setting is completed).
(6) Set H'0000 2000 in FRQCRD.
(7) Wait until FRQCRD bit31 (DDRPCHG bit) is cleared to 0 (the division setting is completed).
(8) Set H'00004000 in PLLC01CR.
(9) Wait until PLLC01CR (PLLC01E bit) is set to 1 (the oscillation of PLL circuit C1 is settled).

Through these steps (1) to (14), the frequency of each system clock available when the clock input frequency of EXTAL1 is 26 MHz is determined as follows.

RT domain: Iϕ = 398.7 MHz, Bϕ = 99.7 MHz, M1ϕ = 170.9MHz, CSIRϕ = 49.8 MHz, ISPBϕ = 149.5MHz

SY domain: ZGϕ = 199.3HMz, ZTϕ = 199.3MHz, ZTRϕ = 199.3HMz, Zϕ = 806MHz, ZXϕ = 398.7 MHz, HPϕ = 99.7 MHz

Common domain: ZSϕ = 199.3 MHz, ZBϕ = 99.7 MHz, ZB3ϕ = 299.00 MHz, CPϕ = 12.5 MHz

11.6.7 Restrictions on Clock Ratio

The clock ratio specified by each frequency control register involves the restrictions shown in table 11.6.

Table 11.6 Restrictions on Clock Ratio

Domain	Clock	Clock Limitation	Clock Ratio	Setting Example
Realtime	Iϕ:ZSϕ	Integer clock ratio	Iϕ:ZSϕ = N:1 *	398.7MHz: 199.3MHz
		Inverted clock ratio	Iϕ:Sϕ = 1:N *	
	ZSϕ:Bϕ	Integer clock ratio	Sϕ:Bϕ = N:1 *	When CSI2 is used, the setting of ZSϕ:Bϕ=1:1 is prohibited.
	Iϕ:HPϕ	Integer clock ratio	Iϕ:HPϕ = N:1 *	
System	ZXϕ:ZSϕ	Integer clock ratio	ZXϕ:ZSϕ = N:1 *	398.7MHz : 199.3Hz
Realtime/ System	ZSϕ:HPϕ	Integer clock ratio	ZSϕ:HPϕ = N:1 *	
Common	ZSϕ:ZBϕ	Integer clock ratio	ZSϕ:ZBϕ = N:1 *	
Others	HPϕ:TCKϕ	Magnitude relation	HPϕ > TCK	

Note: * N = 16,12,8,4,3,2,1

11.7 Sleep Mode

11.7.1 Transition to SH-CPU Core Sleep Mode

Executing the SLEEP instruction in the SH-CPU core causes a transition from the program execution state to sleep mode. Although the SH-CPU core halts immediately after executing the SLEEP instruction, the contents of the SH-CPU core registers remain unchanged. The on-chip peripheral modules in the Realtime block continue to operate in sleep mode.

11.7.2 Canceling SH-CPU Core Sleep Mode

Sleep mode is canceled by an interrupt (software NMI, IRQ, or on-chip peripheral module in the Realtime block) or a reset.

Interrupts are accepted in sleep mode even when the BL bit in SR is 1. If necessary, save SPC and SSR in the stack before executing the SLEEP instruction.

11.7.3 Transition to System CPU Sleep Mode

Executing the WFI instruction in the system CPU causes a transition from the program execution state to system CPU sleep mode. Although the system CPU halts immediately after executing the WFI instruction, the contents of the system CPU registers remain unchanged. The on-chip peripheral modules in the System block continue to operate in sleep mode.

11.7.4 Canceling System CPU Sleep Mode

System CPU sleep mode is canceled by an interrupt (NMI, IRQ, or on-chip peripheral module in the System block) to the system CPU or a reset.

11.8 Core Standby Mode

11.8.1 Transition to SH-CPU Core Standby Mode

Executing the SLEEP instruction in the SH-CPU core when the CSTBY bit in RTSTBCR is 1 causes a transition from the program execution state to SH-CPU core standby mode. The SH-CPU core halts immediately after executing the SLEEP instruction. In core standby mode, the cache in the SH-CPU core enters RAM standby state and the power supply to the SH-CPU core logic is turned off. The on-chip peripheral modules in the Realtime block continue to operate in core standby mode.

11.8.2 Canceling SH-CPU Core Standby Mode

SH-CPU core standby mode is canceled by an interrupt (software NMI, IRQ, or on-chip peripheral module in the Realtime block) or a reset.

Interrupts are accepted in SH-CPU core standby mode even when the BL bit in SR is 1.

11.8.3 Transition to System CPU Core Standby Mode

Executing the WFI instruction in the system CPU when the CSTBY bit in SYSTBCR is 1 causes a transition from the program execution state to system CPU core standby mode. The system CPU halts immediately after executing the WFI instruction. In system CPU core standby mode, the cache in the system CPU enters RAM standby state and the power supply to the system CPU logic is turned off. The on-chip peripheral modules in the System block continue to operate in sleep mode.

11.8.4 Canceling System CPU Core Standby Mode

System CPU core standby mode is canceled by an interrupt (NMI, IRQ, or on-chip peripheral module in the System block) to the system CPU or a reset.

11.9 Module Standby Function

11.9.1 Transition to Module Standby State

Setting the MSTP bits in the module stop control registers to 1 stops the clock supply to the corresponding on-chip peripheral modules. This function can be used to reduce power consumption in normal mode.

Modules in module standby state keep the state immediately before the transition to the module standby state. The registers keep the contents before the clock supply is stopped, and the external pins keep the state before the clock supply is stopped. When the module standby state is canceled, operation is restarted from the condition immediately before the clock supply is stopped.

Note: Make sure to set the MSTP bit to 1 while the corresponding module has completed the operation and is in an idle state and no other module or external pin may activate the module.

11.9.2 Canceling Module Standby State

The module standby state can be canceled by clearing the respective MSTP bit to 0.

After clearing the respective MSTP bit, be sure to read the MSTP bit and check that the bit value has changed.

11.10 Music Player Mode

The power supply of the A4S area, PLLC0, PLLC1, and the clock signal input on the EXTAL1 pin are automatically controlled by the request from the SPU, which indicates the music player mode.

Set the MPMODE register to the following value according to the clocks used by the SPUϕ and SUBϕ.

— When SPUϕ and SUBϕ are generated from EXTAL2

The power supply of the A4S area, PLLC0, PLLC1, and the clock signal input on the EXTAL1 pin are automatically controlled by the request from the SPU.

CPGA.MPMODE = H'0000 0000

— When SPUϕ and SUBϕ are generated from the signal generated by dividing PLLC2 output and the PLLC2 input is generated by dividing EXTAL1 by two

The power supply of the A4S area, PLLC0, and PLLC1 are automatically controlled by the request from the SPU. The clock signal input on the EXTAL1 pin is not automatically controlled by the request from the SPU.

CPGA.MPMODE = H'0000 000A

Set the SYSC register to the following value to enable the control of the power supply of the A4S area and the clock signal input on the EXTAL1 pin by the SPU request.

SYSC.A4SPOWCR = H'0000 000C
SYSC.SYSCKENMSK = H'0000 0020

Clear the A4SSTP bit in the SYSC.APSCSTP register to 0 so that the clock signal input on the EXTAL1 pin is not disabled by power supply condition of the A4S area.

Example: SYSC.APSCSTP = H'0000 3822 (A3SG, A3SM, A3SP, A4R, A4LC)

The SPU request controls only PLLC1 by setting the PLLC0STP bit (bit 28) in the CPGA.PLLC01STPCR register to 1. PLLC0 is controlled by the power supply status of the A3SM area with the PLLC0STP bit set to 1.

Example: CPGA.PLLC01STPCR = H'1000 0400
(PLLC0 A3SM synchronization , PLLC1 A4S synchronization)

11.11 Clock Control

An outline of the control registers in CPGA and each AP clock control is explained.

11.11.1 Control of PLL Circuit C0 , PLL Circuit C1 and PLL Circuit C2

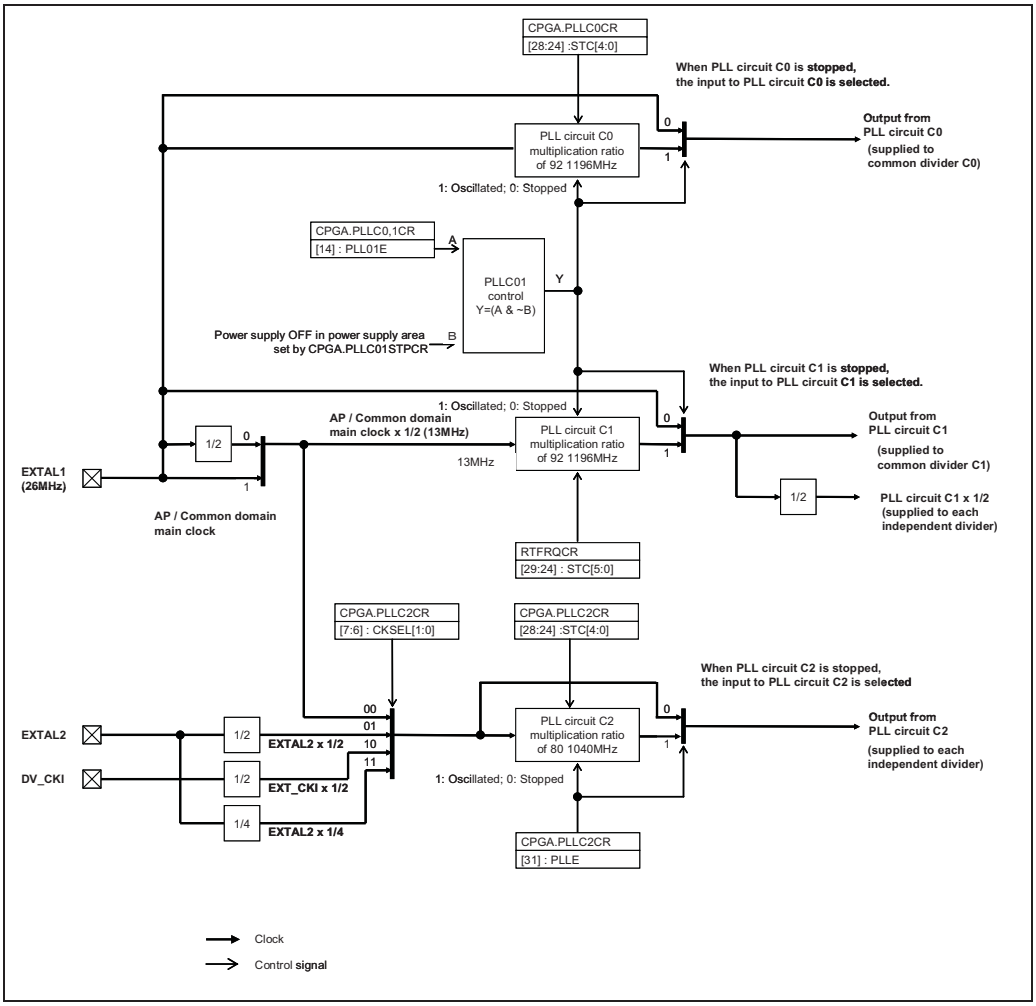


Figure 11.2 Control of PLL Circuit C0 , PLL Circuit C1 and PLL Circuit C2

11.11.2 Clock Control Related to Divider C0 and Divider C1

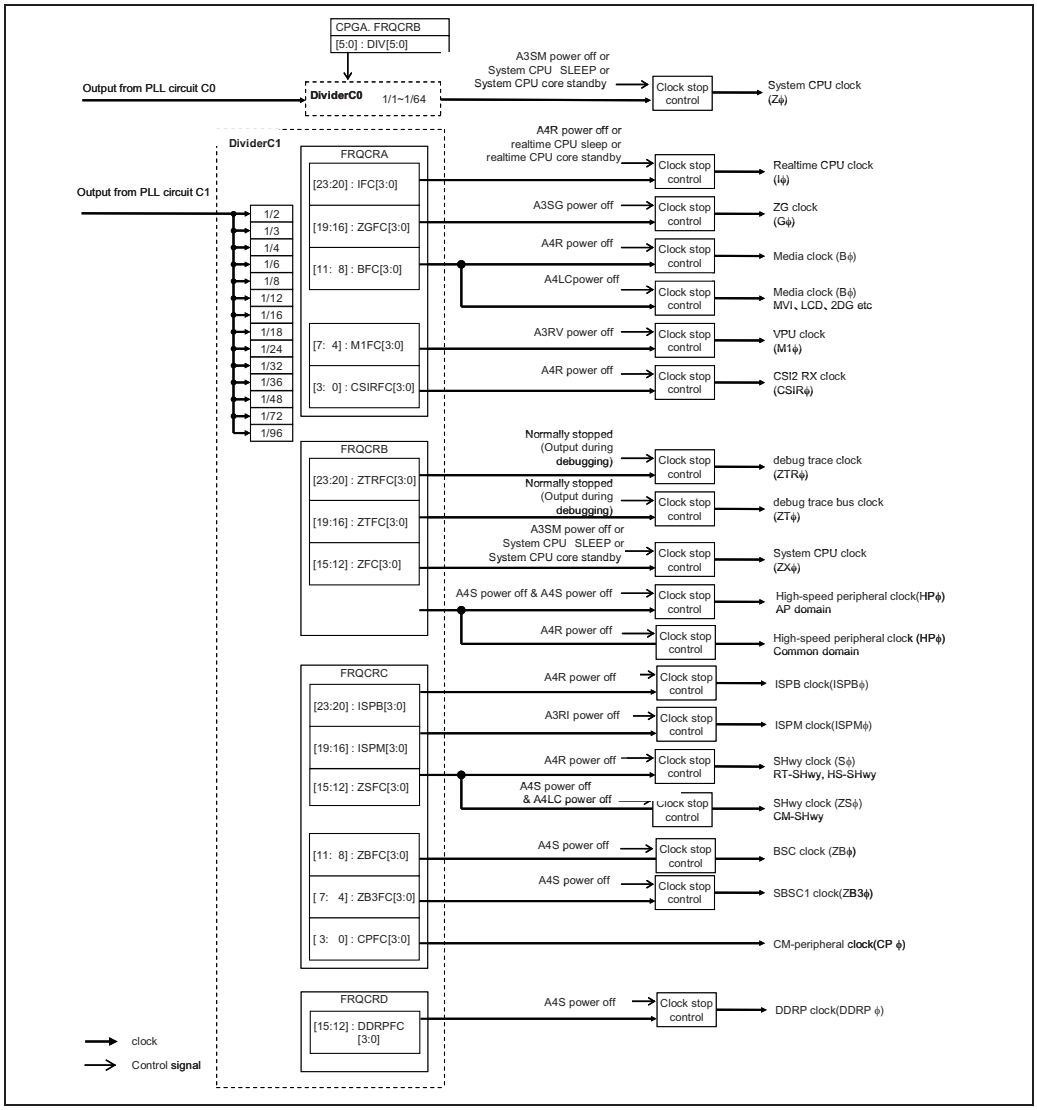


Figure 11.3 Clock Control Related to Divider C0 and Divider C1

11.11.3 Clock Control Related to Independent Divider

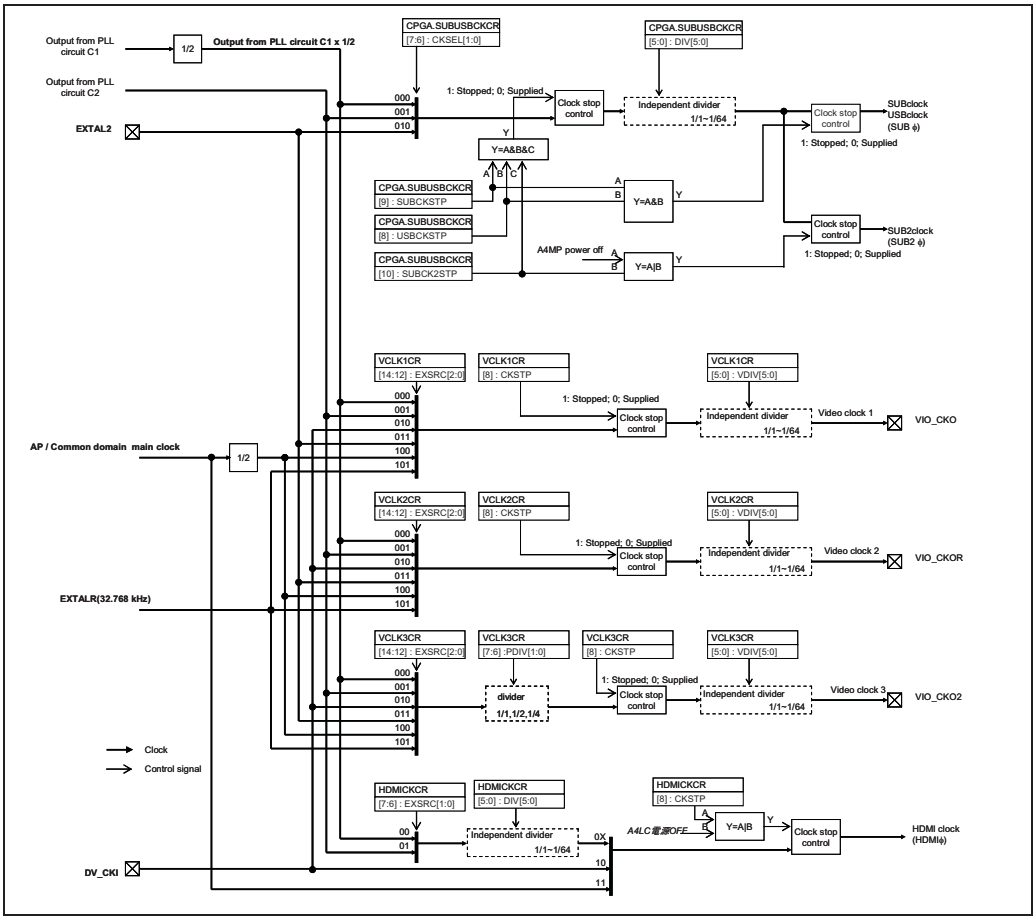


Figure 11.4 Clock Control Related to Independent Divider (1)

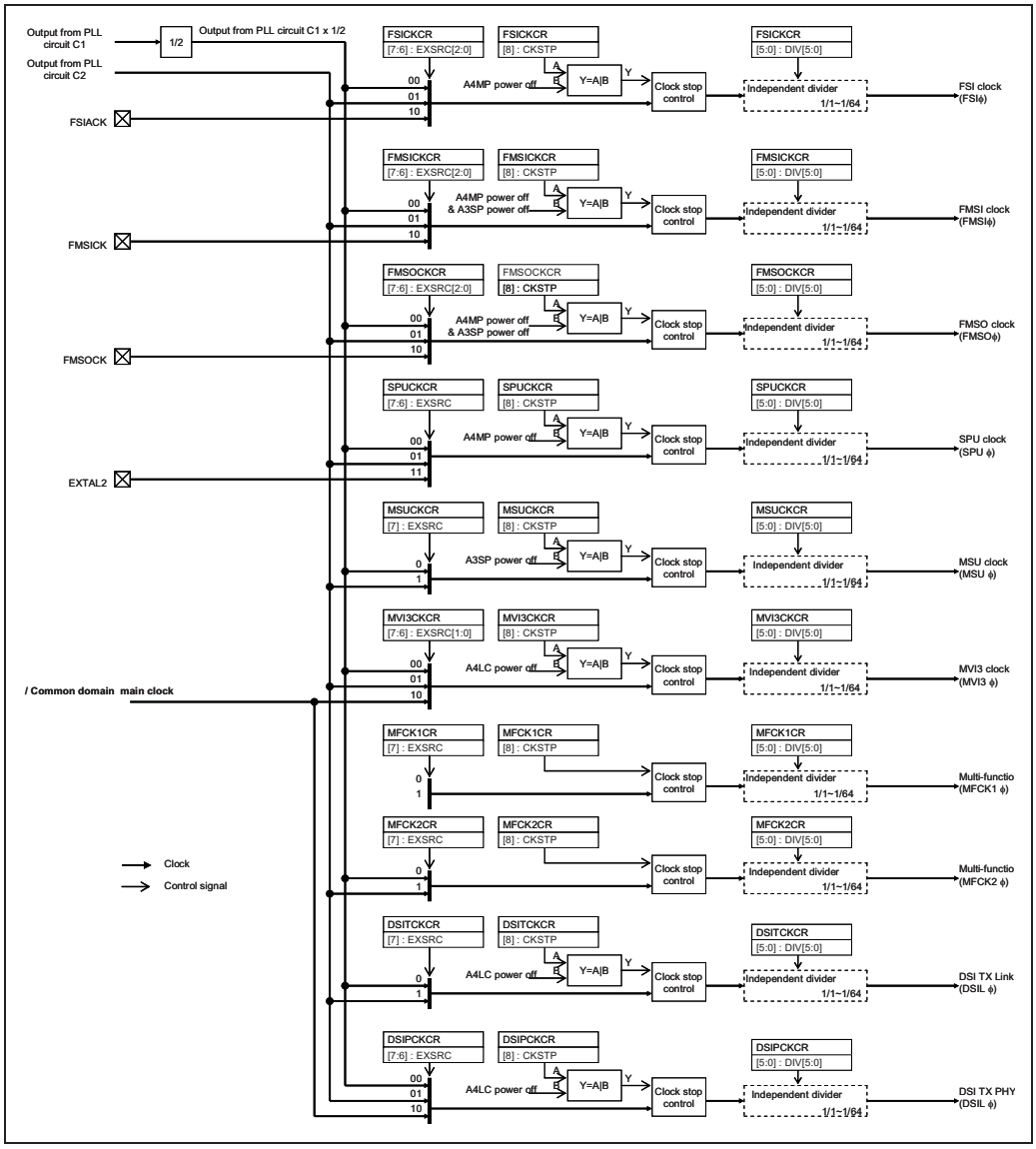


Figure 11.5 Clock Control Related to Independent Divider (2)

11.12 Notes on Board Designing

11.12.1 Bypass Capacitor

Insert laminated ceramic capacitors as bypass capacitors for each V_{SS}/V_{CC} pair. Mount the bypass capacitor near the power supply pins of the LSI. Use components with a frequency characteristic suitable for the operating frequency of the LSI, as well as a suitable capacitance value.

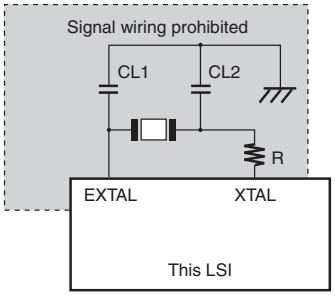
11.12.2 When Using a PLL Oscillation Circuit

Keep the wiring from the PLL V_{DD} and V_{SS} connection pattern to the power supply pins short, and make the pattern width large, to minimize the inductance component.

The analog power supply system of the PLL circuits is sensitive to noise. Therefore system malfunction may occur by the intervention with another power supply. Do not supply the analog power supply with the same resource as the digital power supply of V_{DD} and $V_{CC}Q$.

11.12.3 When Using an External Crystal Resonator

Place the crystal resonator, capacitors CL1 and CL2, and damping resistor R as close to the XTAL2, and EXTAL2 pins as possible. To minimize induction and thus obtain oscillation at the correct frequency, the capacitors to be attached to the resonator must be grounded to the same ground. Do not bring wiring patterns close to these components.



Note: The values for CL1, CL2, and damping resistance should be determined after consultation with the crystal resonator manufacturer.

Figure 11.6 Note on Using a Crystal Resonator

Section 12 RCLK Watchdog Timer (RWDT)

This LSI includes the RCLK watchdog timer (RWDT).

This LSI can be reset by the overflow of the counter when the value of the counter has not been updated because of a system runaway.

The RWDT is a single-channel timer that uses a RTC clock as an input and can be used as a watchdog timer.

12.1 Features

- One channel are provided in the common domain.
- Can be used as a watchdog timer. A system reset is generated when the counter overflows.
- A counter input clock can be chosen from:
  Clocks (RCLK/1 to RCLK/(128×60×30)) that are obtained by dividing the RCLK.

Figure 12.1 shows block diagrams of the RWDT.

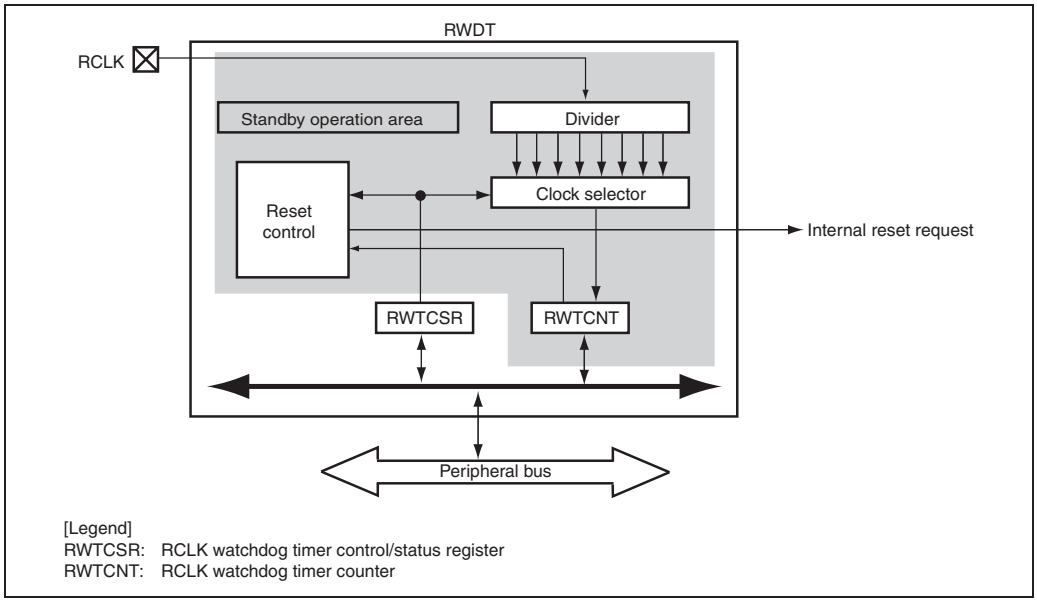


Figure 12.1 Block Diagram of RWDT

12.2 Input/Output Pins for RWDT

Table 12.1 shows the pin configuration and functions of the RWDT.

Table 12.1 RWDT Pin Configuration

Pin Name	Function	I/O	Description
EXTALR (RCLK)	RTC clock	Input	Clock input from an external RTC

12.3 Register Descriptions for RWDT

Table 12.2 shows the RWDT register configuration. Table 12.3 shows the register state in each processing mode.

Table 12.2 Register Configuration of RWDT

Name	Abbreviation	R/W	Address*[3]	Access Size
RCLK watchdog timer counter 0	RWTCNT0	R/W	H'E602 0000 H'E702 0000	8/16*[1]
RCLK watchdog timer control/status register A0	RWTCSRA0	R/W	H'E602 0004 H'E702 0004	8/16*[2]
RCLK watchdog timer control/status register B0	RWTCSRB0	R/W	H'E602 0008 H'E702 0008	8/16*[2]
RCLK watchdog timer counter 1	RWTCNT1	R/W	H'E603 0000 H'E703 0000	8/16*[1]
RCLK watchdog timer control/status register A1	RWTCSRA1	R/W	H'E603 0004 H'E703 0004	8/16*[2]
RCLK watchdog timer control/status register B1	RWTCSRB1	R/W	H'E603 0008 H'E703 0008	8/16*[2]

Notes: 1. Write is performed in 16 bits and read in 8 bits.
2. This register is accessible both from HPBC (E6 space) and HPBD (E7 space).

Table 12.3 Register State of RWDT in Each Processing Mode

Register Abbreviation				
Register	**Bit**	**Power-On Reset**	**System Reset (Including RWDT Overflow Reset)**	**RWDT Software Reset**
RWTCNT0	All	Initialized	Initialized	Initialized
RWTCSRA0	WOVF	Initialized*	Retained	Initialized
	Other than WOVF	Initialized	Initialized	Initialized
RWTCSRB0	All	Initialized*	Initialized	Initialized
RWTCNT1	All	Initialized	Initialized	Initialized
RWTCSRA1	WOVF	Initialized*	Retained	Initialized
	Other than WOVF	Initialized	Initialized	Initialized
RWTCSRB1	All	Initialized*	Initialized	Initialized

Note: * The WOVF bit is initialized only by a power-on reset (RESETP/software), and not by an RWDT overflow reset.

12.3.1 RCLK Watchdog Timer Counter (RWTCNT)

RWTCNT is an 8-bit readable/writable register that increments on the selected clock. When an overflow occurs, it generates a system reset or a power-on reset. The RWTCNT counter is initialized to H'00 by a power-on reset, system reset, and RWDT software reset.

Use a word access to write to the RWTCNT counter, with H'5A in the upper byte. Use a byte access to read RWTCNT.

Bit:	7	6	5	4	3	2	1	0
	RWTCNT							
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

12.3.2 RCLK Watchdog Timer Control/Status Register A (RWTCSRA)

RWTCSRA is an 8-bit readable/writable register composed of bits to select the clock used for the count, overflow flags, and enable bit.

RWTCSRA is initialized to H'87 by a power-on reset and RWDT software reset. Except for the WOVF bit, the system reset is initialized.

Use a word access to write to RWTCSRA, with H'A5 in the upper byte. Use a byte access to read RWTCSRA.

Bit:	7	6	5	4	3	2	1	0
	TME	—	WR FLG	WOVF	WOVFE	CKS[2:0]		
Initial value:	1	0	0	0	1	1	1	1
R/W:	R/W	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	TME	1	R/W	Starts and stops timer operation. 0: Timer disabled: Count-up stops and RWTCNT value is retained 1: Timer enabled
6	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
5	WRFLG	0	R	Write Status Flag The writing to the RWTCNT is disabled during this bit is 1.The writing to the RWTCNT is masked for the prescribed period to synchronize after the writing to the RWTCNT. Confirm that this bit is 0 to write to continuously the RWTCNT.
4	WOVF	0	R/W	Indicates that the RWTCNT has overflowed. This bit is not initialized by a reset generated upon an RWDT overflow. Write 0 to this bit before using the RWDT. 0: No overflow 1: RWTCNT has overflowed
3	WOVFE	1	R/W	Overflow Interrupt Disable/Enable 0: Disables interrupts due to overflow 1: Enables interrupts due to overflow
2 to 0	CKS0[2:0]	111	R/W	RTC Clock Select These bits select the clock to be used for the RWTCNT count from the eight types obtainable by dividing the RTC clock. The overflow period that is shown inside the parenthesis in the table is the value when the RTC clock is 32.768 kHz. 000: Rϕ (7.8 ms) 001: Rϕ/4 (31.3 ms) 010: Rϕ/16 (125.0 ms) 011: Rϕ/32 (250.0 ms) 100: Rϕ/64 (500.0 ms) 101: Rϕ/128 (1.0 s) 110: Rϕ/1024 (8.0 s) 111: RTC clock select expanded mode The clock cycle varies depending on the CKS1 bit in RWTCSRB. Its initial value is Rϕ/4096 (32.0 s).

Note: * If bits CKS[2:0] are modified when the RWDT is operating, the up-count may not be performed correctly. Ensure that the bits CKS[2:0] are modified only when the RWDT is not operating.

12.3.3 RCLK Watchdog Timer Control/Status Register B (RWTCSRB)

RWTCSRB is an 8-bit readable/writable register composed of bits to select the clock used for the count.

RWTCSRB is initialized to H'00 by a power-on reset. Use a word access to write to RWTCSRB, with H'A5 in the upper byte. Use a byte access to read RWTCSRB.

Bit:	7	6	5	4	3	2	1	0
	—	—	CKS1[5:0]					
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
5 to 0	CKS1[5:0]	All 0	R/W	RTC Clock Select for RTC Clock Select Expanded Mode Selects the clock used for the RWTCNT count when the CKS0 bit in RWTCSRA is B'111. The following table shows the time values used to cause an overflow from the counter H'00. Assuming that Rϕ/128 = 1 s, the overflow cycle in the table is calculated for the case when the RTC clock is 32.768 kHz.

CKS[5:4] / CKS[3:0]	2'b00	2'b01	2'b10	2'b11
H'0	32s			
H'1	1 s	5 s	1 min	5 min
H'2	2 s	10 s	2 min	10 min
H'3	3 s	15 s	3 min	15 min
H'4	4 s	20 s	4 min	20 min
H'5	5 s	25 s	5 min	25 min
H'6	6 s	30 s	6 min	30 min
H'7	7 s	35 s	7 min	—
H'8	8 s	40 s	8 min	—
H'9	9 s	45 s	9 min	—
H'A	10 s	50 s	10 min	—
H'B	—	55 s	—	—
H'C	—	60 s	—	—
from H'D	—	—	—	—

Note: * If the CKS15 to CKS10 bits are modified when the RWDT is running, the up-count may not be performed correctly. Ensure that these bits are modified only when the RWDT is not running.

12.3.4 Notes on Register Access

The writing procedure to RWTCNT, RWTCSRA, and RWTCSRB differs from that of other registers with the purpose of preventing an unintended write. The procedure for writing to these registers is given below.

Writing to RWTCNT, RWTCSRA, and RWTCSRB:

- These registers must be written by a word transfer instruction. They cannot be written by a byte or longword transfer instruction.
- When writing to RWTCNT, set the upper byte to H'5A and transfer the lower byte as the write data. When writing to RWTCSRA and RWTCSRB, set the upper byte to H'A5 and transfer the lower byte as the write data.

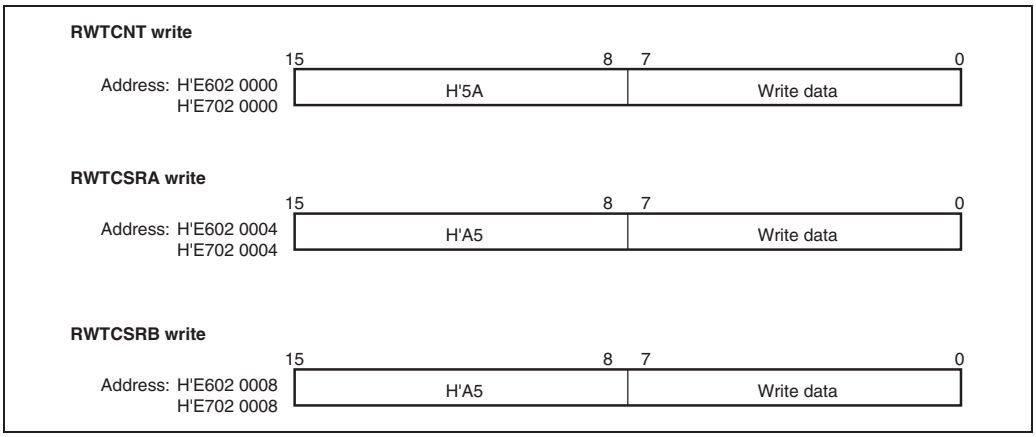


Figure 12.2 Writing to RWTCNT, RWTCSRA, and RWTCSRB

12.4 RWDT Usage

12.4.1 Control of System Runaway

After a power-on reset, RWDT is in the operating state and the counter operates with the Rϕ/4096 clock (initial setting). When the counter overflow occurs, an internal reset is again generated. By this function, a reset can be automatically generated even when this LSI has caused a system runaway. While this LSI is operating correctly, write H'00 to RWTCNT periodically so that RWTCNT does not overflow.

Take the following steps to use the RWDT.

1. Clear the TME bit in RWTCSRA to 0 to temporarily stop counting.
2. Clear the WOVF bit in RWTCSRA to 0.
3. Set the kind of count clock to the CKS2 to CKS0 bits in RWTCSRA.
4. Start the counting by setting the TME bit in RWTCSRA to 1.
5. While this LSI is operating correctly, write H'00 to RWTCNT periodically so that RWTCNT does not overflow.
6. When RWTCNT overflows, a system reset is generated because the RWDT sets the WOVF flag in RWTCSRA to 1. At this time, RWTCNT, RWTCSRA (excluding the WOVF bit), and RWTCSRB are initialized.

   For each reset type and setting, see section 13, System Controller (SYSC).

12.4.2 Debugging Operation

When debugging the CPU core consisting of application processor AP-System/AP-Realtime unit stop counting up RWTCNT and retain the value of RWTCNT.

Section 13 System Controller（SYSC）

The system controller (SYSC) consists of the following two blocks.

1. SYSCIF, the bus interface block, which is resided on common peripheral bus (HPB-C) and operated on CP Clock.
2. SYSC, the main control block which is operated on SP clock. The frequency of SP clock is same as that of CP clock when the External oscillator is enabled and equals to RCK when the oscillator is disabled.

13.1 Features

The following functions are implemented by SYSC

- Boot mode management
- Reset Generation
- Power management (power domain management, Voltage switch control, etc.,)

13.2 Prolonged music play back mode (PMPB)

SYSC implements this mode of operation in conjunction with CPGA and SPU modules. Refer to CPGA module specifications for more details on PMPB. SYSC/CPGA performs optimal power management during this mode by receiving control signals from SPU. During this mode, power of A4S, PLL and EXTAL1 are hardware controlled.

13.3 Debug mode

When the LSI is operated in emulator debug mode, the power supply for all areas is set to be ON by default. That means when a power down request for an area/areas is occurred, the power down sequence is executed but the power supply of that aera/areas in not turned off. The power supply can be made to turn off in debug mode by setting configuration registers. Refer to DBGPOWCR, RESCNT registers.

13.3.1 Operating mode

The LSI can be made to operate in one of the following modes by setting the mode pins TST_N, MD7, MD6, MD4, and MD3 and MD2.

Table 13.1 Operating modes for LSI development phase

TST_N	MD4	MD3	MD2	MD6	MD7	Boot Area	Master processor	Remarks
1	1	0	0	0	0	External memory	System CPU	External ROM
1	0	0	0	0	0	External memory	System CPU	ROM Debug mode*3
1	0/1	0	0	0	1	External memory	System CPU	ROM Debug mode*3
1	0/1	1	0/1	0/1	0/1	built-in memory	System CPU	MaskROM*1
1	0/1	0/1	1	0/1	0/1	built-in memory	System CPU	MaskROM*1
1	0/1	0/1	0/1	1	0/1	built-in memory	System CPU	MaskROM*1
0	1	0	1	0/1	0/1	External memory	System CPU	Standalone mode*2
0	1	1	0	0/1	0/1	External memory	Realtime CPU	Standalone mode*2

Table 13.2 Operating modes for mass production

TST_N	MD4	MD3	MD2	MD6	MD7	Boot Area	Maste Processor	Remarks
0	1	0	1	0/1	0/1	External memory	System CPU	Standalone mode*2
0	1	1	0	0/1	0/1	External memory	Realtime CPU	Standalone mode*2
1	0/1	0/1	0/1	0/1	0/1	Built-in memory	System CPU	MaskROM*1

Note:

**1 Refer to Appendix B for MMFROM programming specifications*

**2 Pin multiplexing for this mode is different from Normal mode. Set TSTMD pin to high when using this mode.*

**3 This mode is used for debugging MaskRom. The boot area is mapped to CS4 area.*

13.4 LSI Pins connected to SYSC

LSI external pins connected to SYSC are shown in the following table.

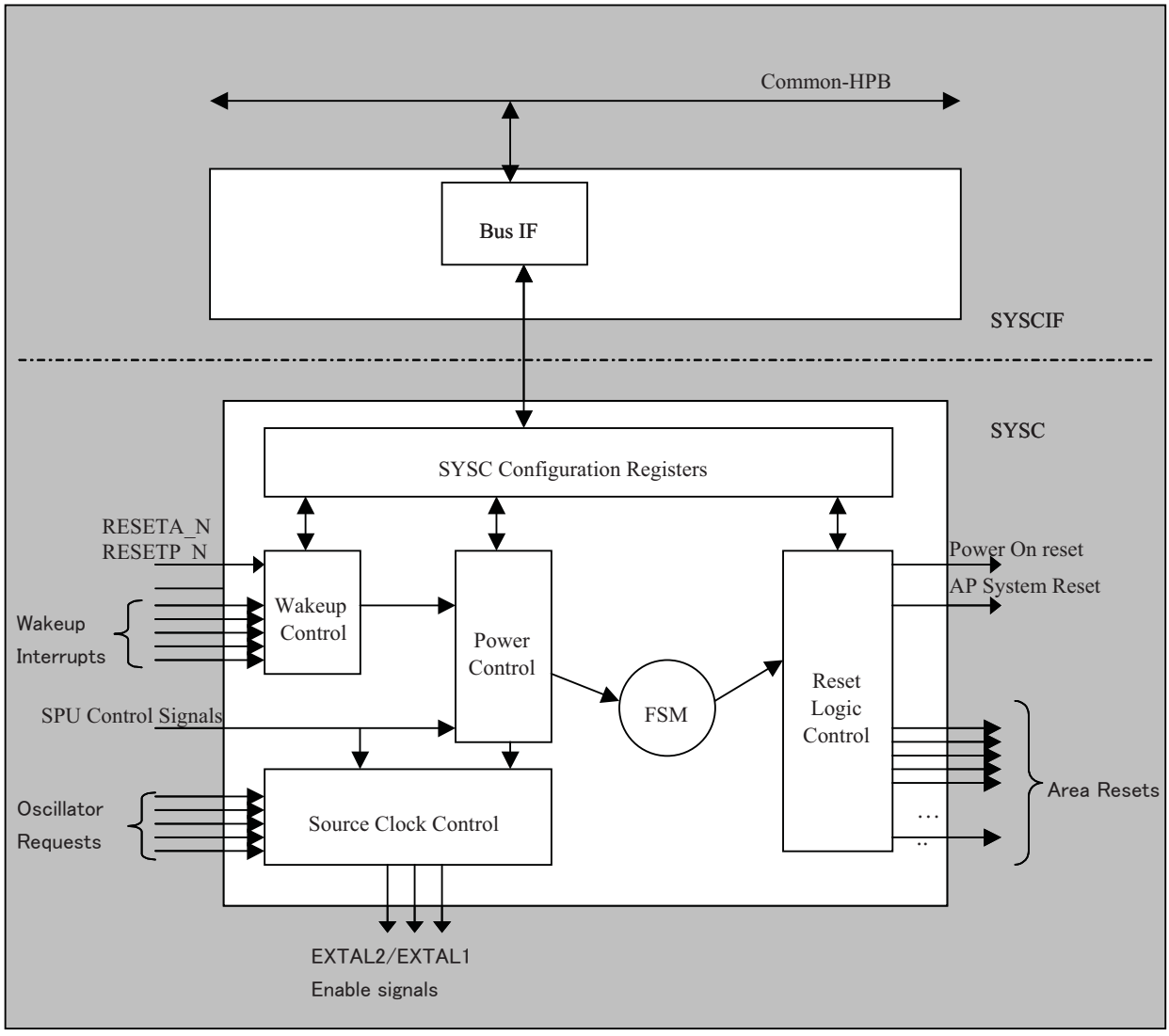
Table 13.3 External pins for SYSC

Pin Name	Function	Direction	Remarks
RESETP_N	Power On Reset	IN	Power On Reset
RESETA_N	AP block system reset	IN	Ap block's system reset
RESETOUTS_N	Indicates internal Reset (System reset /CPU reset)	OUT	System reset /CPU reset can be selected by RESCNT.ROBMD[1:0] bits

13.5 Block diagram

SYSC block diagram is shown in the following figure.

Figure 13.1 Block Diagram



13.6 Register Details

Table 13.4 SYSC Register Details

Register Name	Mnemonic	R/W	Address	Access size	Access permission
Standby Flag Register0	STBCHR0	R/W	H'E618 0000	8/32	ALL
Standby Flag Register 1	STBCHR1	R/W	H'E618 0001	8/32	ALL
Standby Flag Register 2	STBCHR2	R/W	H'E618 0002	8/32	ALL
Standby Flag Register 3	STBCHR3	R/W	H'E618 0003	8/32	ALL
RT Power Down Control Register	RPDCR	R/W	H'E618 0004	32	RT
SYS Power Down Control Register	SPDCR	R/W	H'E618 0008	32	SYS
RT Wakeup Control Register	RWUCR	R/W	H'E618 0010	32	RT
SYS Wakeup Control Register	SWUCR	R/W	H'E618 0014	32	SYS
RT Boot Address Register	RBAR	R/W	H'E618 001C	32	ALL
SYS Boot Address Register	SBAR	R/W	H'E618 0020	32	ALL
WakeUpR Factor Mask Register	WUPRMSK	R/W	H'E618 0028	32	ALL
WakeUpS Factor Mask Register	WUPSMSK	R/W	H'E618 002C	32	ALL
Standby Flag Register B0	STBCHRB0	R/W	H'E618 0040	8/32	ALL
Standby Flag Register B1	STBCHRB1	R/W	H'E618 0041	8/32	ALL
Standby Flag Register B2	STBCHRB2	R/W	H'E618 0042	8/32	ALL
Standby Flag Register B3	STBCHRB3	R/W	H'E618 0043	8/32	ALL
WakeUpR Factor Mask Register2	WUPRMSK2	R/W	H'E618 0044	32	ALL
WakeUpS Factor Mask Register2	WUPSMSK2	R/W	H'E618 0048	32	ALL
A4S Area Power Control Register	A4SPOWCR	R/W	H'E618 004C	32	ALL
Power Status Register	PSTR	R	H'E618 0080	32	ALL
EXTAL2 State Monitor Register	EXSTMON2	R	H'E618 0088	32	ALL
EXTAL1 State Monitor Register	EXSTMON1	R	H'E618 008C	32	ALL
WakeUpR Factor Register	WUPRFAC	R	H'E618 0094	32	ALL
WakeUpS Factor Register	WUPSFAC	R	H'E618 0098	32	ALL
RT Reset Flag Register	RRSTFR	R/(W) *3	H'E618 00B0	32	RT
SYS Reset Flag Register	SRSTFR	R/(W) *3	H'E618 00B4	32	SYS
Debug mode Power Control Register	DGBPOWCR	R/W	H'E618 00C0	32	ALL
RT Write Block Control Register	RWBCR	R/W	H'E618 0200	32	ALL
SYS Write Block Control Register	SWBCR	R/W	H'E618 0204	32	ALL
EXTAL2 Mask Count Register	EXMSKCNT2	R/W	H'E618 0210	32	ALL
EXTAL1 Mask Count Register	EXMSKCNT1	R/W	H'E618 0214	32	ALL
Reset Control Register	RESCNT	R/W	H'E618801C*1	32	ALL
Reset Control Register2	RESCNT2	R/W	H'E6188020*1	32	ALL
WakeUp Area Selection Register	WUPSEL	R/W	H'E618 0228	32	ALL
IRQ Detection Mode Control Register	IRQCR	R/W	H'E618 022C	32	ALL
EXTAL1 Clock Stop Control Register	APSCSTP	R/W	H'E618 0234	32	ALL
IRQ Detection Mode Control Register 2	IRQCR2	R/W	H'E618 0238	32	ALL

IRQ Detection Mode Control Register 3	IRQCR3	R/W	H'E618 0244	32	ALL
IRQ Detection Mode Control Register 4	IRQCR4	R/W	H'E618 0248	32	ALL
EXTAL1 Control Register	SYCKENMSK	R/W	H'E618 024C	32	ALL
WakeUp Area Selection Register2	WUPSEL2	R/W	H'E618 0250	32	ALL
A4S Area Power Control Register2	PDNSEL	R/W	H'E618 0254	32	ALL

Note:

1 Registers with address H'E618 8* should be updated through HPB semaphore. Please release the semaphore bit once the write accesses to these registers is completed. (Refer Appendix A for semaphore register details)*

**2 The CPU number which can access these registers is registered in one of the semaphore registers.Please don't access these registers from CPU's other than this CPU.*

**3 To clear the flag write `0`. Please write 1 to other flag to avoid unintentional clears.*

Table 13.5 State of the Registers on Reset

Mnemonic	Power On Reset	AP System Reset
STBCHR0	Initialize*	Retain
STBCHR1	Initialize*	Retain
STBCHR2	Initialize*	Retain
STBCHR3	Initialize*	Retain
RPDCR	Initialize	Retain
SPDCR	Initialize	Retain
RWUCR	Initialize	Retain
SWUCR	Initialize	Retain
RBAR	Initialize	Retain
SBAR	Initialize	Retain
WUPRMSK	Initialize	Retain
WUPSMSK	Initialize	Retain
STBCHRB0	Initialize*	Retain
STBCHRB1	Initialize*	Retain
STBCHRB2	Initialize*	Retain
STBCHRB3	Initialize*	Retain
WUPRMSK2	Initialize	Retain
WUPSMSK2	Initialize	Retain
PSTR	Initialize	Retain
EXSTMON2	Initialize	Retain
EXSTMON1	Initialize	Retain
WUPRFAC	Initialize	Retain
WUPSFAC	Initialize	Retain
RRSTFR	Initialize	Retain
SRSTFR	Initialize	Retain
BRSTFR	Initialize	Retain
RWBCR	Initialize	Retain
SWBCR	Initialize	Retain
EXMSKCNT2	Initialize	Retain
EXMSKCNT1	Initialize	Retain
RESCNT	Initialize	Retain
RESCNT2	Initialize	Retain
STATUSCR	Initialize	Retain
WUPSEL	Initialize	Retain
IRQCR	Initialize	Retain
PINTACR	Initialize	Retain
APSCSTP	Initialize	Retain
IRQCR2	Initialize	Retain
IRQCR3	Initialize	Retain

IRQCR4	Initialize	Retain
SYCKENMSK	Initialize	Retain
WUPSEL2	Initialize	Retain
A4SPOWCR	Initialize	Retain
DGBPOWCR	Initialize*	Retain

Note: * *Initialized only on Power On Reset caused RESETP_N.*

13.6.1 Standby Flag Register（STBCHRn）

STBCHRn are 8-bit Read/Write registers. These registers are accessed byte wise. Moreover STBCHR0 to 3 are combined to form a single 32-bit register, in that case this register is accessed in long words.

This register is defined purely for software purpose. Setting this register doesn't influence the LSI operation. As this bit is initialized only during Power On Reset caused by RESETP, the programmer can use this register at their convenience.

Bit	7	6	5	4	3	2	1	0
	STBn[7:0]							
Initial Value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Initial Value	R/W	Details
7 to 0	STBn[7:0]	B'00000000	R/W	defined purely for software purpose

13.6.2 RT Power Down Control Register（RPDCR）

RPDCR is a 32 bit Read/Write register, which can be accessed only in long words. Writing 1 to these bits generates a power down request for the corresponding areas. When the power down sequence of the requested area/areas is completed, the corresponding bits are cleared automatically. When power supply of an area is turned off by setting this register, the areas, which are under lower hierarchy of that area, are also turned off at the same time. For example, if A4S area is set to turn off, A3SP/ A3SM areas are also turned off automatically.

This register should be accessed only from RT-CPU

This register is only initialized on Power On Reset.

For power domain hierarchy, refer to section 13.7, Power Domain Specifications.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DLYED	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	A3SGPD	A3SMPD	A3SPPD	A4SPD	-	A3RIPD	-	A3RVPD	A4RPD	-	D4PD	A4MPPD	A4LCPD	-
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R/W	R/W	R/W	R/W	R	R/W	R	R/W	R/W	R	R/W	R/W	R/W	R

Bit	Bit Name	Initial Value	R/W	Description
31	DLYED	0	R/W	Delayed power down request bit 0: Request for normal power down The power down sequence is started when any of the bits in this register are set. 1: Request for delayed power-down Power-down sequence is triggered on detecting SLEEP instruction from RT-CPU. (The required bits of this register should be set prior to SLEEP instruction)
30 to 14	—	All 0	R	Reserved When read, returns 0. The write value should always be 0
13	A3SGPD	0	R/W*[1]	A3SG area power down request bit Write Access: 0：Ignore 1：Generate A3SG Power down request Read Access: 0：A3SG power down sequence is completed 1：A3SG power down sequence is in progress

Bit	Bit Name	Initial Value	R/W	Description
12	A3SMPD	0	R/W*[1]	A3SM area power down request bit Write Access: 0：Ignore 1：Generate A3SM Power down request Read Access: 0：A3SM power down sequence is completed 1：A3SM power down sequence is in progress
11	A3SPPD	0	R/W*[1]	A3SP area power down request bit Write Access: 0：Ignore 1：Generate A3SP Power down request Read Access: 0：A3SP power down sequence is completed 1：A3SP power down sequence is in progress
10	A4SPD	0	R/W*[1]	A4S area power down request bit Write Access: 0：Ignore 1：Generate A4S Power down request Read Access: 0：A4S power down sequence is completed 1：A4S power down sequence is in progress
9	—	0	R	Reserved When read, returns 0. The write value should always be 0
8	A3RIPD	0	R/W*[1]	A3RI area power down request bit Write Access: 0：Ignore 1：Generate A3RI Power down request Read Access: 0：A3RI power down sequence is completed 1：A3RI power down sequence is in progress
7	—	0	R	Reserved When read, returns 0. The write value should always be 0
6	A3RVPD	0	R/W*[1]	A3RV area power down request bit Write Access: 0：Ignore 1：Generate A3RV Power down request Read Access: 0：A3RV power down sequence is completed 1：A3RV power down sequence is in progress

Bit	Bit Name	Initial Value	R/W	Description
5	A4RPD	0	R/W*[1]	A4R area power down request bit Write Access: 0：Ignore 1：Generate A4R Power down request Read Access: 0：A4R power down sequence is completed 1：A4R power down sequence is in progress
4	—	0	R	Reserved When read, returns 0. The write value should always be 0
3	D4PD	0	R/W*[1]	D4 area power down request bit Write Access: 0：Ignore 1：Generate D4 Power down request Read Access: 0：D4 power down sequence is completed 1：D4 power down sequence is in progress
2	A4MPPD	0	R/W*[1]	A4MP area power down request bit Write Access: 0：Ignore 1：Generate A4MP Power down request Read Access: 0：A4MP power down sequence is completed 1：A4MP power down sequence is in progress
1	A4LCPD	0	R/W*[1]	A4LC area power down request bit Write Access: 0：Ignore 1：Generate A4LC Power down request Read Access: 0：A4LC power down sequence is completed 1：A4LC power down sequence is in progress
0	—	0	R	Reserved When read, returns 0. The write value should always be 0

*Note: *1 The bits of this register cannot be written when the corresponding bits of RT write Block control register are set. Do not attempt a Write access to this register when any of these bits are set to 1.*

13.6.3 SYS Power Down Control Register（SPDCR）

SPDCR is a 32 bit Read/Write register, which can be accessed only in long words. Writing 1 to these bits generates a power down request for the corresponding areas. When the power down sequence of the requested area/areas is completed, the corresponding bits are cleared automatically. When power supply of an area is turned off by setting this register, the areas, which are under lower hierarchy of that area, are also turned off at the same time. For example, if A4S area is set to turn off, A3SP/ A3SM areas are also turned off automatically.

This register should be accessed only from SYS-CPU

This register is only initialized on Power On Reset.

For power domain hierarchy, refer to section 13.7, Power Domain Specifications.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DLYED	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	A3SGPD	A3SMPD	A3SPPD	A4SPD	-	A3RIPD	-	A3RVPD	A4RPD	-	D4PD	A4MPPD	A4LCPD	-
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R/W	R/W	R/W	R/W	R	R/W	R	R/W	R/W	R	R/W	R/W	R/W	R

Bit	Bit Name	Initial Value	R/W	Description
31	DLYED	0	R/W	Delayed power down request bit 0: Request for normal power down The power down sequence is started when any of the bits in this register are set. 1: Request for delayed power-down Power-down sequence is triggered on detecting WFI instruction from SYS-CPU. (The required bits of this register should be set prior to WFI instruction)
30 to 14	—	All 0	R	Reserved When read, returns 0. The write value should always be 0
13	A3SGPD	0	R/W*[1]	A3SG area power down request bit Write Access: 0：Ignore 1：Generate A3SG Power down request Read Access: 0：A3SG power down sequence is completed 1：A3SG power down sequence is in progress

Bit	Bit Name	Initial Value	R/W	Description
12	A3SMPD	0	R/W*[1]	A3SM area power down request bit Write Access: 0：Ignore 1：Generate A3SM Power down request Read Access: 0：A3SM power down sequence is completed 1：A3SM power down sequence is in progress
11	A3SPPD	0	R/W*[1]	A3SP area power down request bit Write Access: 0：Ignore 1：Generate A3SP Power down request Read Access: 0：A3SP power down sequence is completed 1：A3SP power down sequence is in progress
10	A4SPD	0	R/W*[1]	A4S area power down request bit Write Access: 0：Ignore 1：Generate A4S Power down request Read Access: 0：A4S power down sequence is completed 1：A4S power down sequence is in progress
9	—	0	R	Reserved When read, returns 0. The write value should always be 0
8	A3RIPD	0	R/W*[1]	A3RI area power down request bit Write Access: 0：Ignore 1：Generate A3RI Power down request Read Access: 0：A3RI power down sequence is completed 1：A3RI power down sequence is in progress
7	—	0	R	Reserved When read, returns 0. The write value should always be 0
6	A3RVPD	0	R/W*[1]	A3RV area power down request bit Write Access: 0：Ignore 1：Generate A3RV Power down request Read Access: 0：A3RV power down sequence is completed 1：A3RV power down sequence is in progress

Bit	Bit Name	Initial Value	R/W	Description
5	A4RPD	0	R/W*[1]	A4R area power down request bit Write Access: 0：Ignore 1：Generate A4R Power down request Read Access: 0：A4R power down sequence is completed 1：A4R power down sequence is in progress
4	—	0	R	Reserved When read, returns 0. The write value should always be 0
3	D4PD	0	R/W*[1]	D4 area power down request bit Write Access: 0：Ignore 1：Generate D4 Power down request Read Access: 0：D4 power down sequence is completed 1：D4 power down sequence is in progress
2	A4MPPD	0	R/W*[1]	A4MP area power down request bit Write Access: 0：Ignore 1：Generate A4MP Power down request Read Access: 0：A4MP power down sequence is completed 1：A4MP power down sequence is in progress
1	A4LCPD	0	R/W*[1]	A4LC area power down request bit Write Access: 0：Ignore 1：Generate A4LC Power down request Read Access: 0：A4LC power down sequence is completed 1：A4LC power down sequence is in progress
0	—	0	R	Reserved When read, returns 0. The write value should always be 0

*Note: *1 The bits of this register cannot be written when the corresponding bits of RT write Block control register are set.*

Do not attempt a Write access to this register when any of these bits are set to 1.

13.6.4 RT Wakeup Control Register（RWUCR）

RWUCR is a Read/Write 32 bit register, which can be accessed only in long words. Writing 1 to these bits generates a Wake up request to the corresponding areas. When the Wake up sequence of the requested area/areas is completed, the corresponding bits are cleared automatically.

When power supply of an area is turned on by setting this register, the areas, which are under higher hierarchy of that area, are also turned on at the same time. For example, if A3SP area is set to turn on, A4S area is also turned on automatically.

This register should be accessed only from RT-CPU

This register is only initialized on Power On Reset.

For power domain hierarchy, refer to section 12.5, Power Domain Specifications.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	A3SGWU	A3SMWU	A3SPWU	A4SWU	-	A3RIWU	-	A3RVWU	A4RWU	-	D4WU	A4MPWU	A4LCWU	-
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R/W	R/W	R/W	R/W	R	R/W	R	R/W	R/W	R	R/W	R/W	R/W	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All 0	R	Reserved When read, returns 0. The write value should always be 0
13	A3SGWU	0	R/W*1	A3SG area wakeup request bit Write Access: 0：Ignore 1：Generate A3SG Wakeup request Read Access: 0：A3SG wakeup sequence is completed 1：A3SG wakeup sequence is in progress
12	A3SMWU	0	R/W*1	A3SM area wakeup request bit Write Access: 0：Ignore 1：Generate A3SM Wakeup request Read Access: 0：A3SM wakeup sequence is completed 1：A3SM wakeup sequence is in progress

Bit	Bit Name	Initial Value	R/W	Description
11	A3SPWU	0	R/W*1	A3SP area wakeup request bit Write Access: 0：Ignore 1：Generate A3SP Wakeup request Read Access: 0：A3SP wakeup sequence is completed 1：A3SP wakeup sequence is in progress
10	A4SWU	0	R/W*1	A4S area wakeup request bit Write Access: 0：Ignore 1：Generate A4S Wakeup request Read Access: 0：A4S wakeup sequence is completed 1：A4S wakeup sequence is in progress
9	—	0	R	Reserved When read, returns 0. The write value should always be 0
8	A3RIWU	0	R/W*1	A3RI area wakeup request bit Write Access: 0：Ignore 1：Generate A3RI Wakeup request Read Access: 0：A3RI wakeup sequence is completed 1：A3RI wakeup sequence is in progress
7	—	0	R	Reserved When read, returns 0. The write value should always be 0
6	A3RVWU	0	R/W*1	A3RV area wakeup request bit Write Access: 0：Ignore 1：Generate A3RV Wakeup request Read Access: 0：A3RV wakeup sequence is completed 1：A3RV wakeup sequence is in progress
5	A4RWU	0	R/W*1	A4R area wakeup request bit Write Access: 0：Ignore 1：Generate A4R Wakeup request Read Access: 0：A4R wakeup sequence is completed 1：A4R wakeup sequence is in progress
4	—	0	R	Reserved When read, returns 0. The write value should always be 0

Bit	Bit Name	Initial Value	R/W	Description
3	D4WU	0	R/W*[1]	D4 area wakeup request bit Write Access: 0：Ignore 1：Generate D4 Wakeup request Read Access: 0：D4 wakeup sequence is completed 1：D4 wakeup sequence is in progress
2	A4MPWU	0	R/W*[1]	A4MP area wakeup request bit Write Access: 0：Ignore 1：Generate A4MP Wakeup request Read Access: 0：A4MP wakeup sequence is completed 1：A4MP wakeup sequence is in progress
1	A4LCWU	0	R/W*[1]	A4LC area wakeup request bit Write Access: 0：Ignore 1：Generate A4LC Wakeup request Read Access: 0：A4LC wakeup sequence is completed 1：A4LC wakeup sequence is in progress
0	—	0	R	Reserved When read, returns 0. The write value should always be 0

*Note: *1 The bits of this register cannot be written when the corresponding bits of RT write Block control register are set.*

Do not attempt a Write access to this register when any of these bits are set to 1.

13.6.5 SYS Wakeup Control Register（SWUCR）

SWUCR is a Read/Write 32 bit register, which can be accessed only in long words. Writing 1 to these bits generates a Wake up request to the corresponding areas. When the Wake up sequence of the requested area/areas is completed, the corresponding bits are cleared automatically.

When power supply of an area is turned on by setting this register, the areas, which are under higher hierarchy of that area, are also turned on at the same time. For example, if A3SP area is set to turn on, A4S area is also turned on automatically.

This register should be accessed only from SYS-CPU

This register is only initialized on Power On Reset.

For power domain hierarchy, refer to section 13.7, Power Domain Specifications.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	A3SGWU	A3SMWU	A3SPWU	A4SWU	-	A3RIWU	-	A3RVWU	A4RWU	-	D4WU	A4MPWU	A4LCWU	-
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R/W	R/W	R/W	R/W	R	R/W	R	R/W	R/W	R	R/W	R/W	R/W	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All 0	R	Reserved When read, returns 0. The write value should always be 0
13	A3SGWU	0	R/W*[1]	A3SG area wakeup request bit Write Access: 0：Ignore 1：Generate A3SG Wakeup request Read Access: 0：A3SG wakeup sequence is completed 1：A3SG wakeup sequence is in progress
12	A3SMWU	0	R/W*[1]	A3SM area wakeup request bit Write Access: 0：Ignore 1：Generate A3SM Wakeup request Read Access: 0：A3SM wakeup sequence is completed 1：A3SM wakeup sequence is in progress

Bit	Bit Name	Initial Value	R/W	Description
11	A3SPWU	0	R/W*1	A3SP area wakeup request bit Write Access: 0：Ignore 1：Generate A3SP Wakeup request Read Access: 0：A3SP wakeup sequence is completed 1：A3SP wakeup sequence is in progress
10	A4SWU	0	R/W*1	A4S area wakeup request bit Write Access: 0：Ignore 1：Generate A4S Wakeup request Read Access: 0：A4S wakeup sequence is completed 1：A4S wakeup sequence is in progress
9	—	0	R	Reserved When read, returns 0. The write value should always be 0
8	A3RIWU	0	R/W*1	A3RI area wakeup request bit Write Access: 0：Ignore 1：Generate A3RI Wakeup request Read Access: 0：A3RI wakeup sequence is completed 1：A3RI wakeup sequence is in progress
7	—	0	R	Reserved When read, returns 0. The write value should always be 0
6	A3RVWU	0	R/W*1	A3RV area wakeup request bit Write Access: 0：Ignore 1：Generate A3RV Wakeup request Read Access: 0：A3RV wakeup sequence is completed 1：A3RV wakeup sequence is in progress
5	A4RWU	0	R/W*1	A4R area wakeup request bit Write Access: 0：Ignore 1：Generate A4R Wakeup request Read Access: 0：A4R wakeup sequence is completed 1：A4R wakeup sequence is in progress
4	—	0	R	Reserved When read, returns 0. The write value should always be 0

Bit	Bit Name	Initial Value	R/W	Description
3	D4WU	0	R/W*1	D4 area wakeup request bit Write Access: 0：Ignore 1：Generate D4 Wakeup request Read Access: 0：D4 wakeup sequence is completed 1：D4 wakeup sequence is in progress
2	A4MPWU	0	R/W*1	A4MP area wakeup request bit Write Access: 0：Ignore 1：Generate A4MP Wakeup request Read Access: 0：A4MP wakeup sequence is completed 1：A4MP wakeup sequence is in progress
1	A4LCWU	0	R/W*1	A4LC area wakeup request bit Write Access: 0：Ignore 1：Generate A4LC Wakeup request Read Access: 0：A4LC wakeup sequence is completed 1：A4LC wakeup sequence is in progress
0	—	0	R	Reserved When read, returns 0. The write value should always be 0

*Note: *1 The bits of this register cannot be written when the corresponding bits of RT write Block control register are set.*

Do not attempt a Write access to this register when any of these bits are set to 1.

13.6.6 RT Boot Address Register（RBAR）

RBAR is a 32-bit read/write register, which can be accessed only in long words.

This register specifies the boot space of the RT-CPU.

This register is initialized on Power On Reset.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RBAR[31:16]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RBAR[15:4]												-	-	BTMD[1:0]	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0/1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	RBAR[31:4]	H'B000000	R/W	RT CPU Boot Address Specifies the upper 28 bits of RT CPU's boot address
3, 2	－	All 0	R	Reserved When read, returns 0.The write value should always be 0
1, 0	BTMD[1:0]	00/01*	R/W	Specifies the Boot area of RT CPU During Hardware Power On Reset the initial value of these bits depends upon TST_N, MD7, MD6, MD4, MD3, MD2 pin setting. Refer to Table 13.1 for boot mode specifications. 00：RT CPU boots from External Memory 01：Boot address is assigned to RBAR[31:4], lower 4 bits are set to 0. 10：Prohibited 11：Boots from MFRAM area between SYS-RT

*Note : * Initial value depends upon /TST, MD7, MD6, MD4, MD3, MD2 pin setting.*

13.6.7 SYS Boot Address Register（SBAR）

SBAR is a 32-bit read/write register, which can be accessed only in long words.

This register specifies the boot space of the SYS-CPU.

This register is initialized on Power On Reset.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SBAR[31:16]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SBAR[15:12]				-	-	-	-	-	-	-	-	-	-	BTMD[1:0]	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	SBAR[31:12]	H'00000	R/W	SYS-CPU Boot Address When SYS-CPU accesses a physical address within the first 4- to 512-Kbyte area (H'0000 0000 to H'0000 0FFF/H'0007 FFFF)*1, bits 31 to 12 in the address are replaced with the value specified in the SBAR [31:12] bits. As this conversion is performed always, set the SBAR [31:12] bits to H'00000 to disable this conversion.
11 to 2	—	All 0	R	Reserved When read, returns 0. The write value should always be 0.
1, 0	BTMD[1:0]	00 *2	R/W	Specifies the Boot area of SYS CPU During Hardware Power On Reset the initial value of these bits depends upon /TST, MD7, MD6, MD4, MD3, MD2 pin setting . Refer to Table 13.1 for boot mode specifications. 00：SBAR[31:12] is assigned to Boot address, set SBAR[11:0] to 0. 01：Boots From SMFRAM. 10：Boots from Built-in memory. 11：Prohibited.

Note *1 *The address range can be specified in APARMBAREA. For details, refer to section 2, AP-System Core in the AP Block manual*

*2 *Initial value depends upon TST_N, MD7, MD6, MD4, MD3, MD2 pin setting.*

13.6.8 WakeuR Factor Mask Register (WUPRMSK)

WUPRMSK is a 32-bit read/write register, which can be accessed only in long words. RT-CPU Wakeup factor can be masked by setting this register. This register is initialized on Power On Reset. The wakeup factor, which can be masked by this register, wakes up all the power off areas that are required to operate RT-CPU (A4R).This register doesn't specify the areas that can be waken up by WakeUpR.

For power domain hierarchy, refer to section 13.7, Power Domain Specifications

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	MFISM	CPTS2RM	-	-	-	-	-	-	-	-	IRQ15M	IRQ14M	IRQ13M	IRQ12M
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R/W	R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IRQ11M	IRQ10M	IRQ9M	IRQ8M	IRQ7M	IRQ6M	IRQ5M	IRQ4M	IRQ3M	IRQ2M	IRQ1M	IRQ0M	LCRCM	KEYM	CMTM	ASBM
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 30	—	ALL 0	R	Reserved When read, returns 0. The write value should always be 0.
29	MFISM	0	R/W	MFIS Interrupt mask bit 0：MFIS Interrupt can be a factor for WakeupR generation 1：MFIS Interrupt can not be a factor for WakeupR generation
28	CPTS2RM	0	R/W	CPTS2RM Interrupt Mask Bit 0：CPTS2RM Interrupt can be a factor for WakeupR generation 1：CPTS2RM Interrupt can not be a factor for WakeupR generation
27 to 20	—	ALL 0	R	Reserved When read, returns 0. The write value should always be 0.
19	IRQ15M	0	R/W	IRQ15 Interrupt Mask Bit 0：IRQ15 Interrupt can be a factor for WakeupR generation 1：IRQ15 Interrupt can not be a factor for WakeupR generation
18	IRQ14M	0	R/W	IRQ14 Interrupt Mask Bit 0：IRQ14 Interrupt can be a factor for WakeupR generation 1：IRQ14 Interrupt can not be a factor for WakeupR generation
17	IRQ13M	0	R/W	IRQ13 Interrupt Mask Bit 0：IRQ13 Interrupt can be a factor for WakeupR generation 1：IRQ13 Interrupt can not be a factor for WakeupR generation
16	IRQ12M	0	R/W	IRQ12 Interrupt Mask Bit 0：IRQ12 Interrupt can be a factor for WakeupR generation 1：IRQ12 Interrupt can not be a factor for WakeupR generation

15	IRQ11M	0	R/W	IRQ11 Interrupt Mask Bit 0：IRQ11Interrupt can be a factor for WakeupR generation 1：IRQ11Interrupt can be a factor for WakeupR generation
14	IRQ10M	0	R/W	IRQ10 Interrupt Mask Bit 0：IRQ10 Interrupt can be a factor for WakeupR generation 1：IRQ10 Interrupt can not be a factor for WakeupR generation
13	IRQ9M	0	R/W	IRQ9 Interrupt Mask Bit 0：IRQ9 Interrupt can be a factor for WakeupR generation 1：IRQ9 Interrupt can not be a factor for WakeupR generation
12	IRQ8M	0	R/W	IRQ8 Interrupt Mask Bit 0：IRQ8 Interrupt can be a factor for WakeupR generation 1：IRQ8 Interrupt can not be a factor for WakeupR generation
11	IRQ7M	0	R/W	IRQ7 Interrupt Mask Bit 0：IRQ7 Interrupt can be a factor for WakeupR generation 1：IRQ7 Interrupt can not be a factor for WakeupR generation
10	IRQ6M	0	R/W	IRQ6 Interrupt Mask Bit 0：IRQ6 Interrupt can be a factor for WakeupR generation 1：IRQ6 Interrupt can not be a factor for WakeupR generation
9	IRQ5M	0	R/W	IRQ5 Interrupt Mask Bit 0：IRQ5 Interrupt can be a factor for WakeupR generation 1：IRQ5 Interrupt can not be a factor for WakeupR generation
8	IRQ4M	0	R/W	IRQ4 Interrupt Mask Bit 0：IRQ4 Interrupt can be a factor for WakeupR generation 1：IRQ4 Interrupt can not be a factor for WakeupR generation
7	IRQ3M	0	R/W	IRQ3 Interrupt Mask Bit 0：IRQ3 Interrupt can be a factor for WakeupR generation 1：IRQ3 Interrupt can not be a factor for WakeupR generation
6	IRQ2M	0	R/W	IRQ2 Interrupt Mask Bit 0：IRQ2 Interrupt can be a factor for WakeupR generation 1：IRQ2 Interrupt can not be a factor for WakeupR generation
5	IRQ1M	0	R/W	IRQ1 Interrupt Mask Bit 0：IRQ1 Interrupt can be a factor for WakeupR generation 1：IRQ1 Interrupt can not be a factor for WakeupR generation
4	IRQ0M	0	R/W	IRQ0 Interrupt Mask Bit 0：IRQ0 Interrupt can be a factor for WakeupR generation 1：IRQ0 Interrupt can not be a factor for WakeupR generation
3	LCRCM	0	R/W	LCRC Interrupt Mask Bit 0：LCRC Interrupt can be a factor for WakeupR generation 1：LCRC Interrupt can not be a factor for WakeupR generation

2	KEYM	0	R/W	KEYSC Interrupt Mask Bit 0：KEYSC Interrupt can be a factor for WakeupR generation 1：KEYSC Interrupt can not be a factor for WakeupR generation
1	CMTM	0	R/W	CMT Interrupt Mask Bit 0：CMT Interrupt can be a factor for WakeupR generation 1：CMT Interrupt can not be a factor for WakeupR generation
0	ASBM	0	R/W	ASEBRK Mask bit 0：ASEBRK can be a factor for WakeupR generation 1： ASEBRK can not be a factor for WakeupR generation

13.6.9 WakeupS Factor Mask Register (WUPSMSK)

WUPSMSK is a 32-bit read/write register, which can be accessed only in long words. SYS-CPU Wakeup factor can be masked by setting this register.

The wakeup factor, which can be masked by this register, wakes up all the power off areas that are required to operate SYS CPU (A4S/A3SM). This register doesn't specify the areas that can be waken up by WakeUpS. This register is initialized on Power On Reset.

For power domain hierarchy, refer to section 13.7, Power Domain Specifications

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SPUM	LCRCM	-	-	-	-	-	-	-	-	MFIM	EDBQM	IRQ15M	IRQ14M	IRQ13M	IRQ12M
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IRQ11M	IRQ10M	IRQ9M	IRQ8M	IRQ7M	IRQ6M	IRQ5M	IRQ4M	IRQ3M	IRQ2M	IRQ1M	IRQ0M	NMIM	KEYM	CMTM	INTCAM
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	SPUM	0	R/W	SPU Interrupt Mask Bit 0：SPU Interrupt can be a factor for WakeupS generation 1：SPU Interrupt can not be a factor for WakeupS generation
30	LCRCM	0	R/W	LCRC Interrupt Mask Bit 0：LCRC Interrupt can be a factor for WakeupS generation 1：LCRC Interrupt can not be a factor for WakeupS generation
29 to 22	—	All 0	R	Reserved When read, returns 0. The write value should always be 0.
21	MFIM	0	R/W	INTREQ_MFI Interrupt Mask Bit 0：INTREQ_MFI Interrupt can be a factor for WakeupS generation 1：INTREQ_MFI Interrupt can not be a factor for WakeupS generation
20	EDBQM	0	R/W	EDBGRQ Interrupt Mask Bit 0：EDBGRQ Interrupt can be a factor for WakeupS generation 1：EDBGRQ Interrupt can not be a factor for WakeupS generation
19	IRQ15M	0	R/W	IRQ15Interrupt Mask Bit 0：IRQ15 Interrupt can be a factor for WakeupS generation 1：IRQ15 Interrupt can not be a factor for WakeupS generation
18	IRQ14M	0	R/W	IRQ14Interrupt Mask Bit 0：IRQ14 Interrupt can be a factor for WakeupS generation 1：IRQ14 Interrupt can not be a factor for WakeupS generation

Bit	Bit Name	Initial Value	R/W	Description
17	IRQ13M	0	R/W	IRQ13Interrupt Mask Bit 0：IRQ13 Interrupt can be a factor for WakeupS generation 1：IRQ13 Interrupt can not be a factor for WakeupS generation
16	IRQ12M	0	R/W	IRQ12Interrupt Mask Bit 0：IRQ12 Interrupt can be a factor for WakeupS generation 1：IRQ12 Interrupt can not be a factor for WakeupS generation
15	IRQ11M	0	R/W	IRQ11Interrupt Mask Bit 0：IRQ11 Interrupt can be a factor for WakeupS generation 1：IRQ11 Interrupt can not be a factor for WakeupS generation
14	IRQ10M	0	R/W	IRQ10Interrupt Mask Bit 0：IRQ10 Interrupt can be a factor for WakeupS generation 1：IRQ10 Interrupt can not be a factor for WakeupS generation
13	IRQ9M	0	R/W	IRQ9Interrupt Mask Bit 0：IRQ9 Interrupt can be a factor for WakeupS generation 1：IRQ9 Interrupt can not be a factor for WakeupS generation
12	IRQ8M	0	R/W	IRQ8Interrupt Mask Bit 0：IRQ8 Interrupt can be a factor for WakeupS generation 1：IRQ8 Interrupt can not be a factor for WakeupS generation
11	IRQ7M	0	R/W	IRQ7Interrupt Mask Bit 0：IRQ7 Interrupt can be a factor for WakeupS generation 1：IRQ7 Interrupt can not be a factor for WakeupS generation
10	IRQ6M	0	R/W	IRQ6Interrupt Mask Bit 0：IRQ6 Interrupt can be a factor for WakeupS generation 1：IRQ6 Interrupt can not be a factor for WakeupS generation
9	IRQ5M	0	R/W	IRQ5Interrupt Mask Bit 0：IRQ5 Interrupt can be a factor for WakeupS generation 1：IRQ5 Interrupt can not be a factor for WakeupS generation
8	IRQ4M	0	R/W	IRQ4Interrupt Mask Bit 0：IRQ4 Interrupt can be a factor for WakeupS generation 1：IRQ4 Interrupt can not be a factor for WakeupS generation
7	IRQ3M	0	R/W	IRQ3Interrupt Mask Bit 0：IRQ3 Interrupt can be a factor for WakeupS generation 1：IRQ3 Interrupt can not be a factor for WakeupS generation
6	IRQ2M	0	R/W	IRQ2Interrupt Mask Bit 0：IRQ2 Interrupt can be a factor for WakeupS generation 1：IRQ2 Interrupt can not be a factor for WakeupS generation
5	IRQ1M	0	R/W	IRQ1Interrupt Mask Bit 0：IRQ1 Interrupt can be a factor for WakeupS generation 1：IRQ1 Interrupt can not be a factor for WakeupS generation

Bit	Bit Name	Initial Value	R/W	Description
4	IRQ0M	0	R/W	IRQ0 Interrupt Mask Bit 0：IRQ0 Interrupt can be a factor for WakeupS generation 1：IRQ0 Interrupt can not be a factor for WakeupS generation
3	NMIM	0	R/W	NMI Interrupt Mask Bit 0：NMI Interrupt can be a factor for WakeupS generation 1：NMI Interrupt can not be a factor for WakeupS generation
2	KEYM	0	R/W	KEYSC Interrupt Mask Bit 0：KEYSC Interrupt can be a factor for WakeupS generation 1：KEYSC Interrupt can not be a factor for WakeupS generation
1	CMTM	0	R/W	CMT Interrupt Mask Bit 0：CMT Interrupt can be a factor for WakeupS generation 1：CMT Interrupt can not be a factor for WakeupS generation
0	INTCAM	0	R/W	INTCA Mask Bit 0： Interrupt from INTCA can be a factor for WakeupS generation 1： Interrupt from INTCA can not be a factor for WakeupS generation

13.6.10 WakeupR Factor Mask Register2 (WUPRMSK2)

WUPRMSK is a 32-bit read/write register, which can be accessed only in long words. RT-CPU Wakeup factor can be masked by setting this register.

The wakeup factor, which can be masked by this register, wakes up all the power off areas that are required to operate RT CPU (A4R).This register doesn't specify the areas that can be waken up by WakeUpR. This register is initialized on Power On Reset.

For power domain hierarchy, refer to section 13.7, Power Domain Specifications

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IRQ 31M	IRQ 30M	IRQ 29M	IRQ 28M	IRQ 27M	IRQ 26M	IRQ 25M	IRQ 24M	IRQ 23M	IRQ 22M	IRQ 21M	IRQ 20M	IRQ 19M	IRQ 18M	IRQ 17M	IRQ 16M
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	ALL 0	R	Reserved When read, returns 0. The write value should always be 0
15	IRQ31M	0	R/W	IRQ31 Interrupt Mask Bit 0：IRQ31Interrupt can be a factor for WakeupR generation 1：IRQ31 Interrupt can not be a factor for WakeupR generation
14	IRQ30M	0	R/W	IRQ30 Interrupt Mask Bit 0：IRQ30 Interrupt can be a factor for WakeupR generation 1：IRQ30 Interrupt can not be a factor for WakeupR generation
13	IRQ29M	0	R/W	IRQ29 Interrupt Mask Bit 0：IRQ29 Interrupt can be a factor for WakeupR generation 1：IRQ29 Interrupt can not be a factor for WakeupR generation
12	IRQ28M	0	R/W	IRQ28 Interrupt Mask Bit 0：IRQ28 Interrupt can be a factor for WakeupR generation 1：IRQ28 Interrupt can not be a factor for WakeupR generation
11	IRQ27M	0	R/W	IRQ27 Interrupt Mask Bit 0：IRQ27 Interrupt can be a factor for WakeupR generation 1：IRQ27 Interrupt can not be a factor for WakeupR generation
10	IRQ26M	0	R/W	IRQ26 Interrupt Mask Bit 0：IRQ26 Interrupt can be a factor for WakeupR generation 1：IRQ26 Interrupt can not be a factor for WakeupR generation

9	IRQ25M	0	R/W	IRQ25 Interrupt Mask Bit 0：IRQ25 Interrupt can be a factor for WakeupR generation 1：IRQ25 Interrupt can not be a factor for WakeupR generation
8	IRQ24M	0	R/W	IRQ24 Interrupt Mask Bit 0：IRQ24 Interrupt can be a factor for WakeupR generation 1：IRQ24 Interrupt can not be a factor for WakeupR generation
7	IRQ23M	0	R/W	IRQ23 Interrupt Mask Bit 0：IRQ23 Interrupt can be a factor for WakeupR generation 1：IRQ23 Interrupt can not be a factor for WakeupR generation
6	IRQ22M	0	R/W	IRQ22 Interrupt Mask Bit 0：IRQ22 Interrupt can be a factor for WakeupR generation 1：IRQ22 Interrupt can not be a factor for WakeupR generation
5	IRQ21M	0	R/W	IRQ21 Interrupt Mask Bit 0：IRQ21 Interrupt can be a factor for WakeupR generation 1：IRQ21 Interrupt can not be a factor for WakeupR generation
4	IRQ20M	0	R/W	IRQ20 Interrupt Mask Bit 0：IRQ20 Interrupt can be a factor for WakeupR generation 1：IRQ20 Interrupt can not be a factor for WakeupR generation
3	IRQ19M	0	R/W	IRQ19 Interrupt Mask Bit 0：IRQ19 Interrupt can be a factor for WakeupR generation 1：IRQ19 Interrupt can not be a factor for WakeupR generation
2	IRQ18M	0	R/W	IRQ18 Interrupt Mask Bit 0：IRQ18 Interrupt can be a factor for WakeupR generation 1：IRQ18 Interrupt can not be a factor for WakeupR generation
1	IRQ17M	0	R/W	IRQ17 Interrupt Mask Bit 0：IRQ17 Interrupt can be a factor for WakeupR generation 1：IRQ17 Interrupt can not be a factor for WakeupR generation
0	IRQ16M	0	R/W	IRQ16 Interrupt Mask Bit 0：IRQ16 Interrupt can be a factor for WakeupR generation 1：IRQ16 Interrupt can not be a factor for WakeupR generation

13.6.11 WakeupS Factor Mask Register2 (WUPSMSK2)

WUPSMSK is a 32-bit read/write register, which can be accessed only in long words. SYS-CPU Wakeup factor can be masked by setting this register.

The wakeup factor, which can be masked by this register, wakes up all the power off areas that are required to operate SYS CPU (A4S/A3SM). This register doesn't specify the areas that can be waken up by WakeUpS. This register is initialized on Power On Reset.

For power domain hierarchy, refer to section 13.7, Power Domain Specifications

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	MFISM	CPTR2SM
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IRQ31M	IRQ30M	IRQ29M	IRQ28M	IRQ27M	IRQ26M	IRQ25M	IRQ24M	IRQ23M	IRQ22M	IRQ21M	IRQ20M	IRQ19M	IRQ18M	IRQ17M	IRQ16M
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 18	—	ALL 0	R	Reserved When read, returns 0. The write value should always be 0
17	MFISM	0	R/W	MFIS Interrupt Mask Bit 0：MFIS Interrupt can be a factor for WakeupS generation 1：MFIS Interrupt can not be a factor for WakeupS generation
16	CPTR2S	0	R/W	CPTR2S Interrupt Mask Bit 0：CPTR2S Interrupt can be a factor for WakeupS generation 1：CPTR2S Interrupt can not be a factor for WakeupS generation
15	IRQ31M	0	R/W	IRQ31 Interrupt Mask Bit 0：IRQ31 Interrupt can be a factor for WakeupS generation 1：IRQ31 Interrupt can not be a factor for WakeupS generation
14	IRQ30M	0	R/W	IRQ30 Interrupt Mask Bit 0：IRQ30 Interrupt can be a factor for WakeupS generation 1：IRQ30 Interrupt can not be a factor for WakeupS generation
13	IRQ29M	0	R/W	IRQ29 Interrupt Mask Bit 0：IRQ29 Interrupt can be a factor for WakeupS generation 1：IRQ29 Interrupt can not be a factor for WakeupS generation
12	IRQ28M	0	R/W	IRQ28 Interrupt Mask Bit 0：IRQ28 Interrupt can be a factor for WakeupS generation 1：IRQ28 Interrupt can not be a factor for WakeupS generation

11	IRQ27M	0	R/W	IRQ27 Interrupt Mask Bit 0：IRQ27 Interrupt can be a factor for WakeupS generation 1：IRQ27 Interrupt can not be a factor for WakeupS generation
10	IRQ26M	0	R/W	IRQ26 Interrupt Mask Bit 0：IRQ26 Interrupt can be a factor for WakeupS generation 1：IRQ26 Interrupt can not be a factor for WakeupS generation
9	IRQ25M	0	R/W	IRQ25 Interrupt Mask Bit 0：IRQ25 Interrupt can be a factor for WakeupS generation 1：IRQ25 Interrupt can not be a factor for WakeupS generation
8	IRQ24M	0	R/W	IRQ24 Interrupt Mask Bit 0：IRQ24 Interrupt can be a factor for WakeupS generation 1：IRQ24 Interrupt can not be a factor for WakeupS generation
7	IRQ23M	0	R/W	IRQ23 Interrupt Mask Bit 0：IRQ23 Interrupt can be a factor for WakeupS generation 1：IRQ23 Interrupt can not be a factor for WakeupS generation
6	IRQ22M	0	R/W	IRQ22 Interrupt Mask Bit 0：IRQ22 Interrupt can be a factor for WakeupS generation 1：IRQ22 Interrupt can not be a factor for WakeupS generation
5	IRQ21M	0	R/W	IRQ21 Interrupt Mask Bit 0：IRQ21 Interrupt can be a factor for WakeupS generation 1：IRQ21 Interrupt can not be a factor for WakeupS generation
4	IRQ20M	0	R/W	IRQ20 Interrupt Mask Bit 0：IRQ20 Interrupt can be a factor for WakeupS generation 1：IRQ20 Interrupt can not be a factor for WakeupS generation
3	IRQ19M	0	R/W	IRQ19 Interrupt Mask Bit 0：IRQ19 Interrupt can be a factor for WakeupS generation 1：IRQ19 Interrupt can not be a factor for WakeupS generation
2	IRQ18M	0	R/W	IRQ18 Interrupt Mask Bit 0：IRQ18 Interrupt can be a factor for WakeupS generation 1：IRQ18 Interrupt can not be a factor for WakeupS generation
1	IRQ17M	0	R/W	IRQ17 Interrupt Mask Bit 0：IRQ17 Interrupt can be a factor for WakeupS generation 1：IRQ17 Interrupt can not be a factor for WakeupS generation
0	IRQ16M	0	R/W	IRQ16 Interrupt Mask Bit 0：IRQ16 Interrupt can be a factor for WakeupS generation 1：IRQ16 Interrupt can not be a factor for WakeupS generation

13.6.12 Standby Flag Register B (STBCHRn)

STBCHRn are 8-bit Read/Write registers. These registers are accessed byte wise. More over STBCHR0 to 3 are combined to form a single 32-bit register, in that case this register is accessed in long words. This register is defined purely for software purpose. Setting this register doesn't influence the LSI operation. As this bit is initialized only during Power On Reset caused by RESETP, the programmer can use this register at their convenience.

MMFROM uses STBCHRB2, STBCHRB3 registers. Refer to Appendix B, MMFROM programming specifications.

Bit	7	6	5	4	3	2	1	0
	STBBn[7:0]							
Initial Value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Initial Value	R/W	Description
7 to 0	STBBn[7:0]	B'00000000	R/W	defined purely for software purpose

13.6.13 Power Status Register (PSTR)

PSTR is a Read-Only 32 bit register. It can be accessed only in long words.

This Register indicates Power status of each area. When Power is supplied to an area the corresponding bit is read as 1 and reads as 0 when the power is not supplied.

For power domain hierarchy, refer to section 13.7, Power Domain Specifications

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	A3SGST	A3SMST	A3SPST	A4SST	–	A3RIST	–	A3RVST	A4RST	–	D4ST	A4MPST	A4LCST	C5ST
Initial Value	0	0	1	1	1	1	0	1	0	1	1	0	1	1	1	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Name	Initial Value	R/W	Description
31 to 14	—	ALL 0	R	Reserved When read, returns 0. The write access is prohibited.
13	A3SGST	1	R	A3SG Area Power Status Bit 0： Power is not supplied to A3SG area 1： Power is supplied to A3SG area
12	A3SMST	1	R	A3SM Area Power Status Bit 0： Power is not supplied to A3SM area 1： Power is supplied to A3SM area
11	A3SPST	1	R	A3SP Area Power Status Bit 0： Power is not supplied to A3SP area 1： Power is supplied to A3SP area
10	A4SST	1	R	A4S Area Power Status Bit 0： Power is not supplied to A4S area 1： Power is supplied to A4S area
9	—	0	R	Reserved When read, returns 0. The write access is prohibited.
8	A3RIST	1	R	A3RI Area Power Status Bit 0： Power is not supplied to A3RI area 1： Power is supplied to A3RI area
7	—	0	R	Reserved When read, returns 0. The write access is prohibited.

Bit	Name	Initial Value	R/W	Description
6	A3RVST	1	R	A3RV Area Power Status Bit 0： Power is not supplied to A3RV area 1： Power is supplied to A3RV area
5	A4RST	1	R	A4R Area Power Status Bit 0： Power is not supplied to A4R area 1： Power is supplied to A4R area
4	—	0	R	Reserved When read, returns 0. The write access is prohibited.
3	D4ST	1	R	D4 Area Power Status Bit 0： Power is not supplied to D4area 1： Power is supplied to D4area
2	A4MPST	1	R	A4MP Area Power Status Bit 0： Power is not supplied to A4MP area 1： Power is supplied to A4MP area
1	A4LCST	1	R	A4LC Area Power Status Bit 0： Power is not supplied to A4LC area 1： Power is supplied to A4LC area
0	C5ST	1	R	C5 Area Power Status Bit 0： Power is not supplied to C5area 1： Power is supplied to C5 area

13.6.14 EXTAL2 State Monitor Register (EXSTMON2)

EXSTMON2 is a Read-Only 32 bit register. It can be accessed only in long words.
The Status of the EXTAL2 clock is known from this register. The remaining time that the EXTAL2 clock could be in unstable state is also known from this register.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	EX2MSK
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RCNT[15:0]															
Initial Value	0	0	0	0	0	0	0	0	1	0	1	0	0	1	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Name	Initial Value	R/W	Description
31 to 17	—	ALL 0	R	Reserved When read, returns 0. The write access is prohibited.
16	EX2MSK	0	R	EXTAL2 input clock mask status bit 0：EXTAL2 clock is supplied to internal parts of LSI. 1：EXTAL2 clock is masked(clock is not stable)
15 to 0	RCNT[15:0]	H'00A4	R	Remaining Count These bits indicate the remaining count value (RCLKs) that is required by EXTAL2 to supply a stable clock. Refer to EXMSKCNT2.CNT [15:0] to setup the unstable clock time... When this value matches with EXMSKCNT2.CNT [15:0] EXTAL2 clock is said to be stabilized and supplied to internal parts of the LSI.

13.6.15 EXTAL1 State Monitor Register（EXSTMON1）

EXSTMON1 is a Read-Only 32 bit register. It can be accessed only in long words.
The Status of the EXTAL1 clock is known from this register. The remaining time that the EXTAL1 clock could be in unstable state is also known from this register.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	EX1MSK
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RCNT[15:0]															
Initial Value	0	0	0	0	0	0	0	0	1	0	1	0	0	1	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Name	Initial Value	R/W	Description
31 to 17	—	ALL 0	R	Reserved When read, returns 0. The write access is prohibited.
16	EX1MSK	0	R	EXTAL1 input clock mask status bit 0：EXTAL1 clock is supplied to internal parts of LSI. 1：EXTAL1 clock is masked(clock is not stable)
15 to 0	RCNT[15:0]	H'00A4	R	Remaining Count These bits indicate the remaining count value (RCLKs) that is required by EXTAL1 to supply a stable clock. Refer to EXMSKCNT1.CNT [15:0] to setup the unstable clock time... When this value matches with EXMSKCNT1.CNT [15:0] EXTAL1 clock is said to be stabilized and supplied to internal parts of the LSI.

13.6.16 WakeupR Interrupt Factor Register

WUPRFAC is a Read-Only 32 bit register. It can be accessed only in long words. The interrupt factor is cleared by reading this register. This register stores WakeUpR interrupt factor. Please read this register and clear the factor when wakeup process is completed. Moreover, please make sure that all factors are cleared before executing power down Sequence.

This register is cleared automatically when RT-CPU area's power supply is off.

For power domain hierarchy, refer to section 13.7, Power Domain's Specifications

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	-	-	-	-	-	MFISFC	CPTS2RFC	-	IRQFC	LCRCFC	KEYFC	CMTFC	ASBFC
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Name	Initial Value	R/W	Description
31 to 6	–	All 0	R	Reserved When read, returns 0. The write access is prohibited.
7	MFISFC	0	R	MFIS Interrupt Factor Bit 0：MFIS interrupt is not WakeupR interrupt factor 1：MFIS interrupt is WakeupR interrupt factor
6	CPTS2RFC	0	R	CPTS2R Interrupt Factor Bit 0：CPTS2R interrupt is not WakeupR interrupt factor 1：CPTS2R interrupt is WakeupR interrupt factor
5	–	0	R	Reserved When read, returns 0. The write access is prohibited.
4	IRQFC*	0	R	IRQ Interrupt Factor Bit 0：IRQ interrupt is not WakeupR interrupt factor 1：IRQ interrupt is WakeupR interrupt factor
3	LCRCFC	0	R	LCRC Interrupt Factor Bit 0：LCRC interrupt is not WakeupR interrupt factor 1：LCRC interrupt is WakeupR interrupt factor
2	KEYFC	0	R	KEYSC Interrupt Factor Bit 0：KEYSC interrupt is not WakeupR interrupt factor 1：KEYSC interrupt is WakeupR interrupt factor

Bit	Name	Initial Value	R/W	Description
1	CMTFC	0	R	CMT Interrupt Factor Bit 0：CMT interrupt is not WakeupR interrupt factor 1：CMT interrupt is WakeupR interrupt factor
0	ASBFC	0	R	ASEBRK Factor Bit 0：ASEBRK is not WakeUpR interrupt factor 1：ASEBRK is WakeUpR interrupt factor

13.6.17 WakeUpS Interrupt Factor Register (WUPSFAC)

WUPSFAC is a Read-Only 32 bit register. It can be accessed only in longwords. The interrupt factor is cleared by reading this register. This register stores WakeUpS interrupt factor. Please read this register and clear the factor when wakeup process is completed. Moreover, please make sure that all factors are cleared before executing power down Sequence.

This register is cleared automatically when SYS-CPU area's power supply is off.

For power domain hierarchy, refer to section 13.7, Power Domain's Specifications

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	-	MFISFC	CPTR2SFC	SPUFC	LCRCFC	-	MFIFC	EDBQFC	IRQFC	NMIFC	KEYFC	CMTFC	INTCAFC
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Name	Initial Value	R/W	Description
31 to 10	—	All 0	R	Reserved When read, returns 0. The write access is prohibited.
11	MFISFC	0	R	MFIS Interrupt Factor Bit 0：MFIS interrupt is not WakeupS interrupt factor 1：MFIS interrupt is WakeupS interrupt factor
10	CPTR2SFC	0	R	CPTR2S Interrupt Factor Bit 0：CPTR2S interrupt is not WakeupS interrupt factor 1：CPTR2S interrupt is WakeupS interrupt factor
9	SPUFC	0	R	SPU Interrupt Factor Bit 0：SPU interrupt is not WakeupS interrupt factor 1：SPU interrupt is WakeupS interrupt factor
8	LCRCFC	0	R	LCRC Interrupt Factor Bit 0：LCRC interrupt is not WakeupS interrupt factor 1：LCRC interrupt is WakeupS interrupt factor
7	—	0	R	Reserved When read, returns 0. The write access is prohibited.
6	MFIFC	0	R	INTREQ_MFI Interrupt Factor Bit 0：INTREQ_MFI interrupt is not WakeupS interrupt factor 1：INTREQ_MFI interrupt is WakeupS interrupt factor

Bit	Name	Initial Value	R/W	Description
5	EDBQFC	0	R	EDBGRQ Interrupt Factor Bit 0：EDBGRQ interrupt is not WakeupS interrupt factor 1：EDBGRQ interrupt is WakeupS interrupt factor
4	IRQFC*	0	R	IRQ Interrupt Factor Bit 0：IRQ interrupt is not WakeupS interrupt factor 1：IRQ interrupt is WakeupS interrupt factor
3	NMIFC	0	R	NMI Interrupt Factor Bit 0：NMI interrupt is not WakeupS interrupt factor 1：NMI interrupt is WakeupS interrupt factor
2	KEYFC	0	R	KEYSC Interrupt Factor Bit 0：KEYSC interrupt is not WakeupS interrupt factor 1：KEYSC interrupt is WakeupS interrupt factor
1	CMTFC	0	R	CMT Interrupt Factor Bit 0：CMT interrupt is not WakeupS interrupt factor 1：CMT interrupt is WakeupS interrupt factor
0	INTCAFC	0	R	INTCA Factor Bit 0： Interrupt from INTCA is not WakeupS interrupt factor 1： Interrupt from INTCA is WakeupS interrupt factor

13.6.18 RT Reset Flag Register (RRSTFR)

RRSTFR is a Read/Write 32 bit register. It can be accessed only in long words. However, the write access is performed only to clear the flag bits. Please access this register from RT-CPU. This register sets the reset flags when soft Power On Reset (Power On Reset other than RESETP_N) or system reset is detected. By reading this register at the time of reboot etc., it is known that what kind of reset was detected. These flags cannot be cleared during reset process (i.e. when Reset pin is still not released or reset bit is still not cleared).

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	RAMST	RASLV	RAPIN	RALNK
Initial Value	unknown												0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	(R/W)*1	(R/W)*1	(R/W)*1	(R/W)*1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RAWD1	RAWD2	-	-	-	-	-	-	RCLNK	-	RCPRES	RCWD1	RCWD2	RAF	-	RPF
Initial Value	0	0	unknown						0	0/1	0	0	0	0	0/1	0
R/W	(R/W)*1	(R/W)*1	R	R	R	R	R	R	(R/W)*1	R	(R/W)*1	(R/W)*1	(R/W)*1	(R/W)*1	R	(R/W)*1

Bit	Name	Initial Value	R/W	Description
31 to 20	—	UnKnown	R	Reserved When read, returns 0. The write value should always be 0.
19	RAMST	0	R/(W)*1	AP System Reset Factor Bit 0：RESCNT.MRES is not AP System reset factor. 1：RESCNT.MRES is AP System reset factor.
18	—	UnKnown	R	Reserved When read, returns 0. The write value should always be 0.
17	RAPIN	0	R/(W)*1	AP System Reset Factor Bit 0：RESETA_N is not AP System reset factor. 1：RESETA_N is AP System reset factor.
16	—	UnKnown	R	Reserved When read, returns 0. The write value should always be 0.
15	RAWD1	0	R/(W)*1	AP System Reset Factor Bit 0：RWDT0 is not AP System reset factor. 1：RWDT0 is AP System reset factor.
14 to 8	—	UnKnown	R	Reserved When read, returns 0. The write value should always be 0.
7	RCLNKA	0	R/(W)*1	Power On Reset Factor Bit 0：RESCNT. SRESLNKS is not soft Power On Reset factor. 1：RESCNT. SRESLNKS is soft Power On Reset factor.

6	－	UnKnown	R	Reserved When read, returns 0. The write value should always be 0.
5	RCPRES	0	R/(W)*1	Power On Reset Factor Bit 0：RESCNT2.PRES is not soft Power On Reset factor. 1：RESCNT2.PRES is soft Power On Reset factor.
4	RCWD1	0	R/(W)*1	Power On Reset Factor Bit 0：RWDT0 is not soft Power On Reset factor. 1：RWDT0 is soft Power On Reset factor.
3	－	UnKnown	R	Reserved When read, returns 0. The write value should always be 0.
2	RAF	0	R/(W)*1	AP Block system reset detection bit 0：Indicates AP Block System Reset is not detected. 1：Indicates AP Block System Reset is detected.
1	－	UnKnown	R	Reserved When read, returns 0. The write value should always be 0.
0	RPF	0	R/(W)*1	Power On Reset detection bit (soft Power On Reset) 0：Power On Reset other than RESETP_N is not detected. 1：Power On Reset other than RESETP_N is detected..

*Note *1 Write 0 to clear the flags. Write 1 to the other bits to avoid unintentional clears*
Regarding the systems which assert RESETA_N instead of RESETP_N during Cold Reset, initialization values for system reset detection bits may be '1'

13.6.19 SYS Reset Flag Register（SRSTFR）

SRSTFR is a Read/Write 32 bit register. It can be accessed only in long words. However, the write access is performed only to clear the flag bits. Please access this register from SYS-CPU. This register sets the reset flags when soft Power On Reset (Power On Reset other than RESETP_N) or system reset is detected. By reading this register at the time of reboot etc., it is known that what kind of reset was detected. These flags cannot be cleared during reset process. (I.e. when Reset pin is still not released or reset bit is still not cleared)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	RAMST	RASLV	RAPIN	RALNK
Initial Value	unknown												0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	(R/W)*1	(R/W)*1	(R/W)*1	(R/W)*1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RAWD1	RAWD2	-	-	-	-	-	-	RCLNK	-	RCPRES	RCWD1	RCWD2	RAF	-	RPF
Initial Value	0	0	unknown						0	0/1	0	0	0	0	0/1	0
R/W	(R/W)*1	(R/W)*1	R	R	R	R	R	R	(R/W)*1	R	(R/W)*1	(R/W)*1	(R/W)*1	(R/W)*1	R	(R/W)*1

Bit	Name	Initial Value	R/W	Description
31 to 20	—	UnKnown	R	Reserved When read, returns 0. The write value should always be 0.
19	RAMST	0	R/(W)*1	AP System Reset Factor Bit 0：RESCNT.MRES is not AP System reset factor. 1：RESCNT.MRES is AP System reset factor.
18	—	UnKnown	R	Reserved When read, returns 0. The write value should always be 0.
17	RAPIN	0	R/(W)*1	AP System Reset Factor Bit 0：RESETA_N is not AP System reset factor. 1：RESETA_N is AP System reset factor.
16	—	UnKnown	R	Reserved When read, returns 0. The write value should always be 0.
15	RAWD1	0	R/(W)*1	AP System Reset Factor Bit 0：RWDT0 is not AP System reset factor. 1：RWDT0 is AP System reset factor.
14 to 8	—	UnKnown	R	Reserved When read, returns 0. The write value should always be 0.
7	RCLNKA	0	R/(W)*1	Power On Reset Factor Bit 0：RESCNT. SRESLNKS is not soft Power On Reset factor 1：RESCNT. SRESLNKS is soft Power On Reset factor.

6	－	UnKnown	R	Reserved When read, returns 0. The write value should always be 0.
5	RCPRES	0	R/(W)*1	Power On Reset Factor Bit 0：RESCNT2.PRES is not soft Power On Reset factor. 1：RESCNT2.PRES is soft Power On Reset factor.
4	RCWD1	0	R/(W)*1	Power On Reset Factor Bit 0：RWDT0 is not soft Power On Reset factor. 1：RWDT0 is soft Power On Reset factor.
3	－	UnKnown	R	Reserved When read, returns 0. The write value should always be 0.
2	RAF	0	R/(W)*1	AP Block system reset detection bit 0：Indicates AP Block System Reset is not detected 1：Indicates AP Block System Reset is detected.
1	－	UnKnown	R	Reserved When read, returns 0. The write value should always be 0.
0	RPF	0	R/(W)*1	Power On Reset detection bit (soft Power On Reset) 0：Power On Reset other than RESETP_N is not detected 1：Power On Reset other than RESETP_N is detected.

Note *1 *Write 0 to clear the flags. Write 1 to the other bits to avoid unintentional clears*
Regarding the systems which assert RESETA_N instead of RESETP_N during Cold Reset, initialization values for system reset detection bits may be '1'.

13.6.20 Debug Mode Power Control Register（DGBPOWCR）

DGBPOWCR is a Read/Write 32 bit register. It can be accessed only in long words. This register is intended for debug purpose. This register controls the power supply of each power area during power down sequence. This register operation is enabled only when RESCNT.DBGNOPDNEN bit is set to 1.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	A3SGPD	A3SMPD	A3SPPD	A4SPD	—	A3RIPD	—	A3RVPD
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	A4RPD	—	D4PD	A4MPPD	A4LCPD	C5PD	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R

Bit	Name	Initial Value	R/W	Description
31 to 24	—	ALL 0	R	Reserved When read, returns 0. The write value should always be 0
23	A3SGPD	0	R/W*[1]	A3SG Area Power Control Bit Normal Mode (When Emulator is not connected) 0： A3SG Power Supply can be turned off 1： A3SG Power Supply can not be turned off Debug mode (When emulator is connected) 0： A3SG Power Supply can not be turned off 1： A3SG Power Supply can be turned off
22	A3SMPD	0	R/W*[1]	A3SM Area Power Control Bit Normal Mode (When Emulator is not connected) 0： A3SM Power Supply can be turned off 1： A3SM Power Supply can not be turned off Debug mode (When emulator is connected) 0： A3SM Power Supply can not be turned off 1： A3SM Power Supply can be turned off
21	A3SPPD	0	R/W*[1]	A3SP Area Power Control Bit Normal Mode (When Emulator is not connected) 0： A3SP Power Supply can be turned off 1： A3SP Power Supply can not be turned off Debug mode (When emulator is connected) 0： A3SP Power Supply can not be turned off 1： A3SP Power Supply can be turned off

20	A4SPD	0	R/W*[1]	A4S Area Power Control Bit Normal Mode (When Emulator is not connected) 0： A4S Power Supply can be turned off 1： A4S Power Supply can not be turned off Debug mode (When emulator is connected) 0： A4S Power Supply can not be turned off 1： A4S Power Supply can be turned off
19	—	0	R/W*1	Reserved When read, returns 0. The write value should always be 0.
18	A3RIPD	0	R/W*[1]	A3RI Area Power Control Bit Normal Mode (When Emulator is not connected) 0： A3RI Power Supply can be turned off 1： A3RI Power Supply can not be turned off Debug mode (When emulator is connected) 0： A3RI Power Supply can not be turned off 1： A3RI Power Supply can be turned off
17	—	0	R/W*1	Reserved When read, returns 0. The write value should always be 0.
16	A3RVPD	0	R/W*[1]	A3RV Area Power Control Bit Normal Mode (When Emulator is not connected) 0： A3RV Power Supply can be turned off 1： A3RV Power Supply can not be turned off Debug mode (When emulator is connected) 0： A3RV Power Supply can not be turned off 1： A3RV Power Supply can be turned off
15	A4RPD	0	R/W*[1]	A4R Area Power Control Bit Normal Mode (When Emulator is not connected) 0： A4R Power Supply can be turned off 1： A4R Power Supply can not be turned off Debug mode (When emulator is connected) 0： A4R Power Supply can not be turned off 1： A4R Power Supply can be turned off
14	—	0	R	Reserved When read, returns 0. The write value should always be 0.

13	D4PD	0	R/W*[1]	D4 Area Power Control Bit Normal Mode (When Emulator is not connected) 0： D4 Power Supply can be turned off 1： D4 Power Supply can not be turned off Debug mode (When emulator is connected) 0： D4 Power Supply can not be turned off 1： D4 Power Supply can be turned off
12	A4MPPD	0	R/W*[1]	A4MP Area Power Control Bit Normal Mode (When Emulator is not connected) 0： A4MP Power Supply can be turned off 1： A4MP Power Supply can not be turned off Debug mode (When emulator is connected) 0： A4MP Power Supply can not be turned off 1： A4MP Power Supply can be turned off
11	A4LCPD	0	R/W*[1]	A4LC Area Power Control Bit Normal Mode (When Emulator is not connected) 0： A4LC Power Supply can be turned off 1： A4LC Power Supply can not be turned off Debug mode (When emulator is connected) 0： A4LC Power Supply can not be turned off 1： A4LC Power Supply can be turned off
10	C5PD	0	R/W*[1]	C5 Area Power Control Bit Normal Mode (When Emulator is not connected) 0： C5 Power Supply can be turned off 1： C5 Power Supply can not be turned off Debug mode (When emulator is connected) 0： C5 Power Supply can not be turned off 1： C5 Power Supply can be turned off
9 to 0	—	ALL 0	R	Reserved When read, returns 0. The write value should always be 0.

*Note : *1 Initialized only on RESETP_N Power On Reset.*

13.6.21 RT Write Block Control Register（RWBCR）

RWBCR is a 32-bit read/write register, which can be accessed only in long words.
Setting bits of this register, prohibits write operations to the corresponding bits in RPDCR/RWUC. To prevent the unintentional power down wakeup operations of area whose power is not controlled from RT-CPU, write access to corresponding bits in RPDCR/RWUCR can be prohibited by setting this register. This register is initialized on Power On Reset.
For power domain hierarchy, refer to section 13.7, Power Domain Specifications.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	A3SGBL	A3SMBL	A3SPBL	A4SBL	-	A3RIBL	-	A3RVBL	A4RBL	-	D4BL	A4MPBL	A4LCBL	-
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R/W	R/W	R/W	R/W	R	R/W	R	R/W	R/W	R	R/W	R/W	R/W	R

Bit	Name	Initial Value	R/W	Description
31 to 14	—	ALL 0	R	Reserved When read, returns 0. The write value should always be 0.
13	A3SGBL	0	R/W	A3SG Power area mask bit 0：A3SG area's power is allowed to be controlled by RPDCR/RWUCR 1：A3SG area's power is not allowed to be controlled by RPDCR/RWUCR
12	A3SMBL	0	R/W	A3SM Power area mask bit 0：A3SM area's power is allowed to be controlled by RPDCR/RWUCR 1：A3SM area's power is not allowed to be controlled by RPDCR/RWUCR
11	A3SPBL	0	R/W	A3SP Power area mask bit 0：A3SP area's power is allowed to be controlled by RPDCR/RWUCR 1：A3SP area's power is not allowed to be controlled by RPDCR/RWUCR
10	A4SBL	0	R/W	A4S Power area mask bit 0：A4S area's power is allowed to be controlled by RPDCR/RWUCR 1：A4S area's power is not allowed to be controlled by RPDCR/RWUCR

Bit	Name	Initial Value	R/W	Description
9	—	0	R	Reserved When read, returns 0. The write value should always be 0
8	A3RIBL	0	R/W	A3RV Power area mask bit 0：A3RI area's power is allowed to be controlled by RPDCR/RWUCR 1：A3RI area's power is not allowed to be controlled by RPDCR/RWUCR
7	—	0	R	Reserved When read, returns 0. The write value should always be 0.
6	A3RVBL	0	R/W	A3RV Power area mask bit 0：A3RV area's power is allowed to be controlled by RPDCR/RWUCR 1：A3RV area's power is not allowed to be controlled by RPDCR/RWUCR
5	A4RBL	0	R/W	A4R Power area mask bit 0：A4R area's power is allowed to be controlled by RPDCR/RWUCR 1：A4R area's power is not allowed to be controlled by RPDCR/RWUCR
4	—	0	R	Reserved When read, returns 0. The write value should always be 0.
3	D4BL	0	R/W	D4 Power area mask bit 0：D4 area's power is allowed to be controlled by RPDCR/RWUCR 1：D4 area's power is not allowed to be controlled by RPDCR/RWUCR
2	A4MPBL	0	R/W	A4MP Power area mask bit 0：A4MP area's power is allowed to be controlled by RPDCR/RWUCR 1：A4MP area's power is not allowed to be controlled by RPDCR/RWUCR
1	A4LCBL	0	R/W	A4LC Power area mask bit 0：A4LC area's power is allowed to be controlled by RPDCR/RWUCR 1：A4LC area's power is not allowed to be controlled by RPDCR/RWUCR
4	—	0	R	Reserved When read, returns 0. The write value should always be 0.

13.6.22 SYS Write Block Control Register (SWBCR)

SWBCR is a 32-bit read/write register, which can be accessed only in long words.
Setting bits of this register, prohibits write operations to the corresponding bits in SPDCR/SWUC. To prevent the unintentional power down wakeup operations of area whose power is not controlled from SYS-CPU, write access to corresponding bits in SPDCR/SWUCR can be prohibited by setting this register. This register is initialized on Power On Reset.
For power domain hierarchy, refer to section 13.7, Power Domain Specifications.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	A3SGBL	A3SMBL	A3SPBL	A4SBL	-	A3RIBL	-	A3RVBL	A4RBL	-	D4BL	A4MPBL	A4LCBL	-
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R/W	R/W	R/W	R/W	R	R/W	R	R/W	R/W	R	R/W	R/W	R/W	R

Bit	Name	Initial Value	R/W	Description
31 to 14	—	ALL 0	R	Reserved When read, returns 0. The write value should always be 0.
13	A3SGBL	0	R/W	A3SG Power area mask bit 0：A3SG area's power is allowed to be controlled by SPDCR/SWUCR 1：A3SG area's power is not allowed to be controlled by SPDCR/SWUCR
12	A3SMBL	0	R/W	A3SM Power area mask bit 0：A3SM area's power is allowed to be controlled by SPDCR/SWUCR 1：A3SM area's power is not allowed to be controlled by SPDCR/SWUCR
11	A3SPBL	0	R/W	A3SP Power area mask bit 0：A3SP area's power is allowed to be controlled by SPDCR/SWUCR 1：A3SP area's power is not allowed to be controlled by SPDCR/SWUCR
10	A4SBL	0	R/W	A4S Power area mask bit 0：A4S area's power is allowed to be controlled by SPDCR/SWUCR 1：A4S area's power is not allowed to be controlled by SPDCR/SWUCR
9	—	0	R	Reserved When read, returns 0. The write value should always be 0.

Bit	Name	Initial Value	R/W	Description
8	A3RIBL	0	R/W	A3RV Power area mask bit 0：A3RI area's power is allowed to be controlled by SPDCR/SWUCR 1：A3RI area's power is not allowed to be controlled by SPDCR/SWUCR
7	—	0	R	Reserved When read, returns 0. The write value should always be 0.
6	A3RVBL	0	R/W	A3RV Power area mask bit 0：A3RV area's power is allowed to be controlled by SPDCR/SWUCR 1：A3RV area's power is not allowed to be controlled by SPDCR/SWUCR
5	A4RBL	0	R/W	A4R Power area mask bit 0：A4R area's power is allowed to be controlled by SPDCR/SWUCR 1：A4R area's power is not allowed to be controlled by SPDCR/SWUCR
4	—	0	R	Reserved When read, returns 0. The write value should always be 0.
3	D4BL	0	R/W	D4 Power area mask bit 0：D4 area's power is allowed to be controlled by SPDCR/SWUCR 1：D4 area's power is not allowed to be controlled by SPDCR/SWUCR
2	A4MPBL	0	R/W	A4MP Power area mask bit 0：A4MP area's power is allowed to be controlled by SPDCR/SWUCR 1：A4MP area's power is not allowed to be controlled by SPDCR/SWUCR
1	A4LCBL	0	R/W	A4LC Power area mask bit 0：A4LC area's power is allowed to be controlled by SPDCR/SWUCR 1：A4LC area's power is not allowed to be controlled by SPDCR/SWUCR
4	—	0	R	Reserved When read, returns 0. The write value should always be 0.

13.6.23 EXTAL2 Mask Count Register (EXMSKCNT2)

EXMSKCNT2 is a 32-bit read/write register, which can be accessed only in long words. EXTAL2 Clock supply to the internal parts of the LSI is masked when the clock is not stable using this register. Time required for EXTAL2 to supply a stable clock is set by this register in terms of RCLK. The initial value is H'A4 (164RCLK cycles = 5 ms). When setting this register, perform a 32 bit write operation by placing H'A55 to the upper 12bits in the data field.
This register is initialized by a Power On Reset.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	X2ON
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CNT[15:0]															
Initial Value	0	0	0	0	0	0	0	0	1	0	1	0	0	1	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Name	Initial Value	R/W	Description
31 to 17	—	ALL 0	R	Reserved When read, returns 0. The write value should be H'A550.
16	X2ON	0	R/W	Crystal Oscillator Control bit. 0：CPG holds the XTAL2 Crystal Oscillator control. 1：XTAL2 Crystal Oscillator is forcibly ON.
15 to 0	CNT[15:0]	H'00A4	R/W	UnStable clock time Time required for EXTAL2 to supply a stable clock is set by this register in terms of RCLK. When EXTAL2 is enabled, an internal counter starts counting up and continues to count up until the count value reaches CNT[15:0]. To know the remaining count value refer to EXSTMON2

13.6.24 EXTAL1 Mask Count Register (EXMSKCNT1)

EXMSKCNT1 is a 32-bit read/write register, which can be accessed only in long words. EXTAL1 Clock supply to the internal parts of the LSI is masked when the clock is not stable using this register. Time required for EXTAL1 to supply a stable clock is set by this register in terms of RCLK. The initial value is H'A4 (164RCLK cycles = 5 ms). When setting this register, perform a 32 bit write operation by placing H'A55 to the upper 12bits in the data field.
This register is initialized by a Power On Reset.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	X1ON
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CNT[15:0]															
Initial Value	0	0	0	0	0	0	0	0	1	0	1	0	0	1	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Name	Initial Value	R/W	Description
31 to 17	—	ALL 0	R	Reserved When read, returns 0. The write value should be H'A550.
16	X1ON	0	R/W	Crystal Oscillator Control bit. 0：CPG holds the XTAL1 Crystal Oscillator control. 1：XTAL1 Crystal Oscillator is forcibly ON.
15 to 0	CNT[15:0]	H'00A4	R/W	UnStable clock time Time required for EXTAL1 to supply a stable clock is set by this register in terms of RCLK. When EXTAL1 is enabled, an internal counter starts counting up and continues to count up until the count value reaches CNT[15:0]. To know the remaining count value refer to EXSTMON1.

13.6.25 Reset Control Register（RESCNT）

RESCNT is a 32-bit read/write register, which can be accessed only in long words. The initialization condition differs by bit. For details, refer to the description of each bit. This register is protected by HPB semaphore.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TST	MD4	MD3	MD2	MD6	MD7	–	–	RSTOUTSEL	DBGNOPDNEN	–	–	–	–	RESV	–
Initial value	TST	MD4	MD3	MD2	DM6	MD7	0/1	0/1	1	0	0/1	0/1	0/1	0/1	1	0/1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ROMMD[1:0]	–	ROBMD[1:0]	–	–	MSTPAS*3	MSTPAR*3	–	–	–	–	–	–	–	–	-
Initial Value	0	0/1	0	0/1	0/1	*1/0	*1/0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
R/W	R/W	R	R/W	R	R	R/W	R/W	R	R	R	R	R	R	R	R	R

Bit	Name	Initial Value	R/W	Description
31	/TST*[1]	/TST	R	TST_N Pin Monitor TST_N Pin level is monitored. 0：TST_N Pin level is 0 at Power On 1：TST_N Pin level is 1 at Power On This bit captures the TST_ Nin value at Power On Reset.
30	MD4*[1]	MD4	R	MD4 Pin Monitor MD4 Pin level is monitored. 0：MD4 Pin level is 0 at Power On 1：MD4 Pin level is 1 at Power On This bit captures the MD4in value at Power On Reset.
29	MD3*[1]	MD3	R	MD3 Pin Monitor MD3 Pin level is monitored. 0：MD3 Pin level is 0 at Power On 1：MD3 Pin level is 1 at Power On This bit captures the MD3in value at Power On Reset.
28	MD2*[1]	MD2	R	MD2 Pin Monitor MD2 Pin level is monitored. 0：MD2 Pin level is 0 at Power On 1：MD2 Pin level is 1 at Power On This bit captures the TST_ Pin value at Power On Reset.

Bit	Name	Initial Value	R/W	Description
27	MD6*[1]	MD6	R	MD6 Pin Monitor MD6 Pin level is monitored. 0：MD6 Pin level is 0 at Power On 1：MD6 Pin level is 1 at Power On This bit captures the TST_ Pin value at Power On Reset.
26	MD7*[1]	MD7	R	MD7 Pin Monitor MD7 Pin level is monitored. 0：MD7 Pin level is 0 at Power On 1：MD7 Pin level is 1 at Power On This bit captures the TST_ Pin value at Power On Reset.
25 to 24	—	UnKnown	R	Reserved When read, returns 0. The writing perform a Read-Modify-Write.
23	RSTOUTSEL	1	R/W	RESETOUTS_N pin's assert condition selection bit This bit in conjunction with ROBMD[1:0] controls the assert condition for RESETOUTS output pins. Refer to ROBMD[1:0] bits for different conditions. This bit is initialized only when hard Power On Reset. 0：RESETOUTS_N pin is asserted when processor reset is asserted 1：RESETOUTS_N pin is asserted when system reset is asserted *Note : RESETOUTS_N pin active period depends upon various factors like areas whose power is turned down, extal2/1 status, type of reset it is connected to, etc., The minimum and maximum periods are 40uS/5.5mS respectively*
22	DBGNOPDNEN	0	R/W	DBGPOWCR Enable bit 0： Disable DBGPOWCR Register functionality 1： Enable DBGPOWCR Register functionality This bit is initialized only when hard Power On Reset
21 to 20	—	UnKnown	R	Reserved When read, returns 0. The writing perform a Read-Modify-Write.
19	SRESLNK	1	R/W	System reset domain selection bit This bit selects the power areas which are initialized on system reset. This bit is initialized on Power On Reset. 0: All power areas excluding C5, and D4 are initialized 1: All power areas including C5, and D4 are initialized
18	—	UnKnown	R	Reserved When read, returns 0. The writing perform a Read-Modify-Write.
17	RESV	1	R/W	RESETA_N Pin enable bit This bit indicates whether RESETA_N is enabled or disabled. This bit is initialized on Power On Reset. 0：RESETA_N Pin is disabled 1：RESETA_N Pin is enabled

Bit	Name	Initial Value	R/W	Description
16	－	UnKnown	R	Reserved When read, returns 0. The writing perform a Read-Modify-Write.
15, 14	－	00	R	Reserved When read, returns 0. The writing perform a Read-Modify-Write.
13, 12	ROBMD[1:0]	00	R/W	RESETOUTS_N Pin assert condition Indicates RESETOUTS_N assert condition. This bit is initialized on Power On Reset. When RSTOUTSEL＝0 00：Reserved 01：Reserved 10：RESETOUTS_N is asserted along with processor reset 11：Reserved When RSTOUTSEL＝0 00：Reserved 01：Reserved 10：RESETOUTS_N is asserted along with System reset 11：Reserved
11	－	UnKnown	R	Reserved When read, returns 0. The writing perform a Read-Modify-Write.
10	MSTPAS	*2	R/W	SYS-CPU Module stop This bit is used to stop System CPU's clock and hold the boot start process after a system reset is released. This bit should only be used when the master processor controls the boot sequence of the slave CPU. In RT master mode, activate System CPUs by clearing MSTPS bit to 0. When System CPU is the master processor, this bit is set to 1 as the initial value. This bit is initialized on Power On Reset. 0：clock is supplied 1：clock is stopped
9	MSTPAR	*2	R/W	RT-CPU Module stop This bit is used to stop Real-time CPU's clock and hold the boot start process after a system reset is released. This bit should only be used when the master processor controls the boot sequence of the slave CPU. In SYS master mode, activate RT CPUs by clearing MSTPR bit to 0. When RT CPU is the master processor, this bit is set to 1 as the initial value. This bit is initialized on Power On Reset. 0：clock is supplied 1：clock is stopped
8 to 0	－	UnKnown	R	Reserved When read, returns 0. The writing perform a Read-Modify-Write

*Note: *1. The boot mode depends on the TST_N, MD4, MD3, MD2, MD6 and MD7 pin settings. For details*

on the boot mode, refer to section 13.3, Operating Modes.

**2. Depends on the setting of the TST_N, MD4, MD3, MD2, MD6 and MD7 Mode pins*

13.6.26 Reset Control Register2（RESCNT2）

RESCNT2 is a 32-bit read/write register, which can be accessed only in long words. The initialization condition differs by bit. For details, refer to the description of each bit. This register is protected by HPB semaphore.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PRES	—	MRES	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0/1	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
R/W :	R/W	R	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RWD1A		RWD0A		—	—	—	—	CKE MD10	—	CKE MD20	—	—	RAFLG	—	—
Initial Value	1	1	1	1	0/1	0/1	0/1	0/1	0	0/1	0	0/1	0/1	0	0/1	0/1
R/W :	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R	R/W	R	R	R	R	R

Bit	Name	Initial Value	R/W	Description
31	PRES	0	R/W	Soft Power On Reset Soft Power On Reset is asserted. This bit is initialized on Power On Reset. 0：Ignored 1：Power On Reset is asserted. *Note: Soft Power On Reset is asserted when 1 is written to this bit. When Power On Reset process is completed, this bit gets cleared. (All power areas including C5, and D4 are initialized)*
30	—	UnKnown	R	Reserved When read, returns 0. The writing perform a Read-Modify-Write
29	MRES	0	R/W	System reset. System reset is asserted. This bit is initialized on Power On Reset. 0：Ignored. 1：system reset is asserted. *Note: This bit is cleared by hardware automatically. SRESLNK bit selects the system reset domain.*
28 to 16	—	UnKnown	R	Reserved When read, returns 0. The writing perform a Read-Modify-Write
15 to 14	—	UnKnown	R	Reserved When read, returns 0. The writing performa Read-Modify-Write

Bit	Name	Initial Value	R/W	Description
13 to 12	RWD0A	1	R/W	RWDT0-system reset selection bit These bits select whether to generate a system reset or soft Power On Reset on RWDT0 expiration. This bit is initialized on Power On Reset. 00：Reserved 01：Reserved 10：System Reset is asserted 11：Soft Power On Reset is asserted
11 to 8	－	UnKnown	R	Reserved When read, returns 0. The writing perform a Read-Modify-Write
7	CKEMD10	0	R/W	LPACKEA/B out put control bit This bit control LPACKEA/B out put during SBSC1 reset period（during Power On Reset, System reset, A4S power is turned off ） 0： LPACKEA/B of SBSC1 is set to low 1： LPACKEA/B of SBSC1 is set to High This bit is initialized only on RESETP_N Power On Reset
6	－	UnKnown	R	Reserved When read, returns 0. The writing perform a Read-Modify-Write
5	－	0	R	Reserved When read, returns 0. The writing perform a Read-Modify-Write
4 to 3	－	UnKnown	R	Reserved When read, returns 0. The writing perform a Read-Modify-Write
2	RAFLG*[1]	0	R	System Reset Flag bit This bit is set when System Reset is asserted. This bit is initialized on Power On Reset. 0：System reset is not asserted 1：System reset is asserted
1 to 0	－	UnKnown	R	Reserved When read, returns 0. The writing perform a Read-Modify-Write

*Note : *1 Reset flag bit is cleared automatically when RESCNT2 register is read.*

13.6.27 Wakeup Area Selection Register (WUPSEL)

WUPSEL is a 32-bit read/write register, which can be accessed only in long words. By setting this register areas other than CPU can be waken up by Wakeup* interrupts.

This register is initialized on Power On Reset.

For power domain hierarchy, refer to section 13.7, Power Domain Specifications

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	A3SGWU					A3SPWU					–			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	A3RVWU					A4MPWU					A4LCWU				
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Initial Value	R/W	Description
31, 30	—	ALL 0	R	Reserved When read, returns 0. The writing perform a Read-Modify-Write
29 to 25	A3SGWU[4:0]	00000	R/W	A3SG Wakeup interrupt selection bits Selects WakeUp* interrupt signal by which A3SG can be waken up. 0：A3SG area is not waken up by WakeUp* interrupt 1：A3SG area can be waken up by WakeUp* interrupt A3SG WU[4]： wake up by WakeUpR interrupt A3SG WU[3]： wake up by WakeUpS interrupt A3SG WU[2:0]：Reserved
24 to 20	A3SPWU[4:0]	00000	R/W	A3SP Wakeup interrupt selection bits Selects WakeUp* interrupt signal by which A3SP can be waken up. 0：A3SP area is not waken up by WakeUp* interrupt 1：A3SP area can be waken up by WakeUp* interrupt A3SP WU[4]： wake up by WakeUpR interrupt A3SP WU[3]： wake up by WakeUpS interrupt A3SP WU[2:0]：Reserved
19 to 15	—	ALL 0	R	Reserved When read, returns 0. The writing perform a Read-Modify-Write

Bit	Name	Initial Value	R/W	Description
14 to 10	A3RVWU[4:0]	00000	R/W	A3RV Wakeup interrupt selection bits Selects WakeUp* interrupt signal by which A3RV can be waken up. 0：A3RV area is not waken up by WakeUp* interrupt 1：A3RV area can be waken up by WakeUp* interrupt A3RV WU[4]： wake up by WakeUpR interrupt A3RV WU[3]： wake up by WakeUpS interrupt A3RV WU[2:0]：Reserved
9 to 5	A4MPWU[4:0]	00000	R/W	A4MP Wakeup interrupt selection bits Selects WakeUp* interrupt signal by which A4MP can be waken up. 0：A4MP area is not waken up by WakeUp* interrupt 1：A4MP area can be waken up by WakeUp* interrupt A4MP WU[4]： wake up by WakeUpR interrupt A4MP WU[3]： wake up by WakeUpS interrupt A4MP WU[2:0]：Reserved
4 to 0	A4LCWU[4:0]	00000	R/W	A4LC Wakeup interrupt selection bits Selects WakeUp* interrupt signal by which A4LC can be waken up. 0：A4LC area is not waken up by WakeUp* interrupt 1：A4LC area can be waken up by WakeUp* interrupt A4LC WU[4]： wake up by WakeUpR interrupt A4LC WU[3]： wake up by WakeUpS interrupt A4LC WU[2:0]：Reserved

13.6.28 Interrupt Detection Mode Control Register （IRQCR）

IRQCR is a 32-bit read/write register, which can be accessed only in long words. IRQ detection mode is determined by this register.

This register is initialized on Power On Reset.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IRQ15S[1:0]		IRQ14S[1:0]		IRQ13S[1:0]		IRQ12S[1:0]		IRQ11S[1:0]		IRQ10S[1:0]		IRQ9S[1:0]		IRQ8S[1:0]	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IRQ7S[1:0]		IRQ6S[1:0]		IRQ5S[1:0]		IRQ4S[1:0]		IRQ3S[1:0]		IRQ2S[1:0]		IRQ1S[1:0]		IRQ0S[1:0]	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Initial Value	R/W	Description
31, 30	IRQ15S[1:0]	00	R/W	IRQn detection mode selection bits（n=0 to 15）
29, 28	IRQ14S[1:0]	00	R/W	Interrupt pin IRQ0 to IRQ15 is detected in one of the following four modes.
27, 26	IRQ13S[1:0]	00	R/W	Rising edge, Falling edge, High-level, Low level
25, 24	IRQ12S[1:0]	00	R/W	IRQnS[1:0]=00：A Falling edge on IRQn is detected as Interrupt request
23, 22	IRQ11S[1:0]	00	R/W	IRQnS[1:0]=01：A Rising edge on IRQn is detected as Interrupt request
21, 20	IRQ10S[1:0]	00	R/W	IRQnS[1:0]=10：A Low-level on IRQn is detected as interrupt request.
19, 18	IRQ9S[1:0]	00	R/W	IRQnS[1:0]=11：A High-level on IRQn is detected as interrupt request
17, 16	IRQ8S[1:0]	00	R/W	
15, 14	IRQ7S[1:0]	00	R/W	* When IRQn is set to be detected by both edges, set 00 to these bits.
13, 12	IRQ6S[1:0]	00	R/W	
11, 10	IRQ5S[1:0]	00	R/W	
9, 8	IRQ4S[1:0]	00	R/W	
7, 6	IRQ3S[1:0]	00	R/W	
5, 4	IRQ2S[1:0]	00	R/W	
3, 2	IRQ1S[1:0]	00	R/W	
1, 0	IRQ0S[1:0]	00	R/W	

13.6.29 EXTAL1 Clock Stop Control Register (APSCSTP)

APSCSTP is a 32-bit read/write register, which can be accessed only in long words. This register can be used to generate EXTAL1 oscillator stop request when the desired power areas are shut down. Setting a particular bit also sets other bits, which are having hierarchal relation with that bit. For example, if A4S is set, A3SM, A3SP are also set automatically.

This register is initialized on Power On Reset.

For power domain hierarchy, refer to section 13.7, Power Domain Specifications.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	A3SG STP	A3SM STP	A3SP STP	-	-	A3RI STP	-	A3RV STP	A4RS TP	A4GP STP	D4 STP	A4MP STP	A4LC STP	-
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R

Bit	Name	Initial Value	R/W	Description
31 to 14	—	ALL 0	R	Reserved When read, returns 0. The write value should always be 0.
13	A3SGSTP	0	R/W	Generate Oscillator stop request on A3SG shut down 0：Oscillator Stop Request does not follow A3SG power status 1：Oscillator Stop request is generated when A3SG is shut down
12	A3SMSTP	0	R/W	Generate Oscillator stop request on A3SM shut down 0：Oscillator Stop Request does not follow A3SM power status 1：Oscillator Stop request is generated when A3SM is shut down
11	A3SPSTP	0	R/W	Generate Oscillator stop request on A3SP shut down 0：Oscillator Stop Request does not follow A3SP power status 1：Oscillator Stop request is generated when A3SP is shut down
10	—	0	R	Reserved When read, returns 0. The write value should always be 0.
9	—	0	R	Reserved When read, returns 0. The write value should always be 0.
8	A3RISTP	0	R/W	Generate Oscillator stop request on A3RI shut down 0：Oscillator Stop Request does not follow A3RI power status 1：Oscillator Stop request is generated when A3RI is shut down
7	—	0	R	Reserved When read, returns 0. The write value should always be 0.

Bit	Name	Initial Value	R/W	Description
6	A3RVSTP	0	R/W	Generate Oscillator stop request on A3RV shut down 0：Oscillator Stop Request does not follow A3RV power status 1：Oscillator Stop request is generated when A3RV is shut down
5	A4RSTP	0	R/W	Generate Oscillator stop request on A4R shut down 0：Oscillator Stop Request does not follow A4R power status 1：Oscillator Stop request is generated when A4R is shut down
4	—	0	R	Reserved When read, returns 0. The write value should always be 0.
3	D4STP	0	R/W	Generate Oscillator stop request on D4 shut down 0：Oscillator Stop Request does not follow D4 power status 1：Oscillator Stop request is generated when D4 is shut down
2	A4MPSTP	0	R/W	Generate Oscillator stop request on A4MP shut down 0：Oscillator Stop Request does not follow A4MP power status 1：Oscillator Stop request is generated when A4MP is shut down
1	A4LCSTP	0	R/W	Generate Oscillator stop request on A4LC shut down 0：Oscillator Stop Request does not follow A4LC power status 1：Oscillator Stop request is generated when A4LC is shut down
0	—	0	R	Reserved When read, returns 0. The write value should always be 0.

13.6.30 IRQ Detection Mode control Register2（IRQCR2）

IRQCR is a 32-bit read/write register, which can be accessed only in long words. IRQ detection mode is determined by this register.

This register is initialized on Power On Reset.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IRQ15S2[1:0]		IRQ14S2[1:0]		IRQ13S2[1:0]		IRQ12S2[1:0]		IRQ11S2[1:0]		IRQ10S2[1:0]		IRQ9S2[1:0]		IRQ8S2[1:0]	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IRQ7S2[1:0]		IRQ6S2[1:0]		IRQ5S2[1:0]		IRQ4S2[1:0]		IRQ3S2[1:0]		IRQ2S2[1:0]		IRQ1S2[1:0]		IRQ0S2[1:0]	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Initial Value	R/W	Description
31, 30	IRQ15S2[1:0]	00	R/W	IRQn Detection mode selection bits2（n=0 to 15） Set these bits only when IRQ0 to IRQ15 pins are detected on both edges. IRQnS2[1:0]=00：Detection mode is decided by IRQns[1:0] bits. IRQnS2[1:0]=01：Interrupt is detected on both edges IRQnS2[1:0]=1x：Prohibited * When IRQn set to be detected by both edges, set 00 to IRQnS bits.
29, 28	IRQ14S2[1:0]	00	R/W	
27, 26	IRQ13S2[1:0]	00	R/W	
25, 24	IRQ12S2[1:0]	00	R/W	
23, 22	IRQ11S2[1:0]	00	R/W	
21, 20	IRQ10S2[1:0]	00	R/W	
19, 18	IRQ9S2[1:0]	00	R/W	
17, 16	IRQ8S2[1:0]	00	R/W	
15, 14	IRQ7S2[1:0]	00	R/W	
13, 12	IRQ6S2[1:0]	00	R/W	
11, 10	IRQ5S2[1:0]	00	R/W	
9, 8	IRQ4S2[1:0]	00	R/W	
7, 6	IRQ3S2[1:0]	00	R/W	
5, 4	IRQ2S2[1:0]	00	R/W	
3, 2	IRQ1S2[1:0]	00	R/W	
1, 0	IRQ0S2[1:0]	00	R/W	

13.6.31 IRQ Detection Mode Control Register3（IRQCR3）

IRQCR is a 32-bit read/write register, which can be accessed only in long words. IRQ detection mode is determined by this register.

This register is initialized on Power On Reset.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IRQ31S[1:0]		IRQ30S[1:0]		IRQ29S[1:0]		IRQ28S[1:0]		IRQ27S[1:0]		IRQ26S[1:0]		IRQ25S[1:0]		IRQ24S[1:0]	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IRQ23S[1:0]		IRQ22S[1:0]		IRQ21S[1:0]		IRQ20S[1:0]		IRQ19S[1:0]		IRQ18S[1:0]		IRQ17S[1:0]		IRQ16S[1:0]	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Initial Value	R/W	Description
31, 30	IRQ31S[1:0]	00	R/W	IRQn detection mode selection bits（n=16 to 31）
29, 28	IRQ30S[1:0]	00	R/W	Interrupt pin IRQ16 to IRQ31 is detected in one of the following four modes.
27, 26	IRQ29S[1:0]	00	R/W	Rising edge, Falling edge, High-level, Low level
25, 24	IRQ28S[1:0]	00	R/W	IRQnS[1:0]=00：A Falling edge on IRQn is detected as Interrupt request
23, 22	IRQ27S[1:0]	00	R/W	IRQnS[1:0]=01：A Rising edge on IRQn is detected as Interrupt request
21, 20	IRQ26S[1:0]	00	R/W	IRQnS[1:0]=10：A Low-level on IRQn is detected as interrupt request.
19, 18	IRQ25S[1:0]	00	R/W	IRQnS[1:0]=11：A High-level on IRQn is detected as interrupt request
17, 16	IRQ24S[1:0]	00	R/W	
15, 14	IRQ23S[1:0]	00	R/W	* When IRQn is set to be detected by both edges, set 00 to these bits.
13, 12	IRQ22S[1:0]	00	R/W	
11, 10	IRQ21S[1:0]	00	R/W	
9, 8	IRQ20S[1:0]	00	R/W	
7, 6	IRQ19S[1:0]	00	R/W	
5, 4	IRQ18S[1:0]	00	R/W	
3, 2	IRQ17S[1:0]	00	R/W	
1, 0	IRQ16S[1:0]	00	R/W	

13.6.32 IRQ Detection Mode Control Register4（IRQCR4）

IRQCR is a 32-bit read/write register, which can be accessed only in long words. IRQ detection mode is determined by this register.

This register is initialized on Power On Reset.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IRQ31S2[1:0]		IRQ30S2[1:0]		IRQ29S2[1:0]		IRQ28S2[1:0]		IRQ27S2[1:0]		IRQ26S2[1:0]		IRQ25S2[1:0]		IRQ24S2[1:0]	
nitial Valu	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IRQ23S2[1:0]		IRQ22S2[1:0]		IRQ21S2[1:0]		IRQ20S2[1:0]		IRQ19S2[1:0]		IRQ18S2[1:0]		IRQ17S2[1:0]		IRQ16S2[1:0]	
nitial Valu	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Initial Value	R/W	Description
31, 30	IRQ31S2[1:0]	00	R/W	IRQn Detection mode selection bits2（n=16 to 31） Set these bits only when IRQ16 to IRQ31 pins are detected on both edges. IRQnS2[1:0]=00：Detection mode is decided by IRQns[1:0] bits. IRQnS2[1:0]=01：Interrupt is detected on both edges IRQnS2[1:0]=1x：Prohibited * When IRQn set to be detected by both edges, set 00 to IRQnS bits.
29, 28	IRQ30S2[1:0]	00	R/W	
27, 26	IRQ29S2[1:0]	00	R/W	
25, 24	IRQ28S2[1:0]	00	R/W	
23, 22	IRQ27S2[1:0]	00	R/W	
21, 20	IRQ26S2[1:0]	00	R/W	
19, 18	IRQ25S2[1:0]	00	R/W	
17, 16	IRQ24S2[1:0]	00	R/W	
15, 14	IRQ23S2[1:0]	00	R/W	
13, 12	IRQ22S2[1:0]	00	R/W	
11, 10	IRQ21S2[1:0]	00	R/W	
9, 8	IRQ20S2[1:0]	00	R/W	
7, 6	IRQ19S2[1:0]	00	R/W	
5, 4	IRQ18S2[1:0]	00	R/W	
3, 2	IRQ17S2[1:0]	00	R/W	
1, 0	IRQ16S2[1:0]	00	R/W	

13.6.33 EXTAL1 Control Register（SYCKENMSK）

SYCKENMSK is a 32-bit read/write register, which can be accessed only in long words. This register can be used to select the EXTAL1 enable events. This register is initialized on Power On Reset.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	-	-	—	—	—	-	EXTAL1MSK			—	—	-	-
Initial Value	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R

Bit	Name	Initial Value	R/W	Description
31 to 7	—	ALL 0	R	Reserved When read, returns 0. The write value should always be 0
6	EXTAL1MSK[2]	1	R/W	A4S area's Oscillator ON request 0： EXTAL1 cannot be stopped when A4S area's power is ON 1： EXTAL1 can be stopped even when A4S area's power is ON
5	—	1	R	Reserved When read, returns 0. The write value should always be 0
4	EXTAL1MSK[0]	1	R/W	SPU's Oscillator ON request 0： EXTAL1 On Request from SPU enables EXTAL1 1： EXTAL1 On Request from SPU is masked.
3 to 0	—	ALL 0	R	Reserved When read, returns 0. The write value should always be 0

13.6.34 A4S Area Power Control Register（A4SPOWCR）

A4SPOWCR is a 32-bit read/write register, which can be accessed only in long words. This register can be use to select A4S area's power on/off request. This register is initialized on Power On Reset.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	SPC4MSK	EXTMSK
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Name	Initial Value	R/W	Description
31 to 4	−	ALL 0	R	Reserved When read, returns 0. The write value should always be 0.
4	−	0	R	Reserved When read, returns 0. The write value should always be 0.
3	−	1	R	Reserved When read, returns 1. The write value should always be 0.
2	−	1	R	Reserved When read, returns 1. The write value should always be 0.
1	SPA4SMSK	1*[1]	R/W	SPU's A4S On/OFF request mask bit 0：A4S area's power is controlled by SPU's request 1：SPU's request is masked
0	EXA4SMSK	1*[2]	R/W	EXTALB1's A4S On/OFF request mask bit 0：A4S areas Power cannot be turned down when EXTAL1 is on 1：A4S areas power can be turned down even when EXTAL1 is on

*Note: *1 {SPA4SMSK, SYCKENMSK. EXTAL1MSK[0]} = 01,10 setting is prohibited*

**2 {EXA4SMSK, SYCKENMSK. EXTAL1MSK[2]} = 01,10 setting is prohibited*

13.6.35 WakeUp Area Selection Register2 (WUPSEL2)

WUPSEL is a 32-bit read/write register, which can be accessed only in long words. By setting this register areas other than CPU can be waken up by Wakeup* interrupts.

This register is initialized on Power On Reset.

For power domain hierarchy, refer to section 13.7, Power Domain Specifications

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	A3RIWU			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	A3RIWU	A4SWU	–	–	–	–	D4WU					C4WU				
Initial Value	0	1	0	0	0	0	0	0	0	0	0	1	1	1	1	1
R/W	R	R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Initial Value	R/W	Description
31 to 15	–	ALL 0	R	Reserved When read, returns 0. The write value should always be 0
19 to 15	A3RIWU[4:0]	00000	R/W	A3RI Wakeup interrupt selection bits Selects WakeUp* interrupt signal by which A3RI can be waken up. 0：A3RI area is not waken up by WakeUp* interrupt 1：A3RI area can be waken up by WakeUp* interrupt A3RI WU[4]： wake up by WakeUpR interrupt A3RI WU[3]： wake up by WakeUpS interrupt A3RI WU[2:0]：Reserved
14	A4SWU	1	R/W	A4S Wakeup interrupt selection bits This bit enables A4S area to wake up with WakeUpR interrupt signal 0：WakepR interrupt cannot wakeup A4S area 1：WakeupR interrupt wakeup A4S area
13 to 10	–	ALL 0	R	Reserved When read, returns 0. The write value should always be 0
9 to 5	D4WU[4:0]	00000	R/W	D4 Wakeup interrupt selection bits Selects WakeUp* interrupt signal by which D4 can be waken up. 0：D4 area is not waken up by WakeUp* interrupt 1：D4 area can be waken up by WakeUp* interrupt D4 WU[4]： wake up by WakeUpR interrupt D4 WU[3]： wake up by WakeUpS interrupt D4 WU[2:0]：Reserved
4 to 0	-	11111	R	Reserved When read, returns 11111. The write value should always be 11111

13.6.36 A4S Area Power Control Register2 (PDNSEL)

PDNSEL is a 32-bit read/write register, which can be accessed only in long words. By setting this register, A4S areas power can be turned down automatically. When the power of the areas set in this register is turned off, Power of A4S area also turns down automatically. When multiple bits in this register are set, A4S power is turned off when all the areas set in this register are turned off. This register is initialized on Power On Reset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	A4SPD[3:0]			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Name	Initial Value	R/W	Description
31 to 4	–	ALL 0	R	Reserved When read, returns 0. The write value should always be 0
3 to 0	A4SPD[3:0]	1111	R/W	A4S Power down selection bits 0：A4S power down request is not generated 1：A4S power down request is generated. A4SPD[3]：A3SM power down request generates A4S power down request A4SPD[2]：A3SP power down request generates A4S power down request A4SPD[1]：A3SG power down request generates A4S power down request A4SPD[0]：A4R power down request generates A4S power down request

13.7 Power Domain Specifications

13.7.1 Power Area hierarchy

This LSI consists of 12 power areas. The hierarchal relationship between the power areas is shown in the following figure.

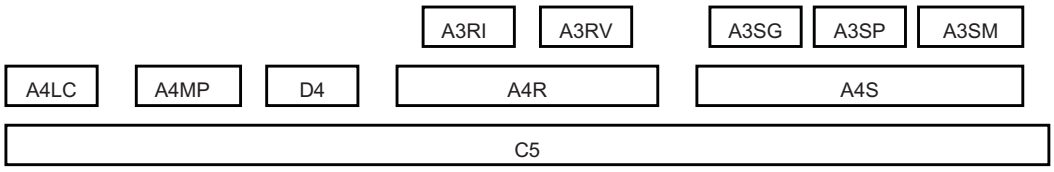


Fig 13.2 Power area hierarchy

13.7.2 Area wise module list

Modules that are placed in each power area are listed in the following table.

13.6 Module list separated by power area

	Area	Module
Common	C5	SYSC, WUC, PowerControlParts, GPIO, PAD (IO macro), HDMI-Phy, DBG Backup registers, CPG, CMT1/2/3/4, RWDT, KEYSC, SMFRAM
Debug	D4	Coresight-ETM
System	A4S	Common-SHwy, Common-HPB, BSC, MFIS,MFIM, MMFROM ACMFI1,ACMFI2, HS-SHwy, SYS-HPB, INTCA modules, SBSC
	A3SM	System CPU (Cortex-A8)
	A3SP	DMAC1/2/3, IPMMUD, DDM, FLCTL, SYS-HPB, BBIF1, MSIOF1/2, SCIFA,SCIFB, IIC1/3/4, IrDA, HDMI-Link, USBHS0/1, USBDMAC, SDHI0/1/2, CMT1, TPU, Crypt, DREQPAK (Sys), MIPI-HSI, MMCIF
	A3SG	SGX540
Realtime	A4R	Realtime CPU(SH-X2), Realtime CPU debug modules, H-UDI, RT-SHwy, INTCS modules, RT-HPB, TSIF, VPU, CEU, VEU, BEU, VOU, JPU, RTDMAC1/2,TSIF TMU, IIC0/2, MSIOF0, CMT0, ICB, DREQPAK (RT), 2DDMAC, IPMMUI,IPMMUR, IPMMUR2, CSI2
	A3RV	VPU
	A3RI	ISP
	A4LC	MERAM, LCDC, DSI
	A4MP	SPU2, FSI, FMSI, BBIF2

13.7.3 Power Control Flow

The power control flow of this LSI is shown in the following flow chart.

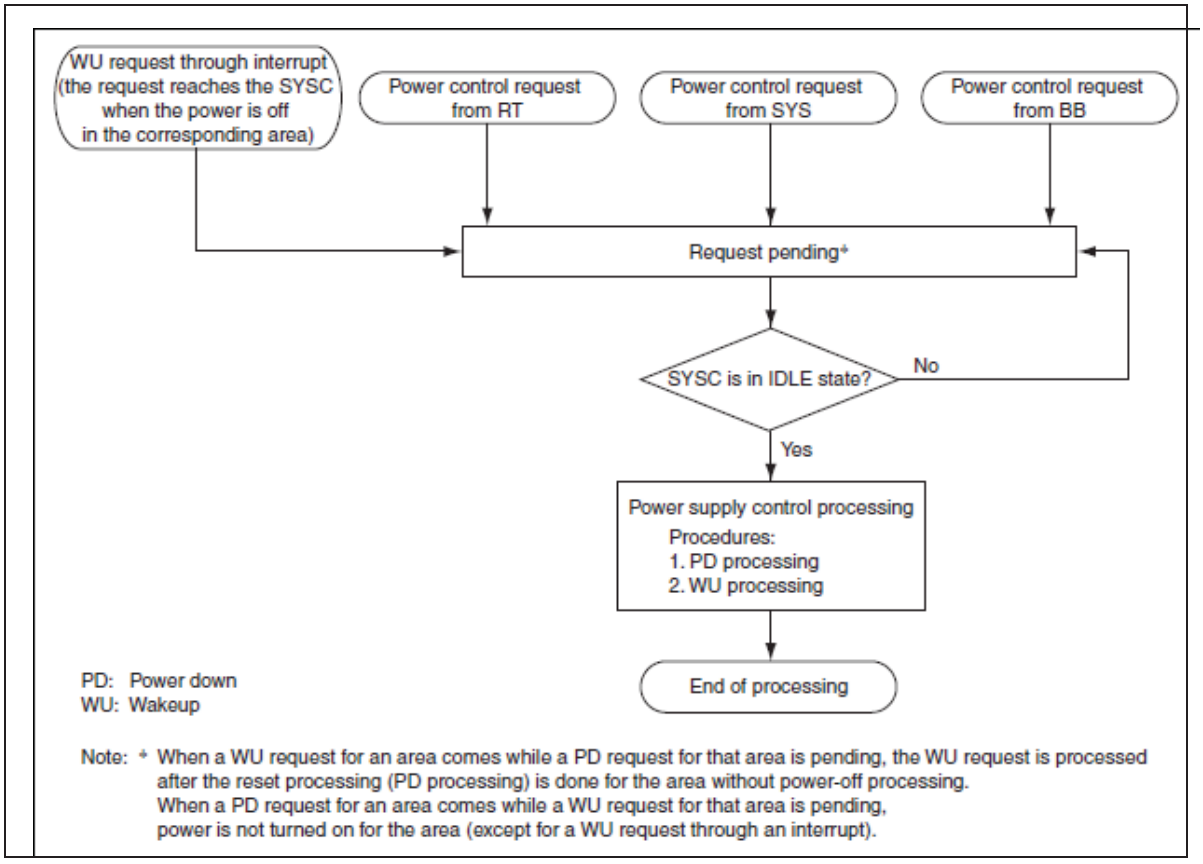


Fig 13.3 Power Control Flow chart

13.8 Reset Specifications

13.8.1 Reset Layer Structure

SYSC controls the following three types of resets.

(1) Power On Reset

Power On Reset initializes all modules of LSI. The following are the sources of this reset.

1. RESETP_N = 0 (Hard Power On Reset)
2. RESCNT2. PRES = 1
3. RESCNT2.MRES= 1 & RESCNT.SRESLNK=1
4. RESETA_N = 0 & RESCNT.SRESLNK=1
5. RWDT0 over flow & RESCNT2. RWD0A=11

All resources of the LSI including Test, Debug are initialized with this reset. Since TAP controller of the JTAG is only initialized by TRST, TRST is also asserted during Power On Reset.

When a Power On Reset is asserted the SYSC wakeup areas whose power was turned off, keeps asserting the internal Power On Reset signal for certain period necessary to initialize the internal resources and then releases it when the process is completed.

(2) System Reset

System Rest initializes all modules other than C5, and D4. Few modules residing in C5, D4 also gets initialized.

The following are the sources for this reset.

1. RESETA_N = 0 & RESCNT.SRESLNK=0
2. RESCNT2.MRES= 1 & RESCNT.SRESLNK=0
3. RWDT0 over flow & RESCNT2. RWD0A=10

When a Power On Reset is asserted the SYSC wakeup areas whose power was turned off, keeps asserting the internal Power On Reset signal for certain period necessary to initialize the internal resources and then releases it when the process is completed.

(3) Power Area Reset

Each of 11 power areas consists of area reset.

This reset is asserted during Power down/wakeup process. Modules other than backup modules are initialized by this reset before the power is turned OFF. Also during wakeup process the modules other than backup modules turned ON in initialization state. There exist some cases where area reset is asserted even though power down process is cancelled.

Area reset is asserted → Power down → Wakeup → Area reset release

Refer to CPGA module specification of more details on reset specifications..

(4) Reset Boundaries

The following figures shows reset boundaries.

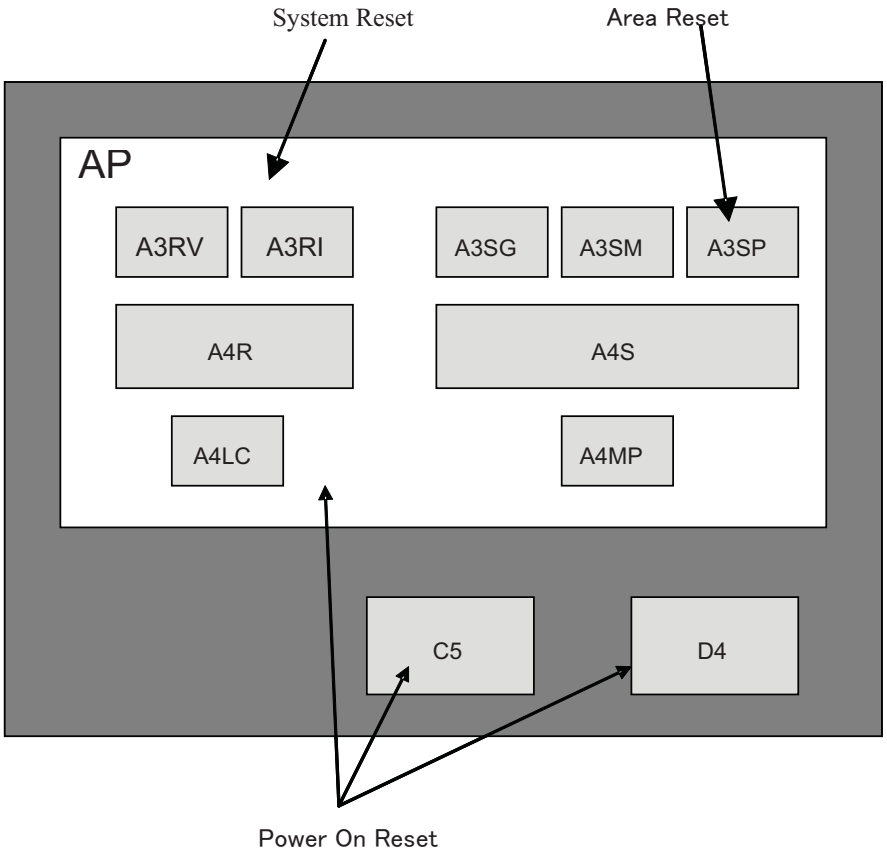


Fig13. 4 Reset Boundaries

Section 14 Timer Unit (TMU)

This LSI includes three-channel 32-bit timer unit (TMU) of two sets.

14.1 Features

- Three channels are provided in the real-time domain
- Each channel is provided with an auto-reload 32-bit down counter
- All channels are provided with 32-bit constant registers and 32-bit down counters that can be read or written to at any time
- All channels generate interrupt requests when the 32-bit down counter underflows (H'00000000 → H'FFFFFFFF)
- Allows selection among five counter input clocks: SUBϕ/4, SUBϕ/16, SUBϕ/64, SUBϕ/256, and SUBϕ/1024

Figure 14.1 shows a block diagram of the TMU.

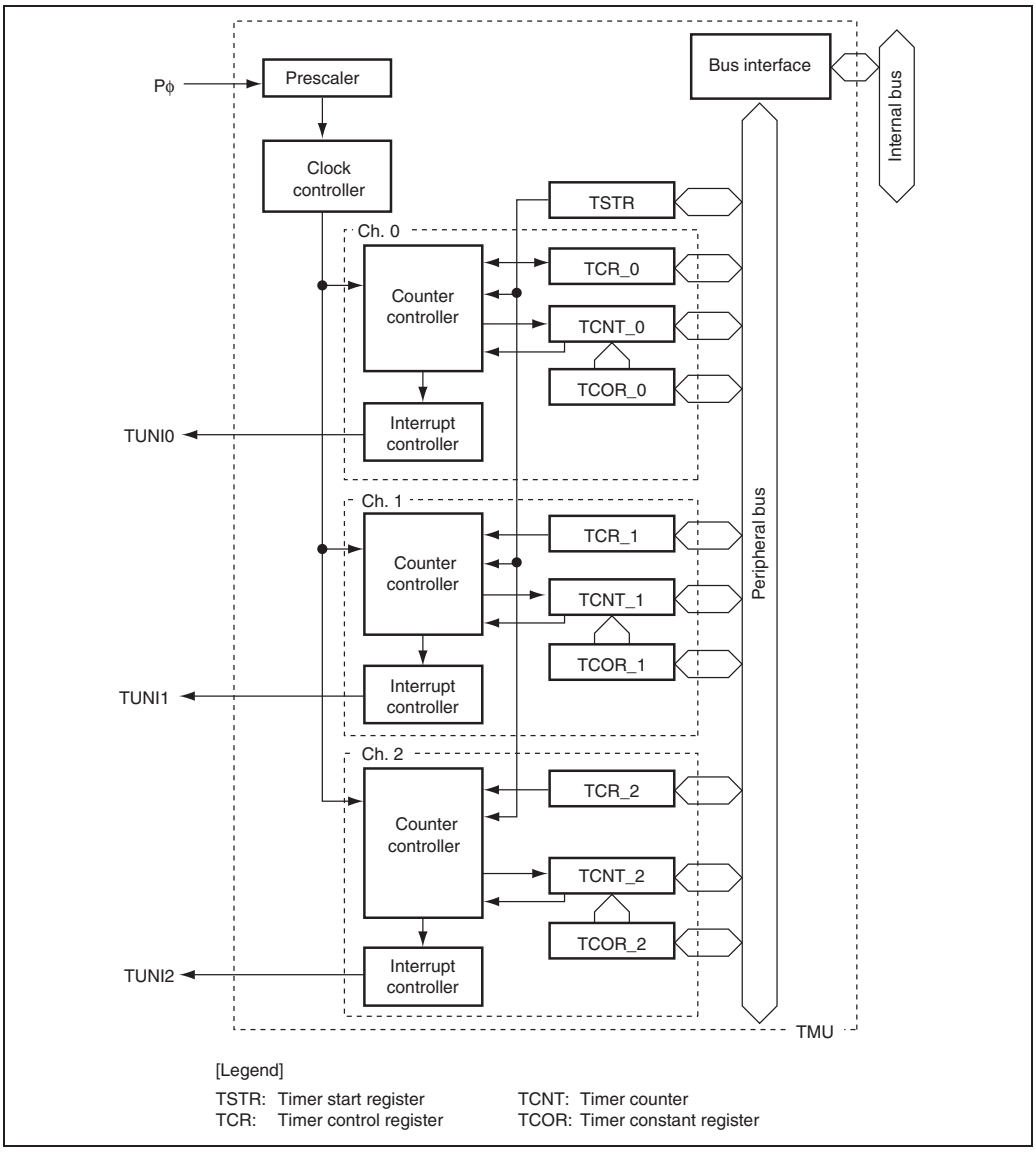


Figure 14.1 Block Diagram of TMU

14.2 Register Descriptions

Table 14.1 shows the TMU register configuration. Table 14.2 shows the register states in each operating mode. In the following descriptions, TCOR for channel 0 is noted as TCOR_0.

Table 14.1 Register Configuration

Register	Abbreviation	R/W	Address	Access Size
Timer start register 0	TSTR 0	R/W	H'FFF6 0004	8
Timer constant register0_0	TCOR0_0	R/W	H'FFF6 0008	32
Timer counter0_0	TCNT0_0	R/W	H'FFF6 000C	32
Timer control register0_0	TCR0_0	R/W	H'FFF6 0010	16
Timer constant register0_1	TCOR0_1	R/W	H'FFF6 0014	32
Timer counter0_1	TCNT0_1	R/W	H'FFF6 0018	32
Timer control register0_1	TCR0_1	R/W	H'FFF6 001C	16
Timer constant register0_2	TCOR0_2	R/W	H'FFF6 0020	32
Timer counter0_2	TCNT0_2	R/W	H'FFF6 0024	32
Timer control register0_2	TCR0_2	R/W	H'FFF6 0028	16
Timer start register 1	TSTR 1	R/W	H'FFF7 0004	8
Timer constant register1_0	TCOR1_0	R/W	H'FFF7 0008	32
Timer counter1_0	TCNT1_0	R/W	H'FFF7 000C	32
Timer control register1_0	TCR1_0	R/W	H'FFF7 0010	16
Timer constant register1_1	TCOR1_1	R/W	H'FFF7 0014	32
Timer counter1_1	TCNT1_1	R/W	H'FFF7 0018	32
Timer control register1_1	TCR1_1	R/W	H'FFF7 001C	16
Timer constant register1_2	TCOR1_2	R/W	H'FFF7 0020	32
Timer counter1_2	TCNT1_2	R/W	H'FFF7 0024	32
Timer control register1_2	TCR1_2	R/W	H'FFF7 0028	16

Table 13.2 Register States in Each Operating Mode

Register Abbreviation	Power-On Reset	Software Standby	Module Standby	Sleep
TSTR 0	Initialized	Retained	Retained	Retained
TCOR0_0	Initialized	Retained	Retained	Retained
TCNT0_0	Initialized	Retained	Retained	Retained
TCR0_0	Initialized	Retained	Retained	Retained
TCOR0_1	Initialized	Retained	Retained	Retained
TCNT0_1	Initialized	Retained	Retained	Retained
TCR0_1	Initialized	Retained	Retained	Retained
TCOR0_2	Initialized	Retained	Retained	Retained
TCNT0_2	Initialized	Retained	Retained	Retained
TCR0_2	Initialized	Retained	Retained	Retained
TSTR 1	Initialized	Retained	Retained	Retained
TCOR1_0	Initialized	Retained	Retained	Retained
TCNT1_0	Initialized	Retained	Retained	Retained
TCR1_0	Initialized	Retained	Retained	Retained
TCOR1_1	Initialized	Retained	Retained	Retained
TCNT1_1	Initialized	Retained	Retained	Retained
TCR1_1	Initialized	Retained	Retained	Retained
TCOR1_2	Initialized	Retained	Retained	Retained
TCNT1_2	Initialized	Retained	Retained	Retained
TCR1_2	Initialized	Retained	Retained	Retained

14.2.1 Timer Start Register (TSTR)

TSTR is an 8-bit readable/writable register that selects whether to operate or halt the timer counters (TCNT).

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	STR2	STR1	STR0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	STR2	0	R/W	Counter Start 2 Selects whether to operate or halt timer counter 2 (TCNT_2). 0: TCNT_2 count halted 1: TCNT_2 counts
1	STR1	0	R/W	Counter Start 1 Selects whether to operate or halt timer counter 1 (TCNT_1). 0: TCNT_1 count halted 1: TCNT_1 counts
0	STR0	0	R/W	Counter Start 0 Selects whether to operate or halt timer counter 0 (TCNT_0). 0: TCNT_0 count halted 1: TCNT_0 counts

14.2.2 Timer Control Registers (TCR)

TCR is a 16-bit readable/writable register that controls the timer counters (TCNT) and interrupts.

TCR controls the issuance of interrupts when the flag indicating timer counter (TCNT) underflow has been set to 1, and also carries out counter clock selection.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	UNF	—	—	UNIE	—	—	TPSC[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/(W)*	R	R	R/W	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	UNF	0	R/(W)*	Underflow Flag Status flag that indicates occurrence of a TCNT underflow. 0: TCNT has not underflowed [Clearing condition] 0 is written to UNF 1: TCNT has underflowed [Setting condition] TCNT underflows
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	UNIE	0	R/W	Underflow Interrupt Control Controls enabling of interrupt generation when the status flag (UNF) indicating TCNT underflow has been set to 1. 0: Interrupt due to UNF (TUNI) is disabled 1: Interrupt due to UNF (TUNI) is enabled
4, 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
2 to 0	TPSC[2:0]	000	R/W	Timer Prescaler 2, 1, and 0 Select the TCNT count clock. 000: Count on SUBϕ/4 001: Count on SUBϕ/16 010: Count on SUBϕ/64 011: Count on SUBϕ/256 100: Count on SUBϕ/1024 Others: Setting prohibited

Note: * Only 0 can be written to clear the flag.

14.2.3 Timer Constant Registers (TCOR)

TCOR is a 32-bit readable/writable register that specifies the value to be set in TCNT when TCNT underflows.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TCOR															
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TCOR															
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

14.2.4 Timer Counters (TCNT)

TCNT counts down upon input of a clock. The clock input is selected using bits TPSC[1:0] in TCR.

When a TCNT countdown results in an underflow (H'00000000 → H'FFFFFFFF), the underflow flag (UNF) in TCR that is corresponding to the channel is set. The TCOR value is simultaneously set in TCNT itself and the countdown continues from that value.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TCNT															
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TCNT															
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

14.3 Operation

Each channel has a 32-bit TCNT and a 32-bit TCOR. TCNT counts down. The auto-reload function enables cyclic counting.

14.3.1 Counter Operation

When bits STR2 to STR0 in TSTR are set to 1, the corresponding TCNT starts counting. When TCNT underflows, the UNF flag in the corresponding TCR is set. At this moment, if the UNIE bit in TCR is 1, an interrupt request is sent to the CPU. Also, the value in TCOR is copied to TCNT and the count down operation continues.

(1) Count Operation Setting Procedure

An example procedure for setting the count operation is shown in figure 14.2.

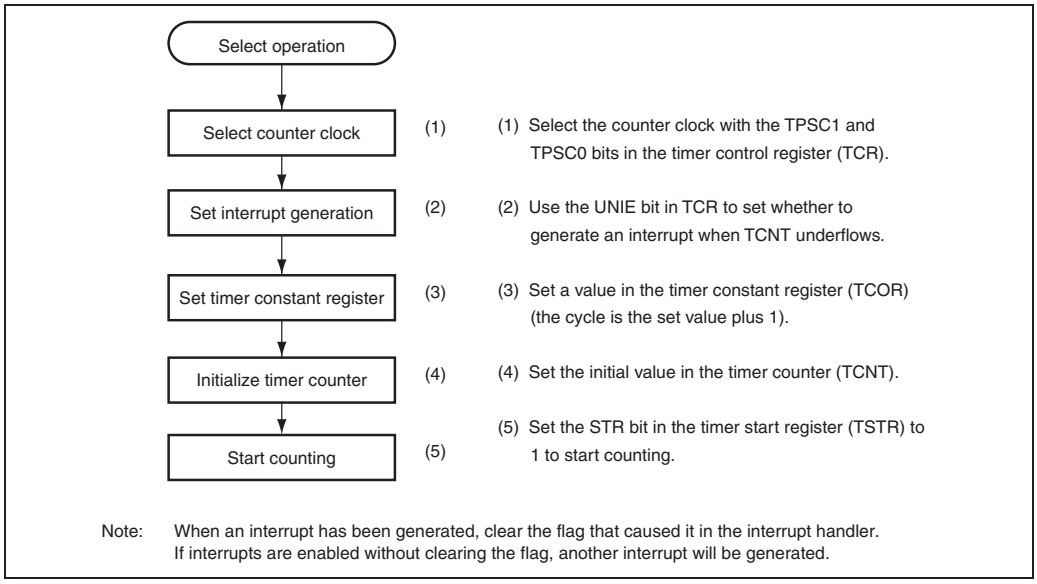


Figure 14.2 Setting Count Operation

(2) Auto-Reload Count Operation

Figure 14.3 shows the TCNT auto-reload operation.

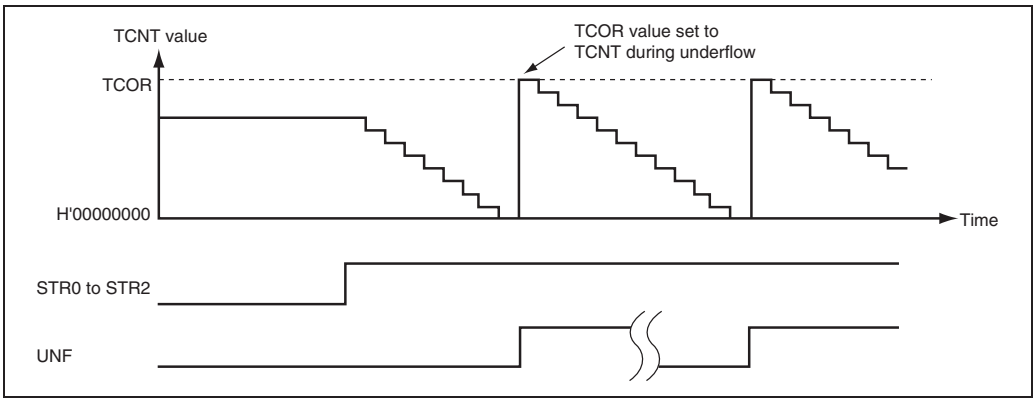


Figure 14.3 Auto-Reload Count Operation

(3) TCNT Count Timing

Setting bits TPSC1 and TPSC0 in TCR allows to select one of the five internal clocks (SUBϕ/4, SUBϕ/16, SUBϕ/64, SUBϕ/256, and SUBϕ/1024) that are generated by dividing the peripheral module clock. Figure 14.4 shows the timing.

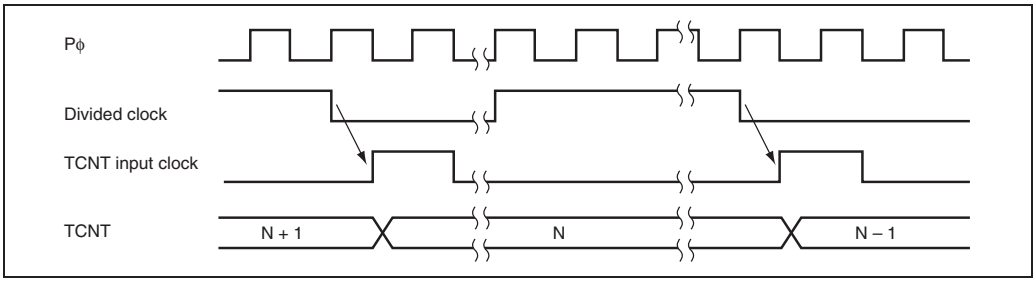


Figure 14.4 Count Timing when Internal Clock is Operating

14.4 Interrupts

There is one source of TMU interrupts: underflow interrupts (TUNI).

14.4.1 Status Flag Set Timing

The UNF bit is set to 1 when TCNT underflows. Figure 14.5 shows the timing.

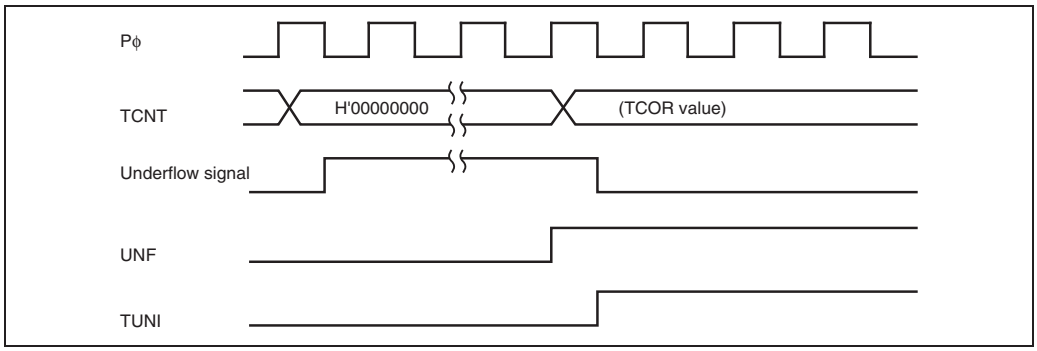


Figure 14.5 UNF Set Timing

14.4.2 Status Flag Clear Timing

The status flag can be cleared by writing 0 from the CPU. Figure 14.6 shows the timing.

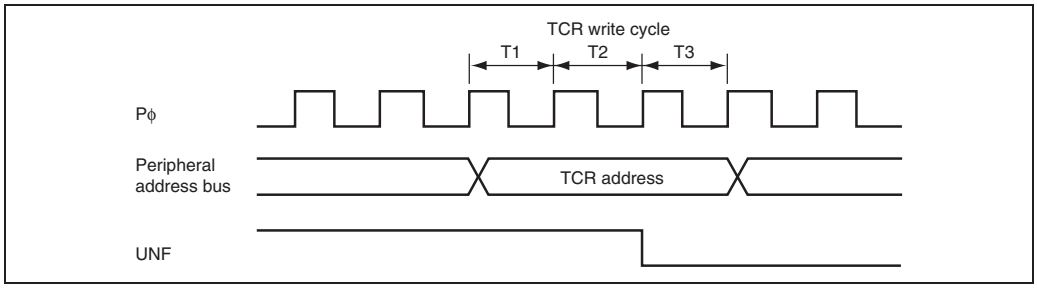


Figure 14.6 Status Flag Clear Timing

14.4.3 Interrupt Sources and Priorities

The TMU generates underflow interrupts for each channel. When the interrupt request flag and interrupt enable bit are both set to 1, the interrupt is requested. A specific code is set in the interrupt event register (INTEVT) for this interrupt and interrupt processing must be executed according to the code.

The priorities between channels are changeable by the interrupt controller. Table 14.3 lists TMU interrupt sources.

Table 14.3 TMU Interrupt Sources

Channel	Interrupt Source	Description	Priority
0	TUNI0	Underflow interrupt 0	High
1	TUNI1	Underflow interrupt 1	↕
2	TUNI2	Underflow interrupt 2	Low

14.5 Usage Notes

14.5.1 Writing to Registers

Synchronization processing is not performed for timer counting during register writes. When writing to registers, be sure to clear the start bits (STR2 to STR0) of the channel in TSTR and halt the timer counting.

14.5.2 Reading Registers

Synchronization processing is performed for timer counting during register reads. When the timer counting and register read are performed simultaneously, the register value stored before the TCNT countdown is read through the synchronization processing.

Section 15 16-Bit Timer Pulse Unit (TPU)

This LSI has a five on-chip 16-bit timer pulse units (TPU), which consists of four 16-bit timer channels.

15.1 Features

TPU 0 have the following features.

- 4-channel timers are mounted in the system domain.
- Up to four pulses output is possible.
  TPU 0 has a total of 16 timer general registers provided with four registers (TPU0_TGRA, TPU0_TGRB, TPU0_TGRC, TPU0_TGRD) for each channel. TPU0_TGRA enables an output compare setting. TPU0_TGRB, TPU0_TGRC, and TPU0_TGRD in each channel can be used as the timer counter clear registers. TPU0_TGRC and TPU0_TGRD can be used as the buffer registers.
- The following operation can be set for each channel:
  Waveform output by compare match: 0 output, 1 output, toggle output selection is possible.
  Counter clear operation: counter clearing possible by compare match
  PMW mode: PMW output of any duty cycle is possible.
  Up to four phases of PMW output is possible.
- Setting stepping motor control mode using channel 0 is possible.
- Buffer operation settable for each channel
  Automatic rewriting of output compare register possible
- One interrupt request from TPU 0
  Enabling or disabling the compare match/overflow interrupt request can be set independently for each interrupt source.
  In stepping motor control mode, setting of transition, data request, permission, and prohibition of data overflow interruption is possible by channel 0.

Table 15.1 describes the TPU functions.

Table 15.1 TPU Functions

Item		TPU0: Channel 0	TPU0: Channel 1	TPU0: Channel 2	TPU0: Channel 3
Count clock		CPϕ/1 CPϕ/4 CPϕ/16 CPϕ/64	CPϕ/1 CPϕ/4 CPϕ/16 CPϕ/64	CPϕ/1 CPϕ/4 CPϕ/16 CPϕ/64	CPϕ/1 CPϕ/4 CPϕ/16 CPϕ/64
General register		TPU0_TGR0A TPU0_TGR0B	TPU0_TGR1A TPU0_TGR1B	TPU0_TGR2A TPU0_TGR2B	TPU0_TGR3A TPU0_TGR3B
General register/ Buffer register		TPU0_TGR0C TPU0_TGR0D	TPU0_TGR1C TPU0_TGR1D	TPU0_TGR2C TPU0_TGR2D	TPU0_TGR3C TPU0_TGR3D
Output pin	Normal Operation	TPU0: TPU0TO0	TPU0: TPU0TO1	TPU0: TPU0TO2	TPU0: TPU0TO3
Output pin	Stepping motor control mode	TPU0: TPU0TO0 to TPU0TO3	None	None	None
Counter clear function		TPU0_TGR compare match	TPU0_TGR compare match	TPU0_TGR compare match	TPU0_TGR compare match
Compare match output	0 output	Applicable	Applicable	Applicable	Applicable
	1 output	Applicable	Applicable	Applicable	Applicable
	Toggle output	Applicable	Applicable	Applicable	Applicable
PWM mode		Applicable	Applicable	Applicable	Applicable

Item	TPU0: Channel 0	TPU0: Channel 1	TPU0: Channel 2	TPU0: Channel 3
Buffer operation	Applicable 5 sources Compare match/ Overflow 6 more sources added in stepping motor control mode. /Acceleration transition /Normal transition /Deceleration transition /Stop transition /Data request /Data overflow	Applicable	Applicable	Applicable

15.2 Block Diagram

A block diagram of the TPU is shown in figure 15.1.

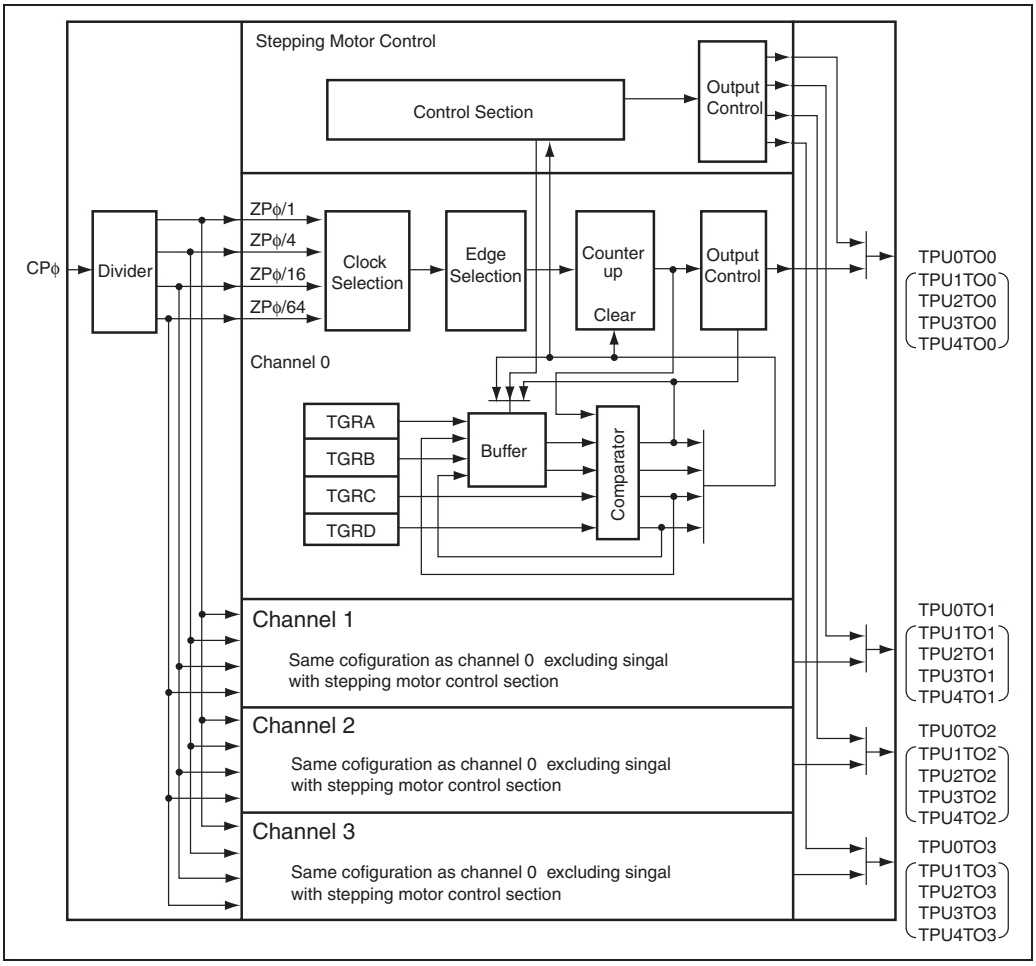


Figure 15.1 TPU Block Diagram

15.3 Input/Output Pin

Table 15.2 shows the pin configuration of the TPU 0.

Table 15.2 Pin Configuration

TPU 0 to 4	Channel	Pin Name	Function	I/O	Description
TPU0	0	TPU0TO0	TPU0 output compare match 0	Output	TPU0_TGR0A output compare output/ PWM output pin/PWM output pin/Pattern output 0 in stepping motor control mode
	1	TPU0TO1	TPU0 output compare match 1	Output	TPU0_TGR1A output compare output/ PWM output pin/PWM output pin/Pattern output 1 in stepping motor control mode
	2	TPU0TO2	TPU0 output compare match 2	Output	TPU0_TGR2A output compare output/ PWM output pin/PWM output pin/Pattern output 2 in stepping motor control mode
	3	TPU0TO3	TPU0 output compare match 3	Output	TPU0_TGR3A output compare output/ PWM output pin/PWM output pin/Pattern output 3 in stepping motor control mode

15.4 Register Descriptions

Table 15.3 shows the TPU0 register configuration. Table 15.4 shows the register states.

Table 15.3 Register Configuration

Register Name	Abbreviation	R/W	Address	Access Size
Timer start register	TPU0_TSTR	R/W	H'E660 0000 H'E760 0000	16
Timer control register 0	TPU0_TCR0	R/W	H'E660 0010 H'E760 0010	16
Timer mode register 0	TPU0_TMDR0	R/W	H'E660 0014 H'E760 0014	16
Timer I/O control register 0	TPU0_TIOR0	R/W	H'E660 0018 H'E760 0018	16
Timer interrupt enable register 0	TPU0_TIER0	R/W	H'E660 001C H'E760 001C	16
Timer status register 0	TPU0_TSR0	R/W	H'E660 0020 H'E760 0020	16
Timer counter 0	TPU0_TCNT0	R/W	H'E660 0024 H'E760 0024	16
Timer general register 0A	TPU0_TGR0A	R/W	H'E660 0028 H'E760 0028	16
Timer general register 0B	TPU0_TGR0B	R/W	H'E660 002C H'E760 002C	16
Timer general register 0C	TPU0_TGR0C	R/W	H'E660 0030 H'E760 0030	16
Timer general register 0D	TPU0_TGR0D	R/W	H'E660 0034 H'E760 0034	16
Timer control register 1	TPU0_TCR1	R/W	H'E660 0050 H'E760 0050	16
Timer mode register 1	TPU0_TMDR1	R/W	H'E660 0054 H'E760 0054	16
Timer I/O control register 1	TPU0_TIOR1	R/W	H'E660 0058 H'E760 0058	16

Register Name	Abbreviation	R/W	Address	Access Size

Timer interrupt enable register 1	TPU0_TIER1	R/W	H'E660 005C H'E760 005C	16
Timer status register 1	TPU0_TSR1	R/W	H'E660 0060 H'E760 0060	16
Timer counter 1	TPU0_TCNT1	R/W	H'E660 0064 H'E760 0064	16
Timer general register 1A	TPU0_TGR1A	R/W	H'E660 0068 H'E760 0068	16
Timer general register 1B	TPU0_TGR1B	R/W	H'E660 006C H'E760 006C	16
Timer general register 1C	TPU0_TGR1C	R/W	H'E660 0070 H'E760 0070	16
Timer general register 1D	TPU0_TGR1D	R/W	H'E660 0074 H'E760 0074	16
Timer control register 2	TPU0_TCR2	R/W	H'E660 0090 H'E760 0090	16
Timer mode register 2	TPU0_TMDR2	R/W	H'E660 0094 H'E760 0094	16
Timer I/O control register 2	TPU0_TIOR2	R/W	H'E660 0098 H'E760 0098	16
Timer interrupt enable register 2	TPU0_TIER2	R/W	H'E660 009C H'E760 009C	16
Timer status register 2	TPU0_TSR2	R/W	H'E660 00A0 H'E760 00A0	16
Timer counter 2	TPU0_TCNT2	R/W	H'E660 00A4 H'E760 00A4	16
Timer general register 2A	TPU0_TGR2A	R/W	H'E660 00A8 H'E760 00A8	16
Timer general register 2B	TPU0_TGR2B	R/W	H'E660 00AC H'E760 00AC	16
Timer general register 2C	TPU0_TGR2C	R/W	H'E660 00B0 H'E760 00B0	16
Timer general register 2D	TPU0_TGR2D	R/W	H'E660 00B4 H'E760 00B4	16

Register Name	Abbreviation	R/W	Address	Access Size
Timer control register 3	TPU0_TCR3	R/W	H'E660 00D0 H'E760 00D0	16
Timer mode register 3	TPU0_TMDR3	R/W	H'E660 00D4 H'E760 00D4	16
Timer I/O control register 3	TPU0_TIOR3	R/W	H'E660 00D8 H'E760 00D8	16
Timer interrupt enable register 3	TPU0_TIER3	R/W	H'E660 00DC H'E760 00DC	16
Timer status register 3	TPU0_TSR3	R/W	H'E660 00E0 H'E760 00E0	16
Timer counter 3	TPU0_TCNT3	R/W	H'E660 00E4 H'E760 00E4	16
Timer general register 3A	TPU0_TGR3A	R/W	H'E660 00E8 H'E760 00E8	16
Timer general register 3B	TPU0_TGR3B	R/W	H'E660 00EC H'E760 00EC	16
Timer general register 3C	TPU0_TGR3C	R/W	H'E660 00F0 H'E760 00F0	16
Timer general register 3D	TPU0_TGR3D	R/W	H'E660 00F4 H'E760 00F4	16
Motor control configuration register*	TPU0_TMIR	R/W	H'E660 0100 H'E760 0100	16
Motor deceleration (stop) transition configuration register*	TPU0_TMRR	R/W	H'E660 0104 H'E760 0104	16
Motor control status register*	TPU0_TMSR	R	H'E660 0108 H'E760 0108	16
Motor operation pattern storage register 0*	TPU0_TMMPR0	R/W	H'E660 0110 H'E760 0110	16
Motor operation pattern storage register 1*	TPU0_TMMPR1	R/W	H'E660 0114 H'E760 0114	16
Motor stop pattern storage register 0*	TPU0_TMSPR0	R/W	H'E660 0118 H'E760 0118	16
Motor stop pattern storage register 1*	TPU0_TMSPR1	R/W	H'E660 011C H'E760 011C	16

Register Name	Abbreviation	R/W	Address	Access Size
Motor output pattern storage register*	TPU0_TMOPR	R/W	H'E660 0120 H'E760 0120	16
Motor acceleration the number of steps register*	TPU0_TMASR	R/W	H'E660 0130 H'E760 0130	16
Motor normal the number of steps register*	TPU0_TMTSR	R/W	H'E660 0134 H'E760 0134	16
Motor deceleration the number of steps register*	TPU0_TMRSR	R/W	H'E660 0138 H'E760 0138	16
Motor control sequence counter register*	TPU0_TMSCR	R/W	H'E660 0140 H'E760 0140	16
Motor control normal counter register*	TPU0_TMTCR	R	H'E660 0144 H'E760 0144	16

Note: * Use only when stepping motor control is performed.

Table 15.4 Register States in Each Operating Mode

Register Abbreviation	Reset *	Module Standby
TPU0_TSTR	Initialized	Retained
TPU0_TCR0 to TPU0_TCR3	Initialized	Retained
TPU0_TMDR0 to TPU0_TMDR3	Initialized	Retained
TPU0_TIOR0 to TPU0_TIOR3	Initialized	Retained
TPU0_TIER0 to TPU0_TIER3	Initialized	Retained
TPU0_TSR0 to TPU0_TSR3	Initialized	Retained
TPU0_TCNT0 to TPU0_TCNT3	Initialized	Retained
TPU0_TGRnA (n=0 to 3)	Initialized	Retained
TPU0_TGRnB (n=0 to 3)	Initialized	Retained
TPU0_TGRnC (n=0 to 3)	Initialized	Retained
TPU0_TGRnD (n=0 to 3)	Initialized	Retained
TPU0_TMIR	Initialized	Retained
TPU0_TMRR	Initialized	Retained
TPU0_TMSR	Initialized	Retained
TPU0_TMMPRO0, TPU0_TMMPRO1	Initialized	Retained
TPU0_TMOPR0, TPU0_TMOPR1	Initialized	Retained
TPU0_TMASR	Initialized	Retained
TPU0_TMTSR	Initialized	Retained
TPU0_TMRSR	Initialized	Retained
TPU0_TMSCR	Initialized	Retained
TPU0_TMTCR	Initialized	Retained

Note: * For details, refer to section 1-D Overview of reset.

15.4.1 Timer Control Register (TPU0_TCR)

TPU0_TCR controls the TPU0_TCNT for each channel. The TPU has one TPU0_TCR register for each channel. TPU0_TCR is initialized to H'0000 at a reset.

TPU0_TCR register settings should be made only while TPU0_TCNT operation is stopped.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	CCLR[2:0]			CKEG[1:0]		TPSC[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 8	—	All 0	R	Reserved These bits are always read as 0 and cannot be modified.

Bit	Bit Name	Initial Value	R/W	Description
7 to 5	CCLR[2:0]	000	R/W	Counter Clear Select the TPU0_TCNT clearing source. 000: TPU0_TCNT clearing disabled 001: TPU0_TCNT cleared by TPU0_TGRA compare match 010: TPU0_TCNT cleared by TPU0_TGRB compare match 011: Setting prohibited 100: TPU0_TCNT clearing disabled 101: TPU0_TCNT cleared by TPU0_TGRC compare match 110: TPU0_TCNT cleared by TPU0_TGRD compare match 111: Setting prohibited
4, 3	CKEG[1:0]	00	R/W	Clock Edge Select the input clock edge. When the internal clock is counted using both edges, the input clock period is halved (e.g., both edges of CPϕ/4 = rising edge of CPϕ/2). When the phase coefficient mode is set, this setting is ignored. 00: Count at rising edge 01: Count at falling edge* 1X: Count at both edges* [Legend] X: Don't care Note: * If the input clock is CPϕ/1, no operation is performed.
2 to 0	TPSC[2:0]	000	R/W	Timer Prescaler Select the TPU0_TCNT count clock. The clock source can be selected independently for each channel. Table 15.5 shows the clock sources that can be set for each channel. For more information on count clock selection, see table 15.6.

Table 15.5 TPU Clock Sources

	Internal Clock			
Channel	**CPϕ/1**	**CPϕ/4**	**CPϕ/16**	**CPϕ/64**
0	O	O	O	O
1	O	O	O	O
2	O	O	O	O
3	O	O	O	O

[Legend]
O: Setting

Table 15.6 Count Clock Selection by the TPSC[2:0] Bits

Channel	TPSC[2]	TPSC[1]	TPSC[0]	Description
0 to 3	0	0	0	Internal clock: counts on CPϕ/1(initial value)
			1	Internal clock: counts on CPϕ/4
		1	0	Internal clock: counts on CPϕ/16
			1	Internal clock: counts on CPϕ/64
	1	*	*	Setting prohibited

[Legend]
*: Don't care.

15.4.2 Timer Mode Register (TPU0_TMDR)

TPU0_TMDR specifies the operation mode for each channel. The TPU has one TPU0_TMDR register for each channel. TPU0_TMDR is initialized to H'0000 at a reset.

TPU0_TMDR register settings should be made only while TPU0_TCNT operation is stopped.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	BFWT	BFB	BFA	—	MD[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 7	—	All 0	R	Reserved These bits are always read as 0 and cannot be modified.
6	BFWT	0	R/W	Buffer Write Timing Specifies TPU0_TGRA and TPU0_TGRB update timing when TPU0_TGRC and TPU0_TGRD are used as a compare match buffer. When TPU0_TGRC and TPU0_TGRD are not used as a compare match buffer register, this bit does not function. 0: TPU0_TGRA and TPU0_TGRB are rewritten at compare match of each register. 1: TPU0_TGRA and TPU0_TGRB are rewritten at counter clearing.
5	BFB	0	R/W	Buffer Operation B Specifies whether TPU0_TGRB is used in normal operation, or TPU0_TGRB and TPU0_TGRD are used in combination for buffer operation. 0: TPU0_TGRB normal operation 1: TPU0_TGRB and TPU0_TGRD used for buffer operation
4	BFA	0	R/W	Buffer Operation A Specifies whether TPU0_TGRA is used in normal operation, or TPU0_TGRA and TPU0_TGRC are used in combination for buffer operation. 0: TPU0_TGRA normal operation 1: TPU0_TGRA and TPU0_TGRC used for buffer operation

Bit	Bit Name	Initial Value	R/W	Description
3	—	0	R	Reserved This bit is always read as 0 and cannot be modified.
2 to 0	MD[2:0]	000	R/W	Timer Operating Mode Set the timer-operating mode. 000: Normal operating 001: Setting prohibited 010: PWM mode 011: Setting prohibited 100: Setting prohibited 101: Setting prohibited 110: Setting prohibited 111: Setting prohibited

15.4.3 Timer I/O Control Register (TPU0_TIOR)

TPU0_TIOR controls the TPU0TO0 to 3 pin, and this LSI provides channel 0 only. TPU0_TIOR is initialized to H'0000 at a reset.

TPU0_TIOR register setting should be made only while TPU0_TCNT operation is stopped. Note that the setting of TPU0_TMDR may affect TPU0_TIOR.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	IOA[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 3	—	All 0	R	Reserved These bits are always read as 0 and cannot be modified.
2 to 0	IOA[2:0]	000	R/W	I/O Control Bits IOA2 to IOA0 specify the functions of TPU0_TGRA and the TPU0TO0 to 3 pin. For details, see table 15.7.

Table 15.7 Settings for Bits IOA[2:0], Initial States of Pin TPUTO0 to 3, and Results of Matching with TPU0_TGRA

Channel	IOA[2]	IOA[1]	IOA[0]	Description	
0 to 3	0	0	0	Always output 0 (initial value)	
			1	Initial output of the TPU0TO0 to 3 pin is 0	Output 0 on compare match with TPU0_TGRA*
		1	0		Output 1 on compare match with TPU0_TGRA
			1		Toggle output on compare match with TPU0_TGRA*
	1	0	0	Always output 1	
			1	Initial output of the TPU0TO0 to 3 pin is 1	Output 0 on compare match with TPU0_TGRA*
		1	0		Output 1 on compare match with TPU0_TGRA
			1		Toggle output on compare match with TPU0_TGRA*

Note: * Do not use this setting in PWM mode.

15.4.4 Timer Interrupt Enable Register (TPU0_TIER)

TPU0_TIER is used to enable and disable interrupt requests for each channel. The TPU has one TPU0_TIER register for each channel. TPU0_TIER is initialized to H'0000 by a reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	TMDOFE	TMDRFE	TMS1ER	TMS1ET	TMS1EA	TMS1ES	—	—	—	TC1EV	TG1ED	TG1EC	TG1EB	TG1EA
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15, 14	—	All 0	R	Reserved These bits are always read as 0 and cannot be modified.

Bit	Bit Name	Initial Value	R/W	Description
13	TMDOFE	0	R/W	Motor Control Data Transfer Data Overflow Detection Enable When the TMDOS flag in TPU0_TSR is set to 1 (data transfer overflow) in stepping motor control mode of channel 0, this bit enables or disables interrupt requests corresponding to the state of the TMDOFS flag. This bit is reserve bit in channel 1 to 3. This bit is always read as 0 and cannot be modified. 0: Interrupt requests by TMDOFS flag disabled 1: Interrupt requests by TMDOFS flag enabled
12	TMDRFE	0	R/W	Motor Control Data Transfer Request Detection Enable When the TMDRFS flag in TPU0_TSR is set to 1 (data transfer request) in stepping motor control mode of channel 0, this bit enables or disables interrupt requests corresponding to the state of the TMDRFS flag. This bit is reserve bit in channel 1 to 3. This bit is always read as 0 and cannot be modified. 0: Interrupt requests by TMDRFS flag disabled 1: Interrupt requests by TMDRFS flag enabled
11	TMS1ER	0	R/W	Motor Control Deceleration Transition Detection Enable When the TMCFR flag in TPU0_TSR is set to 1 (deceleration transition detection) in stepping motor control mode of channel 0, this bit enables or disables interrupt requests corresponding to the state of the TMCFR flag. This bit is reserve bit in channel 1 to 3. This bit is always read as 0 and cannot be modified. 0: Interrupt requests by TMCFR flag disabled 1: Interrupt requests by TMCFR flag enabled

Bit	Bit Name	Initial Value	R/W	Description
10	TMS1ET	0	R/W	Motor Control Normal Transition Detection Enable When the TMCFT flag in TPU0_TSR is set to 1 (acceleration normal transition detect) in stepping motor control mode of channel 0, this bit enables or disables interrupt requests corresponding to the state of the TMCFT flag. This bit is reserve bit in channel 1 to 3. This bit is always read as 0 and cannot be modified. 0: Interrupt requests by TMCFT flag disabled 1: Interrupt requests by TMCFT flag enabled
9	TMS1EA	0	R/W	Motor Control Acceleration Transition Detection Enable When the TMCFA flag in TPU0_TSR is set to 1 (acceleration normal transition detection) in stepping motor control mode of channel 0, this bit enables or disables interrupt requests corresponding to the state of the TMCFA flag. This bit is reserve bit in channel 1 to 3. This bit is always read as 0 and cannot be modified. 0: Interrupt requests by TMCFA flag disabled 1: Interrupt requests by TMCFA flag enabled
8	TMS1ES	0	R/W	Motor Control Stop Transition Detection Enable When the TMCFS flag in TPU0_TSR is set to 1 (stop transition detection) in stepping motor control mode of channel 0, this bit enables or disables interrupt requests corresponding to the state of the TMCFS flag. This bit is reserve bit in channel 1 to 3. This bit is always read as 0 and cannot be modified. 0: Interrupt requests by TMCFS flag disabled 1: Interrupt requests by TMCFS flag enabled
7 to 5	—	All 0	R	Reserved These bits are always read as 0 and cannot be modified.

Bit	Bit Name	Initial Value	R/W	Description
4	TC1EV	0	R/W	Overflow Interrupt Enable When the TCFV flag in TPU0_TSR is set to 1 (TCNT overflow occur), this bit enables or disables interrupt requests corresponding to the state of the TCFV flag. 0: Interrupt requests by TCFV flag disabled 1: Interrupt requests by TCFV flag enabled
3	TG1ED	0	R/W	TPU0_TGR Interrupt Enable D. When the TGFD bit in TPU0_TSR is set to 1 (compare match occurs between TPU0_TCNT and TPU0_TGRD), this bit enables or disables interrupt requests corresponding to the state of the TGFD bit. 0: Interrupt requests by TGFD bit disabled 1: Interrupt requests by TGFD bit enabled
2	TG1EC	0	R/W	TPU0_TGR Interrupt Enable C When the TGFC bit in TPU0_TSR is set to 1 (compare match occurs between TPU0_TCNT and TPU0_TGRC), this bit enables or disables interrupt requests corresponding to the state of the TGFC bit. 0: Interrupt requests by TGFC bit disabled 1: Interrupt requests by TGFC bit enabled
1	TG1EB	0	R/W	TPU0_TGR Interrupt Enable B When the TGFB bit in TPU0_TSR is set to 1 (compare match occurs between TPU0_TCNT and TPU0_TGRB), this bit enables or disables interrupt requests corresponding to the state of the TGFB bit. 0: Interrupt requests by TGFB bit disabled 1: Interrupt requests by TGFB bit enabled
0	TG1EA	0	R/W	TPU0_TGR Interrupt Enable A When the TGFA bit in TPU0_TSR is set to 1 (compare match occurs between TPU0_TCNT and TPU0_TGRA), this bit enables or disables interrupt requests corresponding to the state of the TGFA bit. 0: Interrupt requests by TGFA bit disabled 1: Interrupt requests by TGFA bit enabled

15.4.5 Timer Status Registers (TPU0_TSR)

TPU0_TSR displays information on the state of each channel. The TPU has one TPU0_TSR register for each channel. TPU0_TSR is initialized to H'0000 by a reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	TMDOFS	TMDRFS	TMCFR	TMCFT	TMCFA	TMCFS	—	—	TCFU	TCFV	TGFD	TGFC	TGFB	TGFA
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R	R	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Bit	Bit Name	Initial Value	R/W	Description
15, 14	—	All 0	R	Reserved These bits are always read as 0 and cannot be modified.
13	TMDOFS	0	R/(W)*	Motor Control Data Transfer Overflow Detection Enable Detection flag of data transfer overflow in channel 0 stepping motor control mode. This bit is reserve bit in channels 1 to 3. This bit is always read as 0 and cannot be modified. [Clearing condition] Writing 0 to the TMDOFS bit after reading TMDOFS bit when TMDOFS = 1 [Setting condition] When DMA transfer overflow occurs.
12	TMDRFS	0	R/(W)*	Motor Control Data Transfer Request Detection Enable Detection flag of data transfer request in channel 0 stepping motor control mode. Writing data in TGR0D using this interrupt when DMA transfer is not used. This bit is reserve bit in channels 1 to 3. This bit is always read as 0 and cannot be modified. [Clearing condition] Writing 0 to the TMDRFS bit after reading TMDRFS bit when TMDRFS = 1 [Setting condition] When data transfer request occurs.

Bit	Bit Name	Initial Value	R/W	Description
11	TMCFR	0	R/(W)*	Motor Control Deceleration Transfer Detection Enable Detection flag when sequence state transfers deceleration state in channel 0 stepping motor control mode. This bit is reserve bit in channels 1 to 3. This bit is always read as 0 and cannot be modified. [Clearing condition] Writing 0 to the TMCFR bit after reading TMCFR bit = 1 [Setting condition] When sequence state transfers deceleration state.
10	TMCFT	0	R/(W)*	Motor Control Normal Transfer Detection Enable. Detection flag when sequence state transfers normal state in channel 0 stepping motor control mode. This bit is reserve bit in channels 1s to 3. This bit is always read as 0 and cannot be modified. [Clearing condition] Writing 0 to the TMCFT bit after reading TMCFT bit = 1 [Setting condition] When sequence state transfers normal state.
9	TMCFA	0	R/(W)*	Motor Control Acceleration Transition Detection Enable Detection flag when sequence state transfers acceleration state in channel 0 stepping motor control mode. This bit is reserve bit in channels 1 to 3. This bit is always read as 0 and cannot be modified. [Clearing condition] Writing 0 to the TMCFA bit after reading TMCFA bit = 1 [Setting condition] When sequence state transfers acceleration state.

Bit	Bit Name	Initial Value	R/W	Description
8	TMCFS	0	R/(W)*	Motor Control Stop Transition Detection Enable Detection flag when sequence state transfers stop state in channel 0 stepping motor control mode. This bit is reserve bit in channels 1 to 3. This bit is always read as 0 and cannot be modified. [Clearing condition] Writing 0 to the TMCFS bit after reading TMCFS bit = 1 [Setting condition] When sequence state transfers stop state.
7, 6	—	All 0	R	Reserved These bits are always read as 0 and cannot be modified.
5	TCFU	0	R/(W)*	Underflow Flag Status flag indicates TPU0_TCNT underflow in channel 2 and 3 phase figure mode. This bit is reserve bit in channels 0, 1. This bit is always read as 0 and cannot be modified. [Clearing condition] Writing 0 to the TCFU bit after reading TCFU bit = 1 [Setting condition] When the value of TPU0_TCNT underflow (H'0000→ H'FFFF)
4	TCFV	0	R/(W)*	Overflow Flag Status flag indicates TPU0_TCNT overflow occurs. [Clearing condition] Writing 0 to the TCFV bit after reading TCFV bit = 1 [Setting condition] When the value of TPU0_TCNT overflow (H'FFFF→ H'0000)

Bit	Bit Name	Initial Value	R/W	Description
3	TGFD	0	R/(W)*	Compare Flag D Status flag indicates TPU0_TCRD compare match occurs. [Clearing condition] Writing 0 to the TGFD bit after reading TGFD bit = 1 [Setting condition] When TPU0_TCNT = TPU0_TGRD
2	TGFC	0	R/(W)*	Compare Flag C Status flag indicates TPU0_TGRC compare match occurs. [Clearing condition] Writing 0 to the TGFC bit after reading TGFC bit = 1 [Setting condition] When TPU0_TCNT = TPU0_TGRC
1	TGFB	0	R/(W)*	Compare Flag B Status flag indicates TPU0_TGRB compare match occurs. [Clearing condition] Writing 0 to the TGFB bit after reading TGFB bit = 1 [Setting condition] When TPU0_TCNT = TPU0_TGRB
0	TGFA	0	R/(W)*	Output Compare Flag A Status flag indicates TPU0_TGRA compare match occurs. [Clearing condition] Writing 0 to the TGFA bit after reading TGFA bit = 1 [Setting condition] When TPU0_TCNT = TPU0_TGRA

Note: * Writing a 0 is the only way to clear this flag.

15.4.6 Timer Counter (TPU0_TCNT)

TPU0_TCNT indicates a 16-bit counter. The TPU has one TPU0_TCNT per channel.

TPU0_TCNT is initialized to H'0000 by a reset.

15.4.7 Timer General Register (TPU0_TGR)

TPU0_TGR indicates a 16-bit general register. Four general registers (TPU0_TGRA, TPU0_TGRB, TPU0_TGRC, and TPU0_TGRD) are provided for each channel. TPU0_TGRC and TPU0_TGRD can be designated for operation as buffer registers*. TPU0_TGR is initialized to H'FFFF by a reset.

Note: * The combination of TPU0_TGR and buffer register are TPU0_TGRA to TPU0_TGRC and TPU0_TGRB to TPU0_TGRD.

15.4.8 Timer Start Register (TPU0_TSTR)

TPU0_TSTR starts and stops TCNT operation for channels 0 to 3.

TPU0_TSTR is initialized to H'0000 by a reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	TMST	CST3	CST2	CST1	CST0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 5	—	All 0	R	Reserved These bits are always read as 0 and cannot be modified.
4	TMST	0	R/W	Motor Control Sequence Start This bit selects either start or stop of motor control sequence. This bit is set to 0 in stop state after motor control operation. 0: Stops motor control sequence 1: Starts motor control sequence
3	CST3	0	R/W	Counter Start
2	CST2	0	R/W	These bits select either start or stop of TPU0_TCNT
1	CST1	0	R/W	0: Stops TPU0_TCNTm count operation
0	CST0	0	R/W	1: TPU0_TCNTm count operation [Legend] m = 3 to 0

15.4.9 Motor Control Setting Register (TPU0_TMIR)

TPU0_TMIR selects setting in motor control mode.

TPU0_TMIR is initialized to H'0000 by a reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	TDMAE	MTRPATDOWN	MTRPATKIND[1:0]		MTRON
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 5	—	All 0	R	Reserved These bits are always read as 0 and cannot be modified.
4	TDMAE	0	R/W	DMA used/unused Bit Select bit to determine to use DMA for step interval input (TPU0_TGR0D writing) in motor control mode. 0: DMA unused 1: DMA used
3	MTRPAT DOWN	0	R/W	Start and Stop Pattern Transition Ascending/Descending Select Bit Select bit to determine to select the direction of transition from ascending /descending of start and stop pattern in motor control mode. 0: Ascending 1: Descending
2, 1	MTRPAT KIND[1:0|	00	R/W	Start and Stop Pattern Type Select Bit Select bit to determine to select stop and start in motor control mode. 00: Four types 01: Eight types 10: Setting prohibited 11: Setting prohibited
0	MTRON	0	R/W	TPU mode/Stepping Motor Control Mode Select Bit 0: TPU mode 1: Stepping motor control mode Note: This bit is also a selecting signal to switch TPU0TO0 to 3 output. Set to 1 after initial pattern setting. Do not modify this bit during counter operation.

15.4.10 Motor Deceleration (Stop) Transition Register (TPU0_TMRR)

Setting TPU0_TMRR to transit from normal to deceleration in motor control mode

TPU0_TMRR is initialized to H'0000 by a reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	REDUON0	REDUON
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 2	—	All 0	R	Reserved These bits are always read as 0 and cannot be modified.
1	REDUON0	0	R/W	This bit changes compulsorily from normal to deceleration (stop) in motor control mode. However, transition occurs when pattern is 0. If the state is other than normal, nothing is performed this bit automatically becomes 0, when transits to the stop state. 0: Nothing is performed. 1: Changes compulsorily from normal to deceleration (stop)
0	REDUON	0	R/W	This bit changes compulsorily from normal to deceleration (stop). If the state is other than normal, nothing is performed. This bit automatically becomes 0, when transits to the stop state. 0: Nothing is performed. 1: Changes compulsorily from normal to deceleration (stop)

15.4.11 Motor Control Status Register (TPU0_TMSR)

TPU0_TMSR is read only register and indicates the sequence transit state in motor control mode.

TPU0_TMSR is initialized to H'0001 by a reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	SITR	SITT	SITA	SITS
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 4	—	All 0	R	Reserved These bits are always read as 0 and cannot be modified.
3	SITR	0	R	This bit indicates the sequence state in motor control mode. 1: The sequence state is decelerating. 0: The sequence state is other than deceleration.
2	SITT	0	R	This bit indicates the sequence state in motor control mode. 1: The sequence state is normal. 0: The sequence state is other than normal.
1	SITA	0	R	This bit indicates the sequence state in motor control mode. 1: The sequence state is accelerating. 0: The sequence state is other than accelerating.
0	SITS	1	R	This bit indicates the sequence state in motor control mode. 1: The sequence state is stopped. 0: The sequence state is other than stopped.

15.4.12 Motor Operation Pattern Storing Register 0 (TPU0_TMMPR0)

TPU0_TMMPR0 is a register to set motor operation pattern [3 to 0] in motor control mode.

TPU0_TMMPR0 is initialized to H'0000 by a reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MP33	MP32	MP31	MP30	MP23	MP22	MP21	MP20	MP13	MP12	MP11	MP10	MP03	MP02	MP01	MP00
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	MP33	0	R/W	Motor Operation Pattern [3] in Motor Control Mode
14	MP32	0	R/W	MP33: TPU0TO3 output value in motor operation pattern [3]
13	MP31	0	R/W	
12	MP30	0	R/W	MP32: TPU0TO2 output value in motor operation pattern [3]
				MP31: TPU0TO1 output value in motor operation pattern [3]
				MP30: TPU0TO0 output value in motor operation pattern [3]
11	MP23	0	R/W	Motor Operation Pattern [2] in Motor Control Mode
10	MP22	0	R/W	MP23: TPU0TO3 output value in motor operation pattern [2]
9	MP21	0	R/W	
8	MP20	0	R/W	MP22: TPU0TO2 output value in motor operation pattern [2]
				MP21: TPU0TO1 output value in motor operation pattern [2]
				MP20: TPU0TO0 output value in motor operation pattern [2]

Bit	Bit Name	Initial Value	R/W	Description
7	MP13	0	R/W	Motor Operation Pattern [1] in Motor Control Mode
6	MP12	0	R/W	MP13: TPU0TO3 output value in motor operation pattern [1]
5	MP11	0	R/W	
4	MP10	0	R/W	MP12: TPU0TO2 output value in motor operation pattern [1]
				MP11: TPU0TO1 output value in motor operation pattern [1]
				MP10: TPU0TO0 output value in motor operation pattern [1]
3	MP03	0	R/W	Motor Operation Pattern [0] in Motor Control Mode
2	MP02	0	R/W	MP03: TPU0TO3 output value in motor operation pattern [0]
1	MP01	0	R/W	
0	MP00	0	R/W	MP02: TPU0TO2 output value in motor operation pattern [0]
				MP01: TPU0TO1 output value in motor operation pattern [0]
				MP00: TPU0TO0 output value in motor operation pattern [0]

15.4.13 Motor Operation Pattern Storing Register 1 (TPU0_TMMPR1)

TPU0_TMMPR1 is a register to set motor operation pattern [7 to 4] in motor control mode.

TPU0_TMMPR1 is initialized to H'0000 by a reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MP73	MP72	MP71	MP70	MP63	MP62	MP61	MP60	MP53	MP52	MP51	MP50	MP43	MP42	MP41	MP40
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	MP73	0	R/W	Motor Operation Pattern [7] in Motor Control Mode
14	MP72	0	R/W	MP73: TPU0TO3 output value in motor operation pattern [7]
13	MP71	0	R/W	
12	MP70	0	R/W	MP72: TPU0TO2 output value in motor operation pattern [7]
				MP71: TPU0TO1 output value in motor operation pattern [7]
				MP70: TPU0TO0 output value in motor operation pattern [7]
11	MP63	0	R/W	Motor Operation Pattern [6] in Motor Control Mode
10	MP62	0	R/W	MP63: TPU0TO3 output value in motor operation pattern [6]
9	MP61	0	R/W	
8	MP60	0	R/W	MP62: TPU0TO2 output value in motor operation pattern [6]
				MP61: TPU0TO1 output value in motor operation pattern [6]
				MP60: TPU0TO0 output value in motor operation pattern [6]
7	MP53	0	R/W	Motor Operation Pattern [5] in Motor Control Mode
6	MP52	0	R/W	MP53: TPU0TO3 output value in motor operation pattern [5]
5	MP51	0	R/W	
4	MP50	0	R/W	MP52: TPU0TO2 output value in motor operation pattern [5]
				MP51: TPU0TO1 output value in motor operation pattern [5]
				MP50: TPU0TO0 output value in motor operation pattern [5]
3	MP43	0	R/W	Motor Operation Pattern [4] in Motor Control Mode
2	MP42	0	R/W	MP43: TPU0TO3 output value in motor operation pattern [4]
1	MP41	0	R/W	
0	MP40	0	R/W	MP42: TPU0TO2 output value in motor operation pattern [4]
				MP41: TPU0TO1 output value in motor operation pattern [4]
				MP40: TPU0TO0 output value in motor operation pattern [4]

15.4.14 Motor Stop Pattern Storing Register 0 (TPU0_TMSPR0)

TPU0_TMSPR0 is a register to set motor operation pattern [3 to 0] in motor control mode.

TPU0_TMSPR0 is initialized to H'0000 by a reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SP33	SP32	SP31	SP30	SP23	SP22	SP21	SP20	SP13	SP12	SP11	SP10	SP03	SP02	SP01	SP00
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	SP33	0	R/W	Motor Stop Pattern [3] in Motor Control Mode
14	SP32	0	R/W	SP33: TPU0TO3 output value in motor stop pattern [3]
13	SP31	0	R/W	SP32: TPU0TO2 output value in motor stop pattern [3]
12	SP30	0	R/W	SP31: TPU0TO1 output value in motor stop pattern [3]
				SP30: TPU0TO0 output value in motor stop pattern [3]
11	SP23	0	R/W	Motor Stop Pattern [2] in Motor Control Mode
10	SP22	0	R/W	SP23: TPU0TO3 output value in motor stop pattern [2]
9	SP21	0	R/W	SP22: TPU0TO2 output value in motor stop pattern [2]
8	SP20	0	R/W	SP21: TPU0TO1 output value in motor stop pattern [2]
				SP20: TPU0TO0 output value in motor stop pattern [2]
7	SP13	0	R/W	Motor Stop Pattern [1] in Motor Control Mode
6	SP12	0	R/W	SP13: TPU0TO3 output value in motor stop pattern [1]
5	SP11	0	R/W	SP12: TPU0TO2 output value in motor stop pattern [1]
4	SP10	0	R/W	SP11: TPU0TO1 output value in motor stop pattern [1]
				SP10: TPU0TO0 output value in motor stop pattern [1]
3	SP03	0	R/W	Motor Stop Pattern [0] in Motor Control Mode
2	SP02	0	R/W	SP03: TPU0TO3 output value in motor stop pattern [0]
1	SP01	0	R/W	SP02: TPU0TO2 output value in motor stop pattern [0]
0	SP00	0	R/W	SP01: TPU0TO1 output value in motor stop pattern [0]
				SP00: TPU0TO0 output value in motor stop pattern [0]

15.4.15 Motor Stop Pattern Storing Register 1 (TPU0_TMSPR1)

TPU0_TMSPR1 is a register to set motor operation pattern [7 to 4] in motor control mode.

TPU0_TMSPR1 is initialized to H'0000 by a reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SP73	SP72	SP71	SP70	SP63	SP62	SP61	SP60	SP53	SP52	SP51	SP50	SP43	SP42	SP41	SP40
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	SP73	0	R/W	Motor Stop Pattern [7] in Motor Control Mode
14	SP72	0	R/W	SP73: TPU0TO3 output value in motor stop pattern [7]
13	SP71	0	R/W	SP72: TPU0TO2 output value in motor stop pattern [7]
12	SP70	0	R/W	SP71: TPU0TO1 output value in motor stop pattern [7]
				SP70: TPU0TO0 output value in motor stop pattern [7]
11	SP63	0	R/W	Motor Stop Pattern [6] in Motor Control Mode
10	SP62	0	R/W	SP63: TPU0TO3 output value in motor stop pattern [6]
9	SP61	0	R/W	SP62: TPU0TO2 output value in motor stop pattern [6]
8	SP60	0	R/W	SP61: TPU0TO1 output value in motor stop pattern [6]
				SP60: TPU0TO0 output value in motor stop pattern [6]
7	SP53	0	R/W	Motor Stop Pattern [5] in Motor Control Mode
6	SP52	0	R/W	SP53: TPU0TO3 output value in motor stop pattern [5]
5	SP51	0	R/W	SP52: TPU0TO2 output value in motor stop pattern [5]
4	SP50	0	R/W	SP51: TPU0TO1 output value in motor stop pattern [5]
				SP50: TPU0TO0 output value in motor stop pattern [5]
3	SP43	0	R/W	Motor Stop Pattern [4] in Motor Control Mode
2	SP42	0	R/W	SP43: TPU0TO3 output value in motor stop pattern [4]
1	SP41	0	R/W	SP42: TPU0TO2 output value in motor stop pattern [4]
0	SP40	0	R/W	SP41: TPU0TO1 output value in motor stop pattern [4]
				SP40: TPU0TO0 output value in motor stop pattern [4]

15.4.16 Motor Output Pattern Storing Register (TPU0_TMOPR)

TPU0_TMOPR is a register to set motor output pattern in motor control mode. It indicates types of pattern currently outputted. When this register is written when stopped, a corresponding pattern is outputted. TPU0_TMOPR is initialized to H'0000 by a reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	NOWPAT[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 13	—	All 0	R	Reserved These bits are always read as 0 and cannot be modified.
2 to 0	NOWPAT [2:0]	000	R/W	In Motor Control Mode, Reading: A current output pattern number is read. Writing: Outputs pattern number when stopped.

15.4.17 Motor Acceleration the Number of Steps Register (TPU0_TMASR)

TPU0_TMASR is a register to set the number of steps in the acceleration state of motor control mode. TPU0_TMASR is initialized to H'0000 by a reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	AS[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 0	AS[15:0]	H'0000	R/W	The number of steps in the acceleration state of motor control mode. When H'0000 is set, skips the acceleration state.

15.4.18 Motor Normal the Number of Steps Register (TPU0_TMTSR)

TPU0_TMTSR is a register to set the number of steps in normal state of motor control mode. TPU0_TMTSR is initialized to H'0000 by a reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TS[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 0	TS[15:0]	H'0000	R/W	The number of steps in normal state of motor control mode. When H'0000 is set, the normal state is maintained until 1 is written to the REDUON0 bit or REDUON bit in TPU0_TMRR.

15.4.19 Motor Deceleration the Number of Steps Register (TPU0_TMRSR)

TPU0_TMRSR is a register to set the number of steps in deceleration state of motor control mode. TPU0_TMRSR is initialized to H'0000 by a reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RS[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 0	RS[15:0]	H'0000	R/W	The number of steps in deceleration state of motor control mode. When H'0000 is set, skips deceleration state.

15.4.20 Motor Control Sequence Counter Register (TPU0_TMSCR)

TPU0_TMSCR is a register to read the sequence counter in motor control mode. It is possible to write only when motor control mode is in a normal state.

TPU0_TMSCR is initialized to H'0000 by a reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SC[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 0	SC[15:0]	H'0000	R/W	The sequence counter number in motor control mode. Reading: A sequence counter value is read. Writing: Writing is possible only in the normal state. A written value is directly stored in the sequence counter.

15.4.21 Motor Control Normal Counter Register (TPU0_TMTCR)

TPU0_TMTCR is a read only register and indicates the number of steps in the normal state of motor control mode. TPU0_TMTCR is initialized to H'0000 by a reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TCR[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 0	TCR[15:0]	H'0000	R	The number of steps in the normal state of motor control mode

15.5 Operation

15.5.1 Overview

Operation overview for each mode is as follows.

(1) Ordinary Operation

Each channel is provided with TPU0_TCNT and TPU0_TGR registers. TPU0_TCNT performs up counting, and is also capable of free-running operation, periodic counting, and external event counting.

(a) Buffer Operation

When a compare match occurs, the buffer register value in the corresponding channel is transferred to TPU0_TGR. Updating timing to rewrite from buffer registers can be selected either when a compare match occurs or when the counter is cleared.

(b) PWM Mode

In PWM mode, PWM waveform is output. The output level can be set by TPU0_TGR. PWM waveform, whose duty cycle is in the range of 0 to 100%, can be output by the settings of TPU0_TGRA and TPU0_TGRB.

(c) Stepping Motor Control Mode

A defined pattern can be outputted from TPU0TO3 to TPU0TO0 by setting channel 0 to stepping motor control mode. It changes a pattern of one step period.

15.5.2 Basic Functions

(1) Counter Operation

When the bits CST3 to CST0 in TPU0_TSTR are set to 1, the TPU0_TCNT for the corresponding channel starts counting. TPU0_TCNT can operate as a free-running counter, periodic counter, and so on.

(a) Example of Count Operation Setting Procedure

Figure 15.2 shows an example of the count operation setting procedure.

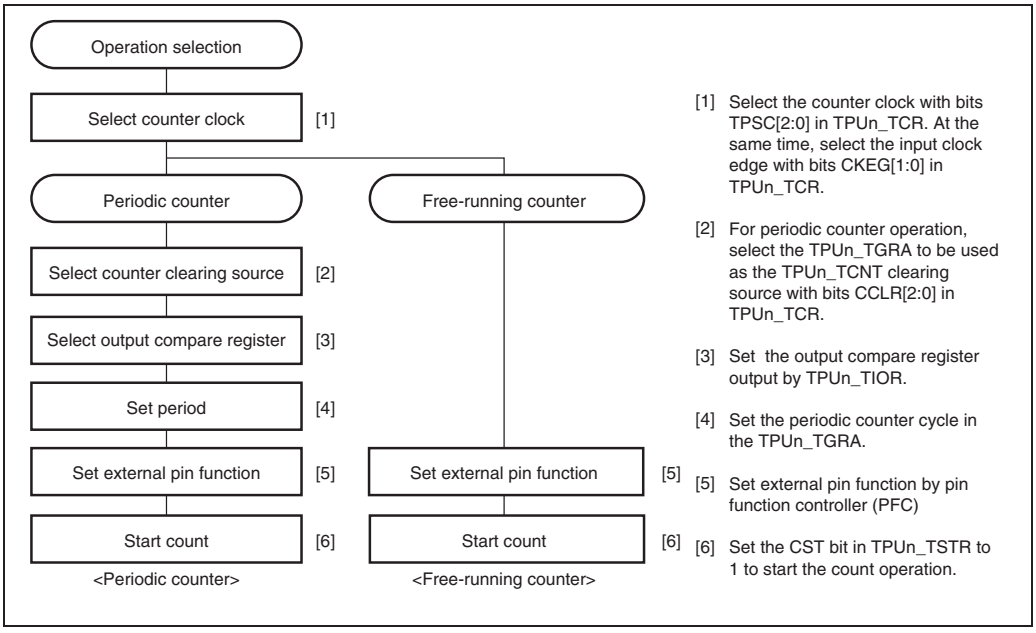


Figure 15.2 Example of Counter Operation Setting Procedure

(b) Free-Running Count Operation and Periodic Count Operation

Immediately after a reset, the TPU0_TCNT counters are all designated as free-running counters. When the relevant bit in TPU0_TSTR is set to 1, the corresponding TPU0_TCNT counter starts up-count operation as a free-running counter. When TPU0_TCNT has overflowed (changes from H'FFFF to H'0000), the TCFV bit in TPU0_TSR is set to 1. TPU0_TCNT starts counting up again from H'0000 after an overflow.

Figure 15.3 illustrates free-running counter operation.

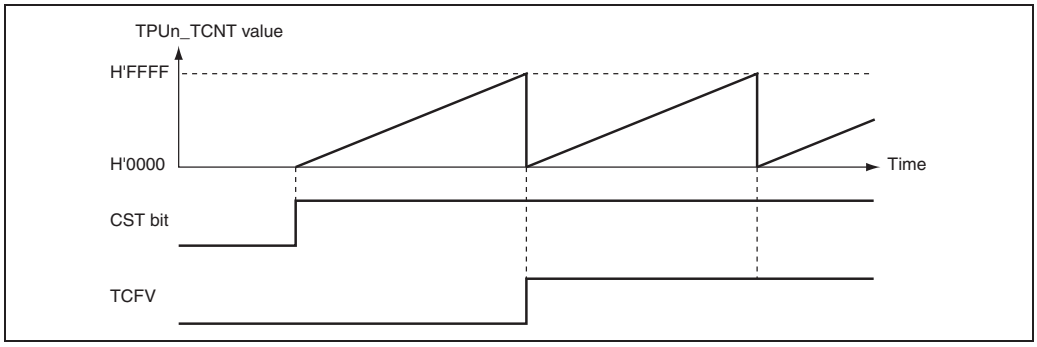


Figure 15.3 Free-Running Counter Operation

When a compare match is selected as the TPU0_TCNT clearing source, the TPU0_TCNT counter for the relevant channel performs periodic count operation. The TPU0_TGR register for setting the period is designated as an output compare register, and counter clearing by compare match is selected by means of bits CCLR[2:0] in TPU0_TCR. After the settings have been made, TPU0_TCNT starts count-up operation as a periodic counter when the corresponding bit in TPU0_TSTR is set to 1. When the count value matches the value in TPU0_TGR, the TGF bit in TPU0_TSR is set to 1 and TPU0_TCNT is cleared to H'0000.

After a compare match, TPU0_TCNT starts counting up again from H'0000.

Figure 15.4 illustrates periodic counter operation.

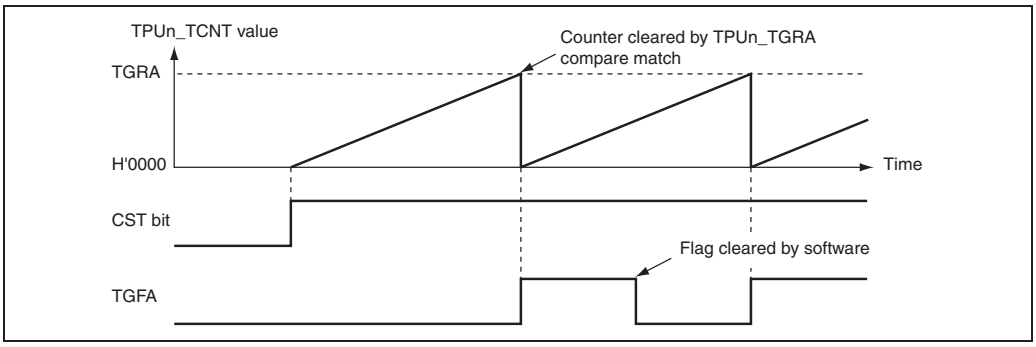


Figure 15.4 Periodic Counter Operation

(2) Waveform Output by Compare Match

The TPU can perform 0-, 1-, or toggle-output from the output pin (TPU0TO0 to 3 pins) using a TPU0_TGRA compare match.

(a) Example of Setting Procedure for Waveform Output by Compare Match

Figure 15.5 shows an example of the setting procedure for waveform output by a compare match.

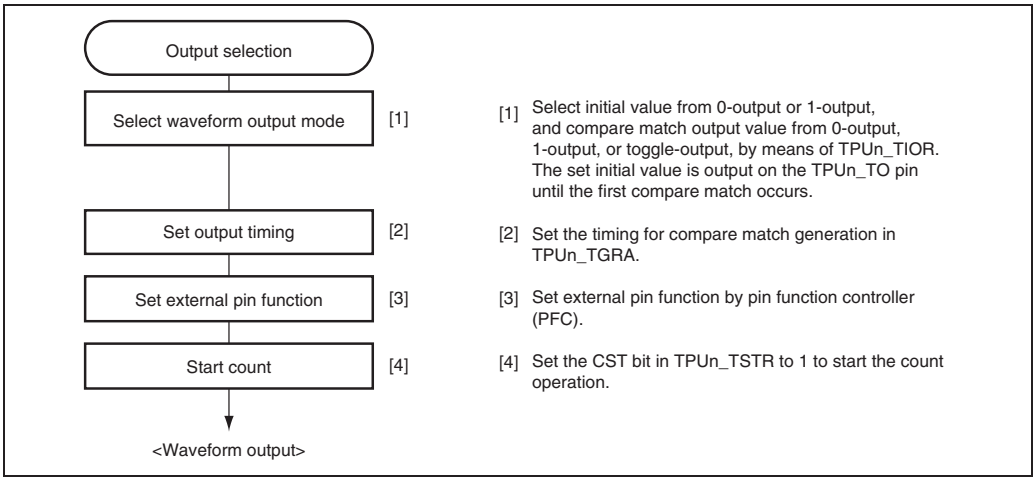


Figure 15.5 Example of Setting Procedure for Waveform Output by Compare Match

(b) Examples of Waveform Output Operation

Figure 15.6 shows an example of 0-output and 1-output.

In this example, TPU0_TCNT has been designated as a free-running counter, and settings have been made so that 1 or 0 is output by compare match A. When the set level and the pin level match, the pin level does not change.

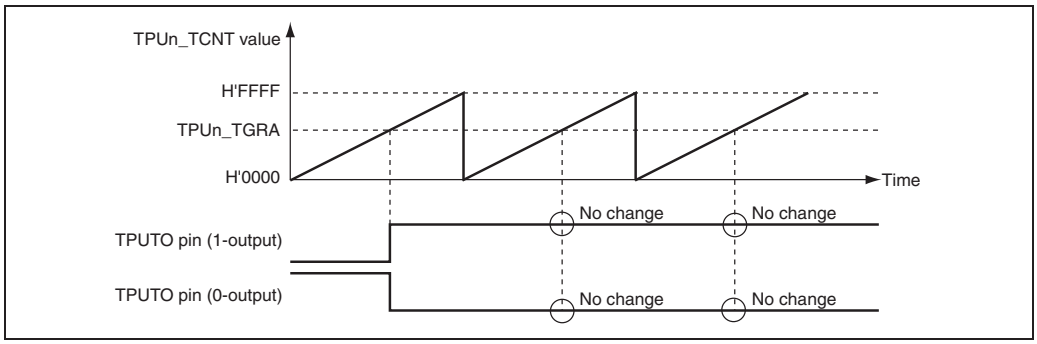


Figure 15.6 Example of 0-Output/1-Output Operation

Figure 15.7 shows an example of toggle output.

In this example, TPU0_TCNT has been designated as a periodic counter (with counter clearing performed by compare match B), and settings have been made so that output is toggled by compare match A.

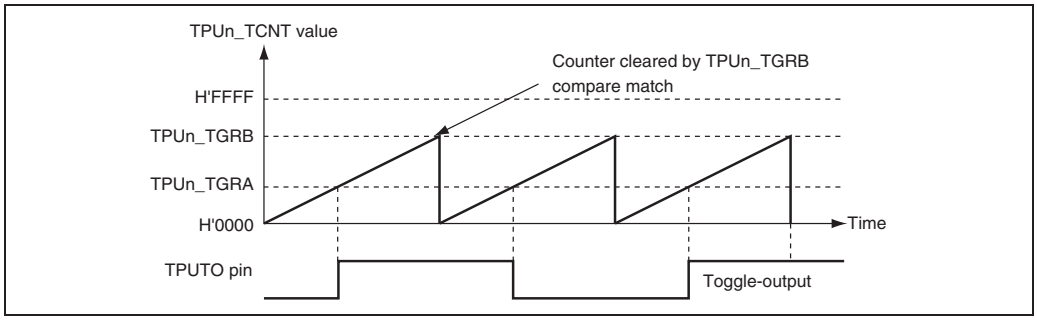


Figure 15.7 Example of Toggle Output Operation

15.5.3 Buffer Operation

TPU0_TGRC and TPU0_TGRD can be used as buffer registers.

Table 15.8 shows the register combinations used in buffer operation.

Table 15.8 Register Combinations in Buffer Operation

Timer General Register	Buffer Register
TPU0_TGRA	TPU0_TGRC
TPU0_TGRB	TPU0_TGRD

When a compare match occurs, the value in the buffer register for the corresponding channel is transferred to the timer general register. Updating timing to rewrite from buffer registers can be selected either when compare match occurs or when the counter is cleared.

This operation is illustrated in figure 15.8.

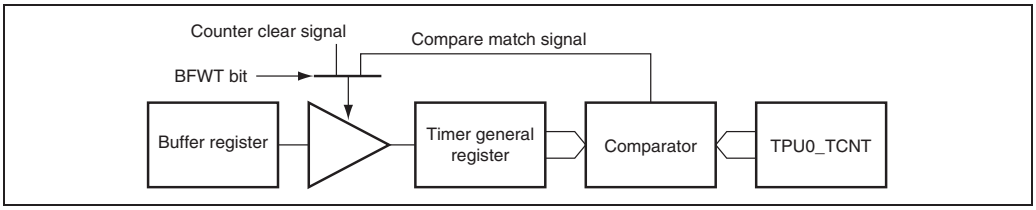


Figure 15.8 Compare Match Buffer Operation

(1) Example of Buffer Operation Setting Procedure

Figure 15.9 shows an example of the buffer operation setting procedure.

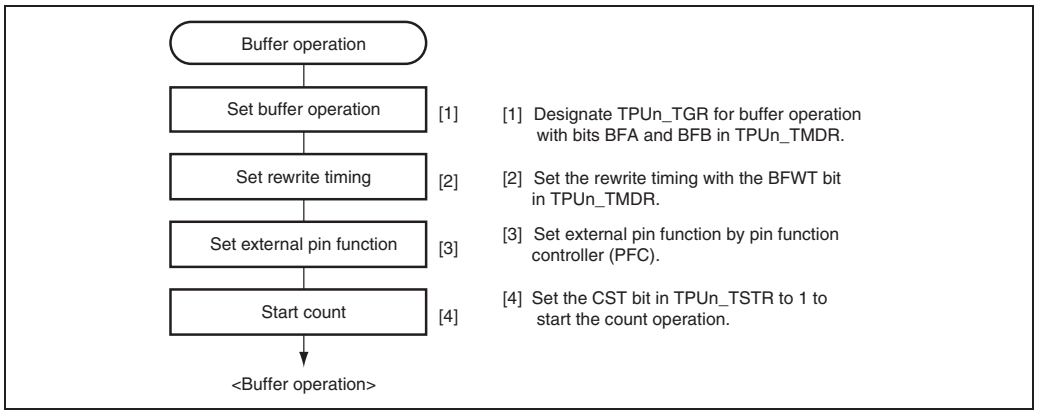


Figure 15.9 Example of Buffer Operation Setting Procedure

(2) Examples of Buffer Operation

Figure 15.10 shows an operation example in which PWM mode has been designated for channel 0, and buffer operation has been designated for TPU0_TGRA and TPU0_TGRC. The settings used in this example are TPU0_TCNT clearing by compare match B, 1-output (TPU0TO0 to 3 pin) at compare match A, initial value 0 output by counter clearing, and the rewrite timing from buffer register at counter clearing.

When compare match A occurs, the output changes. When a counter clear is generated by TPU0_TGRB, the output changes and the value in buffer register TPU0_TGRC is simultaneously transferred to the timer general register TPU0_TGRA. This operation is repeated every time compare match A occurs.

For details on PWM modes, see section 15.5.4, PWM Modes.

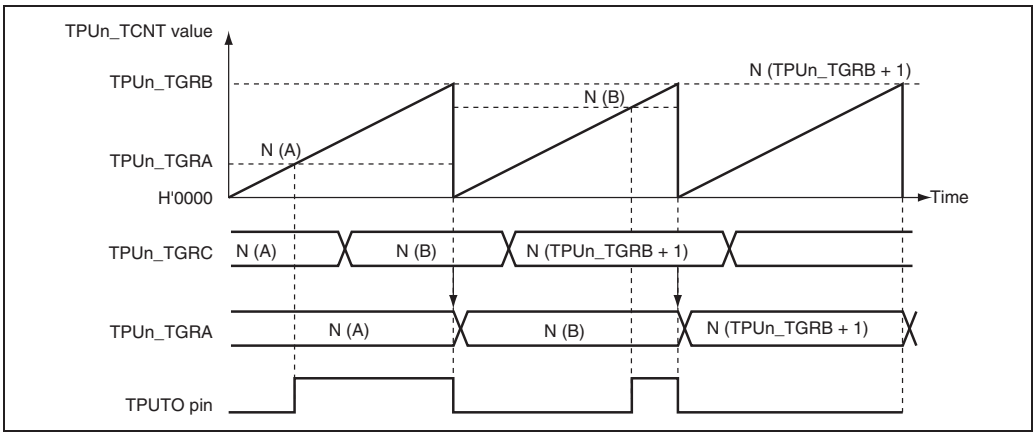


Figure 15.10 Example of Buffer Operation

15.5.4 PWM Modes

In PWM mode, PWM waveforms are output from the output pins. 0-, or 1-output can be selected as the output level in response to compare match of each TPU0_TGRA.

Designating TPU0_TGRB compare match as the counter clearing source enables the cycle to be set in that register. All channels can be designated for PWM mode independently.

PWM output is generated from the TPU0TO0 to 3 pins by using TPU0_TGRA and TPU0_TGRB as duty-cycle register and periodic register respectively. The initial output specified by TPU0_TIOR is output to TPU0TO0 to 3 pins by counter clearing due to periodic register compare match. Be sure to set TPU0_TIOR so that the initial output level is different from the compare match output. Selecting the same level or toggle output activates no operation.

Conditions on 0% and 100% duties are shown below.

- 0% duty cycle: When periodic register (TPU0_TGRB) is set to the value equal to duty-cycle register TGRA + 1
- 100% duty cycle: When duty-cycle register (TPU0_TGRA) is set to 0

In PWM mode, up to four types of PMW outputs are available.

(1) Example of PWM Mode Setting Procedure

Figure 15.11 shows an example of the PWM mode setting procedure.

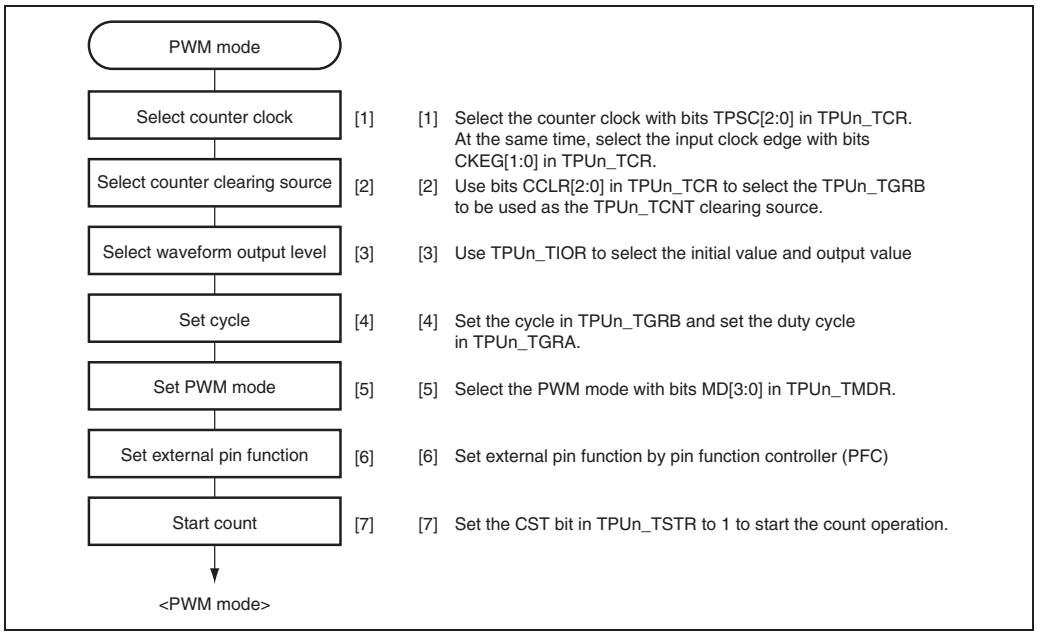


Figure 15.11 Example of PWM Mode Setting Procedure

(2) Examples of PWM Mode Operation

Figure 15.12 shows an example of PWM mode operation.

In this example, TPU0_TGRB compare match is set as the TPU0_TCNT clearing source, 0 is set for the TPU0_TGRA initial output value, and 1 is set as the output value.

In this case, the value set in TPU0_TGRB is used as the cycle, and the value set in TPU0_TGRA as the duty cycle.

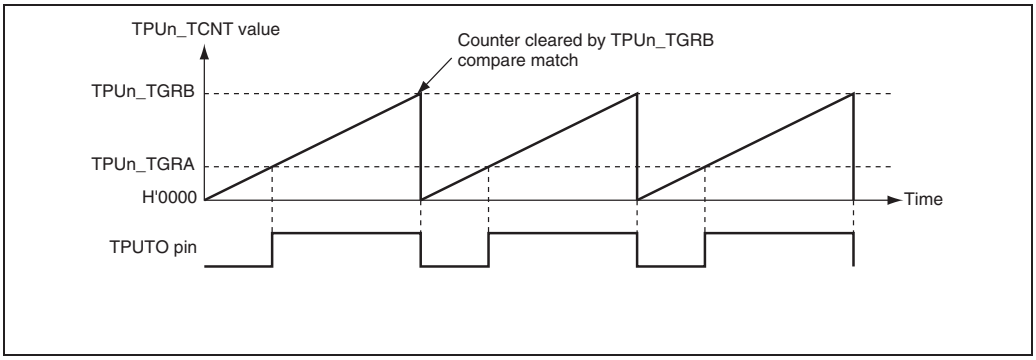


Figure 15.12 Example of PWM Mode Operation (1)

Figure 15.13 shows an example of PWM waveform output with 0% and 100% duty cycles in PWM mode.

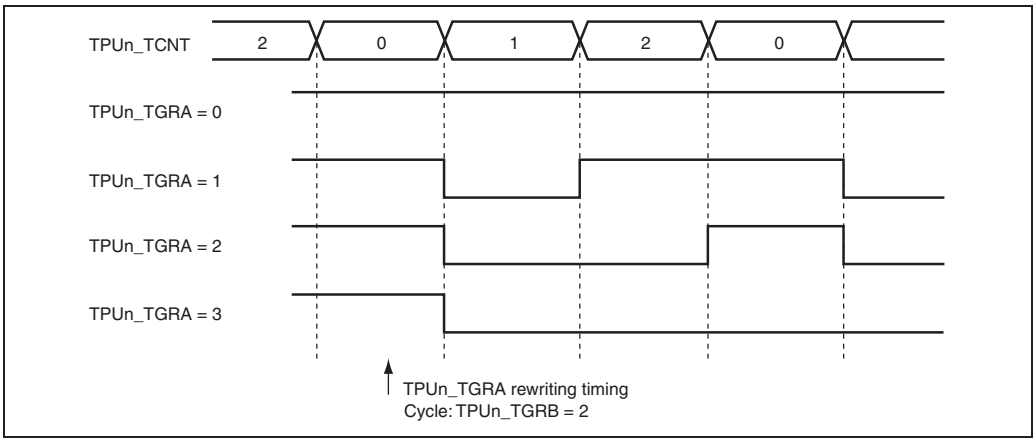


Figure 15.13 Example of PWM Mode Operation (2)

15.5.5 Stepping-Motor Control Mode

(1) Features of Stepping-Motor Control Mode

- In this mode, signals for stepping-motor control are output on four pins using only channel 0 is possible. This mode is only available on channel 0.
- States of the output pins change by counter compare matches on channel 0.

  By using the DMAC or an interrupt to rewrite the values of the compare-match registers, the intervals between transitions of the states of the output pins can be specified as desired.
- Specified patterns are output to the output pins.
- The pattern cycle consist of a four-pattern cycle and an eight-pattern cycle.
- The pattern-number counter increments or decrements by 1 by every counter compare match on channel 0.

  When the pattern-number counter overflows, its value returns to 0. When the pattern-number counter underflows, its value becomes 3 (for a four-pattern cycle) and 7 (for an eight-pattern cycle).
- Patterns consist of the stop pattern and operating patterns. Operating patterns are output while the counter is running, and a stop pattern is output while the counter is stopped.
- While the counter is running, the three states are present (the acceleration, deceleration, or normal state). Only for acceleration and deceleration, the interval of pattern change can be controlled by the DMAC or an interrupt.
- The acceleration or deceleration state can be skipped by writing H'0000 to TPU0_TMASR and TPU0_TMRSR.
- TPU0_TMRR can be used to force the transition from the normal to the deceleration state.

(2) Glossary

Sequence State:	The four states in the sequence, i.e. the acceleration, normal, deceleration, and stop states
Sequence Counter:	Counter to transit to the next sequence state. The counter is decremented with every counter compare match on channel 0 and, when the value reaches 1, the control state will make the transition to the next state in the sequence on a further counter compare match on channel 0.
Auto Mode:	Mode of operation when a value other than H'0000 has been written to TPU0_TMTSR In the normal state, pattern transitions are made by the number of times corresponding to TPU0_TMTSR, after which the transitions to the deceleration state is automatically made (when TPU0_TMRSR = H'0000, transits to the stop state).
Manual Mode:	Mode of operation when H'0000 has been written to TPU0_TMTSR. In this case, the transition from the normal to the deceleration state (stopped when TPU0_TMRSR = H'0000),) is not made unless B'1 is written to the REDUON0 and REDUON bits in TPU0_TMRR.
Pulse Mode:	Mode of operation when H'0000 has been written to TPU0_TMASR and TPU0_TMRSR. Operation is only in the normal state, so patterns with constant intervals are output.
Step:	The pattern is changed with every counter compare match on channel 0. Step refers to the interval of time between the change to one pattern and the change to the next.
Operation Pattern:	The four-bit patterns for output in the acceleration, normal, and deceleration states.
Stop Pattern:	The four-bit patterns for output in stop state.

(3) Setting up Basic Motor Control Operation

An example of operation in stepping motor control is shown in figure 15.14.

Stepping-motor control mode allows the output of patterns with a variable step interval.

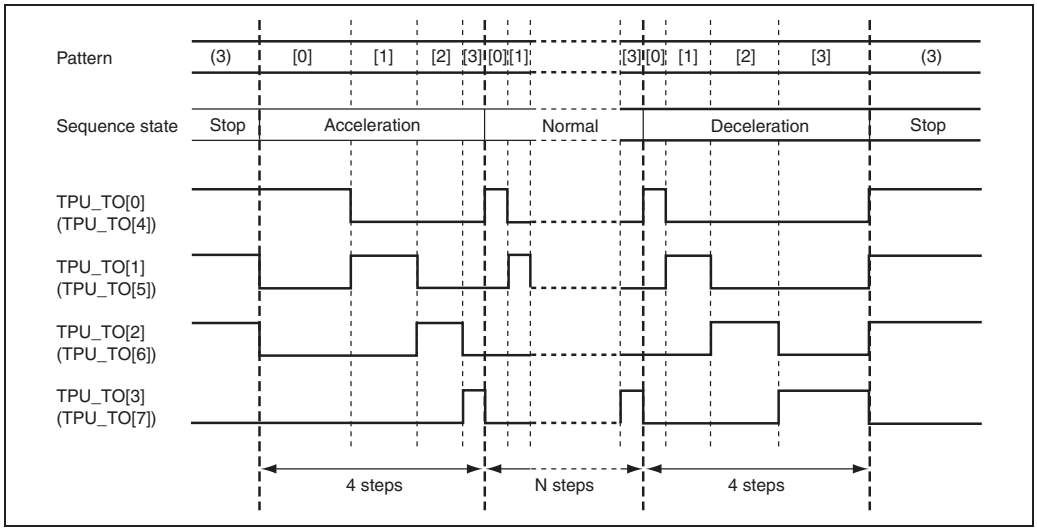


Figure 15.14 Example of Stepping-Motor Control

(a) Compare Match Settings on Channel 0

For stepping motor control, set TPU0_TCR0 and TPU0_TMDR0 as follows:

Table 15.9 Compare Match Settings on Channel 0

Register	Setting	Description
TPU0_TCR0	B'0000 0000 0100 0xxx	CCLR[2:0] bits = B'010 CKEG[1:0] bits = B'00 TPSC[2:0] bits = B'xxx (optional)
TPU0_TMDR0	B'0000 0000 0110 0000	BFWT bit = B'1 BFB bit = B'1 BFA bit = B'0 MD[2:0] bits = B'000

[Legend]
x: Don't care.

With the above settings, TPU0_TGR0B and TPU0_TGR0D can be used as buffer registers, and the contents of the buffer are rewritten when the counter is cleared. The step interval can be changed by using DMA transfer or an interrupt by writing a desired value in TPU0_TGR0D.

The TPSC[2:0] bits in TPU0_TCR0 are for a timer prescaler setting. The step interval is calculated from the following formula.

Let CPϕ be 33 MHz, TPSC[2:0] in TPU0_TCR0 contain =B'011, and TPU0_TGR0D contain H'1425.

$$\text{Step interval} = P\phi \text{ cycle} \times \left\{ \begin{array}{l} 1\ (\text{TPU0_TCR0.TPSC[2:0]} = \text{B'000}) \\ 4\ (\text{TPU0_TCR0.TPSC[2:0]} = \text{B'001}) \\ 16\ (\text{TPU0_TCR0_TPSC[2:0]} = \text{B'010}) \\ 64\ (\text{TPU0_TCR0.TPSC[2:0]} = \text{B'011}) \end{array} \right\} \times \text{TPU0_TGR0D}$$

The result for the above settings is 30.3 ns × 64 × 5157 (H'1425) = 10,000,454.4 ns ≅ 10 ms. The pattern will change after approximately 10 ms.

(b) Sequence State and the Number of Steps

In stepping-motor control mode, the three states (acceleration, normal, and deceleration) are present during counter operation. In acceleration and deceleration states, the step interval can be changed. In this case, the number of times patterns are changed is set to TPU0_TGR0D.

In the normal state, the step interval cannot be changed. So, TPU0_TGR0D is only set once for a given period.

The numbers of steps in the acceleration, normal, and deceleration states are set in TPU0_TMASR, TPU0_TMTSR, and TPU0_TMRSR, respectively. If H'0000 is written to TPU0_TMASR or TPU0_TMRSR, the corresponding state is skipped. Furthermore, the manual mode can be selected by writing H'0000 to TPU0_TMTSR. In this mode, the transition from normal mode can only be initiated by changing the value in TPU0_TMRR.

Table 15.10 gives descriptions of the sequence states and figure 15.15 shows the transitions between sequence states.

Table 15.10 Description of Sequence States

		Description	
Start/Stop	**State**	**Step Interval**	**Definition in TPU0_TGR0D**
Start	Acceleration	Variable	The number of steps specified for this state
	Normal	Not variable	Only once
	Deceleration	Variable	The number of steps specified for this state
Stop	Stop	—	—

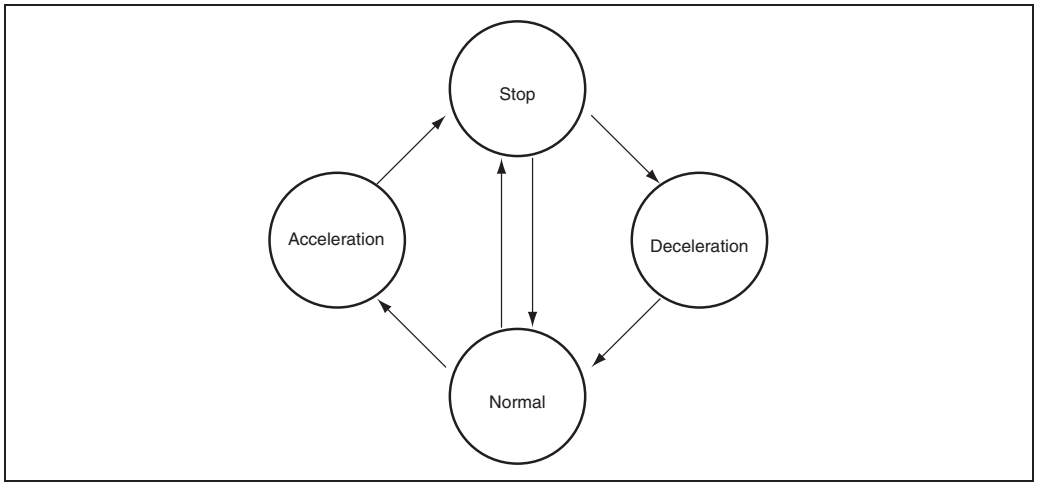


Figure 15.15 Sequence State Transition

(c) Setting of Step Interval

Direct memory access or interrupt-driven transfer can be used to set the step interval

- DMA transfer

Setting the TDMAE bit in TPU0_TMIR to B'1 allows the use of DMA transfer to modify the step interval.

The number of requests for DMA is given by TPU0_TMASR + 1 (the step interval in the normal state) + TPU0_TMRSR. The step intervals must be defined in sequence on the basis of the address indicated by the DMA source address register. Figure 15.16 shows an example of timing in operation with DMA transfer requests used to set up the step intervals. Figure 15.17 shows the definitions of step interval in the address map for this example.

Table 15.11 lists an example of DMA configurations.

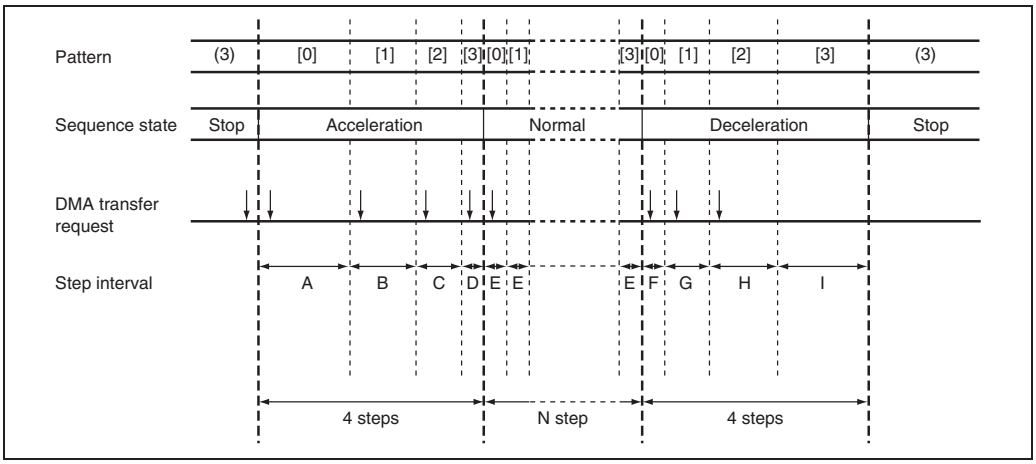


Figure 15.16 Operation with DMA Transfer Requests Used to Adjust the Step Interval

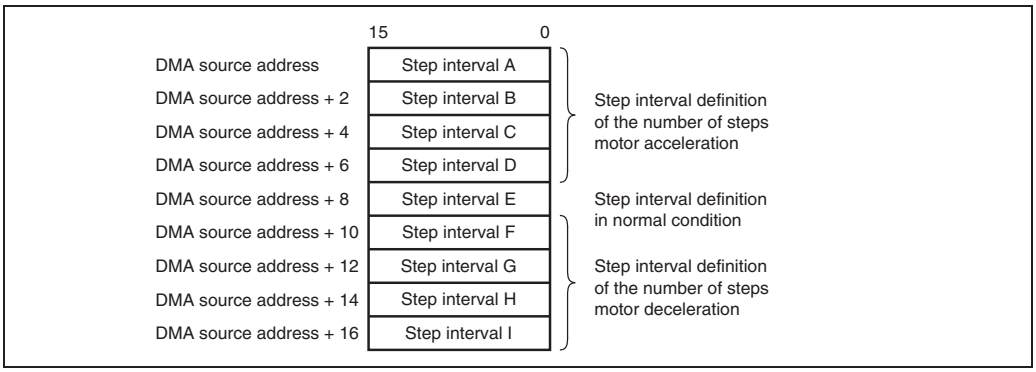


Figure 15.17 Address Map of Step Interval Definitions for the Example of Operation

Table 15.11 DMA Configurations

DMA Register	Setting	Description
DMA source address register	H'XXXX XXXX	Address where the table of step intervals starts
DMA destination address register	H'E660 0034, H'E661 0034, H'E662 0034 H'E663 0034, or H'E664 0034	Address of TPU0_TGR0D
DMA transfer count register	H'0000 0000	(The maximum number of transfer operations.) *
DMA transfer count register B	H'XXXX XXXX	The number of DMA transfer requests are set in the higher- and lower-order 16 bits. (for figure 15.16, H'0009 0009)
DMA channel control register	H'0E00 1809	Reload mode: Use source address registers (SARs) as the source for reloading. Fixed destination address. Incrementation of source address. Make selections with the DMA extension resource selector. DMA word (two-byte) unit transfer. The other bits are in the default settings
DMA extended resource register	H'F1 in the bit field for the selected DMA channel	TPU0
DMA operation register	H'0001	Permits DMA transfer on all channels. The other bits are in the default settings

Note: * Transfer is stopped when the DMA transfer counter is reaches 0. Rewrite the value of the DMA transfer counter to 1 after TPU-related operation is finished.

- Interrupt-driven transfer

Setting the TMDRFE bit in TPU0_TIER0 to B'1 allows the use of interrupt-driven transfer to change the step interval.

TPU0_TMASR−1 + 1 (the step interval in the normal state) + TPU0_TMRSR gives the number of times TPU0_TGR0D must be written to by interrupt-driven transfer.

This method is unlike DMA transfer in that an interrupt is not generated when the initial transfer is required. The Initial value should be written to TPU0_TGR0D before counter operation starts.

Once an interrupt is generated, write the step interval to TPU0_TGR0D on the interrupt subroutine and write B'0 after read B'1 from the TMDRFS bit.

Figure 15.18 shows an example of timing in operation with interrupt-driven transfer used to set up the step intervals.

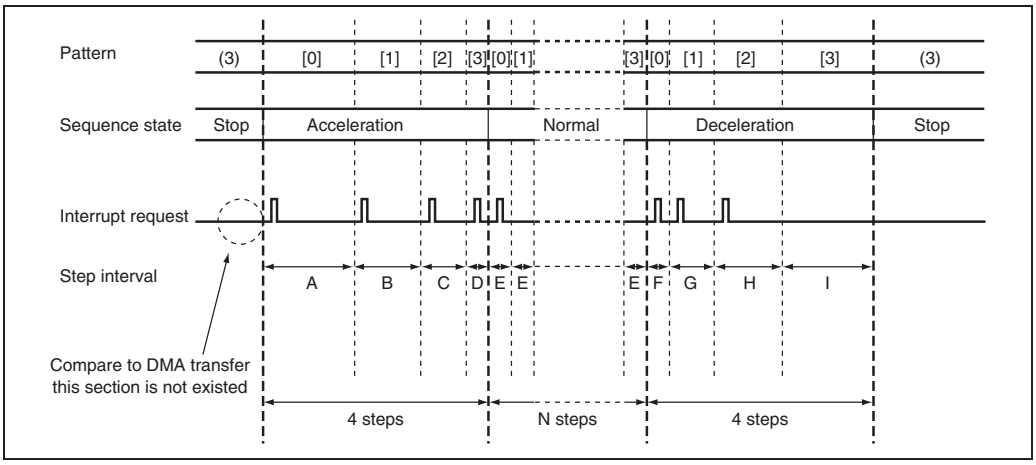


Figure 15.18 Interrupt Request and Step Interval

The step-interval definition in the example of operation shown in figure 15.18 is as follows.

Write step interval A in TPU0_TGR0D before counter starts.
Write step interval B in TPU0_TGR0D at first interrupt. } Step interval definition of the number
Write step interval C in TPU0_TGR0D at second interrupt. } of steps motor acceleration
Write step interval D in TPU0_TGR0D at third interrupt.
Write step interval E in TPU0_TGR0D at fourth interrupt. Step interval definition in normal condetion
Write step interval F in TPU0_TGR0D at fifth interrupt.
Write step interval G in TPU0_TGR0D at sixth interrupt. } Step interval definition of the number
Write step interval H in TPU0_TGR0D at seventh interrupt. } of steps motor deceleration
Write step interval I in TPU0_TGR0D at eighth interrupt.

(d) Pattern Setting

In stepping-motor control mode, each four-bit value for output on pins TPU0TO0 to TPU0TO3 is regarded as a single pattern. The patterns are in a sequence, and a counter compare match triggers the transition to the next pattern.

The following rules apply to pattern transfer.

- Either a four- or an eight-pattern cycle is available. This is determined by the MTRPATKIND bit in TPU0_TMIR0.
- Each pattern is indicated by a pattern number. The current pattern number is either incremented or decremented on each counter compare match. Incrementation or decrementation is determined by the MTRPATDOWN bit in TPU0_TMIR0.
- The pattern-number counter returns to 0 when it overflows. When it underflows, the pattern number is three (for a four-pattern cycle) or seven (for an eight-pattern cycle).
- Operating patterns are defined as the output patterns in the acceleration, normal, and deceleration states, and stop patterns are defined as the output patterns in the stop state. In transitions from an operating pattern to a stop pattern, the pattern number remains the same. In transitions from a stop pattern to an operating pattern, the current pattern number is changed to that of the next pattern.

Operating patterns are set in TPU0_TMMPR0 and TPU0_TMMPR1, and stop patterns are set in TPU0_TMSPR0 and TPU0_TMSPR1.

Table 15.12 lists the order of patterns for different settings of the MTRPATDOWN and MTRPATKIND bits in TPU0_TMIR.

Table 15.12 Settings of the MTRPATDOWN and MTRPATKIND Bits in TPU0_TMIR and Pattern Order

TPU0_TMIR		Example of Pattern Order
MTRPATDOWN Bit	MTRPATKIND Bits	(Operating Pattern [ ], Stop Pattern ( ))
B'0	B'00	[0]→[1]→[2]→[3]→[0]→[1]→[2]→[3]→(3)→[0]
B'1		[0]→[3]→[2]→[1]→[0]→[3]→[2]→[1]→(1)→[0]
B'0	B'01	[0]→[1]→[2]→[3]→[4]→[5]→[6]→[7]→(7)→[0]
B'1		[0]→[7]→[6]→[5]→[4]→[3]→[2]→[1]→(1)→[0]

(e) Specifying the Output Pattern in the Stop State

When a pattern number is specified in the NOWPAT[2:0] bits in TPU0_TMOPR in the stop state, the corresponding pattern is output on pins TPU0TO3 to TPU0TO0. The Initial value is 0.

(f) Selecting the Stepping-Motor control Mode

Stepping-motor control by the TPU circuit is selected by setting the MTRON bit in TPU0_TMIR to 1. The output on pins TPU0TO3 to TPU0TO0 is switched to the output corresponding to stepping-motor control.

Switching should be performed while the motor is stopped.

The stop pattern specified as pattern 0 in TPU0_TMOPR is output after switching. Therefore, verify the value in TPU0_TMOPR or write the desired pattern to TPU0_TMOPR.

(g) Start Stepping-Motor Control

Stepping-motor control is started by setting the TMST bit in TPU0_TSTR to 1. This bit is automatically cleared (to 0) in the stop state after motor-control operations are over.

(h) Example of the Procedure for Setting up Stepping-Motor Control

Figure 15.19 is a flowchart for stepping-motor control.

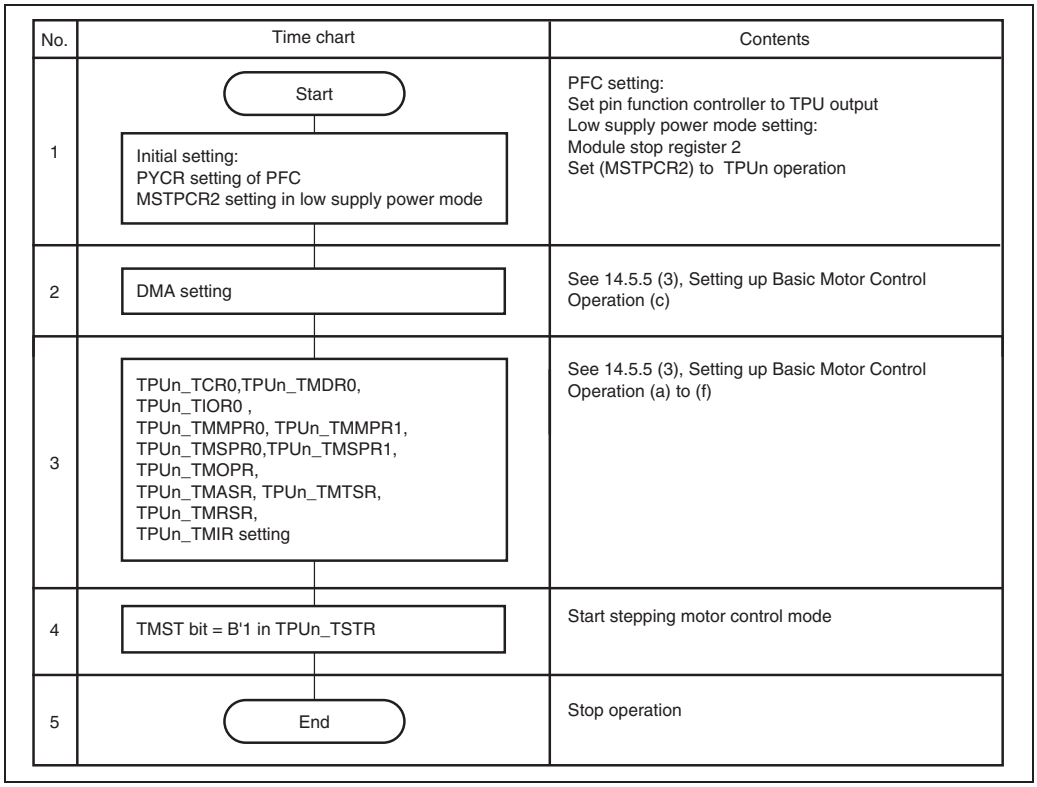


Figure 15.19 Flowchart

(4) Changing the Number of Steps in Normal State.

The number of steps in the normal state is set in TPU0_TMTSR. To change the number of steps, take the procedure given under (a) or (b) below.

In manual mode (TPU0_TMTSR = H'0000), it is impossible to switch from the normal state without performing (a).

(a) Changes by TPU0_TMRR

Writing 1 to the REDUON0 bit or the REDUON bit in TPU0_TMRR initiates the transition to the deceleration state (if TPU0_TMRSR = H'0000, the transition is to the stop state).

Table 15.13 describes how operation in response to the writing of 1 to the REDUON0 bit varies with the operating state. Table 15.14 describes how operation in response to the writing of 1 to the REDUON bit varies with the operating state.

Table 15.13 Timing of Writing 1 to the REDUON0 Bit and Operation

Timing of Writing 1 to the REDUON0 Bit	Operation
Acceleration	Operation continues normally until the end of acceleration. Control then enters the normal state and remains there until the pattern number becomes [0]. The transition to the deceleration state (or the stop state if TPU0_TMRSR is H'0000) is made at the end of the step in the normal state with pattern number [0].
Normal	Control remains in the normal state until the pattern number becomes [0]. The transition to the deceleration state (or the stop state if TPU0_TMRSR is H'0000) is made at the end of the step in the normal state with pattern number [0].
Deceleration	Writing 1 to the bit has no effect.
Stop	Writing to this bit after control has made the transition from the normal or deceleration state to the stop state clears TPU0_TMRR to H'0000. When 1 is written to the REDUON0 bit after the stop state, the normal state continues until the pattern number becomes [0] when it enters the normal state in the next round of the motor control. The transition to the deceleration state (or the stop state if TPU0_TMRSR is H'0000) is made at the end of the step in the normal state with pattern number [0].

Table 15.14 Timing of Writing 1 to the REDUON Bit and Operation

Timing to Write 1 in REDUON Bit	Operation
Acceleration	Operation continues normally until the end of acceleration. The transition to the deceleration state (or the stop state if TPU0_TMRSR is H'0000) is then made after a single step in the normal state.
Normal	The transition to the deceleration state (or the stop state if TPU0_TMRSR is H'0000) is made at the end of the current step interval
Deceleration	Writing 1 to the bit has no effect
Stop	Writing to this bit after control has made the transition from the normal or deceleration state to the stop state clears TPU0_TMRR to H'0000. In this case, the normal state in the next round of motor control will only continue through a single step. The transition to the deceleration state (or the stop state if TPU0_TMRSR is H'0000) is made at the end of that step.

(b) Changing the Number of Steps by Changing the Value in TPU0_TMSCR

In auto mode (TPU0_TMTSR ≠ H'0000), TMSCR indicates the remaining number of steps in the current state.

In the normal state, the number of steps can be changed by writing the desired number of steps. Writing is invalid in states other than the normal state.

Do not write to this register in manual mode (TPU0_TMTSR = H'0000).

(5) Acquiring the Number of Steps in the Normal State

In the stop state, TPU0_TMTCR can be read to acquire the number of steps in the immediately preceding normal state.

(6) Pulse Mode

Writing H'0000 to TPU0_TMASR and TPU0_TMSSR selects operation in the normal state alone, when the step interval is constant. Operation starts with the step interval defined for the normal mode and the interval does not subsequently change. Operation of this kind is referred to as pulse mode.

Examples of pulse-mode operation are described below.

(a) Single Pulse Shift in Pulse Mode and Auto Mode

Table 15.15 gives an example of register settings for a given number of pulse steps in auto mode.

Figure 15.20 is a timing chart for single pulse shift in auto mode

Table 15.15 Register Settings to Select the Number of Steps for One Pulse in Auto Mode

Register Setting Value	Contents
TPU0_TMASR: H'0000	No acceleration state
TPU0_TMTSR: H'0001	Only one step in the normal state
TPU0_TMRSR: H'0000	No deceleration state

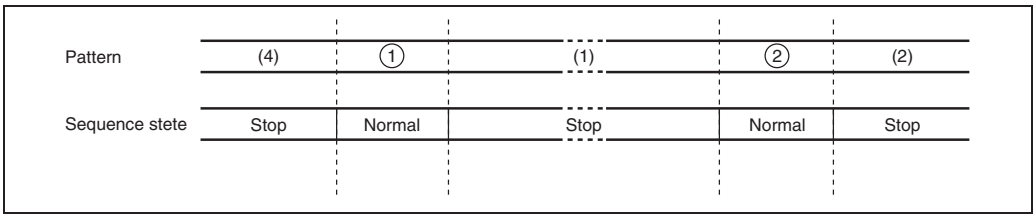


Figure 15.20 Timing of Single Pulse Shift in Auto Mode

(b) Single Pulse Shift in Pulse Mode and Manual Mode

Setting REDUON0 and REDUON bits in TPU0_TMRR to 1 in the normal state enables a single pulse shift in manual mode.

Table 15.16 gives an example of register settings for a given number of pulse steps in manual mode.

Figure 15.21 is a timing chart for single pulse shift in manual mode

Table 15.16 Register Settings to Select the Number of Steps for One Pulse in Manual Mode

Register Setting Value	Contents
TPU0_TMASR: H'0000	No acceleration state
TPU0_TMTSR: H'0000	Looping in the normal state
TPU0_TMRSR: H'0000	No deceleration state

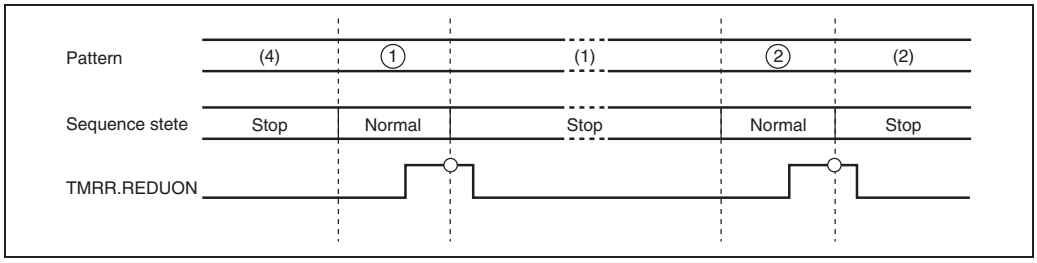


Figure 15.21 Timing of Single Pulse Shift in Manual Mode

(7) Interrupts

For stepping-motor control mode, six interrupt conditions have been added to channel 0.

The interrupt conditions are described below.

(a) Detection of Overflows of Data Transferred for Motor Control

Setting the TMDOFE bit in TPU0_TIER0 to 1 selects the detection of overflow of data transferred for motor control (motor control data transfer overflow). This condition arises when buffer operation, i.e. the transfer of the data from TPU0_TGR0D, is delayed; that is, when the operation TPU0_TGR0D→ TPU0_TGR0B is delayed. To cancel this interrupt, write 0 to the TMDOFS bit of TPU0_TSR0 after having read it as 1.

Figure 15.22 shows an example of DMA transfer where an overflow of data transferred for motor control occurs and detection of this overflow has been enabled.

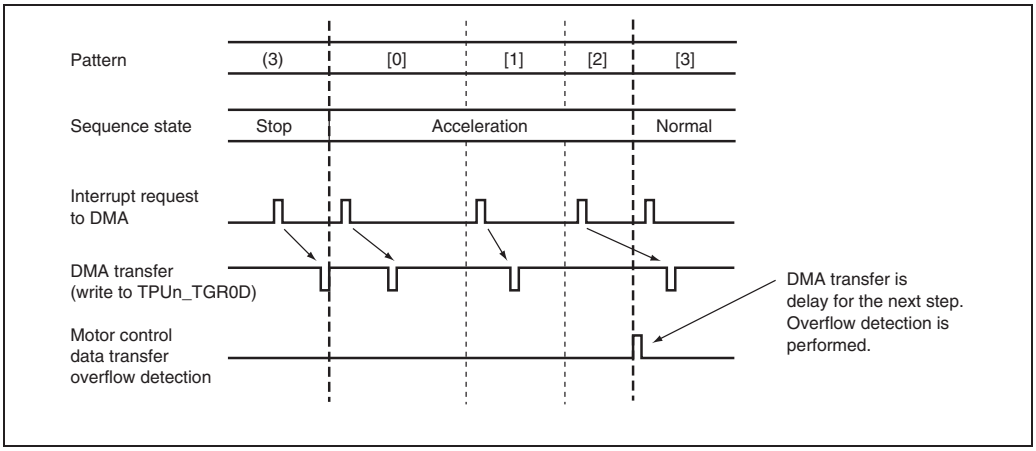


Figure 15.22 DMA Transfer with Detection of Motor Control Data Transfer Overflow Enabled

Since this interrupt is for use in the debugging of defective operation, normal operation will not be restored even if it is detected.

(b) Detection of Requirement for Transfer of Motor control Data

Detection of requirement for transfer of the motor control data (detect motor control data transfer request) is enabled by setting the TMDRFE bit of TPU0_TIER0. This interrupt occurs when the next pattern interval can change from the current interval. On detection of this interrupt, the setting for the next interval should be written to TPU0_TGR0D. After writing the new interval data, write 0 to the TMDRFS bit of TPU0_TGR0 after having read it as 1.

Do not use this interrupt if DMA transfer has been selected (the TDMAE bit in TPU0_TMIR = 1).

See figure 15.18 for an example of usage of this interrupt.

(c) Detecting the Transition to Deceleration.

Setting the TMS1ER bit in TPU0_TIER0 to B'1 enables detection of the transition to deceleration (detect motor control deceleration transition) After writing, write 0 to the TMCFR bit of TPU0_TSR0 after having read it as 1.

(d) Detecting the Transition to the Normal State

Setting the TMS1ET bit in TPU0_TIER0 to B'1 enables detection of the transition to the normal state (detect motor control normal transition). After writing, write 0 to the TMCFT bit of TPU0_TSR0 after having read it as 1.

(e) Detecting the Transition to Acceleration

Setting the TMS1EA bit in TPU0_TIER0 to B'1 enables detection of the transition to acceleration (detect motor control acceleration transition). After writing, write 0 to the TMCFA bit of TPU0_TSR0 after having read it as 1.

(f) Detecting the Transition to the Stop State

Setting the TMS1ES bit in TPU0_TIER0 to B'1 enables detection of the transition to the stop state (detect motor control stop transition) After writing, write 0 to the TMCFS bit of TPU0_TSR0 after having read it as 1.

(8) Checking the State of Operation

Read TPU0_TMSR and TPU0_TMSCR to check the current state of operations. TPU0_TMSCR indicates a value that is decremented (for every counter compare match) from the value in the number of steps register (TPU0_TMASR, TPU0_TMTSR, or TPU0_TMRSR) during sequence transition.

Figure 15.23 shows how the values in TPU0_TMSR and TPU0_TMSCR vary through the four states. As is shown in the figure, the current interval within the overall sequence of state transitions can be estimated by, for example reading TPU0_TMSR = H'0008 and TPU0_TMSCR = H'0003.

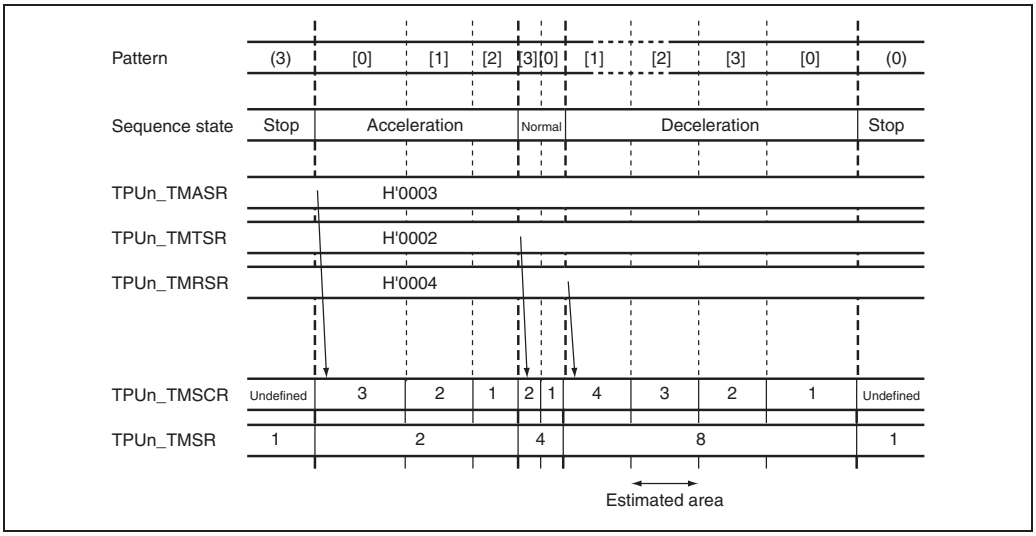


Figure 15.23 Values of TPU0_TMSR and TPU0_TMSCR

Section 16 Compare Match Timer 0 (CMT0)

This LSI includes a 32-bit compare match timer (CMT0) of one channel.

16.1 Features

- One channel installed in the real-time domain
- 16 bits/32 bits can be selected.
- Provided with an auto-reload up counter.
- Provided with 32-bit constant registers and 32-bit up counters that can be written or read at any time.
- The CMT0 can perform counting even if this LSI is in power control mode controlled by the SYSC.
- Allows selection among three counter input clocks:
  - External clock (RCLK) input: 1/8, 1/32, and 1/128
- One-shot operation and free-running operation are selectable.
- Allows selection of compare match or overflow for the interrupt source.
- Supports the cancel of the standby state in power control mode controlled by the SYSC.
- Module standby mode can be set.
- Allows selection of counter operation/stop during debugging with the debug mode operation selector.

Figure 16.1 shows a block diagram of the CMT0.

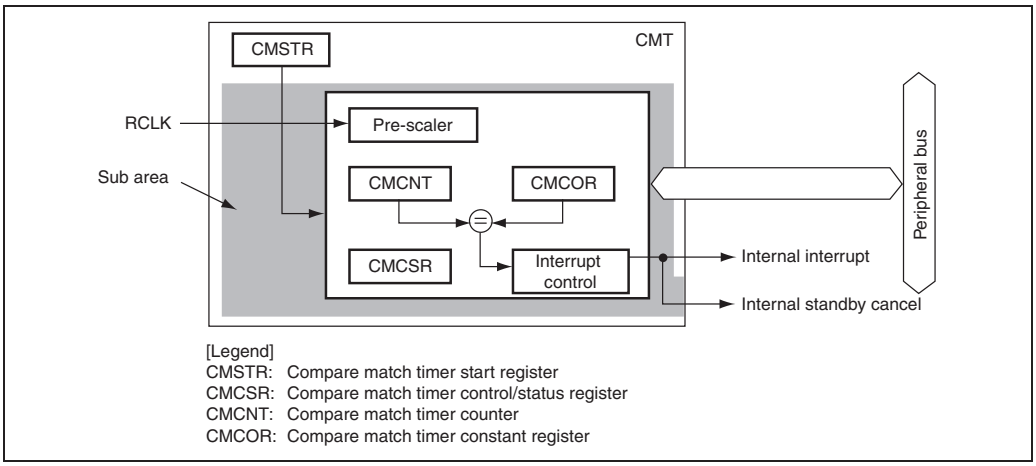


Figure 16.1 Block Diagram of CMT0

Table 16.1 shows the CMT functions list.

Table 16.1 Functions List

Function		CMT0	CMT1						CMT2	CMT3	CMT4
			ch0	ch1	ch2	ch3	ch4	ch5			
Counter size	16 bits	Available	Available	Available	Available	Available	Available	Available	Available	Available	Available
	32 bits	Available	Available	Available	Available	Available	Available	Available	Available	Available	Available
	48 bits	N/A	Available	Available	Available	Available	Available	Available	N/A	N/A	N/A
Counter input clock *	COMCLK 1/1	N/A	Available	N/A	N/A	N/A	Available	Available	N/A	N/A	N/A
	COMCLK 1/8	N/A	Available	N/A	N/A	N/A	Available	Available	N/A	N/A	N/A
	COMCLK 1/32	N/A	Available	N/A	N/A	N/A	Available	Available	N/A	N/A	N/A
	COMCLK 1/128	N/A	Available	N/A	N/A	N/A	Available	Available	N/A	N/A	N/A
	RCLK 1/1	N/A	N/A	N/A	N/A	Available	N/A	N/A	Available	Available	Available
	RCLK 1/8	Available	Available	Available	Available	Available	Available	Available	Available	Available	Available
	RCLK 1/32	Available	Available	Available	Available	Available	Available	Available	Available	Available	Available
	RCLK 1/128	Available	Available	Available	Available	Available	Available	Available	Available	Available	Available
	Pseudo 32kHz 1/1	N/A	Available	Available	Available	Available	Available	Available	N/A	N/A	N/A
Mode of operation	One shot	Available	Available	Available	Available	Available	Available	Available	Available	Available	Available
	Free running	Available	Available	Available	Available	Available	Available	Available	Available	Available	Available
Operation at the time of a comparison match.	Interrupt request	Available	Available	Available	Available	Available	Available	Available	Available	Available	Available
	Wakeup request	Available	N/A	Available	Available	Available	N/A	N/A	Available	N/A	N/A
	DMA transfer request	N/A	Available	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
"Counter start/halt" RCLK synchronous mode.		N/A	Available	N/A	N/A	Available	N/A	N/A	N/A	N/A	N/A
Debug Mode Operation(Counter enable/halt) Select.		Available	Available	Available	Available	Available	Available	Available	Available	Available	Available
Counting the number of comparison matches.		N/A	Available	N/A	N/A	Available	N/A	N/A	N/A	N/A	N/A

* COMCLK : AP / common part main clocks 1/2

16.2 Register Descriptions

Table 16.2 shows the CMT0 register configuration. Table 16.3 shows the register states in each operating mode.

Table 16.2 Register Configuration

Register Name	Abbreviation	R/W	Address	Access Size
Compare match timer start register	CMSTR	R/W	H'FFCA 0000	16
Compare match timer control/status register	CMCSR	R/W	H'FFCA 0060	16
Compare match timer counter	CMCNT	R/W	H'FFCA 0064	32
Compare match timer constant register	CMCOR	R/W	H'FFCA 0068	32

Table 16.3 Register States in Each Operating Mode

Register Abbreviation	Reset *	A4R Area Reset	Module Standby
CMSTR	Initialized	Retained	Retained
CMCSR	Initialized	Retained	Retained
CMCNT	Initialized	Retained	Retained
CMCOR	Initialized	Retained	Retained

Note: * For details, refer to section 1-D Overview of reset.

16.2.1 Compare Match Timer Start Register (CMSTR)

CMSTR is a 16-bit register that selects whether the compare match timer counter (CMCNT) is operated or halted.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	STR5	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	STR5	0	R/W	Count Start Selects whether to operate or halt the compare match timer counter (CMCNT). 0: Halts CMCNT count 1: Starts CMCNT count
4 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

16.2.2 Compare Match Timer Control/Status Register (CMCSR)

CMCSR is a 16-bit register that indicates the occurrence of compare matches, enables interrupts, and sets the counter input clocks.

Do not change bits other than the CMF and OVF bits during the compare match timer counter (CMCNT) operation.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMF	OVF	WR FLG	—	—	—	CMS	CMM	CMTOUT_IE	—	CMR[1:0]		DBG IVD	CKS[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
R/W:	R/(W)*	R/(W)*	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	CMF	0	R/(W)*	Compare Match Flag This flag indicates whether or not values of the compare match timer counter (CMCNT) and compare match timer constant register (CMCOR) have matched. Software cannot write 1 to the bit. When one-shot is selected for the counter operation, counting resumes by clearing this bit. 0: CMCNT and CMCOR values have not matched [Clearing condition] • Write 0 to CMF 1: CMCNT and CMCOR values have matched
14	OVF	0	R/(W)*	Overflow Flag This flag indicates whether or not the compare match timer counter (CMCNT) has overflowed and been cleared to 0. Software cannot write 1 to this bit. 0: CMCNT has not overflowed [Clearing condition] • Write 0 to OVF 1: CMCNT has overflowed

Bit	Bit Name	Initial Value	R/W	Description
13	WRFLG	0	R	Write State Flag CMCNT cannot be written to when this bit is 1. This bit indicates the period that the writing to CMCNT is masked for synchronization after the writing to CMCNT. Confirm that this flag is 0 when CMCNT is written to continuously.
12 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	CMS	0	R/W	Compare Match Timer Counter Size Selects whether the compare match timer counter (CMCNT) is used as a 16-bit counter or a 32-bit counter. This setting becomes the valid size for the compare match timer constant register (CMCOR). 0: Operates as a 32-bit counter 1: Operates as a 16-bit counter
8	CMM	0	R/W	Compare Match Mode Selects one-shot operation or free-running operation of the counter. 0: One-shot operation 1: Free-running operation
7	CMTOUT_IE	0	R/W	Compare Match Standby Mode Cancel Enable Enables or disables the cancel of various standby modes. 0: The cancel of various standby modes by this CMT0 is disabled. 1: The cancel of various standby modes by this CMT0 is enabled. This bit is backed up.
6	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
5, 4	CMR[1:0]	00	R/W	Compare Match Request These bits enable or disable an internal interrupt request in a compare match. 00: Disables an internal interrupt request. 01: Setting prohibited 10: Enables an internal interrupt request. 11: Setting prohibited Note: When various standby modes are canceled by the CMT0, these bits should be set to B'10. These bits are backed up.
3	DBGIVD	1	R/W	Debug Mode Operation Select Sets the counter operation in debug mode. 0: Stops the counter operation in debug mode. 1: Enables the counter operation even in debug mode.
2 to 0	CKS[2:0]	100	R/W	Clock Select These bits select the clock input to CMCNT. When the count start bit (STR5) in CMSTR is set to 1, CMCNT begins incrementing with the clock selected by these bits. 000: Setting prohibited 001: Setting prohibited 010: Setting prohibited 011: Setting prohibited 100: RCLK/8 101: RCLK/32 110: RCLK/128 111: Setting prohibited

Note: * Only 0 can be written to clear the flag.

16.2.3 Compare Match Timer Counter (CMCNT)

CMCNT is a 32-bit register that is used as an up-counter.

A counter operation is set by the compare match timer control/status register (CMCSR). Therefore, set CMCSR first, before starting a channel operation corresponding to the compare match timer start register (CMSTR). When the 16-bit counter operation is selected by the CMS bit, bits 15 to 0 of this register become valid. When the register should be written to, write the data that is added H'0000 to the upper half in a 32-bit operation. The contents of this register are initialized to H'00000000.

Counter operation of CMT0 is enabled even when the peripheral clock is stopped. Counter operation is also enabled in a state where the core-area power supply is turned off during power control mode controlled by the SYSC.

When CMCNT is going to be read during the counter operation, the value that is read out may be wrong because of an asynchronous clock. Read several times with software and compare the read-out values.

16.2.4 Compare Match Timer Constant Register (CMCOR)

CMCOR is a 32-bit register that sets the compare match period with CMCNT.

When the 16-bit counter operation is selected by the CMS bit in CMCSR, bits 15 to 0 of this register become valid. When the register should be written to, write the data that is added H'0000 to the upper half in a 32-bit operation.

An overflow is detected when CMCNT is cleared to 0 and this register is H'FFFFFFFF. The contents of this register are initialized to H'FFFFFFFF.

16.3 Operation

16.3.1 Counter Operation

The CMT0 starts the operation of the counter by writing B'1 to the STR5 bit in CMSTR after each register has been set. Complete all of the settings before starting the operation. Do not change the register settings other than by clearing flag bits during the compare match timer (CMCNT) operation.

The counter operates in one of two ways.

- One-Shot Operation

  One-shot operation is selected by setting the CMM bit in CMCSR to B'0. When the value in CMCNT matches the value in CMCOR, the value in CMCNT is cleared to H'00000000 and the CMF bit in CMCSR is set to B'1. Counting by CMCNT stops after it has been cleared.

  To detect an overflow interrupt, set the value in CMCOR to H'FFFFFFFF. When the value in CMCNT matches the value in CMCOR, CMCNT is cleared to H'00000000 and the CMF and OVF bits in CMCSR are set to B'1.

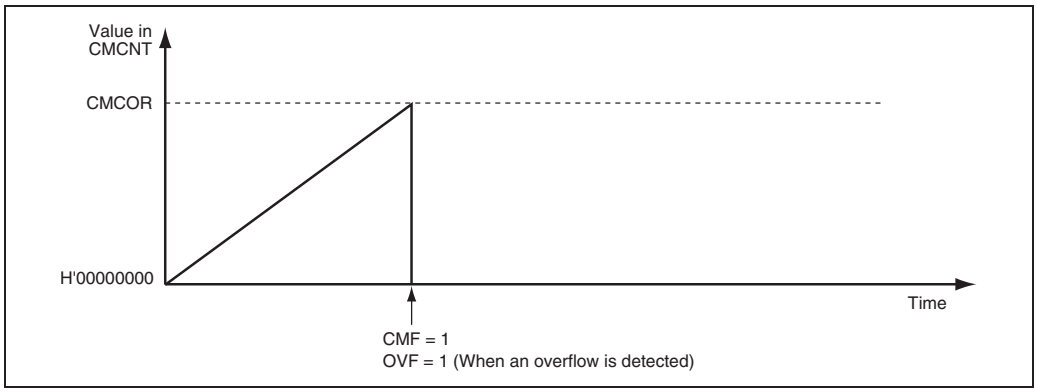


Figure 16.2 Counter Operation (One-Shot Operation)

- Free-Running Operation

  Free-running operation is selected by setting the CMM bit in CMCSR to B'1. When the value in CMCNT matches the value in CMCOR, CMCNT is cleared to H'00000000 and the CMF bit in CMCSR is set to B'1. CMCNT resumes counting-up after it has been cleared.

To detect an overflow interrupt, set CMCOR to H'FFFFFFFF. When the values in CMCNT and CMCOR match, CMCNT is cleared to H'00000000 and the CMF and OVF bits in CMCSR are set to B'1.

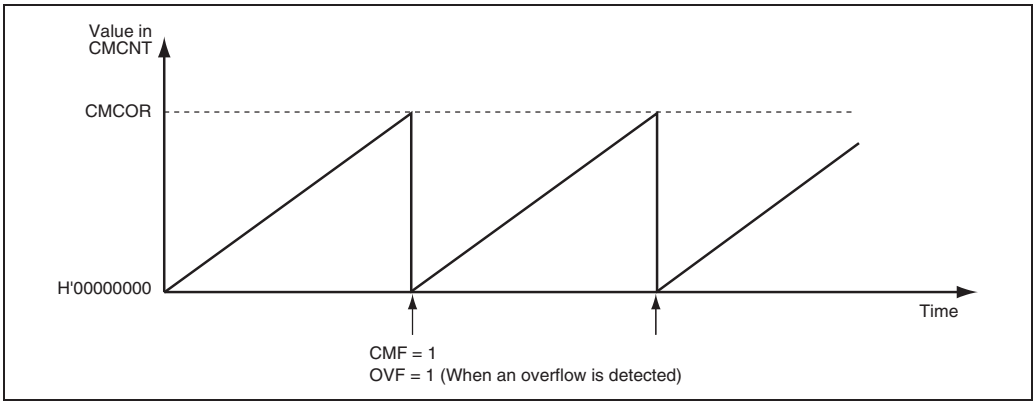


Figure 16.3 Counter Operation (Free-Running Operation)

16.3.2 Counter Size

In this module, the size of the counter is selectable as either 16 or 32 bits. This is selected by the CMS bit in CMCSR.

When the 16-bit size is selected, use a 32-bit value which has H'0000 as its upper half to set CMCOR. To detect an overflow interrupt, CMCOR must be set to H'0000FFFF.

16.3.3 Timing for Counting by CMCNT

In this module, the clock for the counter can be selected from among the following:

- External clock (RCLK): 1/8, 1/32, and 1/128

The clock for the counter is selected by the CKS bits in CMCSR. CMCNT is incremented at the rising edge of the selected clock.

16.3.4 Internal Interrupt Request to CPU

The setting of the CMR bits in CMCSR selects the sending of an internal interrupt request to the CPU at a compare match.

To clear the internal interrupt request to the CPU, the CMF bit should be set to B'0. Set the CMF bit to 0 in the handling routine for the CMT0 interrupt.

16.3.5 CMT0 Operation

As CMCNT can be operated only by the RCLK, it continues the counter operation even when this LSI makes the transition to power control mode controlled by the SYSC and the core-area power supply is turned off after the necessary register settings have been made and B'1 has been written to the STR5 bit in CMSTR.

- Register Access

  The counter for the CMT0 is located in the sub area because the counter has to be able to count-up even when this LSI is in power control mode controlled by the SYSC. The registers that are needed for the counter's operation are set from the core area. The following restrictions thus apply to the modification of the registers.

After the following registers have been modified, do not make the transition to power control mode controlled by the SYSC until you are sure that, according to the restrictions given below, the result of the modification has been reflected in the LSI's actual operation. Otherwise, the modification may not be reflected in an actual result.

- CMCSR: Bits CKS, CMM, CMS, and CMTOUT_IE
- CMCOR: Bits 31 to 0
- CMSTR: Bit STR5

Two RCLK cycles are necessary before this register is either read or any modification of the value it holds is reflected in the LSI's actual operation.

- CMCNT: Bits 31 to 0

Two RCLK cycles are necessary before this register is either read or any modification of the value it holds is reflected in the LSI's actual operation. Writing to this register, once started, is protected from further write operations until the writing operation has been completed.

- Cancel of Various Standby Modes
  When an interrupt occurs while the system is in standby mode or power control mode controlled by the SYSC, various standby modes can be canceled if the CMTOUT_IE bit in CMCSR is set to B'1 and the CMR bits to B'10.
  Set the CMF bit in CMCSR to B'0 after various standby modes are canceled.

16.3.6 Compare Match Flag Set Timing

The CMF bit in CMCSR is set to 1 by the compare match signal generated when CMCOR and CMCNT match. The compare match signal is generated upon the final state of the match (timing at which the CMCNT value is updated to H'0). Consequently, after CMCOR and CMCNT match, a compare match signal will not be generated until a CMCNT counter clock is input. Figure 16.4 shows the set timing of the CMF bit.

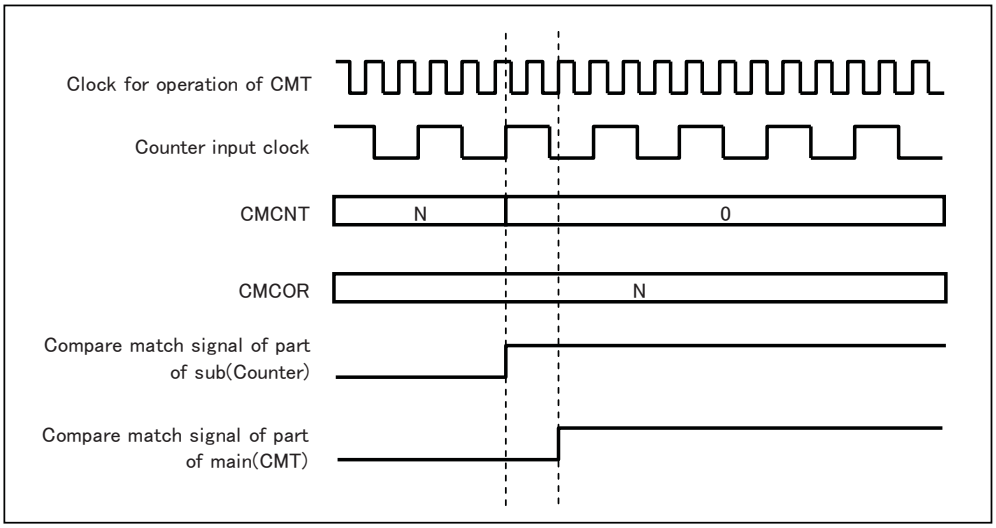


Figure 16.4 CMF Set Timing

Section 17 Compare Match Timer 1 (CMT1)

This LSI includes a 32-bit compare match timer (CMT1) of four channels (channel 0 to channel 3).

17.1 Features

- Six channels installed in the system domain
- 16 bits/32 bits/48 bits can be selected.
- Provided with an auto-reload up counter.
- Provided with 48-bit constant registers and 48-bit up counters that can be written or read at any time.
- Allows selection among eight counter input clocks for channel 0,4,5:
  - AP/COMMON MAIN CLOCK 1/2 (13 MHz) input: 1/8, 1/32, 1/128, and 1/1
  - External clock (RCLK) input: 1/8, 1/32, and 1/128
  - External clock (Pseudo32KHz) input: 1/1
- Allows selection among four counter input clocks for channels 1 and 2:
  - External clock (RCLK) input: 1/8, 1/32, and 1/128
  - External clock (Pseudo32KHz) input: 1/1
- Allows selection among five counter input clocks for channel 3:
  - External clock (RCLK) input: 1/1, 1/8, 1/32, and 1/128
  - External clock (Pseudo32KHz) input: 1/1
- One-shot operation and free-running operation are selectable.
- Allows selection of compare match for the interrupt source.
- Supports the cancellation of the standby state in power control mode controlled by the SYSC for channels 1 to 3.
- DMA transfer requests are enabled at a compare match for channel 0.
- Module standby mode can be set.
- RCLK-synchronous counter start/stop mode for channel 0 , enable interrupt request in RCLK-synchronous counter start/stop mode
- Counter operation can be enabled or disabled at the time of debugging using the debugging mode operation selector.

Figure 17.1 shows a block diagram of the CMT1.

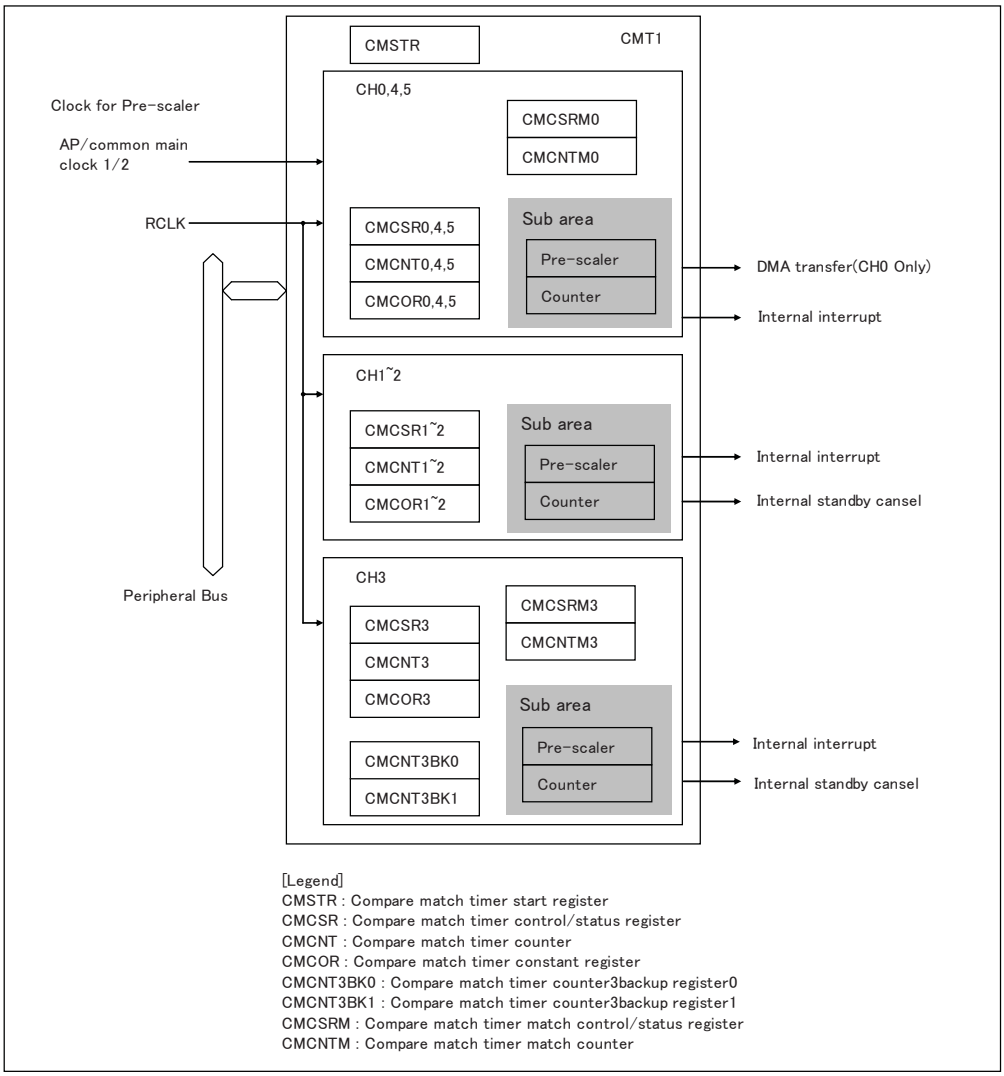


Figure 17.1 Block Diagram of CMT1

17.2 Register Descriptions

Table 17.1 shows the CMT1 register configuration. Table 17.2 shows the register states in each operating mode.

Table 17.1 Register Configuration

Register Name	Abbreviation	R/W	Address		Access Size
			Regular	Shadow	
Compare match timer start register	CMSTR	R/W	H'E613 8000	H'E713 8000	16
Compare match timer control/status register 0	CMCSR0	R/W	H'E613 8010	H'E713 8010	16
Compare match timer control/status register 1	CMCSR1	R/W	H'E613 8020	H'E713 8020	16
Compare match timer control/status register 2	CMCSR2	R/W	H'E613 8030	H'E713 8030	16
Compare match timer control/status register 3	CMCSR3	R/W	H'E613 8040	H'E713 8040	16
Compare match timer control/status register 4	CMCSR4	R/W	H'E613 8050	H'E713 8050	16
Compare match timer control/status register 5	CMCSR5	R/W	H'E613 8060	H'E713 8060	16
Compare match timer control/status register H0	CMCSRH0	R/W	H'E613 8110	H'E713 8110	16
Compare match timer control/status register H1	CMCSRH1	R/W	H'E613 8120	H'E713 8120	16
Compare match timer control/status register H2	CMCSRH2	R/W	H'E613 8130	H'E713 8130	16
Compare match timer control/status register H3	CMCSRH3	R/W	H'E613 8140	H'E713 8140	16
Compare match timer control/status register H4	CMCSRH4	R/W	H'E613 8150	H'E713 8150	16
Compare match timer control/status register H5	CMCSRH5	R/W	H'E613 8160	H'E713 8160	16
Compare match timer counter 0	CMCNT0	R/W	H'E613 8014	H'E713 8014	32
Compare match timer counter 1	CMCNT1	R/W	H'E613 8024	H'E713 8024	32
Compare match timer counter 2	CMCNT2	R/W	H'E613 8034	H'E713 8034	32
Compare match timer counter 3	CMCNT3	R/W	H'E613 8044	H'E713 8044	32
Compare match timer counter 4	CMCNT4	R/W	H'E613 8054	H'E713 8054	32

Compare match timer counter 5	CMCNT5	R/W	H'E613 8064	H'E713 8064	32
Compare match timer counter H0	CMCNTH0	R/W	H'E613 8114	H'E713 8114	16
Compare match timer counter H1	CMCNTH1	R/W	H'E613 8124	H'E713 8124	16
Compare match timer counter H2	CMCNTH2	R/W	H'E613 8134	H'E713 8134	16
Compare match timer counter H3	CMCNTH3	R/W	H'E613 8144	H'E713 8144	16
Compare match timer counter H4	CMCNTH4	R/W	H'E613 8154	H'E713 8154	16
Compare match timer counter H5	CMCNTH5	R/W	H'E613 8164	H'E713 8164	16
Compare match timer constant register 0	CMCOR0	R/W	H'E613 8018	H'E713 8018	32
Compare match timer constant register 1	CMCOR1	R/W	H'E613 8028	H'E713 8028	32
Compare match timer constant register 2	CMCOR2	R/W	H'E613 8038	H'E713 8038	32
Compare match timer constant register 3	CMCOR3	R/W	H'E613 8048	H'E713 8048	32
Compare match timer constant register 4	CMCOR4	R/W	H'E613 8058	H'E713 8058	32
Compare match timer constant register 5	CMCOR5	R/W	H'E613 8068	H'E713 8068	32
Compare match timer constant register H0	CMCORH0	R/W	H'E613 8118	H'E713 8118	16
Compare match timer constant register H1	CMCORH1	R/W	H'E613 8128	H'E713 8128	16
Compare match timer constant register H2	CMCORH2	R/W	H'E613 8138	H'E713 8138	16
Compare match timer constant register H3	CMCORH3	R/W	H'E613 8148	H'E713 8148	16
Compare match timer constant register H4	CMCORH4	R/W	H'E613 8158	H'E713 8158	16
Compare match timer constant register H5	CMCORH5	R/W	H'E613 8168	H'E713 8168	16
Compare match timer counter 3 backup 0	CMCNT3BK0	R	H'E613 8080	H'E713 8080	32
Compare match timer counter 3 backup 1	CMCNT3BK1	R	H'E613 8084	H'E713 8084	32
Compare match timer match control/status register 0	CMCSRM0	R/W	H'E613 8090	H'E713 8090	16
Compare match timer match control/status register 3	CMCSRM3	R/W	H'E613 80C0	H'E713 80C0	16
Compare match timer match counter 0	CMCNTM0	R/W	H'E613 8094	H'E713 8094	32
Compare match timer match counter 3	CMCNTM3	R/W	H'E613 80C4	H'E713 80C4	32

Table 17.2 Register States in Each Operating Mode

Register Abbreviation	Reset *	Module Standby
CMSTR	Initialized	Retained
CMCSR0	Initialized	Retained
CMCSR1	Initialized	Retained
CMCSR2	Initialized	Retained
CMCSR3	Initialized	Retained
CMCSR4	Initialized	Retained
CMCSR5	Initialized	Retained
CMCSRH0	Initialized	Retained
CMCSRH1	Initialized	Retained
CMCSRH2	Initialized	Retained
CMCSRH3	Initialized	Retained
CMCSRH4	Initialized	Retained
CMCSRH5	Initialized	Retained
CMCNT0	Initialized	Retained
CMCNT1	Initialized	Retained
CMCNT2	Initialized	Retained
CMCNT3	Initialized	Retained
CMCNT4	Initialized	Retained
CMCNT5	Initialized	Retained
CMCNTH0	Initialized	Retained
CMCNTH1	Initialized	Retained
CMCNTH2	Initialized	Retained
CMCNTH3	Initialized	Retained
CMCNTH4	Initialized	Retained
CMCNTH5	Initialized	Retained
CMCOR0	Initialized	Retained
CMCOR1	Initialized	Retained
CMCOR2	Initialized	Retained
CMCOR3	Initialized	Retained
CMCOR4	Initialized	Retained

CMCOR5	Initialized	Retained
CMCORH0	Initialized	Retained
CMCORH1	Initialized	Retained
CMCORH2	Initialized	Retained
CMCORH3	Initialized	Retained
CMCORH4	Initialized	Retained
CMCORH5	Initialized	Retained
CMCNT3BK0	Initialized	Retained
CMCNT3BK1	Initialized	Retained
CMCSRM0	Initialized	Retained
CMCSRM3	Initialized	Retained
CMCNTM0	Initialized	Retained
CMCNTM3	Initialized	Retained

Note: * For details, refer to section 1-D Overview of reset.

17.2.1 Compare Match Timer Start Register (CMSTR)

CMSTR is a 16-bit register that selects whether the compare match timer counter (CMCNT) is operated or halted.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	STR0RS	–	–	STR5	STR4	STR3	STR2	STR1	STR0
Initial Value:	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	STR0RS	0	R/W	RCLK-Synchronous Counter Start/Stop Mode Select (only in channel 0) 0: Normal operation Channel 0 starts or stops counting immediately after STR0 is written to. 1: RCLK-synchronous counter start/stop mode Channel 0 starts or stops counting on detecting an RCLK rising edge after STR0 is written to.
7 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5 to 0	STR5	0	R/W	Count Start 5 to 0 These bits select whether to operate or halt the compare match timer counter (CMCNT5 to CMCNT0) of each channel. 0: Halts CMCNTn count 1: Starts CMCNTn count Note: n corresponds to the channel number from 5 to 0.
	STR4	0	R/W	
	STR3	1	R/W	
	STR2	0	R/W	
	STR1	0	R/W	
	STR0	0	R/W	

17.2.2 Compare Match Timer Control/Status Register 0 to 5 (CMCSR)

CMCSR is a 16-bit register that indicates the occurrence of compare matches, enables interrupts and DMA transfer requests, and sets the counter input clocks.

Do not change bits other than the CMF and OVF bits during the compare match timer counter (CMCNT) operation.

CMCSR0

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMF	OVF	WRFLG	CH0 STTF	CH0 STPF	CH0 SSIE	CMS	CMM	–	–	CMR[1:0]		DBG IVD	CKS[2:0]		
Initial Value:	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
R/W:	R/(W)*	R/(W)*	R	R/(W)*	R/(W)*	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

CMCSR1

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMF	OVF	WRFLG	–	–	–	CMS	CMM	CMT OUT_IE	–	CMR		DBG IVD	CKS		
Initial Value:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
R/W:	R/(W)*	R/(W)*	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W

CMCSR2

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMF	OVF	WRFLG	–	–	–	CMS	CMM	CMT OUT_IE	–	CMR		DBG IVD	CKS		
Initial Value:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
R/W:	R/(W)*	R/(W)*	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W

CMCSR3

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMF	OVF	WRFLG	–	–	–	CMS	CMM	CMT OUT_IE	–	CMR		DBG IVD	CKS		
Initial Value:	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	1
R/W:	R/(W)*	R/(W)*	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W

CMCSR4

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMF	OVF	WRFLG	–	–	–	CMS	CMM	–	–	CMR[1:0]		DBG IVD	CKS[2:0]		
Initial Value:	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
R/W:	R/(W)*	R/(W)*	R	R	R	R	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

CMCSR5

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMF	OVF	WRFLG	–	–	–	CMS	CMM	–	–	CMR[1:0]		DBG IVD	CKS[2:0]		
Initial Value:	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
R/W:	R/(W)*	R/(W)*	R	R	R	R	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description

Bit	Bit Name	Initial Value	R/W	Description
15	CMF	0	R/(W)*	Compare Match Flag This flag indicates whether or not values of the compare match timer counter (CMCNT) and compare match timer constant register (CMCOR) have matched. Software cannot write 1 to the bit. When one-shot is selected for the counter operation, counting resumes by clearing this bit. 0: CMCNT and CMCOR values have not matched [Clearing conditions] • Write 0 to CMF after reading CMF = 1 (channel 0) • Write 0 to CMF (channels 1 to 3) 1: CMCNT and CMCOR values have matched
14	OVF	0	R/(W)*	Overflow Flag This flag indicates whether or not the compare match timer counter (CMCNT) has overflowed and been cleared to 0. Software cannot write 1 to this bit. 0: CMCNT has not overflowed [Clearing conditions] • Write 0 to OVF after reading OVF = 1 (channel 0) • Write 0 to OVF (channels 1 to 3) 1: CMCNT has overflowed

Bit	Bit Name	Initial Value	R/W	Description
13	WRFLG	0	R	Write State Flag CMCNT cannot be written to when this bit is 1. This bit indicates the period that the writing to CMCNT is masked for synchronization after the writing to CMCNT. Confirm that this flag is 0 when CMCNT is written to continuously.
12	CH0STTF (valid only in channel 0)	0	R/(W)*	Channel 0 Start Flag When RCLK-synchronous channel 0 counter start/stop mode is selected, this flag indicates whether the counter in channel 0 started on detecting an RCLK rising edge after 1 was written to the STR0 bit in CMSR. 0: Channel 0 counter has not started. [Clearing condition] Write 0 to CH0STTF. 1: Channel 0 counter has started. This bit is valid only for channel 0 when RCLK-synchronous counter start/stop mode is selected.
11	CH0STPF (valid only in channel 0)	0	R/(W)*	Channel 0 Stop Flag When RCLK-synchronous channel 0 counter start/stop mode is selected, this flag indicates whether the counter in channel 0 stopped on detecting an RCLK rising edge after 1 was written to the STR0 bit in CMSR. 0: Channel 0 counter has not stopped. [Clearing condition] Write 0 to CH0STPF. 1: Channel 0 counter has stopped. This bit is valid only for channel 0 when RCLK-synchronous counter start/stop mode is selected.

Bit	Bit Name	Initial Value	R/W	Description
10	CH0SSIE (valid only in channel 0)	0	R/W	Channel 0 Start/Stop Interrupt Enable When RCLK-synchronous channel 0 counter start/stop mode is selected, this bit enables or disables an interrupt due to the start or stop of the counter in channel 0. 0: Disables an interrupt due to start or stop of channel 0 counter. 1: Enables an interrupt due to start or stop of channel 0 counter. This bit is valid only for channel 0 when RCLK-synchronous counter start/stop mode is selected.
9	CMS	0	R/W	Compare Match Timer Counter Size This bit and CMCSRH.CMSH select whether the compare match timer counter (CMCNTH[15:0]+CMCNT[31:0]) is used as a 16-bit counter or a 32-bit counter or a 48-bit counter. This setting becomes the valid size for the compare match timer constant register (CMCORH[15:0]+CMCOR[31:0]). CMCSRH.CMSH[9]+CMCSR.CMS[9] = 1x: Operates as a 48-bit counter 00: Operates as a 32-bit counter 01: Operates as a 16-bit counter
8	CMM	0 (1 for only channel 3)	R/W	Compare Match Mode Selects one-shot operation or free-running operation of the counter. 0: One-shot operation 1: Free-running operation
7	CMTOUT_IE	0	R/W	Compare Match Standby Mode Cancel Enable (channels 1 to 3) Enables or disables the cancellation of various standby modes. This bit is reserved in channel 0,4,5. This bit is always read as 0. The write value should always be 0. 0: The cancellation of various standby modes by this CMT1 is disabled. 1: The cancellation of various standby modes by this

Bit	Bit Name	Initial Value	R/W	Description
				CMT1 is enabled.

Bit	Bit Name	Initial Value	R/W	Description
6	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
5, 4	CMR[1:0]	00	R/W	Compare Match Request These bits enable or disable a DMA transfer request or internal interrupt request in a compare match. 00: Disables a DMA transfer request or internal interrupt request 01: Enables a DMA transfer request (This setting is valid in channel 0 and prohibited in channels 1 to 5.) 10: Enables an internal interrupt request 11: Setting prohibited Note: When various standby modes are canceled by the CMT1, these bits should be set to B'10.
3	DBGIVD	1	R/W	Debug Mode Operation Select Sets the counter operation in debugging mode. 0: Stops the counter operation in debugging mode. 1: Continues the counter operation even in debugging mode.

Bit	Bit Name	Initial Value	R/W	Description
2 to 0	CKS[2:0]	100 (000 for only channel 0, and 111 for only channel 3)	R/W	Clock Select These bits and CMCSRH.CKSH select the clock input to CMCNT. When the count start bit (STRn (n = 5 to 0)) for the corresponding channel is set to 1, CMCNT begins incrementing with the clock selected by these bits. CMCSRH.CKSH[0]+CMCSR.CKS[2:0] = x000: (AP/COMMON MAIN CLOCK 1/2)/8 (This setting is valid in channel 0,4,5 and prohibited in channels 1 to 3.) x001: (AP/COMMON MAIN CLOCK 1/2)/32 (This setting is valid in channel 0,4,5 and prohibited in channels 1 to 3.) x010: (AP/COMMON MAIN CLOCK 1/2)/128 (This setting is valid in channel 0,4,5 and prohibited in channels 1 to 3.) x011: (AP/COMMON MAIN CLOCK 1/2)/1 (This setting is valid in channel 0,4,5 and prohibited in channels 1 to 3.) 0100: RCLK/8 0101: RCLK/32 0110: RCLK/128 0111: RCLK/1 (This setting is valid in channel 3 and prohibited in channels 0,1,2,4,5.) 1111: Pseudo 32KHz/1

Note: * Only 0 can be written to clear the flag.

17.2.3 Compare Match Timer Control/Status Register H0 to 5 (CMCSRH)

CMCSRH is a 16-bit register that sets the counter size and input clocks.

CMCSRH0

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	CMSH	–	–	–	–	–	–	–	–	CKSH
Initial Value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R	R/W

CMCSRH1

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	CMSH	–	–	–	–	–	–	–	–	CKSH
Initial Value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R	R/W

CMCSRH2

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	CMSH	–	–	–	–	–	–	–	–	CKSH
Initial Value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R	R/W

CMCSRH3

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	CMSH	–	–	–	–	–	–	–	–	CKSH
Initial Value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R	R/W

CMCSRH4

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	CMSH	–	–	–	–	–	–	–	–	CKSH
Initial Value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R	R/W

CMCSRH5

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	CMSH	–	–	–	–	–	–	–	–	CKSH
Initial Value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	All 0	R	Reserved This bit is always read as 0. The write value should always be 0.
9	CMSH	0	R/W	Compare Match Timer Counter Size This bit and CMCSR.CMS select whether the compare match timer counter (CMCNTH[15:0]+CMCNT[31:0]) is used as a 16-bit counter or a 32-bit counter or a 48-bit counter. This setting becomes the valid size for the compare match timer constant register (CMCORH[15:0]+CMCOR[31:0]). CMCSRH.CMSH[9]+CMCSR.CMS[9] = 1x: Operates as a 48-bit counter 00: Operates as a 32-bit counter 01: Operates as a 16-bit counter
8 to 1	—	All 0	R	Reserved This bit is always read as 0. The write value should always be 0.
0	CKSH	0	R/W	Clock Select This bit and CMCSR.CKS[2:0] select the clock input to CMCNT. When the count start bit (STRn (n = 5 to 0)) for the corresponding channel is set to 1, CMCNT begins incrementing with the clock selected by these bits. CMCSRH.CKSH[0]+CMCSR.CKS[2:0] = x000: (AP/COMMON MAIN CLOCK 1/2)/8 (This setting is valid in channel 0,4,5 and prohibited in channels 1 to 3.) x001: (AP/COMMON MAIN CLOCK 1/2)/32 (This setting is valid in channel 0,4,5 and prohibited in channels 1 to 3.) x010: (AP/COMMON MAIN CLOCK 1/2)/128 (This setting is valid in channel 0,4,5 and prohibited in channels 1 to 3.) x011: (AP/COMMON MAIN CLOCK 1/2)/1 (This setting is valid in channel 0,4,5 and prohibited in channels 1 to 3.) 0100: RCLK/8

Bit	Bit Name	Initial Value	R/W	Description
				0101: RCLK/32
				0110: RCLK/128
				0111: RCLK/1 (This setting is valid in channel 3 and prohibited in channels 0,1,2,4,5.)
				1111: Pseudo 32KHz/1

17.2.4 Compare Match Timer Counter 0 to 5 (CMCNT)

CMCNT is a 32-bit register that is used as an up-counter for each channel.

A counter operation is set by the compare match timer control/status register (CMCSR/CMCSRH). Therefore, set CMCSR/CMCSRH first, before starting operation of the channel corresponding to the compare match timer start register (CMSTR). When the 16-bit counter operation is selected by the CMCSRH.CMSH+CMCSR.CMS bits, bits 15 to 0 of this register become valid. When the register should be written to, write the data that is added H'0000 to the upper half in a 32-bit operation. The contents of this register are initialized to H'0000 0000.

Counter operation of channels 1 to 3 is enabled even when the peripheral clock is stopped. Counter operation is also enabled in a state where the core-area power supply is turned off during power control mode controlled by the SYSC. (* Counter operation of channels 0,4,5 also is enabled only when the counter is operated by RCLK(pseudo32KHz also includes).

17.2.5 Compare Match Timer Counter H0 to 5 (CMCNTH)

CMCNTH is a 16-bit register that is used as an up-counter for each channel.

A counter operation is set by the compare match timer control/status register (CMCSR/CMCSRH). Therefore, set CMCSR/CMCSRH first, before starting operation of the channel corresponding to the compare match timer start register (CMSTR). When the 48-bit counter operation is selected by the CMCSRH.CMSH+CMCSR.CMS bits, bits 15 to 0 of this register become valid as the upper 16-bit of 48-bit counter. The value written to this register is reflected at the same time the register CMCNT is written. Therefore, write to this register first, before writing to CMCNT. The value is not reflected even if it writes only to this register. The contents of this register are initialized to H'0000.

Counter operation of channels 1 to 3 is enabled even when the peripheral clock is stopped. Counter operation is also enabled in a state where the core-area power supply is turned off during power control mode controlled by the SYSC.(* Counter operation of channels 0,4,5 also is enabled only when the counter is operated by RCLK(pseudo32KHz also includes).

17.2.6 Compare Match Timer Constant Register 0 to 5 (CMCOR)

CMCOR is a 32-bit register that sets the compare match period with CMCNT for each channel.

When the 16-bit counter operation is selected by the CMCSRH.CMSH+CMCSR.CMS bits, bits 15 to 0 of this register become valid. When the register should be written to, write the data that is added H'0000 to the upper half in a 32-bit operation.

An overflow is detected when CMCNT is cleared to 0 and this register is H'FFFF FFFF(when the 16-bit counter operation it is H’0000 FFFF). The contents of this register are initialized to H'FFFF FFFF.

17.2.7 Compare Match Timer Constant Register H0 to 5 (CMCORH)

CMCORH is a 16-bit register that sets the compare match period with CMCNTH for each channel.

When the 48-bit counter operation is selected by the CMCSRH.CMSH+CMCSR.CMS bits, bits 15 to 0 of this register become valid as the upper 16-bit of 48-bit counter.

An overflow is detected when CMCNTH is cleared to 0 and this register is H'FFFF. The contents of this register are initialized to H'FFFF.

17.2.8 Compare Match Timer Counter 3 Backup 0 (CMCNT3BK0)

CMCNT3BK0 is a 32-bit register that stores a copy of the CMCNT3 value immediately after the counter in channel 0 stops in RCLK-synchronous channel 0 counter start/stop mode.

17.2.9 Compare Match Timer Counter 3 Backup 1 (CMCNT3BK1)

CMCNT3BK1 is a 32-bit register that stores a copy of the CMCNT3 value immediately after the counter in channel 0 starts in RCLK-synchronous channel 0 counter start/stop mode.

17.2.10 Compare Match Timer Match Control/Status Register (CMCSRM)

CMCSRM is a 16-bit register that resets to Compare match timer match counter, and sets the counter start/halt. This register is only for channel 0 and 3.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WRFLG	–	–	–	–	–	–	–	–	–	–	–	–	–	CMPCLR	CMP START
Initial Value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	WRFLG	0	R	Write state flag. When this Bit is 1, CMCNTM can not be cleared. After CMCNTM is cleared, this Bit become 1 for a while(*) as purpose of synchronization. Needs to confirm this flag is 0 or wait the period enough when continuously clearing. *In the maximum, "Counter input clock 5 cycle + CPCLK 3 cycle" ・Counter input clock CMCSR.CKS2=0: AP/common main clock 1/2 CMCSR.CKS2=1: RCLK
14 to 2	—	All 0	R	Reserved This bit is always read as 0. The write value should always be 0.
1	CMPCLR	0	R/W	Counter Clear [When writing] 0: No operation 1: CMCNTM becomes 0 (And CMCSRM.WRFLG will get high 1'b1.) When CMPCLR and CMPSTART are written 1 at the same time, the counter starts after clearing the counter. [When reading] This bit is always read as 0.
0	CMPSTART	0	R/W	Count Start This bit select whether to operate or halt the compare match timer match counter (CMCNTM) of each channel. 0: Halts CMCNTM count 1: Starts CMCNTM count

17.2.11 Compare Match Timer Match Counter (CMCNTM)

CMCNTM is a 32-bit register that is used as an up-counter. This register is only for channel 0 and 3.

A counter operation is set by the compare match timer match control/status register (CMCSRM). After the counter CMCNT starts, this counter increases whenever at a compare match.

17.3 Operation

17.3.1 Counter Operation

The CMT1 starts the operation of the counter by writing B'1 to the STRn (n = 5 to 0) bit in CMSTR after each register has been set. Complete all of the settings before starting the operation. Do not change the register settings other than clearing flag bits during the compare match timer (CMCNT) operation.

The counter operates in one of two ways.

- One-Shot Operation

  One-shot operation is selected by setting the CMM bit in CMCSR to B'0. When the value in CMCNT matches the value in CMCOR, the value in CMCNT is cleared to H'0000 0000 and the CMF bit in CMCSR is set to B'1. Counting by CMCNT stops after it has been cleared.

  To detect an overflow interrupt, set the value in CMCOR to H'FFFF FFFF. When the value in CMCNT matches the value in CMCOR, CMCNT is cleared to H'0000 0000 and the CMF and OVF bits in CMCSR are set to B'1.

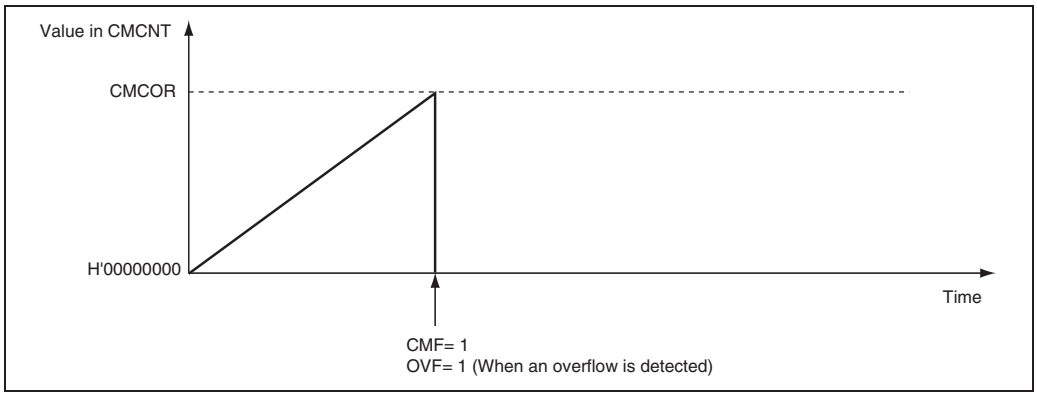


Figure 17.2 Counter Operation (One-Shot Operation)

- Free-Running Operation

  Free-running operation is selected by setting the CMM bit in CMCSR to B'1. When the value in CMCNT matches the value in CMCOR, CMCNT is cleared to H'0000 0000 and the CMF bit in CMCSR is set to B'1. CMCNT resumes counting-up after it has been cleared.

To detect an overflow interrupt, set CMCOR to H'FFFF FFFF. When the values in CMCNT and CMCOR match, CMCNT is cleared to H'0000 0000 and the CMF and OVF bits in CMCSR are set to B'1.

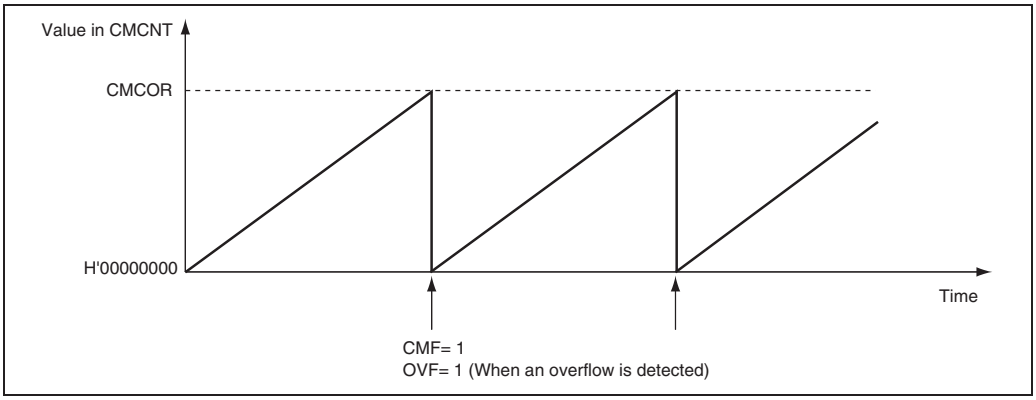


Figure 17.3 Counter Operation (Free-Running Operation)

17.3.2 Counter Size

In this module, the size of the counter is selectable as either 16 or 32 or 48 bits. This is selected by the CMS bit in CMCSR and CMSH bit in CMCSRH.

When the 16-bit/32-bit size is selected, it ignores the upper 32 bits/16 bits of CMCOR. To detect an overflow interrupt, the value 1 must be set to valid bits of CMCOR.
(ex. H’00000000FFFF, H’0000FFFFFFFF)

17.3.3 Timing for Counting by CMCNT

In this module, the clock for the counter can be selected from among the following:

Channels 0,4,5: (AP/COMMON MAIN CLOCK 1/2) clock: 1/8, 1/32, 1/128, and 1/1
External clock (RCLK): 1/8, 1/32, and 1/128
External clock (Pseudo32KHz): 1/1

Channels 1 to 2: External clock (RCLK): 1/8, 1/32, and 1/128
External clock (Pseudo32KHz): 1/1

Channel 3: External clock (RCLK): 1/1, 1/8, 1/32, and 1/128
External clock (Pseudo32KHz): 1/1

The clock for the counter is selected by the CKS bits in CMCSR and CKSH bit in CMCSRH. CMCNT is incremented at the rising edge of the selected clock.

17.3.4 DMA Transfer Request and Internal Interrupt Request to CPU

The setting of CMR bits in CMCSR for a DMA transfer request (this setting is only valid for channel 0) or the sending of an internal interrupt request (valid for all channels) to the CPU at a compare match.

When a DMA transfer request occurs, the request is continuously issued until the number of transfers set in the DMAC has been finished and output of the request is automatically halted on completion of the specified transfer count.

To clear the internal interrupt request to the CPU, the CMF bit should be set to B'0. Set the CMF bit to 0 in the handling routine for the CMT1 interrupt.

17.3.5 Operation of Channels 0 to 5 in power control mode

As CMCNT of channels 0 to 5 can be operated only by the RCLK(Pseudo32KHz), it continues the counter operation even when this LSI makes the transition to power control mode controlled by the SYSC and the core-area power supply is turned off after the necessary register settings have been made and B'1 has been written to the STRn (n = 5 to 0) bit in CMSTR.

- Register Access
  The counters for channels 0 to 5 are located in the sub-area because the counters have to be able to count-up even when this LSI is in power control mode controlled by the SYSC. The registers that are needed for the counter's operation are set from the core area. The following restrictions thus apply to the modification of the registers.

After the following registers have been modified, do not make the transition to power control mode controlled by the SYSC until you are sure that, according to the restrictions given below, the result of the modification has been reflected in the LSI's actual operation. Otherwise, the modification may not be reflected in an actual result.

- CMCSR: Bits CH0SSIE(ch0), CMS, CMM, CMTOUT_IE(ch1,2,3), CMR[1:0], DBGIVD, CKS[2:0]
- CMCOR: Bits 48 to 0
- CMSTR: Bit STR0RS, STRn (n = 5 to 0)
- CMCSRM: Bit CMPCLR, CMPSTART

Two RCLK cycles are necessary before this register is either read or any modification of the value it holds is reflected in the LSI's actual operation.

- CMCNT: Bits 48 to 0

Two RCLK cycles are necessary before this register is either read or any modification of the value it holds is reflected in the LSI's actual operation. Writing to this register, once started, is protected from further write operations until the writing operation has been completed.

- Cancellation of Various Standby Modes

  When an interrupt among channels 1 to 3 occurs while the system is in standby mode or power control mode controlled by the SYSC, various standby modes can be canceled if the CMTOUT_IE bit in CMCSR1 to CMCSR3 is set to B'1 and the CMR bits to B'10.

  Set the CMF bit in CMCSR1 to CMCSR3 to B'0 after various standby modes are canceled.

17.3.6 Compare Match Flag Set Timing

The CMF bit in CMCSR is set to 1 by the compare match signal generated when CMCOR and CMCNT match. The compare match signal is generated upon the final state of the match (timing at which the CMCNT value is updated to H'0). Consequently, after CMCOR and CMCNT match, a compare match signal will not be generated until a CMCNT counter clock is input. Figure 17.4 shows the set timing of the CMF bit.

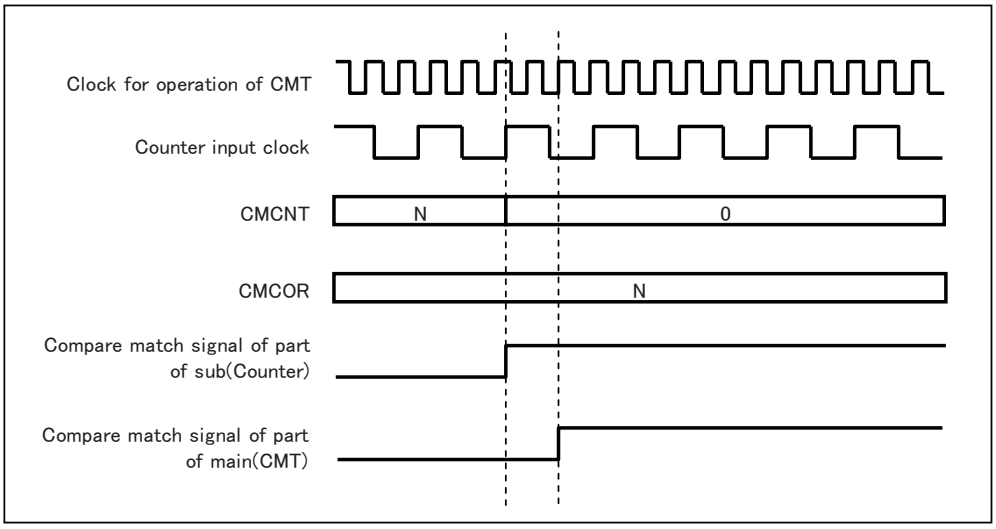


Figure 17.4 CMF Set Timing

17.3.7 RCLK-Synchronous Counter Start/Stop Mode in Channel 0

The CMT1 provides the RCLK-synchronous counter start/stop mode in channel 0, in which channels 0 and 3 can be used together for time measurement.

Figure 17.5 shows a flow chart for preparation.

Figure 17.6 shows a flow chart for starting measurement.

Figure 17.7 shows a flow chart for stopping measurement.

Figure 17.8 shows a timing chart when measurement starts.

Figure 17.9 shows a timing chart when measurement stops.

Figure 17.10 shows how to calculate the time measured by the counters.

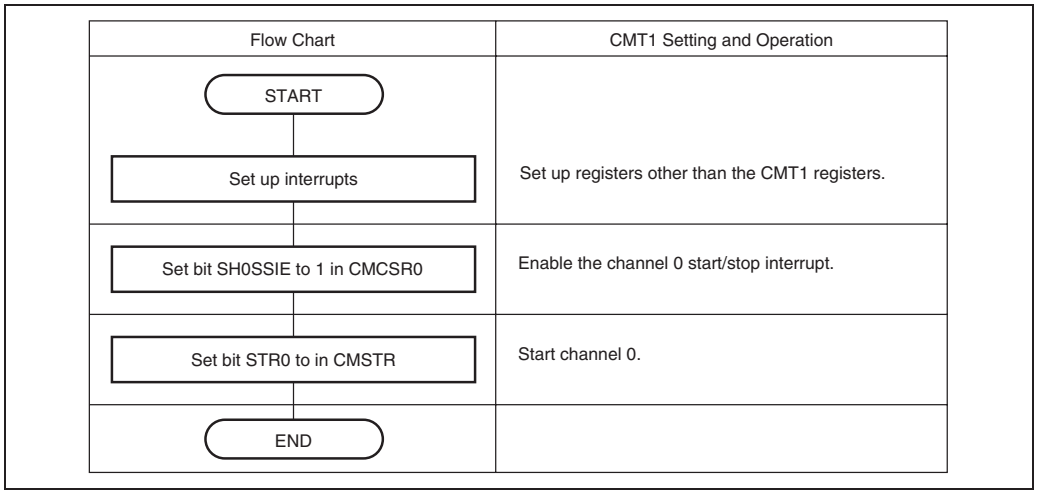


Figure 17.5 Flow Chart for Preparation

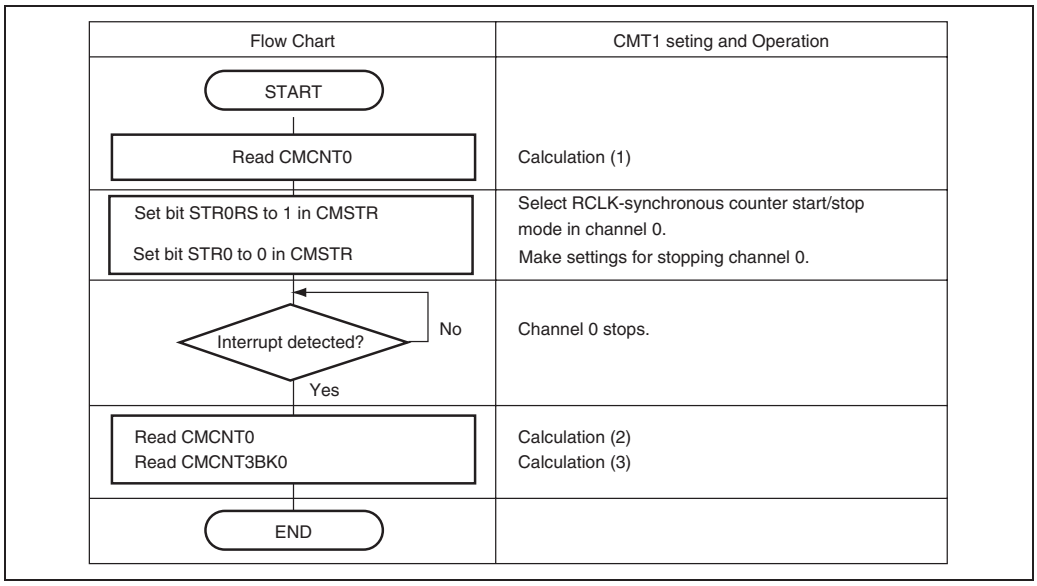


Figure 17.6 Flow Chart for Starting Measurement

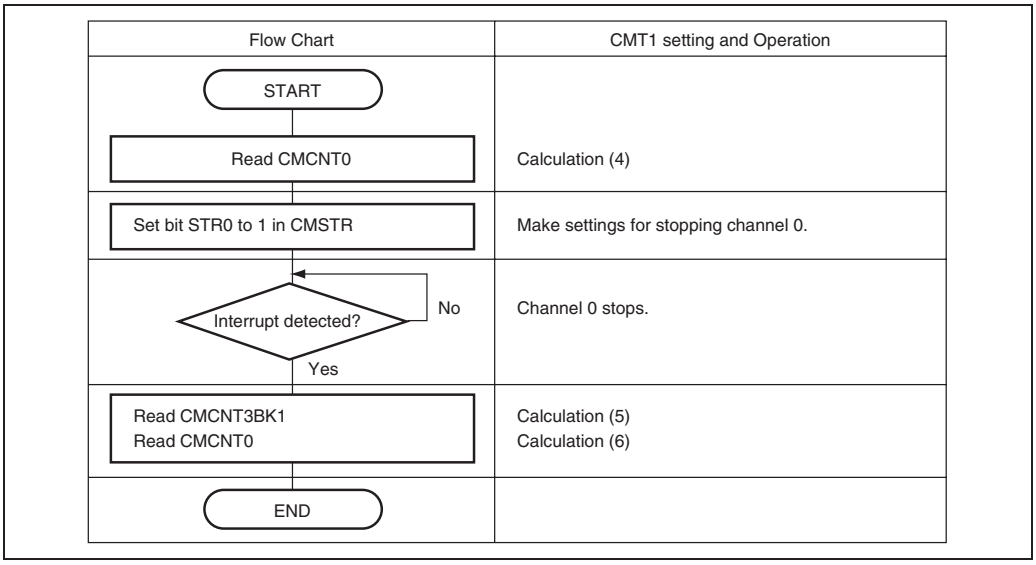


Figure 17.7 Flow Chart for Stopping Measurement

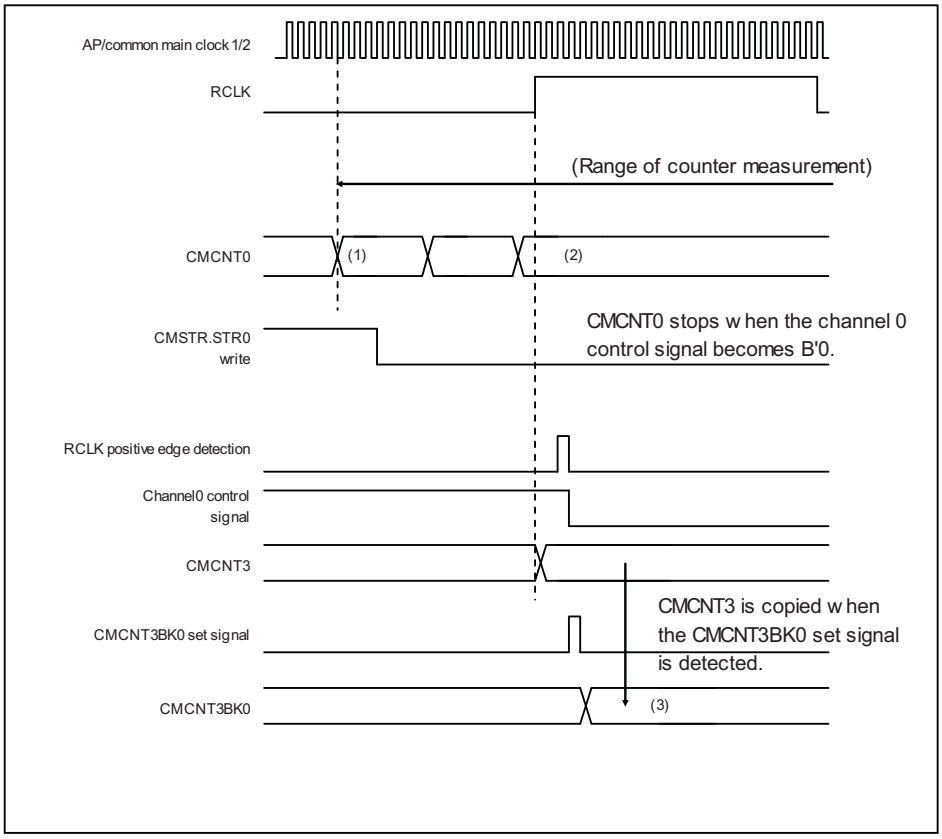


Figure 17.8 Timing Chart When Measurement Starts

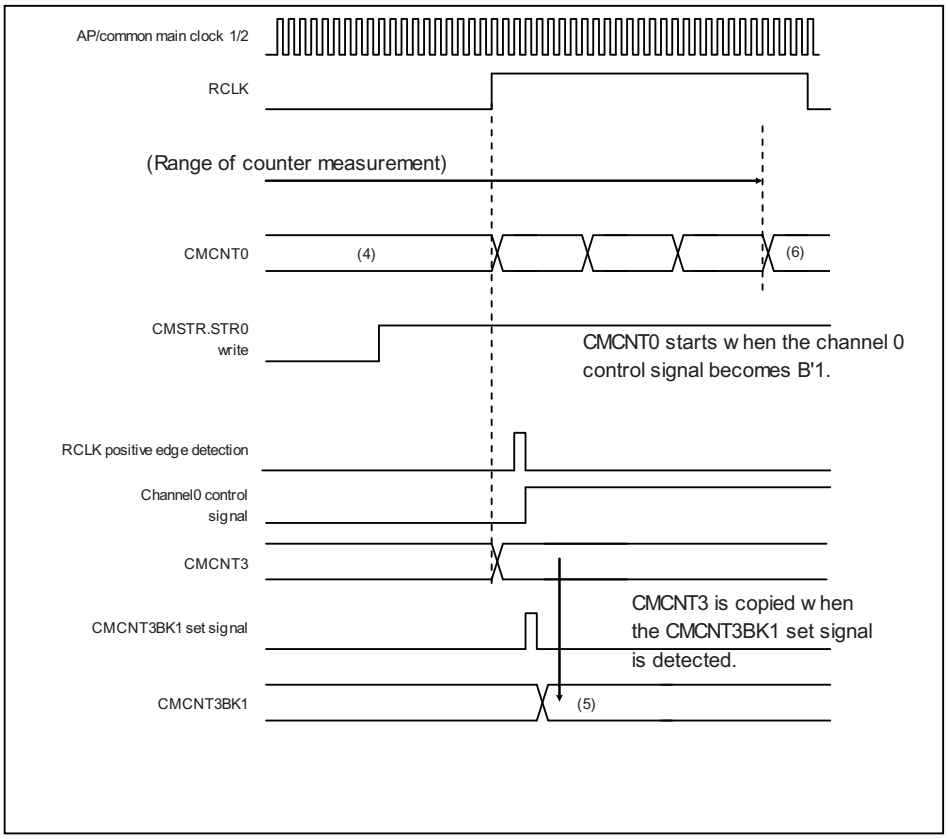


Figure 17.9 Timing Chart When Measurement Stops

$$(((2)-(1))+((6)-(4)-1)) \times Tapc+((5)-(3)) \times Tr$$

Tapc : Cycle of AP/common main clock 1/2

Tr : Cycle of RCLK

Figure 17.10 Calculation of Time Measured by Counters

Section 18 Compare Match Timer 2 (CMT2)

This LSI includes a 32-bit compare match timer (CMT2) of one channel.

18.1 Features

- One channel installed in the common domain
- 16 bits/32 bits can be selected.
- Provided with an auto-reload up counter.
- Provided with 32-bit constant registers and 32-bit up counters that can be written or read at any time.
- The CMT2 can perform counting even if this LSI is in power control mode controlled by the SYSC.
- Allows selection among four counter input clocks:
  - External clock (RCLK) input: 1/1, 1/8, 1/32, and 1/128
- One-shot operation and free-running operation are selectable.
- Allows selection of compare match or overflow for the interrupt source.
- Supports the cancel of the standby state in power control mode controlled by the SYSC.
- Module standby mode can be set.
- Allows selection of counter operation/stop during debugging with the debug mode operation selector.

Figure 18.1 shows a block diagram of the CMT2.

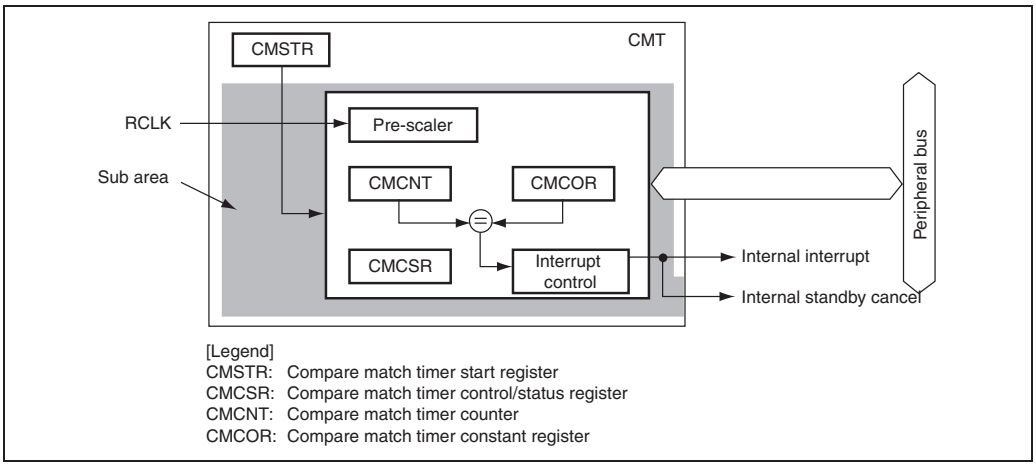


Figure 18.1 Block Diagram of CMT2

18.2 Register Descriptions

Table 18.1 shows the CMT2 register configuration. Table 18.2 shows the register states in each operating mode.

Table 18.1 Register Configuration

Register Name	Abbreviation	R/W	Address		Access Size
			Regular	Shadow	
Compare match timer start register	CM2STR	R/W	H'E613 0000	H'E713 0000	16
			H'E613 4000	H'E713 4000	
Compare match timer control/status register	CM2CSR	R/W	H'E613 0040	H'E713 0040	16
			H'E613 4040	H'E713 4040	
Compare match timer counter	CM2CNT	R/W	H'E613 0044	H'E713 0044	32
			H'E613 4044	H'E713 4044	
Compare match timer constant register	CM2COR	R/W	H'E613 0048	H'E713 0048	32
			H'E613 4048	H'E713 4048	

Note: * Accessing to H'E6130XXX, H'E7130XXX is off the subject of HPB semaphore.
Accessing to H'E6134XXX, H'E7134XXX is a subject of HPB semaphore.

Table 18.2 Register States in Each Operating Mode

Register Abbreviation	Reset *	Module Standby
CM2STR	Initialized	Retained
CM2CSR	Initialized	Retained
CM2CNT	Initialized	Retained
CM2COR	Initialized	Retained

Note: * For details, refer to section 1-D Overview of reset.

18.2.1 Compare Match Timer Start Register (CM2STR)

CM2STR is a 16-bit register that selects whether the compare match timer counter (CM2CNT) is operated or halted.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	STR5	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	STR5	1	R/W	Count Start Selects whether to operate or halt the compare match timer counter (CM2CNT). 0: Halts CM2CNT count. 1: Starts CM2CNT count.
4 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

18.2.2 Compare Match Timer Control/Status Register (CM2CSR)

CM2CSR is a 16-bit register that indicates the occurrence of compare matches, enables interrupts, and sets the counter input clocks.

Do not change bits other than the CMF and OVF bits during the compare match timer counter (CM2CNT) operation.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMF	OVF	WR FLG	—	—	—	CMS	CMM	CMTOUT_IE	—	CMR[1:0]		DBG IVD	CKS[2:0]		
Initial value:	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	1
R/W:	R/(W)*	R/(W)*	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	CMF	0	R/(W)*	Compare Match Flag This flag indicates whether or not values of the compare match timer counter (CM2CNT) and compare match timer constant register (CM2COR) have matched. Software cannot write 1 to the bit. When one-shot is selected for the counter operation, counting resumes by clearing this bit. 0: CM2CNT and CM2COR values have not matched. [Clearing condition] • Write 0 to CMF 1: CM2CNT and CM2COR values have matched.
14	OVF	0	R/(W)*	Overflow Flag This flag indicates whether or not the compare match timer counter (CM2CNT) has overflowed and been cleared to 0. Software cannot write 1 to this bit. 0: CM2CNT has not overflowed. [Clearing condition] • Write 0 to OVF 1: CM2CNT has overflowed.

Bit	Bit Name	Initial Value	R/W	Description
13	WRFLG	0	R	Write State Flag CM2CNT cannot be written to when this bit is 1. This bit indicates the period that the writing to CM2CNT is masked for synchronization after the writing to CM2CNT. Confirm that this flag is 0 when CM2CNT is written to continuously.
12 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	CMS	0	R/W	Compare Match Timer Counter Size Selects whether the compare match timer counter (CM2CNT) is used as a 16-bit counter or a 32-bit counter. This setting becomes the valid size for the compare match timer constant register (CM2COR). 0: Operates as a 32-bit counter. 1: Operates as a 16-bit counter.
8	CMM	1	R/W	Compare Match Mode Selects one-shot operation or free-running operation of the counter. 0: One-shot operation 1: Free-running operation
7	CMTOUT_IE	0	R/W	Compare Match Standby Mode Cancel Enable Enables or disables the cancel of various standby modes. 0: The cancel of various standby modes by this CMT2 is disabled. 1: The cancel of various standby modes by this CMT2 is enabled.
6	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
5, 4	CMR[1:0]	00	R/W	Compare Match Request These bits enable or disable an internal interrupt request in a compare match. 00: Disables an internal interrupt request. 01: Setting prohibited 10: Enables an internal interrupt request. 11: Setting prohibited Note: When various standby modes are canceled by the CMT2, these bits should be set to B'10.
3	DBGIVD	1	R/W	Debug Mode Operation Select Sets the counter operation in debug mode. 0: Stops the counter operation in debug mode. 1: Enables the counter operation even in debug mode.
2 to 0	CKS[2:0]	111	R/W	Clock Select These bits select the clock input to CM2CNT. When the count start bit (STR5) in CM2STR is set to 1, CM2CNT begins incrementing with the clock selected by these bits. 000: Setting prohibited 001: Setting prohibited 010: Setting prohibited 011: Setting prohibited 100: RCLK/8 101: RCLK/32 110: RCLK/128 111: RCLK/1

Note: * Only 0 can be written to clear the flag.

18.2.3 Compare Match Timer Counter (CM2CNT)

CM2CNT is a 32-bit register that is used as an up-counter.

A counter operation is set by the compare match timer control/status register (CM2CSR). Therefore, set CM2CSR first, before starting a channel operation corresponding to the compare match timer start register (CM2STR). When the 16-bit counter operation is selected by the CMS bit, bits 15 to 0 of this register become valid. When the register should be written to, write the data that is added H'0000 to the upper half in a 32-bit operation. The contents of this register are initialized to H'00000000.

Counter operation of CMT2 is enabled even when the peripheral clock is stopped. Counter operation is also enabled in a state where the core-area power supply is turned off during power control mode controlled by the SYSC.

When CM2CNT is going to be read during the counter operation, the value that is read out may be wrong because of an asynchronous clock. Read several times with software and compare the read-out values.

18.2.4 Compare Match Timer Constant Register (CM2COR)

CM2COR is a 32-bit register that sets the compare match period with CM2CNT.

When the 16-bit counter operation is selected by the CMS bit in CM2CSR, bits 15 to 0 of this register become valid. When the register should be written to, write the data that is added H'0000 to the upper half in a 32-bit operation.

An overflow is detected when CM2CNT is cleared to 0 and this register is H'FFFFFFFF. The contents of this register are initialized to H'FFFFFFFF.

18.3 Operation

18.3.1 Counter Operation

The CMT2 starts the operation of the counter by writing B'1 to the STR5 bit in CM2STR after each register has been set. Complete all of the settings before starting the operation. Do not change the register settings other than clearing flag bits during the compare match timer (CM2CNT) operation.

The counter operates in one of two ways.

- One-Shot Operation

  One-shot operation is selected by setting the CMM bit in CM2CSR to B'0. When the value in CM2CNT matches the value in CM2COR, the value in CM2CNT is cleared to H'00000000 and the CMF bit in CM2CSR is set to B'1. Counting by CM2CNT stops after it has been cleared.

  To detect an overflow interrupt, set the value in CM2COR to H'FFFFFFFF. When the value in CM2CNT matches the value in CM2COR, CM2CNT is cleared to H'00000000 and the CMF and OVF bits in CM2CSR are set to B'1.

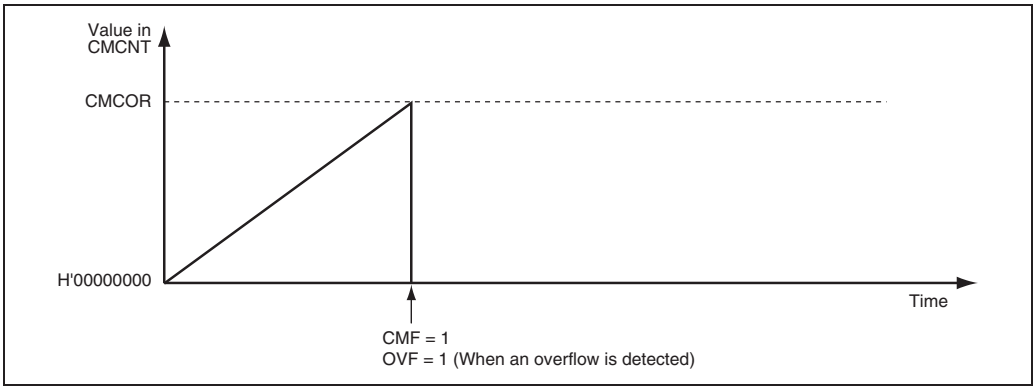


Figure 18.2 Counter Operation (One-Shot Operation)

- Free-Running Operation

  Free-running operation is selected by setting the CMM bit in CM2CSR to B'1. When the value in CM2CNT matches the value in CM2COR, CM2CNT is cleared to H'00000000 and the CMF bit in CM2CSR is set to B'1. CM2CNT resumes counting-up after it has been cleared.

To detect an overflow interrupt, set CM2COR to H'FFFFFFFF. When the values in CM2CNT and CM2COR match, CM2CNT is cleared to H'00000000 and the CMF and OVF bits in CM2CSR are set to B'1.

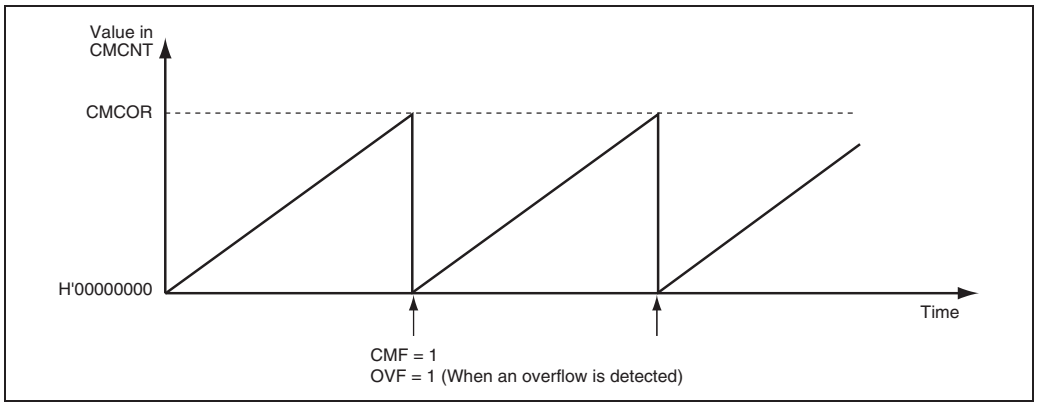


Figure 18.3 Counter Operation (Free-Running Operation)

18.3.2 Counter Size

In this module, the size of the counter is selectable as either 16 or 32 bits. This is selected by the CMS bit in CM2CSR.

When the 16-bit size is selected, use a 32-bit value which has H'0000 as its upper half to set CM2COR. To detect an overflow interrupt, CM2COR must be set to H'0000FFFF.

18.3.3 Timing for Counting by CM2CNT

In this module, the clock for the counter can be selected from among the following:

- External clock (RCLK): 1/1, 1/8, 1/32, and 1/128

The clock for the counter is selected by the CKS bits in CM2CSR. CM2CNT is incremented at the rising edge of the selected clock.

18.3.4 Internal Interrupt Request to CPU

The setting of the CMR bits in CM2CSR selects the sending of an internal interrupt request to the CPU at a compare match.

To clear the internal interrupt request to the CPU, the CMF bit should be set to B'0. Set the CMF bit to 0 in the handling routine for the CMT2 interrupt.

18.3.5 CMT2 Operation

As CM2CNT can be operated only by the RCLK, it continues the counter operation even when this LSI makes the transition to power control mode controlled by the SYSC and the core-area power supply is turned off after the necessary register settings have been made and B'1 has been written to the STR5 bit in CM2STR.

- Register Access

  The counter for the CMT2 is located in the sub area because the counter has to be able to count-up even when this LSI is in power control mode controlled by the SYSC. The registers that are needed for the counter's operation are set from the core area. The following restrictions thus apply to the modification of the registers.

After the following registers have been modified, do not make the transition to power control mode controlled by the SYSC until you are sure that, according to the restrictions given below, the result of the modification has been reflected in the LSI's actual operation. Otherwise, the modification may not be reflected in an actual result.

- CM2CSR: Bits CKS, CMM, CMS, and CMTOUT_IE
- CM2COR: Bits 31 to 0
- CM2STR: Bit STR5

Two RCLK cycles are necessary before this register is either read or any modification of the value it holds is reflected in the LSI's actual operation.

- CM2CNT: Bits 31 to 0

Two RCLK cycles are necessary before this register is either read or any modification of the value it holds is reflected in the LSI's actual operation. Writing to this register, once started, is protected from further write operations until the writing operation has been completed.

- Cancel of Various Standby Modes

  When an interrupt occurs while the system is in standby mode or power control mode controlled by the SYSC, various standby modes can be canceled if the CMTOUT_IE bit in CM2CSR is set to B'1 and the CMR bits to B'10.

  Set the CMF bit in CM2CSR to B'0 after various standby modes are canceled.

18.3.6 Compare Match Flag Set Timing

The CMF bit in CM2CSR is set to 1 by the compare match signal generated when CM2COR and CM2CNT match. The compare match signal is generated upon the final state of the match (timing at which the CM2CNT value is updated to H'0). Consequently, after CM2COR and CM2CNT match, a compare match signal will not be generated until a CM2CNT counter clock is input. Figure 18.4 shows the set timing of the CMF bit.

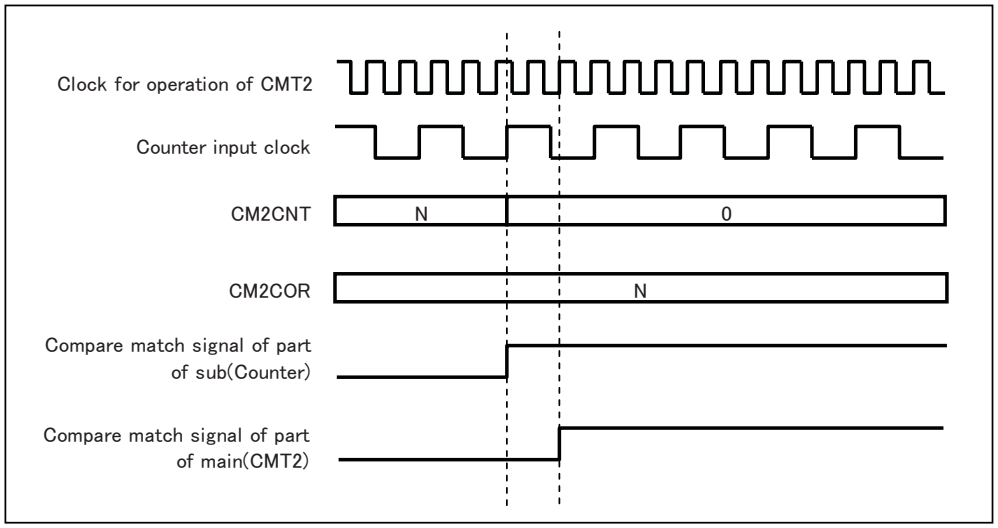


Figure 18.4 CMF Set Timing

Section 19 Compare Match Timer 3 (CMT3)

[Note: The CMT3 is reserved for use with TrustZone software. Do not use the CMT3 with other software.]

This LSI includes a 32-bit compare match timer (CMT3) of one channel.

19.1 Features

- One channel installed in the common domain
- 16 bits/32 bits can be selected.
- Provided with an auto-reload up-counter.
- Provided with 32-bit constant registers and 32-bit up-counters that can be written or read at any time.
- The CMT3 can perform counting even if this LSI is in power control mode controlled by the SYSC.
- Allows selection among four counter input clocks
  - External clock (RCLK) input: 1/1, 1/8, 1/32, and 1/128
- One-shot operation and free-running operation are selectable.
- Allows selection of compare match or overflow for the interrupt source.
- Module standby mode can be set.
- Counter operation ON/OFF function in debug mode.

Figure 19.1 shows a block diagram of the CMT3.

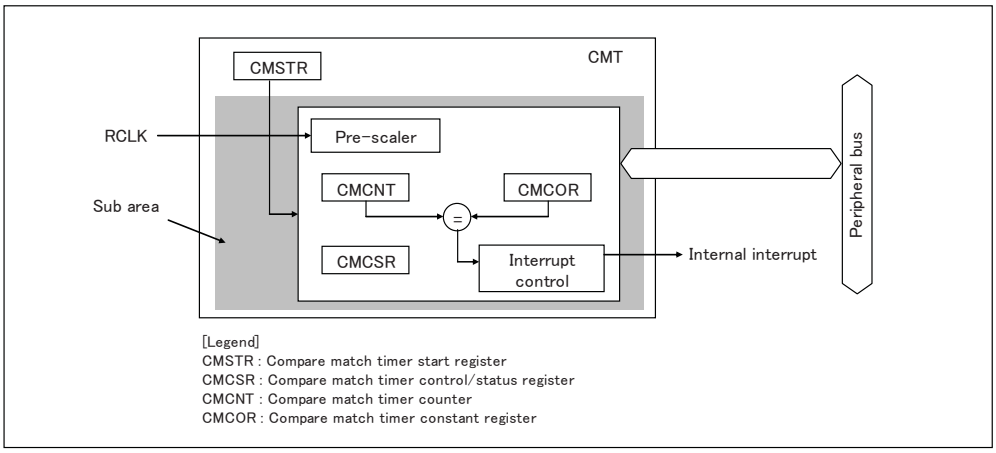


Figure 19.1 Block Diagram of CMT3

19.2 Register Descriptions

Table 19.1 shows the CMT3 register configuration. Table 19.2 shows the register states in each operating mode.

Table 19.1 Register Configuration

Register Name	Abbreviation	R/W	Address		Access Size
			Regular	Shadow	
Compare match timer start register	CM3STR	R/W	H'E614 0000	H'E714 0000	16
Compare match timer control/status register	CM3CSR	R/W	H'E614 0040	H'E714 0040	16
Compare match timer counter	CM3CNT	R/W	H'E614 0044	H'E714 0044	32
Compare match timer constant register	CM3COR	R/W	H'E614 0048	H'E714 0048	32

Table 19.2 Register States in Each Operating Mode

Register Abbreviation	Reset *	Module Standby
CM3STR	Initialized	Retained
CM3CSR	Initialized	Retained
CM3CNT	Initialized	Retained
CM3COR	Initialized	Retained

Note: * For details, refer to section 1-D Overview of reset.

19.2.1 Compare Match Timer Start Register (CM3STR)

CM3STR is a 16-bit register that selects whether the compare match timer counter (CM3CNT) is operated or halted.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	STR5	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	STR5	1	R/W	Count Start Selects whether to operate or halt the compare match timer counter (CM3CNT). 0: Halts CM3CNT count. 1: Starts CM3CNT count.
4 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

19.2.2 Compare Match Timer Control/Status Register (CM3CSR)

CM3CSR is a 16-bit register that indicates the occurrence of compare matches, enables interrupts, and sets the counter input clocks.

Do not change bits other than the CMF and OVF bits during the compare match timer counter (CM3CNT) operation.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMF	OVF	WRFLG	–	–	–	CMS	CMM	–	–	CMR[1:0]		DBG IVD	CKS[2:0]		
Initial Value:	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	1
R/W:	R/(W)*	R/(W)*	R	R	R	R	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	CMF	0	R/(W)*	Compare Match Flag This flag indicates whether or not the values of the compare match timer counter (CM3CNT) and the compare match timer constant register (CM3COR) have matched. Software cannot write 1 to the bit. When one-shot is selected for the counter operation, counting resumes by clearing this bit. 0: CM3CNT and CM3COR values have not matched. [Clearing condition] ● Write 0 to CMF 1: CM3CNT and CM3COR values have matched.
14	OVF	0	R/(W)*	Overflow Flag This flag indicates whether or not the compare match timer counter (CM3CNT) has overflowed and been cleared to 0. Software cannot write 1 to this bit. 0: CM3CNT has not overflowed. [Clearing condition] ● Write 0 to OVF 1: CM3CNT has overflowed.

Bit	Bit Name	Initial Value	R/W	Description
13	WRFLG	0	R	Write State Flag CM3CNT cannot be written to when this bit is 1. This bit indicates the period that the writing to CM3CNT is masked for synchornization after the writing to CM3CNT. Confirm that this flag is 0 when CM3CNT is written to continuously.
12 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	CMS	0	R/W	Compare Match Timer Counter Size This bit selects whether the compare match timer counter (CM3CNT) is used as a 16-bit counter or 32-bit counter. This register setting becomes the valid bit-size for the compare match timer constant register (CM3COR). 0: Operates as a 32-bit counter. 1: Operates as a 16-bit counter.
8	CMM	1	R/W	Compare Match Mode This bit selects one-shot operation or free-running operation of the counter. 0: One-shot operation 1: Free-running operation
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
5, 4	CMR[1:0]	00	R/W	Compare Match Request These bits enable or disable an internal interrupt request at a compare match. 00: Disables an internal interrupt request. 01: Setting prohibited 10: Enables an internal interrupt request. 11: Setting prohibited These bits are backed up.
3	DBGIVD	1	R/W	Debug Mode Operation Select This bit sets counter operation when in debug mode. 0: Stops counter operation when in debug mode. 1: Enables counter operation even when in debug mode.
2 to 0	CKS[2:0]	111	R/W	Clock Select These bits select the clock input to CM3CNT. When the count start bit (STR5) in CM3STR is set to 1, CM3CNT begins incrementing with the clock selected by these bits. 000: Setting prohibited 001: Setting prohibited 010: Setting prohibited 011: Setting prohibited 100: RCLK/8 101: RCLK/32 110: RCLK/128 111: RCLK/1

Note: * Only 0 can be written, for flag clearing.

19.2.3 Compare Match Timer Counter (CM3CNT)

CM3CNT is a 32-bit register that is used as an up-counter.

A counter operation is set by the compare match timer control/status register (CM3CSR). Therefore, set CM3CSR first, before starting a channel operation corresponding to the compare match timer start register (CM3STR). When the 16-bit counter operation is selected by the CMS bit, bits 15 to 0 of this register become valid. When the register should be written to, write the data to which H'0000 has been added to the upper half in a 32-bit operation. The contents of this register are initialized to H'00000000.

Counter operation of the CMT3 is enabled even when the peripheral clock is stopped. Counter operation is also enabled in a state where the core-area power supply is turned off during power control mode controlled by the SYSC.

When CM3CNT is going to be read during the counter operation, the value that is read out may be wrong because of an asynchronous clock. Read several times with software and compare the readout values.

19.2.4 Compare Match Timer Constant Register (CM3COR)

CM3COR is a 32-bit register that sets the compare match period with the compare match timer counter (CM3CNT).

When the 16-bit counter operation is selected by the CMS bit in the compare match timer control/status register (CM3CSR), bits 15 to 0 of this register become valid. When the register should be written to, write the data to which H'0000 has been added to the upper half in a 32-bit operation.

An overflow is detected when CM3CNT is cleared to 0 and this register is set to H'FFFFFFFF. The contents of this register are initialized to H'FFFFFFFF.

19.3 Operation

19.3.1 Counter Operation

The CMT3 starts the operation of the counter by writing B'1 to the STR5 bit in CM3STR after each register has been set. Complete all of the settings before starting the operation. Do not change the register settings other than by clearing flag bits during the compare match timer (CM3CNT) operation.

The counter operates in one of two ways.

- One-Shot Operation

  One-shot operation is selected by setting the CMM bit in CM3CSR to B'0. When the value in CM3CNT matches the value in CM3COR, the value in CM3CNT is cleared to H'00000000, and the CMF bit in CM3CSR is set to B'1. Counting by CM3CNT stops after it has been cleared.

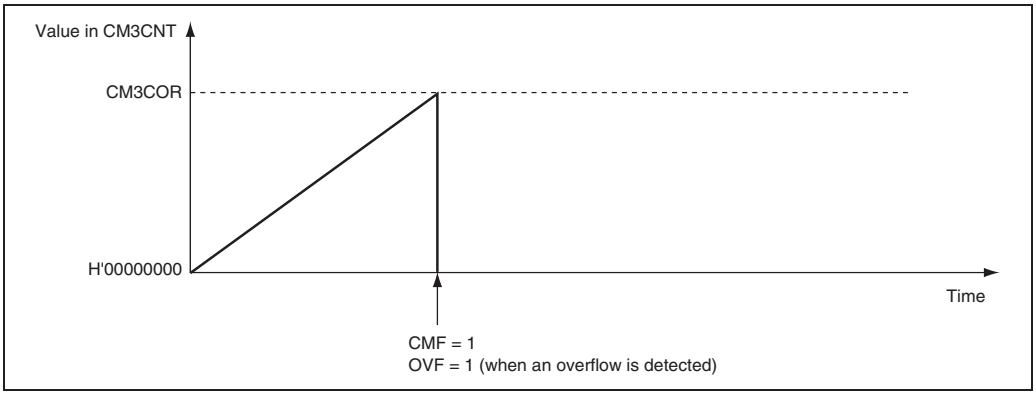


Figure 19.2 Counter Operation (One-Shot Operation)

- Free-Running Operation

  Free-running operation is selected by setting the CMM bit in CM3CSR to B'1. When the value in CM3CNT matches the value in CM3COR, CM3CNT is cleared to H'00000000 and the CMF bit in CM3CSR is set to B'1. CM3CNT resumes counting-up after it has been cleared.

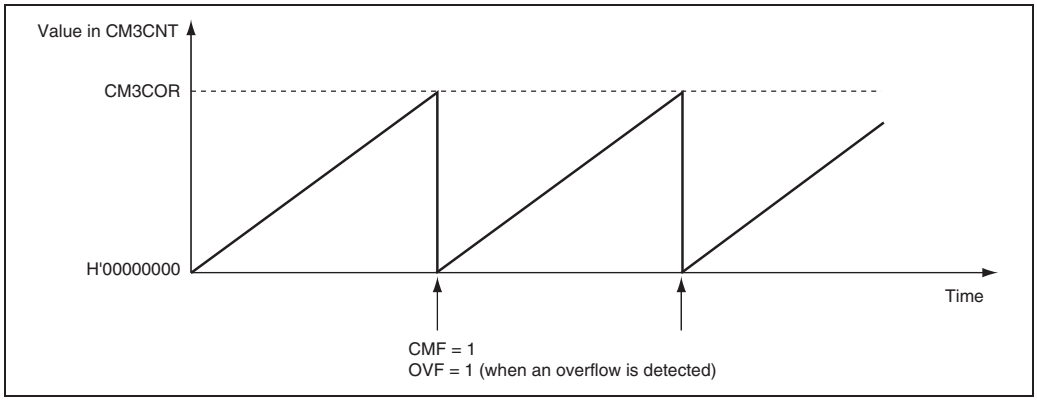


Figure 19.3 Counter Operation (Free-Running Operation)

19.3.2 Counter Size

In this module, the size of the counter is selectable as either 16 or 32 bits. This is selected by the CMS bit in CM3CSR.

When the 16-bit size is selected, use a 32-bit value which has H'0000 as its upper half to set CM3COR. To detect an overflow interrupt, CM3COR must be set to H'0000FFFF.

19.3.3 Timing for Counting by CM3CNT

In this module, the clock for the CM3CNT counter can be selected from among the following:

- External clock (RCLK): 1/1, 1/8, 1/32, and 1/128

The clock for the counter is selected by the CKS bits in CM3CSR. CM3CNT is incremented at the rising edge of the selected clock.

19.3.4 Internal Interrupt Request to CPU

The setting of the CMR bits in CM3CSR selects the sending of an internal interrupt request to the CPU at a compare match.

To clear an internal interrupt request to the CPU, the CMF bit should be set to B'0. Set the CMF bit to 0 in the handling routine for the CMT3 interrupt.

19.3.5 CMT3 Operation

As CM3CNT can be operated only by the RCLK, it continues the counter operation even when this LSI makes the transition to power control mode controlled by the SYSC and the core-area power supply is turned off after the necessary register settings have been made and B'1 has been written to the STR5 bit in CM3STR.

- Register Access

  The counter for the CMT3 is located in the sub-area because the counter has to be able to count-up even when this LSI is in power control mode controlled by the SYSC. The registers that are needed for the counter's operation are set from the core area. The following restrictions thus apply to the modification of registers.

After the following registers have been modified, do not make the transition to power control mode controlled by the SYSC until you are sure that, according to the restrictions given below, the result of the modification has been reflected in the LSI's actual operation. Otherwise, the modification may not be reflected in the register settings.

- CM3CSR: Bits CKS, CMM, and CMS
- CM3COR: Bits 31 to 0
- CM3STR: Bit STR5

These registers can be read immediately after being written to. However, two RCLK cycles are needed before the change is reflected.

- CM3CNT: Bits 31 to 0

After this register has been written to, two RCLK cycles are necessary before it can either be read or the value that it holds is reflected in the LSI's actual operation. Writing to this register, once started, is protected from further write operations until the writing operation has been completed.

19.3.6 Compare Match Flag Set Timing

The CMF bit in CM3CSR is set to 1 by the compare match signal generated when CM3COR and CM3CNT match. The compare match signal is generated upon the final state of the match (timing at which the CM3CNT value is updated to H'0). Consequently, after CM3COR and CM3CNT match, a compare match signal will not be generated until a CM3CNT counter clock is input. Figure 19.4 shows the set timing of the CMF bit.

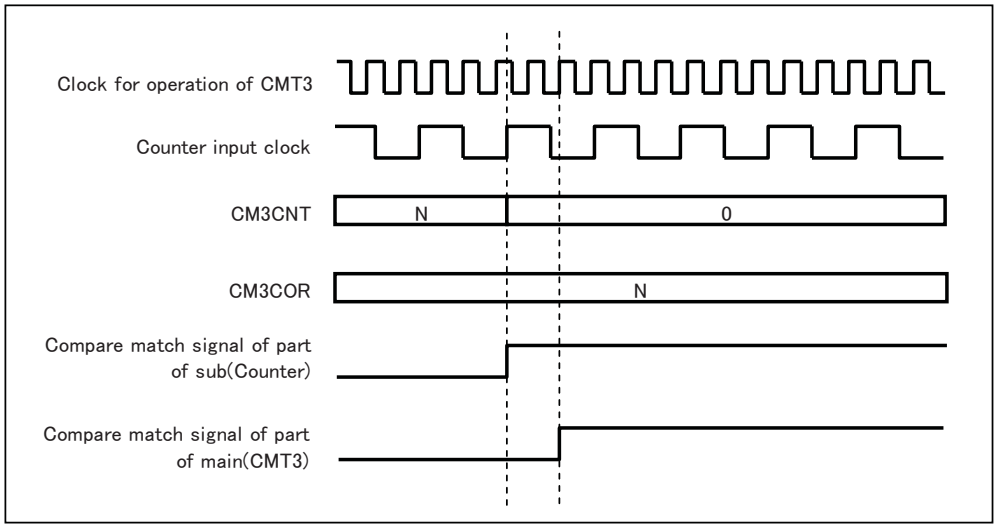


Figure 19.4 CMF Set Timing

Section 20 Compare Match Timer 4 (CMT4)

This LSI includes a 32-bit compare match timer (CMT4) of one channel.

20.1 Features

- One channel installed in the common domain
- 16 bits/32 bits can be selected.
- Provided with an auto-reload up counter.
- Provided with 32-bit constant registers and 32-bit up counters that can be written or read at any time.
- The CMT4 can perform counting even if this LSI is in power control mode controlled by the SYSC.
- Allows selection among four counter input clocks:
  — External clock (RCLK) input: 1/1, 1/8, 1/32, and 1/128
- One-shot operation and free-running operation are selectable.
- Allows selection of compare match or overflow for the interrupt source.
- Module standby mode can be set.
- Allows selection of counter operation/stop during debugging with the debug mode operation selector.

Figure 20.1 shows a block diagram of the CMT4.

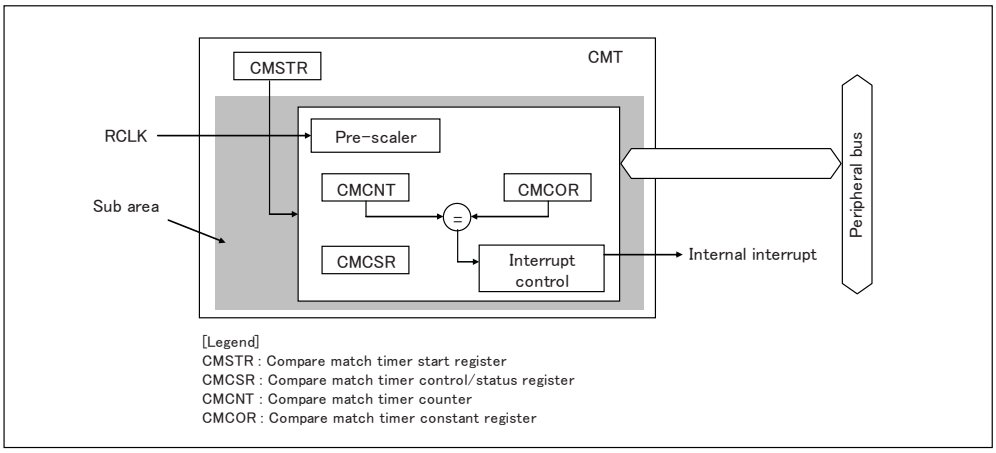


Figure 20.1 Block Diagram of CMT4

20.2 Register Descriptions

Table 20.1 shows the CMT4 register configuration. Table 20.2 shows the register states in each operating mode.

Table 20.1 Register Configuration

Register Name	Abbreviation	R/W	Address		Access Size
			Regular	Shadow	
Compare match timer start register	CM4STR	R/W	H'E614 8000	H'E714 8000	16
Compare match timer control/status register	CM4CSR	R/W	H'E614 8040	H'E714 8040	16
Compare match timer counter	CM4CNT	R/W	H'E614 8044	H'E714 8044	32
Compare match timer constant register	CM4COR	R/W	H'E614 8048	H'E714 8048	32

Table 20.2 Register States in Each Operating Mode

Register Abbreviation	Reset *	Module Standby
CM4STR	Initialized	Retained
CM4CSR	Initialized	Retained
CM4CNT	Initialized	Retained
CM4COR	Initialized	Retained

Note: * For details, refer to section 1-D Overview of reset.

20.2.1 Compare Match Timer Start Register (CM4STR)

CM4STR is a 16-bit register that selects whether the compare match timer counter (CM4CNT) is operated or halted.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	STR5	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	STR5	1	R/W	Count Start Selects whether to operate or halt the compare match timer counter (CM4CNT). 0: Halts CM4CNT count. 1: Starts CM4CNT count.
4 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

20.2.2 Compare Match Timer Control/Status Register (CM4CSR)

CM4CSR is a 16-bit register that indicates the occurrence of compare matches, enables interrupts, and sets the counter input clocks.

Do not change bits other than the CMF and OVF bits during the compare match timer counter (CM4CNT) operation.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMF	OVF	WRFLG	–	–	–	CMS	CMM	–	–	CMR[1:0]		DBG IVD	CKS[2:0]		
Initial Value:	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	1
R/W:	R/(W)*	R/(W)*	R	R	R	R	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	CMF	0	R/(W)*	Compare Match Flag This flag indicates whether or not values of the compare match timer counter (CM4CNT) and compare match timer constant register (CM4COR) have matched. Software cannot write 1 to the bit. When one-shot is selected for the counter operation, counting resumes by clearing this bit. 0: CM4CNT and CM4COR values have not matched. [Clearing condition] • Write 0 to CMF 1: CM4CNT and CM4COR values have matched.
14	OVF	0	R/(W)*	Overflow Flag This flag indicates whether or not the compare match timer counter (CM4CNT) has overflowed and been cleared to 0. Software cannot write 1 to this bit. 0: CM4CNT has not overflowed. [Clearing condition] • Write 0 to OVF 1: CM4CNT has overflowed.

Bit	Bit Name	Initial Value	R/W	Description
13	WRFLG	0	R	Write State Flag CM4CNT cannot be written to when this bit is 1. This bit indicates the period that the writing to CM4CNT is masked for synchronization after the writing to CM4CNT. Confirm that this flag is 0 when CM4CNT is written to continuously.
12 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	CMS	0	R/W	Compare Match Timer Counter Size Selects whether the compare match timer counter (CM4CNT) is used as a 16-bit counter or a 32-bit counter. This setting becomes the valid size for the compare match timer constant register (CM4COR). 0: Operates as a 32-bit counter. 1: Operates as a 16-bit counter.
8	CMM	1	R/W	Compare Match Mode Selects one-shot operation or free-running operation of the counter. 0: One-shot operation 1: Free-running operation
7, 6	—	All 0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
5, 4	CMR[1:0]	00	R/W	Compare Match Request These bits enable or disable an internal interrupt request in a compare match. 00: Disables an internal interrupt request. 01: Setting prohibited 10: Enables an internal interrupt request. 11: Setting prohibited
3	DBGIVD	1	R/W	Debug Mode Operation Select Sets the counter operation in debug mode. 0: Stops the counter operation in debug mode. 1: Enables the counter operation even in debug mode.
2 to 0	CKS[2:0]	111	R/W	Clock Select These bits select the clock input to CM4CNT. When the count start bit (STR5) in CM4STR is set to 1, CM4CNT begins incrementing with the clock selected by these bits. 000: Setting prohibited 001: Setting prohibited 010: Setting prohibited 011: Setting prohibited 100: RCLK/8 101: RCLK/32 110: RCLK/128 111: RCLK/1

Note: * Only 0 can be written to clear the flag.

20.2.3 Compare Match Timer Counter (CM4CNT)

CM4CNT is a 32-bit register that is used as an up-counter.

A counter operation is set by the compare match timer control/status register (CM4CSR). Therefore, set CM4CSR first, before starting a channel operation corresponding to the compare match timer start register (CM4STR). When the 16-bit counter operation is selected by the CMS bit, bits 15 to 0 of this register become valid. When the register should be written to, write the data that is added H'0000 to the upper half in a 32-bit operation. The contents of this register are initialized to H'00000000.

Counter operation of CMT4 is enabled even when the peripheral clock is stopped. Counter operation is also enabled in a state where the core-area power supply is turned off during power control mode controlled by the SYSC.

When CM4CNT is going to be read during the counter operation, the value that is read out may be wrong because of an asynchronous clock. Read several times with software and compare the read-out values.

20.2.4 Compare Match Timer Constant Register (CM4COR)

CM4COR is a 32-bit register that sets the compare match period with CM4CNT.

When the 16-bit counter operation is selected by the CMS bit in CM4CSR, bits 15 to 0 of this register become valid. When the register should be written to, write the data that is added H'0000 to the upper half in a 32-bit operation.

An overflow is detected when CM4CNT is cleared to 0 and this register is H'FFFFFFFF. The contents of this register are initialized to H'FFFFFFFF.

20.3 Operation

20.3.1 Counter Operation

The CMT4 starts the operation of the counter by writing B'1 to the STR5 bit in CM4STR after each register has been set. Complete all of the settings before starting the operation. Do not change the register settings other than clearing flag bits during the compare match timer (CM4CNT) operation.

The counter operates in one of two ways.

- One-Shot Operation

  One-shot operation is selected by setting the CMM bit in CM4CSR to B'0. When the value in CM4CNT matches the value in CM4COR, the value in CM4CNT is cleared to H'00000000 and the CMF bit in CM4CSR is set to B'1. Counting by CM4CNT stops after it has been cleared.

  To detect an overflow interrupt, set the value in CM4COR to H'FFFFFFFF. When the value in CM4CNT matches the value in CM4COR, CM4CNT is cleared to H'00000000 and the CMF and OVF bits in CM4CSR are set to B'1.

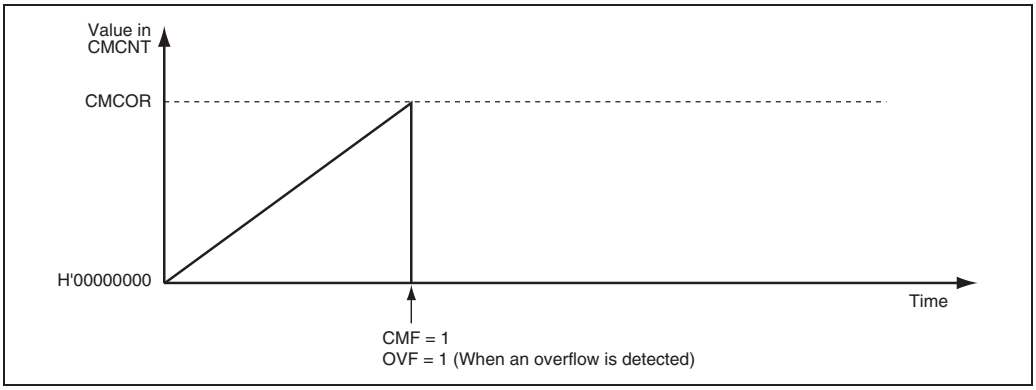


Figure 20.2 Counter Operation (One-Shot Operation)

- Free-Running Operation

  Free-running operation is selected by setting the CMM bit in CM4CSR to B'1. When the value in CM4CNT matches the value in CM4COR, CM4CNT is cleared to H'00000000 and the CMF bit in CM4CSR is set to B'1. CM4CNT resumes counting-up after it has been cleared.

To detect an overflow interrupt, set CM4COR to H'FFFFFFFF. When the values in CM4CNT and CM4COR match, CM4CNT is cleared to H'00000000 and the CMF and OVF bits in CM4CSR are set to B'1.

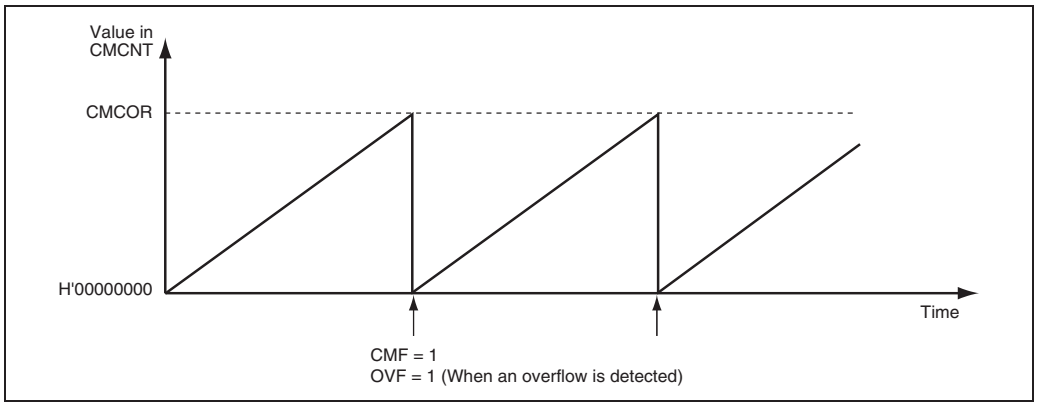


Figure 20.3 Counter Operation (Free-Running Operation)

20.3.2 Counter Size

In this module, the size of the counter is selectable as either 16 or 32 bits. This is selected by the CMS bit in CM4CSR.

When the 16-bit size is selected, use a 32-bit value which has H'0000 as its upper half to set CM4COR. To detect an overflow interrupt, CM4COR must be set to H'0000FFFF.

20.3.3 Timing for Counting by CM4CNT

In this module, the clock for the counter can be selected from among the following:

- External clock (RCLK): 1/1, 1/8, 1/32, and 1/128

The clock for the counter is selected by the CKS bits in CM4CSR. CM4CNT is incremented at the rising edge of the selected clock.

20.3.4 Internal Interrupt Request to CPU

The setting of the CMR bits in CM4CSR selects the sending of an internal interrupt request to the CPU at a compare match.

To clear the internal interrupt request to the CPU, the CMF bit should be set to B'0. Set the CMF bit to 0 in the handling routine for the CMT4 interrupt.

20.3.5 CMT4 Operation

As CM4CNT can be operated only by the RCLK, it continues the counter operation even when this LSI makes the transition to power control mode controlled by the SYSC and the core-area power supply is turned off after the necessary register settings have been made and B'1 has been written to the STR5 bit in CM4STR.

- Register Access

  The counter for the CMT4 is located in the sub area because the counter has to be able to count-up even when this LSI is in power control mode controlled by the SYSC. The registers that are needed for the counter's operation are set from the core area. The following restrictions thus apply to the modification of the registers.

After the following registers have been modified, do not make the transition to power control mode controlled by the SYSC until you are sure that, according to the restrictions given below, the result of the modification has been reflected in the LSI's actual operation. Otherwise, the modification may not be reflected in an actual result.

- CM4CSR: Bits CKS, CMM, and CMS
- CM4COR: Bits 31 to 0
- CM4STR: Bit STR5

Two RCLK cycles are necessary before this register is either read or any modification of the value it holds is reflected in the LSI's actual operation.

- CM4CNT: Bits 31 to 0

Two RCLK cycles are necessary before this register is either read or any modification of the value it holds is reflected in the LSI's actual operation. Writing to this register, once started, is protected from further write operations until the writing operation has been completed.

20.3.6 Compare Match Flag Set Timing

The CMF bit in CM4CSR is set to 1 by the compare match signal generated when CM4COR and CM4CNT match. The compare match signal is generated upon the final state of the match (timing at which the CM4CNT value is updated to H'0). Consequently, after CM4COR and CM4CNT match, a compare match signal will not be generated until a CM4CNT counter clock is input. Figure 20.4 shows the set timing of the CMF bit.

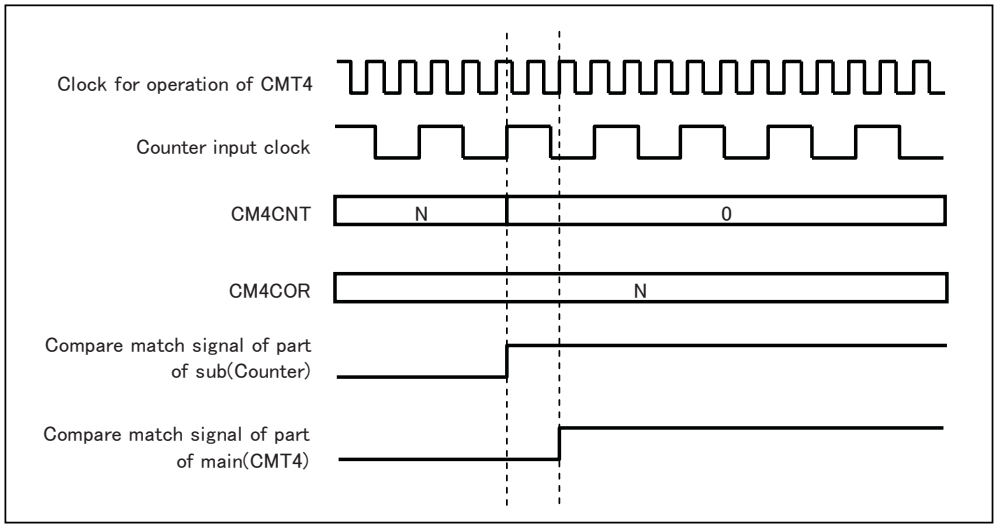


Figure 20.4 CMF Set Timing

Section 21 Serial Communications Interface with FIFO A (SCIFA)

This LSI has six serial communications interfaces incorporating FIFO buffers (Serial Communications Interface with FIFO A: SCIFA) that can perform both asynchronous and clocked synchronous serial communications.

Each interface includes two 64-stage buffers, one for the transmit FIFO register and one for the receive FIFO register, enabling fast, efficient, and continuous communications.

21.1 Features

- Six channels installed in the system domain
- Asynchronous mode

  Serial data communications is executed using an asynchronous system in which synchronization is achieved character by character. Serial data communications can be carried out with standard asynchronous communications chips such as a Universal Asynchronous Receiver/Transmitter (UART) or Asynchronous Communications Interface Adapter (ACIA).

  There is a choice of 8 serial data communication formats.

  — Data length: 7 or 8 bits
  — Stop bit length: 1 or 2 bits
  — Parity: Even/odd/none
  — LSB-first transfer
  — Receive error detection: Parity, framing, and overrun errors
  — Break detection: If a framing error is following by at least one frame at the space "0" (low level), a break is detected.
- Clocked synchronous mode

  Serial data communications is synchronized with a clock. Serial data communications can be carried out with other LSIs that have a clocked synchronous communications function.

  — Data length: 8 bits
  — Receive error detection: Overrun errors
  — A rising or falling edge of a clock is selectable as the data transmit/receive timing.
- On-chip baud rate generator allows any bit rate to be selected.
- Serial clock source: Internal clock signal generated by the baud-rate generator.

- Seven interrupt sources

  There are seven interrupt sources—transmit-data-stop, transmit-FIFO-data-empty, receive-FIFO-data-full, receive-error (framing/parity error), break-receive, and receive-data-ready interrupts. The vectors of each interrupt source are the same.
- The DMA controller (DMAC) can be activated to execute a data transfer in the event of a transmit-FIFO-data-empty, transmit-data-stop, or receive-FIFO-data-full interrupt. The DMAC requests of transmit-FIFO-data-empty and transmit-data-stop interrupts are the same.
- DMA multi-byte data transfer supported
- On-chip modem control functions (CTS_N and RTS_N)
- On-chip transmit-data-stop functions
- When not in use, SCIFA can be stopped by halting its clock supply to reduce power consumption.
- The amount of data in the transmit/receive FIFO registers, and the number of receive errors in the receive data in the receive FIFO register, can be ascertained.

Figure 21.1 shows a block diagram of SCIFA.

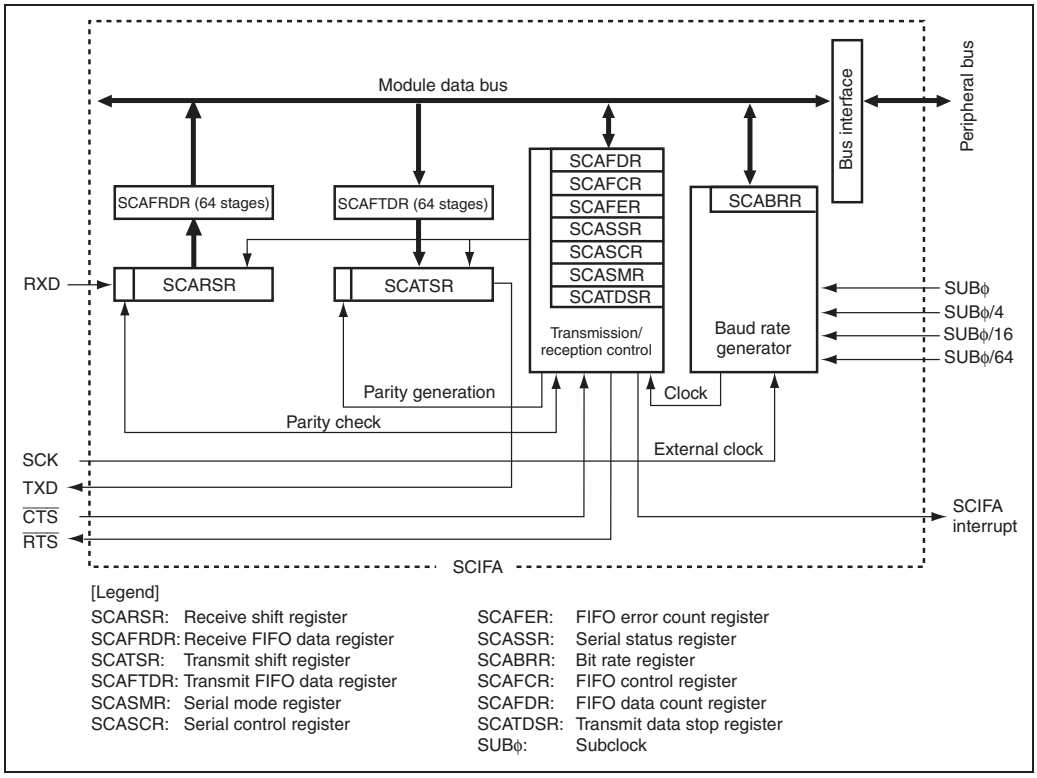


Figure 21.1 Block Diagram of SCIFA

21.2 Input/Output Pins

Table 21.1 shows the SCIFA pin configuration.

Table 21.1 Pin Configuration

Channel	Pin Name	I/O	Function
0	SCIFA0_SCK	Output	Clock output
	SCIFA0_RXD	Input	Receive data input
	SCIFA0_TXD	Output	Transmit data output
	SCIFA0_CTS_N	Input	Transmission enabled
	SCIFA0_RTS_N	Output	Transmit request
1	SCIFA1_SCK1	Output	Clock output
	SCIFA1_RXD1	Input	Receive data input
	SCIFA1_TXD1	Output	Transmit data output
	SCIFA1_CTS1_N	Input	Transmission enabled
	SCIFA1_RTS1_N	Output	Transmit request
2	SCIFA2_SCK1	Output	Clock output
	SCIFA2_RXD1	Input	Receive data input
	SCIFA2_TXD1	Output	Transmit data output
	SCIFA2_CTS1_N	Input	Transmission enabled
	SCIFA2_RTS1_N	Output	Transmit request

Channel	Pin Name	I/O	Function
3	SCIFA3_SCK	Output	Clock output
	SCIFA3_RXD	Input	Receive data input
	SCIFA3_TXD	Output	Transmit data output
	SCIFA3_CTS1_N	Input	Transmission enabled
	SCIFA3_CTS2_N		
	SCIFA3_RTS1_N	Output	Transmit request
	SCIFA3_RTS2_N		
4	SCIFA4_RXD	Input	Receive data input
	SCIFA4_TXD	Output	Transmit data output
5	SCIFA5_RXD	Input	Receive data input
	SCIFA5_TXD	Output	Transmit data output

Notes: The channel number is omitted, and SCK, RxD, TxD, CTS_N, and RTS_N are used as generic terms in the following descriptions.

21.3 Register Descriptions

Table 21.2 shows the SCIFA registers. Table 21.3 shows the register states in the respective processing modes.

Table 21.2 Register Configuration

Register Name	Abbreviation	R/W	Address		Access Size
			Regular	Shadow	
Serial mode register A0	SCASMR0	R/W	H'E6C4 0000	H'E7C4 0000	16
Bit rate register A0	SCABRR0	R/W	H'E6C4 0004	H'E7C4 0004	8
Serial control register A0	SCASCR0	R/W	H'E6C4 0008	H'E7C4 0008	16
Transmit data stop register A0	SCATDSR0	R/W	H'E6C4 000C	H'E7C4 000C	8
FIFO error count register A0	SCAFER0	R	H'E6C4 0010	H'E7C4 0010	16
Serial status register A0	SCASSR0	R/W*	H'E6C4 0014	H'E7C4 0014	16
FIFO control register A0	SCAFCR0	R/W	H'E6C4 0018	H'E7C4 0018	16
FIFO data count register A0	SCAFDR0	R	H'E6C4 001C	H'E7C4 001C	16
Transmit FIFO data register A0	SCAFTDR0	W	H'E6C4 0020	H'E7C4 0020	8
Receive FIFO data register A0	SCAFRDR0	R	H'E6C4 0024	H'E7C4 0024	8
Serial port control register A0	SCAPCR0	R/W	H'E6C4 0030	H'E7C4 0030	16
Serial port data register A0	SCAPDR0	R/W	H'E6C4 0034	H'E7C4 0034	16
Serial mode register A1	SCASMR1	R/W	H'E6C5 0000	H'E7C5 0000	16
Bit rate register A1	SCABRR1	R/W	H'E6C5 0004	H'E7C5 0004	8
Serial control register A1	SCASCR1	R/W	H'E6C5 0008	H'E7C5 0008	16
Transmit data stop register A1	SCATDSR1	R/W	H'E6C5 000C	H'E7C5 000C	8
FIFO error count register A1	SCAFER1	R	H'E6C5 0010	H'E7C5 0010	16
Serial status register A1	SCASSR1	R/W*	H'E6C5 0014	H'E7C5 0014	16
FIFO control register A1	SCAFCR1	R/W	H'E6C5 0018	H'E7C5 0018	16

Register Name	Abbreviation	R/W	Address		Access Size
			Regular	Shadow	
FIFO data count register A1	SCAFDR1	R	H'E6C5 001C	H'E7C5 001C	16
Transmit FIFO data register A1	SCAFTDR1	W	H'E6C5 0020	H'E7C5 0020	8
Receive FIFO data register A1	SCAFRDR1	R	H'E6C5 0024	H'E7C5 0024	8
Serial port control register A1	SCAPCR1	R/W	H'E6C5 0030	H'E7C5 0030	16
Serial port data register A1	SCAPDR1	R/W	H'E6C5 0034	H'E7C5 0034	16
Serial mode register A2	SCASMR2	R/W	H'E6C6 0000	H'E7C6 0000	16
Bit rate register A2	SCABRR2	R/W	H'E6C6 0004	H'E7C6 0004	8
Serial control register A2	SCASCR2	R/W	H'E6C6 0008	H'E7C6 0008	16
Transmit data stop register A2	SCATDSR2	R/W	H'E6C6 000C	H'E7C6 000C	8
FIFO error count register A2	SCAFER2	R	H'E6C6 0010	H'E7C6 0010	16
Serial status register A2	SCASSR2	R/W*	H'E6C6 0014	H'E7C6 0014	16
FIFO control register A2	SCAFCR2	R/W	H'E6C6 0018	H'E7C6 0018	16
FIFO data count register A2	SCAFDR2	R	H'E6C6 001C	H'E7C6 001C	16
Transmit FIFO data register A2	SCAFTDR2	W	H'E6C6 0020	H'E7C6 0020	8
Receive FIFO data register A2	SCAFRDR2	R	H'E6C6 0024	H'E7C6 0024	8
Serial port control register A2	SCAPCR2	R/W	H'E6C6 0030	H'E7C6 0030	16
Serial port data register A2	SCAPDR2	R/W	H'E6C6 0034	H'E7C6 0034	16
Serial mode register A3	SCASMR3	R/W	H'E6C7 0000	H'E7C7 0000	16
Bit rate register A3	SCABRR3	R/W	H'E6C7 0004	H'E7C7 0004	8
Serial control register A3	SCASCR3	R/W	H'E6C7 0008	H'E7C7 0008	16
Transmit data stop register A3	SCATDSR3	R/W	H'E6C7 000C	H'E7C7 000C	8

Register Name	Abbreviation	R/W	Address		Access Size
			Regular	Shadow	
FIFO error count register A3	SCAFER3	R	H'E6C7 0010	H'E7C7 0010	16
Serial status register A3	SCASSR3	R/W*	H'E6C7 0014	H'E7C7 0014	16
FIFO control register A3	SCAFCR3	R/W	H'E6C7 0018	H'E7C7 0018	16
FIFO data count register A3	SCAFDR3	R	H'E6C7 001C	H'E7C7 001C	16
Transmit FIFO data register A3	SCAFTDR3	W	H'E6C7 0020	H'E7C7 0020	8
Receive FIFO data register A3	SCAFRDR3	R	H'E6C7 0024	H'E7C7 0024	8
Serial port control register A3	SCAPCR3	R/W	H'E6C7 0030	H'E7C7 0030	16
Serial port data register A3	SCAPDR3	R/W	H'E6C7 0034	H'E7C7 0034	16
Serial mode register A4	SCASMR4	R/W	H'E6C8 0000	H'E7C8 0000	16
Bit rate register A4	SCABRR4	R/W	H'E6C8 0004	H'E7C8 0004	8
Serial control register A4	SCASCR4	R/W	H'E6C8 0008	H'E7C8 0008	16
Transmit data stop register A4	SCATDSR4	R/W	H'E6C8 000C	H'E7C8 000C	8
FIFO error count register A4	SCAFER4	R	H'E6C8 0010	H'E7C8 0010	16
Serial status register A4	SCASSR4	R/W*	H'E6C8 0014	H'E7C8 0014	16
FIFO control register A4	SCAFCR4	R/W	H'E6C8 0018	H'E7C8 0018	16
FIFO data count register A4	SCAFDR4	R	H'E6C8 001C	H'E7C8 001C	16
Transmit FIFO data register A4	SCAFTDR4	W	H'E6C8 0020	H'E7C8 0020	8
Receive FIFO data register A4	SCAFRDR4	R	H'E6C8 0024	H'E7C8 0024	8
Serial port control register A4	SCAPCR4	R/W	H'E6C8 0030	H'E7C8 0030	16
Serial port data register A4	SCAPDR4	R/W	H'E6C8 0034	H'E7C8 0034	16
Serial mode register A5	SCASMR5	R/W	H'E6CB 0000	H'E7CB 0000	16
Bit rate register A5	SCABRR5	R/W	H'E6CB 0004	H'E7CB 0004	8

Register Name	Abbreviation	R/W	Address		Access Size
			Regular	Shadow	
Serial control register A5	SCASCR5	R/W	H'E6CB 0008	H’E7CB 0008	16
Transmit data stop register A5	SCATDSR5	R/W	H'E6CB 000C	H’E7CB 000C	8
FIFO error count register A5	SCAFER5	R	H'E6CB 0010	H’E7CB 0010	16
Serial status register A5	SCASSR5	R/W*	H'E6CB 0014	H’E7CB 0014	16
FIFO control register A5	SCAFCR5	R/W	H'E6CB 0018	H’E7CB 0018	16
FIFO data count register A5	SCAFDR5	R	H'E6CB 001C	H’E7CB 001C	16
Transmit FIFO data register A5	SCAFTDR5	W	H'E6CB 0020	H’E7CB 0020	8
Receive FIFO data register A5	SCAFRDR5	R	H'E6CB 0024	H’E7CB 0024	8
Serial port control register A5	SCAPCR5	R/W	H'E6CB 0030	H'E7CB 0030	16
Serial port data register A5	SCAPDR5	R/W	H'E6CB 0034	H'E7CB 0034	16

Note: * To clear the flags, 0s can only be written to bits 9 to 7, 5, 4, 1, and 0.

Table 21.3 Register States in Each Operating Mode

Abbreviation	Reset*	Module Standby
SCASMR0	Initialized	Retained
SCABRR0	Initialized	Retained
SCASCR0	Initialized	Retained
SCATDSR0	Initialized	Retained
SCAFER0	Initialized	Retained
SCASSR0	Initialized	Retained
SCAFCR0	Initialized	Retained
SCAFDR0	Initialized	Retained
SCAFTDR0	Undefined	Retained
SCAFRDR0	Undefined	Retained
SCAPCR0	Initialized	Retained
SCAPDR0	Undefined	Retained
SCASMR1	Initialized	Retained
SCABRR1	Initialized	Retained
SCASCR1	Initialized	Retained
SCATDSR1	Initialized	Retained
SCAFER1	Initialized	Retained
SCASSR1	Initialized	Retained
SCAFCR1	Initialized	Retained
SCAFDR1	Initialized	Retained
SCAFTDR1	Undefined	Retained
SCAFRDR1	Undefined	Retained
SCAPCR1	Initialized	Retained
SCAPDR1	Undefined	Retained
SCASMR2	Initialized	Retained
SCABRR2	Initialized	Retained
SCASCR2	Initialized	Retained
SCATDSR2	Initialized	Retained
SCAFER2	Initialized	Retained
SCASSR2	Initialized	Retained

Abbreviation	Reset*	Module Standby
SCAFCR2	Initialized	Retained
SCAFDR2	Initialized	Retained
SCAFTDR2	Undefined	Retained
SCAFRDR2	Undefined	Retained
SCAPCR2	Initialized	Retained
SCAPDR2	Undefined	Retained
SCASMR3	Initialized	Retained
SCABRR3	Initialized	Retained
SCASCR3	Initialized	Retained
SCATDSR3	Initialized	Retained
SCAFER3	Initialized	Retained
SCASSR3	Initialized	Retained
SCAFCR3	Initialized	Retained
SCAFDR3	Initialized	Retained
SCAFTDR3	Undefined	Retained
SCAFRDR3	Undefined	Retained
SCAPCR3	Initialized	Retained
SCAPDR3	Undefined	Retained
SCASMR4	Initialized	Retained
SCABRR4	Initialized	Retained
SCASCR4	Initialized	Retained
SCATDSR4	Initialized	Retained
SCAFER4	Initialized	Retained
SCASSR4	Initialized	Retained
SCAFCR4	Initialized	Retained
SCAFDR4	Initialized	Retained
SCAPCR4	Initialized	Retained
SCAPDR4	Undefined	Retained
SCASMR5	Initialized	Retained
SCABRR5	Initialized	Retained
SCASCR5	Initialized	Retained

Abbreviation	Reset*	Module Standby
SCATDSR5	Initialized	Retained
SCAFER5	Initialized	Retained
SCASSR5	Initialized	Retained
SCAFCR5	Initialized	Retained
SCAFDR5	Initialized	Retained
SCAFTDR5	Undefined	Retained
SCAFRDR5	Undefined	Retained
SCAPCR5	Initialized	Retained
SCAPDR5	Undefined	Retained

Note: * For details, refer to section 1-D Overview of reset.

21.3.1 Receive Shift Register (SCARSR)

SCARSR is the register used to receive serial data.

SCIFA sets serial data input from the RxD pin in SCRASR in the order received, starting with the LSB (bit 0), and converts it to parallel data. When one byte of data has been received, it is automatically transferred to SCAFRDR.

SCARSR cannot be directly read from or written to by the CPU.

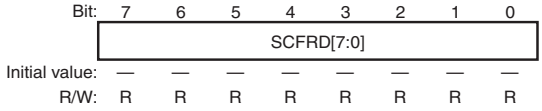
21.3.2 Receive FIFO Data Register (SCAFRDR)

SCAFRDR is a 64-stage FIFO register that stores received serial data.

When SCIFA has received one byte of serial data, it transfers the received data from SCARSR to SCAFRDR where it is stored, and completes the receive operation. SCARSR is then enabled for reception, and consecutive receive operations can be performed until SCAFRDR is full (64-character data).

SCAFRDR is a read-only register, and cannot be written to by the CPU.

If a read is performed when there is no receive data in SCAFRDR, an undefined value will be returned. When SCAFRDR is full of receive data, subsequent serial data is lost.



Bit	Bit Name	Initial Value	R/W	Description
7 to 0	SCFRD[7:0]	Undefined	R	Serial receive data FIFO

21.3.3 Transmit Shift Register (SCATSR)

SCATSR is the register used to transmit serial data.

To perform serial data transmission, SCIFA first transfers transmit data from SCAFTDR to SCATSR, then sends the data to the TxD pin starting with the LSB (bit 0).

When transmission of one byte is completed, the next transmit data is transferred from SCAFTDR to SCATSR, and transmission started automatically.

SCATSR cannot be directly read from or written to by the CPU.

21.3.4 Transmit FIFO Data Register (SCAFTDR)

SCAFTDR is an 8-bit 64-stage FIFO data register that stores data for serial transmission.

If SCATSR is empty when transmit data has been written to SCAFTDR, SCIFA transfers the transmit data written in SCAFTDR to SCATSR and starts serial transmission.

SCAFTDR is a write-only register, and cannot be read by the CPU.

The next data cannot be written when SCAFTDR is filled with 64 bytes of transmit data. Data written in this case is ignored.

Bit:	7	6	5	4	3	2	1	0
	SCFTD[7:0]							
Initial value:	—	—	—	—	—	—	—	—
R/W:	W	W	W	W	W	W	W	W

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	SCFTD[7:0]	Undefined	W	Serial transmit data FIFO

21.3.5 Serial Mode Register (SCASMR)

SCASMR is a 16-bit readable/writable register used to set SCIFA's serial transfer format and select the baud rate generator clock source and the sampling rate.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CKEDG	—	SRC[2:0]			C/$\overline{A}$	CHR	PE	O/E	STOP	—	CKS[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
12	CKEDG	0	R/W	Transmit/Receive Clock Edge Select Selects the clock edge at which the serial data is output in clocked synchronous mode. 0: Serial data is transmitted at the falling edge of output clock. Serial data is received at the rising edge of output clock. 1: Serial data is transmitted at the rising edge of output clock. Serial data is received at the falling edge of output clock.
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10 to 8	SRC[2:0]	000	R/W	Sampling Control These bits select the sampling rate. 000: Sampling rate 1/16 001: Sampling rate 1/5 010: Sampling rate 1/7 011: Sampling rate 1/11 100: Sampling rate 1/13 101: Sampling rate 1/17 110: Sampling rate 1/19 111: Sampling rate 1/27
7	C/$\overline{A}$	0	R/W	Communication Mode Selects asynchronous mode or clocked synchronous mode as the SCIFA operating mode. 0: Asynchronous mode 1: Clocked synchronous mode

Bit	Bit Name	Initial Value	R/W	Description
6	CHR	0	R/W	Character Length Selects 7 or 8 bits as the data length. 0: 8-bit data 1: 7-bit data* Note: * When the 7-bit character is selected, the MSB (bit 7) in SCAFTDR is not transmitted.
5	PE	0	R/W	Parity Enable Selects whether or not parity bit addition is performed in transmission, and parity bit checking in reception. 0: Parity bit addition and checking disabled 1: Parity bit addition and checking enabled* Note: * When the PE bit is set to 1, the parity (even or odd) specified by the O/E bit is added to transmit data before transmission. In reception, the parity bit is checked for the parity (even or odd) specified by the O/E bit.
4	O/E	0	R/W	Parity Mode Selects either even or odd parity for use in parity addition and checking. The O/E bit setting is only valid when the PE bit is set to 1, enabling parity bit addition and checking. The O/E bit setting is invalid when parity addition and checking is disabled. 0: Even parity*[1] 1: Odd parity*[2] Notes: 1. When even parity is set, parity bit addition is performed in transmission so that the total number of 1-bits in the transmit character plus the parity bit is even. In reception, a check is performed to see if the total number of 1-bits in the receive character plus the parity bit is even. 2. When odd parity is set, parity bit addition is performed in transmission so that the total number of 1-bits in the transmit character plus the parity bit is odd. In reception, a check is performed to see if the total number of 1-bits in the receive character plus the parity bit is odd.

Bit	Bit Name	Initial Value	R/W	Description
3	STOP	0	R/W	Stop Bit Length Selects 1 or 2 bits as the stop bit length. In reception, only the first stop bit is checked, regardless of the STOP bit setting. If the second stop bit is 1, it is treated as a stop bit; if it is 0, it is treated as the start bit of the next transmit character. 0: 1 stop bit*[1] 1: 2 stop bits*[2] Notes: 1. In transmission, a single logic-1 bit (stop bit) is added to the end of a transmit character before it is sent. 2. In transmission, two logic-1 bits (stop bits) are added to the end of a transmit character before it is sent.
2	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
1, 0	CKS[1:0]	00	R/W	Clock Select These bits select the clock sources for the on-chip baud rate generator. 00: SUBϕ 01: SUBϕ/4 10: SUBϕ/16 11: SUBϕ/64 Note: SUBϕ: Subclock

21.3.6 Serial Control Register (SCASCR)

SCASCR is a 16-bit readable/writable register that performs enabling or disabling of SCIFA transfer operations and interrupt requests, and selection of the serial clock source.

ビット:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TDRQE	RDRQE	–	TENDE	TSIE	ERIE	BRIE	DRIE	TIE	RIE	TE	RE	–	–	–	CKE0
初期値:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	TDRQE	0	R/W	Transmit Data Transfer Request Enable Switches the transmit FIFO empty interrupt or DMA transfer request when TIE = 1 and the transmit FIFO empty occurs. 0: Interrupt request to CPU is issued 1: Transmit data transfer request to DMAC is issued
14	RDRQE	0	R/W	Receive Data Transfer Request Enable Switches the receive FIFO-data-full interrupt or DMA transfer request when RIE = 1 and the receive FIFO-data-full occurs. 0: Interrupt request to CPU is issued 1: Receive data transfer request to DMAC is issued
13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	TENDE	0	R/W	Transmit End interrupt enable Enables or disables generation of a transmit-end interrupt when the TEND flag in SCASSR is set to 1. 0: Transmit-end interrupt disabled* 1: Transmit-end interrupt enabled
11	TSIE	0	R/W	Transmit Data Stop Interrupt Enable Enables or disables generation of a transmit-data-stop interrupt when the TSE bit in SCAFCR is enabled and the TSF flag in SCASSR is set to 1. 0: Transmit-data-stop interrupt disabled* 1: Transmit-data-stop interrupt enabled

Note: * The TDI interrupt request is cleared by clearing the TSF flag to 0 after reading 1 from it or clearing the TSIE bit to 0.

Bit	Bit Name	Initial Value	R/W	Description
10	ERIE	0	R/W	Receive Error Interrupt Enable Enables or disables generation of a receive-error (framing or parity error) interrupt when the ER flag in SCASSR is set to 1. 0: Receive-error interrupt disabled* 1: Receive-error interrupt enabled Note: * The ERI interrupt request is cleared by clearing the ER flag to 0 after reading 1 from it or clearing the ERIE bit to 0.
9	BRIE	0	R/W	Break Interrupt Enable Enables or disables generation of a break-receive interrupt when the BRK flag in SCASSR is set to 1. 0: Break-receive interrupt disabled* 1: Break-receive interrupt enabled Note: * The BRI interrupt request is cleared by clearing the BRK flag to 0 after reading 1 from it or clearing the BRIE bit to 0.
8	DRIE	0	R/W	Receive Data Ready Interrupt Enable Enables or disables generation of a receive-data-ready interrupt when the DR flag in SCASSR is set to 1. 0: Receive-data-ready interrupt disabled* 1: Receive-data-ready interrupt enabled Note: * The DRI interrupt request is cleared by clearing the DR flag to 0 after reading 1 from it or clearing the DRIE bit to 0.
7	TIE	0	R/W	Transmit Interrupt Enable Enables or disables generation of a transmit-FIFO-data-empty interrupt request when the TDFE flag in SCASSR is set to 1. 0: Transmit-FIFO-data-empty interrupt request disabled* 1: Transmit-FIFO-data-empty interrupt request enabled Note: * Interrupt requests can be cleared by writing transmit data exceeding the transmit trigger set number to SCAFTDR, reading 1 from the TDFE flag, then clearing it to 0, or by clearing the TIE bit to 0.

Bit	Bit Name	Initial Value	R/W	Description
6	RIE	0	R/W	Receive Interrupt Enable Enables or disables generation of a receive-FIFO-data-full interrupt request when the RDF flag in SCASSR is set to 1. 0: Receive-FIFO-data-full interrupt request disabled* 1: Receive-FIFO-data-full interrupt request enabled Note: * Interrupt requests can be cleared by reading 1 from the RDF flag, then clearing the flag to 0, or by clearing the RIE bit to 0.
5	TE	0	R/W	Transmit Enable Enables or disables the start of serial transmission by SCIFA. 0: Transmission disabled 1: Transmission enabled* Note: * SCASMR and SCAFCR settings must be made, the transmit format decided, and the transmit FIFO reset, before the TE bit is set to 1.
4	RE	0	R/W	Receive Enable Enables or disables the start of serial reception by SCIFA. 0: Reception disabled*[1] 1: Reception enabled*[2] Notes: 1. Clearing the RE bit to 0 does not affect the DR, ER, BRK, RDF, FER, PER, and ORER flags, which retain their state. 2. Serial mode register (SCASMR) and FIFO control register (SCAFCR) settings must be made, the receive format decided, and the receive FIFO reset, before the RE bit is set to 1.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
0	CKE0	0	R/W	Clock Enable Enables or disables the clock output from the SCK pin. The CKE0 bit must be set before determining the SCIFA operating mode with SCASMR. 0: SCK pin disabled SCK pin state is Hi-Z. 1: Clock output from SCK* Note: * In clocked synchronous mode, outputs a clock with the same frequency as the bit rate.

21.3.7 FIFO Error Count Register (SCAFER)

SCAFER is a 16-bit read-only register that indicates the number of receive errors (framing errors and parity errors)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	PER[5:0]						—	—	FER[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13 to 8	PER[5:0]	000000	R	Parity Error Count These bits indicate the number of data in which parity errors are generated, in receive data stored in SCAFRDR. After the ER bit in SCASSR is set, the value of bits PER5 to PER0 indicate the number of data in which parity errors are generated. When all 64 bytes of receive data in SCAFRDR have parity errors, these bits indicate 0.

Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5 to 0	FER[5:0]	000000	R	Framing Error Count These bits indicate the number of data in which framing errors are generated, in receive data stored in SCAFRDR. After the ER bit in SCASSR is set, the value of bits FER5 to FER0 indicate the number of data in which framing errors are generated. When all 64 bytes of receive data in SCAFRDR have framing errors, these bits indicate 0.

21.3.8 Serial Status Register (SCASSR)

SCASSR is a 16-bit readable/writable register that indicates the SCIFA status.

However, 1 cannot be written to the ORER, TSF, ER, TDFE, BRK, RDF, and DR flags. Also note that in order to clear these flags to 0, they must be read as 1 beforehand. The TEND, FER, and PER flags are read-only flags and cannot be modified.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	ORER	TSF	ER	TEND	TDFE	BRK	FER	PER	RDF	DR
Initial value:	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/(W)*	R/(W)*	R/(W)*	R	R/(W)*	R/(W)*	R	R	R/(W)*	R/(W)*

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
9	ORER	0	R/(W)*	Overrun Error Indicates that an overrun error occurred during reception. This bit setting is valid only in asynchronous mode. 0: Reception in progress, or reception has ended normally*[1] [Clearing conditions] • Power-on reset or manual reset • When 0 is written to ORER after reading ORER = 1 1: An overrun error occurred during reception*[2] [Setting condition] • When serial reception is completed while receive FIFO is full Notes: 1. The ORER flag is not affected and retains its previous state when the RE bit in SCASCR is cleared to 0. 2. The receive data prior to the overrun error is retained in SCAFRDR, and the data received subsequently is lost. Serial reception cannot be continued while the ORER flag is set to 1.
8	TSF	0	R/(W)*	Transmit Data Stop Indicates that the number of transmit data matches the value of SCATDSR. This bit setting is valid only in asynchronous mode. 0: Number of transmit data does not match value of SCATDSR [Clearing conditions] • Power-on reset or manual reset • When 0 is written to TSF after reading TSF = 1 1: Number of transmit data matches value of SCATDSR

Bit	Bit Name	Initial Value	R/W	Description
7	ER	0	R/(W)*	Receive Error Indicates that a framing error or parity error occurred during reception.*[1] This bit setting is valid only in asynchronous mode. 0: No framing error or parity error occurred during reception [Clearing conditions] • Power-on reset or manual reset • When 0 is written to ER after reading ER = 1 1: A framing error or parity error occurred during reception [Setting conditions] • When SCIFA checks whether the stop bit at the end of the receive data is 1 when reception ends, and the stop bit is 0*[2] • When, in reception, the number of logic-1 bits in the receive data and in the parity bit does not match the parity setting (even or odd) specified by the O/E bit in SCASMR Notes: 1. The ER flag is not affected and retains its previous state when the RE bit in SCASCR is cleared to 0. When a receive error occurs, the receive data is still transferred to SCAFRDR, and reception continues. The FER and PER bits in SCASSR can be used to determine whether there is a receive error in the data read from SCAFRDR. 2. When the stop length is 2 bits, only the first stop bit is checked for a value of 1; the second stop bit is not checked.

Bit	Bit Name	Initial Value	R/W	Description
6	TEND	1	R	Transmit End Indicates that there is no valid data in SCAFTDR when the last bit of the transmit character is sent, and transmission has been ended. 0: Transmission is in progress [Clearing condition] • When data is written to SCAFTDR 1: Transmission has been ended [Setting condition] • When there is no transmit data in SCAFTDR on transmission of a 1-byte serial transmit character
5	TDFE	1	R/(W)*	Transmit FIFO Data Empty Indicates that data has been transferred from SCAFTDR to SCATSR, the number of data bytes in SCAFTDR has fallen to or below the transmit trigger data number set by bits TTRG1 and TTRG0 in SCAFCR, and new transmit data can be written to SCAFTDR. 0: A number of transmit data bytes exceeding the transmit trigger set number have been written to SCAFTDR [Clearing condition] • When transmit data exceeding the transmit trigger set number is written to SCAFTDR, and 0 is written to TDFE after reading TDFE = 1 1: The number of transmit data bytes in SCAFTDR does not exceed the transmit trigger set number [Setting conditions] • Power-on reset or manual reset • When the number of SCAFTDR transmit data bytes falls to or below the transmit trigger set number as the result of a transmit operation* Note: * As SCAFTDR is a 64-byte FIFO register, the maximum number of bytes that can be written when TDFE = 1 is 64 – (transmit trigger set number). Data written in excess of this will be ignored. The number of data bytes in SCAFTDR is indicated by SCAFDR.

Bit	Bit Name	Initial Value	R/W	Description
4	BRK	0	R/(W)*	Break Detect Indicates that a receive data break signal has been detected. This bit setting is valid only in asynchronous mode. 0: A break signal has not been received [Clearing conditions] • Power-on reset or manual reset • When 0 is written to BRK after reading BRK = 1 1: A break signal has been received* [Setting condition] • When data with a framing error is received, followed by the space 0 level (low level) for at least one frame length Note: * When a break is detected, the receive data (H'00) following detection is not transferred to SCAFRDR. When the break ends and the receive signal returns to mark 1, receive data transfer is resumed.
3	FER	0	R	Framing Error Indicates a framing error in the data read from SCAFRDR. This bit setting is valid only in asynchronous mode. 0: There is no framing error in the receive data read from SCAFRDR [Clearing conditions] • Power-on reset or manual reset • When there is no framing error in SCAFRDR read data 1: There is a framing error in the receive data read from SCAFRDR [Setting condition] • When there is a framing error in SCAFRDR read data

Bit	Bit Name	Initial Value	R/W	Description
2	PER	0	R	Parity Error Indicates a parity error in the data read from SCAFRDR. This bit setting is valid only in asynchronous mode. 0: There is no parity error in the receive data read from SCAFRDR [Clearing conditions] • Power-on reset or manual reset • When there is no parity error in SCAFRDR read data 1: There is a parity error in the receive data read from SCAFRDR [Setting condition] • When there is a parity error in SCAFRDR read data
1	RDF	0	R/(W)*	Receive FIFO Data Full Indicates that the received data has been transferred from SCARSR to SCAFRDR, and the number of receive data bytes in SCAFRDR is equal to or greater than the receive trigger number set by bits RTRG1 and RTRG0 in SCAFCR. 0: The number of receive data bytes in SCAFRDR is less than the receive trigger set number [Clearing conditions] • Power-on reset or manual reset • When SCAFRDR is read until the number of receive data bytes in SCAFRDR falls below the receive trigger set number, and 0 is written to RDF after reading RDF = 1 1: The number of receive data bytes in SCAFRDR is equal to or greater than the receive trigger set number [Setting condition] • When SCAFRDR contains at least the receive trigger set number of receive data bytes* Note: * SCAFRDR is a 64-byte FIFO register. When RDF = 1, at least the receive trigger set number of data bytes can be read. If data is read when SCAFRDR is empty, an undefined value will be returned. The number of receive data bytes in SCAFRDR is indicated by the lower bits of SCAFDR.

Bit	Bit Name	Initial Value	R/W	Description
0	DR	0	R/(W)*	Receive Data Ready Indicates that there are data bytes fewer than the receive trigger set number in SCAFRDR, and no further data will arrive at least 15 etu after the stop bit of the last data received. This bit setting is valid only in asynchronous mode. 0: Reception is in progress or has ended normally and there is no receive data left in SCAFRDR [Clearing conditions] (initial value) • Power-on reset or manual reset • When all the receive data in SCAFRDR has been read, and 0 is written to DR after reading DR = 1 1: No further receive data has arrived [Setting condition] • When SCAFRDR contains data bytes fewer than the receive trigger set number, and no further data will arrive at least 15 etu after the stop bit of the last data received* Note: * Corresponds to 1.5 frame time in 8-bit one-stop-bit format. etu: Elementary time unit (time for transfer of 1 bit)

Note: * Only 0 can be written for clearing the flags.

21.3.9 Bit Rate Register (SCABRR)

SCABRR is an 8-bit readable/writable register that sets the serial transfer bit rate in accordance with the baud rate generator operating clock selected by bits CKS1 and CKS0 in SCASMR.

Bit:	7	6	5	4	3	2	1	0
	SCBRD[7:0]							
Initial value:	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	SCBRD[7:0]	H'FF	R/W	Bit Rate

The SCABRR setting is found by using the following equations.

(1) Asynchronous Mode:

When the sampling rate is 1/16,

$$N = \frac{SUB\phi}{16 \times 2^{2n} \times B} \times 10^6 - 1$$

When the sampling rate is 1/5,

$$N = \frac{SUB\phi}{5 \times 2^{2n} \times B} \times 10^6 - 1$$

When the sampling rate is 1/11,

$$N = \frac{SUB\phi}{11 \times 2^{2n} \times B} \times 10^6 - 1$$

When the sampling rate is 1/13,

$$N = \frac{SUB\phi}{13 \times 2^{2n} \times B} \times 10^6 - 1$$

When the sampling rate is 1/27,

$$N = \frac{SUB\phi}{27 \times 2^{2n} \times B} \times 10^6 - 1$$

(2) Clocked Synchronous Mode:

$$N = \frac{SUB\phi}{2 \times 2^{2n-1} \times B} \times 10^6 - 1$$

Where B: Bit rate (bits/s)

N: SCABRR setting for baud rate generator

Asynchronous mode ($0 \leq N \leq 255$)

Clocked synchronous mode ($1 \leq N \leq 255$)

SUBϕ: Subclock frequency (MHz)

n: Baud rate generator input clock (n = 0 to 3)

(See the table below for the relation between n and the clock.)

Table 21.4 SCASMR Settings

		SCASMR Setting
n	**Clock**	**CKS[1:0]**
0	SUBϕ	00
1	SUBϕ/4	01
2	SUBϕ/16	10
3	SUBϕ/64	11

The bit rate error in asynchronous mode is found by using the following equations.

When the sampling rate is 1/16,

$$\text{Error (\%)} = \left(\frac{SUB\phi \times 10^6}{(N + 1) \times 16 \times 2^{2n} \times B} - 1 \right) \times 100$$

When the sampling rate is 1/5,

$$\text{Error (\%)} = \left(\frac{SUB\phi \times 10^6}{(N + 1) \times 5 \times 2^{2n} \times B} - 1 \right) \times 100$$

When the sampling rate is 1/11,

$$\text{Error (\%)} = \left(\frac{SUB\phi \times 10^6}{(N + 1) \times 11 \times 2^{2n} \times B} - 1 \right) \times 100$$

When the sampling rate is 1/13,

$$\text{Error (\%)} = \left(\frac{\text{SUB}\phi \times 10^6}{(\text{N} + 1) \times 13 \times 2^{2n} \times \text{B}} - 1 \right) \times 100$$

When the sampling rate is 1/27,

$$\text{Error (\%)} = \left(\frac{\text{SUB}\phi \times 10^6}{(\text{N} + 1) \times 27 \times 2^{2n} \times \text{B}} - 1 \right) \times 100$$

21.3.10 FIFO Control Register (SCAFCR)

SCAFCR is a 16-bit readable/writable register that clears all data and sets the trigger data number for the transmit and receive FIFO registers, and also contains a loopback test enable bit.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TSE	TCRST	—	—	—	RSTRG[2:0]			RTRG[1:0]		TTRG[1:0]		MCE	TFRST	RFRST	LOOP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	TSE	0	R/W	Transmit Data Stop Enable Enables or disables the transmit data stop function. 0: Transmit data stop function disabled 1: Transmit data stop function enabled
14	TCRST	0	R/W	Transmit Count Reset Clears the transmit count to 0. This bit is valid only when the transmit data stop function is used. 0: Transmit count reset disabled* 1: Transmit count reset enabled (clearing to 0) Note: * Transmit count reset (clearing to 0) is performed at a power-on reset or module reset.
13 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
10 to 8	RSTRG[2:0]	000	R/W	RTS_N Output Active Trigger The RTS_N signal becomes high when the number of receive data stored in SCAFRDR reaches the trigger number shown below. 000: 63 001: 1 010: 8 011: 16 100: 32 101: 48 110: 54 111: 60
7, 6	RTRG[1:0]	00	R/W	Receive FIFO Data Number Trigger Set the number of receive data bytes that sets the RDF flag in SCASSR. The RDF flag is set when the number of receive data bytes in SCAFRDR is equal to or greater than the trigger set number shown below. 00: 1 01: 16 10: 32 11: 48

Bit	Bit Name	Initial Value	R/W	Description
5, 4	TTRG[1:0]	00	R/W	Transmit FIFO Data Number Trigger Set the number of remaining transmit data bytes that sets the TDFE flag in SCASSR. The TDFE flag is set when, as the result of a transmit operation, the number of transmit data bytes in SCAFTDR falls to or below the trigger set number shown below. 00: 32 (32) 01: 16 (49) 10: 2 (62) 11: 0 (64) Note: The values in parentheses are the number of empty bytes in SCAFTDR when the flag is set.
3	MCE	0	R/W	Modem Control Enable Enables the CTS_N and RTS_N modem control signals. 0: Modem signals disabled* 1: Modem signals enabled Note: * CTS_N is fixed at active-0 regardless of the input value, and RTS_N output is also fixed at 0. Note: The MCE bits of SCIFA4 and SCIFA5 are disabeled.
2	TFRST	0	R/W	Transmit FIFO Data Register Reset Invalidates the transmit data in SCAFTDR and resets it to the empty state. 0: Reset operation disabled* 1: Reset operation enabled Note: * A reset operation is performed at a power-on reset or manual reset.
1	RFRST	0	R/W	Receive FIFO Data Register Reset Invalidates the receive data in SCAFRDR and resets it to the empty state. 0: Reset operation disabled* 1: Reset operation enabled Note: * A reset operation is performed in the event of

a power-on reset or manual reset.

Bit	Bit Name	Initial Value	R/W	Description
0	LOOP	0	R/W	Loopback Test Internally connects the transmit output pin (TxD) to receive input pin (RxD) and RTS_N pin to CTS_N pin, enabling loopback testing. 0: Loopback test disabled 1: Loopback test enabled

21.3.11 FIFO Data Count Register (SCAFDR)

SCAFDR is a 16-bit read-only register that indicates the number of data bytes stored in SCAFTDR and SCAFRDR. The T6 to T0 bits show the number of transmit data bytes in SCAFTDR, and the R6 to R0 bits show the number of receive data bytes in SCAFRDR.

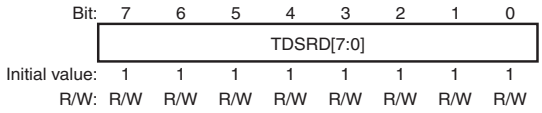
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	T[6:0]							—	R[6:0]						
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14 to 8	T[6:0]	H'00	R	These bits show the number of untransmitted data bytes in SCAFTDR. A value of H'00 means that there is no transmit data, and a value of H'40 means that SCAFTDR is full of transmit data.
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6 to 0	R[6:0]	H'00	R	These bits show the number of receive data bytes in SCAFRDR. A value of H'00 means that there is no receive data, and a value of H'40 means that SCAFRDR is full of receive data.

21.3.12 Transmit Data Stop Register (SCATDSR)

SCATDSR is an 8-bit readable/writable register that sets the number of transmit data bytes. SCATDSR is valid only when the TSE bit in SCAFCR is enabled. Transmit operation is stopped when the number of data bytes set in SCATDSR is transmitted. The setting value should be H'00 (one byte) to H'FF (256 bytes).

SCATDSR is initialized to H'FF.

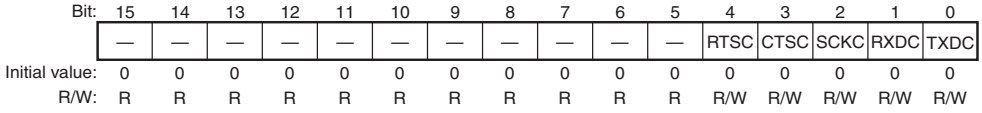


Bit	Bit Name	Initial Value	R/W	Description
7 to 0	TDSRD[7:0]	H'FF	R/W	Transmit Data Stop Setting

21.3.13 Serial Port Control Register (SCAPCR)

SCAPCR is a 16-bit readable/writable register. This register specifies whether the TXD, SCK and RTS_N pins function as output ports or the TXD, SCK and RTS_N pins, respectively. It also specifies whether the RXD and CTS_N pins function as input ports or the RXD and CTS_N pins, respectively.

SCAPCR is initialized to H'0000. This register function is valid only when the SCIFA pin function is selected through the pin function controller (PFC).



Bit	Bit Name	Initial Value	R/W	Description
15 to 5	—	H'000	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
4	RTSC	0	R/W	Selects the RTS_N pin function. 0: The RTS_N pin functions as the RTS_N pin. 1: The RTS_N pin functions as an output port.
3	CTSC	0	R/W	Selects the CTS_N pin function. 0: The CTS_N pin functions as the CTS_N pin. 1: The CTS_N pin functions as an input port.
2	SCKC	0	R/W	Selects the SCK pin function. 0: The SCK pin functions as the SCK pin. 1: The SCK pin functions as an output port.
1	RXDC	0	R/W	Selects the RXD pin function. 0: The RXD pin functions as the RXD pin. 1: The RXD pin functions as an input port.
0	TXDC	0	R/W	Selects the TXD pin function. 0: The TXD pin functions as the TXD pin. 1: The TXD pin functions as an output port.

21.3.14 Serial Port Data Register (SCAPDR)

SCAPDR is a 16-bit readable/writable register. This register specifies data output to the TXD, SCK and RTS_N pins when the SCIFA pin function is selected by SCAPCR. It also specifies the pin level of the RXD and CTS_N pins.

SCAPCR is initialized to H'0000. This register function is valid only when the SCIFA pin function is selected through the pin function controller (PFC).

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	RTSD	CTSD	SCKD	RXDD	TXDD
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	W	R	W	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 5	—	H'000	R	Reserved These bits are always read as 0. The write value should always be 0.
4	RTSD	0	W	Specifies data output to the RTS_N pin. 0: Outputs 0. 1: Outputs 1.
3	CTSD	Undefined	R	Specifies the CTS_N pin level. 0: CTS_N pin level is 0. 1: CTS_N pin level is 1.
2	SCKD	0	W	Specifies data output to the SCK pin. 0: Outputs 0. 1: Outputs 1.
1	RXDD	Undefined	R	Specifies the RXD pin level. 0: RXD pin level is 0. 1: RXD pin level is 1.
0	TXDD	0	R/W	Specifies data output to the TXD pin. 0: Outputs 0. 1: Outputs 1.

21.4 Operation

21.4.1 Overview

SCIFA supports serial communications in asynchronous mode, in which synchronization is achieved character by character, and in clocked synchronous mode, in which synchronization is achieved with clock pulses. 64-stage FIFO buffers are provided for both transmission and reception, reducing the CPU overhead and enabling continuous communications.

21.4.2 Asynchronous Mode

In the asynchronous mode, the transfer format is selected by the setting in SCASMR as shown in Table 21.5. Features in this mode are as follows.

- Data length: 7 or 8 bits
- The addition of parity (even, odd or none) and the choice of stop-bit length (1 or 2 bits), along with the data length, determine the transfer format and character length.
- Receive error detection: Framing, parity, and overrun errors, receive-FIFO-data-full, receive-data-ready, and breaks.
- Independent indications of the number of data stored in the registers of the transmit and receive FIFOs.
- Serial clock source: Internal clock signal generated by the baud-rate generator.

Table 21.5 SCASMR Settings for Serial Transfer Format Selection

SCASMR Settings					SCIFA Transfer Format		
Bit 7: C/$\overline{A}$	**Bit 6: CHR**	**Bit 5: PE**	**Bit 3: STOP**	**Mode**	**Data Length**	**Parity Bit**	**Stop Bit Length**
0	0	0	0	Asynchronous mode	8-bit data	No	1 bit
			1				2 bits
		1	0			Yes	1 bit
			1				2 bits
	1	0	0		7-bit data	No	1 bit
			1				2 bits
		1	0			Yes	1 bit
			1				2 bits
1	*	*	*	Clocked synchronous mode	8-bit data	No	No

Note: * Don't care.

21.4.3 Serial Operation in Asynchronous Mode

(1) Data Transfer Format

Table 21.6 shows the transfer formats that can be used in asynchronous mode. Any of eight transfer formats can be selected according to the SCASMR settings.

Table 21.6 Serial Transfer Formats

SCASMR Settings			Serial Transfer Format and Frame Length											
CHR	PE	STOP	1	2	3	4	5	6	7	8	9	10	11	12
0	0	0	S	8-bit data								STOP		
		1	S	8-bit data								STOP	STOP	
	1	0	S	8-bit data								P	STOP	
		1	S	8-bit data								P	STOP	STOP
1	0	0	S	7-bit data							STOP			
		1	S	7-bit data							STOP	STOP		
	1	0	S	7-bit data							P	STOP		
		1	S	7-bit data							P	STOP	STOP	

[Legend]
S: Start bit
STOP: Stop bit
P: Parity bit

(2) Clock

An internal clock signal generated by the on-chip baud-rate generator provides the transfer clock for SCIFA.

(3) Data Transfer Operations:

1. SCIFA initialization

   Before transmitting and receiving data, it is necessary to clear the TE and RE bits in SCASCR to 0, then initialize SCIFA as described below.

   When the transfer format, etc., is changed, the TE and RE bits must be cleared to 0 before making the change using the following procedure. When the TE bit is cleared to 0, SCATSR is initialized. Note that clearing the TE and RE bits to 0 does not change the contents of SCASSR, SCAFTDR, or SCAFRDR. The TE bit should be cleared to 0 after all transmit data has been sent and the TEND bit in SCASSR has been set to 1. Clearing to 0 can also be performed during transmission, but the data lines that transmit the data will go to the high-impedance state after the clearance. Before setting TE to 1 again to start transmission, the TFRST bit in SCAFCR should first be set to 1 to reset SCAFTDR.

Figure 21.2 shows a sample SCIFA initialization flowchart.

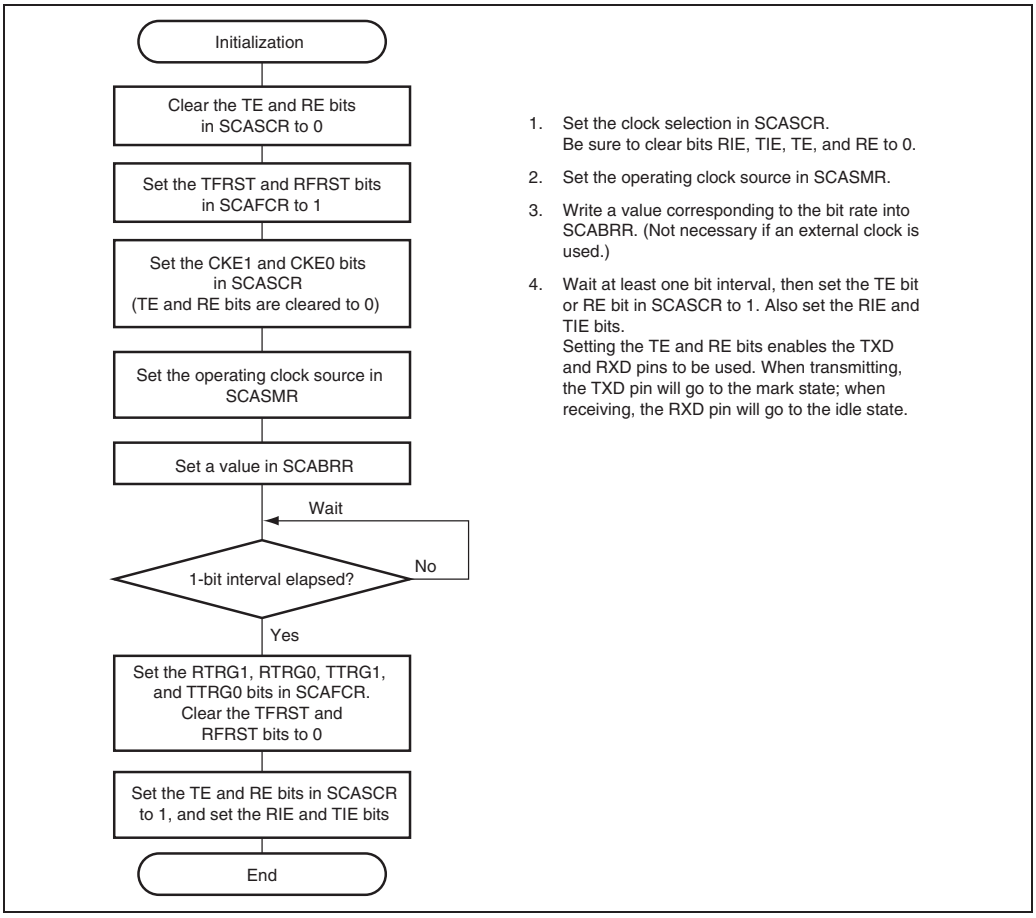


Figure 21.2 Sample SCIFA Initialization Flowchart

2. Serial data transmission

   Figure 21.3 shows a sample flowchart for serial transmission.

   Use the following procedure for serial data transmission after enabling SCIFA for transmission.

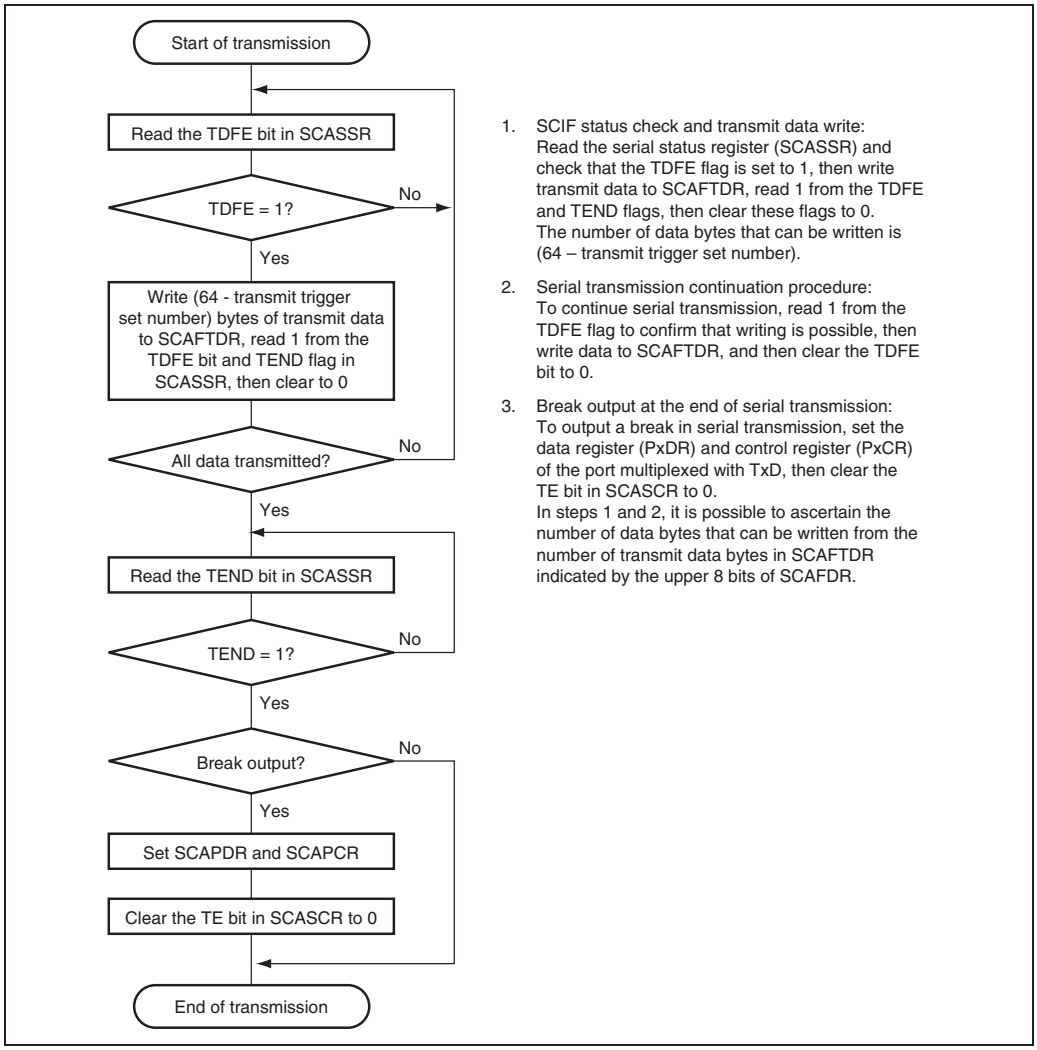


Figure 21.3 Sample Serial Transmission Flowchart

In serial transmission, SCIFA operates as described below.

A. When data is written into SCAFTDR, SCIFA transfers the data from SCAFTDR to SCATSR and starts transmitting. Confirm that the TDFE flag in SCASSR is set to 1 before writing transmit data to SCAFTDR. The number of data bytes that can be written is not less than (64 – transmit trigger set number).

B. When data is transferred from SCAFTDR to SCATSR and transmission is started, consecutive transmit operations are performed until there is no transmit data left in SCAFTDR. When the number of transmit data bytes in SCAFTDR falls to or below the transmit trigger number set in SCAFCR, the TDFE flag is set. If the TIE bit in SCASCR is set to 1 at this time, a transmit-FIFO-data-empty interrupt (TXI) request is generated.

   When the transmit data stop function is used and the number of data bytes set in SCATDSR is matched, transmit operation is stopped, and the TSF flag in SCASSR is set. If the TSIE bit in SCASCR is set to 1, a transmit-data-stop-interrupt (TDI) request is generated. The vectors of TXI and TDI are the same.

   The serial transmit data is sent from the TxD pin in the following order.

   a. Start bit: One logic-0 bit is output.
   b. Transmit data: 8-bit or 7-bit data is output in LSB-first order.
   c. Parity bit: One parity bit (even or odd parity) is output.
   d. A format in which a parity bit is not output can also be selected.
   e. Stop bit(s): One or two logic-1 bits (stop bits) are output.
   f. Mark state: Output of 1 is continued until the start bit is sent to start the next transmission.

C. SCIFA checks the SCAFTDR transmit data at the timing for sending the stop bit. If data is present, the data is transferred from SCAFTDR to SCATSR, the stop bit is sent, and then serial transmission of the next frame is started.

   If there is no transmit data, the TEND flag in SCASSR is set to 1, the stop bit is sent, and then the line goes to the mark state in which 1 is output.

Figure 21.4 shows an example of the operation for transmission in asynchronous mode.

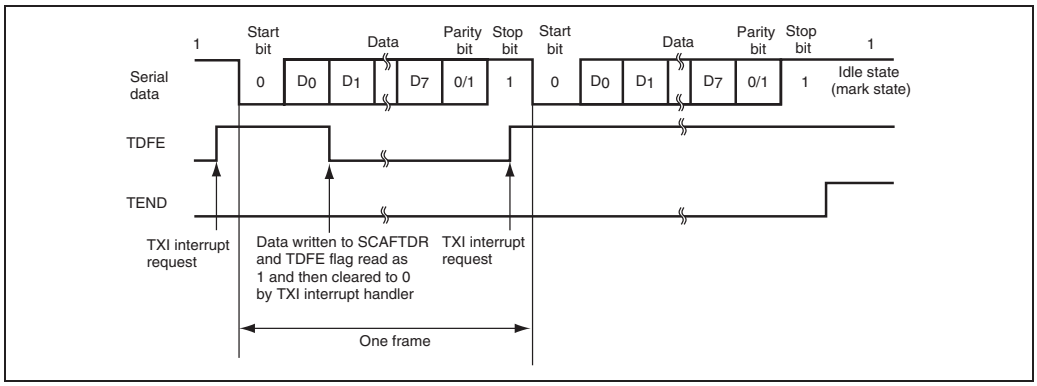


Figure 21.4 Example of Transmit Operation (Example with 8-Bit Data, Parity, One Stop Bit)

- Transmit data stop function
  When (value in SCATDSR + 1) is matched with the number of transmitted data bytes, this function stops the transmit operation. Interrupts can be generated and the DMAC can be activated by setting the TSIE bit (interrupt enable bit) to 1.

Figure 21.5 shows an example of operation for the transmit data stop function.

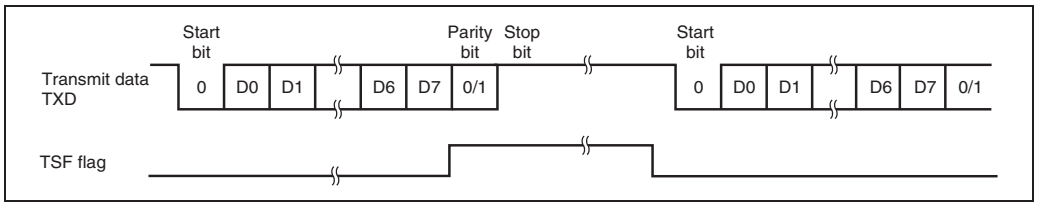


Figure 21.5 Example of Transmit Data Stop Function

Figure 21.6 shows a flowchart for the transmit data stop function.

Before using the transmit data stop function, set the TCRST bit in SCAFCR to 1 to clear the transmit counter. After modifying SCASSR, always confirm that data has been updated.

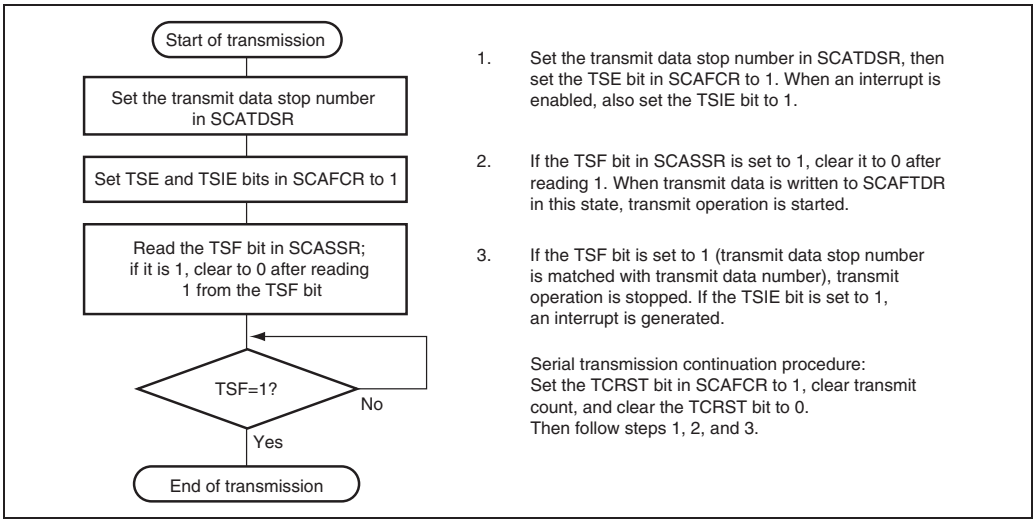


Figure 21.6 Transmit Data Stop Function Flowchart

3. Serial data reception

Figures 19.7 and 19.8 show sample flowcharts for serial reception.

Use the following procedure for serial data reception after enabling SCIFA for reception.

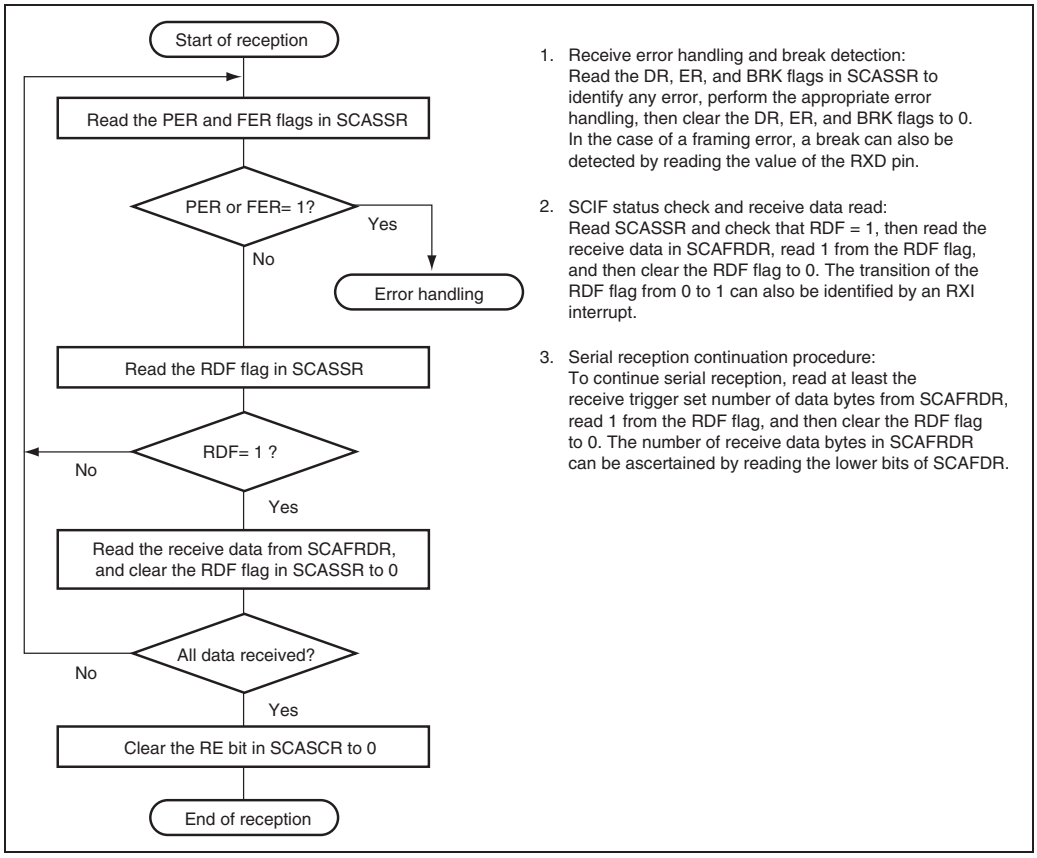


Figure 21.7 Sample Serial Reception Flowchart (1)

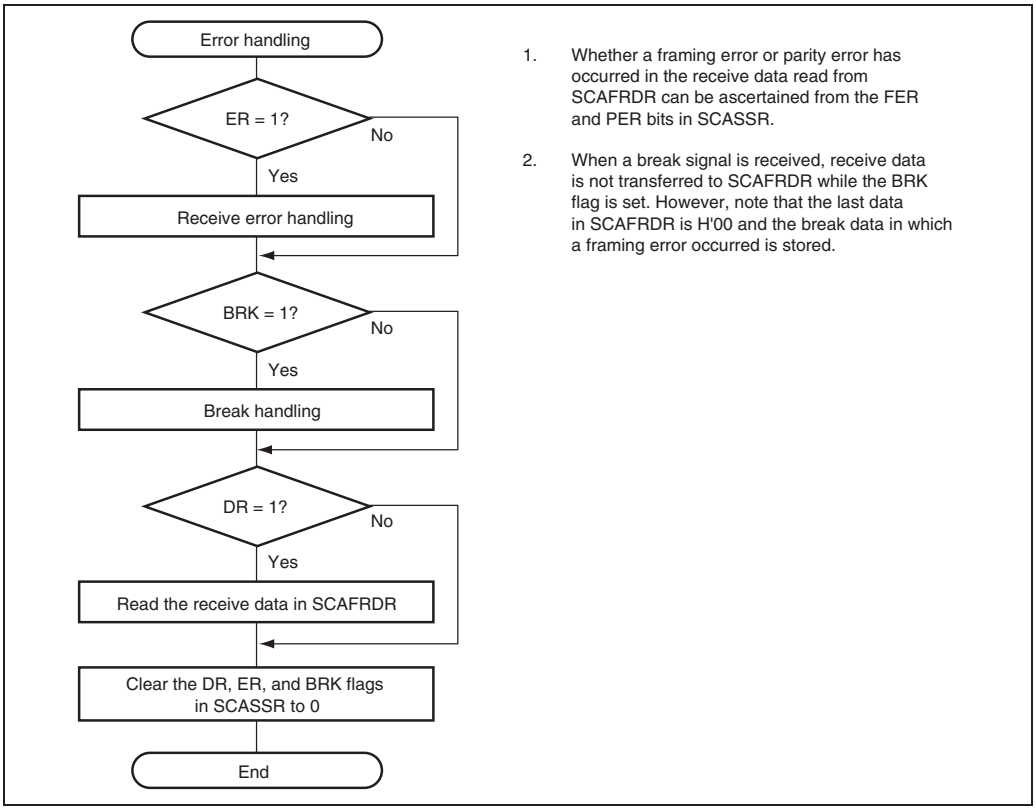


Figure 21.8 Sample Serial Reception Flowchart (2)

In serial reception, SCIFA operates as described below.

A. SCIFA monitors the communication line, and if a 0 start bit is detected, performs internal synchronization and starts reception.

B. The received data is stored in SCARSR in LSB-to-MSB order.

C. The parity bit and stop bit are received.

After receiving these bits, SCIFA carries out the following checks.

a. Stop bit check: SCIFA checks to see if the value in the stop bit position is 1. If the two-stop-bit setting has been made, only the value in the first stop-bit position is checked.

b. SCIFA checks whether received data can be transferred from SCARSR to SCAFRDR.

c. Break check: SCIFA checks to confirm that the BRK flag is 0, indicating that the break state has not been set.

If all the above checks are passed, the receive data is stored in SCAFRDR.

Note: Reception continues when a receive error (a framing error or parity error) occurs.

D. If the RIE bit in SCASCR is set to 1 when the RDF flag changes to 1, a receive-FIFO-data-full interrupt (RXI) request is generated.

If the ERIE bit in SCASCR is set to 1 when the ER flag changes to 1, a receive-error interrupt (ERI) request is generated.

If the BRIE bit in SCASCR is set to 1 when the BRK flag changes to 1, a break reception interrupt (BRI) request is generated.

If the DRIE bit in SCASCR is set to 1 when the DR flag changes to 1, a receive-data-ready interrupt (DRI) request is generated.

The vectors of each interrupt source are the same.

Figure 21.9 shows an example of the operation for reception in asynchronous mode.

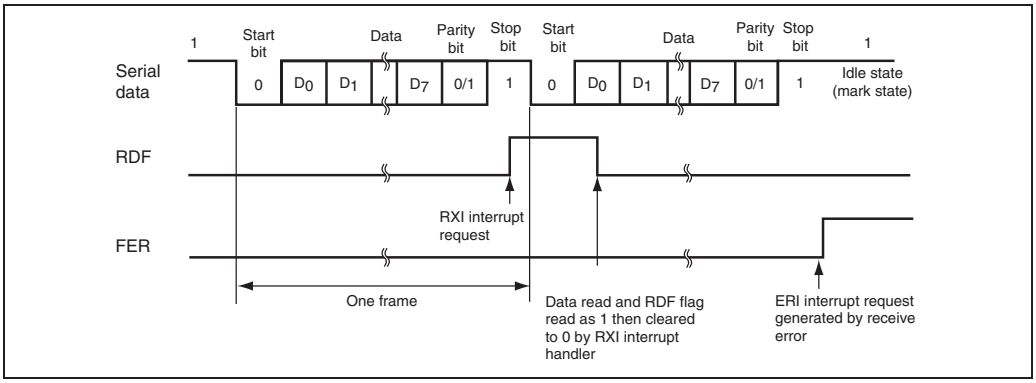


Figure 21.9 Example of SCIFA Receive Operation (Example with 8-Bit Data, Parity, One Stop Bit)

SCIFA has a modem function that allows the stoppage and resumption of transmission according to the input value of CTS_N. Setting CTS_N to 1places the transmission line in the mark state after transmission of the current frame. When CTS_N is set to 0, the next frame for transmission is output, with a start bit as its leader.

Figure 21.10 shows an example of the operation of CTS_N control.

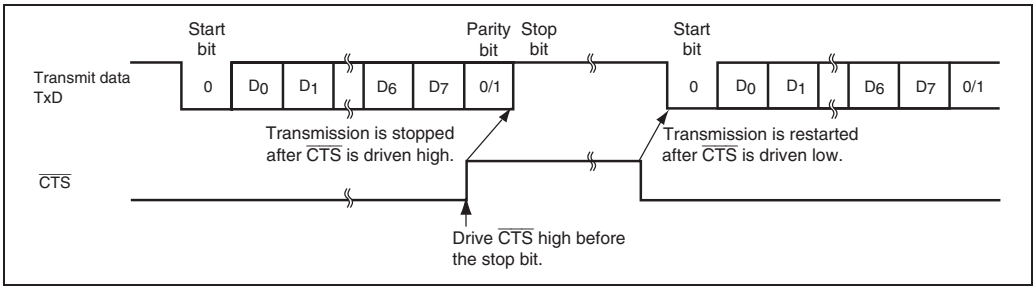


Figure 21.10 Example of CTS_N Control Operation

The RTS_N signal is driven high when the modem function is in use and the received data stored in the receive FIFO register (SCAFRDR) equals or exceeds the number of the RTS_N output triggers.

Figure 21.11 shows an example of the operation for RTS_N control.

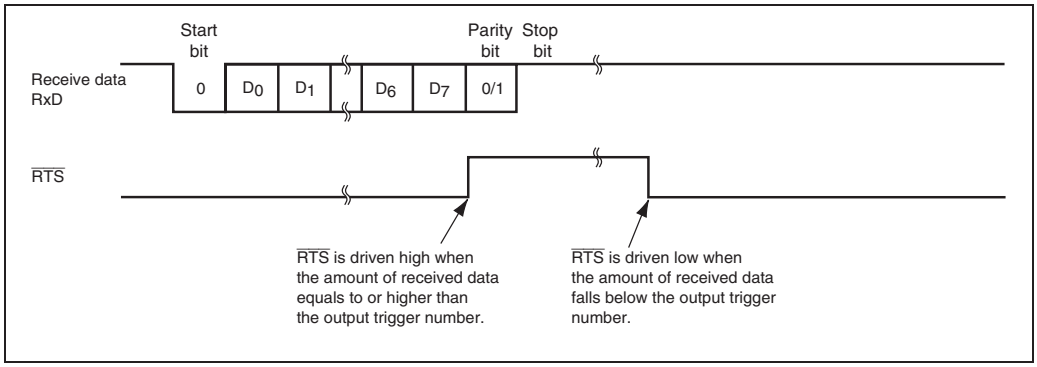


Figure 21.11 Example of RTS_N Control Operation

21.4.4 Operation in Clocked Synchronous Mode

Clocked synchronous mode, in which data is transmitted or received in synchronization with clock pulses, is suitable for fast serial communications.

Since the transmitter and receiver are independent units in SCIFA, full-duplex communications can be achieved by sharing the clock. Both the transmitter and receiver have a 64-stage FIFO buffer structure, so that data can be read or written during transmission or reception, enabling continuous data transfer and reception.

Through the setting of the CKEDG bit, the format for clocked synchronous communications can be selected.

Figures 19.12 and 19.13 show the format for clocked synchronous communications.

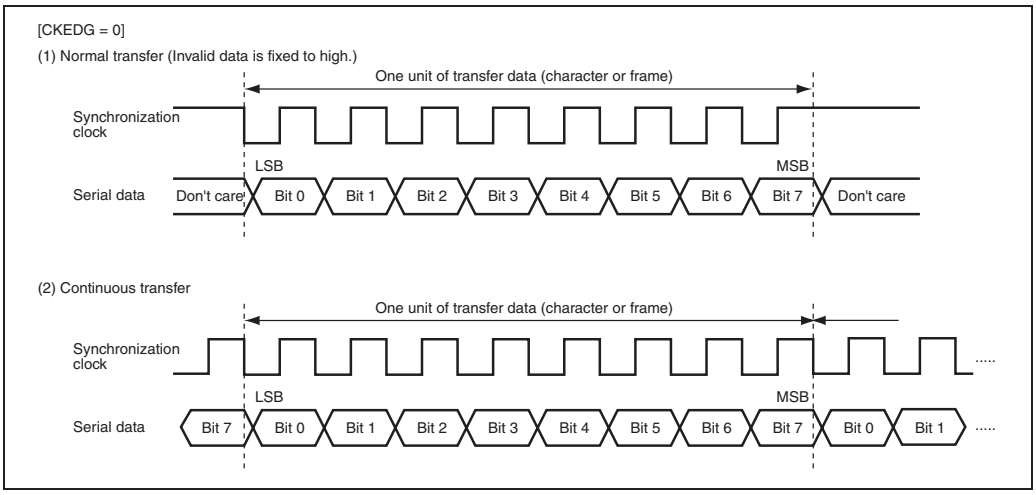


Figure 21.12 Data Format in Clocked Synchronous Communications (CKEDG = 0)

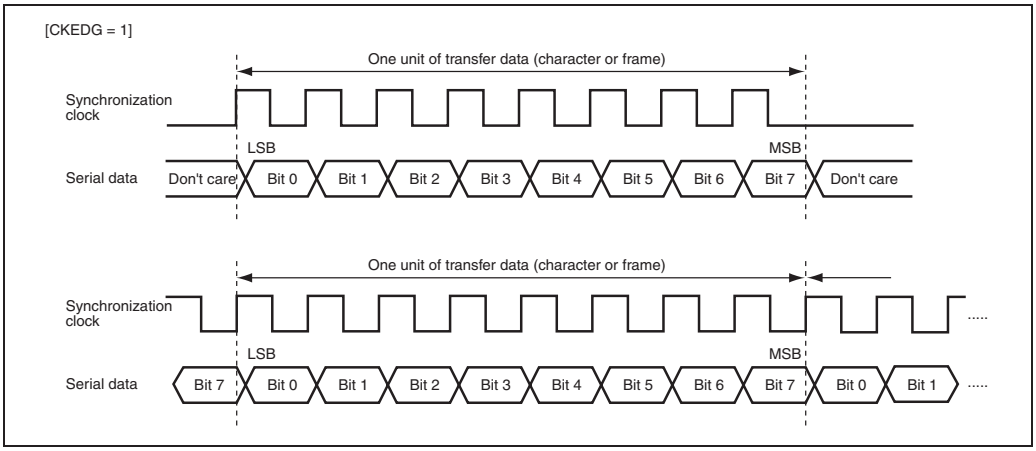


Figure 21.13 Data Format in Clocked Synchronous Communications (CKEDG = 1)

In clock synchronous serial communications, the data selected by the CKEDG bit on the communications line latched on one edge of the synchronization clock signal and output until the next edge. Accuracy of data is guaranteed on the next edge (i.e. that in the opposite direction to the latching edge).

In serial communications, each character is output starting with the LSB and ending with the MSB. After the MSB is output, the communications line remains in the state of the last bit.

Data is received on the opposite edge to that on which data is output.

(1) Data Transfer Format

A fixed 8-bit data format is used. No parity bit can be added.

(2) Clock

An internal clock signal generated by the on-chip baud-rate generator provides the transfer clock for SCIFA. For details on SCIFA clock source selection, see Table 21.5.

(3) SCIFA Initialization (Clocked Synchronous Mode)

Before transmitting and receiving data, it is necessary to clear the TE and RE bits in SCSCR to 0, then initialize SCIFA as described below.

When changing the operating mode or transfer format, etc., the TE and RE bits must be cleared to 0 before making the change using the following procedure. When the TE bit is cleared to 0, SCTSR is initialized. Note that clearing the RE bit to 0 does not initialize the RDF, PER, FER, or ORER flag state or change the contents of SCFRDR.

Figure 21.14 shows a sample SCIFA initialization flowchart.

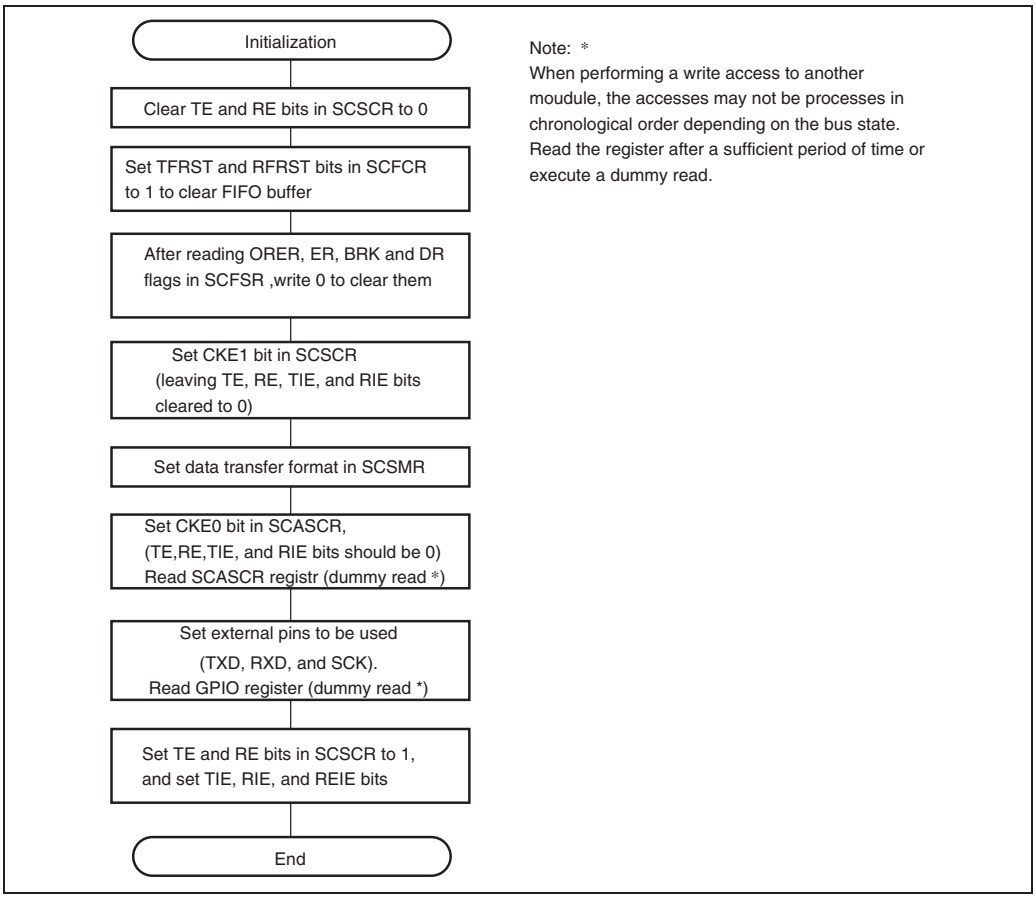


Figure 21.14 Sample Serial Transmission Flowchart

(4) Serial Data Transmission (Clocked Synchronous Mode)

Figure 21.15 shows a sample flowchart for serial transmission.

Use the following procedure for serial data transmission after enabling SCIFA for transmission.

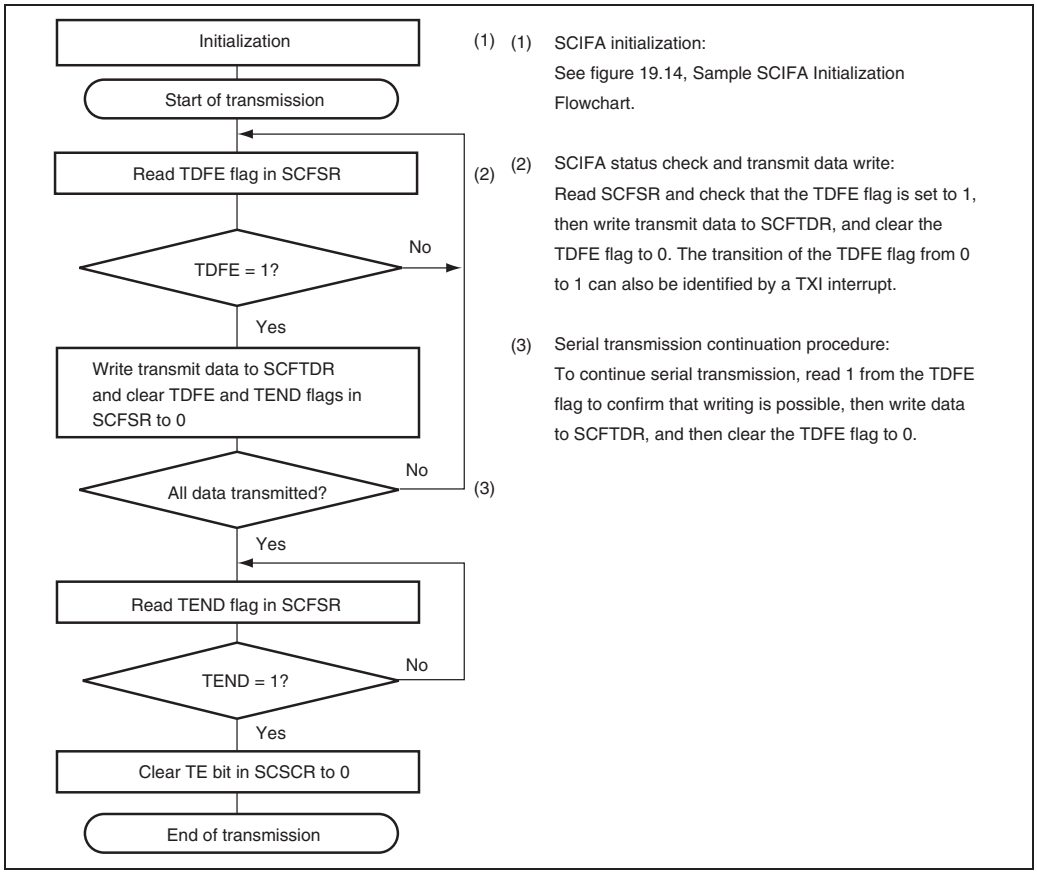


Figure 21.15 Sample Serial Transmission Flowchart

In serial transmission, SCIFA operates as described below.

1. When data is written into SCFTDR, SCIFA transfers data from SCFTDR to SCTSR and starts transmitting. Confirm that the TDFE flag in SCFSR is set to 1 before writing transmit data to SCFTDR. The number of data bytes that can be written is at least 16 – (transmit trigger set number).
2. When data is transferred from SCFTDR to SCTSR and transmission is started, consecutive transmit operations are performed until there is no transmit data left in SCFTDR. When the number of transmit data bytes in SCFTDR falls to or below the transmit trigger number set in SCFCR, the TDFE flag is set. If the TIE bit in SCSCR is set to 1 at this time, a transmit-FIFO-data-empty interrupt (TXI) request is generated.

   When the external clock is selected, data is output in synchronization with the input clock.

   The serial transmit data is sent from the TXD pin in the LSB-first order.
3. SCIFA checks the SCFTDR transmit data at the timing for sending the last bit. If data is present, the data is transferred from SCFTDR to SCTSR, and then serial transmission of the next frame is started. If there is no transmit data, the TEND flag in SCFSR is set to 1 after the last bit is sent, and the transmit data pin (TXD pin) retains the output state of the last bit.

Figure 21.16 shows an example of the operation for transmission in clocked synchronous mode.

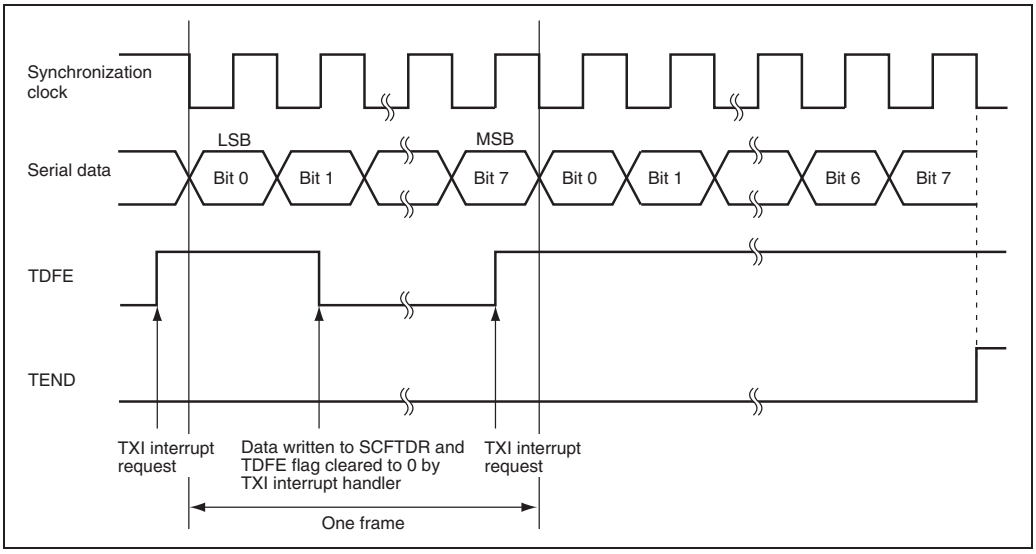


Figure 21.16 Sample SCIFA Transmission Operation in Clocked Synchronous Mode

(5) Serial Data Reception (Clocked Synchronous Mode)

Figures 19.17 and 19.18 show sample flowcharts for serial reception.

Use the following procedure for serial data reception after enabling SCIFA for reception.

When switching the operating mode from asynchronous mode to clocked synchronous mode without initializing SCIFA, make sure that the ORER flag in SCLSR, and PERC and FERC flags in SCLSR are cleared to 0.

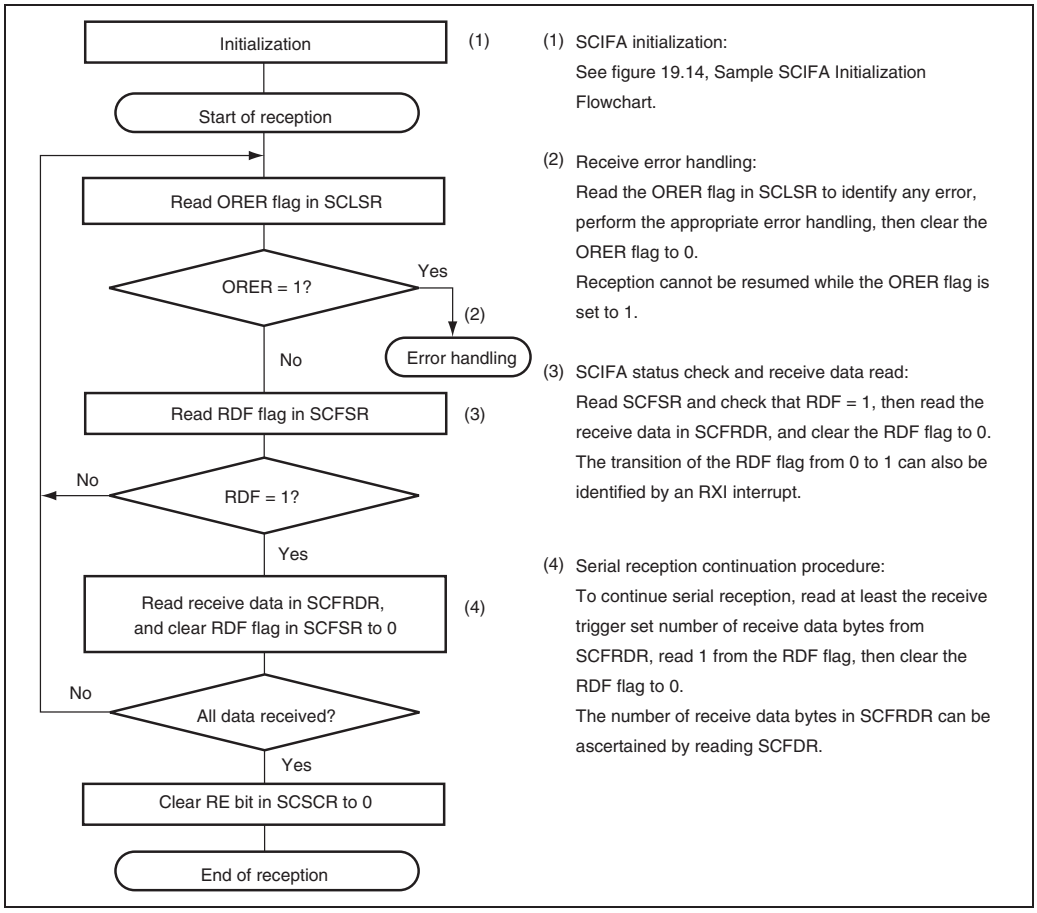


Figure 21.17 Sample Serial Reception Flowchart (1)

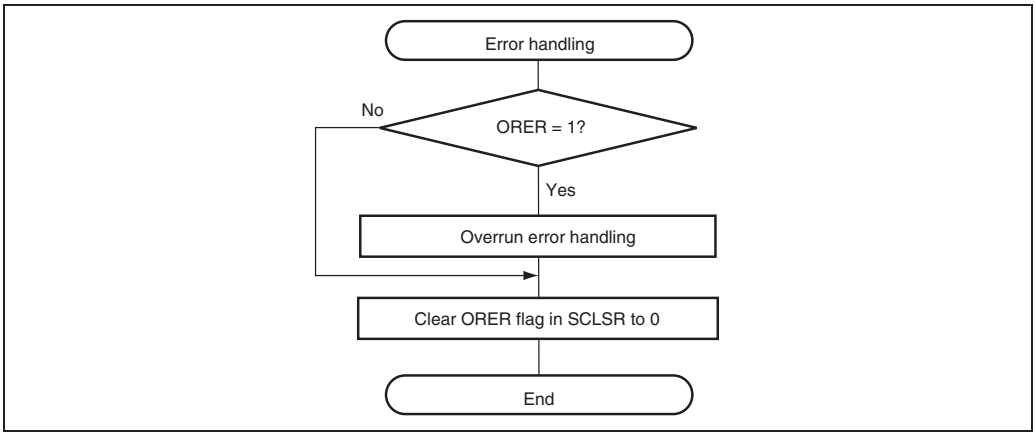


Figure 21.18 Sample Serial Reception Flowchart (2)

In serial reception, SCIFA operates as described below.

1. SCIFA is initialized internally in synchronization with the output of the synchronization clock.
2. The received data is stored in SCRSR in LSB-to-MSB order.
   After receiving the data, SCIFA checks whether the receive data can be transferred from SCRSR to SCFRDR. If this check is passed, the receive data is stored in SCFRDR. If an overrun error is detected in the error check, reception cannot continue.
3. If the RIE bit in SCSCR is set to 1 when the RDF flag changes to 1, a receive-FIFO-data-full interrupt (RXI) request is generated.
   If the RIE or REIE bit in SCSCR is set to 1 when the ORER flag changes to 1, a break interrupt (BRI) request is generated.

Figure 21.19 shows an example of the operation for reception in clocked synchronous mode.

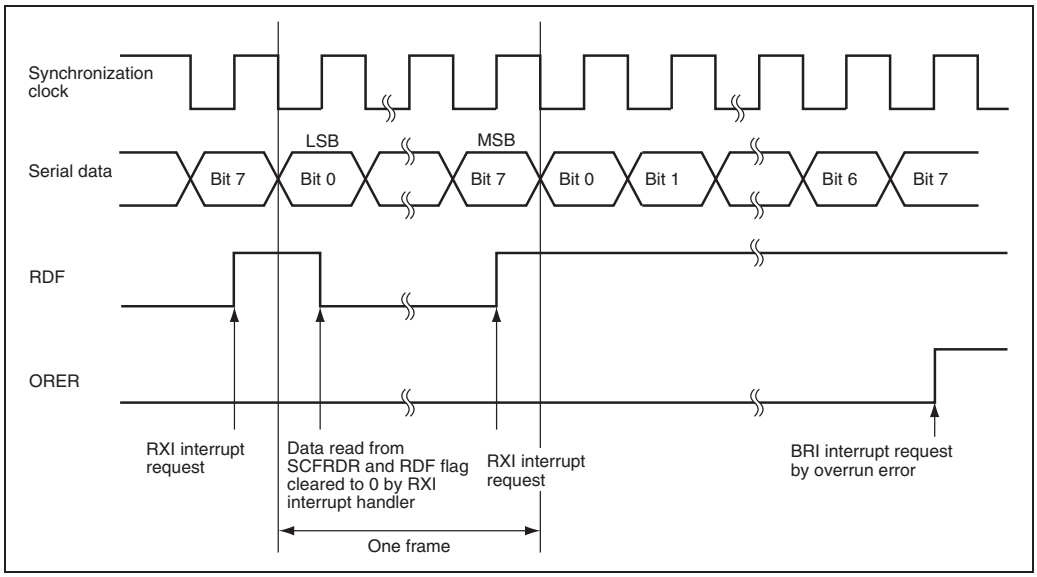


Figure 21.19 Sample SCIFA Reception Operation in Clocked Synchronous Mode

(6) Simultaneous Serial Data Transmission and Reception (Clocked Synchronous Mode)

Figure 21.20 shows a sample flowchart for simultaneous serial data transmission and reception.

Use the following procedure for simultaneous serial transmission and reception after enabling SCIFA for both the transmission and reception.

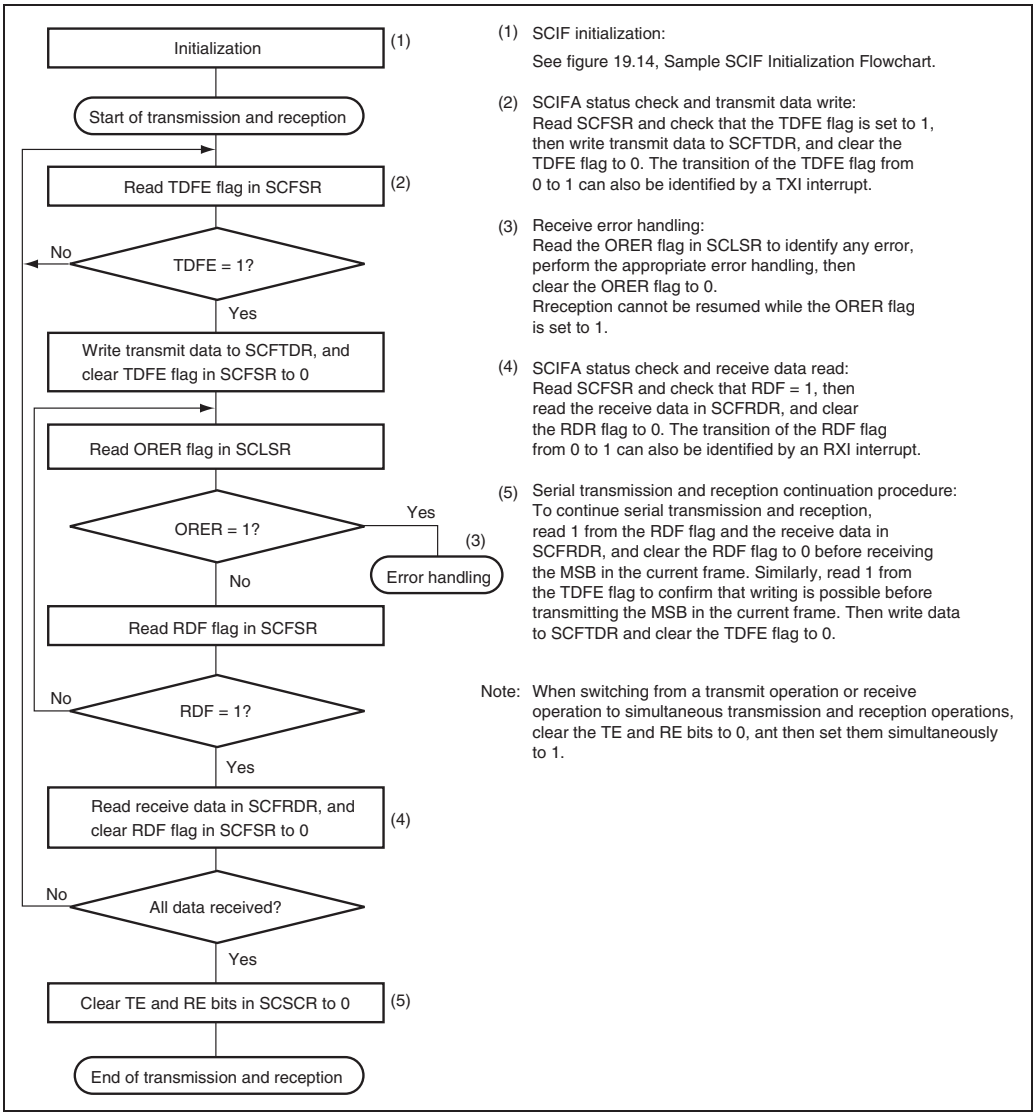


Figure 21.20 Sample Simultaneous Serial Transmission and Reception Flowchart

21.5 SCIFA Interrupt Sources and DMAC

SCIFA supports seven interrupts: transmit-FIFO-data-empty (TXI), transmit-data-stop (TDI), receive-error (ERI), receive-FIFO-data-full (RXI), break (BRI), receive-data-ready (DRI),and transmit-end(TEND). The vectors of each interrupt source are the same.

Table 21.7 shows the interrupt sources. The TIE, RIE, ERIE, BRIE, DRIE, TSIE,and TENDE bits in SCASCR are used to enable or disable the respective interrupt sources.

If the TDFE flag in SCASSR is set to 1, a TXI interrupt request is generated. When the TSF flag in SCASSR is set to 1, a TDI interrupt request is generated. The DMAC can be activated and data transfer performed on generation of TXI and TDI interrupt requests. When data exceeding the transmit trigger set number is written to SCAFTDR by the DMAC, the DMAC transfer request is automatically cleared to 0. The DMAC requests of TXI and TDI are the same.

When the RDF flag in SCASSR is set to 1, an RXI interrupt request is generated. The DMAC can be activated and data transfer performed on generation of an RXI interrupt request. When receive data in SCAFRDR is read by the DMAC until the amount left is less than the receive trigger set number, the DMAC transfer request is automatically cleared to 0.

When using the DMAC for transmission/reception, set the DMAC to the DMAC transfer enabled state before making the SCIFA settings. Transmission/reception is complete when the DMA transfer is terminated.

When the TEND flag in SCASSR is set to 1,the ER flag in SCASSR is set to 1, the BRK flag in SCASSR is set to 1, the DR flag in SCASSR is set to 1, or the TSF flag in SCASSR is set to 1, an interrupt request is generated. Note that the vectors of each interrupt source are the same.

Table 21.7 SCIFA Interrupt Sources

Interrupt Source Type	DMAC Activation
Interrupt initiated by receive error flag (ER) break flag (BRK) or transmit-end(TEND)	Not possible
Interrupt initiated by receive FIFO data full flag (RDF) or receive data ready flag (DR)	Possible*1
Interrupt initiated by transmit FIFO data empty flag (TDFE) or transmit data stop flag (TSF)	Possible*2

Notes: 1. The DMAC can only be activated by an interrupt request initiated by the receive FIFO data full flag (RDF).
2. The DMAC can only be activated by an interrupt request initiated by the transmit FIFO data empty flag (TDFE).

21.6 Usage Notes

Note the following when using SCIFA.

(1) SCAFTDR Writing and the TDFE Flag

The TDFE flag in SCASSR is set when the number of transmit data bytes written in SCAFTDR has fallen to or below the transmit trigger number set by bits TTRG1 and TTRG0 in SCAFCR. After TDFE is set, transmit data up to the number of empty bytes in SCAFTDR can be written, allowing efficient continuous transmission.

However, if the number of data bytes written in SCAFTDR is equal to or less than the transmit trigger number, the TDFE flag will be set to 1 again after being read as 1 and cleared to 0. TDFE clearing should therefore be carried out when SCAFTDR contains more than the transmit trigger number of transmit data bytes.

The number of transmit data bytes in SCAFTDR can be found from the T6 to T0 bits in SCAFDR.

(2) SCAFRDR Reading and the RDF Flag

The RDF flag in SCASSR is set when the number of receive data bytes in SCAFRDR has become equal to or greater than the receive trigger number set by bits RTRG1 and RTRG0 in SCAFCR. After RDF is set, receive data equivalent to the trigger number can be read from SCAFRDR, allowing efficient continuous reception.

However, if the number of data bytes in SCAFRDR is still equal to or greater than the trigger number after a read, the RDF flag will be set to 1 again if it is cleared to 0. RDF should therefore be cleared to 0 after being read as 1 after all receive data has been read.

The number of receive data bytes in SCAFRDR can be found from the R6 to R0 bits in SCAFDR.

(3) Break Detection and Processing

Break signals can be detected by reading the RxD pin directly when a framing error (FER) is detected. In the break state the input from the RxD pin consists of all 0s, so the FER flag is set and the parity error flag (PER) may also be set.

Although SCIFA stops transferring receive data to SCAFRDR after receiving a break, the receive operation continues.

(4) Receive Data Sampling Timing and Receive Margin

As an example, when the sampling rate is 1/16, SCIFA operates on a base clock with a frequency of 8 times the transfer rate.

In reception, SCIFA synchronizes internally with the fall of the start bit, which it samples on the base clock. Receive data is latched at the rising edge of the eighth base clock pulse (when the sampling rate is 1/16).

The timing is shown in Figure 21.21.

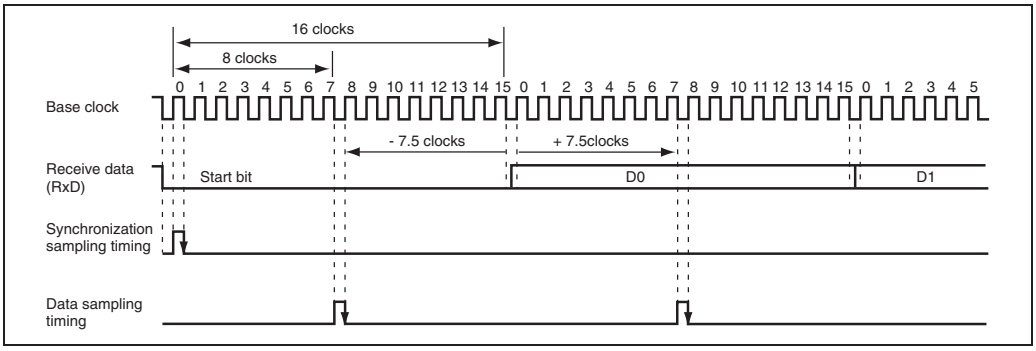


Figure 21.21 Receive Data Sampling Timing

The receive margin can therefore be expressed as shown in equation (1).

$$M = \left| \left(0.5 - \frac{1}{2N}\right) - (L - 0.5)F - \frac{|D - 0.5|}{N}(1 + F) \right| \times 100\% \ldots\ldots (1)$$

M: Receive margin (%)
N: Ratio of clock frequency to bit rate (N = 16)
D: Clock duty cycle (D = 0 to 1.0)
L: Frame length (L = 9 to 12)
F: Absolute deviation of clock frequency

From equation (1), if F = 0 and D = 0.5, the receive margin is 46.875%, as given by equation (2).

When D = 0.5 and F = 0:

$$M = (0.5 - 1/(2 \times 16)) \times 100\% = 46.875\% \ldots\ldots (2)$$

This is a theoretical value. A reasonable margin to allow in system designs is the value above (46.875%) plus 20% to 30%.

(5) PAD Pin when the Pin for SCIF Is Selected

The table below shows the PAD pin state when the pin for SCIF is selected.

When the pin for SCIF is selected	TXD	RXD	RTS_N	CTS_N	SCK
PAD enable	1 (enable)	1 (enable)	SCAFCR.MCE (Initial value: 0, disable)	SCAFCR.MCE (Initial value: 0, disable)	SCASCR.CKE0 (Initial value: 0, disable)
Pin state	Output (initial value: 1)	Input	Hi-Z	Input	Hi-Z
Pull-up/-down	—	Pull-up required	—	Pull-up required	—
Remarks	—	SCIF fixes RXD to 1 internally when SCASCR.RE = 0.	—	SCIF fixes CTS_N to 1 internally when SCAFCR.MCE = 0.	—

Section 22 Serial Communications Interface with FIFO B (SCIFB)

This LSI has a serial communications interface incorporating FIFO buffers (Serial Communications Interface with FIFO B: SCIFB) that can perform both asynchronous and clocked synchronous serial communications.

Each interface includes two 256-stage buffers, one for the transmit FIFO register and one for the receive FIFO register, enabling fast, efficient, and continuous communications.

22.1 Features

- One channel installed in the system domain
- Asynchronous mode

  Serial data communications are executed using an asynchronous system in which synchronization is achieved character by character. Serial data communications can be carried out with standard asynchronous communications chips such as a Universal Asynchronous Receiver/Transmitter (UART) or Asynchronous Communications Interface Adapter (ACIA).

  There is a choice of eight serial data communication formats.

  — Data length: 7 or 8 bits

  — Stop bit length: 1 or 2 bits

  — Parity: Even/odd/none

  — LSB-first transfer

  — Receive error detection: Parity, framing, and overrun errors

  — Break detection: If a framing error is followed by at least one frame at the space "0" (low level), a break is detected.
- Clocked synchronous mode

  Serial data communications in synchronization with a clock can be carried out with other LSIs that have a clocked synchronous communications function.

  — Data length: 8 bits

  — Receive error detection: Overrun error

  — A rising or falling edge of a clock is selectable as the data transmit/receive timing.
- On-chip baud-rate generator allows any bit rate to be selected.

  — Minimum: SUBϕ/5 bps, maximum: SUBϕ/(27 × 256 × 64) bps (asynchronous)

— Minimum: SUBϕ/(2 × 2) bps, maximum: SUBϕ/(2 × 256 × 64) bps (clocked synchronous)

- Serial clock source: Internal clock signal generated by the baud-rate generator.
- Six interrupt sources

  There are six interrupt sources — transmit-data-stop, transmit-FIFO-data-empty, receive-FIFO-data-full, receive-error (framing/parity error), break-receive, and receive-data-ready interrupts. The vectors of each interrupt source are the same.
- The DMA controller (DMAC) can be activated to execute a data transfer in the event of a transmit-FIFO-data-empty, transmit-data-stop, or receive-FIFO-data-full interrupt. The DMAC requests of transmit-FIFO-data-empty and transmit-data-stop interrupts are the same.
- Supports multibyte DMA transfers.
- On-chip modem control functions (CTS_N and RTS_N)
- On-chip transmit-data-stop function
- When not in use, the SCIFB can be stopped by halting its clock supply to reduce power consumption.
- The amount of data in the transmit/receive FIFO registers, and the number of receive errors in the receive data in the receive FIFO register, can be ascertained.

Figure 22.1 shows a block diagram of SCIFB.

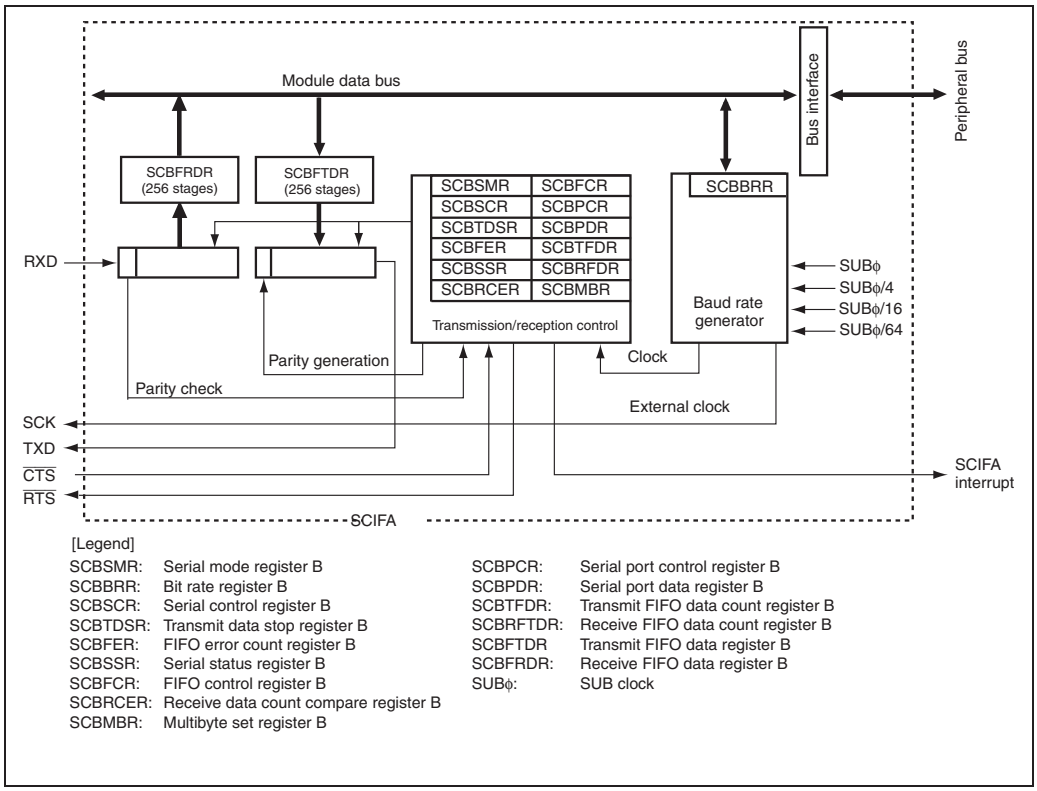


Figure 22.1 Block Diagram of SCIFB

22.2 Input/Output Pins

Table 22.1 shows the SCIFB pin configuration.

Table 22.1 Pin Configuration

Channel	Abbreviation	Input/output	Description
0	SCIFB_SCK	Output	Clock output
	SCIFB_RXD	Input	Receive data
	SCIFB_TXD	Output	Transmit data
	SCIFB_CTS_N	Input	Clear to send
	SCIFB_RTS_N	Output	Request to send

Note: The channel number is omitted, and SCK, RxD, TxD, CTS_N, and RTS_N are used as generic terms in the following descriptions.

22.3 Register Descriptions

Table 22.2 shows the SCIFB registers. Table 22.3 shows the register states in the respective processing modes.

Table 22.2 Register Configuration

Register Name	Register Abbreviation	R/W	Address		Access Size
			Regular	Shadow	
Serial mode register B	SCBSMR	R/W	H'E6C3 0000	H'E7C3 0000	16
Bit rate register B	SCBBRR	R/W	H'E6C3 0004	H'E7C3 0004	8
Serial control register B	SCBSCR	R/W	H'E6C3 0008	H'E7C3 0008	16
Transmit data stop register B	SCBTDSR	R/W	H'E6C3 000C	H'E7C3 000C	16
FIFO error count register B	SCBFER	R	H'E6C3 0010	H'E7C3 0010	16
Serial status register B	SCBSSR	R/W*	H'E6C3 0014	H'E7C3 0014	16
FIFO control register B	SCBFCR	R/W	H'E6C3 0018	H'E7C3 0018	16
Receive data count compare register B	SCBRCER	R/W	H'E6C3 0028	H'E7C3 0028	16
Multibyte set register B	SCBMBR	R/W	H'E6C3 002C	H'E7C3 002C	16
Serial port control register B	SCBPCR	R/W	H'E6C3 0030	H'E7C3 0030	16
Serial port data register B	SCBPDR	R/W	H'E6C3 0034	H'E7C3 0034	16
Transmit FIFO data count register B	SCBTFDR	R	H'E6C3 0038	H'E7C3 0038	16
Receive FIFO data count register B	SCBRFDR	R	H'E6C3 003C	H'E7C3 003C	16
Transmit FIFO data register B	SCBFTDR	W	H'E6C3 0040	H'E7C3 0040	8
Receive FIFO data register B	SCBFRDR	R	H'E6C3 0060	H'E7C3 0060	8

Note: * To clear the flags, 0s can only be written to bits 13, 9, 8, 7, 5, 4, 1, and 0.

Table 22.3 Register States in Each Operating Mode

Register Abbreviation	Reset*	Module Standby
SCBSMR	Initialized	Retained
SCBBRR	Initialized	Retained
SCBSCR	Initialized	Retained
SCBTDSR	Initialized	Retained
SCBFER	Initialized	Retained
SCBSSR	Initialized	Retained
SCBFCR	Initialized	Retained
SCBRCER	Initialized	Retained
SCBMBR	Initialized	Retained
SCBPCR	Initialized	Retained
SCBPDR	Undefined	Retained
SCBTFDR	Initialized	Retained
SCBRFDR	Initialized	Retained
SCBFTDR	Undefined	Retained
SCBFRDR	Undefined	Retained

Note: * For details, refer to section 1-D Overview of reset.

22.3.1 Serial Mode Register (SCBSMR)

SCBSMR is a 16-bit readable/writable register used to set SCIFB's serial transfer format and select the baud-rate generator clock source and the sampling rate.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CKEDG	—	SRC[2:0]			C/$\overline{A}$	CHR	PE	O/E	STOP	—	CKS[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	CKEDG	0	R/W	Transmit/Receive Clock Edge Select Selects the clock edge at which the serial data is output in clocked synchronous mode. 0: Serial data is transmitted at the falling edge of output clock. Serial data is received at the rising edge of output clock. 1: Serial data is transmitted at the rising edge of output clock. Serial data is received at the falling edge of output clock.
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
10 to 8	SRC[2:0]	000	R/W	Sampling Control These bits select the sampling rate. 000: Sampling rate 1/16 001: Sampling rate 1/5 010: Sampling rate 1/7 011: Sampling rate 1/11 100: Sampling rate 1/13 101: Sampling rate 1/17 110: Sampling rate 1/19 111: Sampling rate 1/27
7	C/$\overline{A}$	0	R/W	Communication Mode Selects asynchronous mode or clocked synchronous mode as the SCIFB operating mode. 0: Asynchronous mode 1: Clocked synchronous mode
6	CHR	0	R/W	Character Length Selects 7 or 8 bits as the data length. 0: 8-bit data 1: 7-bit data* Note: * When the 7-bit character is selected, the MSB (bit 7) in SCBFTDR is not transmitted.
5	PE	0	R/W	Parity Enable Selects whether or not parity bit addition is performed in transmission, and parity bit checking in reception. 0: Parity bit addition and checking disabled 1: Parity bit addition and checking enabled* Note: * When the PE bit is set to 1, the parity (even or odd) specified by the O/E bit is added to transmit data before transmission. In reception, the parity bit is checked for the parity (even or odd) specified by the O/E bit.

Bit	Bit Name	Initial Value	R/W	Description
4	O/E	0	R/W	Parity Mode Selects either even or odd parity for use in parity addition and checking. The O/E bit setting is only valid when the PE bit is set to 1, enabling parity bit addition and checking. The O/E bit setting is invalid when parity addition and checking is disabled. 0: Even parity*[1] 1: Odd parity*[2] Notes: 1. When even parity is set, parity bit addition is performed in transmission so that the total number of 1-bits in the transmit character plus the parity bit is even. In reception, a check is performed to see if the total number of 1-bits in the receive character plus the parity bit is even. 2. When odd parity is set, parity bit addition is performed in transmission so that the total number of 1-bits in the transmit character plus the parity bit is odd. In reception, a check is performed to see if the total number of 1-bits in the receive character plus the parity bit is odd.
3	STOP	0	R/W	Stop Bit Length Selects 1 or 2 bits as the stop bit length. In reception, only the first stop bit is checked, regardless of the STOP bit setting. If the second stop bit is 1, it is treated as a stop bit; if it is 0, it is treated as the start bit of the next transmit character. 0: 1 stop bit*[1] 1: 2 stop bits*[2] Notes: 1. In transmission, a single logic-1 bit (stop bit) is added to the end of a transmit character before it is sent. 2. In transmission, two logic-1 bits (stop bits) are added to the end of a transmit character before it is sent.

Bit	Bit Name	Initial Value	R/W	Description
2	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
1, 0	CKS[1:0]	00	R/W	Clock Select Select the clock source of the internal baud-rate generator. 00: SUBϕ 01: SUBϕ/4 10: SUBϕ/16 11: SUBϕ/64 Note: SUBϕ: SUB clock

22.3.2 Bit Rate Register (SCBBRR)

SCBBRR is an 8-bit readable/writable register that sets the serial transfer bit rate in accordance with the baud-rate generator operating clock selected by bits CKS1 and CKS0 in SCBSMR.

Bit:	7	6	5	4	3	2	1	0
	SCBRD[7:0]							
Initial value:	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	SCBRD[7:0]	H'FF	R/W	Bit Rate 0 ≤ SCBRD ≤ 255 (Asynchronus) 1 ≤ SCBRD ≤ 255 (Clocked synchronous)

The SCBBRR setting is found by using the following equations.

(1) Asynchronous Mode:

- When the sampling rate is 1/16,
  $N = \{ SUB\phi/(16 \times 2^{2n} \times B) \} \times 10^6 - 1$
- When the sampling rate is 1/5,
  $N = \{ SUB\phi/(5 \times 2^{2n} \times B) \} \times 10^6 - 1$

- When the sampling rate is 1/11,
  $N = \{ SUB\phi / (11 \times 2^{2n} \times B) \} \times 10^6 - 1$
- When the sampling rate is 1/13,
  $N = \{ SUB\phi / (13 \times 2^{2n} \times B) \} \times 10^6 - 1$
- When the sampling rate is 1/27,
  $N = \{ SUB\phi / (27 \times 2^{2n} \times B) \} \times 10^6 - 1$

(2) Clocked Synchronous Mode:

$$N = \{ SUB\phi / (2 \times 2^{2n} \times B) \} \times 10^6 - 1$$

Where B: Bit rate (bits/s)
N: SCBBRR setting for baud-rate generator
Asynchronous mode ($0 \le N \le 255$)
Clocked synchronous mode ($1 \le N \le 255$)

SUBϕ: Subclock frequency (MHz)

n: Baud-rate generator input clock (n = 0 to 3)
(See the table below for the relation between n and the clock.)

Table 22.4 SCBSMR Setting

		SCBSMR Setting
n	**Clock**	**CKS[1:0]**
0	SUBϕ	00
1	SUBϕ/4	01
2	SUBϕ/16	10
3	SUBϕ/64	11

The bit rate error in asynchronous mode is found by using the following equations.

When the sampling rate is 1/16,

$$\text{Error (\%)} = \{ \{ \text{SUB}\phi / ((N + 1) \times 16 \times 2^{2n} \times B) \} \times 10^{6} - 1 \} \times 100$$

When the sampling rate is 1/5,

$$\text{Error (\%)} = \{ \{ \text{SUB}\phi / ((N + 1) \times 5 \times 2^{2n} \times B) \} \times 10^{6} - 1 \} \times 100$$

When the sampling rate is 1/11,

$$\text{Error (\%)} = \{ \{ \text{SUB}\phi / ((N + 1) \times 11 \times 2^{2n} \times B) \} \times 10^{6} - 1 \} \times 100$$

When the sampling rate is 1/13,

$$\text{Error (\%)} = \{ \{ \text{SUB}\phi / ((N + 1) \times 13 \times 2^{2n} \times B) \} \times 10^{6} - 1 \} \times 100$$

When the sampling rate is 1/27,

$$\text{Error (\%)} = \{ \{ \text{SUB}\phi / ((N + 1) \times 27 \times 2^{2n} \times B) \} \times 10^{6} - 1 \} \times 100$$

22.3.3 Serial Control Register (SCBSCR)

SCBSCR is a 16-bit readable/writable register that performs enabling or disabling of SCIFB transfer operations and interrupt requests, and selection of the serial clock source.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TDRQE	RDRQE	RCEE	—	TSIE	ERIE	BRIE	DRIE	TIE	RIE	TE	RE	—	—	—	CKE0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	TDRQE	0	R/W	Transmit Data Transfer Request Enable Switches the transmit FIFO empty interrupt or DMA transfer request when TIE = 1 and the transmit FIFO empty occurs. 0: Interrupt request to CPU is issued. 1: Transmit data transfer request to DMAC is issued.
14	RDRQE	0	R/W	Receive Data Transfer Request Enable Switches the receive FIFO-data-full interrupt or DMA transfer request when RIE = 1 and the receive FIFO-data-full occurs. 0: Interrupt request to CPU is issued. 1: Receive data transfer request to DMAC is issued.
13	RCEE	0	R/W	Receive Data Count Compare Interrupt Enable Generates an interrupt when the receive data count comparison counter matches the current receive data count. 0: Receive data count compare interrupt disabled* 1: Receive data count compare interrupt enabled Note: * This interrupt request is cleared by clearing the RCEF flag to 0 after reading 1 from it or clearing the RCEE bit to 0.
12	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
11	TSIE	0	R/W	Transmit Data Stop Interrupt Enable Enables or disables generation of a transmit-data-stop interrupt when the TSE bit in SCBFCR is enabled and the TSF flag in SCBSSR is set to 1. 0: Transmit-data-stop interrupt disabled* 1: Transmit-data-stop interrupt enabled Note: * The TDI interrupt request is cleared by clearing the TSF flag to 0 after reading 1 from it or clearing the TSIE bit to 0.
10	ERIE	0	R/W	Receive Error Interrupt Enable Enables or disables generation of a receive-error (framing or parity error) interrupt when the ER flag in SCBSSR is set to 1. 0: Receive-error interrupt disabled* 1: Receive-error interrupt enabled Note: * The ERI interrupt request is cleared by clearing the ER flag to 0 after reading 1 from it or clearing the ERIE bit to 0.
9	BRIE	0	R/W	Break Interrupt Enable Enables or disables generation of a break-receive interrupt when the BRK flag in SCBSSR is set to 1. 0: Break-receive interrupt disabled* 1: Break-receive interrupt enabled Note: * The BRI interrupt request is cleared by clearing the BRK flag to 0 after reading 1 from it or clearing the BRIE bit to 0.
8	DRIE	0	R/W	Receive Data Ready Interrupt Enable Enables or disables generation of a receive-data-ready interrupt when the DR flag in SCBSSR is set to 1. 0: Receive-data-ready interrupt disabled* 1: Receive-data-ready interrupt enabled Note: * The DRI interrupt request is cleared by clearing the DR flag to 0 after reading 1 from it or clearing the DRIE bit to 0.

Bit	Bit Name	Initial Value	R/W	Description
7	TIE	0	R/W	Transmit Interrupt Enable Enables or disables generation of a transmit-FIFO-data-empty interrupt request when the TDFE flag in SCBSSR is set to 1. 0: Transmit-FIFO-data-empty interrupt request disabled* 1: Transmit-FIFO-data-empty interrupt request enabled Note: * This interrupt request is cleared by writing transmit data exceeding the transmit trigger set number to SCBFTDR, reading 1 from the TDFE flag, then clearing it to 0, or by clearing the TIE bit to 0.
6	RIE	0	R/W	Receive Interrupt Enable Enables or disables generation of a receive-FIFO-data-full interrupt request when the RDF flag in SCBSSR is set to 1. 0: Receive-FIFO-data-full interrupt request disabled* 1: Receive-FIFO-data-full interrupt request enabled Note: * This interrupt request is cleared by reading 1 from the RDF flag, then clearing the flag to 0, or by clearing the RIE bit to 0.
5	TE	0	R/W	Transmit Enable Enables or disables the start of serial transmission by SCIFB. 0: Transmission disabled 1: Transmission enabled* Note: * Make SCBSMR and SCBFCR settings, decide the transmit format, and reset the transmit FIFO before setting the TE bit to 1.

Bit	Bit Name	Initial Value	R/W	Description
4	RE	0	R/W	Receive Enable Enables or disables the start of serial reception by SCIFB. 0: Reception disabled*[1] 1: Reception enabled*[2] Notes: 1. Clearing the RE bit to 0 does not affect the DR, ER, BRK, RDF, FER, PER, and ORER flags, which retain their state. 2. Make SCBSMR and SCBFCR settings, decide the receive format, and reset the receive FIFO before setting the RE bit to 1.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	CKE0	0	R/W	Clock Enable Enables or disables the clock output from the SCK pin. The CKE0 bit must be set before determining the SCIFB operating mode with SCBSMR. 0: SCK pin disabled 1: Clock output from SCK* Note: * In clocked synchronous mode, the SCK pin outputs a clock with the same frequency as the bit rate.

22.3.4 Transmit Data Stop Register (SCBTDSR)

SCBTDSR is a 16-bit readable/writable register that sets the number of transmit data bytes. SCBTDSR is valid only when the TSE bit in SCBFCR is enabled. Transmit operation is stopped when the number of data bytes set in SCBTDSR is transmitted. The setting value should be H'0000 (one byte) to H'FFFF (65536 bytes). SCBTDSR is initialized to H'FFFF.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TDSRD[15:0]															
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 0	TDSRD[15:0]	H'FFFF	R/W	Transmit Data Stop Setting

22.3.5 FIFO Error Count Register (SCBFER)

SCBFER is a 16-bit read-only register that indicates the number of receive errors (framing errors and parity errors).

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PER[7:0]								FER[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 8	PER[7:0]	000000	R	Parity Error Count These bits indicate the number of data in which parity errors are generated, in receive data stored in SCBFRDR. After the ER bit in SCBSSR is set, the value of bits PER7 to PER0 indicates the number of data in which parity errors are generated. When all 256 bytes of receive data in SCBFRDR have parity errors, these bits indicate 0.

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	FER[7:0]	000000	R	Framing Error Count These bits indicate the number of data in which framing errors are generated, in receive data stored in SCBFRDR. After the ER bit in SCBSSR is set, the value of bits FER7 to FER0 indicates the number of data in which framing errors are generated. When all 256 bytes of receive data in SCBFRDR have framing errors, these bits indicate 0.

22.3.6 Serial Status Register (SCBSSR)

SCBSSR is a 16-bit readable/writable register that indicates the SCIFB status.

However, 1 cannot be written to the ORER, TSF, ER, TDFE, BRK, RDF, and DR flags. Before these flags can be cleared to 0, they must first be read as 1. The TEND, FER, and PER flags are read-only flags and cannot be modified.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	RCEF	—	—	—	ORER	TSF	ER	TEND	TDFE	BRK	FER	PER	RDF	DR
Initial value:	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
R/W:	R	R	R/(W)*	R	R	R	R/(W)*	R/(W)*	R/(W)*	R	R/(W)*	R/(W)*	R	R	R/(W)*	R/(W)*

Bit	Bit Name	Initial Value	R/W	Description
15 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
13	RCEF	0	R/(W)*	Receive Data Count Match Indicates that the receive data count matches the receive data count comparison counter. 0: Receive data count does not match the receive data count comparison counter. [Clearing conditions] Power-on reset or manual reset When 0 is written to RCEF after reading RCEF = 1 1: Receive data count matches the receive data count comparison counter.*[2] [Setting condition] When the receive data count matches the counter value
12 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
9	ORER	0	R/(W)*	Overrun Error Indicates that an overrun error occurred during reception. This bit is valid only in asynchronous mode. 0: Reception is in progress or has completed normally.*[1] [Clearing conditions] Power-on reset or manual reset When 0 is written to ORER after reading ORER = 1 1: An overrun error occurred during reception.*[2] [Setting condition] When serial data reception is completed while the receive FIFO is full Notes: 1. The ORER flag is not affected and retains its previous state when the RE bit in SCBSCR is cleared to 0. 2. The receive data prior to the overrun error is retained in SCBFRDR, and the data received subsequently is lost. Serial data reception cannot be continued with the ORER flag set to 1.
8	TSF	0	R/(W)*	Transmit Data Stop Indicates that the number of transmit data matches the value of SCBTDSR. This bit is valid only in asynchronous mode. 0: The number of transmit data does not match the SCBTDSR value. [Clearing conditions] Power-on reset or manual reset When 0 is written to TSF after reading TSF = 1 1: The number of transmit data matches the SCBTDSR value.

Bit	Bit Name	Initial Value	R/W	Description
7	ER	0	R/(W)*	Receive Error Indicates that a framing error or parity error occurred during reception.*[1] This bit is valid only in asynchronous mode. 0: No framing error or parity error occurred during reception. [Clearing conditions] Power-on reset or manual reset When 0 is written to ER after reading ER = 1 1: A framing error or parity error occurred during reception. [Setting conditions] When the SCIFB checks whether the stop bit at the end of the receive data is 1 when reception ends, and the stop bit is 0*[2] When, in reception, the number of logic-1 bits in the receive data and in the parity bit does not match the parity setting (even or odd) specified by the O/E bit in SCBSMR Notes: 1. The ER flag is not affected and retains its previous state when the RE bit in SCBSCR is cleared to 0. When a receive error occurs, the receive data is still transferred to SCBFRDR, and reception continues. The FER and PER bits in SCBSSR can be used to determine whether there is a receive error in the data read from SCBFRDR. 2. When the stop-bit length is 2 bits, only the first stop bit is checked for a value of 1 and the second stop bit is not checked.

Bit	Bit Name	Initial Value	R/W	Description
6	TEND	1	R	Transmission End Indicates that there is no valid data in SCBFTDR when the last bit of the transmit character is sent and that transmission has been completed. 0: Transmission is in progress. [Clearing condition] When data is written to SCBFTDR 1: Transmission has been completed. [Setting condition] When there is no transmit data in SCBFTDR during transmission of a 1-byte serial transmit character
5	TDFE	1	R/(W)*	Transmit FIFO Data Empty Indicates that data has been transferred from SCBFTDR to SCBTSR, the number of data bytes in SCBFTDR has fallen to or below the transmit trigger data number set by bits TTRG1 and TTRG0 in SCBFCR, and new transmit data can be written to SCBFTDR. 0: A number of transmit data bytes exceeding the transmit trigger set number have been written to SCBFTDR. [Clearing condition] When transmit data exceeding the transmit trigger set number is written to SCBFTDR, and 0 is written to TDFE after reading TDFE = 1 1: The number of transmit data bytes in SCBFTDR is equal to or less than the transmit trigger set number. [Setting conditions] Power-on reset or manual reset When the number of SCBFTDR transmit data bytes falls to or below the transmit trigger set number after a transmit operation* Note: * As SCBFTDR is a 256-byte FIFO register, the maximum number of bytes that can be written when TDFE = 1 is 256 – (transmit trigger set number). Data written in excess of this will be ignored. The number of data bytes in SCBFTDR is indicated by SCBTFDR.

Bit	Bit Name	Initial Value	R/W	Description
4	BRK	0	R/(W)*	Break Detect Indicates that a receive data break signal has been detected. This bit is valid only in asynchronous mode. 0: A break signal has not been received. [Clearing conditions] Power-on reset or manual reset When 0 is written to BRK after reading BRK = 1 1: A break signal has been received.* [Setting condition] When data with a framing error is received, followed by the space 0 level (low level) for at least one frame length Note: * When a break is detected, the receive data (H'00) following the detection is not transferred to SCBFRDR. When the break ends and the receive signal returns to mark 1, receive data transfer is resumed.
3	FER	0	R	Framing Error Indicates a framing error in the data read from SCBFRDR. This bit is valid only in asynchronous mode. 0: There is no framing error in the receive data read from SCBFRDR. [Clearing conditions] Power-on reset or manual reset When there is no framing error in SCBFRDR read data 1: There is a framing error in the receive data read from SCBFRDR. [Setting condition] When there is a framing error in SCBFRDR read data

Bit	Bit Name	Initial Value	R/W	Description
2	PER	0	R	Parity Error Indicates a parity error in the data read from SCBFRDR. This bit is valid only in asynchronous mode. 0: There is no parity error in the receive data read from SCBFRDR. [Clearing conditions] Power-on reset or manual reset When there is no parity error in SCBFRDR read data 1: There is a parity error in the receive data read from SCBFRDR. [Setting condition] When there is a parity error in SCBFRDR read data
1	RDF	0	R/(W)*	Receive FIFO Data Full Indicates that the received data has been transferred from SCBRSR to SCBFRDR, and the number of receive data bytes in SCBFRDR is equal to or greater than the receive trigger number set by bits RTRG1 and RTRG0 in SCBFCR. 0: The number of receive data bytes in SCBFRDR is less than the receive trigger set number. [Clearing conditions] Power-on reset or manual reset When SCBFRDR is read until the number of receive data bytes in SCBFRDR falls below the receive trigger set number, and 0 is written to RDF after reading RDF = 1 1: The number of receive data bytes in SCBFRDR is equal to or greater than the receive trigger set number. [Setting condition] When SCBFRDR contains at least the receive trigger set number of receive data bytes* Note: * SCBFRDR is a 256-byte FIFO register. When RDF = 1, at least the receive trigger set number of data bytes can be read. If data is read when SCBFRDR is empty, an undefined value will be returned. The number of receive data bytes in SCBFRDR is indicated by the lower bits of SCBRFDR.

Bit	Bit Name	Initial Value	R/W	Description
0	DR	0	R/(W) *	Receive Data Ready Indicates that there are data bytes fewer than the receive trigger set number in SCBFRDR, and no further data will arrive at least 15 etu after the stop bit of the last data received. This bit is valid only in asynchronous mode. 0: Reception is in progress or has ended normally and no receive data is left in SCBFRDR. [Clearing conditions] (initial value) Power-on reset or manual reset When all the receive data in SCBFRDR has been read, and 0 is written to DR after reading DR = 1 1: No further receive data has arrived. [Setting condition] When SCBFRDR contains data bytes fewer than the receive trigger set number, and no further data will arrive at least 15 etu after the stop bit of the last data received* Note: * Corresponds to 1.5 frame time in 8-bit one-stop-bit format. etu: Elementary time unit (time for transfer of 1 bit)

Note: * Only 0 can be written for flag clearing.

22.3.7 FIFO Control Register (SCBFCR)

SCBFCR is a 16-bit readable/writable register that clears all data and sets the trigger data number for the transmit and receive FIFO registers. The register also contains a loopback test enable bit.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TSE	TCRST	RCE	RCRST	—	RSTRG[2:0]			RTRG[1:0]		TTRG[1:0]		MCE	TFRST	RFRST	LOOP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	TSE	0	R/W	Transmit Data Stop Enable Enables or disables the transmit data stop function. 0: Transmit data stop function disabled 1: Transmit data stop function enabled
14	TCRST	0	R/W	Transmit Count Reset Clears the transmit count to 0. This bit is valid only when the transmit data stop function is used. 0: Transmit count reset disabled* 1: Transmit count reset enabled (clearing to 0) Note: * The transmit count is reset (clearing to 0) by a power-on reset or manual reset.
13	RCE	0	R/W	Receive Data Count Comparison Enable Enables or disables the comparison of receive data count. 0: Comparison of receive data count disabled 1: Comparison of receive data count enabled
12	RCRST	0	R/W	Receive Count Reset Clears the receive count to 0. This bit is valid only when the receive data count comparison function is used. 0: Receive count reset disabled* 1：Receive count reset enabled (clearing to 0) Note：* The receive count is reset (clearing to 0) by a power-on reset or manual reset.

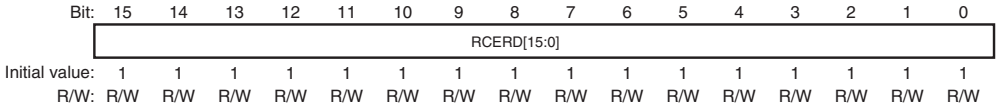
Bit	Bit Name	Initial Value	R/W	Description
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10 to 8	RSTRG[2:0]	000	R/W	RTS_N Output Active Trigger The $\overline{\text{RTS}}$ signal becomes high when the number of receive data stored in SCBFRDR reaches the trigger set number shown below. 000: 255 001: 1 010: 32 011: 64 100: 128 101: 192 110: 224 111: 240
7, 6	RTRG[1:0]	00	R/W	Receive FIFO Data Number Trigger Set the number of receive data bytes that sets the RDF flag in SCBSSR. The RDF flag is set when the number of receive data bytes in SCBFRDR reaches the trigger set number shown below. 00: 1 01: 16 10: 32 11: 48 In multibyte transfer mode, a transfer request is made to the DMAC when the number of receive data bytes in SCBFRDR reaches the trigger set number shown below. (The RDF flag is undefined.) 00: Reserved 01: 32 10: 16 11: 1

Bit	Bit Name	Initial Value	R/W	Description
5, 4	TTRG[1:0]	00	R/W	Transmit FIFO Data Number Trigger Set the number of remaining transmit data bytes that sets the TDFE flag in SCBSSR. The TDFE flag is set when, as the result of a transmit operation, the number of transmit data bytes in SCBFTDR falls to or below the trigger set number shown below. 00: 32 (32) 01: 16 (48) 10: 2 (62) 11: 0 (64) In multibyte transfer mode, a transfer request is made to the DMAC when the number of transmit data bytes in SCBFTDR falls to or below the trigger set number shown below. (The TDFE flag is undefined.) 00: Reserved 01: 224 (32) 10: 240 (16) 11: 255 (1) Note: The values in parentheses are the number of empty bytes in SCBFTDR when the flag is set.
3	MCE	0	R/W	Modem Control Enable Enables the CTS_N and RTS_N modem control signals. 0：Modem signals disabled* 1：Modem signals enabled Note: * CTS_N is fixed at active-0 regardless of the input value, and RTS_N output is also fixed at 0.
2	TFRST	0	R/W	Transmit FIFO Data Register Reset Invalidates the transmit data in SCBFTDR and resets it to the empty state. 0: Reset operation disabled* 1: Reset operation enabled Note: * A reset operation is performed at a power-on reset or manual reset.

Bit	Bit Name	Initial Value	R/W	Description
1	RFRST	0	R/W	Receive FIFO Data Register Reset Invalidates the receive data in SCBFRDR and resets it to the empty state. 0: Reset operation disabled* 1: Reset operation enabled Note: * A reset operation is performed at a power-on reset or manual reset.
0	LOOP	0	R/W	Loopback Test Internally connects the transmit output pin (TxD) to receive input pin (RxD) and RTS_N pin to CTS_N pin, enabling loopback testing. 0: Loopback test disabled 1: Loopback test enabled

22.3.8 Receive Data Count Compare Register (SCBRCER)

SCBRCER is a 16-bit readable/writable register that sets the number of receive data bytes. SCBRCER is valid only when the RCE bit in SCBFCR is set to 1 (enabled). The data reception stops when the number of receive data bytes reaches the value of this register. A value between H'0000 (1 byte) to H'FFFF (65536 bytes) can be set. SCBRCER is initialized to H'FFFF.



Bit	Bit Name	Initial Value	R/W	Description
15 to 0	RCERD[15:0]	H'FFFF	R/W	Receive Data Stop

22.3.9 Multibyte Set Register (SCBMBR)

SCBMBR is a 16-bit readable/writable register for multibyte transfer setting. Settings for transmission in SCBMBR is valid when the TDRQE bit in SCBSCR is set to 1, and settings for reception is valid when the RDRQE bit in SCBSCR is set to 1.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ADD REQ	—	—	—	—	—	—	—	—	—	—	—	RCECR ON	—	MBRON	MBTON
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	ADDREQ	0	R/W	Enables or disables receive data transfer until the receive FIFO data count is decreased to 0. 0: Receive data transfer disabled until the receive FIFO data count is decreased to 0 1: Receive data transfer enabled until the receive FIFO data count is decreased to 0
14 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3	RCECRON	0	R/W	Enables or disables receive data transfer in conjunction with the RCEF bit in SCBSSR. Receive data transfer requests are made until the receive FIFO data count is decreased to 0. 0: Receive data transfer in conjunction with RCEF in SCBSSR enabled 1: Receive data transfer in conjunction with RCEF in SCBSSR disabled

Bit	Bit Name	Initial Value	R/W	Description
2	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
1	MBRON	0	R/W	Enables or disables multibyte receive data transfer 0: Multibyte receive data transfer disabled 1: Multibyte receive data transfer enabled
0	MBTON	0	R/W	Enables or disables multibyte transmit data transfer 0: Multibyte transmit data transfer disabled 1: Multibyte transmit data transfer enabled

22.3.10 Serial Port Control Register (SCBPCR)

SCBPCR is a 16 bit readable/writable register. This register specifies whether the TXD, SCK and RTS_N pins function as output ports or the TXD, SCK and RTS_N pins, respectively. It also specifies whether the RXD and CTS_N pins function as input ports or the RXD and CTS_N pins, respectively.

SCBPCR is initialized to H'0000. This register function is valid only when the SCIFB pin function is selected through the pin function controller (PFC).

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	RTSC	CTSC	SCKC	RXDC	TXDC
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 5	—	H'000	R	Reserved These bits are always read as 0. The write value should always be 0.
4	RTSC	0	R/W	Selects the RTS_N pin function. 0: The RTS_N pin functions as the RTS_N pin. 1: The RTS_N pin functions as an output port.
3	CTSC	0	R/W	Selects the CTS_N pin function. 0: The CTS_N pin functions as the CTS_N pin. 1: The CTS_N pin functions as an input port.
2	SCKC	0	R/W	Selects the SCK pin function. 0: The SCK pin functions as the SCK pin. 1: The SCK pin functions as an output port.
1	RXDC	0	R/W	Selects the RXD pin function. 0: The RXD pin functions as the RXD pin. 1: The RXD pin functions as an input port.
0	TXDC	0	R/W	Selects the TXD pin function. 0: The TXD pin functions as the TXD pin. 1: The TXD pin functions as an output port.

22.3.11 Serial Port Data Register (SCBPDR)

SCBPDR is a 16 bit readable/writable register. This register specifies data output to the TXD, SCK and RTS_N pins when the SCIFB pin function is selected by SCBPCR. It also specifies the pin level of the RXD and CTS_N pins.

SCBPDR is initialized to H'0000. This register function is valid only when the SCIFB pin function is selected through the pin function controller (PFC).

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	RTSD	CTSD	SCKD	RXDD	TXDD
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	—	0	—	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	W	R	W	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 5	—	H'000	R	Reserved These bits are always read as 0. The write value should always be 0.
4	RTSD	0	W	Specifies data output to the RTS_N pin. 0: Outputs 0. 1: Outputs 1.

Bit	Bit Name	Initial Value	R/W	Description
3	CTSD	Undefined	R	Specifies the CTS_N pin level. 0: CTS_N pin level is 0. 1: CTS_N pin level is 1.
2	SCKD	0	W	Specifies data output to the SCK pin. 0: Outputs 0. 1: Outputs 1.
1	RXDD	Undefined	R	Specifies the RXD pin level. 0: RXD pin level is 0. 1: RXD pin level is 1.
0	TXDD	0	R/W	Specifies data output to the TXD pin. 0: Outputs 0. 1: Outputs 1.

22.3.12 Transmit FIFO Data Count Register (SCBTFDR)

SCBTFDR is a 16-bit read-only register that indicates the number of data bytes stored in SCBFTDR.

The T8 to T0 bits indicate the number of transmit data bytes in SCBFTDR.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	T[8:0]								
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8 to 0	T[8:0]	H'000	R	Indicate the number of data bytes remaining in SCBFTDR. H'000 shows that SCBFTDR contains no transmit data, and H'100 shows that SCBFTDR is filled with transmit data.

22.3.13 Receive FIFO Data Count Register (SCBRFDR)

SCBRFDR is a 16-bit read-only register that indicates the number of data bytes stored in SCBFRDR.

The R8 to R0 bits indicate the number of receive data in SCBFRDR.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	R[8:0]								
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8 to 0	R[8:0]	H'000	R	Indicate the number of data bytes remaining in SCBFRDR. H'000 shows that SCBFRDR contains no receive data, and H'100 shows that SCBFRDR is filled with receive data.

22.3.14 Transmit FIFO Data Register (SCBFTDR)

SCBFTDR is an 8-bit 256-stage FIFO data register that stores data for serial transmission.

If SCBTSR is empty when transmit data has been written to SCBFTDR, the SCIFB transfers the transmit data written in SCBFTDR to SCBTSR and starts serial transmission.

SCBFTDR is a write-only register, and cannot be read by the CPU.

The next data cannot be written when SCBFTDR is filled with 256 bytes of transmit data. Data written in this case is ignored.

Bit:	7	6	5	4	3	2	1	0
	SCFTD[7:0]							
Initial value:	—	—	—	—	—	—	—	—
R/W:	W	W	W	W	W	W	W	W

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	SCFTD[7:0]	Undefined	W	Serial transmit data FIFO

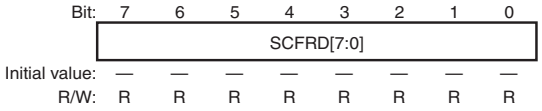
22.3.15 Receive FIFO Data Register (SCBFRDR)

SCBFRDR is a 256-stage FIFO register that stores received serial data.

When the SCIFB has received one byte of serial data, it transfers the received data from SCBRSR to SCBFRDR where it is stored, and completes the receive operation. SCBRSR is then enabled for reception, and consecutive receive operations can be performed until SCBFRDR is full (256-byte data).

SCBFRDR is a read-only register, and cannot be written to by the CPU.

If a read is performed when there is no receive data in SCBFRDR, an undefined value will be returned. When SCBFRDR is full of receive data, subsequent serial data is lost.



Bit	Bit Name	Initial Value	R/W	Description
7 to 0	SCFRD[7:0]	Undefined	R	Serial receive data FIFO

22.4 Operation

22.4.1 Overview

The SCIFB supports serial communications in asynchronous mode, in which synchronization is achieved character by character, and in clocked synchronous mode, in which synchronization is achieved with clock pulses. 256-stage FIFO buffers are provided for both transmission and reception, reducing the CPU overhead and enabling high-speed continuous communications.

22.4.2 Asynchronous Mode

In the asynchronous mode , the transfer format is selected by the setting in SCBSMR as shown in Table 22.5. Features in this mode are as follows.

- Data length: 7 or 8 bits
- The addition of parity (even, odd or none) and the choice of stop-bit length (1 or 2 bits), along with the data length, determine the transfer format and character length.
- Receive error detection: Framing, parity, and overrun errors, receive-FIFO-data-full, receive-data-ready, and breaks.
- Independent indications of the number of data stored in the transmit and receive FIFO registers.
- Serial clock source: Internal clock signal generated by the baud-rate generator.

Table 22.5 SCBSMR Settings for Serial Transfer Format Selection

SCBSMR Setting					SCIFB Transfer Format		
Bit 7	Bit 6	Bit 5	Bit 3		Data Length	Parity Bit	Stop Bit Length
C/A	CHR	PE	STOP	Mode			
0	0	0	0	Asynchronous mode	8-bit data	None	1 bits
			1				2 bits
		1	0			Provided	1 bits
			1				2 bits
	1	0	0		7-bit data	None	1 bits
			1				2 bits
		1	0			Provided	1 bits
			1				2 bits
1	*	*	*	Clocked synchronous mode	8-bit data	None	None

Note: * Don't care

22.4.3 Serial Operation in Asynchronous Mode

(1) Data Transfer Format

Table 22.6 shows the transfer formats that can be used in asynchronous mode. Any of eight transfer formats can be selected according to the SCBSMR settings.

Table 22.6 Serial Transfer Formats

SCBSMR setting			Serial transfer format and frame length
CHR	PE	STOP	1 2 3 4 5 6 7 8 9 10 11 12
0	0	0	START 8 bit data STOP
		1	START 8 bit data STOP STOP
	1	0	START 8 bit data P STOP
		1	START 8 bit data P STOP STOP
1	0	0	START 7 bit data STOP
		1	START 7 bit data STOP STOP
	1	0	START 7 bit data P STOP
		1	START 7 bit data P STOP STOP

(2) Clock

An internal clock signal generated by the on-chip baud-rate generator provides the transfer clock for SCIFB.

(3) Data Transfer Operations:

1. SCIFB initialization

   Before transmitting and receiving data, it is necessary to clear the TE and RE bits in SCBSCR to 0, and then initialize the SCIFB as described below.

   When the transfer format, etc., is changed, the TE and RE bits must be cleared to 0 before making the change using the following procedure. When the TE bit is cleared to 0, SCBTSR is initialized. Note that clearing the TE and RE bits to 0 does not change the contents of SCBSSR, SCBFTDR, or SCBFRDR. The TE bit should be cleared to 0 after all transmit data has been sent and the TEND bit in SCBSSR has been set to 1. Clearing to 0 can also be performed during transmission, but the data lines that transmit the data will go to the high-impedance state after the clearance. Before setting TE to 1 again to start transmission, the TFRST bit in SCBFCR should first be set to 1 to reset SCBFTDR.

   Figure 22.2 shows a sample SCIFB initialization flowchart.

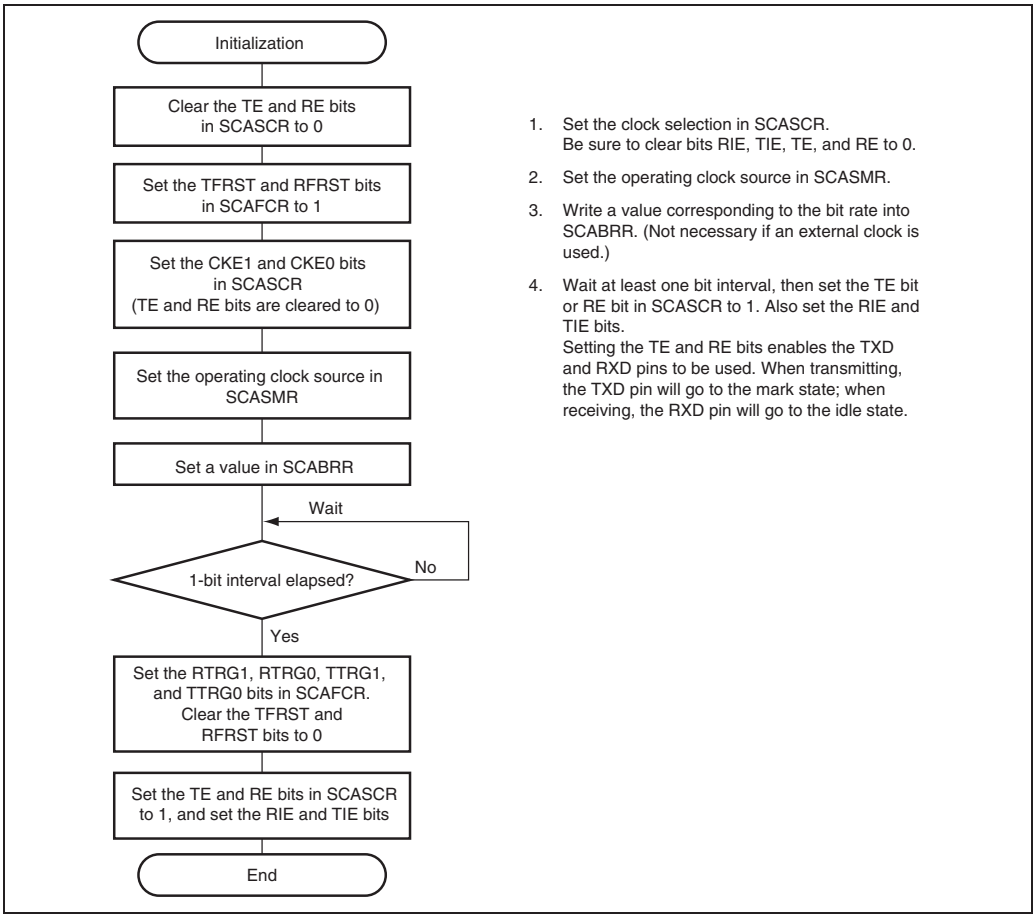


Figure 22.2 Sample SCIFB Initialization Flowchart

2. Serial data transmission

   Figure 22.3 shows a sample flowchart for serial transmission.

   Use the following procedure for serial data transmission after enabling the SCIFB for transmission.

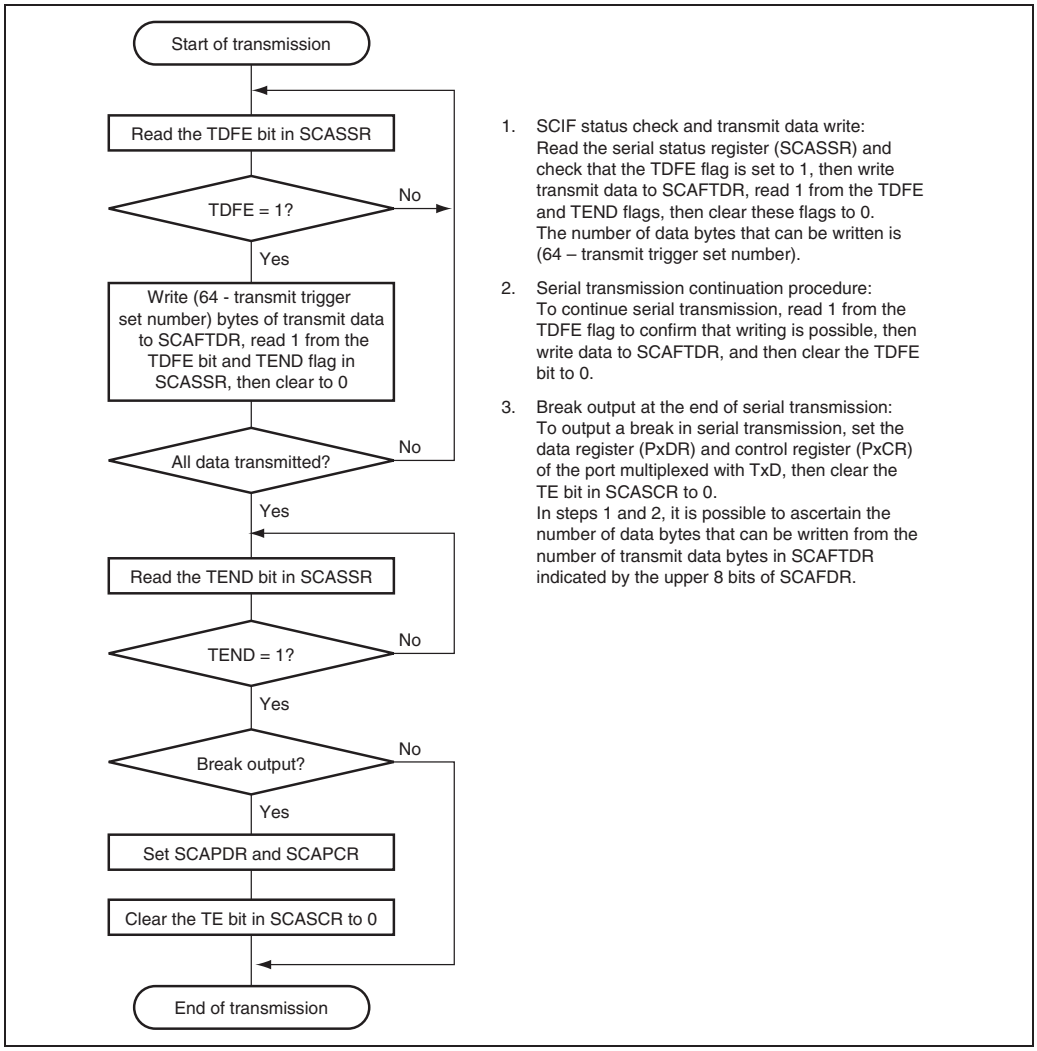


Figure 22.3 Sample Serial Transmission Flowchart

In serial transmission, the SCIFB operates as described below.

A. When data is written into SCBFTDR, the SCIFB transfers the data from SCBFTDR to SCBTSR and starts transmitting. Confirm that the TDFE flag in SCBSSR is set to 1 before writing transmit data to SCBFTDR. The number of data bytes that can be written is not less than (256 – transmit trigger set number).

B. When data is transferred from SCBFTDR to SCBTSR and transmission is started, consecutive transmit operations are performed until there is no transmit data left in SCBFTDR. When the number of transmit data bytes in SCBFTDR falls to or below the transmit trigger number set in SCBFCR, the TDFE flag is set. If the TIE bit in SCBSCR is set to 1 at this time, a transmit-FIFO-data-empty interrupt (TXI) request is generated.

When the transmit data stop function is used and the number of data bytes set in SCBTDSR is matched, transmit operation is stopped and the TSF flag in SCBSSR is set. If the TSIE bit in SCBSCR is set to 1, a transmit-data-stop-interrupt (TDI) request is generated. The vectors of TXI and TDI are the same.

The serial transmit data is sent from the TxD pin in the following order.

a. Start bit: One logic-0 bit is output.
b. Transmit data: 8-bit or 7-bit data is output in LSB-first order.
c. Parity bit: One parity bit (even or odd parity) is output.
d. A format in which a parity bit is not output can also be selected.
e. Stop bit(s): One or two logic-1 bits (stop bits) are output.
f. Mark state: Output of 1 is continued until the start bit is sent to start the next transmission.

C. The SCIFB checks the SCBFTDR transmit data at the timing for sending the stop bit. If data is present, the data is transferred from SCBFTDR to SCBTSR, the stop bit is sent, and then serial transmission of the next frame is started.

If there is no transmit data, the TEND flag in SCBSSR is set to 1, the stop bit is sent, and then the line goes to the mark state in which 1 is output.

Figure 22.4 shows an example of the operation for transmission in asynchronous mode.

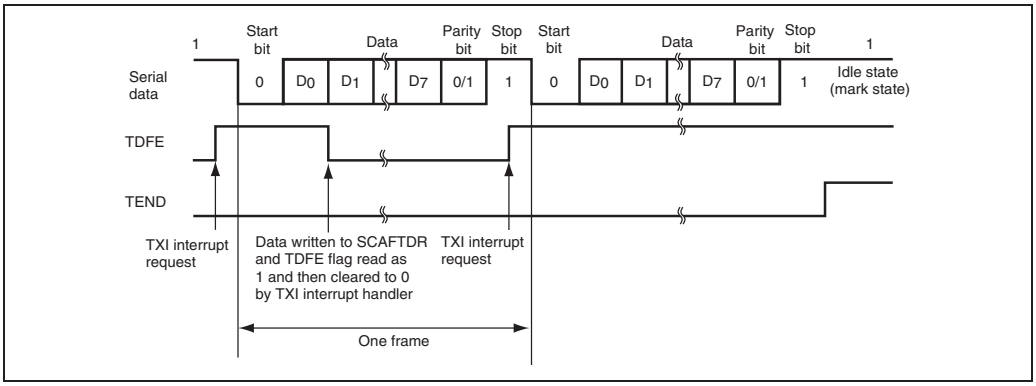


Figure 22.4 Example of Transmit Operation (Example with 8-Bit Data, Parity, One Stop Bit)

- Transmit data stop function

  When the value in SCBTDSR equals the number of transmitted data bytes, this function stops the transmit operation. Interrupts can be generated and the DMAC can be activated by setting the TSIE bit (interrupt enable bit) to 1.

  Figure 22.5 shows an example of operation for the transmit data stop function.

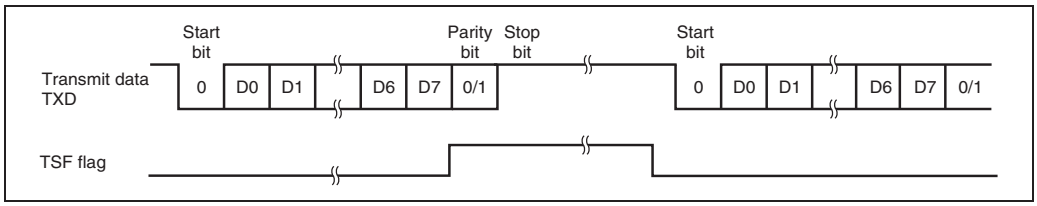


Figure 22.5 Example of Transmit Data Stop Function

Figure 22.6 shows a flowchart for the transmit data stop function.

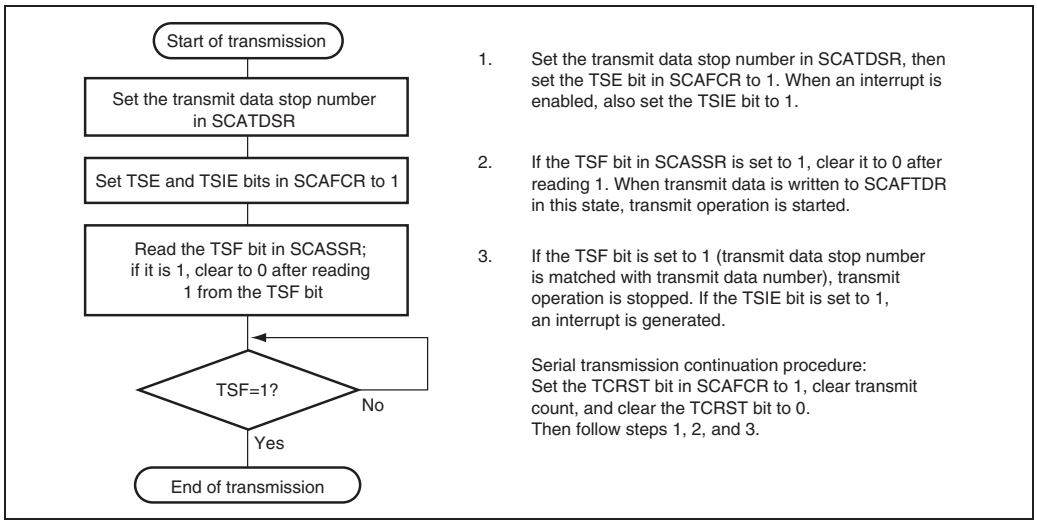


Figure 22.6 Transmit Data Stop Function Flowchart

3. Serial data reception

Figures 20.7 and 20.8 show sample flowcharts for serial reception.

Use the following procedure for serial data reception after enabling the SCIFB for reception.

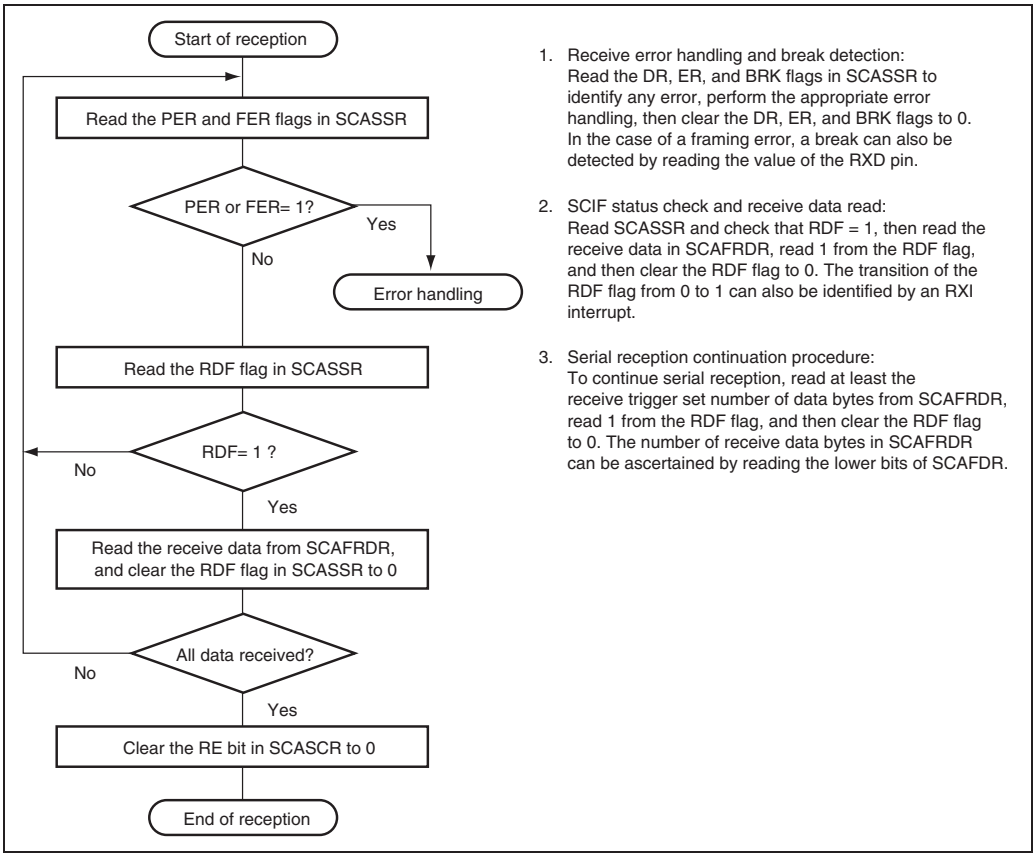


Figure 22.7 Sample Serial Reception Flowchart (1)

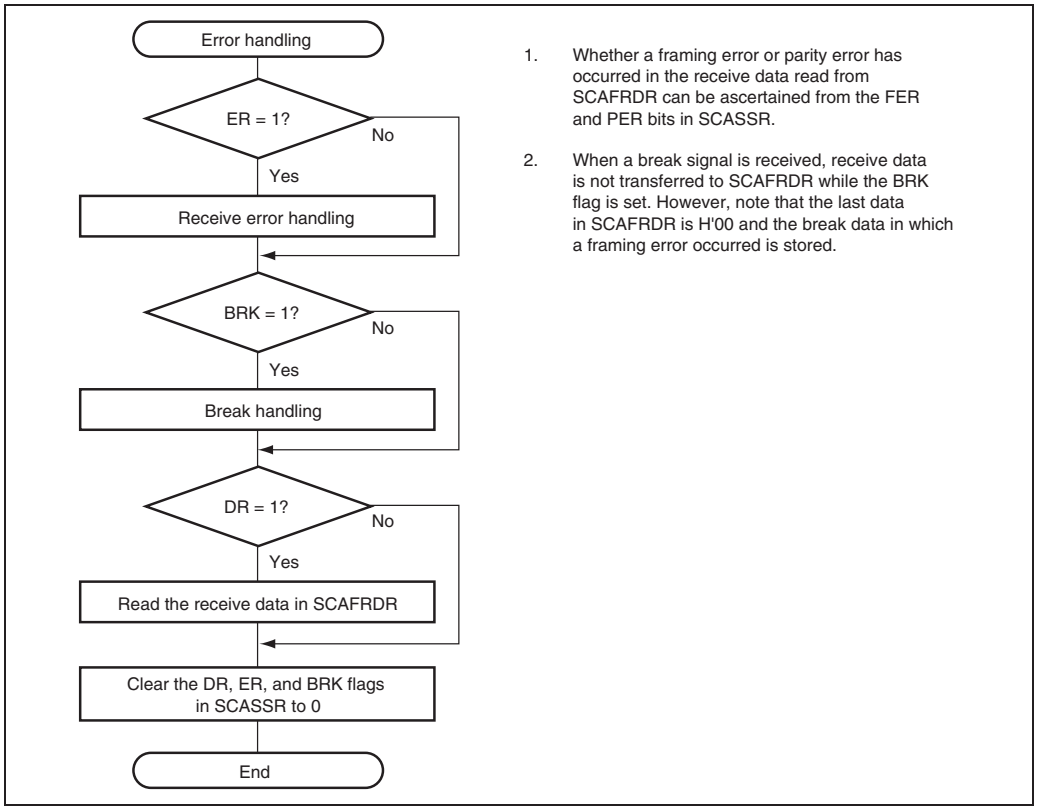


Figure 22.8 Sample Serial Reception Flowchart (2)

In serial reception, the SCIFB operates as described below.

A. The SCIFB monitors the communication line, and if a 0 start bit is detected, performs internal synchronization and starts reception.

B. The received data is stored in SCBRSR in LSB-to-MSB order.

C. The parity bit and stop bit are received.

After receiving these bits, the SCIFB carries out the following checks.

a. Stop bit check: The SCIFB checks to see if the value in the stop bit position is 1. If the two-stop-bit setting has been made, only the value in the first stop-bit position is checked.

b. The SCIFB checks whether received data can be transferred from SCBRSR to SCBFRDR.

c. Break check: The SCIFB checks to confirm that the BRK flag is 0, indicating that the SCIFB is not in the break state.

If all the above checks are passed, the receive data is stored in SCBFRDR.

Note: Reception continues when a receive error (framing error or parity error) occurs.

D. If the RIE bit in SCBSCR is set to 1 when the RDF flag changes to 1, a receive-FIFO-data-full interrupt (RXI) request is generated.

If the ERIE bit in SCBSCR is set to 1 when the ER flag changes to 1, a receive-error interrupt (ERI) request is generated.

If the BRIE bit in SCBSCR is set to 1 when the BRK flag changes to 1, a break reception interrupt (BRI) request is generated.

If the DRIE bit in SCBSCR is set to 1 when the DR flag changes to 1, a receive-data-ready interrupt (DRI) request is generated.

The vectors of each interrupt source are the same.

Figure 22.9 shows an example of the operation for reception in asynchronous mode.

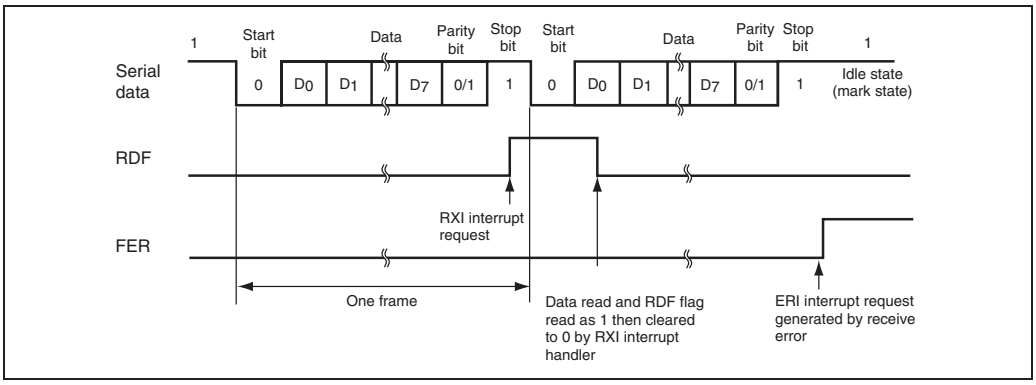


Figure 22.9 Example of SCIFB Receive Operation (Example with 8-Bit Data, Parity, One Stop Bit)

The SCIFB has a modem function that allows the stoppage and resumption of transmission according to the input value of CTS_N. Setting CTS_N to 1 places the transmission line in the mark state after transmission of the current frame. When CTS_N is set to 0, the next frame for transmission is output, with a start bit as its leader.

Figure 22.10 shows an example of the operation of CTS_N control.

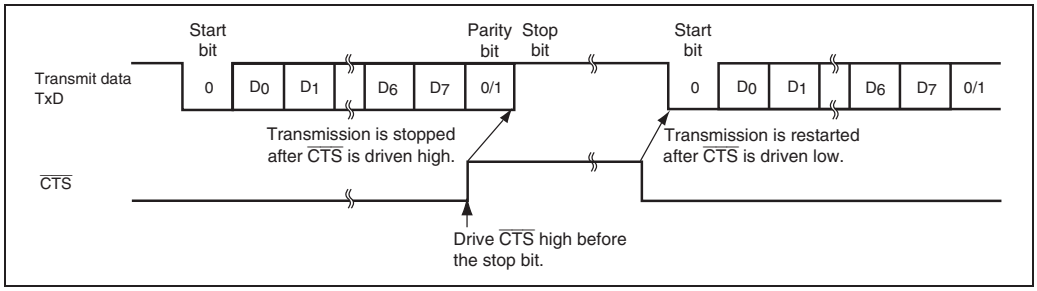


Figure 22.10 Example of CTS_N Control Operation

The RTS_N signal is driven high when the modem function is in use and the received data stored in the receive FIFO register (SCBFRDR) equals or exceeds the number of the RTS_N output triggers.

Figure 22.11 shows an example of the operation for RTS_N control.

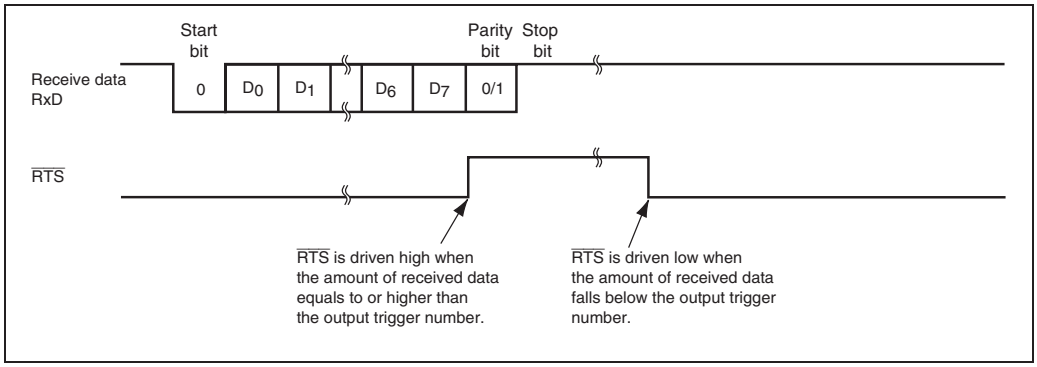


Figure 22.11 Example of RTS_N Control Operation

22.4.4 Operation in Clocked Synchronous Mode

Clocked synchronous mode, in which data is transmitted or received in synchronization with clock pulses, is suitable for fast serial communications.

Since the transmitter and receiver are independent units in SCIFB, full-duplex communications can be achieved by sharing the clock. Both the transmitter and receiver have a 256-stage FIFO buffer structure, so that data can be read or written during transmission or reception, enabling continuous data transmission and reception.

Through the setting of the CKEDG bit, the format for clocked synchronous communications can be selected.

Figures 20.12 and 20.13 show the format for clocked synchronous communications.

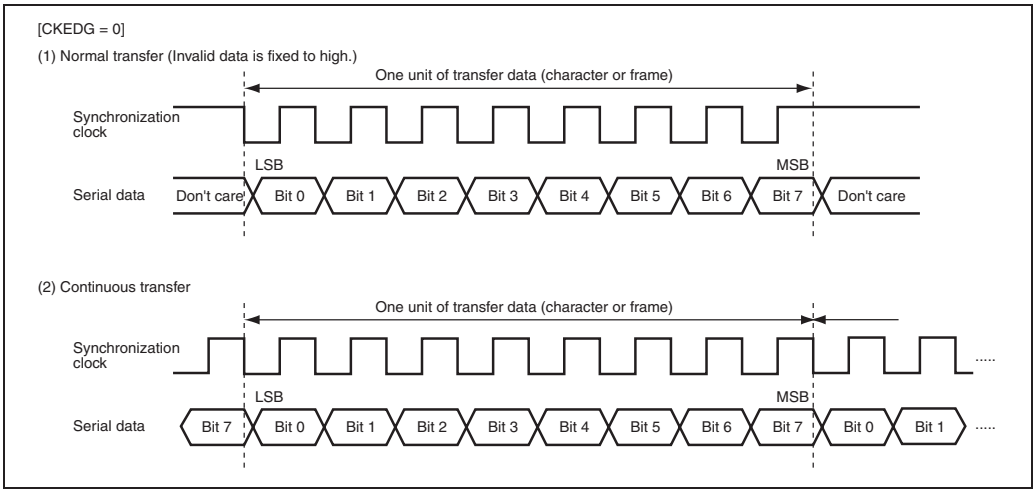


Figure 22.12 Data Format in Clocked Synchronous Communications (CKEDG = 0)

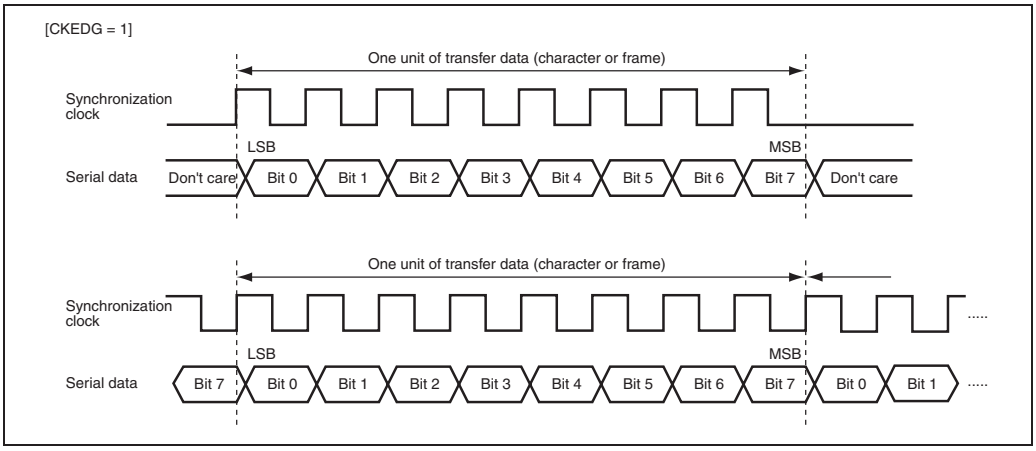


Figure 22.13 Data Format in Clocked Synchronous Communications (CKEDG = 1)

In clock synchronous serial communications, the data on the communications line is latched on one edge selected by the CKEDG bit in SCBSMR and is output until the next edge. Accuracy of data is guaranteed on the next edge (i.e. that in the opposite direction to the latching edge).

In serial communications, each character is output starting with the LSB and ending with the MSB. After the MSB is output, the communications line remains in the state of the last bit.

Data is received on the opposite edge to that on which data is output.

(1) Data Transfer Format

A fixed 8-bit data format is used. No parity bit can be added.

(2) Clock

An internal clock signal generated by the on-chip baud-rate generator provides the transfer clock for SCIFB. For details on SCIFB clock source selection, see Table 22.5.

(3) SCIFB Initialization (Clocked Synchronous Mode)

Before transmitting and receiving data, it is necessary to clear the TE and RE bits in SCBSCR to 0, and then initialize the SCIFB as described below.

When changing the operating mode or transfer format, etc., the TE and RE bits must be cleared to 0 before making the change using the following procedure. When the TE bit is cleared to 0, SCBTSR is initialized. Note that clearing the RE bit to 0 does not initialize the RDF, PER, FER, or ORER flag state or change the contents of SCBFRDR.

Figure 22.14 shows a sample SCIFB initialization flowchart.

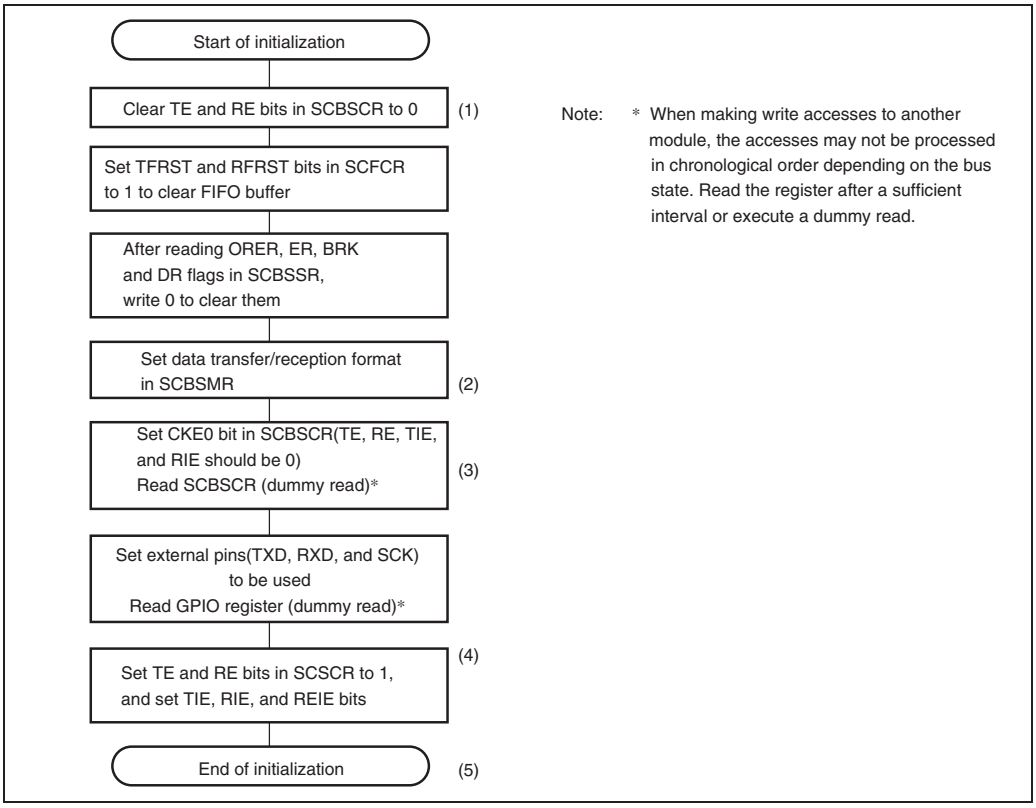


Figure 22.14 Sample SCIFB Initialization Flowchart

(4) Serial Data Transmission (Clocked Synchronous Mode)

Figure 22.15 shows a sample flowchart for serial transmission.

Use the following procedure for serial data transmission after enabling the SCIFB for transmission.

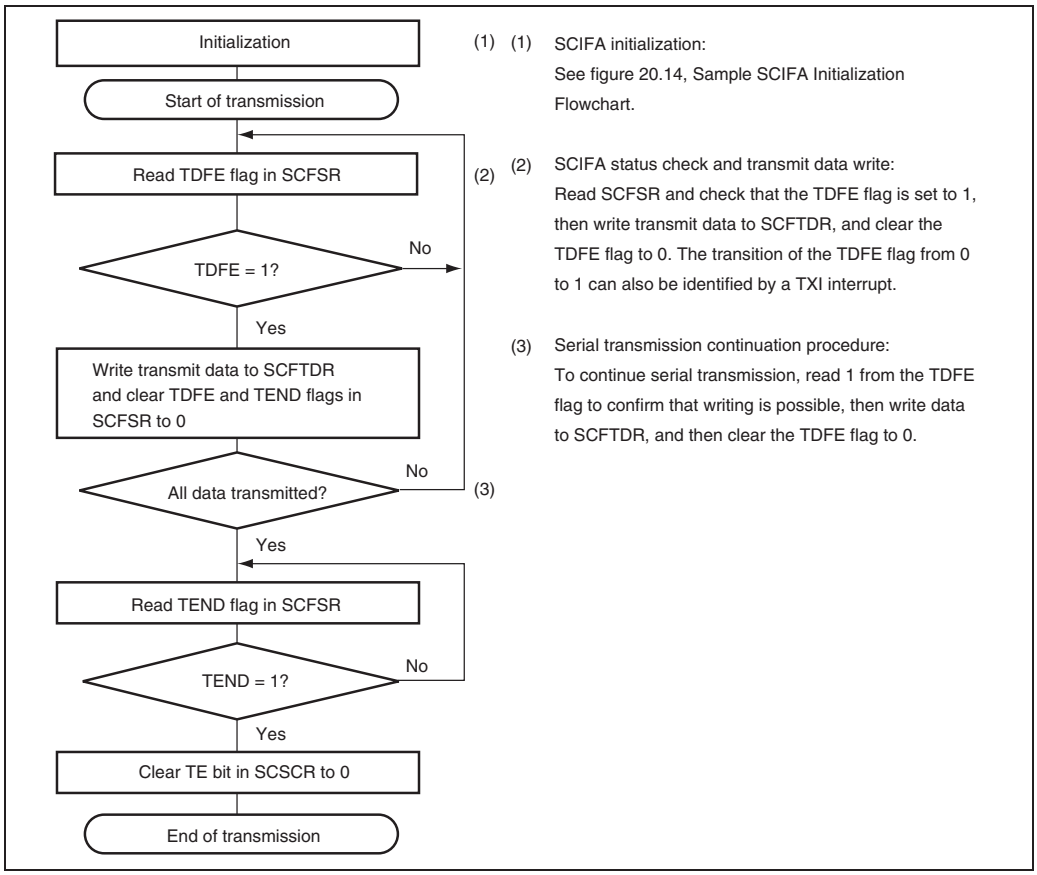


Figure 22.15 Sample Serial Transmission Flowchart

In serial transmission, the SCIFB operates as described below.

1. When data is written into SCBFTDR, the SCIFB transfers data from SCBFTDR to SCTSR and starts transmitting. Confirm that the TDFE flag in SCBSSR is set to 1 before writing transmit data to SCBFTDR. The number of data bytes that can be written is at least 16 – (transmit trigger set number).
2. When data is transferred from SCBFTDR to SCTSR and transmission is started, consecutive transmit operations are performed until there is no transmit data left in SCBFTDR. When the number of transmit data bytes in SCBFTDR falls to or below the transmit trigger number set in SCBFCR, the TDFE flag is set. If the TIE bit in SCBSCR is set to 1 at this time, a transmit-FIFO-data-empty interrupt (TXI) request is generated.

   The SCIFB outputs data in synchronization with the input clock.

   The serial transmit data is sent from the TXD pin in the LSB-first order.
3. The SCIFB checks the SCBFTDR transmit data at the timing for sending the last bit. If data is present, the data is transferred from SCBFTDR to SCTSR, and then serial transmission of the next frame is started. If there is no transmit data, the TEND flag in SCBSSR is set to 1 after the last bit is sent, and the transmit data pin (TXD pin) retains the output state of the last bit.

Figure 22.16 shows an example of the SCIFB operation for transmission in clocked synchronous mode.

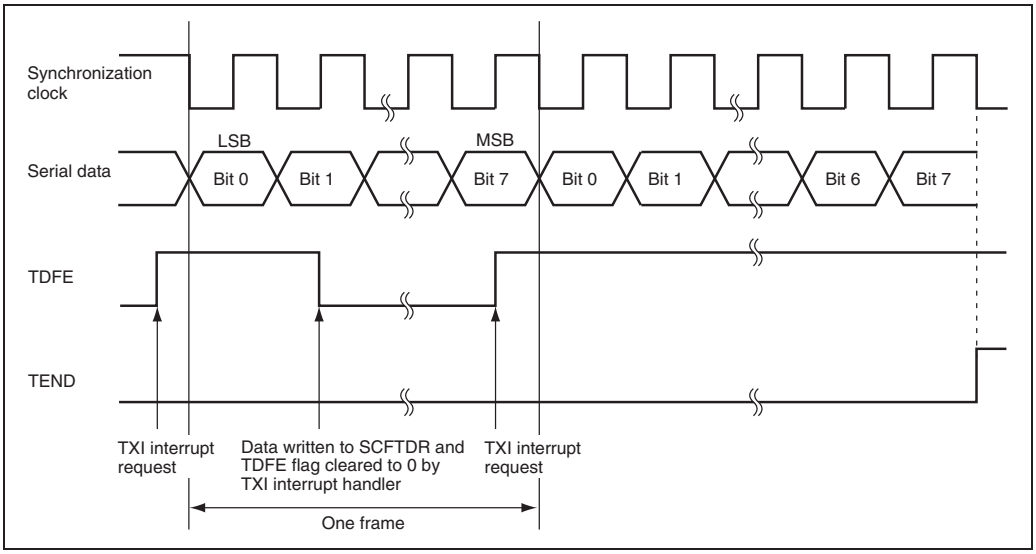


Figure 22.16 Sample SCIFB Transmission Operation in Clocked Synchronous Mode

(5) Serial Data Reception (Clocked Synchronous Mode)

Figures 20.17 and 20.18 show sample flowcharts for serial reception.

Use the following procedure for serial data reception after enabling the SCIFB for reception.

When switching the operating mode from asynchronous mode to clocked synchronous mode without initializing SCIFB, make sure that the ORER flag in SCBSSR, and PERC and FERC flags in SCLSR are cleared to 0.

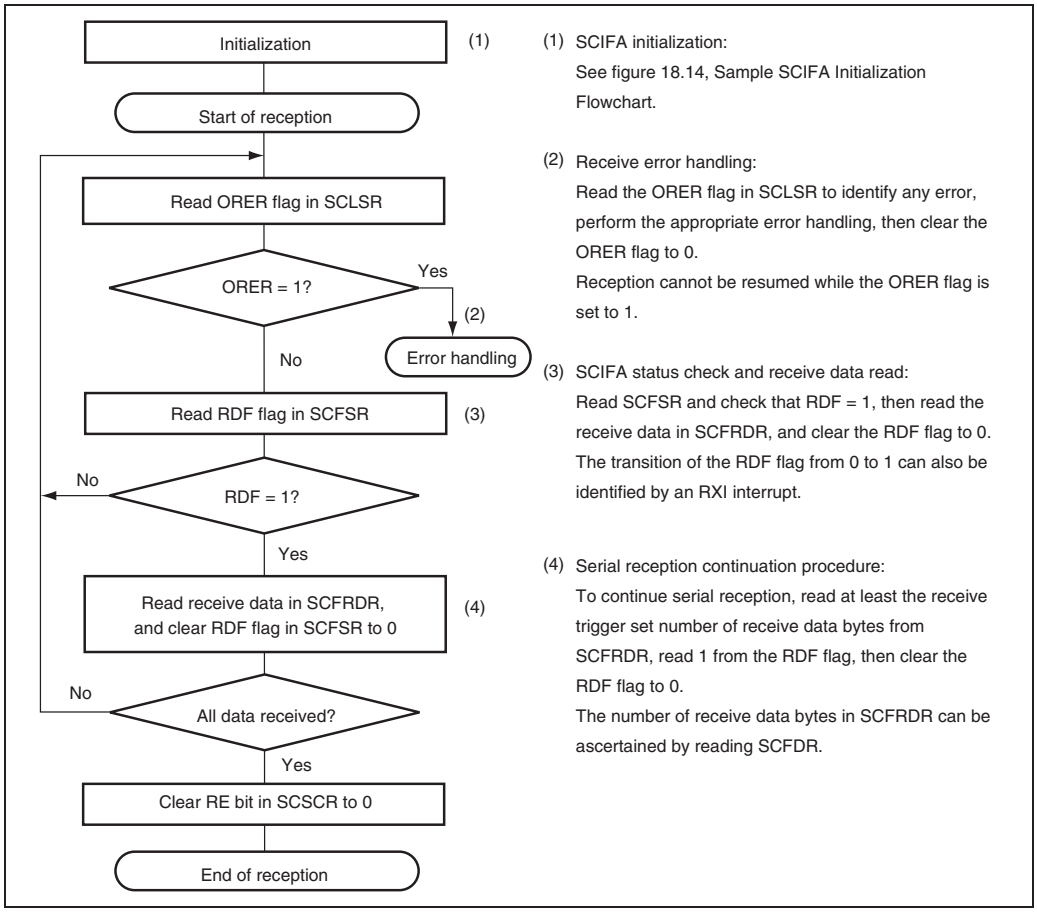


Figure 22.17 Sample Serial Reception Flowchart (1)

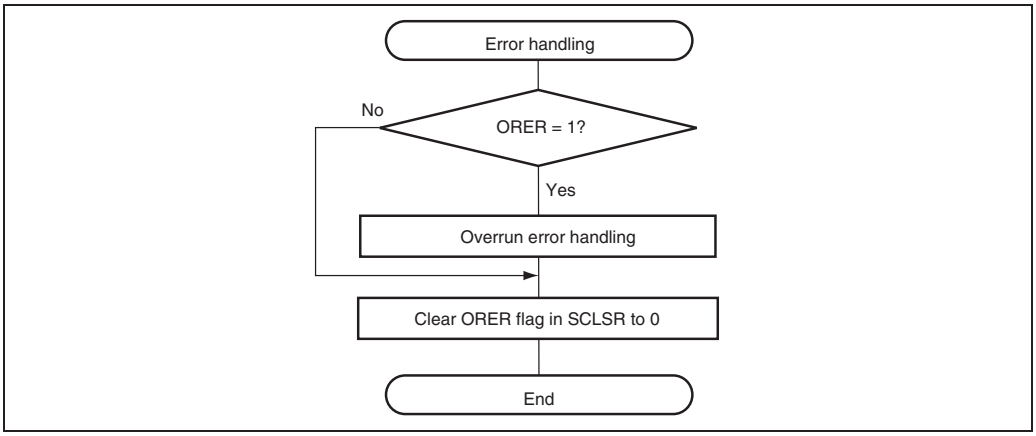


Figure 22.18 Sample Serial Reception Flowchart (2)

In serial reception, the SCIFB operates as described below.

1. The SCIFB starts reception in synchronization with the output of the synchronization clock.
2. The received data is stored in SCRSR in LSB-to-MSB order.
   After receiving the data, the SCIFB checks whether the receive data can be transferred from SCRSR to SCBFRDR. If this check is passed, the receive data is stored in SCBFRDR. If an overrun error is detected in the error check, reception cannot continue.
3. If the RIE bit in SCBSCR is set to 1 when the RDF flag changes to 1, a receive-FIFO-data-full interrupt (RXI) request is generated.
   If the RIE or ERIE bit in SCBSCR is set to 1 when the ORER flag changes to 1, a break interrupt (BRI) request is generated.

Figure 22.19 shows an example of the operation for reception in clocked synchronous mode.

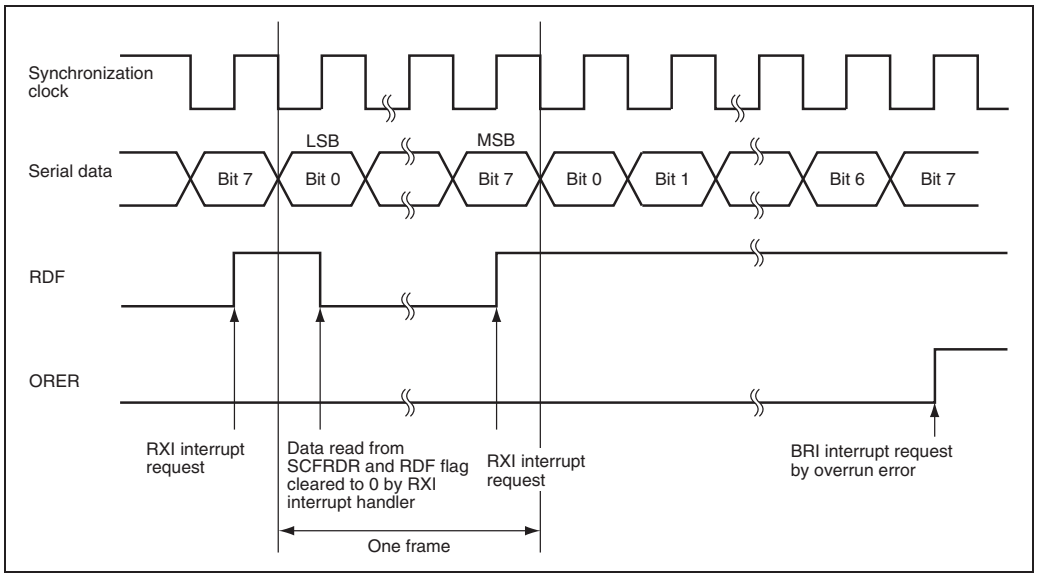


Figure 22.19 Sample SCIFB Reception Operation in Clocked Synchronous Mode

(6) Simultaneous Serial Data Transmission and Reception (Clocked Synchronous Mode)

Figure 22.20 shows a sample flowchart for simultaneous serial data transmission and reception.

Use the following procedure for simultaneous serial transmission and reception after enabling the SCIFB for both the transmission and reception.

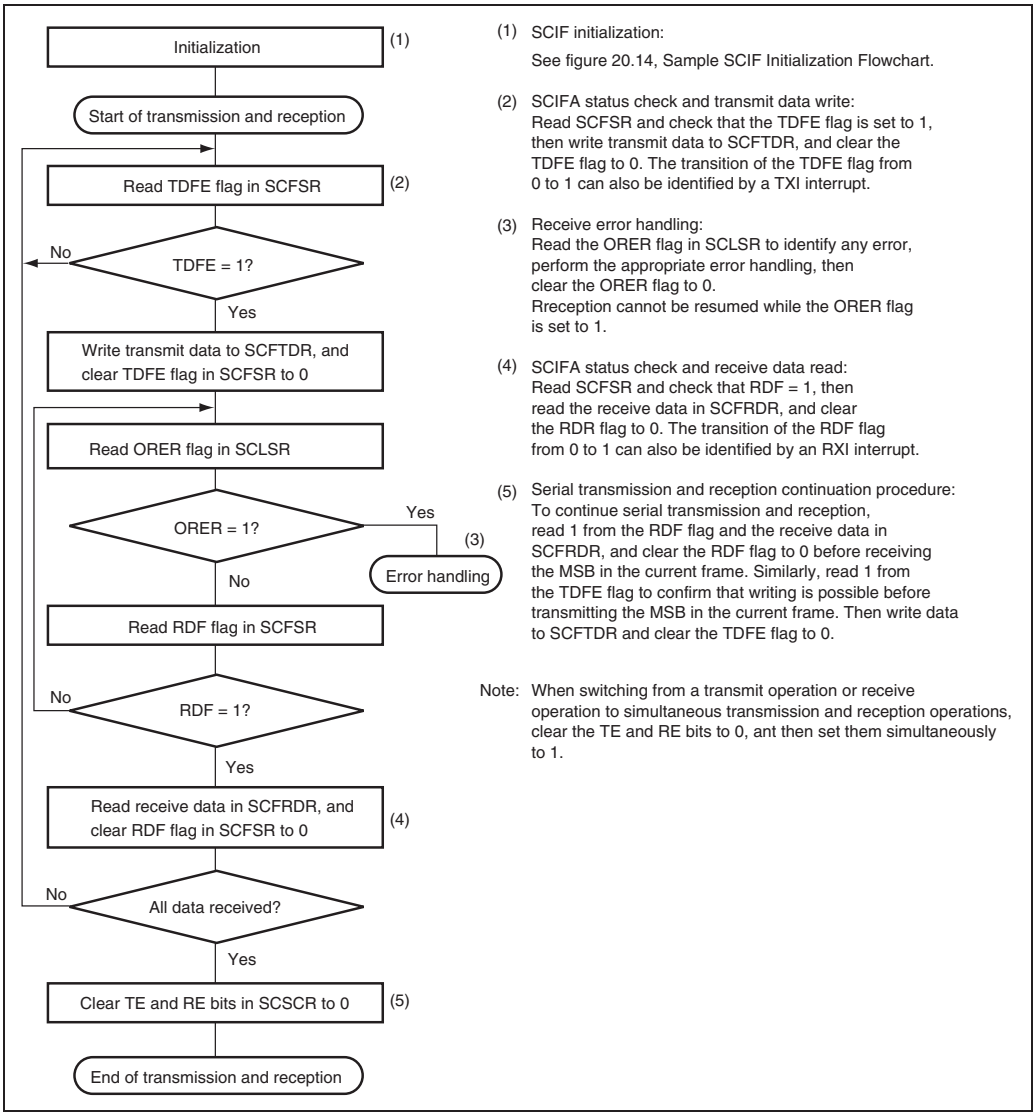


Figure 22.20 Sample Simultaneous Serial Transmission and Reception Flowchart

22.5 SCIFB Interrupt Sources and DMAC

The SCIFB supports six interrupts: transmit-FIFO-data-empty (TXI), transmit-data-stop (TDI), receive-error (ERI), receive-FIFO-data-full (RXI), break (BRI), and receive-data-ready (DRI). The vectors of each interrupt source are the same.

Table 22.7 shows the interrupt sources. The TIE, RIE, ERIE, BRIE, DRIE, and TSIE bits in SCBSCR are used to enable or disable the respective interrupt sources.

If the TDFE flag in SCBSSR is set to 1, a TXI interrupt request is generated. When the TSF flag in SCBSSR is set to 1, a TDI interrupt request is generated. The DMAC can be activated for data transfer on generation of TXI and TDI interrupt requests. When data exceeding the transmit trigger set number is written to SCBFTDR by the DMAC, the DMAC transfer request is automatically cleared to 0. The DMAC requests of TXI and TDI are the same.

When the RDF flag in SCBSSR is set to 1, an RXI interrupt request is generated. The DMAC can be activated for data transfer on generation of an RXI interrupt request. When receive data in SCBFRDR is read by the DMAC until the amount left is less than the receive trigger set number, the DMAC transfer request is automatically cleared to 0.

When using the DMAC for transmission/reception, set the DMAC to the DMAC transfer enabled state before making the SCIFB settings. Transmission/reception is complete when the DMA transfer is terminated.

When the ER, BRK, DR, or TSF flag in SCBSSR is set to 1, an interrupt request is generated. Note that the vectors of each interrupt source are the same.

Table 22.7 SCIFB Interrupt Sources

Interrupt Source Type	DMAC Activation
Interrupt initiated by receive error (ER) or break (BRK) flag	Not possible
Interrupt initiated by receive-FIFO-data-full (RDF) or receive-data-ready (DR) flag	Possible*[1]
Interrupt initiated by transmit-FIFO-data-empty (TDFE) or transmit-data-stop (TSF) flag	Possible*[2]

Notes: 1. The DMAC can only be activated by an interrupt request initiated by the receive-FIFO-data-full (RDF) flag.
2. The DMAC can only be activated by an interrupt request initiated by the transmit-FIFO-data-empty (TDFE) flag.

22.6 Multibyte Transfer

22.6.1 Basic Multibyte Settings

Table 22.8 shows the SCIFB settings and DMA settings for multibyte transfer.

Table 22.8 SCIFB Settings and DMA Settings for Multibyte Transfer

		SCIFB				DMA	
		SCBMBR		SCBFCR		DMACHCR	DMATCR
Transfer Mode	Transmission/ Reception	MBTON	MBRON	RTRG [1:0]	TTRG [1:0]	TS[3:0]	TCR[31:0]
1-byte transfer	Transmission	1	—	B'11	—	B'0000	Transfer count
	Reception	—	1	—	B'11	B'0000	Transfer count
16-byte transfer	Transmission	1	—	B'10	—	B'1010	Transfer count/16 (roundup)
	Reception	—	1	—	B'10	B'1010	Transfer count/16 (roundup)
32-byte transfer	Transmission	1	—	B'01	—	B'1101	Transfer count/32 (roundup)
	Reception	—	1	—	B'01	B'1101	Transfer count/32 (roundup)

22.6.2 Transfer Count Definition

(1) Number of Transfer Data Bytes for Transmission

In 16-byte or 32-byte transfer mode, data more than the transfer count is transferred to the transmit FIFO buffer. Therefore, define the transfer count in SCBTDSR, and set the TSE bit in SCBFCR to 1 to enable the transmit data stop function before starting DMA transfer.

(2) Number of Transfer Data Bytes for Reception

In 16-byte or 32-byte transfer mode, when the receive data remaining in the receive FIFO buffer is less than 16 bytes (or 32 bytes), the data is still left in the FIFO buffer. When the RCEF bit in SCBSSR is set to 1 by setting the RCE bit in SCBFCR and the RCECRON bit in SCBMBR to 1, 16-byte (or 32-byte) transfer requests are made continuously to the DMAC until the receive FIFO buffer becomes empty. In this case, the DMAC attempts to transfer data more than the number of received data bytes, causing an underflow error.

When the ADDREQ bit in SCBMBR is set to 1 after the reception is completed, 16-byte (or 32-byte) transfer requests are made to the DMAC until the receive FIFO buffer becomes empty.

22.7 Usage Notes

Note the following when using SCIFB.

(1) Writing Data to SCBFTDR and TDFE Flag

The TDFE flag in SCBSSR is set when the number of transmit data bytes written in SCBFTDR has fallen to or below the transmit trigger number set by bits TTRG1 and TTRG0 in SCBFCR. After TDFE is set, transmit data up to the number of empty bytes in SCBFTDR can be written, allowing efficient continuous transmission.

However, if the number of data bytes written in SCBFTDR is equal to or less than the transmit trigger number, the TDFE flag will be set to 1 again after being read as 1 and cleared to 0. TDFE should therefore be cleared when SCBFTDR contains transmit data more than the transmit trigger number bytes.

The number of transmit data bytes in SCBFTDR is indicated by the T8 to T0 bits in SCBTFDR.

(2) Reading Data from SCBFRDR and RDF Flag

The RDF flag in SCBSSR is set when the number of receive data bytes in SCBFRDR has become equal to or greater than the receive trigger number set by bits RTRG1 and RTRG0 in SCBFCR. After RDF is set, receive data equivalent to the trigger number can be read from SCBFRDR, allowing efficient continuous reception.

However, if the number of data bytes in SCBFRDR is still equal to or greater than the trigger number after a read, the RDF flag will be set to 1 again if it is cleared to 0. RDF should therefore be cleared to 0 after being read as 1 after all receive data has been read.

The number of receive data bytes in SCBFRDR is indicated by the R8 to R0 bits in SCBRFDR.

(3) Break Detection and Processing

Break signals can be detected by reading the RxD pin directly when a framing error (FER) is detected. Since the input from the RxD pin is always 0 in the break state, the FER flag is set and the parity error (PER) flag may also be set.

Although the SCIFB stops transferring receive data to SCBFRDR after receiving a break, it continues the receive operation.

(4) Receive Data Sampling Timing and Receive Margin

As an example, when the sampling rate is 1/16, the SCIFB operates on a base clock with a frequency of 8 times the transfer rate.

In reception, the SCIFB synchronizes internally by sampling the fall of the start bit with the base clock. Receive data is latched at the rising edge of the eighth base clock pulse (when the sampling rate is 1/16).

The receive data sampling timing is shown in Figure 22.21.

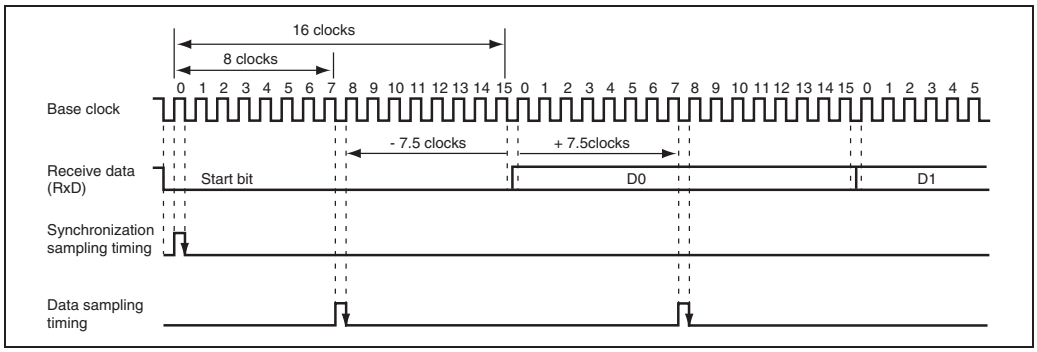


Figure 22.21 Receive Data Sampling Timing

The receive margin can therefore be expressed as shown in equation (1).

$$M = \left| \left(0.5 - \frac{1}{2N}\right) - (L - 0.5)F - \frac{|D - 0.5|}{N}(1 + F) \right| \times 100\% \ldots\ldots (1)$$

M: Receive margin (%)

N: Ratio of clock frequency to bit rate (N = 16)

D: Clock duty cycle (D = 0 to 1.0)

L: Frame length (L = 9 to 12)

F: Absolute deviation of clock frequency

From equation (1), if F = 0 and D = 0.5, the receive margin is 46.875%, as given by equation (2).

When D = 0.5 and F = 0:

$M = (0.5 - 1/(2 \times 16)) \times 100\% = 46.875\% \ldots\ldots (2)$

This is a theoretical value. A reasonable margin to allow in system designs is the value above (46.875%) plus 20 to 30%.

(5) PAD Pin when the Pin for SCIFB Is Selected

The table below shows the PAD pin state when the pin for the SCIFB is selected.

When the pin for SCIFB is selected	TXD	RXD	RTS_N	CTS_N	SCK
PAD enable	1 (enable)	1 (enable)	MCE in SCBFCR (Initial value: 0, disable)	MCE in SCBFCR (Initial value: 0, disable)	CKE0 in SCBSCR (Initial value: 0, disable)
Pin state	Output (initial value: 1)	Input	Hi-Z	Input	Hi-Z
Pull Up/Down	—	Pull-up required	—	Pull-up required	—
Remarks	—	SCIF fixes RXD to 1 internally when RE in SCBSCR = 0.	—	SCIF fixes CTS_N to 0 internally when MCE in SCBFCR = 0	—

Section 23 Clock-Synchronized Serial Interface with FIFO (MSIOF0, MSIOF1 and MSIOF2)

This LSI includes three-channel clock-synchronized serial I/O module with FIFO (MSIOF0/MSIOF1/MSIOF2).

23.1 Features

- MSIOF0 in the realtime domain and MSIOF1/2 in the system domain

- FIFO capacity: 32 bits × 64 stages for transmission and 32 bits × 256 stages for reception
- MSB first or LSB first selectable for data transmission and reception
- Synchronization by frame synchronization pulse, level, or left/right channel switch
- Supports both master and slave modes
- Independent clock and synchronization signals for transmission and reception (common clock and synchronization signals are also selectable)
- Supports multiple-channel communication
  - Transfers multiple groups or words of data in one frame.
  - The word data size for each group can be selected from eight to 32 bits
  - Up to 256 words can be transferred in each group when one or two groups are used, or up to 16 words can be transferred in each group when three or four groups are used.
- Interrupts: One type
- Serial clock

  The internal clock (SUBϕ) or external pin input (MSIOF_MCK0 or MSIOF_MCK1) can be selected as the clock source.
- DMA transfer

  Supports multibyte DMA transfer.
  Supports DMA transfer by a transfer request for transmission and reception
- Serial format

  Supports serial formats such as IIS, SPI (for both master and slave modes), and μWIRE.
- CLK/SYNC in independent transmit/receive mode
  - Up to 12 MHz for both transmission and reception
- CLK/SYNC (SPI) in common transmit/receive mode
  - Up to 12 MHz for transmission alone
  - Up to 6 MHz for reception

Figure 23.1 shows a block diagram of the MSIOF.

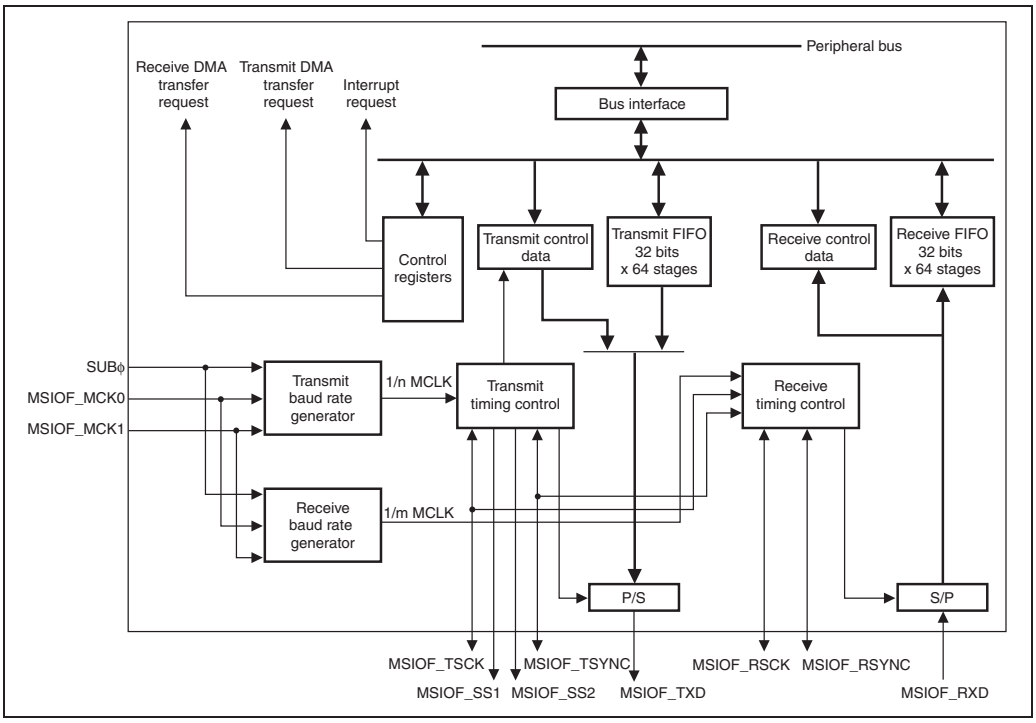


Figure 23.1 Block Diagram of MSIOF

23.2 Input/Output Pins

The pin configuration in this module is shown in table 23.1.

Table 23.1 Pin Configuration

Name	Abbreviation*	I/O	Function
MSIOF0_MCK0 MSIOF0L_MCK0		Input	MSIOF0 master clock input 0
MSIOF0_MCK1 MSIOF0L_MCK1		Input	MSIOF0 master clock input 1
MSIOF0_TSCK (MSIOFSCK) (SCK) MSIOF0L_TSCK (MSIOFSCK) (SCK)	SCK	I/O	MSIOF0 serial clock for transmission Works as SCK when a common clock is used for transmission and reception.
MSIOF0_TSYNC (SS0) MSIOF0L_TSYNC (SS0)	$\overline{\text{SS0}}$	I/O	MSIOF0 frame synchronization signal channel 0 for transmission Works as SYNC when a common synchronization signal is used for transmission and reception.
MSIOF0_SS1 (SS1) MSIOF0L_SS1 (SS1)	$\overline{\text{SS1}}$	Output	MSIOF0 frame synchronization signal channel 1 for transmission This signal works only master transmission mode.
MSIOF0_SS2 (SS2) MSIOF0L_SS2 (SS2)	$\overline{\text{SS2}}$	Output	MSIOF0 frame synchronization signal channel 2 for transmission This signal works only master transmission mode.
MSIOF0_RSCK MSIOF0L_RSCK		I/O	MSIOF0 serial clock for reception
MSIOF0_RSYNC MSIOF0L_RSYNC		I/O	MSIOF0 frame synchronization signal for reception

Name	Abbreviation*	I/O	Function
MSIOF0_TXD (MOSI/MISO)	MOSI/MISO	Output	MSIOF0 transmit data
MSIOF0L_TXD (MOSI/MISO)			
MSIOF0_RXD (MISO/MOSI)	MISO/MOSI	Input	MSIOF0 receive data
MSIOF0L_RXD (MISO/MOSI)			
MSIOF1_MCK0		Input	MSIOF0 master clock input 0
MSIOF1_MCK1		Input	MSIOF0 master clock input 1
MSIOF1_TSCK (MSIOFSCK) (SCK)	SCK	I/O	MSIOF0 serial clock for transmission Works as SCK when a common clock is used for transmission and reception.
MSIOF1_TSYNC (SS0)	$\overline{SS0}$	I/O	MSIOF0 frame synchronization signal channel 0 for transmission Works as SYNC when a common synchronization signal is used for transmission and reception.
MSIOF1_SS1 (SS1)	$\overline{SS1}$	Output	MSIOF0 frame synchronization signal channel 1 for transmission This signal works only master transmission mode.
MSIOF1_SS2 (SS2)	$\overline{SS2}$	Output	MSIOF0 frame synchronization signal channel 2 for transmission This signal works only master transmission mode.
MSIOF1_RSCK		I/O	MSIOF0 serial clock for reception
MSIOF1_RSYNC		I/O	MSIOF0 frame synchronization signal for reception
MSIOF1_TXD (MOSI/MISO)	MOSI/MISO	Output	MSIOF0 transmit data
MSIOF1_RXD (MISO/MOSI)	MISO/MOSI	Input	MSIOF0 receive data
MSIOF2_MCK0		Input	MSIOF2 master clock input 0

Name	Abbreviation*	I/O	Function
MSIOF2_MCK1		Input	MSIOF2 master clock input 1
MSIOF2_TSCK (MSIOFSCK) (SCK)	SCK	I/O	MSIOF2 serial clock for transmission Works as SCK when a common clock is used for transmission and reception.
MSIOF2_TSYNC (SS0)	$\overline{SS0}$	I/O	MSIOF2 frame synchronization signal channel 0 for transmission Works as SYNC when a common synchronization signal is used for transmission and reception.
MSIOF2_SS1 (SS1)	$\overline{SS1}$	Output	MSIOF2 frame synchronization signal channel 1 for transmission This signal works only master transmission mode.
MSIOF2_SS2 (SS2)	$\overline{SS2}$	Output	MSIOF2 frame synchronization signal channel 2 for transmission This signal works only master transmission mode.
MSIOF2_RSCK		I/O	MSIOF2 serial clock for reception
MSIOF2_RSYNC		I/O	MSIOF2 frame synchronization signal for reception
MSIOF2_TXD (MOSI/MISO)	MOSI/MISO	Output	MSIOF2 transmit data
MSIOF2_RXD (MISO/MOSI)	MISO/MOSI	Input	MSIOF2 receive data

Note: * In SPI mode, the pins are called SCK, $\overline{SS0}$, $\overline{SS1}$, $\overline{SS2}$, MOSI, and MISO.
The GPIO register can be used to switch between MSIOF0_**** and MSIOF0L_**** and switch between MSIOF2_****.

23.3 Register Descriptions

Table 23.2 shows the MSIOF0/MSIOF1/MSIOF2 register configuration and table 23.3 shows the register state in each processing mode.

Table 23.2 Register Configuration

Name	Abbreviation	R/W	Address	Access Size
MSIOF0 transmit mode register 1	SI0TMDR1	R/W	H'FFF1 0000	32
MSIOF0 transmit mode register 2	SI0TMDR2	R/W	HFFF1 0004	32
MSIOF0 transmit mode register 3	SI0TMDR3	R/W	H'FFF1 0008	32
MSIOF0 receive mode register 1	SI0RMDR1	R/W	H'FFF1 0010	32
MSIOF0 receive mode register 2	SI0RMDR2	R/W	H'FFF1 0014	32
MSIOF0 receive mode register 3	SI0RMDR3	R/W	H'FFF1 0018	32
MSIOF0 transmit clock select register	SI0TSCR	R/W	H'FFF1 0020	16
MSIOF0 receive clock select register	SI0RSCR	R/W	H'FFF1 0022	16
MSIOF0 control register	SI0CTR	R/W	H'FFF1 0028	32
MSIOF0 FIFO control register	SI0FCTR	R/W	H'FFF1 0030	32
MSIOF0 status register	SI0STR	R/W	H'FFF1 0040	32
MSIOF0 interrupt enable register	SI0IER	R/W	H'FFF1 0044	32
MSIOF0 transmit control data register 1	SI0TDR1	W	H'FFF1 0048	16/32
MSIOF0 transmit control data register 2	SI0TDR2	W	H'FFF1 004C	16/32
MSIOF0 transmit FIFO data register	SI0TFDR	W	H'FFF1 0050	8/16/32
MSIOF0 receive control data register 1	SI0RDR1	R	H'FFF1 0058	16/32
MSIOF0 receive control data register 2	SI0RDR2	R	H'FFF1 005C	16/32
MSIOF0 receive FIFO data register	SI0RFDR	R	H'FFF1 0060	8/16/32
MSIOF1 transmit mode register 1	SI1TMDR1	R/W	H'E6E1 0000 H'E7E1 0000	32
MSIOF1 transmit mode register 2	SI1TMDR2	R/W	HE6E1 0004 HE7E1 0004	32
MSIOF1 transmit mode register 3	SI1TMDR3	R/W	H'E6E1 0008 H'E7E1 0008	32

Name	Abbreviation	R/W	Address	Access Size
MSIOF1 receive mode register 1	SI1RMDR1	R/W	H'E6E1 0010 H'E7E1 0010	32
MSIOF1 receive mode register 2	SI1RMDR2	R/W	H'E6E1 0014 H'E7E1 0014	32
MSIOF1 receive mode register 3	SI1RMDR3	R/W	H'E6E1 0018 H'E7E1 0018	32
MSIOF1 transmit clock select register	SI1TSCR	R/W	H'E6E1 0020 H'E7E1 0020	16
MSIOF1 receive clock select register	SI1RSCR	R/W	H'E6E1 0022 H'E7E1 0022	16
MSIOF1 control register	SI1CTR	R/W	H'E6E1 0028 H'E7E1 0028	32
MSIOF1 FIFO control register	SI1FCTR	R/W	H'E6E1 0030 H'E7E1 0030	32
MSIOF1 status register	SI1STR	R/W	H'E6E1 0040 H'E7E1 0040	32
MSIOF1 interrupt enable register	SI1IER	R/W	H'E6E1 0044 H'E7E1 0044	32
MSIOF1 transmit control data register 1	SI1TDR1	W	H'E6E1 0048 H'E7E1 0048	16/32
MSIOF1 transmit control data register 2	SI1TDR2	W	H'E6E1 004C H'E7E1 004C	16/32
MSIOF1 transmit FIFO data register	SI1TFDR	W	H'E6E1 0050 H'E7E1 0050	8/16/32
MSIOF1 receive control data register 1	SI1RDR1	R	H'E6E1 0058 H'E7E1 0058	16/32
MSIOF1 receive control data register 2	SI1RDR2	R	H'E6E1 005C H'E7E1 005C	16/32
MSIOF1 receive FIFO data register	SI1RFDR	R	H'E6E1 0060 H'E7E1 0060	8/16/32
MSIOF2 transmit mode register 1	SI2TMDR1	R/W	H'E6E0 0000 H'E7E0 0000	32
MSIOF2 transmit mode register 2	SI2TMDR2	R/W	HE6E0 0004 HE7E0 0004	32

Name	Abbreviation	R/W	Address	Access Size
MSIOF2 transmit mode register 3	SI2TMDR3	R/W	H'E6E0 0008 H'E7E0 0008	32
MSIOF2 receive mode register 1	SI2RMDR1	R/W	H'E6E0 0010 H'E7E0 0010	32
MSIOF2 receive mode register 2	SI2RMDR2	R/W	H'E6E0 0014 H'E7E0 0014	32
MSIOF2 receive mode register 3	SI2RMDR3	R/W	H'E6E0 0018 H'E7E0 0018	32
MSIOF2 transmit clock select register	SI2TSCR	R/W	H'E6E0 0020 H'E7E0 0020	16
MSIOF2 receive clock select register	SI2RSCR	R/W	H'E6E0 0022 H'E7E0 0022	16
MSIOF2 control register	SI2CTR	R/W	H'E6E0 0028 H'E7E0 0028	32
MSIOF2 FIFO control register	SI2FCTR	R/W	H'E6E0 0030 H'E7E0 0030	32
MSIOF2 status register	SI2STR	R/W	H'E6E0 0040 H'E7E0 0040	32
MSIOF2 interrupt enable register	SI2IER	R/W	H'E6E0 0044 H'E7E0 0044	32
MSIOF2 transmit control data register 1	SI2TDR1	R/W	H'E6E0 0048 H'E7E0 0048	16/32
MSIOF2 transmit control data register 2	SI2TDR2	R/W	H'E6E0 004C H'E7E0 004C	16/32
MSIOF2 transmit FIFO data register	SI2TFDR	W	H'E6E0 0050 H'E7E0 0050	8/16/32
MSIOF2 receive control data register 1	SI2RDR1	R	H'E6E0 0058 H'E7E0 0058	16/32

Name	Abbreviation	R/W	Address	Access Size
MSIOF2 receive control data register 2	SI2RDR2	R	H'E6E0 005C H'E7E0 005C	16/32
MSIOF2 receive FIFO data register	SI2RFDR	R	H'E6E0 0060 H'E7E0 0060	8/16/32

Note: The MSIOF0 registers (address: H'FFF1 xxxx) are located in the realtime domain, and the MSIOF1 registers (address: H'E6E1 xxxx/H'E76E xxxx) and the MSIOF2 registers (address: H'E6E0 xxxx/H'E7E0 xxxx) are located in the system domain.

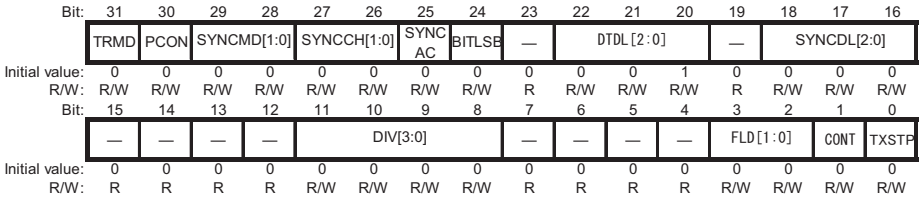
Table 23.3 Register States in Each Operating Mode

Abbreviation	Power-on Reset	Module Standby
SI0TMDR1	Initialized	Retained
SI0TMDR2	Initialized	Retained
SI0TMDR3	Initialized	Retained
SI0RMDR1	Initialized	Retained
SI0RMDR2	Initialized	Retained
SI0RMDR3	Initialized	Retained
SI0TSCR	Initialized	Retained
SI0RSCR	Initialized	Retained
SI0CTR	Initialized	Retained
SI0FCTR	Initialized	Retained
SI0STR	Initialized	Retained
SI0IER	Initialized	Retained
SI0TDR1	Initialized	Initialized
SI0TDR2	Initialized	Initialized
SI0TFDR	Initialized	Initialized
SI0RDR1	Initialized	Initialized
SI0RDR2	Initialized	Initialized
SI0RFDR	Undefined	Initialized
SI1TMDR1	Initialized	Retained
SI1TMDR2	Initialized	Retained
SI1TMDR3	Initialized	Retained
SI1RMDR1	Initialized	Retained
SI1RMDR2	Initialized	Retained
SI1RMDR3	Initialized	Retained
SI1TSCR	Initialized	Retained
SI1RSCR	Initialized	Retained
SI1CTR	Initialized	Retained
SI1FCTR	Initialized	Retained
SI1STR	Initialized	Retained

Abbreviation	Power-on Reset	Module Standby
SI1IER	Initialized	Retained
SI1TDR1	Initialized	Initialized
SI1TDR2	Initialized	Initialized
SI1TFDR	Initialized	Initialized
SI1RDR1	Initialized	Initialized
SI1RDR2	Initialized	Initialized
SI1RFDR	Undefined	Initialized
SI2TMDR1	Initialized	Retained
SI2TMDR2	Initialized	Retained
SI2TMDR3	Initialized	Retained
SI2RMDR1	Initialized	Retained
SI2RMDR2	Initialized	Retained
SI2RMDR3	Initialized	Retained
SI2TSCR	Initialized	Retained
SI2RSCR	Initialized	Retained
SI2CTR	Initialized	Retained
SI2FCTR	Initialized	Retained
SI2STR	Initialized	Retained
SI2IER	Initialized	Retained
SI2TDR1	Initialized	Initialized
SI2TDR2	Initialized	Initialized
SI2TFDR	Initialized	Initialized
SI2RDR1	Initialized	Initialized
SI2RDR2	Initialized	Initialized
SI2RFDR	Undefined	Initialized

23.3.1 MSIOF Transmit Mode Register 1 (SITMDR1)

SITMDR1 is a 32-bit readable/writable register that specifies the MSIOF transmit mode.



Bit	Bit Name	Initial Value	R/W	Descriptions
31	TRMD	1	R/W	Transfer Mode Selects the transfer mode. 0: Slave mode 1: Master mode
30	PCON	0	R/W	Transfer Signal Connection When the TXRST bit is valid when PCON = 1, the RXRST bit is also valid at the same time. When PCON = 1, the receiver should be set to slave mode. 0: MSIOF_TSCK and MSIOF_TSYNC are used only for transmission. 1: MSIOF_TSCK and MSIOF_TSYNC are used as common signals for transmission and reception (MSIOF_SCK and MSIOF_SYNC).
29, 28	SYNCMD [1:0]	00	R/W	SYNC Mode These bits specify the mode for the MSIOF_TSYNC signal. 00: Frame start synchronization pulse 01: 1-bit synchronization pulse for last data in slot 10: Level mode/SPI 11: L/R mode

Bit	Bit Name	Initial Value	R/W	Descriptions
27, 26	SYNCCH [1:0]	00	R/W	Synchronization Signal Channel Select These bits are valid only in master mode. 00: The frame synchronization signal is output from MSIOF_TSYNC. 01: The frame synchronization signal is output from MSIOF_SS1. 10: The frame synchronization signal is output from MSIOF_SS2. 11: Setting prohibited
25	SYNCAC	0	R/W	MSIOF_TSYNC Polarity 0: Active-high signal in synchronization pulse or level mode, or driven high then low in L/R mode 1: Active-low signal in synchronization pulse or level mode, or driven low then high in L/R mode
24	BITLSB	0	R/W	MSB/LSB First 0: MSB first 1: LSB first
23	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
22 to 20	DTDL[2:0]	001	R/W	Data Pin Bit Delay for MSIOF_TSYNC Pin B'1xx is valid only in SPI mode. In SPI mode, these bits should be specified so that the sum of the delays specified through DTDL and SYNCDL becomes an integer value. 000: No bit delay 001: 1-clock-cycle delay 010: 2-clock-cycle delay 101: 0.5-clock-cycle delay 110: 1.5-clock-cycle delay Other than above: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Descriptions
19	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
18 to 16	SYNCDL [2:0]	000	R/W	Frame Synchronization Signal Timing Delay These bits are invalid when SYNCMD[1:0] = B'01. B'1xx is valid only in SPI mode. In SPI mode, these bits should be specified so that the sum of the delays specified through DTDL and SYNCDL becomes an integer value. When L/R mode , these bits should always be set to 000. 000: No bit delay 001: 1-clock-cycle delay 010: 2-clock-cycle delay 011: 3-clock-cycle delay 101: 0.5-clock-cycle delay 110: 1.5-clock-cycle delay Other than above: Setting prohibited
15 to 12	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
11 to 8	DIV[3:0]	0000	R/W	Word Division One 32-bit data stored in the transmit FIFO can be transmitted as two separate 16-bit words through two groups. The word count in each group must be set to 1. In this case, data of groups other than word division target groups must be handled as control data. This setting is valid only in LR mode. 0000: Not divided 0001: Upper word in group 1 and lower word in group 2 0100: Upper word in group 2 and lower word in group 1 Other than above: Setting prohibited
7 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3, 2	FLD[1:0]	00	R/W	Frame Synchronization Signal Interval Specify the minimum idle time between frames in the number of serial clock cycles. This setting is valid only in master mode. When Level mode, set the FLD bits in SITMDR1 for at least 4 cycles of SUBϕ. When L/R mode , these bits should always be set to 00. 00: 0-clock-cycle delay 01: 1-clock-cycle delay 10: 2-clock-cycle delay 11: 3-clock-cycle delay

1	CONT	0	R/W	Continuous Frame Transmission Specifies continuous transmission of multiple frames of data within one frame. This setting is valid when SYNCMD[1:0] = B'00 or B'10 When the TFSE bit in SICTR is set to 0 in master mode, transmission is stopped after one-frame data is transmitted. 0: Does not perform continuous transmission. 1: Performs continuous transmission.
0	TXSTP	0	R/W	Transmission Stop Specifies the processing performed when the remaining number of transmit FIFO stages becomes smaller than the total number of words in the transmit frame. This setting is valid only in master mode. When transmission is continued, the value specified with TXDIZ is output as transmit data. If, with TXSTP = 1, the remaining number of transmit FIFO stages becomes smaller than the total number of words in the transmit frame, transmission is stopped temporarily. After this, however, transmission is automatically restarted if writing into the transmit FIFO causes the remaining number to become larger than the total number of words in the transmit frame. 0: Continues transmission when the transmit FIFO is empty. (The frame synchronization signal is output.) 1: Temporarily stops transmission when the remaining number of transmit FIFO stages becomes smaller than the total number of words in the transmit frame. (The frame synchronization signal is not output.)

23.3.2 MSIOF Transmit Mode Register 2 (SITMDR2)

SITMDR2 is a 32-bit readable/writable register that specifies the MSIOF transmit mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GRP[1:0]		—	BITLEN1[4:0]					WDLEN1[7:0]							
Initial value:	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GRPDL1[1:0]		GRPDL3[1:0]		CRDE4	CRDE3	CRDE2	CRDE1	CRDNUM4	CRDNUM3	CRDNUM2	CRDNUM1	GRPMASK4	GRPMASK3	GRPMASK2	GRPMASK1
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31, 30	GRP[1:0]	00	R/W	Group Count The number of groups is set to the value specified in these bits + 1. When three or more groups are specified, the data size (BITLEN) is set to 16 bits or less.
29	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
28 to 24	BITLEN1[4:0] (BITLEN3)	01111	R/W	Data Size (8 to 32 bits) The word size (bits) of groups 1 and 3 is set to the value specified in these bits + 1. (BITLEN1 = BITLEN3) Eight bits or a larger size should be specified. When three or four groups are used, the word size is set to 16 bits or less (the highest bit is ignored).
23 to 16	WDLEN1[7:0] (WDLEN1[3:0], WDLEN3[3:0])	H'00	R/W	Word Count (1 to 256 words) The word counts of groups 1 and 3 are set to WDLEN1 + 1 and WDLEN3 + 1 respectively. When one or two groups are used, the 8-bit value is set to WDLEN1. When three or four groups are used, the upper 4-bit value is set to WDLEN1, and the lower 4-bit value is set to WDLEN3.

Bit	Bit Name	Initial Value	R/W	Descriptions
15, 14	GRPDL1[1:0]	00	R/W	Group 1 Data Transmission Delay Specify the number of blank bits to be inserted before transmission of group 1. The value specified with TXDIZ in SICTR is output during transmission. 00: 0-clock-cycle delay 01: 1-clock-cycle delay 10: 2-clock-cycle delay 11: 3-clock-cycle delay
13, 12	GRPDL3[1:0]	00	R/W	Group 3 Data Transmission Delay Specify the number of blank bits to be inserted before transmission of group 3. The value specified with TXDIZ in SICTR is output during transmission. 00: 0-clock-cycle delay 01: 1-clock-cycle delay 10: 2-clock-cycle delay 11: 3-clock-cycle delay
11	CRDE4	0	R/W	Control Data Enable
10	CRDE3	0	R/W	“x” in CRDEx represents a group. Each of these bits specifies whether the group transmits FIFO data or control data. 0: The specified group transmits FIFO data. 1: The specified group transmits control data.
9	CRDE2	0	R/W	
8	CRDE1	0	R/W	
7	CRDNUM4	0	R/W	Control Data Transmit Count
6	CRDNUM3	0	R/W	“x” in CRDNUMx represents a group. Each of these bits specifies the transmission count of control data when multiple words are set for a control data group. Each bit is valid only when the corresponding CRDEx bit is 1. When CRDNUMx = 1, control data is transmitted only for the first word, and the value specified with TXDIZ is output for remaining words. 0: Transmits control data continuously. 1: Transmits control data only once.
5	CRDNUM2	0	R/W	
4	CRDNUM1	0	R/W	

Bit	Bit Name	Initial Value	R/W	Descriptions
3	GRPMASK4	0	R/W	Group Output Mask
2	GRPMASK3	0	R/W	“x” in GRPMASKx represents a group. When GRPMASKx = 1, the group outputs the value specified with TXDIZ.
1	GRPMASK2	0	R/W	
0	GRPMASK1	0	R/W	

23.3.3 MSIOF Transmit Mode Register 3 (SITMDR3)

SITMDR3 is a 32-bit readable/writable register that specifies the MSIOF transmit mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	BITLEN2[4:0]					WDLEN2[7:0]							
Initial value:	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GRPDL2[1:0]		GRPDL4[1:0]		—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 24	BITLEN2[4:0] (BITLEN4)	01111	R/W	Word Size (8 to 32 bits) The word size is set to the value specified in these bits + 1. Eight bits or a larger size should be specified. When three or four groups are used, the word size is set to 16 bits or less (the highest bit is ignored).
23 to 16	WDLEN2[7:0] (WDLEN2[3:0], WDLEN4[3:0])	H'00	R/W	Word Count (1 to 256 words) The word counts of groups 2 and 4 are set to WDLEN2 + 1 and WDLEN4 + 1 respectively. When one or two groups are used, the 8-bit value is set to WDLEN2. When three or four groups are used, the upper 4-bit value is set to WDLEN2, and the lower 4-bit value is set to WDLEN4.

Bit	Bit Name	Initial Value	R/W	Descriptions
15, 14	GRPDL2[1:0]	00	R/W	Group 2 Data Transmission Delay These bits specify the number of blank bits to be inserted before transmission of group 2. The value specified with TXDIZ in SICTR is output during transmission. 00: 0-clock-cycle delay 01: 1-clock-cycle delay 10: 2-clock-cycle delay 11: 3-clock-cycle delay
13, 12	GRPDL4[1:0]	00	R/W	Group 4 Data Transmission Delay These bits specify the number of blank bits to be inserted before transmission of group 4. The value specified with TXDIZ in SICTR is output during transmission. 00: 0-clock-cycle delay 01: 1-clock-cycle delay 10: 2-clock-cycle delay 11: 3-clock-cycle delay
11 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

23.3.4 MSIOF Receive Mode Register 1 (SIRMDR1)

SIRMDR1 is a 32-bit readable/writable register that specifies the MSIOF receive mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TRMD	PCON	SYNCMD[1:0]		SYNCCH[1:0]		SYNC AC	BITLSB	—	DTDL[2:0]			—	SYNCDL[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	MRG[3:0]				—	—	—	—	FLD[1:0]		CONT	RXSTP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31	TRMD	1	R/W	Transfer Mode Selects the transfer mode. This bit should be set to 0 (slave mode) when setting the PCON bit in SITMDR1 to 1. 0: Slave mode 1: Master mode
30	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
29, 28	SYNCMD [1:0]	00	R/W	SYNC Mode These bits specify the mode for the MSIOF_RSYNC signal. 00: Frame start synchronization pulse 01: 1-bit synchronization pulse for last data in slot 10: Level mode/SPI 11: L/R mode
27, 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25	SYNCAC	0	R/W	MSIOF_RSYNC Polarity 0: Active-high signal in synchronization pulse or level mode, or driven high then low in L/R mode 1: Active-low signal in synchronization pulse or level mode, or driven low then high in L/R mode

Bit	Bit Name	Initial Value	R/W	Descriptions
24	BITLSB	0	R/W	MSB/LSB First 0: MSB first 1: LSB first
23	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
22 to 20	DTDL[2:0]	001	R/W	Data Pin Bit Delay for MSIOF_RSYNC Pin B'1xx is valid only in SPI mode. In SPI mode, these bits should be specified so that the sum of the delays specified through DTDL and SYNCDL becomes an integer value. 000: No bit delay 001: 1-clock-cycle delay 010: 2-clock-cycle delay 101: 0.5-clock-cycle delay 110: 1.5-clock-cycle delay Other than above: Setting prohibited
19	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
18 to 16	SYNCDL [2:0]	000	R/W	MSIOF_RSYNC Timing Delay The synchronization signal is extended for the clock cycles specified in these bits. These bits are invalid when SYNCMD[1:0] = B'01. B'1xx is valid only in SPI mode. In SPI mode, these bits should be specified so that the sum of the delays specified through DTDL and SYNCDL becomes an integer value. When L/R mode , these bits should always be set to 000. 000: No bit delay 001: 1-clock-cycle delay 010: 2-clock-cycle delay 011: 3-clock-cycle delay 101: 0.5-clock-cycle delay 110: 1.5-clock-cycle delay Other than above: Setting prohibited
15 to 12	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
11 to 8	MRG[3:0]	0000	R/W	Word Merge The data received as 16-bit words of two groups can be merged into one 32-bit word and the 32-bit word is stored in the receive FIFO. The word count of the two groups to be merged must be set to 1. In this case, data of groups other than word merging target groups must be handled as control data. This setting is valid only in LR mode. 0000: Not merged 0001: Upper word in group 1 and lower word in group 2 0100: Upper word in group 2 and lower word in group 1 Other than above: Setting prohibited
7 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3, 2	FLD[1:0]	00	R/W	Frame Synchronization Signal Interval These bits specify the minimum idle time between frames in the number of serial clock cycles. This setting is valid only in master mode. When Level mode, set the FLD bits in SIRMDR1 for at least 4 cycles of SUBϕ. When L/R mode , these bits should always be set to 00. 00: 0-clock-cycle delay 01: 1-clock-cycle delay 10: 2-clock-cycle delay 11: 3-clock-cycle delay

Bit	Bit Name	Initial Value	R/W	Descriptions
1	CONT	0	R/W	Continuous Frame Reception Specifies continuous reception of multiple frames of data within one frame. This setting is valid when SYNCMD[1:0] =B'00 or B'10 When the RFSE bit in SICTR is set to 0 in master mode, reception is terminated after one-frame data is received. 0: Does not perform continuous reception. 1: Performs continuous reception.
0	RXSTP	0	R/W	Reception Stop with Receive FIFO Full Specifies the processing when the receive FIFO becomes full. This setting is valid only in master mode. 0: Continues reception when the receive FIFO is full. (The receive frame synchronization signal is output.) 1: Terminates reception when the receive FIFO is full. (The receive frame synchronization signal is not output.)

23.3.5 MSIOF Receive Mode Register 2 (SIRMDR2)

SIRMDR2 is a 32-bit readable/writable register that specifies the MSIOF receive mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GRP[1:0]		—	BITLEN1[4:0]					WDLEN1[7:0]							
Initial value:	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GRPDL1[1:0]		GRPDL3[1:0]		CRDE4	CRDE3	CRDE2	CRDE1	CRDNUM4	CRDNUM3	CRDNUM2	CRDNUM1	GRPMASK4	GRPMASK3	GRPMASK2	GRPMASK1
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31, 30	GRP[1:0]	00	R/W	Group Count The number of groups is set to the value specified in these bits + 1. When three or more groups are specified, the word size (BITLEN) is set to 16 bits or less. When using transfer signal connection (PCON = 1), set the same value as the value specified by the GRP bits in SITMDR2.
29	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
28 to 24	BITLEN1[4:0] (BITLEN3)	01111	R/W	Word Size (8 to 32 bits) The word size (bits) of groups 1 and 3 is set to the value specified in these bits + 1. (BITLEN1 = BITLEN3) Eight bits or a larger size should be specified. When three or four groups are used, the word size is set to 16 bits or less (the highest bit is ignored). When using transfer signal connection (PCON = 1), set the same value as the value specified by the BITLEN1 bits in SITMDR2.

Bit	Bit Name	Initial Value	R/W	Descriptions
23 to 16	WDLEN1[7:0] (WDLEN1[3:0] WDLEN3[3:0])	H'00	R/W	Word Count (1 to 256 words) The word counts of groups 1 and 3 are set to WDLEN1 + 1 and WDLEN3 + 1 respectively. When one or two groups are used, the 8-bit value is set to WDLEN1. When three or four groups are used, the upper 4-bit value is set to WDLEN1, and the lower 4-bit value is set to WDLEN3. When using transfer signal connection (PCON = 1), set the same value as the value specified by the WDLEN1 bits in SITMDR2.
15, 14	GRPDL1[1:0]	00	R/W	Group 1 Data Reception Delay These bits specify the delay in data reception of group 1. 00: 0-clock-cycle delay 01: 1-clock-cycle delay 10: 2-clock-cycle delay 11: 3-clock-cycle delay When using transfer signal connection (PCON = 1), set the same value as the value specified by the GRPDL1 bits in SITMDR2.
13, 12	GRPDL3[1:0]	00	R/W	Group 3 Data Reception Delay These bits specify the delay in data reception of group 3. 00: 0-clock-cycle delay 01: 1-clock-cycle delay 10: 2-clock-cycle delay 11: 3-clock-cycle delay When using transfer signal connection (PCON = 1), set the same value as the value specified by the GRPDL3 bits in SITMDR2.

Bit	Bit Name	Initial Value	R/W	Descriptions
11	CRDE4	0	R/W	Control Data Enable
10	CRDE3	0	R/W	"x" in CRDEx represents a group. Each of these bits specifies whether the group receives FIFO data or control data. 0: The specified group receives FIFO data. 1: The specified group receives control data.
9	CRDE2	0	R/W	
8	CRDE1	0	R/W	
7	CRDNUM4	0	R/W	Control Data Reception Count
6	CRDNUM3	0	R/W	"x" in CRDNUMx represents a group. Each of these bits specifies the reception count of control data when multiple words are set for a control data group. Each bit is valid only when the corresponding CRDEx bit is 1. When CRDNUMx = 1, only the first word is received as control data, and the other words are discarded as invalid data. 0: Receives control data continuously. 1: Receives control data only once in a frame.
5	CRDNUM2	0	R/W	
4	CRDNUM1	0	R/W	
3	GRPMASK4	0	R/W	Group Input Mask
2	GRPMASK3	0	R/W	"x" in GRPMASKx represents a group. When GRPMASKx = 1, inputs of the group are masked and discarded as invalid data.
1	GRPMASK2	0	R/W	
0	GRPMASK1	0	R/W	

23.3.6 MSIOF Receive Mode Register 3 (SIRMDR3)

SIRMDR3 is a 32-bit readable/writable register that specifies the MSIOF receive mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	BITLEN2[4:0]					WDLEN2[7:0]							
Initial value:	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GRPDL2[1:0]		GRPDL4[1:0]		—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 24	BITLEN2[4:0] (BITLEN4)	01111	R/W	Word Size (8 to 32 bits) The word size is set to the value specified in these bits + 1. Eight bits or a larger size should be specified. When three or four groups are used, the word size is set to 16 bits or less (the highest bit is ignored). When using transfer signal connection (PCON = 1), set the same value as the value specified by the BITLEN2 bits in SITMDR3.
23 to 16	WDLEN2[7:0] (WDLEN4)	H'00	R/W	Word Count (1 to 256 words) The word counts of groups 2 and 4 are set to WDLEN2 + 1 and WDLEN4 + 1 respectively. When one or two groups are used, the 8-bit value is set to WDLEN2. When three or four groups are used, the upper 4-bit value is set to WDLEN2, and the lower 4-bit value is set to WDLEN4. When using transfer signal connection (PCON = 1), set the same value as the value specified by the WDLEN2 bits in SITMDR3.

Bit	Bit Name	Initial Value	R/W	Descriptions
15, 14	GRPDL2[1:0]	00	R/W	Group 2 Data Reception Delay These bits specify the delay in data reception of group 2. 00: 0-clock-cycle delay 01: 1-clock-cycle delay 10: 2-clock-cycle delay 11: 3-clock-cycle delay When using transfer signal connection (PCON = 1), set the same value as the value specified by the GRPDL2 bits in SITMDR3.
13, 12	GRPDL4[1:0]	00	R/W	Group 4 Data Reception Delay These bits specify the delay in data reception of group 4 00: 0-clock-cycle delay 01: 1-clock-cycle delay 10: 2-clock-cycle delay 11: 3-clock-cycle delay When using transfer signal connection (PCON = 1), set the same value as the value specified by the GRPDL4 bits in SITMDR3.
11 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

23.3.7 MSIOF Control Register (SICTR)

SICTR is a 32-bit readable/writable register that specifies the MSIOF operating state.

The values written to the TXE, RXE, TFSE, RFSE, TSCKE, and RSCKE bits become valid (can be read from the bits) several cycles after writing. These bits should not be modified together; modify one bit at a time, check that the new value can be read from the bit, and then modify another bit.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TSCKIZ[1:0]		RSCKIZ[1:0]		TEDG	REDG	—	—	TXDIZ[1:0]		—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TSCKE	TFSE	RSCKE	RFSE	—	—	TXE	RXE	—	—	—	—	—	—	TXRST	RXRST
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31, 30	TSCKIZ[1:0]	00	R/W	Transmit Clock Input/Output Polarity Select in SPI Mode When Transmission is Disabled When SPI mode is not used, these bits must always be set to 00. These bits must always be set 10 or 11 when SPI mode. [Master mode] 00: Outputs MSIOF_TSCK when transmission is disabled. 01: Setting prohibited 10: Outputs 0. 11: Outputs 1. [Slave mode] 00: Inputs MSIOF_TSCK when transmission is disabled. 01: Setting prohibited 10: Inputs 0 through MSIOF_TSCK when transmission is disabled. 11: Inputs 1 through MSIOF_TSCK when transmission is disabled.

Bit	Bit Name	Initial Value	R/W	Descriptions
29, 28	RSCKIZ[1:0]	00	R/W	Receive Clock Input/Output Polarity Select in SPI Mode In SPI mode, set these bits to the TSCKIZ value. [Master mode] 00: Outputs MSIOF_RSCK when transmission is disabled. 01: Setting prohibited 10: Outputs 0. 11: Outputs 1. [Slave mode] 00: Inputs MSIOF_RSCK when transmission is disabled. 01: Setting prohibited 10: Inputs 0 through MSIOF_RSCK when transmission is disabled. 11: Inputs 1 through MSIOF_RSCK when transmission is disabled.
27	TEDG	0	R/W	Transmit Timing 0: Outputs transmit data at the rising edge of the clock. 1: Outputs transmit data at the falling edge of the clock.
26	REDG	0	R/W	Receive Timing 0: Samples receive data at the falling edge of the clock. 1: Samples receive data at the rising edge of the clock.
25, 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23, 22	TXDIZ[1:0]	00	R/W	Pin Output When Transmission is Disabled These bits specify the MSIOF_TXD pin output state when transmission is disabled. 00: Outputs 0. 01: Outputs 1. 10: Output is in high-impedance state. 11: Setting prohibited
21 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
15	TSCKE	0	R/W	Transmit Serial Clock Output Enable This bit is valid in master mode. When this bit is set to 1, the MSIOF initializes the baud rate generator and initiates the operation. At the same time, the MSIOF outputs the clock generated by the baud rate generator to the MSIOF_TSCK pin. After the clock is output, 1 can be read. When transmitting data, set this bit to 1 before setting the TFSE and TXE bits. After data transmission, clear the TFSE and TXE bits and then clear this bit to 0. [Write data] 0: Disables the MSIOF_TSCK output. (Outputs the value specified with TSCKIZ.) 1: Enables the MSIOF_TSCK output. [Read data] 0: Does not output MSIOF_TSCK. (Outputs the value specified with TSCKIZ.) 1: Outputs MSIOF_TSCK.
14	TFSE	0	R/W	Transmit Frame Synchronization Signal Output Enable This bit is valid in master mode. When this bit is set to 1, the MSIOF initializes the frame counter and initiates the operation. After the transmit frame synchronization signal is output, 1 can be read. When 0 is written to this bit, 0 is set after transmission of the frame. [Write data] 0: Disables the MSIOF_TSYNC output. (Outputs the value specified with SYNCAC.) 1: Enables the MSIOF_TSYNC output. [Read data] 0: Does not output MSIOF_TSYNC. (Outputs the value specified with SYNCAC.) 1: Outputs MSIOF_TSYNC.

Bit	Bit Name	Initial Value	R/W	Descriptions
13	RSCKE	0	R/W	Receive Serial Clock Output Enable This bit is valid in master mode. When this bit is set to 1, the MSIOF initializes the baud rate generator and initiates the operation. At the same time, the MSIOF outputs the clock generated by the baud rate generator to the MSIOF_RSCK pin. After the clock is output, 1 can be read. When receiving data, set this bit to 1 before setting the RFSE and RXE bits. After data reception, clear the RFSE and RXE bits and then clear this bit to 0. [Write data] 0: Disables the MSIOF_RSCK output. (Outputs the value specified with RSCKIZ.) 1: Enables the MSIOF_RSCK output. [Read data] 0: Does not output MSIOF_RSCK. (Outputs the value specified with RSCKIZ.) 1: Outputs MSIOF_RSCK.
12	RFSE	0	R/W	Receive Frame Synchronization Signal Output Enable This bit is valid in master mode. When this bit is set to 1, the MSIOF initializes the frame counter and initiates the operation. After the receive frame synchronization signal is output, 1 can be read. When 0 is written to this bit, 0 is set after reception of the frame. [Write data] 0: Disables the MSIOF_RSYNC output. (Outputs the value specified with SYNCAC.) 1: Enables the MSIOF_RSYNC output. [Read data] 0: Does not output MSIOF_RSYNC. (Outputs the value specified with SYNCAC.) 1: Outputs MSIOF_RSYNC.
11, 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
9	TXE	0	R/W	Transmit Enable When this bit is set to 1, the MSIOF starts data transmission from the beginning of the next frame (at the rising edge of the frame synchronization signal). After the valid data is output, 1 can be read. When value 1 set to this bit becomes valid, the MSIOF issues a transmit data transfer request according to the setting of the TFWM bits in SIFCTR. When transmit data is stored in the transmit FIFO, transmission of data from the MSIOF_TXD pin begins. When 0 is written to this bit, 0 is set after transmission of the frame. This bit is initialized upon a transmit reset. [Write data] 0: Disables the MSIOF_TXD output. (Outputs the value specified with TXDIZ.) 1: Enables the MSIOF_TXD output. [Read data] 0: Does not output MSIOF_TXD. (Outputs the value specified with TXDIZ.) 1: Outputs MSIOF_TXD.
8	RXE	0	R/W	Receive Enable When this bit is set to 1, the MSIOF starts data reception from the beginning of the next frame (at the rising edge of the frame synchronization signal). When value 1 set to this bit becomes valid, the MSIOF starts receiving data through the MSIOF_RXD pin. When receive data is stored in the receive FIFO, the MSIOF issues a receive data transfer request according to the setting of the RFWM bits in SIFCTR. This bit is initialized upon a receive reset. [Write data] 0: Disables data reception through MSIOF_RXD. 1: Enables data reception through MSIOF_RXD. [Read data] 0: Data is not received through MSIOF_RXD. 1: Data can be received through MSIOF_RXD.

Bit	Bit Name	Initial Value	R/W	Descriptions
7 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	TXRST	0	R/W	Transmit Reset When value 1 set to this bit becomes valid, the MSIOF immediately sets transmit data through the MSIOF_TXD pin to 0, and initializes the transmit data registers and transmit-related status. When value 1 set to this bit becomes valid when PCON = 1, the RXRST bit is also becomes valid. The following registers and bits are initialized. SITDR1 and SITDR2 SITFDR Transmit FIFO write pointer TCRDY, TFEMP, and TDREQ bits in SISTR TXE bit This bit is read as 1 until the reset operation is completed for about SUBϕ20 cycles. No data should be written to SICTR or the transmit FIFO during this time period. [Write data] 0: Does not reset transmit operation. 1: Resets transmit operation. [Read data] 0: Transmit operation reset is completed. 1: Transmit operation is being reset.

Bit	Bit Name	Initial Value	R/W	Descriptions
0	RXRST	0	R/W	Receive Reset When value 1 set to this bit becomes valid, the MSIOF immediately disables reception through the MSIOF_RXD pin, and initializes the receive data registers and receive-related status. The following registers and bits are initialized. SIRDR1 and SIRDR2 SIRFDR Receive FIFO read pointer RCRDY, RFFUL, and RDREQ bits in SISTR RXE bit This bit is read as 1 until the reset operation is completed for about SUBϕ20 cycles. No data should be written to SICTR or read the receive FIFO during this time period. [Write data] 0: Does not reset receive operation. 1: Resets receive operation. [Read data] 0: Receive operation reset is completed. 1: Receive operation is being reset.

23.3.8 MSIOF Transmit Clock Select Register (SITSCR)

SITSCR is a 16-bit readable/writable register that specifies the conditions for generating the transmit serial clock in master mode. SITSCR can be specified when the TRMD bit in SITMDR1 is set to B'1.

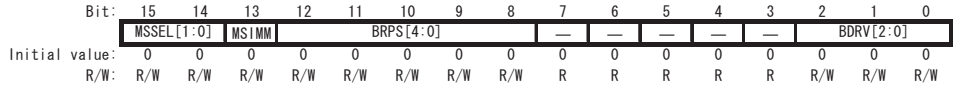
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSSEL[1:0]		MSIMM	BRPS[4:0]					—	—	—	—	—	BDRV[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
15, 14	MSSEL[1:0]	00	R/W	Master Clock Source Select The master clock is the clock input to the baud rate generator. 00: Selects SUBϕ as the master clock. 01: Selects the signal input from the MSIOF_MCK0 pin as the master clock. 10: Selects the signal input from the MSIOF_MCK1 pin as the master clock. 11: Setting prohibited
13	MSIMM	0	R/W	Master Clock Direct Select When setting MSIMM = 1, the master clock source should be set to 24 MHz or lower. Set 0 when MSSEL = 2’b00. 0: Selects the clock output from the baud rate generator as the serial clock. 1: Selects the master clock itself as the serial clock.
12 to 8	BRPS[4:0]	00000	R/W	Prescalar Setting These bits specify the master clock division ratio in the count value of the prescalar in the baud rate generator. The specifiable value is from B'00000 (× 1/1) to B'11111 (× 1/32).
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
2 to 0	BRDV[2:0]	000	R/W	Baud Rate Generator's Division Ratio These bits specify the frequency division ratio for the output stage of the baud rate generator. The final frequency division ratio of the baud rate generator is determined as BRPS × BRDV (1/1024 max.). 000: Prescalar output × 1/2 001: Prescalar output × 1/4 010: Prescalar output × 1/8 011: Prescalar output × 1/16 100: Prescalar output × 1/32 101: Setting prohibited 110: Setting prohibited 111: Prescalar output × 1/1 Note: B'111 is valid only when the BRPS[4:0] bits are set to B'00000 or B'00001.

23.3.9 MSIOF Receive Clock Select Register (SIRSCR)

SIRSCR is a 16-bit readable/writable register that specifies the conditions for generating the receive serial clock in master mode. SIRSCR can be specified when the TRMD bit in SIRMDR1 is set to B'1.



Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSSEL[1:0]		MSIMM	BRPS[4:0]					—	—	—	—	—	BDRV[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
15, 14	MSSEL[1:0]	00	R/W	Master Clock Source Select The master clock is the clock input to the baud rate generator. 00: Selects SUBϕ as the master clock. 01: Selects the signal input from the MSIOF_MCK0 pin as the master clock. 10: Selects the signal input from the MSIOF_MCK1 pin as the master clock. 11: Setting prohibited
13	MSIMM	0	R/W	Master Clock Direct Select When setting MSIMM = 1, the master clock source should be set to 24 MHz or lower. Set 0 when MSSEL = 2'b00. 0: Selects the clock output from the baud rate generator as the serial clock. 1: Selects the master clock itself as the serial clock.
12 to 8	BRPS[4:0]	00000	R/W	Prescalar Setting These bits specify the master clock division ratio in the count value of the prescalar in the baud rate generator. The specifiable value is from B'00000 (× 1/1) to B'11111 (× 1/32).
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
2 to 0	BRDV[2:0]	000	R/W	Baud Rate Generator's Division Ratio These bits specify the frequency division ratio for the output stage of the baud rate generator. The final frequency division ratio of the baud rate generator is determined as BRPS × BRDV (1/1024 max.). 000: Prescalar output × 1/2 001: Prescalar output × 1/4 010: Prescalar output × 1/8 011: Prescalar output × 1/16 100: Prescalar output × 1/32 101: Setting prohibited 110: Setting prohibited 111: Prescalar output × 1/1 Note: B'111 is valid only when the BRPS[4:0] bits are set to B'00000 or B'00001.

23.3.10 MSIOF Transmit Control Data Register 1 (SITDR1)

SITDR1 is a 32-bit write-only register that specifies the transmit control data of the MSIOF.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TCRD1[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TCRD2[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 16	TCRD1[15:0]	H'0000	W	When one or two groups are used: These bits specify the transmit control data for the upper 16 bits of a word in group 1 When three or four groups are used: These bits specify the transmit control data for a word in group 1.
15 to 0	TCRD2[15:0]	H'0000	W	When one or two groups are used: These bits specify the transmit control data for the lower 16 bits of a word in group 1 when the word size is larger than 16 bits. When three or four groups are used: These bits specify the transmit control data for a word in group 3.

23.3.11 MSIOF Transmit Control Data Register 2 (SITDR2)

SITDR2 is a 32-bit write-only register that specifies the transmit control data of the MSIOF.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TCRD3[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TCRD4[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 16	TCRD3[15:0]	H'0000	W	When one or two groups are used: These bits specify the transmit control data for the upper 16 bits of a word in group 2. When three or four groups are used: These bits specify the transmit control data for a word in group 2.
15 to 0	TCRD4[15:0]	H'0000	W	When one or two groups are used: These bits specify the transmit control data for the lower 16 bits of a word in group 2 when the word size is larger than 16 bits. When three or four groups are used: These bits specify the transmit control data for a word in group 4.

23.3.12 MSIOF Transmit FIFO Data Register (SITFDR)

SITFDR is a 32-bit write-only register that specifies the transmit FIFO data of the MSIOF.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SITFD1[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SITFD2[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 16	SITFD1[15:0]	H'0000	W	These bits specify the upper 16 bits of the FIFO data to be output through MSIOF_TXD.
15 to 0	SITFD2[15:0]	H'0000	W	These bits specify the lower 16 bits of the FIFO data to be output through MSIOF_TXD.

23.3.13 MSIOF Receive Control Data Register 1 (SIRDR1)

SIRDR1 is a 32-bit read-only register that stores the receive control data of the MSIOF.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RCRD1[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RCRD2[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 16	RCRD1[15:0]	H'0000	R	When one or two groups are used: Store the receive control data for the upper 16 bits of a word in group 1. When three or four groups are used: Store the receive control data for a word in group 1.
15 to 0	RCRD2[15:0]	H'0000	R	When one or two groups are used: Store the receive control data for the lower 16 bits of a word in group 1 when the word size is larger than 16 bits. When three or four groups are used: Store the receive control data for a word in group 3.

23.3.14 MSIOF Receive Control Data Register 2 (SIRDR2)

SIRDR2 is a 32-bit read-only register that stores the receive control data of the MSIOF.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RCRD3[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RCRD4[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 16	RCRD3[15:0]	H'0000	R	When one or two groups are used: Store the receive control data for the upper 16 bits of a word in group 2. When three or four groups are used: Store the receive control data for a word in group 2.
15 to 0	RCRD4[15:0]	H'0000	R	When one or two groups are used: Store the receive control data for the lower 16 bits of a word in group 2 when the word size is larger than 16 bits. When three or four groups are used: Store the receive control data for a word in group 4.

23.3.15 MSIOF Receive FIFO Data Register (SIRFDR)

SIRFDR is a 32-bit read-only register that stores the receive FIFO data of the MSIOF.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SIRFD1[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SIRFD2[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 16	SIRFD1[15:0]	Undefined	R	Store the upper 16 bits of the FIFO data received through MSIOF_RXD.
15 to 0	SIRFD2[15:0]	Undefined	R	Store the lower 16 bits of the FIFO data received through MSIOF_RXD.

23.3.16 MSIOF Status Register (SISTR)

Each bit in SISTR becomes an MSIOF interrupt source when the corresponding bit in SIIER is set to 1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	TCRDY	TFEMP	TDREQ	—	—	—	—	TEOF	—	TFSERR	TFOVF	TFUDF	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R	R	R	R	R	R/W	R	R/W	R/W	R/W	R	R	R
Bit:																
	—	RCRDY	RFFUL	RDREQ	—	—	—	—	REOF	—	RFSERR	RFUDF	RFOVF	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R	R	R	R	R	R/W	R	R/W	R/W	R/W	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
30	TCRDY	0	R/W	Transmit Control Data Ready If SITDR1 or SITDR2 is written while this bit is cleared to 0, SICTR is overwritten and the previous contents are not output through the MSIOF_TXD pin. If the interrupt request from this bit is enabled, an MSIOF interrupt is issued. When this bit is set to 1, the contain is cleared. Write 0 to this bit is invalid. 0: SITDR1 and SITDR2 are not ready to be written. 1: SITDR1 and SITDR2 are ready to be written.

Bit	Bit Name	Initial Value	R/W	Descriptions
29	TFEMP	0	R/W	Transmit FIFO Empty This bit is valid when the TXE bit in SICTR is 1. When this bit is set to 1, the content is cleared. Writing 0 to this bit is invalid. If the interrupt request from this bit is enabled, an MSIOF interrupt is issued. 0: Transmit FIFO is not empty. 1: Transmit FIFO is empty.
28	TDREQ	0	R	Transmit Data Transfer Request A transmit data transfer request is issued when the empty space in the transmit FIFO exceeds the size specified by the TFWM bits in SIFCTR. When transferring transmit data through the DMAC, this bit is always cleared after one DMAC access. After DMAC access, when the conditions for setting this bit are satisfied, the MSIOF again sets this bit to 1. This bit is valid when the TXE bit in SICTR is 1. This bit indicates a state; if the size of empty space in the transmit FIFO becomes less than the size specified by the TFWM bits in SIFCTR, the MSIOF clears this bit. If the interrupt request from this bit is enabled, an MSIOF interrupt is issued. However, when the TDMAE bit is 1, only a DMAC transfer request is issued. 0: The size of empty space in the transmit FIFO has not exceeded the size specified by the TFWM bits in SIFCTR. 1: The size of empty space in the transmit FIFO has exceeded the size specified by the TFWM bits in SIFCTR.
27 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
23	TEOF	0	R/W	Frame Transmission End The MSIOF issues the frame transmission end flag upon completion of one-frame data transmission. This bit is valid when the TXE bit in SICTR is 1. When this bit is set to 1, the content is cleared. Writing 0 to this bit is invalid. If the interrupt request from this bit is enabled, an MSIOF interrupt is issued. 0: One-frame transmission end is not detected. 1: One-frame transmission end is detected.
22	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
21	TFSERR	0	R/W	Transmit Frame Synchronization Error A transmit frame synchronization error occurs when the next transmit frame synchronization timing arrives before the previous data or control data transmission has been completed. If a transmit frame synchronization error occurs, the MSIOF performs transmission only for the slots that can be transferred. This bit is valid when the TXE bit in SICTR is 1. When 1 is written to this bit, it is cleared. Writing 0 to this bit is invalid. If the interrupt request from this bit is enabled, an MSIOF interrupt is issued. 0: No transmit frame synchronization error has occurred. 1: A transmit frame synchronization error has occurred.

Bit	Bit Name	Initial Value	R/W	Descriptions
20	TFOVF	0	R/W	Transmit FIFO Overflow A transmit FIFO overflow means that there has been an attempt to write to SITFDR when the transmit FIFO is full. If a transmit FIFO overflow occurs, the MSIOF ignores the write operation causing the overflow. This bit is valid when the TXE bit in SICTR is 1. When 1 is written to this bit, it is cleared. Writing 0 to this bit is invalid. If the interrupt request from this bit is enabled, an MSIOF interrupt is issued. 0: No transmit FIFO overflow has occurred. 1: A transmit FIFO overflow has occurred.
19	TFUDF	0	R/W	Transmit FIFO Underflow A transmit FIFO underflow means that loading for transmission has occurred when the transmit FIFO is empty. This bit is valid when the TXE bit in SICTR is 1. When 1 is written to this bit, it is cleared. Writing 0 to this bit is invalid. If the interrupt request from this bit is enabled, an MSIOF interrupt is issued. 0: No transmit FIFO underflow has occurred. 1: A transmit FIFO underflow has occurred.
18 to 15	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
14	RCRDY	0	R/W	Receive Control Data Ready When data different from the previous data is stored during reception of control data, this bit is set to 1 indicating that valid data was written. When the first data that is not 0 is stored, this bit is set to 1. If valid data is written to SIRDR1 or SIRDR2 when this bit is set to 1, SIRDR1 or SIRDR2 is overwritten with the latest data. This bit is valid when the RXE bit in SICTR is 1. If the interrupt request from this bit is enabled, an MSIOF interrupt is issued. When this bit is set to 1, the contain is cleared. Write 0 to this bit is invalid. 0: SIRDR1 and SIRDR2 store no valid data. 1: SIRDR1 and SIRDR2 store valid data.
13	RFFUL	0	R/W	Receive FIFO Full This bit is valid when the RXE bit in SICTR is 1. When this bit is set to 1, the content is cleared. Writing 0 to this bit is invalid. If the interrupt request from this bit is enabled, an MSIOF interrupt is issued. 0: Receive FIFO is not full. 1: Receive FIFO is full.

Bit	Bit Name	Initial Value	R/W	Descriptions
12	RDREQ	0	R	Receive Data Transfer Request A receive data transfer request is issued when the valid data space in the receive FIFO exceeds the size specified by the RFWM bits in SIFCTR. When transferring receive data through the DMAC, this bit is always cleared by one DMAC access. After DMAC access, when the conditions for setting this bit are satisfied, the MSIOF again sets this bit to 1. This bit is valid when the RXE bit in SICTR is 1. This bit indicates a state; if the size of valid data space in the receive FIFO becomes less than the size specified by the RFWM bits in SIFCTR, the MSIOF clears this bit. If the interrupt request from this bit is enabled, an MSIOF interrupt is issued. However, when the RDMAE bit is 1, only a DMAC transfer request is issued. 0: The size of valid data space in the receive FIFO has not exceeded the size specified by the RFWM bits in SIFCTR. 1: The size of valid data space in the receive FIFO has exceeded the size specified by the RFWM bits in SIFCTR.
11 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	REOF	0	R/W	Frame Reception End The MSIOF issues the frame reception end flag upon completion of one-frame data reception. This bit is valid when the RXE bit in SICTR is 1. When this bit is set to 1, the content is cleared. Writing 0 to this bit is invalid. If the interrupt request from this bit is enabled, an MSIOF interrupt is issued. 0: One-frame reception end is not detected. 1: One-frame reception end is detected.

Bit	Bit Name	Initial Value	R/W	Descriptions
6	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
5	RFSERR	0	R/W	Receive Frame Synchronization Error A receive frame synchronization error occurs when the next receive frame synchronization timing arrives before the previous data or control data reception has been completed. If a receive frame synchronization error occurs, the MSIOF performs reception only for the slots that can be transferred. This bit is valid when the RXE bit in SICTR is 1. When 1 is written to this bit, it is cleared. Writing 0 to this bit is invalid. If the interrupt request from this bit is enabled, an MSIOF interrupt is issued. 0: No receive frame synchronization error has occurred 1: A receive frame synchronization error has occurred
4	RFUDF	0	R/W	Receive FIFO Underflow A receive FIFO underflow means that reading of SIRFDR has occurred when the receive FIFO is empty. If a receive FIFO underflow occurs, the value read from SIRFDR is not guaranteed. This bit is valid when the RXE bit in SICTR is 1. When 1 is written to this bit, it is cleared. Writing 0 to this bit is invalid. If the interrupt request from this bit is enabled, an MSIOF interrupt is issued. 0: No receive FIFO underflow has occurred. 1: A receive FIFO underflow has occurred.

Bit	Bit Name	Initial Value	R/W	Descriptions
3	RFOVF	0	R/W	Receive FIFO Overflow A receive FIFO overflow means that writing has been caused by receiving operation when the receive FIFO is full. If a receive FIFO overflow occurs, the receive data causing the overflow is lost. This bit is valid when the RXE bit in SICTR is 1. When 1 is written to this bit, it is cleared. Writing 0 to this bit is invalid. If the interrupt request from this bit is enabled, an MSIOF interrupt is issued. 0: No receive FIFO overflow has occurred. 1: A receive FIFO overflow has occurred.
2 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

23.3.17 MSIOF Interrupt Enable Register (SIIER)

SIIER is a 32-bit readable/writable register that enables the issue of MSIOF interrupts. When each bit in this register is set to 1 and the corresponding bit in SISTR is set to 1, the MSIOF issues an interrupt.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TDMAE	TCRDYE	TFEMPE	TDREQE	—	—	—	—	TEOFE	—	TFSERRE	TFOVFE	TFUDFE	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R	R/W	R/W	R/W	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RDMAE	RCRDYE	RFFULE	RDREQE	—	—	—	—	REOFE	—	RFSERRE	RFUDFE	RFOVFE	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R	R/W	R/W	R/W	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31	TDMAE	0	R/W	Transmit Data DMA Transfer Request Enable Specifies whether to send an interrupt as an interrupt request to the CPU or a transfer request to the DMAC. The TDREQE bit can be set as the request source. 0: Sends an interrupt request to the CPU. 1: Sends a DMA transfer request to the DMAC.
30	TCRDYE	0	R/W	Transmit Control Data Ready Enable 0: Disables interrupts due to transmit control data ready. 1: Enables interrupts due to transmit control data ready.
29	TFEMPE	0	R/W	Transmit FIFO Empty Enable 0: Disables interrupts due to transmit FIFO empty. 1: Enables interrupts due to transmit FIFO empty.
28	TDREQE	0	R/W	Transmit Data Transfer Request Enable 0: Disables interrupts due to transmit data transfer requests. 1: Enables interrupts due to transmit data transfer requests.

Bit	Bit Name	Initial Value	R/W	Descriptions
27 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23	TEOFE	0	R/W	Frame Transmission End Enable 0: Disables a frame transmission end interrupt. 1: Enables a frame transmission end interrupt.
22	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
21	TFSERRE	0	R/W	Transmit Frame Synchronization Error Enable 0: Disables interrupts due to transmit frame synchronization errors. 1: Enables interrupts due to transmit frame synchronization errors.
20	TFOVFE	0	R/W	Transmit FIFO Overflow Enable 0: Disables interrupts due to transmit FIFO overflow. 1: Enables interrupts due to transmit FIFO overflow.
19	TFUDFE	0	R/W	Transmit FIFO Underflow Enable 0: Disables interrupts due to transmit FIFO underflow. 1: Enables interrupts due to transmit FIFO underflow.
18 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	RDMAE	0	R/W	Receive Data DMA Transfer Request Enable Specifies whether to send an interrupt as an interrupt request to the CPU or a transfer request to the DMAC. The RDREQE bit can be set as the request source. 0: Sends an interrupt request to the CPU. 1: Sends a DMA transfer request to the DMAC.

Bit	Bit Name	Initial Value	R/W	Descriptions
14	RCRDYE	0	R/W	Receive Control Data Ready Enable 0: Disables interrupts due to receive control data ready. 1: Enables interrupts due to receive control data ready.
13	RFFULE	0	R/W	Receive FIFO Full Enable 0: Disables interrupts due to receive FIFO full. 1: Enables interrupts due to receive FIFO full.
12	RDREQE	0	R/W	Receive Data Transfer Request Enable 0: Disables interrupts due to receive data transfer requests. 1: Enables interrupts due to receive data transfer requests.
11 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	REOFE	0	R/W	Frame Reception End Enable 0: Disables a frame reception end interrupt. 1: Enables a frame reception end interrupt.
6	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
5	RFSERRE	0	R/W	Receive Frame Synchronization Error Enable 0: Disables interrupts due to receive frame synchronization errors. 1: Enables interrupts due to receive frame synchronization errors.
4	RFUDFE	0	R/W	Receive FIFO Underflow Enable 0: Disables interrupts due to receive FIFO underflow. 1: Enables interrupts due to receive FIFO underflow.

Bit	Bit Name	Initial Value	R/W	Descriptions
3	RFOVFE	0	R/W	Receive FIFO Overflow Enable 0: Disables interrupts due to receive FIFO overflow. 1: Enables interrupts due to receive FIFO overflow.
2 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

23.3.18 MSIOF FIFO Control Register (SIFCTR)

SIFCTR is a 32-bit readable/writable register that indicates the area available for the transmit/receive FIFO transfer.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TFWM[2:0]			-	-	TFUA[6:0]							-	-	-	-
Initial value	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RFWM[2:0]			RFUA[8:0]									-	-	-	-
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 29	TFWM[2:0]	000	R/W	Transmit FIFO Watermark A transfer request of the transmit FIFO is issued by the TDREQE bit in SIIER. The transmit FIFO always operates as a 64-stage FIFO regardless of these bit settings. 000: Issues a transfer request when 64 stages of the transmit FIFO are empty. 001: Issues a transfer request when 32 or more stages of the transmit FIFO are empty. 010: Issues a transfer request when 24 or more stages of the transmit FIFO are empty. 011: Issues a transfer request when 16 or more stages of the transmit FIFO are empty. 100: Issues a transfer request when 12 or more stages of the transmit FIFO are empty. 101: Issues a transfer request when 8 or more stages of the transmit FIFO are empty. 110: Issues a transfer request when 4 or more stages of the transmit FIFO are empty. 111: Issues a transfer request when 1 or more stages of transmit FIFO are empty.

Bit	Bit Name	Initial Value	R/W	Descriptions
28, 27	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
26 to 20	TFUA[6:0]	H'40	R	Transmit FIFO Usable Area Indicate the number of words that can be transferred by the CPU or DMAC as B'0000000 (full) to B'1000000 (empty).
19 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 13	RFWM[2:0]	000	R/W	Receive FIFO Watermark A transfer request of the receive FIFO is issued by the RDREQE bit in SIIER. The receive FIFO always operates as a 256-stage FIFO regardless of these bit settings. 000: Issues a transfer request when 1 stage or more of the receive FIFO are valid. 001: Issues a transfer request when 4 or more stages of the receive FIFO are valid. 010: Issues a transfer request when 8 or more stages of the receive FIFO are valid. 011: Issues a transfer request when 16 or more stages of the receive FIFO are valid. 100: Issues a transfer request when 32 or more stages of the receive FIFO are valid. 101: Issues a transfer request when 64 or more stages of the receive FIFO are valid. 110: Issues a transfer request when 128 or more stages of the receive FIFO are valid. 111: Issues a transfer request when 256 stages of the receive FIFO are valid.
12, 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
10 to 4	RFUA[8:0]	H'00	R	Receive FIFO Usable Area Indicate the number of words that can be transferred by the CPU or DMAC as B'000000000 (empty) to B'100000000 (full).
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

23.4 Operation

23.4.1 Operating Mode

(1) Independent Transmit/Receive Mode

Dedicated clock and frame synchronization signals can be specified each for transmission and reception.

Master mode: MSIOF_TSCK, MSIOF_TSYNC, MSIOF_RSCK, and MSIOF_RSYNC are output.

Slave mode: MSIOF_TSCK, MSIOF_TSYNC, MSIOF_RSCK, and MSIOF_RSYNC are input.

(2) Common Transmit/Receive Mode

Common clock and frame synchronization signals are used for transmission and reception.

Master mode: MSIOF_TSCK (MSIOF_SCK) and MSIOF_TSYNC (MSIOF_SYNC) are output.

Slave mode: MSIOF_TSCK (MSIOF_SCK) and MSIOF_TSYNC (MSIOF_SYNC) are input.

23.4.2 Serial Clocks

(1) Clock Output in Master Mode

In master mode, the baud rate generator is used to generate the serial clock. The division ratio is from 1/1 to 1/1024.

(2) Clock Input in Slave Mode

In slave mode, the clock input for transmission and reception is used as the serial clock.

(3) Multiple Channel Function

This module provides the multiple channel function as shown in figure 23.2.

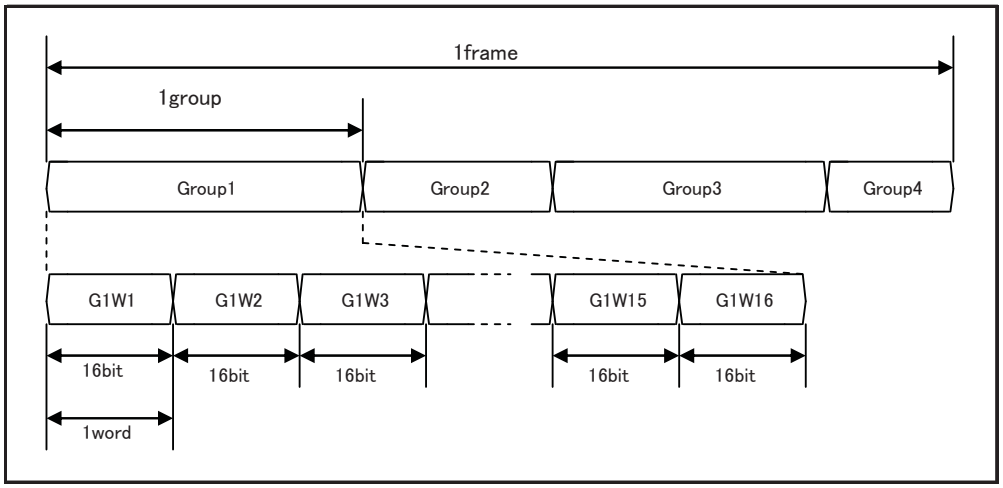


Figure 23.2 Multiple Channel Structure

The following conditions can be specified for the multiple channel function.

- Up to four groups in one frame
- Up to 256 words in one group
- Eight bits to 32 bits in one word
- Up to three blank bits can be inserted between groups

Note the following limitations by the number of groups.

Table 23.4 Maximum Word Size and Group Size Limited by Number of Groups

Number of Groups	Maximum Word Size	Maximum Group Size
One or two	32 bits	256 words
Three or four	16 bits	16 words

23.4.3 Serial Timing

(1) MSIOF_TSYNC, MSIOF_RSYNC

The MSIOF_TSYNC and MSIOF_RSYNC are frame synchronization signals. The following four modes are available.

- Frame start synchronization pulse: 1-bit-width pulse indicating the start of a frame
- Last bit synchronization pulse: 1-bit-width pulse indicating the last bit in a word
- Level/SPI: Level signal asserted during frame transmission
- L/R: 1/2-frame-width pulse indicating the first-half groups in a high level and the last-half groups in a low level

Figures 23.3 to 23.6 show the synchronization timing in these modes using the MSIOF_TSYNC and MSIOF_RSYNC signals.

(a) Frame Start Synchronization Pulse

The rising edge of the synchronization pulse indicates the start of a frame.

The delay between the rising edge of the synchronization signal and the start of data transmission or reception can be specified with the DTDL bits. The width of the synchronization pulse can be extended through the SYNCDL bit setting.

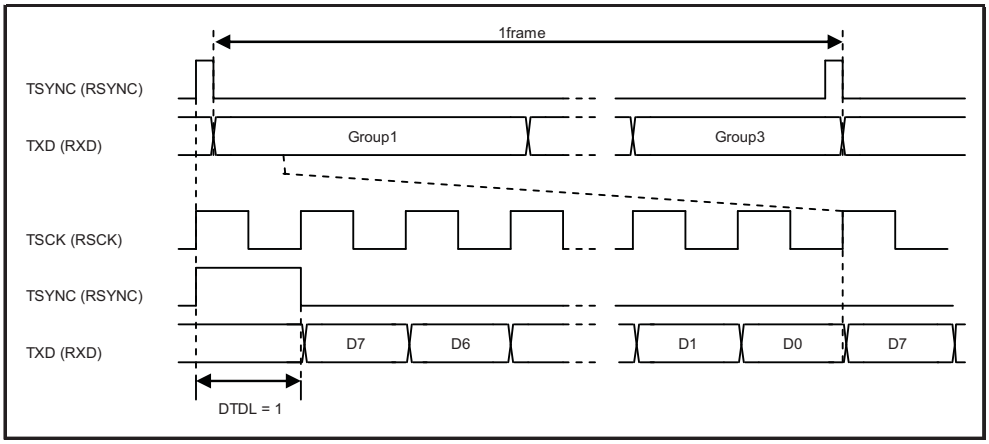


Figure 23.3 Synchronization Timing in Start Frame Synchronization Pulse Mode

(b) Last Bit Synchronization Pulse

The rising edge of the synchronization pulse indicates the last bit of each word.

The delay between the last bit of a word and the synchronization pulse can be specified with the DTDL bits.

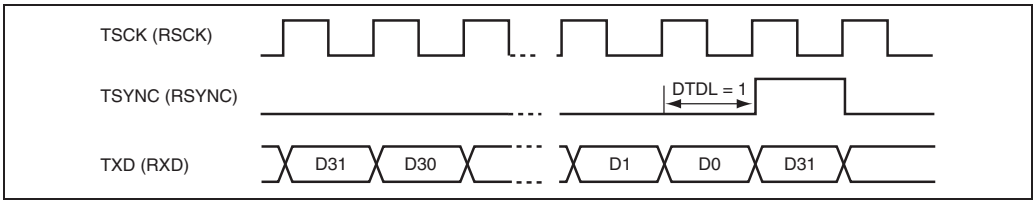


Figure 23.4 Synchronization Timing in Last Bit Synchronization Pulse Mode

(c) Level Synchronization

The synchronization signal is driven high for the frame length.

The delay between the rising edge of the synchronization signal and the start of transmission or reception can be specified with the DTDL bits and the delay between the end of transmission or reception and the falling edge of the synchronization signal can be specified with the SYNCDL bits (DTDL = 0 to 2 and SYNCDL = 0 to 3). This mode is available for the SPI master or slave operation.

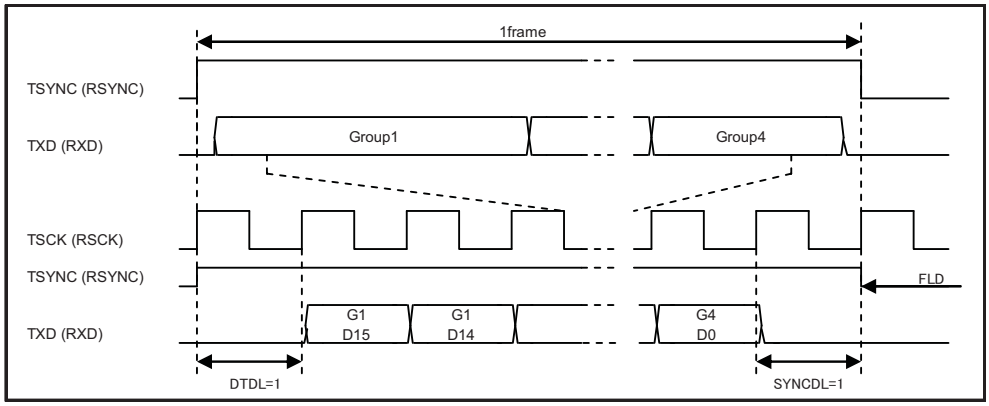


Figure 23.5 Synchronization Timing in Level Synchronization Mode

(d) L/R Synchronization

A high level in the synchronization signal indicates the first-half groups and a low level indicates the last-half groups.

The delay between the rising or falling edge of the synchronization signal and the start of transmission or reception can be specified with the DTDL bits and the delay between the end of transmission or reception and the falling or rising edge of the synchronization signal can be specified with the SYNCDL bits (DTDL = 0 to 2 and SYNCDL = 0 to 3).

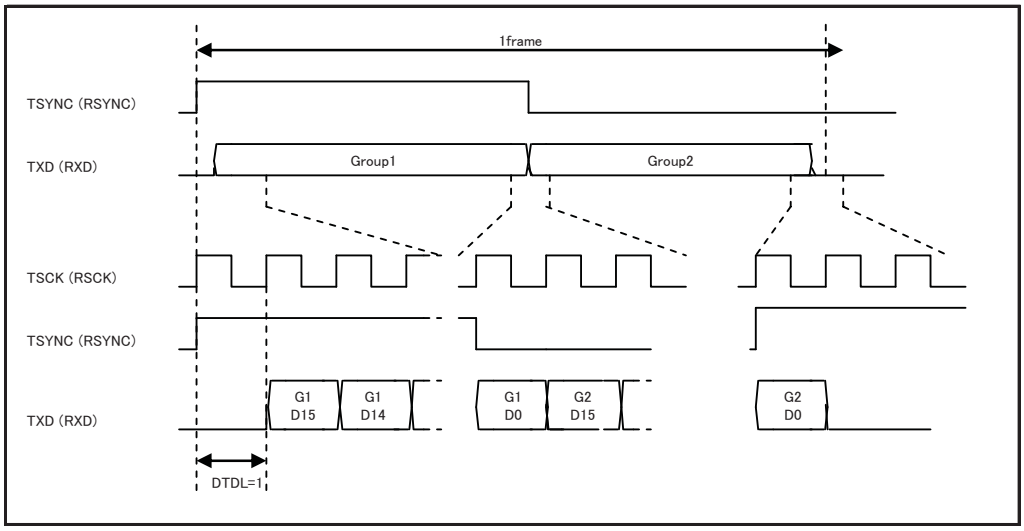


Figure 23.6 Synchronization Timing in L/R Synchronization Mode

(2) Transmit/Receive Timing

The timing of MSIOF_TXD transmission relative to MSIOF_TSCK and of MSIOF_RXD reception relative to MSIOF_RSCK can be specified as sampling on either edge, as listed below. The respective settings are made in TEDG and REDG bits of SICTR.

- Falling-edge sampling
- Rising-edge sampling

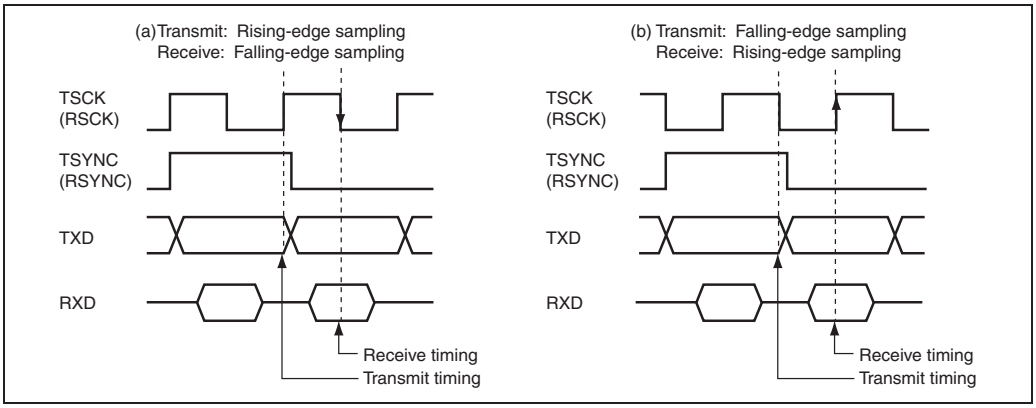


Figure 23.7 Transmit/Receive Timing.

23.4.4 Control Data Interface

For the groups specified with the CRDE bits in SITMDR2 and SIRMDR2, data is not stored in the FIFOs but handled as control data to be stored in SITDR1/SITDR2 and SIRDR1/SIRDR2.

Control data is transferred in the following two ways, which can be selected through the CRDNUM bits in SITMDR2 and SIRMDR2, as shown in figure 23.8.

- Only the first word in the group is transferred as valid data.
- All words in the group is transferred as valid data.

For the invalid data period during transmission, the value specified in the TXDIZ bit is output. The invalid receive data is not stored in SIRDR1 or SIRDR2.

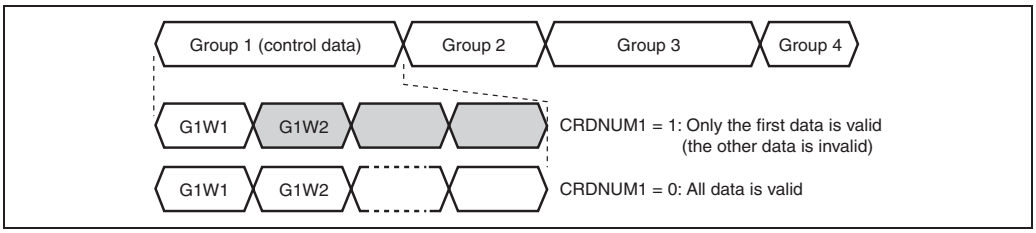


Figure 23.8 Control Data Allocation

23.4.5 Transfer Data Allocation to Registers

(1) Transmit/Receive Data

Transmit/receive data (FIFO data and control data) should be written to or read from the following registers.

- Transmit FIFO data writing: SITFDR (32-/16-/8-bit access)
- Control data writing: SITDR1 and SITDR2 (32-/16-bit access)
- Receive FIFO data reading: SIRFDR (32-/16-/8-bit access)
- Control data reading: SIRDR1 and SIRDR2 (32-/16-bit access)

Only 16-bit access to FIFO data is allowed. However, both upper 16-bit access and lower 16-bit access are possible to control data.

When the word size is smaller than the transmit FIFO data access size, the upper bits are transmitted as valid data. For example, when writing data to the transmit FIFO by 32-bit access and transmitting a16-bit word, the upper 16 bits are transmitted and the lower 16 bits are discarded as invalid data.

In the same way, when the word size is larger than the receive FIFO data access size, the upper bits are received as valid data. For example, when 32-bit data is stored in the receive FIFO and the data is read by 16-bit access, the lower 16 bits are discarded as invalid data.

Figure 23.9 shows the bit alignment of these registers.

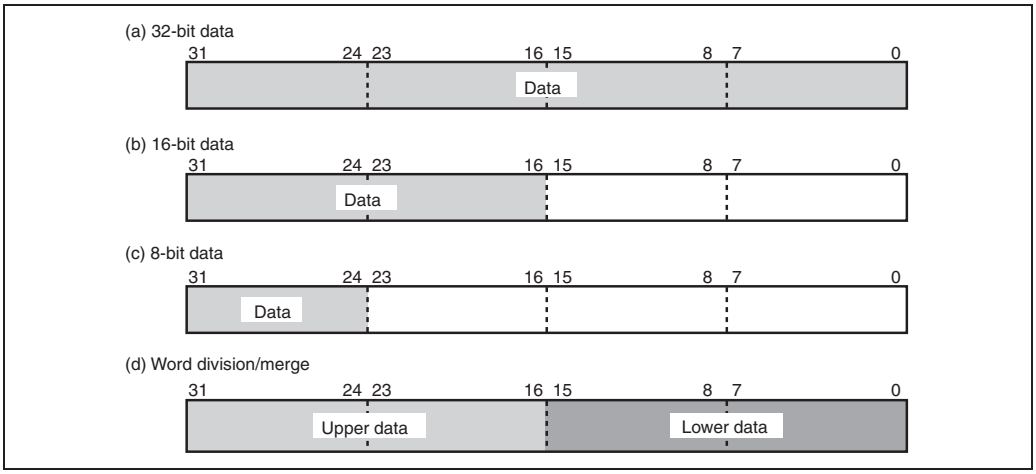


Figure 23.9 Transmit/Receive Data Bit Alignment

23.4.6 FIFO

(1) Overview

The transmit and receive FIFOs of the MSIOF have the following features.

- 32 bits × 64 stages for transmission and 32 bits × 256 stages for reception
- The FIFO pointer is updated in one read or write cycle regardless of the access size of the CPU or DMAC. (One access cannot be divided into multiple accesses.)

(2) Transfer Request

A request for FIFO data transfer can be issued to the CPU or DMAC as the following interrupt sources.

- FIFO transmit request: TDREQ (interrupt source for transmission)
- FIFO receive request: RDREQ (interrupt source for reception)

The conditions for requesting FIFO data transfer can be specified separately for transmission and reception. The conditions for the transmit FIFO and receive FIFO are specified in the TFWM[2:0] bits and RFWM[2:0] bits in SIFCTR, respectively.

Table 23.5 Condition for Issuing Transmit Request

TFWM[2:0]	Number of Requested Stages	Condition for Transmit Request	Areas Used
000	1	64 stages of empty area	Smallest
001	32	32 or more stages of empty area	↑
010	40	24 or more stages of empty area	↑
011	48	16 or more stages of empty area	↑
100	52	12 or more stages of empty area	↑
101	56	8 or more stages of empty area	↑
110	60	4 or more stages of empty area	↑
111	64	1 or more stages of empty area	Largest

Table 23.6 Condition for Issuing Receive Request

RFWM[2:0]	Number of Requested Stages	Condition for Receive Request	Areas Used
000	1	1 or more stages of valid data	Smallest
001	4	4 or more stages of valid data	
010	8	8 or more stages of valid data	
011	16	16 or more stages of valid data	
100	32	32 or more stages of valid data	
101	64	64 or more stages of valid data	
110	128	128 or more stages of valid data	
111	256	256 stages of valid data	Largest

The maximum FIFO stages are always available even if the data area or empty area exceeds the size specified for the transfer condition. Accordingly, an overflow error or an underflow error occurs if the data area or empty area exceeds the maximum number of FIFO stages.

The FIFO transfer request is canceled when the specified condition is not satisfied even if the FIFO does not become empty or full.

(3) Number of FIFOs

The number of transmit and receive FIFO stages used are indicated by the following registers.

- Transmit FIFO: The number of empty FIFO stages is indicated by the TFUA[6:0] bits in SIFCTR.
- Receive FIFO: The number of valid data stages is indicated by the RFUA[8:0] bits in SIFCTR.

These registers show the number of data stages that can be transferred by the CPU or DMAC.

23.4.7 Transmit and Receive Procedures

(1) Transmission in Master Mode

Figure 23.10 shows an example of settings and operation for transmission in master mode.

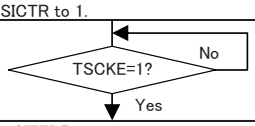
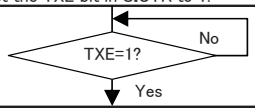
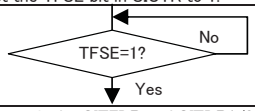
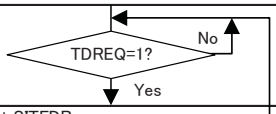
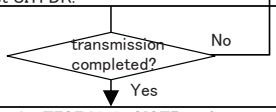
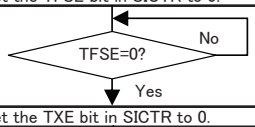
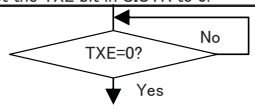
No.	Flow chart	Setting	operation
1	Set SITMDR1/2/3 SITSCR , SIFCTR , and SIIER.	Set the operating mode, serial clock , and FIFO threshold value, and enable interrupts.	
2	Set the TSCKE bit in SICTR to 1.	Set output sampling and start the baud rate generator.	Outputs the serial clock.
3		Read 1 from TSCKE bit in SICTR.	
4	Set SITFDR, SITDR1/2.	Set transmit data.	
5	Set the TXE bit in SICTR to 1.	Enable transmittion.	
6		Read 1 from TXE bit in SICTR.	
7	Set the TFSE bit in SICTR to 1.	Starting output frame of synchronization signal.	Outputs the frame syncronization signal.
8		Read 1 from TFSE bit in SICTR.	
9	Transmit the SITFDR and SITDR1/2 contents through TXD in synchronization with		Transmit data.
10			Assert transmit data transfer request according to the FIFO threshold valu
11	Set SITFDR.	Set transfer data.	
12		Read 1 from TFEMP bit in SICTR.	
13	Set the TFSE bit in SICTR to 0.	Disable output frame of synchronization signal.	
14		Read 0 from TFSE bit in SICTR.	
15	Set the TXE bit in SICTR to 0.	Disable transmit enable.	
16	 Transmission complete.	Read 0 from TXE bit in SICTR.	

Figure 23.10 Example of Transmit Procedure in Master Mode

(2) Reception in Master Mode with SITMDR1.PCON=0

Figure 23.11 shows an example of settings and operation for reception in master mode with SITMDR1.PCON=0.

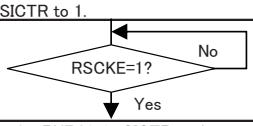
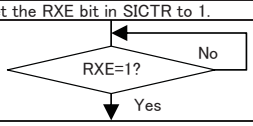
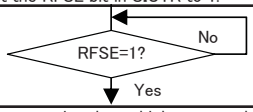
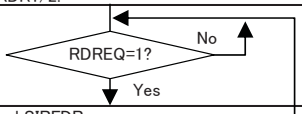
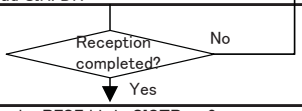
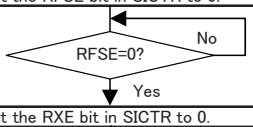
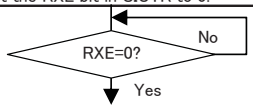
No.	Flow chart	Setting	operating
1	Set SIRMDR1/2/3 SITMDR1/2/3 SIRSCR , SIFCTR and SIIER.	Set the operating mode serial clock FIFO threshold value, and enable interrupts.	
2	Set the RSCKE bit in SICTR to 1.	Set output sampling and start the baud rate generator.	Outputs the serial clock.
3		Read 1 from RSCKE bit in SICTR.	
4	Set the RXE bit in SICTR to 1.	Enable reception.	
5		Read 1 from RXE bit in SICTR.	
6	Set the RFSE bit in SICTR to 1.	Starting output frame of synchronization signal.	Outputs the frame syncronization signal.
7		Read 1 from RFSE bit in SICTR.	
8	The reception data which was synchronized with RSYNC are stored to SIRFDR or SIRDR1/2.		Data Reception.
10			Assert receiving data transfer enable according to the FIFO threshold valu
11	Read SIRFDR	Read reception data.	
12			
13	Set the RFSE bit in SICTR to 0.	Disable output frame of synchronization signal.	
14		Read 0 from RFSE bit in SICTR.	
15	Set the RXE bit in SICTR to 0.	Disable receive enable.	
16	 Receiving data complete.	Read0 from RXE bit in SICTR	

Figure 23.11 Example of Receive Procedure in Master Mode(SITMDR1.PCON=0)

(3) Reception in Master Mode with SITMDR1.PCON=1

Figure 23.12 shows an example of settings and operation for reception in master mode with SITMDR1.PCON=1.

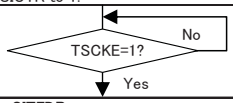
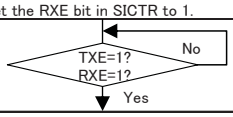
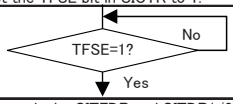
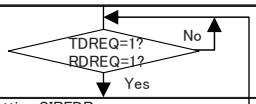
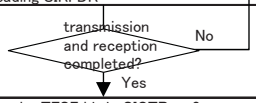
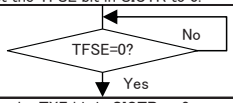
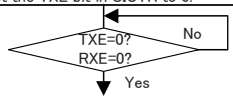
No.	Flow chart	Setting	operation
1	Set SIRMDR1/2/3 SITMDR1/2/3 SIRSCR , SIFCTR and SIIER.	Set the operating mode with dummy transmit when SPI mode. serial clock FIFO threshold value, and enable interrupts.	
2	Set the TSCKE bit in SICTR to 1.	Set output sampling and start the baud rate generator.	Outputs the serial clock.
3		Read 1 from TSCKE bit in SICTR.	
4	Set SITFDR, SITDR1/2.	Set transmit dummy data. Dummy write need same size as required receiving data.	
5	Set the TXE bit in SICTR to 1. Set the RXE bit in SICTR to 1.	Enable transmittion. Enable reception.	
6		Read 1 from TXE bit in SICTR. Read 1 from RXE bit in SICTR.	
7	Set the TFSE bit in SICTR to 1.	Starting output frame of synchronization signal.	Outputs the frame syncronization signal.
8		Read 1 from TFSE bit in SICTR.	
9	Transmit the SITFDR and SITDR1/2 contents through TXD in synchronization with Receiving data was stored to SIRFDR and SIRDR1/2 in synchronization with MSIOF_TSYNC.		Transmit and reception.
10			Assert transmit data transfer request and reception data transfer request according to the FIFO threshold valu
11	Setting SIRFDR Reading SIRFDR	Writing transmit data. Reading receiving data.	
12			
13	Set the TFSE bit in SICTR to 0.	Disable output frame of synchronization signal.	
14		Read 0 from TFSE bit in SICTR.	
15	Set the TXE bit in SICTR to 0.	Disable transmit enable.	
16	 Transmission complete.	Read 0 from TXE bit in SICTR. Read 0 from RXE bit in SICTR.	

Figure 23.12 Example of Receive Procedure in Master Mode(SITMDR1.PCON=1)

(4) Transmission in Slave Mode

Figure 23.13 shows an example of settings and operation for transmission in slave mode.

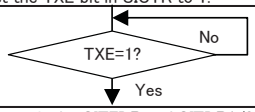
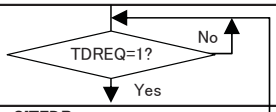
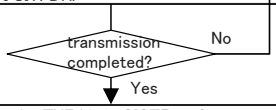
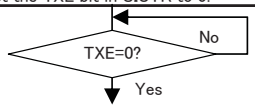
No.	Flow chart	Setting	operation
1	Setting master device polarity	Depend on master device.	Decide SYNC/SCK polarity
2	Set SITMDR1/2/3 SIFCTR and SIIER.	Set operating mode FIFO threshold value and enable interrupts.	
3	Set SITFDR, SITDR1/2.	Set transmit data.	
4	Set the TXE bit in SICTR to 1.	Enable transmittion.	
5		Read 1 from TXE bit in SICTR.	
6	Transmit the SITFDR and SITDR1/2 contents through TXD in synchronization with		Data transmit
7			Assert transmit data transfer request according to the FIFO threshold valu
8	Set SITFDR.	Set transfer data.	
9			
10	Set the TXE bit in SICTR to 0.	Disable transmit enable.	
11	 Transmission complete.	Read 0 from TXE bit in SICTR.	

Figure 23.13 Example of Transmit Procedure in Slave Mode

(5) Reception in Slave Mode

Figure 23.14 shows an example of settings and operation for reception in slave mode.

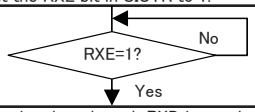
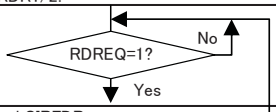
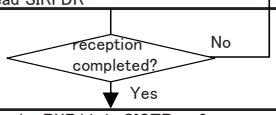
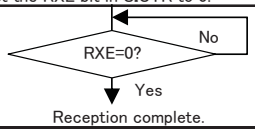
No.	Flow chart	Setting	operation
1	Setting master device polarity	Depend on master device.	Decide SYNC/SCK polarity
2	Set SIRMDR1/2/3 SIFCTR and SIIER.	Set operating mode FIFO threshold value and enable interrupts.	
3	Set the RXE bit in SICTR to 1.	Enable reception.	
4		Read 1 from RXE bit in SICTR.	
5	Receive data through RXD in synchronization with MSIOF_RSYNC and store it in SIRFDR and SIRDR1/2.		Data receive
6			Assert reception data transfer request according to the FIFO threshold valu
7	Read SIRFDR	Read reception data.	
8			
9	Set the RXE bit in SICTR to 0.	Disable reception enable	
10		Read 0 from RXE bit in SICTR.	

Figure 23.14 Example of Receive Procedure in Slave Mode

(6) Reset

After a power-on reset is applied, module stop state is canceled, or a reset signal is asserted through the TXRST or RXRST setting in SICTR, it takes about SUBϕ20 cycles to complete the internal reset of the module. During a period from the beginning of reset until the TXRST or RXRST value is read as 0, do not modify the control register or access the FIFOs.

The MSIOF can separately reset the transmit and receive units by setting the following bits to 1.

- Transmit reset: TXRST bit in SICTR
- Receive reset: RXRST bit in SICTR

Table 23.7 Transmit and Receive Reset

Type	Objects Initialized
Transmit reset	SITDR1, SITDR2, and SITFDR
	Transmit FIFO write pointer
	TCRDY, TFEMP, and TDREQ bits in SISTR
	TXE bit in SICTR
Receive reset	SIRDR1, SIRDR2, and SIRFDR
	Receive FIFO read pointer
	RCRDY, RFFUL, and RDREQ bits in SISTR
	RXE bit in SICTR

(7) Initial Operating Mode

After a power-on reset, both the transmit and receive units are initialized to master mode (0 is output through CLK and SYNC). When using slave mode, keep the connected device outputting 0 until the operating mode setting is completed.

23.4.8 Interrupts

The MSIOF has one type of interrupt.

(1) Interrupt Sources

Interrupts can be generated by several sources. Each source is shown as an MSIOF status in SISTR. Table 23.8 lists the MSIOF interrupt sources.

Table 23.8 MSIOF Interrupt Sources

No.	Classification	Bit Name	Function Name	Description
1	Transmission	TDREQ	Transmit FIFO transfer request	The transmit FIFO has empty space of specified size or more.
2		TFEMP	Transmit FIFO empty	The transmit FIFO is empty.
3		TEOF	Frame Transmission End	Transmission of data with a length of one frame is completed.
4	Reception	RDREQ	Receive FIFO transfer request	The receive FIFO stores data of specified size or more.
5		RFFUL	Receive FIFO full	The receive FIFO is full.
6		REOF	Frame reception end	Reception of data with a length of one frame is completed.
7	Control	TCRDY	Transmit control data ready	The transmit control data register is ready to be written.
8		RCRDY	Receive control data ready	The receive control data register stores valid data.
9	Error	TFUDF	Transmit FIFO underflow	Serial data transmit timing has arrived while the transmit FIFO is empty.
10		TFOVF	Transmit FIFO overflow	The transmit FIFO is written to while it is full.
11		RFOVF	Receive FIFO overflow	Serial data is received while the receive FIFO is full.
12		RFUDF	Receive FIFO underflow	The receive FIFO is read while the receive FIFO is empty.
13		TFSERR	Transmit FS error	A transmit frame synchronization signal is input before the specified number of bits has been reached (in slave mode).
14		RFSERR	Receive FS error	A receive frame synchronization signal is input before the specified number of bits has been reached (in slave mode).

Whether an interrupt is issued from an interrupt source is determined by the SIIER settings. If an interrupt source bit is set to 1 and the corresponding bit in SIIER is set to 1, an MSIOF interrupt is issued.

(2) TDREQ and RDREQ

The transmit FIFO transfer request (TDREQ) and receive FIFO transfer request (RDREQ) are signals indicating the state. If the state changes after TDREQ or RDREQ is set, it is automatically cleared by the MSIOF.

When the DMA transfer is used, a DMA transfer request signal is pulled low for one cycle at the end of DMA transfer.

(3) Processing when Errors Occur

- Transmit FIFO underflow (TFUDF)
  The value specified with TXDIZ in SICTR is output.
- Transmit FIFO overflow (TFOVF)
  The contents of the transmit FIFO are protected, and the write operation causing the overflow is ignored.
- Receive FIFO overflow (RFOVF)
  Data causing the overflow is discarded and lost.
- Receive FIFO underflow (RFUDF)
  An undefined value is output on the bus.
- Transmit FS error (TFSERR)
  The internal counter is reset according to the synchronization signal in which an error occurs.
- Receive FS error (RFSERR)
  The internal counter is reset according to the synchronization signal in which an error occurs.

23.4.9 Transmit and Receive Timing

Examples of the MSIOF serial transmission and reception are shown in figures 23.14 and 23.15.

(1) 16-Bit Synchronization Pulse

Synchronization pulse method, one group, one word, 16 bits in a word, no bit delay

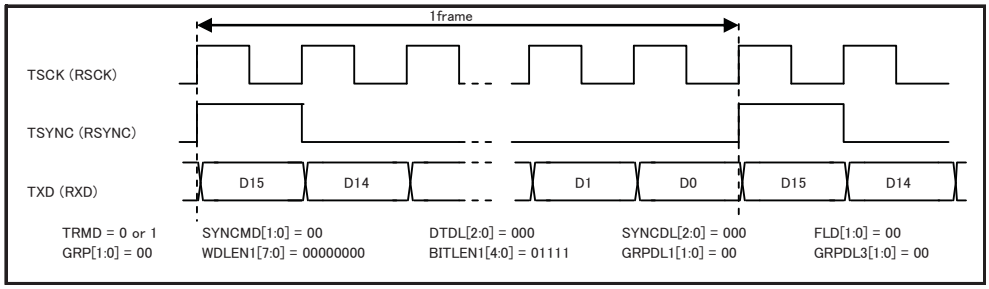


Figure 23.15 Transmit and Receive Timing (16 Bits)

(2) 32-Bit Synchronization Pulse

Synchronization pulse method, one group, 32 words, 32 bits in a word, 1-bit delay

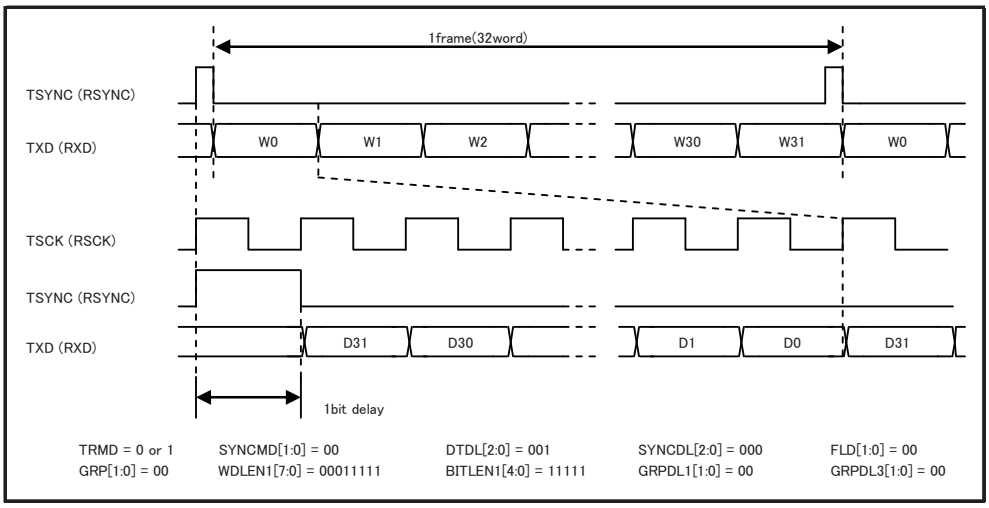


Figure 23.16 Transmit and Receive Timing (32 Bits)

(3) 24-Bit IIS Transmission

L/R mode, 2 groups, 1 word for each group, 24-bit word for each group, 1-bit delay

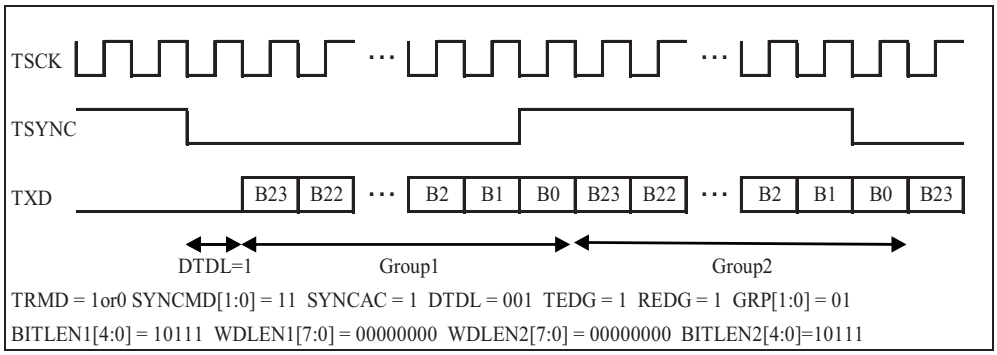


Figure 23.17 Transmit Timing(24-Bit IIS)

(4) μ-WIRE (Transmission Only)

Level mode, 2 groups, 1 word for each group, 8-bit/16-bit words, 1-bit delay

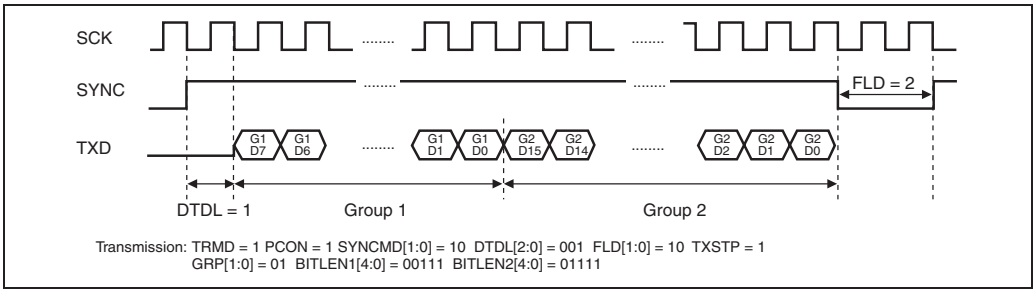


Figure 23.18 Transmit Timing (μ-WIRE Transmission)

(5) μ-WIRE (Transmission/Reception Switching)

Level mode, 2 groups, 1 word for each group, 16-bit/32-bit words, 1-bit delay

Transmit group 1 output masking, and receive group 2 input masking

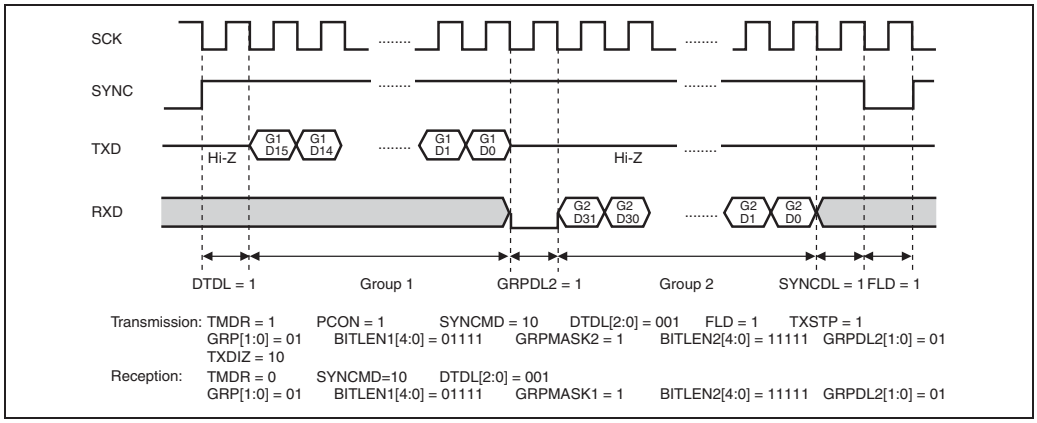


Figure 23.19 Transmit and Receive Timing (μ-WIRE)

23.4.10 SPI

With the appropriate register settings, the MSIOF can be used as an SPI device.

(1) Example of SPI Device Connection

Figure 23.19 shows an example of connection with an SPI device.

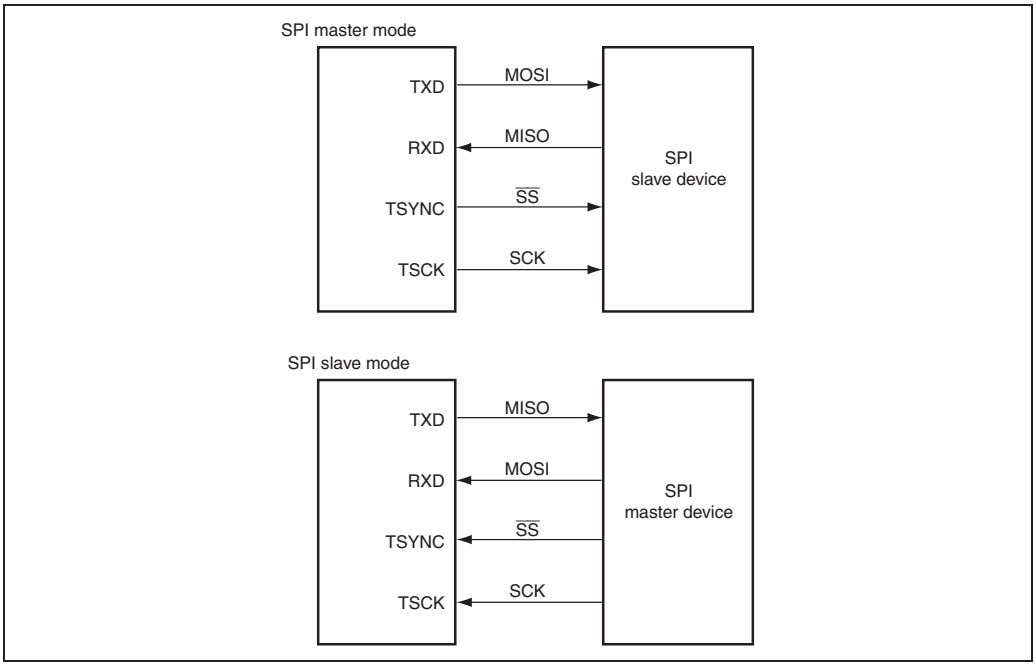
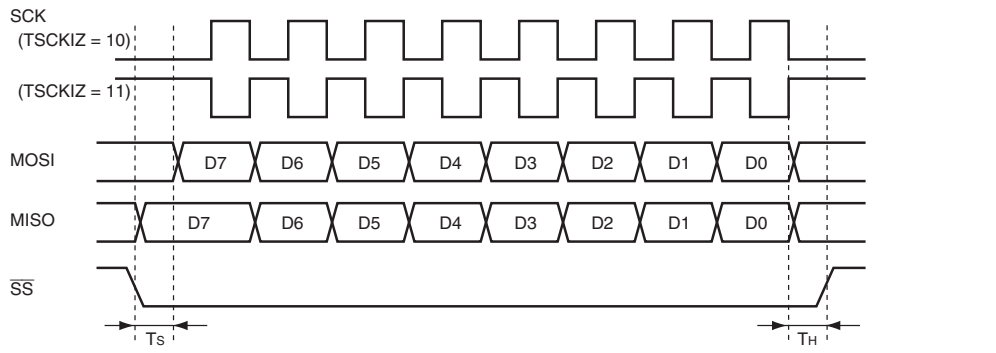


Figure 23.20 Example of SPI Device Connection

(2) SPI Serial Clock Timing

Figures 23.20 and 23.21 show the data and clock timing in SPI mode. As shown in the figures, four types of serial transfer formats can be used.



Transmit: TRMD = 1 (master) or 0 (slave) PCON = 1 SYNCMD[1:0] = 10 SYNCAC = 1
GRP[1:0] = 00 BITLEN1[4:0] = 00111 WDLEN1[7:0] = 00000000 GRPDL1[1:0] = 00 GRPDL3[1:0] = 00

Receive: TRMD = 0 SYNCMD[1:0] = 10 SYNCAC = 1
GRP[1:0] = 00 BITLEN1[4:0] = 00111 WDLEN1[7:0] = 00000000 GRPDL1[1:0] = 00 GRPDL3[1:0] = 00

Set DTDL to satisfy T_S (0 to 2 can be specified in 0.5-clock-cycle units)
Set SYNCDL to satisfy T_H (0 to 2 can be specified in 0.5-clock-cycle units)
The sum of DTDL and SYNCDL settings should be an integer.

SICTR: Upper: TSCKIZ[1:0] = 10, RSCKIZ[1:0] = 10, TEDG = 1, REDG = 1
Lower: TSCKIZ[1:0] = 11, RSCKIZ[1:0] = 11, TEDG = 0, REDG = 0

Figure 23.21 SPI Clock and Data Timing 1

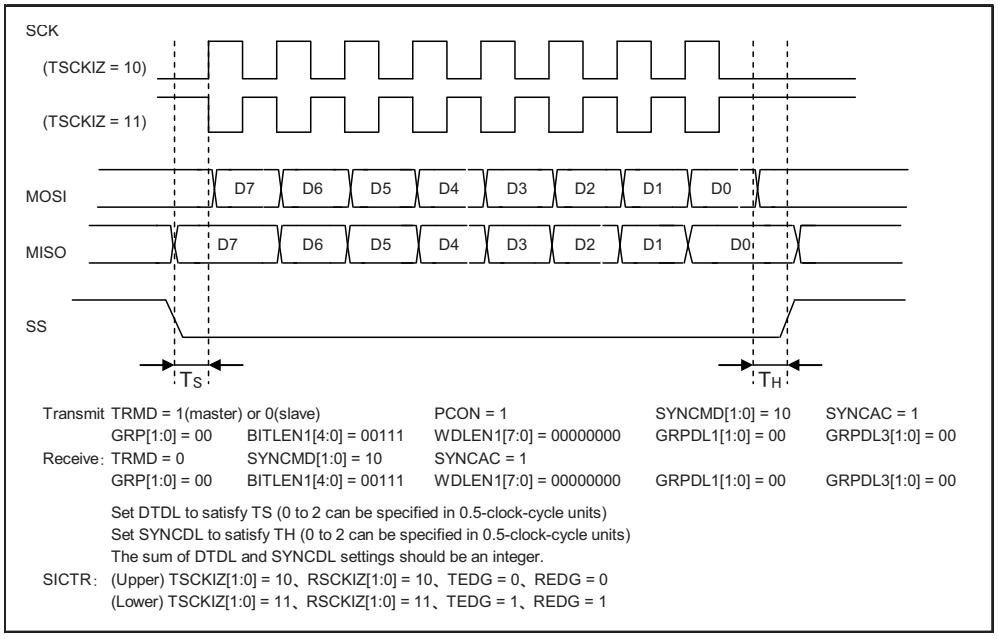


Figure 23.22 SPI Clock and Data Timing 2

23.4.11 Notes for Using SPI Mode

- When the module stop release or software reset is performed in SPI mode, set the control register (SICTR) again with each of the receive-setting bits (RSCKIZ/REDG) being 0.
- For SPI master mode operation, set the FLD bits in SITMDR1 for at least 4 cycles of SUBϕ.
- For SPI slave mode operation, set the frame synchronization signal interval to at least 4 cycles of SUBϕ.
- For SPI slave mode operation, The setting for data delay should always set 0.
- For SPI slave mode operation, TXDIZ bits work on SS signal invalid state.

23.4.12 IIS

This module can support IIS format with following setting which is shown Figure 23.23 and Figure 23.24.BITLEN1/2 bit will change by usage.

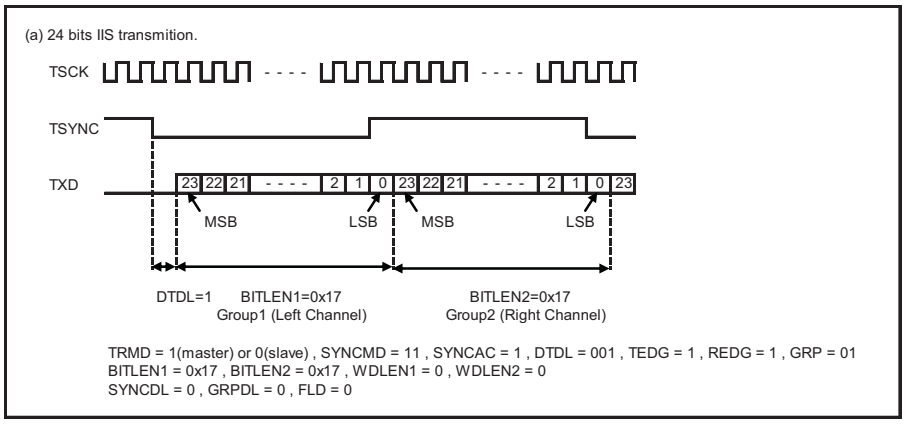


Figure 23.23 24 bits IIS transmition

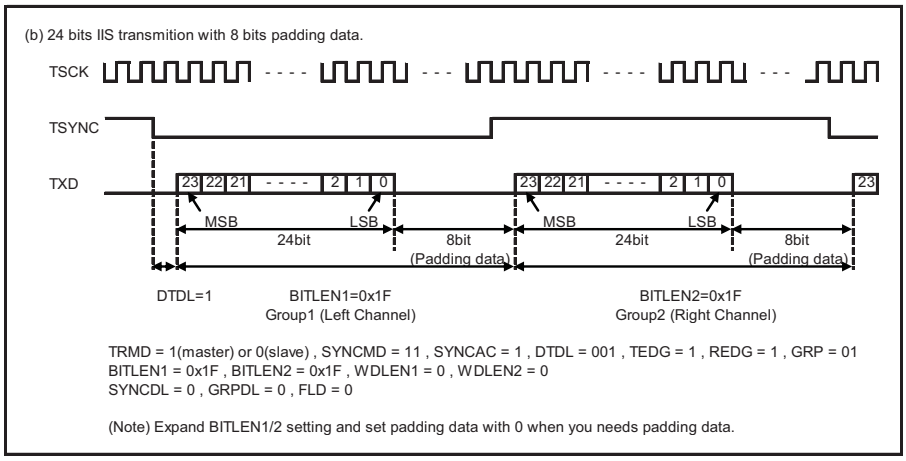


Figure 23.24 24 bits IIS transmition with 8 bits padding data

Section 24 Baseband Interface (BBIF1)

This LSI includes one channel of clock-synchronized serial I/O module (BBIF1) with FIFO, which can be connected to the BB domain MMIF.

24.1 Features

- Secure read processing from the MMIF to BBIF1 using the flow control pin.
- FIFO capacity: 32 bits × 64 stages for transmission and 32 bits × 256 stages for reception
- MSB first or LSB first selectable for data transmission and reception
- Synchronization in frame synchronization pulse, level, or left/right channel switch mode
- Supports both transmit master mode and receive slave mode (fixed).
- Independent clock and synchronization signals for transmission and reception
- Supports multiple-channel communication
  - Transfers multiple groups or words in one frame.
  - The word size for each group can be selected from eight to 32 bits.
  - Up to 256 words can be transferred in each group when one or two groups are used, or up to 16 words can be transferred in each group when three or four groups are used.
- Interrupts: One type
- Serial clock

  The internal clock (SUBϕ) is used as the serial clock source for transmission, and the receive serial clock input is used for reception.
- DMA transfer

  Supports multibyte DMA transfer.
  Supports DMA transfer by a transfer request for transmission and reception
- Serial format

  Supports the IIS and SPI serial formats (for master mode).

Figure 24.1 shows a block diagram of the BBIF1.

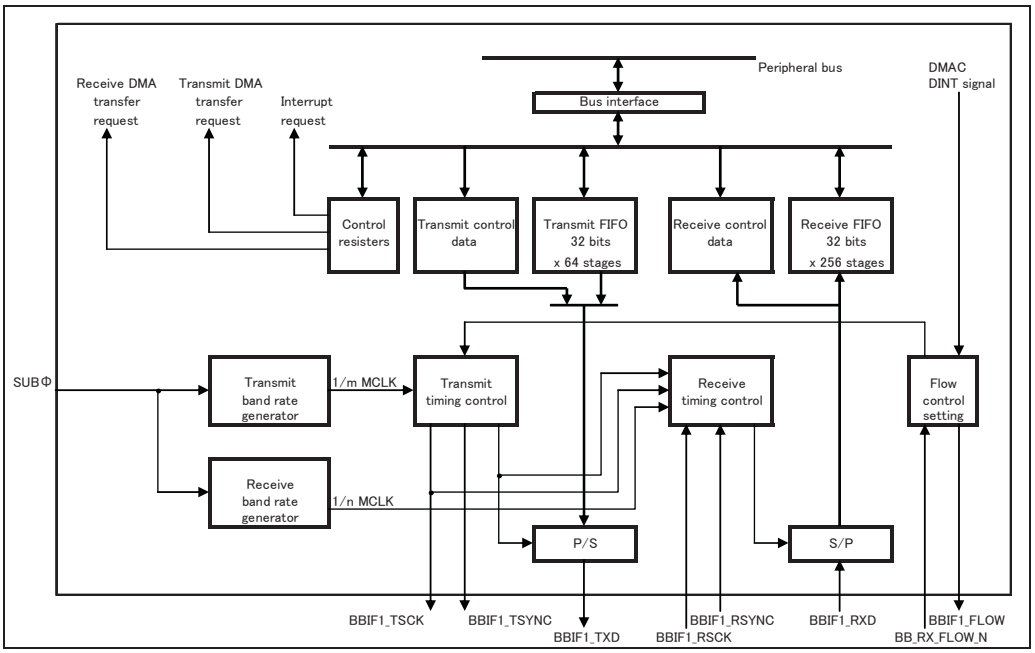


Figure 24.1 Block Diagram of BBIF1

24.2 Input/Output Pins

The pin configuration in this module is shown in Table 24.1.

Table 24.1 Pin Configuration

Name	I/O	Function
BBIF1_TSCK	Output	Serial clock for transmission
BBIF1_TSYNC	Output	Frame synchronization signal for transmission
BBIF1_RSCK	Input	Serial clock for reception
BBIF1_RSYNC	Input	Frame synchronization signal for reception
BBIF1_TXD	Output	Transmit data
BBIF1_RXD	Input	Receive data
BBIF1_FLOW	Output	APL Flow control signal
BB_RX_FLOW_N	Input	BB Flow control signal

24.3 Register Descriptions

Table 24.2 shows the register configuration of the BBIF1. Table 22.3 shows the register state in each processing mode.

Table 24.2 BBIF1 Register Configuration

Name	Abbreviation	R/W	Address	Access Size
BBIF1 transmit mode register 1	SITMDR1	R/W	H'E6C90000 H'E7C90000	32
BBIF1 transmit mode register 2	SITMDR2	R/W	HE6C90004 HE7C90004	32
BBIF1 transmit mode register 3	SITMDR3	R/W	H'E6C90008 H'E7C90008	32
BBIF1 receive mode register 1	SIRMDR1	R/W	H'E6C90010 H'E7C90010	32
BBIF1 receive mode register 2	SIRMDR2	R/W	H'E6C90014 H'E7C90014	32
BBIF1 receive mode register 3	SIRMDR3	R/W	H'E6C90018 H'E7C90018	32
BBIF1 transmit clock select register	SITSCR	R/W	H'E6C90020 H'E7C90020	16
BBIF1 control register	SICTR	R/W	H'E6C90028 H'E7C90028	32
BBIF1 FIFO control register	SIFCTR	R/W	H'E6C90030 H'E7C90030	32
BBIF1 status register	SISTR	R/W	H'E6C90040 H'E7C90040	32
BBIF1 interrupt enable register	SIIER	R/W	H'E6C90044 H'E7C90044	32
BBIF1 transmit control data register 1	SITDR1	W	H'E6C90048 H'E7C90048	16/32
BBIF1 transmit control data register 2	SITDR2	W	H'E6C9004C H'E7C9004C	16/32

Name	Abbreviation	R/W	Address	Access Size
BBIF1 transmit FIFO data register	SITFDR	W	H'E6C90050 H'E7C90050	16/32
BBIF1 receive control data register 1	SIRDR1	R	H'E6C90058 H'E7C90058	16/32
BBIF1 receive control data register 2	SIRDR2	R	H'E6C9005C H'E7C9005C	16/32
BBIF1 receive FIFO data register	SIRFDR	R	H'E6C90060 H'E7C90060	16/32
BBIF1 flow control register	SIFLCTR	R/W	H'E6C90064 H'E7C90064	32

Table 24.3 Register States in Each Operating Mode

Abbreviation	Power-on Reset	Module Standby
SITMDR1	Initialized	Retained
SITMDR2	Initialized	Retained
SITMDR3	Initialized	Retained
SIRMDR1	Initialized	Retained
SIRMDR2	Initialized	Retained
SIRMDR3	Initialized	Retained
SITSCR	Initialized	Retained
SICTR	Initialized	Retained
SIFCTR	Initialized	Retained
SISTR	Initialized	Retained
SIIER	Initialized	Retained
SITDR1	Initialized	Initialized
SITDR2	Initialized	Initialized
SITFDR	Initialized	Initialized
SIRDR1	Initialized	Initialized
SIRDR2	Initialized	Initialized
SIRFDR	Undefined	Initialized
SIFLCTR	Initialized	Retained

24.3.1 BBIF1 Transmit Mode Register 1 (SITMDR1)

SITMDR1 is a 32-bit readable/writable register that specifies the BBIF1 transmit mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TRMD	—	SYNCMD[1:0]		SYNCCH[1:0]		SYNCA0	BITLSB	—	DTDL[2:0]			—	SYNCDL[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
R/W:	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	DIV[3:0]				—	—	—	—	FLD[1:0]		CONT	TXSTP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31	TRMD	1	R/W	Transfer Mode Selects the transfer mode. 0: Setting prohibited 1: Master mode
30	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
29, 28	SYNCMD [1:0]	00	R/W	SYNC Mode These bits specify the mode for the BBIF1_TSYNC signal. 00: Frame start synchronization pulse 01: 1-bit synchronization pulse for last data in slot 10: Level mode/SPI 11: L/R mode
27, 26	SYNCCH [1:0]	00	R/W	Synchronization Signal Channel Select 00: The frame synchronization signal is output from BBIF1_TSYNC. Other than above: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Descriptions
25	SYNCAC	0	R/W	BBIF1_TSYNC Polarity 0: Active-high signal in synchronization pulse or level mode, or driven high then low in L/R mode 1: Active-low signal in synchronization pulse or level mode, or driven low then high in L/R mode
24	BITLSB	0	R/W	MSB/LSB First 0: MSB first 1: LSB first
23	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
22 to 20	DTDL[2:0]	001	R/W	Data Pin Bit Delay for BBIF1_TSYNC Pin B'1xx is valid only in SPI mode. In SPI mode, these bits should be specified so that the sum of the delays specified through the DTDL[2:0] and SYNCDL[2:0] bits becomes an integer value. 000: No bit delay 001: 1-clock-cycle delay 010: 2-clock-cycle delay 101: 0.5-clock-cycle delay 110: 1.5-clock-cycle delay Other than above: Setting prohibited
19	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
18 to 16	SYNCDL [2:0]	000	R/W	Frame Synchronization Signal Timing Delay These bits extend the transmit frame synchronization signal. This setting is invalid when SYNCMD[1:0] = B'01. B'1xx is valid only in SPI mode. In SPI mode, these bits should be specified so that the sum of the delays specified through the DTDL[2:0] and SYNCDL[2:0] bits becomes an integer value. When L/R mode , these bits should always be set to 000. 000: No bit delay 001: 1-clock-cycle delay 010: 2-clock-cycle delay 011: 3-clock-cycle delay 101: 0.5-clock-cycle delay 110: 1.5-clock-cycle delay Other than above: Setting prohibited
15 to 12	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
11 to 8	DIV[3:0]	0000	R/W	Word Division One 32-bit word stored in the transmit FIFO can be transmitted as two separate 16-bit words through two groups. The word count in each group must be set to 1. In this case, data of groups other than word division target groups must be handled as control data. This setting is valid only in LR mode. 0000: Not divided 0001: Upper word in group 1 and lower word in group 2 0100: Upper word in group 2 and lower word in group 1 Other than above: Setting prohibited
7 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3, 2	FLD[1:0]	00	R/W	Frame Synchronization Signal Interval These bits specify the minimum idle time between frames in the number of serial clock cycles. When Level mode, set the FLD bits in SIRMDR1 for at least 4 cycles of SUBφ When L/R mode , these bits should always be set to 00. 00: 0-clock-cycle delay 01: 1-clock-cycle delay 10: 2-clock-cycle delay 11: 3-clock-cycle delay

Bit	Bit Name	Initial Value	R/W	Descriptions
1	CONT	0	R/W	Continuous Frame Transmission Specifies continuous transmission of multiple frames of data within one frame. This setting is valid when SYNCMD[1:0] = B'00 or B'10. When the TFSE bit in SICTR is set to 0, transmission is terminated after one-frame data is transmitted. 0: Does not perform continuous transmission. 1: Performs continuous transmission.
0	TXSTP	0	R/W	Transmission Stop Specifies the processing performed when the remaining number of stages in the transmit FIFO becomes smaller than the total number of words in the transmit frame. This setting is valid only in master mode. When transmission is continued, the value specified with TXDIZ is output as transmit data. If, with TXSTP = 1, the remaining number of stages in the transmit FIFO becomes smaller than the total number of words in the transmit frame, transmission is stopped temporarily. After this, however, transmission is automatically restarted if writing into the transmit FIFO causes the remaining number to become larger than the total number of words in the transmit frame. 0: Continues transmission when the transmit FIFO is empty. (The frame synchronization signal is output.) 1: Temporarily stops transmission when the remaining number of stages in the transmit FIFO becomes smaller than the total number of words in the transmit frame. (The frame synchronization signal is not output.)

24.3.2 BBIF1 Transmit Mode Register 2 (SITMDR2)

SITMDR2 is a 32-bit readable/writable register that specifies the BBIF1 transmit mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GRP[1:0]		—	BITLEN1[4:0]					WDLEN1[7:0]							
Initial value:	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GRPDL1[1:0]		GRPDL3[1:0]		CRDE4	CRDE3	CRDE2	CRDE1	CRDNUM4	CRDNUM3	CRDNUM2	CRDNUM1	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31, 30	GRP[1:0]	00	R/W	Group Count The number of groups is set to the value specified in these bits + 1. When three or more groups are specified, the word size (BITLEN) is set to 16 bits or less.
29	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
28 to 24	BITLEN1[4:0] (BITLEN3)	01111	R/W	Word Size (8 to 32 bits) The word size (bits) of groups 1 and 3 is set to the value specified in these bits + 1. (BITLEN1 = BITLEN3) Eight bits or a larger size should be specified. When three or four groups are used, the word size is set to 16 bits or less. (the highest bit is ignored).
23 to 16	WDLEN1[7:0] (WDLEN1[3:0] WDLEN3[3:0])	H'00	R/W	Word Count (1 to 256 words) The word counts of groups 1 and 3 are set to WDLEN1 + 1 and WDLEN3 + 1 respectively. When one or two groups are used, the 8-bit value is set to WDLEN1. When three or four groups are used, the upper 4-bit value is set to WDLEN1, and the lower 4-bit value is set to WDLEN3.

Bit	Bit Name	Initial Value	R/W	Descriptions
15, 14	GRPDL1[1:0]	00	R/W	Group 1 Data Transmission Delay These bits specify the number of blank bits to be inserted before transmission of group 1. The value specified with TXDIZ in SICTR is output during transmission. 00: 0-clock-cycle delay 01: 1-clock-cycle delay 10: 2-clock-cycle delay 11: 3-clock-cycle delay
13, 12	GRPDL3[1:0]	00	R/W	Group 3 Data Transmission Delay These bits specify the number of blank bits to be inserted before transmission of group 3. The value specified with TXDIZ in SICTR is output during transmission. 00: 0-clock-cycle delay 01: 1-clock-cycle delay 10: 2-clock-cycle delay 11: 3-clock-cycle delay
11	CRDE4	0	R/W	Control Data Enable "x" in CRDEx represents a group. Each of these bits specifies whether the group transmits FIFO data or control data. 0: The specified group transmits FIFO data. 1: The specified group transmits control data.
10	CRDE3	0	R/W	
9	CRDE2	0	R/W	
8	CRDE1	0	R/W	
7	CRDNUM4	0	R/W	Control Data Transmit Count "x" in CRDNUMx represents a group. Each of these bits specifies the transmission count of control data when multiple words are set for a control data group. Each bit is valid only when the corresponding CRDE bit is 1. When CRDNUMx = 1, control data is transmitted only for the first word, and the value specified with TXDIZ is output for other words. 0: Transmits control data continuously. 1: Transmits control data only once.
6	CRDNUM3	0	R/W	
5	CRDNUM2	0	R/W	
4	CRDNUM1	0	R/W	

Bit	Bit Name	Initial Value	R/W	Descriptions
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

24.3.3 BBIF1 Transmit Mode Register 3 (SITMDR3)

SITMDR3 is a 32-bit readable/writable register that specifies the BBIF1 transmit mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	BITLEN2[4:0]					WDLEN2[7:0]							
Initial value:	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

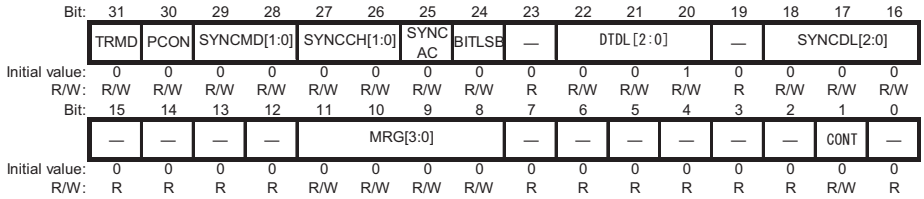
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GRPDL2[1:0]		GRPDL4[1:0]		—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 24	BITLEN2[4:0] (BITLEN4)	01111	R/W	Word Size (8 to 32 bits) The word size is set to the value specified in these bits + 1. When three or four groups are used, the word size is set to 16 bits or less (the highest bit is ignored). Eight bits or a larger size should be specified.
23 to 16	WDLEN2[7:0] (WDLEN2[3:0] WDLEN4[3:0]	H'00	R/W	Word Count (1 to 256 words) The word counts of groups 2 and 4 are set to WDLEN2 + 1 and WDLEN4 + 1 respectively. When one or two groups are used, the 8-bit value is set to WDLEN2. When three or four groups are used, the upper 4-bit value is set to WDLEN2, and the lower 4-bit value is set to WDLEN4.

Bit	Bit Name	Initial Value	R/W	Descriptions
15, 14	GRPDL2[1:0]	00	R/W	Group 2 Data Transmission Delay These bits specify the number of blank bits to be inserted before transmission of group 2. The value specified with TXDIZ in SICTR is output during transmission. 00: 0-clock-cycle delay 01: 1-clock-cycle delay 10: 2-clock-cycle delay 11: 3-clock-cycle delay
13, 12	GRPDL4[1:0]	00	R/W	Group 4 Data Transmission Delay These bits specify the number of blank bits to be inserted before transmission of group 4. The value specified with TXDIZ in SICTR is output during transmission. 00: 0-clock-cycle delay 01: 1-clock-cycle delay 10: 2-clock-cycle delay 11: 3-clock-cycle delay
11 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

24.3.4 BBIF1 Receive Mode Register 1 (SIRMDR1)

SIRMDR1 is a 32-bit readable/writable register that specifies the BBIF1 receive mode.



Bit	Bit Name	Initial Value	R/W	Descriptions
31	TRMD	1	R/W	Transfer Mode Selects the transfer mode. 0: Slave mode 1: Master mode
30	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
29, 28	SYNCMD [1:0]	00	R/W	SYNC Mode These bits specify the mode for the BBIF1_RSYNC signal. 00: Frame start synchronization pulse 01: 1-bit synchronization pulse for last data in slot 10: Level mode/SPI 11: L/R mode
27, 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25	SYNCAC	0	R/W	BBIF1_RSYNC Polarity 0: Active-high signal in synchronization pulse or level mode, or driven high then low in L/R mode 1: Active-low signal in synchronization pulse or level mode, or driven low then high in L/R mode

Bit	Bit Name	Initial Value	R/W	Descriptions
24	BITLSB	0	R/W	MSB/LSB First 0: MSB first 1: LSB first
23	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
22 to 20	DTDL[2:0]	001	R/W	Data Pin Bit Delay for BBIF1_RSYNC Pin B'1xx is valid only in SPI mode. In SPI mode, these bits should be specified so that the sum of the delays specified through the DTDL[2:0] and SYNCDL[2:0] bits becomes an integer value. 000: No bit delay 001: 1-clock-cycle delay 010: 2-clock-cycle delay 101: 0.5-clock-cycle delay 110: 1.5-clock-cycle delay Other than above: Setting prohibited
19	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

18 to 16	SYNCDL [2:0]	000	R/W	BBIF1_RSYNC Timing Delay The synchronization signal is extended for the clock cycles specified in these bits. This setting is invalid when SYNCMD[1:0] = B'01. B'1xx is valid only in SPI mode. In SPI mode, these bits should be specified so that the sum of the delays specified through the DTDL[2:0] and SYNCDL[2:0] bits becomes an integer value. When L/R mode , these bits should always be set to 000. 000: No bit delay 001: 1-clock-cycle delay 010: 2-clock-cycle delay 011: 3-clock-cycle delay 101: 0.5-clock-cycle delay 110: 1.5-clock-cycle delay Other than above: Setting prohibited
15 to 12	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
11 to 8	MRG[3:0]	0000	R/W	Word Merge The data received as 16-bit words of two groups can be merged into one 32-bit word and the 32-bit word is stored in the receive FIFO. The word count in the groups to be merged must be set to 1. In this case, data of groups other than word merging target groups must be handled as control data. This setting is valid only in LR mode. 0000: Not merged 0001: Upper word in group 1 and lower word in group 2 0100: Upper word in group 2 and lower word in group 1 Other than above: Setting prohibited
7 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	CONT	0	R/W	Continuous Frame Reception Specifies continuous reception of multiple frames of data within one frame. This setting is valid when SYNCMD[1:0] = B'00 or B'10. When the RFSE bit in SICTR is set to 0 in master mode, reception is terminated after one-frame data is received. 0: Does not perform continuous reception. 1: Performs continuous reception.
0	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

24.3.5 BBIF1 Receive Mode Register 2 (SIRMDR2)

SIRMDR2 is a 32-bit readable/writable register that specifies the BBIF1 receive mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GRP[1:0]		—	BITLEN1[4:0]					WDLEN1[7:0]							
Initial value:	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GRPDL1[1:0]		GRPDL3[1:0]		CRDE4	CRDE3	CRDE2	CRDE1	CRDNUM4	CRDNUM3	CRDNUM2	CRDNUM1	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31, 30	GRP[1:0]	00	R/W	Group Count The number of groups is set to the value specified in these bits + 1. When three or more groups are specified, the word size (BITLEN) is set to 16 bits or less.

Bit	Bit Name	Initial Value	R/W	Descriptions
29	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
28 to 24	BITLEN1[4:0] (BITLEN3)	01111	R/W	Word Size (8 to 32 bits) The word size (bits) of groups 1 and 3 is set to the value specified in these bits + 1 (BITLEN1 = BITLEN3). Eight bits or a larger size should be specified. When three or four groups are used, the word size is set to 16 bits or less (the highest bit is ignored).
23 to 16	WDLEN1[7:0] (WDLEN1[3:0] WDLEN3[3:0])	H'00	R/W	Word Count (1 to 256 words) The word counts of groups 1 and 3 are set to WDLEN1 + 1 and WDLEN3 + 1 respectively. When one or two groups are used, the 8-bit value is set to WDLEN1. When three or four groups are used, the upper 4-bit value is set to WDLEN1, and the lower 4-bit value is set to WDLEN3.
15, 14	GRPDL1[1:0]	00	R/W	Group 1 Data Reception Delay These bits specify the delay in data reception of group 1. 00: 0-clock-cycle delay 01: 1-clock-cycle delay 10: 2-clock-cycle delay 11: 3-clock-cycle delay
13, 12	GRPDL3[1:0]	00	R/W	Group 3 Data Reception Delay These bits specify the delay in data reception of group 3. 00: 0-clock-cycle delay 01: 1-clock-cycle delay 10: 2-clock-cycle delay 11: 3-clock-cycle delay

Bit	Bit Name	Initial Value	R/W	Descriptions
11	CRDE4	0	R/W	Control Data Enable
10	CRDE3	0	R/W	“x” in CRDEx represents a group. Each of these bits specifies whether the group receives FIFO data or control data.
9	CRDE2	0	R/W	
8	CRDE1	0	R/W	0: The specified group receives FIFO data.
				1: The specified group receives control data.
7	CRDNUM4	0	R/W	Control Data Reception Count
6	CRDNUM3	0	R/W	“x” in CRDNUMx represents a group. Each of these bits specifies the reception count of control data when multiple words are set for a control data group. When CRDNUMx = 1, only the first word is received as control data, and the other words are discarded as invalid data.
5	CRDNUM2	0	R/W	
4	CRDNUM1	0	R/W	0: Receives control data continuously.
				1: Receives only one word of control data.
3 to 0	—	All 0	R	Reserved
				These bits are always read as 0. The write value should always be 0.

24.3.6 BBIF1 Receive Mode Register 3 (SIRMDR3)

SIRMDR3 is a 32-bit readable/writable register that specifies the BBIF1 receive mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	BITLEN2[4:0]					WDLEN2[7:0]							
Initial value:	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GRPDL2[1:0]		GRPDL4[1:0]		—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 24	BITLEN2[4:0] (BITLEN4)	01111	R/W	Word Size (8 to 32 bits) The word size is set to the value specified in these bits + 1. When three or four groups are used, the word size is set to 16 bits or less (the highest bit is ignored). These bits should be set to eight bits or more.
23 to 16	WDLEN2[7:0] (WDLEN4)	H'00	R/W	Word Count (1 to 256 words) The word counts of groups 2 and 4 are set to WDLEN2 + 1 and WDLEN4 + 1 respectively. When one or two groups are used, the 8-bit value is set to WDLEN2. When three or four groups are used, the upper 4-bit value is set to WDLEN2, and the lower 4-bit value is set to WDLEN4.
15, 14	GRPDL2[1:0]	00	R/W	Group 2 Data Reception Delay These bits specify the delay in data reception of group 2. 00: 0-clock-cycle delay 01: 1-clock-cycle delay 10: 2-clock-cycle delay 11: 3-clock-cycle delay
13, 12	GRPDL4[1:0]	00	R/W	Group 4 Data Reception Delay These bits specify the delay in data reception of group 4. 00: 0-clock-cycle delay 01: 1-clock-cycle delay 10: 2-clock-cycle delay 11: 3-clock-cycle delay
11 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

24.3.7 BBIF1 Control Register (SICTR)

SICTR is a 32-bit readable/writable register that specifies the BBIF1 operating state.

The values written to the TXE, RXE, TFSE, RFSE, TSCKE, and RSCKE bits become valid (can be read from the bits) several cycles after writing. These bits should not be modified together; modify one bit at a time, check that the new value can be read from the bit, and then modify another bit.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TSCKIZ[1:0]		RSCKIZ[1:0]		TEDG	REDG	—	—	TXDIZ[1:0]		—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TSCKE	TFSE	—	—	—	—	TXE	RXE	—	—	—	—	—	—	TXRST	RXRST
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R	R	R	R/W	R/W	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31, 30	TSCKIZ[1:0]	00	R/W	Transmit Clock Output Polarity Select in SPI Mode When Transmission is Invalid When SPI mode is not used, these bits should always be set to 00. 00: Outputs BBIF1_TSCK when transmission is invalid. 01: Setting prohibited 10: Outputs 0. 11: Outputs 1.

Bit	Bit Name	Initial Value	R/W	Descriptions
29, 28	RSCKIZ[1:0]	00	R/W	Receive Clock Input Polarity Select in SPI Mode In SPI mode, set these bits to the TSCKIZ value. 00: Inputs BBIF1_RSCK when transmission is invalid 01: Setting prohibited 10: Inputs 0 through BBIF1_RSCK when transmission is invalid. 11: Inputs 1 through BBIF1_RSCK when transmission is invalid.
27	TEDG	0	R/W	Transmit Timing 0: Outputs transmit data at the rising edge of the clock. 1: Outputs transmit data at the falling edge of the clock.
26	REDG	0	R/W	Receive Timing 0: Samples receive data at the falling edge of the clock. 1: Samples receive data at the rising edge of the clock.
25, 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23, 22	TXDIZ[1:0]	00	R/W	Pin Output When Transmission is Invalid These bits specify the BBIF1_TXD pin output state when transmission is invalid. 00: Outputs 0. 01: Outputs 1. 10: Setting prohibited 11: Setting prohibited
21 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
15	TSCKE	0	R/W	Transmit Serial Clock Output Enable This bit is valid in master mode. When this bit is set to 1, the BBIF1 initializes the baud rate generator and initiates the operation. At the same time, the BBIF1 outputs the clock generated by the baud rate generator to the BBIF1_TSCK pin. After the clock is output, 1 can be read. When transmitting data, set this bit to 1 before setting the TFSE and TXE bits. After data transmission, clear the TFSE and TXE bits and then clear this bit to 0. [Write data] 0: Disables the BBIF1_TSCK output. (Outputs the value specified with TSCKIZ.) 1: Enables the BBIF1_TSCK output. [Read data] 0: Does not output BBIF1_TSCK. (Outputs the value specified with TSCKIZ.) 1: Outputs BBIF1_TSCK.
14	TFSE	0	R/W	Transmit Frame Synchronization Signal Output Enable This bit is valid in master mode. When this bit is set to 1, the BBIF1 initializes the frame counter and initiates the operation. After the transmit frame synchronization signal is output, 1 can be read. When 0 is written to this bit, 0 is set after transmission of the frame. [Write data] 0: Disables the BBIF1_TSYNC output. (Outputs the value specified with SYNCAC.) 1: Enables the BBIF1_TSYNC output. [Read data] 0: Does not output BBIF1_TSYNC. (Outputs the value specified with SYNCAC.) 1: Outputs BBIF1_TSYNC.

Bit	Bit Name	Initial Value	R/W	Descriptions
13 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	TXE	0	R/W	Transmit Enable When this bit is set to 1, the BBIF1 starts data transmission from the beginning of the next frame (at the rising edge of the frame synchronization signal). When value 1 set to this bit becomes valid, the BBIF1 issues a transmit data transfer request according to the setting of the TFWM bits in SIFCTR. When transmit data is stored in the transmit FIFO, transmission of data from the BBIF1_TXD pin begins. When 0 is written to this bit, 0 is set after transmission of the frame. This bit is initialized upon a transmit reset. [Write data] 0: Disables the BBIF1_TXD output. (Outputs the value specified with TXDIZ.) 1: Enables the BBIF1_TXD output. [Read data] 0: Does not output BBIF1_TXD. (Outputs the value specified with TXDIZ.) 1: Outputs BBIF1_TXD.

Bit	Bit Name	Initial Value	R/W	Descriptions
8	RXE	0	R/W	Receive Enable When this bit is set to 1, the BBIF1 starts data reception from the beginning of the next frame (at the rising edge of the frame synchronization signal). When value 1 set to this bit becomes valid, the BBIF1 begins reception of data through the BBIF1_RXD pin. When receive data is stored in the receive FIFO, the BBIF1 issues a receive data transfer request according to the setting of the RFWM bits in SIFCTR. This bit is initialized upon a receive reset. [Write data] 0: Disables data reception through BBIF1_RXD. 1: Enables data reception through BBIF1_RXD. [Read data] 0: Data is not received through BBIF1_RXD. 1: Data can be received through BBIF1_RXD.
7 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
1	TXRST	0	R/W	Transmit Reset When value 1 set to this bit becomes valid, the BBIF1 immediately sets transmit data through the BBIF1_TXD pin to 0, and initializes the transmit data registers and transmit-related status. The following registers and bits are initialized. • SITDR1 and SITDR2 • SITFDR • Transmit FIFO write pointer • TCRDY, TFEMP, and TDREQ bits in SISTR • TXE bit This bit is read as 1 until the reset operation is completed for about 20 cycles. No data should be written to SICTR or the transmit FIFO during this time period. [Write data] 0: Does not reset transmit operation. 1: Resets transmit operation. [Read data] 0: Transmit operation reset is completed. 1: Transmit operation is being reset.

Bit	Bit Name	Initial Value	R/W	Descriptions
0	RXRST	0	R/W	Receive Reset When value 1 set to this bit becomes valid, the BBIF1 immediately disables reception through the BBIF1_RXD pin, and initializes the receive data registers and receive-related status. The following registers and bits are initialized. • SIRDR1 and SIRDR2 • SIRFDR • Receive FIFO read pointer • RCRDY, RFFUL, and RDREQ bits in SISTR • RXE bit This bit is read as 1 until the reset operation is completed for about 20 cycles. No data should be written to SICTR or read the receive FIFO during this time period. [Write data] 0: Does not reset receive operation. 1: Resets receive operation. [Read data] 0: Receive operation reset is completed. 1: Receive operation is being reset.

24.3.8 BBIF1 Transmit Clock Select Register (SITSCR)

SITSCR is a 16-bit readable/writable register that specifies the conditions for generating the transmit serial clock in master mode. SITSCR can be specified when the TRMD bit in SITMDR1 is set to B'1.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSSEL[1:0]		MSIMM	BRPS[4:0]					—	—	—	—	—	BRDV[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
15, 14	MSSEL[1:0]	00	R/W	Master Clock Source Select The master clock is the clock input to the baud rate generator. 00: Selects SUBϕ as the master clock. Other than above: Setting prohibited
13	MSIMM	0	R/W	Master Clock Direct Select 0: Selects the clock output from the baud rate generator as the serial clock. 1: Selects the master clock itself as the serial clock.
12 to 8	BRPS[4:0]	00000	R/W	Prescalar Setting These bits specify the master clock division ratio in the count value of the prescalar in the baud rate generator. The specifiable value is from B'00000 ($\times$ 1/1) to B'11111 ($\times$ 1/32).
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
2 to 0	BRDV[2:0]	000	R/W	Baud Rate Generator's Division Ratio These bits specify the frequency division ratio for the output stage of the baud rate generator. The final frequency division ratio of the baud rate generator is determined as BRPS × BRDV (1/1024 max.). 000: Prescalar output × 1/2 001: Prescalar output × 1/4 010: Prescalar output × 1/8 011: Prescalar output × 1/16 100: Prescalar output × 1/32 101: Setting prohibited 110: Setting prohibited 111: Prescalar output × 1/1 Note: B'111 is valid only when the BRPS[4:0] bits are set to B'00000 or B'00001.

24.3.9 BBIF1 Transmit Control Data Register 1 (SITDR1)

SITDR1 is a 32-bit write-only register that specifies the transmit control data of the BBIF1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TCRD1[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TCRD2[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 16	TCRD1[15:0]	H'0000	W	• When one or two groups are used: These bits specify the transmit control data for the upper 16 bits of a word in group 1 • When three or four groups are used: These bits specify the transmit control data for a word in group 1.
15 to 0	TCRD2[15:0]	H'0000	W	• When one or two groups are used: These bits specify the transmit control data for the lower 16 bits of a word in group 1 when the word size is larger than 16 bits. • When three or four groups are used: These bits specify the transmit control data for a word in group 3.

24.3.10 BBIF1 Transmit Control Data Register 2 (SITDR2)

SITDR2 is a 32-bit write-only register that specifies the transmit control data of the BBIF1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TCRD3[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TCRD4[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 16	TCRD3[15:0]	H'0000	W	• When one or two groups are used: These bits specify the transmit control data for the upper 16 bits of a word in group 2. • When three or four groups are used: These bits specify the transmit control data for a word in group 2.
15 to 0	TCRD4[15:0]	H'0000	W	• When one or two groups are used: These bits specify the transmit control data for the lower 16 bits of a word in group 2 when the word size is larger than 16 bits. • When three or four groups are used: These bits specify the transmit control data for a word in group 4.

24.3.11 BBIF1 Transmit FIFO Data Register (SITFDR)

SITFDR is a 32-bit write-only register that specifies the transmit FIFO data of the BBIF1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SITFD1[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SITFD2[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 16	SITFD1[15:0]	H'0000	W	These bits specify the upper 16 bits of the FIFO data to be output through BBIF1_TXD.
15 to 0	SITFD2[15:0]	H'0000	W	These bits specify the lower 16 bits of the FIFO data to be output through BBIF1_TXD.

24.3.12 BBIF1 Receive Control Data Register 1 (SIRDR1)

SIRDR1 is a 32-bit read-only register that stores the receive control data of the BBIF1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RCRD1[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RCRD2[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 16	RCRD1[15:0]	H'0000	R	• When one or two groups are used: Store the receive control data for the upper 16 bits of a word in group 1 • When three or four groups are used: Store the receive control data for a word in group 1.
15 to 0	RCRD2[15:0]	H'0000	R	• When one or two groups are used: Store the receive control data for the lower 16 bits of a word in group 1 when the word size is larger than 16 bits. • When three or four groups are used: Store the receive control data for a word in group 3.

24.3.13 BBIF1 Receive Control Data Register 2 (SIRDR2)

SIRDR2 is a 32-bit read-only register that stores the receive control data of the BBIF1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RCRD3[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RCRD4[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 16	RCRD3[15:0]	H'0000	R	• When one or two groups are used: Store the receive control data for the upper 16 bits of a word in group 2 • When three or four groups are used: Store the receive control data for a word in group 2.
15 to 0	RCRD4[15:0]	H'0000	R	• When one or two groups are used: Store the receive control data for the lower 16 bits of a word in group 2 when the word size is larger than 16 bits. • When three or four groups are used: Store the receive control data for a word in group 4.

24.3.14 BBIF1 Receive FIFO Data Register (SIRFDR)

SIRFDR is a 32-bit read-only register that stores the receive FIFO data of the BBIF1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SIRFD1[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SIRFD2[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 16	SIRFD1[15:0]	Undefined	R	Store the upper 16 bits of the FIFO data received through BBIF1_RXD.
15 to 0	SIRFD2[15:0]	Undefined	R	Store the lower 16 bits of the FIFO data received through BBIF1_RXD.

24.3.15 BBIF1 Status Register (SISTR)

Each bit in SISTR becomes a BBIF1 interrupt source when the corresponding bit in SIIER is set to 1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	TCRDY	TFEMP	TDREQ	—	—	—	—	TEOF	—	TFSERR	TFOVF	TFUDF	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R	R	R	R	R	R/W	R	R/W	R/W	R/W	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	RCRDY	RFFUL	RDREQ	—	—	—	—	REOF	—	RFSERR	RFUDF	RFOVF	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R	R	R	R	R	R/W	R	R/W	R/W	R/W	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
30	TCRDY	0	R/W	Transmit Control Data Ready If SITDR1 or SITDR2 is written while this bit is cleared to 0, SICTR is overwritten and the previous contents are not output through the BBIF1_TXD pin. This bit is valid when the TXE bit in SICTR is 1. If the interrupt request from this bit is enabled, a BBIF1 interrupt is issued. 0: SITDR1 and SITDR2 are not ready to be written. 1: SITDR1 and SITDR2 are ready to be written.

Bit	Bit Name	Initial Value	R/W	Descriptions
29	TFEMP	0	R/W	Transmit FIFO Empty This bit is valid when the TXE bit in SICTR is 1. When this bit is set to 1, the content is cleared. Writing 0 to this bit is invalid. If the interrupt request from this bit is enabled, a BBIF1 interrupt is issued. 0: Transmit FIFO is not empty. 1: Transmit FIFO is empty.
28	TDREQ	0	R	Transmit Data Transfer Request A transmit data transfer request is issued when the empty space in the transmit FIFO exceeds the size specified by the TFWM bits in SIFCTR. When transferring transmit data through the DMAC, this bit is always cleared after one DMAC access. After DMAC access, when the conditions for setting this bit are satisfied, the BBIF1 again sets this bit to 1. This bit is valid when the TXE bit in SICTR is 1. This bit indicates a state; if the size of empty space in the transmit FIFO becomes less than the size specified by the TFWM bits in SIFCTR, the BBIF1 clears this bit. If the interrupt request from this bit is enabled, a BBIF1 interrupt is issued. However, when the TDMAE bit is 1, only a DMAC transfer request is issued. 0: The size of empty space in the transmit FIFO has not exceeded the size specified by the TFWM bits in SIFCTR. 1: The size of empty space in the transmit FIFO has exceeded the size specified by the TFWM bits in SIFCTR.
27 to 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
23	TEOF	0	R/W	Frame Transmission End The BBIF1 issues the frame transmission end flag upon completion of one-frame data transmission. This bit is valid when the TXE bit in SICTR is 1. When this bit is set to 1, the content is cleared. Writing 0 to this bit is invalid. If the interrupt request from this bit is enabled, a BBIF1 interrupt is issued. 0: One-frame transmission end is not detected. 1: One-frame transmission end is detected.
22	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
21	TFSERR	0	R/W	Transmit Frame Synchronization Error A transmit frame synchronization error occurs when the next transmit frame synchronization timing arrives before the previous data or control data transmission has been completed. If a transmit frame synchronization error occurs, the BBIF1 performs transmission only for the slots that can be transferred. This bit is valid when the TXE bit in SICTR is 1. When 1 is written to this bit, it is cleared. Writing 0 to this bit is invalid. If the interrupt request from this bit is enabled, a BBIF1 interrupt is issued. 0: No transmit frame synchronization error has occurred. 1: A transmit frame synchronization error has occurred.

Bit	Bit Name	Initial Value	R/W	Descriptions
20	TFOVF	0	R/W	Transmit FIFO Overflow A transmit FIFO overflow means that there has been an attempt to write to SITFDR when the transmit FIFO is full. If a transmit FIFO overflow occurs, the BBIF1 ignores the write operation causing the overflow. This bit is valid when the TXE bit in SICTR is 1. When 1 is written to this bit, it is cleared. Writing 0 to this bit is invalid. If the interrupt request from this bit is enabled, a BBIF1 interrupt is issued. 0: No transmit FIFO overflow has occurred. 1: A transmit FIFO overflow has occurred.
19	TFUDF	0	R/W	Transmit FIFO Underflow A transmit FIFO underflow means that loading for transmission has occurred when the transmit FIFO is empty. This bit is valid when the TXE bit in SICTR is 1. When 1 is written to this bit, it is cleared. Writing 0 to this bit is invalid. If the interrupt request from this bit is enabled, a BBIF1 interrupt is issued. 0: No transmit FIFO underflow has occurred. 1: A transmit FIFO underflow has occurred.
18 to 15	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
14	RCRDY	0	R/W	Receive Control Data Ready When data different from the previous data is stored during reception of control data, this bit is set to 1 indicating that valid data was written. When the first data that is not 0 is stored, this bit is set to 1. If valid data is written to SIRDR1 or SIRDR2 when this bit is set to 1, SIRDR1 or SIRDR2 is overwritten with the latest data. This bit is valid when the RXE bit in SICTR is 1. If the interrupt request from this bit is enabled, a BBIF1 interrupt is issued. 0: SIRDR1 and SIRDR2 store no valid data. 1: SIRDR1 and SIRDR2 store valid data.
13	RFFUL	0	R/W	Receive FIFO Full This bit is valid when the RXE bit in SICTR is 1. When this bit is set to 1, the content is cleared. Writing 0 to this bit is invalid. If the interrupt request from this bit is enabled, a BBIF1 interrupt is issued. 0: Receive FIFO is not full. 1: Receive FIFO is full.

Bit	Bit Name	Initial Value	R/W	Descriptions
12	RDREQ	0	R	Receive Data Transfer Request A receive data transfer request is issued when the valid data space in the receive FIFO exceeds the size specified by the RFWM bits in SIFCTR. When transferring transmit data through the DMAC, this bit is always cleared by one DMAC access. After DMAC access, when the conditions for setting this bit are satisfied, the BBIF1 again sets this bit to 1. This bit is valid when the RXE bit in SICTR is 1. This bit indicates a state; if the size of valid data space in the receive FIFO becomes less than the size specified by the RFWM bits in SIFCTR, the BBIF1 clears this bit. If the interrupt request from this bit is enabled, a BBIF1 interrupt is issued. However, when the RDMAE bit is 1, only a DMAC transfer request is issued. 0: The size of valid data space in the receive FIFO has not exceeded the size specified by the RFWM bits in SIFCTR. 1: The size of valid data space in the receive FIFO has exceeded the size specified by the RFWM bits in SIFCTR.
11 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
7	REOF	0	R/W	Frame Reception End The BBIF1 issues the frame reception end flag upon completion of one-frame data reception. This bit is valid when the RXE bit in SICTR is 1. When this bit is set to 1, the content is cleared. Writing 0 to this bit is invalid. If the interrupt request from this bit is enabled, a BBIF1 interrupt is issued. 0: One-frame reception end is not detected. 1: One-frame reception end is detected.
6	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
5	RFSERR	0	R/W	Receive Frame Synchronization Error A receive frame synchronization error occurs when the next receive frame synchronization timing arrives before the previous data or control data reception has been completed. If a receive frame synchronization error occurs, the BBIF1 performs reception only for the slots that can be transferred. This bit is valid when the RXE bit in SICTR is 1. When 1 is written to this bit, it is cleared. Writing 0 to this bit is invalid. If the interrupt request from this bit is enabled, a BBIF1 interrupt is issued. 0: No receive frame synchronization error has occurred. 1: A receive frame synchronization error has occurred.

Bit	Bit Name	Initial Value	R/W	Descriptions
4	RFUDF	0	R/W	Receive FIFO Underflow A receive FIFO underflow means that reading of SIRFDR has occurred when the receive FIFO is empty. If a receive FIFO underflow occurs, the value read from SIRFDR is not guaranteed. This bit is valid when the RXE bit in SICTR is 1. When 1 is written to this bit, it is cleared. Writing 0 to this bit is invalid. If the interrupt request from this bit is enabled, a BBIF1 interrupt is issued. 0: No receive FIFO underflow has occurred. 1: A receive FIFO underflow has occurred.
3	RFOVF	0	R/W	Receive FIFO Overflow A receive FIFO overflow means that writing has been caused by receiving operation when the receive FIFO is full. If a receive FIFO overflow occurs, the receive data causing the overflow is lost. This bit is valid when the RXE bit in SICTR is 1. When 1 is written to this bit, it is cleared. Writing 0 to this bit is invalid. If the interrupt request from this bit is enabled, a BBIF1 interrupt is issued. 0: No receive FIFO overflow has occurred. 1: A receive FIFO overflow has occurred.
2 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

24.3.16 BBIF1 Interrupt Enable Register (SIIER)

SIIER is a 32-bit readable/writable register that enables the issue of BBIF1 interrupts. When each bit in this register is set to 1 and the corresponding bit in SISTR is set to 1, the BBIF1 issues an interrupt.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TDMAE	TCRDYE	TFEMPE	TDREQE	—	—	—	—	TEOFE	—	TFSERRE	TFOVFE	TFUDFE	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R	R/W	R/W	R/W	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RDMAE	RCRDYE	RFFULE	RDREQE	—	—	—	—	REOFE	—	RFSERRE	RFUDFE	RFOVFE	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R	R/W	R/W	R/W	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31	TDMAE	0	R/W	Transmit Data DMA Transfer Request Enable Specifies whether to send an interrupt as an interrupt request to the CPU or a transfer request to the DMAC. The TDREQE bit can be set as the request source. 0: Sends an interrupt request to the CPU. 1: Sends a DMA transfer request to the DMAC.
30	TCRDYE	0	R/W	Transmit Control Data Ready Enable 0: Disables interrupts due to transmit control data ready. 1: Enables interrupts due to transmit control data ready.
29	TFEMPE	0	R/W	Transmit FIFO Empty Enable 0: Disables interrupts due to transmit FIFO empty 1: Enables interrupts due to transmit FIFO empty
28	TDREQE	0	R/W	Transmit Data Transfer Request Enable 0: Disables interrupts due to transmit data transfer requests. 1: Enables interrupts due to transmit data transfer requests.

Bit	Bit Name	Initial Value	R/W	Descriptions
27 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23	TEOFE	0	R/W	Frame Transmission End Enable 0: Disables a frame transmission end interrupt. 1: Enables a frame transmission end interrupt.
22	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
21	TFSERRE	0	R/W	Transmit Frame Synchronization Error Enable 0: Disables interrupts due to transmit frame synchronization errors. 1: Enables interrupts due to transmit frame synchronization errors.
20	TFOVFE	0	R/W	Transmit FIFO Overflow Enable 0: Disables interrupts due to transmit FIFO overflow. 1: Enables interrupts due to transmit FIFO overflow.
19	TFUDFE	0	R/W	Transmit FIFO Underflow Enable 0: Disables interrupts due to transmit FIFO underflow. 1: Enables interrupts due to transmit FIFO underflow.
18 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	RDMAE	0	R/W	Receive Data DMA Transfer Request Enable Specifies whether to send an interrupt as an interrupt request to the CPU or a transfer request to the DMAC. The RDREQE bit can be set as the request source. 0: Sends an interrupt request to the CPU. 1: Sends a DMA transfer request to the DMAC.

Bit	Bit Name	Initial Value	R/W	Descriptions
14	RCRDYE	0	R/W	Receive Control Data Ready Enable 0: Disables interrupts due to receive control data ready. 1: Enables interrupts due to receive control data ready.
13	RFFULE	0	R/W	Receive FIFO Full Enable 0: Disables interrupts due to receive FIFO full. 1: Enables interrupts due to receive FIFO full.
12	RDREQE	0	R/W	Receive Data Transfer Request Enable 0: Disables interrupts due to receive data transfer requests. 1: Enables interrupts due to receive data transfer requests.
11 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	REOFE	0	R/W	Frame Reception End Enable 0: Disables a frame reception end interrupt. 1: Enables a frame reception end interrupt.
6	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
5	RFSERRE	0	R/W	Receive Frame Synchronization Error Enable 0: Disables interrupts due to receive frame synchronization errors. 1: Enables interrupts due to receive frame synchronization errors.
4	RFUDFE	0	R/W	Receive FIFO Underflow Enable 0: Disables interrupts due to receive FIFO underflow. 1: Enables interrupts due to receive FIFO underflow.

Bit	Bit Name	Initial Value	R/W	Descriptions
3	RFOVFE	0	R/W	Receive FIFO Overflow Enable 0: Disables interrupts due to receive FIFO overflow. 1: Enables interrupts due to receive FIFO overflow.
2 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

24.3.17 BBIF1 FIFO Control Register (SIFCTR)

SIFCTR is a 32-bit readable/writable register that indicates the area available for the transmit/receive FIFO transfer.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TFWM[2:0]			—	—	TFUA[6:0]							—	—	—	—
Initial value:	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RFWM[2:0]			RFUA[8:0]									—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 29	TFWM[2:0]	000	R/W	Transmit FIFO Watermark A transfer request of the transmit FIFO is issued by the TDREQE bit in SIIER. The transmit FIFO always operates as a 64-stage FIFO regardless of these bit settings. 000: Issues a transfer request when 64 stages of the transmit FIFO are empty. 001: Issues a transfer request when 32 or more stages of the transmit FIFO are empty. 010: Issues a transfer request when 24 or more stages of the transmit FIFO are empty. 011: Issues a transfer request when 16 or more stages of the transmit FIFO are empty. 100: Issues a transfer request when 12 or more stages of the transmit FIFO are empty. 101: Issues a transfer request when 8 or more stages of the transmit FIFO are empty. 110: Issues a transfer request when 4 or more stages of the transmit FIFO are empty. 111: Issues a transfer request when 1 or more stages of transmit FIFO are empty.

Bit	Bit Name	Initial Value	R/W	Descriptions
28, 27	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
26 to 20	TFUA[6:0]	H'40	R	Transmit FIFO Usable Area Indicate the number of words that can be transferred by the CPU or DMAC as B'0000000 (full) to B'1000000 (empty).
19 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 13	RFWM[2:0]	000	R/W	Receive FIFO Watermark A transfer request of the receive FIFO is issued by the RDREQE bit in SIIER. The receive FIFO always operates as a 256-stage FIFO regardless of these bit settings. 000: Issues a transfer request when 1 stage or more of the receive FIFO are valid. 001: Issues a transfer request when 4 or more stages of the receive FIFO are valid. 010: Issues a transfer request when 8 or more stages of the receive FIFO are valid. 011: Issues a transfer request when 16 or more stages of the receive FIFO are valid. 100: Issues a transfer request when 32 or more stages of the receive FIFO are valid. 101: Issues a transfer request when 64 or more stages of the receive FIFO are valid. 110: Issues a transfer request when 128 or more stages of the receive FIFO are valid. 111: Issues a transfer request when 256 stages of the receive FIFO are valid.
12 to 4	RFUA[8:0]	H'000	R	Receive FIFO Usable Area Indicate the number of words that can be transferred by the CPU or DMAC as B'000000000 (empty) to B'100000000 (full).

Bit	Bit Name	Initial Value	R/W	Descriptions
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

24.3.18 BBIF1 Flow Control Register (SIFLCTR)

SIFLCTR is a 32-bit readable/writable register that controls the output of the flow control pin.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	APFLE	APFLMASK	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	BBFLE	BBFLMASK	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31	APFLE	0	R/W	AP-Flow Control Pin Forcible Output 0: Does not forcibly assert the flow control pin. (Outputs the DINT signal.) 1: Forcibly asserts the flow control pin.
30	APFLMASK	0	R/W	AP-Flow Control Pin Output Mask 0: Does not mask the flow control pin output. 1: Masks the flow control pin output. Setting this bit to 1 takes precedence over the APFLE bit.
29 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	BBFLE	0	R/W	BB-Flow Control Pin Forcible Input 0: Does not forcibly assert the flow control pin. (Inputs the BB_RX_FLOW signal.) 1: Forcibly asserts the flow control pin.
14	BBFLMASK	0	R/W	BB-Flow Control Pin Input Mask 0: Does not mask the flow control pin input. 1: Masks the flow control pin output. Setting this bit to 1 takes precedence over the BBFLE bit.
13 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

24.4 Operation

24.4.1 Operating Mode

(1) Independent Transmit/Receive Mode

Dedicated clock and frame synchronization signals can be specified each for transmission and reception.

Master mode: BBIF1_TSCK and BBIF1_TSYNC (BBIF1_RSCK and BBIF1_RSYNC) are output.

Slave mode: BBIF1_TSCK and BBIF1_TSYNC (BBIF1_RSCK and BBIF1_RSYNC) are input.

(2) Common Transmit/Receive Mode

Common clock and frame synchronization signals are used for transmission and reception.

Master mode: BBIF1_TSCK (BBIF1_SCK) and BBIF1_TSYNC (BBIF1_SYNC) are output.

Slave mode: BBIFTSCK (BBIF1_SCK) and BBIF1_TSYNC (BBIF1_SYNC) are input.

24.4.2 Serial Clocks

(1) Clock Output in Master Mode

In master mode, the baud rate generator is used to generate the serial clock. The division ratio is from 1/1 to 1/1024.

(2) Clock Input in Slave Mode

In slave mode, the clock input for transmission and reception is used as the serial clock.

(3) Multiple Channel Function

This module provides the multiple channel function as shown in Figure 24.2.

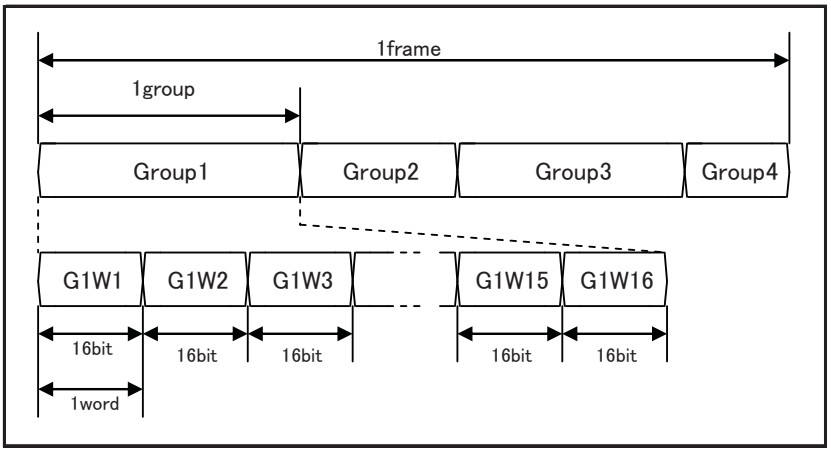


Figure 24.2 Multiple Channel Structure

The following conditions can be specified for the multiple channel function.

- Up to four groups in one frame
- Up to 256 words in one group
- Eight bits to 32 bits in one word
- Up to three blank bits can be inserted between groups

Note the following limitations by the number of groups.

Table 24.4 Maximum Word Size and Group Size Limited by Number of Groups

Number of Groups	Maximum Word Size	Maximum Group Size
One or two	32 bits	256 words
Three or four	16 bits	16 words

24.4.3 Serial Timing

(1) BBIF1_TSYNC, BBIF1_RSYNC

The BBIF1_TSYNC and BBIF1_RSYNC are frame synchronization signals. The following four modes are available.

- Frame start synchronization pulse: 1-bit-width pulse indicating the start of a frame
- Last bit synchronization pulse: 1-bit-width pulse indicating the last bit in a word
- Level/SPI: Level signal asserted during frame transmission
- L/R: 1/2-frame-width pulse indicating the first-half groups in a high level and the last-half groups in a low level

Figure 24.3 to 24.6 show the BBIF1_SYNC synchronization timing in these modes.

(2) Frame Start Synchronization Pulse

The rising edge of the synchronization pulse indicates the start of a frame.

The delay between the rising edge of the synchronization signal and the start of data transmission or reception can be specified with the DTDL bits. The width of the synchronization pulse can be extended through the SYNCDL bit setting.

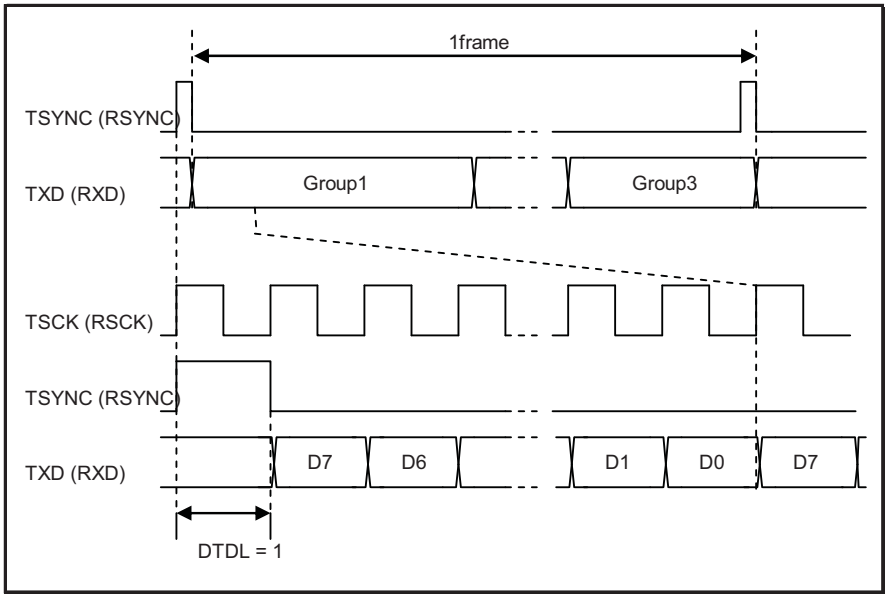


Figure 24.3 Synchronization Timing in Start Frame Synchronization Pulse Mode

(3) Last Bit Synchronization Pulse

The rising edge of the synchronization pulse indicates the last bit of each word.

The delay between the last bit of a word and the synchronization pulse can be specified with the DTDL bits.

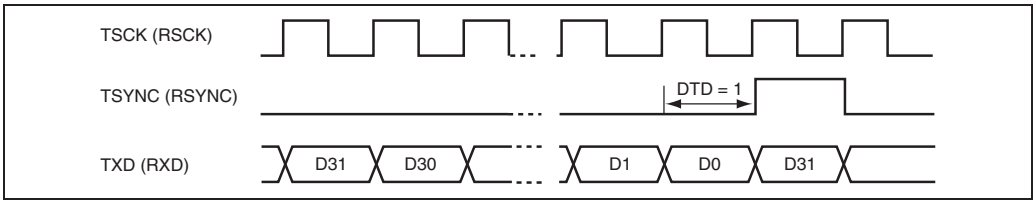


Figure 24.4 Synchronization Timing in Last Bit Synchronization Pulse Mode

(4) Level Synchronization

The synchronization signal is driven high for the frame length.

The delay between the rising edge of the synchronization signal and the start of transmission or reception can be specified with the DTDL bits and the delay between the end of transmission or reception and the falling edge of the synchronization signal can be specified with the SYNCDL bits (DTDL = 0 to 2 and SYNCDL = 0 to 3). This mode is available for the SPI master or slave operation.

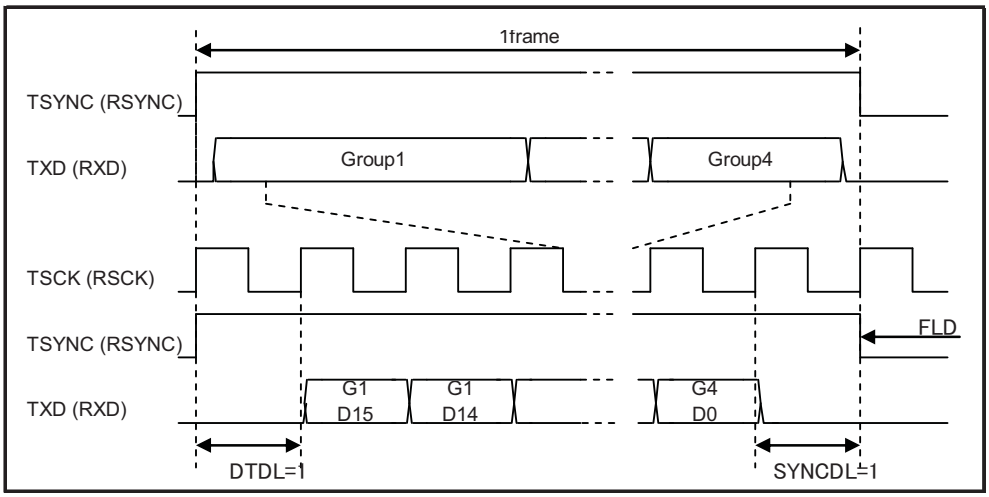


Figure 24.5 Synchronization Timing in Level Synchronization Mode

(5) L/R Synchronization

A high level in the synchronization signal indicates the first-half groups and a low level indicates the last-half groups.

The delay between the rising or falling edge of the synchronization signal and the start of transmission or reception can be specified with the DTDL bits and the delay between the end of transmission or reception and the falling or rising edge of the synchronization signal can be specified with the SYNCDL bits (DTDL = 0 to 2 and SYNCDL = 0 to 3).

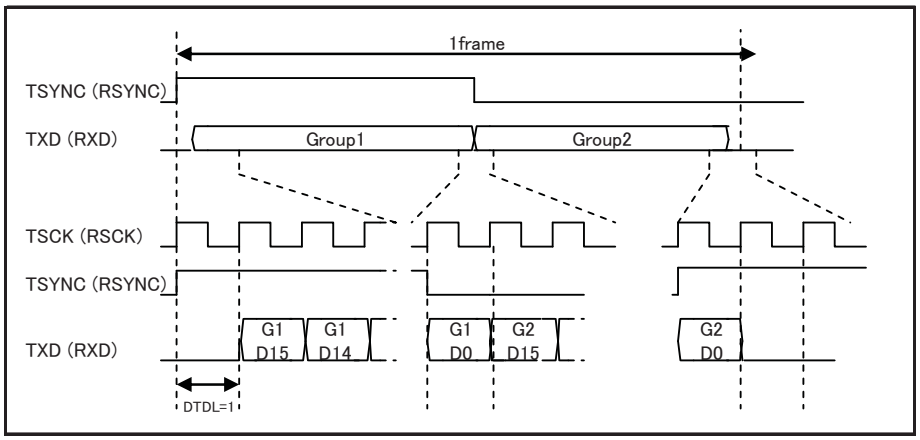


Figure 24.6 Synchronization Timing in L/R Synchronization Mode

(6) Transmit/Receive Timing

The BBIF1_TXD transmit timing and BBIF1_RXD receive timing relative to the BBIF1_TSCK and BBIF1_RSCK can be specified as the sampling timing in the following two ways through the TEDG and REDG bits in SIMDR.

- Falling-edge sampling
- Rising-edge sampling

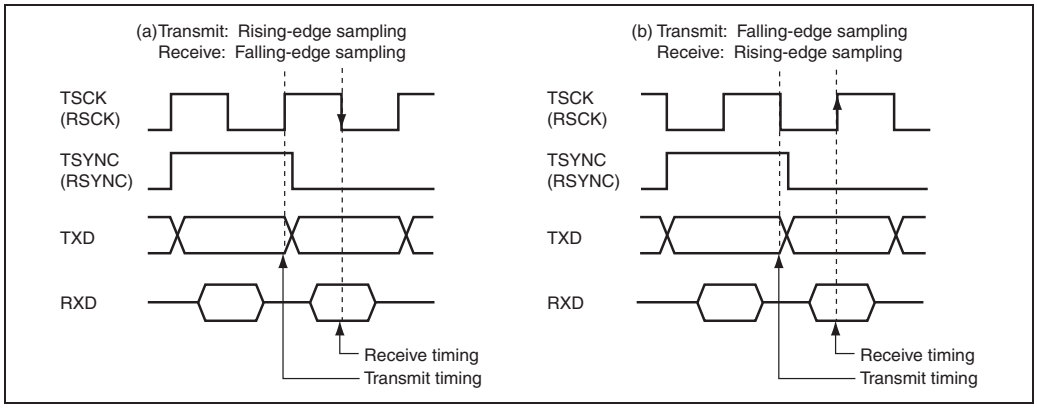


Figure 24.7 Transmit/Receive Timing.

24.4.4 Control Data Interface

For the groups specified with the CRDE bits in SITMDR2 and SIRMDR2, data is not stored in the FIFOs but handled as control data to be stored in SITDR1/SITDR2 and SIRDR1/SIRDR2.

Control data is transferred in the following two ways, which can be selected through the CRDNUM bits in SITMDR2 and SIRMDR2, as shown in figure 22.8.

- Only the first word in the group is transferred as valid data.
- All words in the group is transferred as valid data.

For the invalid data period during transmission, the value specified in the TXDIZ bit is output. The invalid receive data is not stored in SIRDR1 or SIRDR2.

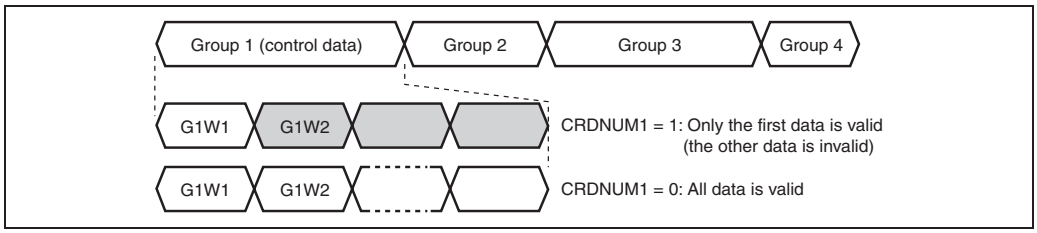


Figure 24.8 Control Data Allocation

24.4.5 Transfer Data Allocation to Registers

(1) Transmit/Receive Data

Transmit/receive data (FIFO data and control data) should be written to or read from the following registers.

- Transmit FIFO data writing: SITFDR (32/16-bit access)
- Control data writing: SITDR1 and SITDR2 (32/16-bit access)
- Receive FIFO data reading: SIRFDR (32/16-bit access)
- Control data reading: SIRDR1 and SIRDR2 (32/16-bit access)

When making a 16-bit access, only upper 16 bits of FIFO data is accessible. However, both upper 16 bits and lower 16 bits of control data are accessible.

When the word size is smaller than the transmit FIFO data access size, the upper bits are transmitted as valid data. For example, when writing data to the transmit FIFO by 32-bit access and transmitting a16-bit word, the upper 16 bits are transmitted and the lower 16 bits are discarded as invalid data.

In the same way, when the word size is larger than the receive FIFO data access size, the upper bits are received as valid data. For example, when 32-bit data is stored in the receive FIFO and the data is read by 16-bit access, the lower 16 bits are discarded as invalid data.

Figure 24.9 shows the bit alignment of these registers.

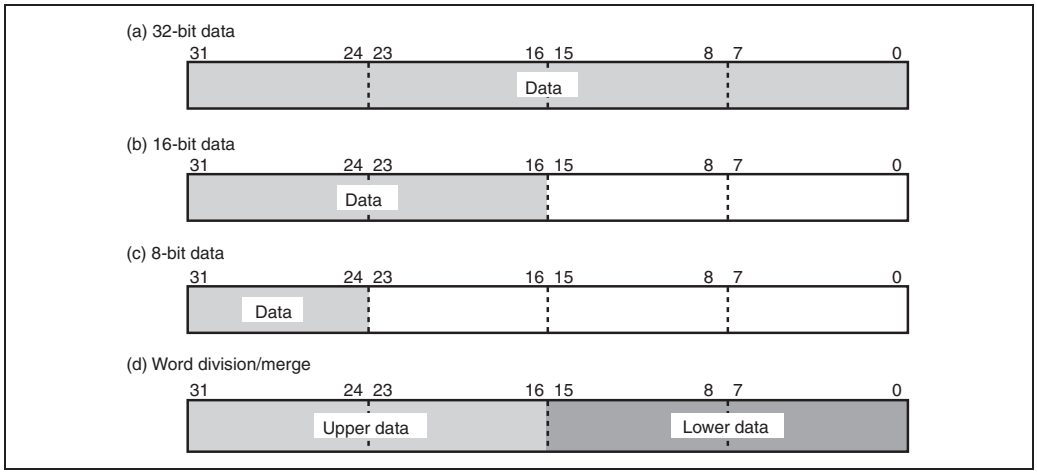


Figure 24.9 Transmit/Receive Data Bit Alignment

24.4.6 FIFO

(1) Overview

The transmit and receive FIFOs of the BBIF1 have the following features.

- 32 bits × 64 stages for transmission and 32 bits × 256 stages for reception
- The FIFO pointer is updated in one read or write cycle regardless of the access size of the CPU or DMAC. (One access cannot be divided into multiple accesses.)

(2) Transfer Request

A request for FIFO data transfer can be issued to the CPU or DMAC as the following interrupt sources.

- FIFO transmit request: TDREQ (interrupt source for transmission)
- FIFO receive request: RDREQ (interrupt source for reception)

The conditions for requesting FIFO data transfer can be specified separately for transmission and reception. The conditions for the transmit FIFO and receive FIFO are specified in the TFWM[2:0] bits and RFWM[2:0] bits in SIFCTR, respectively.

Table 24.5 Condition for Issuing Transmit Request

TFWM[2:0]	Number of Requested Stages	Condition for Transmit Request	Areas Used
000	1	64 stages of empty area	Smallest
001	32	32 or more stages of empty area	↕
010	40	24 or more stages of empty area	
011	48	16 or more stages of empty area	
100	52	12 or more stages of empty area	
101	56	8 or more stages of empty area	
110	60	4 or more stages of empty area	
111	64	1 or more stages of empty area	Largest

Table 24.6 Condition for Issuing Receive Request

RFWM[2:0]	Number of Requested Stages	Condition for Receive Request	Areas Used
000	1	1 or more stages of valid data	Smallest
001	4	4 or more stages of valid data	
010	8	8 or more stages of valid data	
011	16	16 or more stages of valid data	
100	32	32 or more stages of valid data	
101	64	64 or more stages of valid data	
110	128	128 or more stages of valid data	
111	256	256 stages of valid data	Largest

The maximum FIFO stages are always available even if the data area or empty area exceeds the size specified for the transfer condition. Accordingly, an overflow error or an underflow error occurs if the data area or empty area exceeds the maximum number of FIFO stages.

The FIFO transfer request is canceled when the specified condition is not satisfied even if the FIFO does not become empty or full.

(3) Number of FIFOs

The number of transmit and receive FIFO stages used are indicated by the following registers.

- Transmit FIFO: The number of empty FIFO stages is indicated by the TFUA[6:0] bits in SIFCTR.
- Receive FIFO: The number of valid data stages is indicated by the RFUA[8:0] bits in SIFCTR.

These registers show the number of data stages that can be transferred by the CPU or DMAC.

24.4.7 MMIF Transmission Flow Control

(1) Overview

The BBIF1_FLOW signal is a flow control output generated from the DMAC interrupt (DINT) signal as the input. While the BBIF1_FLOW output is active low indicating the flow state, data transmission from the MMIF is suspended, which allows secure reading of receive data during this time period. Table 22.7 shows the BBIF1_FLOW output state according to the values of the SIFLCTR register.

Table 24.7 BBIF1_FLOW Output State

State	DINT	FLE Bit	FLMASK Bit	BBIF1_FLOW
During transfer	H	0	0	H
During DMAC interrupt processing	L	0	0	L
FLE bit forcible flow	*	1	0	L
Flow output mask	*	*	1	H

Note: * Don't care

(2) Flow Control Procedure (when two buffers are used)

The following shows an example of DMAC setting to set two buffers (side A and side B) in the SDRAM for BBIF1 receive data (when using channel 1 of DMAC1, for example).

DMA1SAR_1 in DMAC1 = SIRFDR in BBIF1 (or BB1PKDATAR1 in DREQPAK)
DMA1DAR_1 in DMAC1 = Start address of side A buffer
DMA1TCR_1 in DMAC1 = Transfer count of side A/side B total buffer size
DMA1CHCR_1 in DMAC1 = (HIE = 1 and IE = 1)
DMA1DMICR in DMAC1 = H'00000091

When a DMA transfer starts, a half end interrupt or a transfer end interrupt is output upon completion of the transfer of side A or side B. The DINT signal is also asserted at the same time, and the BBIF1_FLOW output turns low indicating the flow state.

This automatically suspends the MMIF transmit data output. Setting the APFLE bit in BBIF1 to 1 within the DMAC1 interrupt handler maintains the flow state until the buffer read operation is completed. Clearing the APFLE bit to 0 automatically restarts transfer of the transmit data from the suspended position.

Figure 24.10 shows the overview of receive data read processing.

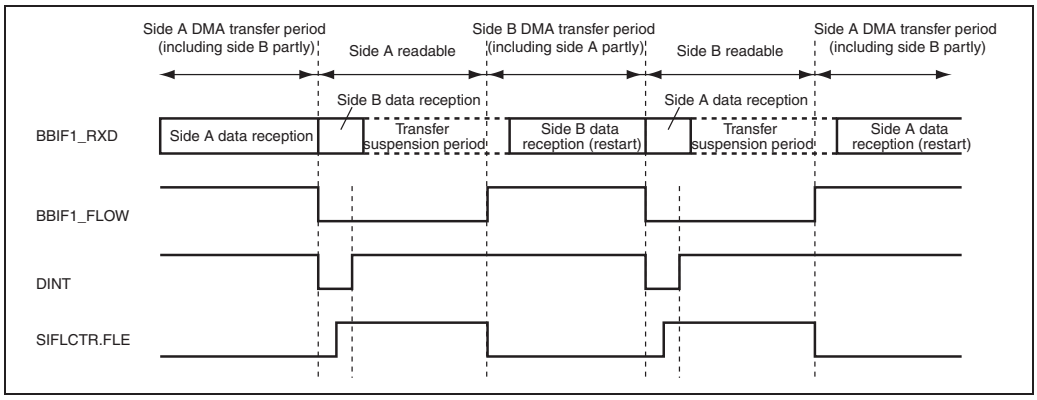


Figure 24.10 Receive Data Read Using BBIF1_FLOW

24.4.8 BBIF transmit flow control

BBIF1 can dynamic control the transmission of a message data output for MMIF with BB_RX_FLOW_N. MMIF can read data safty when BB_RX_FLOW_N is low level. Because BBIF1 doen't transmit data.

BBIF1 stop transmission when detect BBFLE = 1 or flow signal asserted if BBFLMASK bit set 0.BBIF1 stop till BB_RX_FLOW_N negate.

BBIF1 re-start transmit when detect BB_FLOW_N negated and BBFLE=0.The value of BB_RX_FLOW_N and BBFLE is masked when BBFLMASK=1.

The transmition was expanded after BB_RX_FLOW_N asserted.Because BBIF1 need least 2 cycle of BBIF1_TSCK for detection BB_RX_FLOW_N for synchronization.Fig24.11 shown timing chart of RX_FLOW_N.

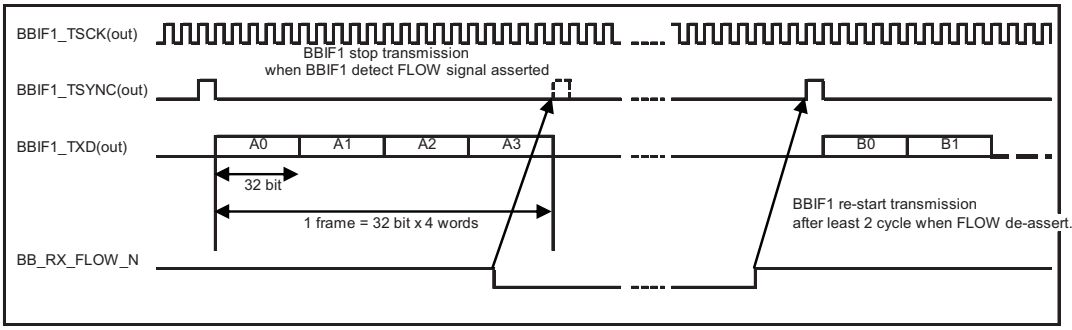


Figure 24.11 Timing chart of BB_RX_FLOW_N

24.4.9 Transmit and Receive Procedures

(1) Transmission in Master Mode

Figure 24.12 shows an example of settings and operation for transmission in master mode.

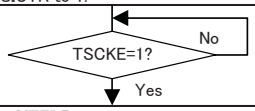
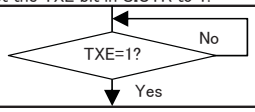
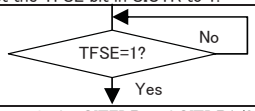
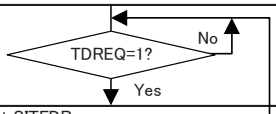
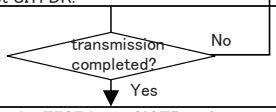
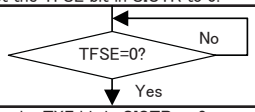
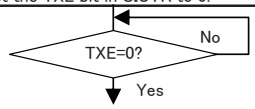
No.	Flow chart	Setting	operation
1	Set SITMDR1/2/3 SITSCR , SIFCTR , and SIIER.	Set the operating mode, serial clock , and FIFO threshold value, and enable interrupts.	
2	Set the TSCKE bit in SICTR to 1.	Set output sampling and start the baud rate generator.	Outputs the serial clock.
3		Read 1 from TSCKE bit in SICTR.	
4	Set SITFDR, SITDR1/2.	Set transmit data.	
5	Set the TXE bit in SICTR to 1.	Enable transmittion.	
6		Read 1 from TXE bit in SICTR.	
7	Set the TFSE bit in SICTR to 1.	Starting output frame of synchronization signal.	Outputs the frame syncronization signal.
8		Read 1 from TFSE bit in SICTR.	
9	Transmit the SITFDR and SITDR1/2 contents through TXD in synchronization with		Transmit data.
10			Assert transmit data transfer request according to the FIFO threshold valu
11	Set SITFDR.	Set transfer data.	
12		Read 1 from TFEMP bit in SICTR.	
13	Set the TFSE bit in SICTR to 0.	Disable output frame of synchronization signal.	
14		Read 0 from TFSE bit in SICTR.	
15	Set the TXE bit in SICTR to 0.	Disable transmit enable.	
16	 Transmission complete.	Read 0 from TXE bit in SICTR.	

Figure 24.12 Example of Transmit Procedure in Master Mode

(2) Reception in Slave Mode

Figure 24.13 shows an example of settings and operation for reception in slave mode.

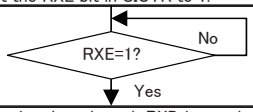
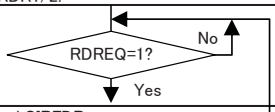
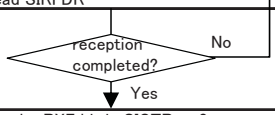
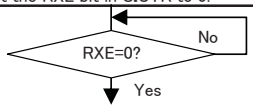
No.	Flow chart	Setting	operation
1	Setting master device polarity	Depend on master device.	Decide SYNC/SCK polarity
2	Set SIRMDR1/2/3 SIFCTR and SIIER.	Set operating mode FIFO threshold value and enable interrupts.	
3	Set the RXE bit in SICTR to 1.	Enable reception.	
4		Read 1 from RXE bit in SICTR.	
5	Receive data through RXD in synchronization with MSIOF_RSYNC and store it in SIRFDR and SIRDR1/2.		Receive data
6			Assert reception data transfer request according to the FIFO threshold valu
7	Read SIRFDR	Read reception data.	
8			
9	Set the RXE bit in SICTR to 0.	Disable reception enable	
10	 Reception complete.	Read 0 from RXE bit in SICTR.	

Figure 24.13 Example of Receive Procedure in Slave Mode

(3) Reset

After a power-on reset is applied, module stop state is canceled, or a reset signal is asserted through the TXRST or RXRST setting in SICTR, it takes about SUBϕ20 cycles to complete the internal reset of the module. During a period from the beginning of reset until the TXRST or RXRST value is read as 0, do not modify the control register or access the FIFOs.

The BBIF1 can separately reset the transmit and receive units by setting the following bits to 1.

- Transmit reset: TXRST bit in SICTR
- Receive reset: RXRST bit in SICTR

Table 24.8 Transmit and Receive Reset

Type	Objects Initialized
Transmit reset	SITDR1, SITDR2, and SITFDR
	Transmit FIFO write pointer
	TCRDY, TFEMP, and TDREQ bits in SISTR
	TXE bit in SICTR
Receive reset	SIRDR1, SIRDR2, and SIRFDR
	Receive FIFO read pointer
	RCRDY, RFFUL, and RDREQ bits in SISTR
	RXE bit in SICTR

(4) Initial Operating Mode

After a power-on reset, both the transmit and receive units are initialized to master mode (0 is output through CLK and SYNC). When using slave mode, keep the connected device outputting 0 until the operating mode setting is completed.

24.4.10 Interrupts

The BBIF1 has one type of interrupt.

(1) Interrupt Sources

Interrupts can be issued by several sources. Each source is shown as a BBIF1 status in SISTR. Table 24.9 lists the BBIF1 interrupt sources.

Table 24.9 BBIF1 Interrupt Sources

No.	Classification	Bit Name	Function Name	Description
1	Transmission	TDREQ	Transmit FIFO transfer request	The transmit FIFO has empty space of specified size or more.
2		TFEMP	Transmit FIFO empty	The transmit FIFO is empty.
3		TEOF	Frame transmission end	Transmission of data with a length of one frame is completed.
4	Reception	RDREQ	Receive FIFO transfer request	The receive FIFO stores data of specified size or more.
5		RFFUL	Receive FIFO full	The receive FIFO is full.
6		REOF	Frame reception end	Reception of data with a length of one frame is completed.
7	Control	TCRDY	Transmit control data ready	The transmit control data register is ready to be written.
8		RCRDY	Receive control data ready	The receive control data register stores valid data.
9	Error	TFUDF	Transmit FIFO underflow	Serial data transmit timing has arrived while the transmit FIFO is empty.
10		TFOVF	Transmit FIFO overflow	The transmit FIFO is written to while it is full.
11		RFOVF	Receive FIFO overflow	Serial data is received while the receive FIFO is full.
12		RFUDF	Receive FIFO underflow	The receive FIFO is read while the receive FIFO is empty.
13		TFSERR	Transmit FS error	A transmit frame synchronization signal is input before the specified number of bits has been reached (in slave mode).
14		RFSERR	Receive FS error	A receive frame synchronization signal is input before the specified number of bits has been reached (in slave mode).

Whether an interrupt is issued from an interrupt source is determined by the SIIER settings. If an interrupt source bit is set to 1 and the corresponding bit in SIIER is set to 1, a BBIF1 interrupt is issued.

(2) TDREQ and RDREQ

The transmit FIFO transfer request (TDREQ) and receive FIFO transfer request (RDREQ) are signals indicating the state. If the state changes after TDREQ or RDREQ is set, it is automatically cleared by the BBIF1.

When the DMA transfer is used, a DMA transfer request signal is pulled low for one cycle at the end of DMA transfer.

(3) Processing when Errors Occur

- Transmit FIFO underflow (TFUDF)
  The value specified with TXDIZ in SICTR is output.
- Transmit FIFO overflow (TFOVF)
  The contents of the transmit FIFO are protected, and the write operation causing the overflow is ignored.
- Receive FIFO overflow (RFOVF)
  Data causing the overflow is discarded and lost.
- Receive FIFO underflow (RFUDF)
  An undefined value is output on the bus.
- Transmit FS error (TFSERR)
  The internal counter is reset according to the synchronization signal in which an error occurs.
- Receive FS error (RFSERR)
  The internal counter is reset according to the synchronization signal in which an error occurs.

24.4.11 Transmit and Receive Timing

Examples of the BBIF1 serial transmission and reception are shown in Figure 24.14 and 24.15.

(1) 16-Bit Synchronization Pulse

Synchronization pulse method, one group, one word, 16 bits in a word, no bit delay

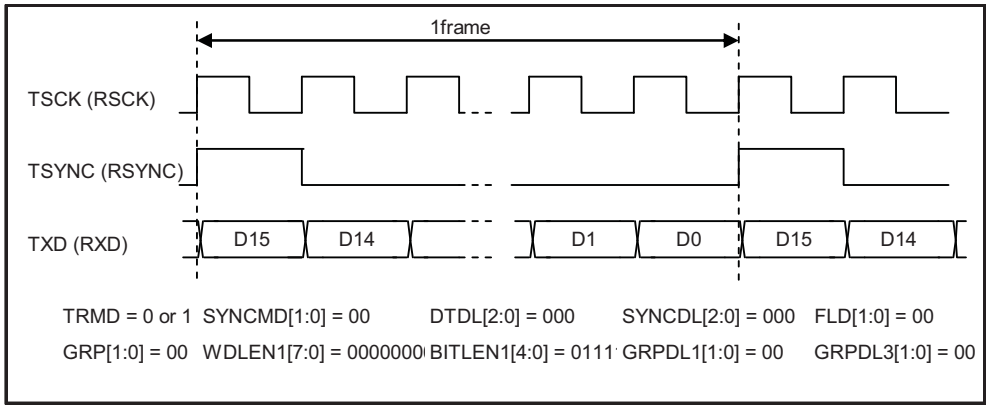


Figure 24.14 Transmit and Receive Timing (16 Bits)

(2) 32-Bit Synchronization Pulse

Synchronization pulse method, one group, 32 words, 32 bits in a word, 1-bit delay

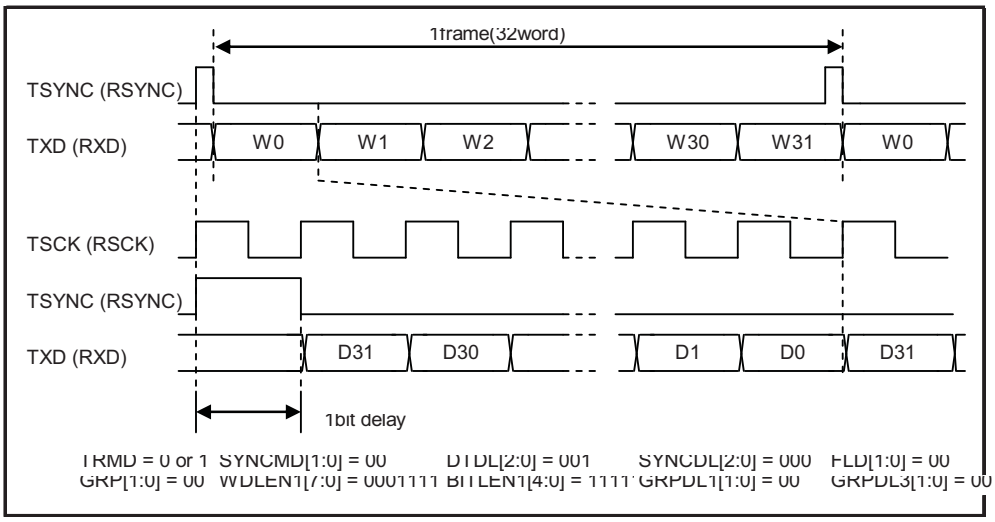


Figure 24.15 Transmit and Receive Timing (32 Bits)

24.4.12 SPI

The BBIF can be used as an SPI device by setting the registers appropriately.

(1) Example of SPI Device Connection

Figure 24.16 shows an example of connection with an SPI device.

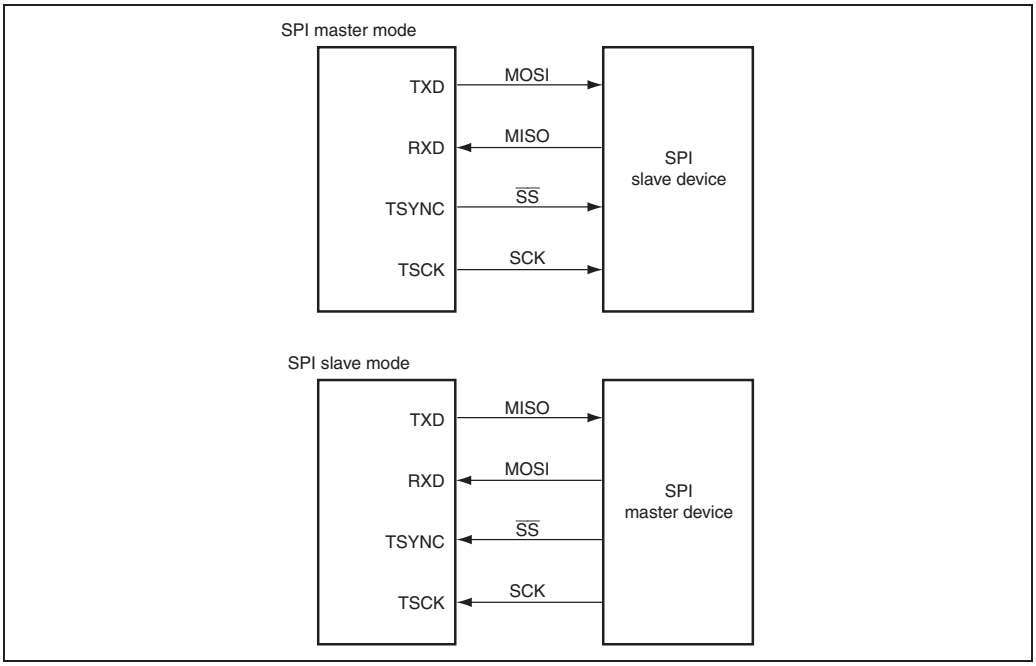
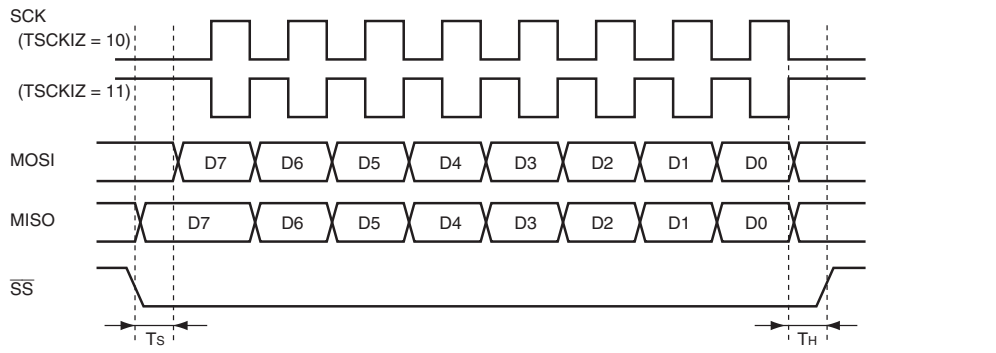


Figure 24.16 Example of SPI Device Connection

(2) SPI Serial Clock Timing

Figure 24.17 and 24.18 show the data and clock timing in SPI mode. As shown in the figures, four types of serial transfer formats can be used.



Transmit: TRMD = 1 (master) or 0 (slave) PCON = 1 SYNCMD[1:0] = 10 SYNCAC = 1
GRP[1:0] = 00 BITLEN1[4:0] = 00111 WDLEN1[7:0] = 00000000 GRPDL1[1:0] = 00 GRPDL3[1:0] = 00

Receive: TRMD = 0 SYNCMD[1:0] = 10 SYNCAC = 1
GRP[1:0] = 00 BITLEN1[4:0] = 00111 WDLEN1[7:0] = 00000000 GRPDL1[1:0] = 00 GRPDL3[1:0] = 00

Set DTDL to satisfy TS (0 to 2 can be specified in 0.5-clock-cycle units)
Set SYNCDL to satisfy TH (0 to 2 can be specified in 0.5-clock-cycle units)
The sum of DTDL and SYNCDL settings should be an integer.

SICTR: Upper: TSCKIZ[1:0] = 10, RSCKIZ[1:0] = 10, TEDG = 1, REDG = 1
Lower: TSCKIZ[1:0] = 11, RSCKIZ[1:0] = 11, TEDG = 0, REDG = 0

Figure 24.17 SPI Clock and Data Timing 1

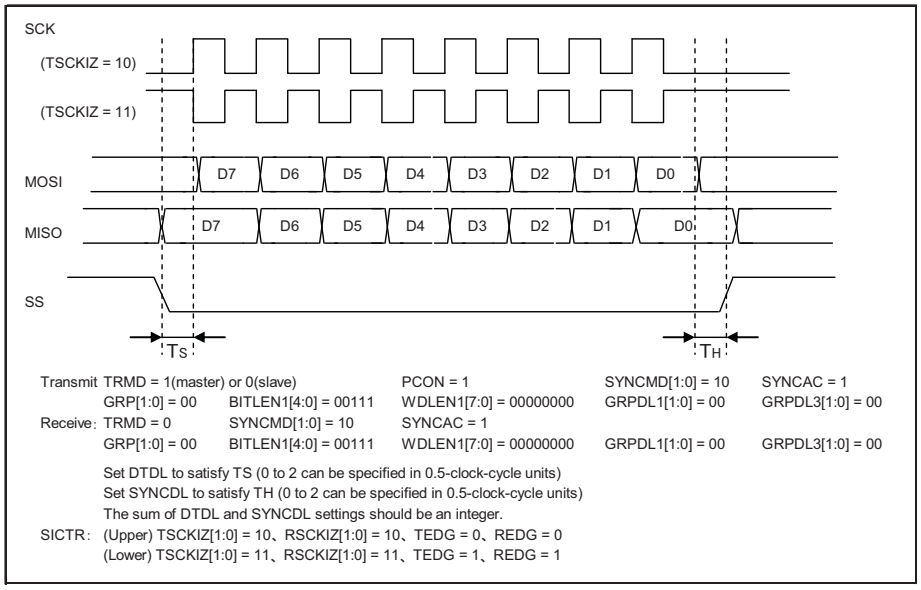


Figure 24.18 SPI Clock and Data Timing 2

24.4.13 Notes on Using SPI Mode

When the module stop release or software reset is performed in SPI mode, set the control register (SICTR) again with each of the receive-setting bits (RSCKIZ/REDG) being 0.

When using SPI master mode, set the FLD bits in SITMDR1 to ensure four SUBϕ cycles or more.

24.4.14 IIS

This module can support IIS format with following setting which is shown Figure 23.22 and Figure 23.23.BITLEN1/2 bit will change by usage.

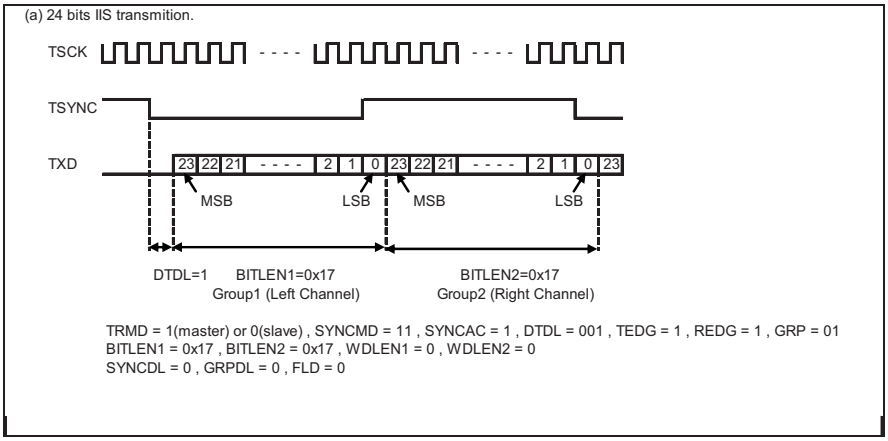


Figure 24.19 24 bits IIS transmition

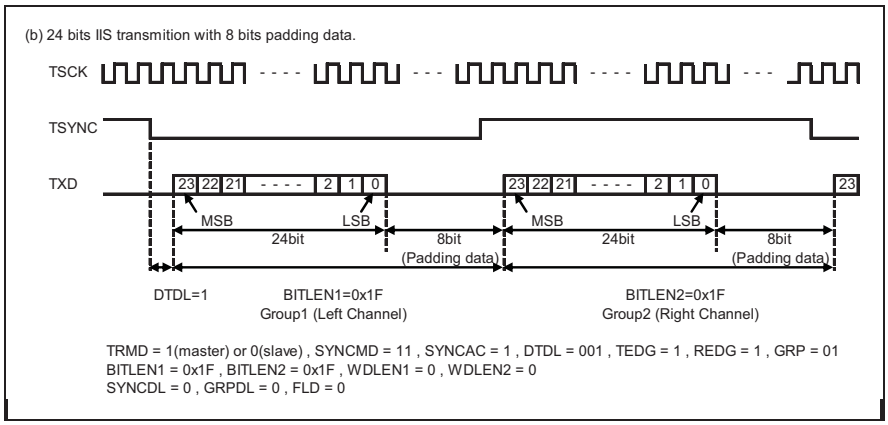


Figure 24.20 24 bits IIS transmition with 8 bits padding data

Section 25 Baseband Interface 2 (BBIF2)

This LSI includes one channel of clock-synchronized serial I/O module (BBIF2) with FIFO, which can be connected to the BB-domain PCMSEL.

25.1 Features

- FIFO capacity: 32 bits × 64 stages for transmission and 32 bits × 256 stages for reception
- MSB first or LSB first selectable for data transmission and reception
- Synchronization in frame synchronization pulse, level, or left/right channel switch mode
- Supports both transmit master/slave modes and receive slave mode.
- Common clock and synchronization signals for transmission and reception
- Supports multiple-channel communication
  - Transfers multiple groups or words data in one frame.
  - The word size for each group can be selected from eight to 32 bits.
  - Up to 256 words can be transferred in each group when one or two groups are used, or up to 16 words can be transferred in each group when three or four groups are used.
- Interrupts: One type
- Serial clock

  Internal clock SUBϕ, FSIϕ, or FMSOϕ is selectable as the master clock source.
- DMA transfer

  Supports DMA transfer by a transfer request for transmission and reception.

  Supports multibyte DMA transfer.
- Serial format

  Supports serial formats such as IIS (transmission only) and SPI (for master and slave modes).

Figure 25.1 shows a block diagram of the BBIF2.

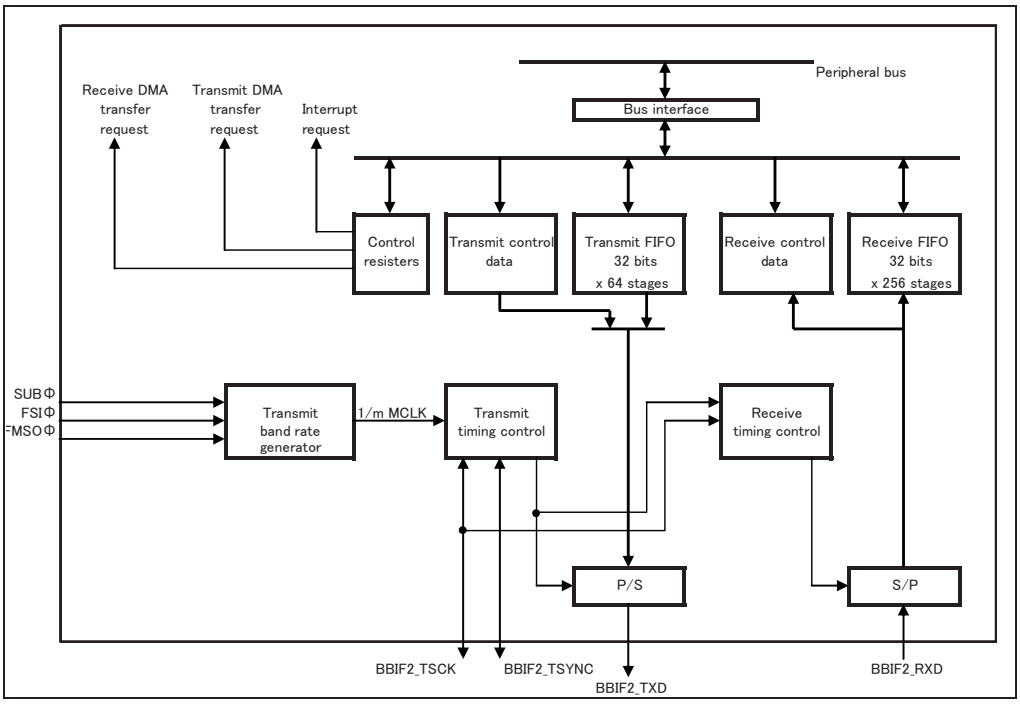


Figure 25.1 Block Diagram of BBIF2

25.2 Input/Output Pins

The pin configuration in this module is shown in Table 25.1.

Table 25.1 Pin Configuration

Name	Abbreviation*	I/O	Function
BBIF2_TSCK	SCK	I/O	BBIF2 serial clock input/output Used as BBIF2_SCK when the clock common to transmission and reception is used.
BBIF2_TSYNC($\overline{SS0}$)	$\overline{SS0}$	I/O	BBIF2 frame synchronization signal channel-0 input/output Used as BBIF2_SYNC when the synchronization signal common to transmission and reception is used.
BBIF2_TXD(MOSI/MISO)	MOSI/MISO	Output	BBIF2 transmit data
BBIF2_RXD(MISO/MOSI)	MISO/MOSI	Input	BBIF2 receive data

Note: * In SPI mode, names SCK, $\overline{SS0}$, $\overline{SS1}$, $\overline{SS2}$, MOSI, and MISO are used.

25.3 Register Descriptions

Table 25.2 shows the register configuration of the BBIF2. Table 25.3 shows the register state in each processing mode.

Table 25.2 BBIF2 Register Configuration

Name	Abbreviation	R/W	Address	Access Size
BBIF2 transmit mode register 1	SITMDR1	R/W	H'E6CA0000 H'E7CA0000 H'FFFA0000	32
BBIF2 transmit mode register 2	SITMDR2	R/W	HE6CA0004 HE7CA0004 HFFFA0004	32
BBIF2 transmit mode register 3	SITMDR3	R/W	H'E6CA0008 H'E7CA0008 H'FFFA0008	32
BBIF2 receive mode register 1	SIRMDR1	R/W	H'E6CA0010 H'E7CA0010 H'FFFA0010	32
BBIF2 receive mode register 2	SIRMDR2	R/W	H'E6CA0014 H'E7CA0014 H'FFFA0014	32
BBIF2 receive mode register 3	SIRMDR3	R/W	H'E6CA0018 H'E7CA0018 H'FFFA0018	32
BBIF2 transmit clock select register	SITSCR	R/W	H'E6CA0020 H'E7CA0020 H'FFFA0020	16
BBIF2 control register	SICTR	R/W	H'E6CA0028 H'E7CA0028 H'FFFA0028	32
BBIF2 FIFO control register	SIFCTR	R/W	H'E6CA0030 H'E7CA0030 H'FFFA0030	32

Name	Abbreviation	R/W	Address	Access Size
BBIF2 status register	SISTR	R/W	H'E6CA0040	32
			H'E7CA0040	
			H'FFFA0040	
BBIF2 interrupt enable register	SIIER	R/W	H'E6CA0044	32
			H'E7CA0044	
			H'FFFA0044	
BBIF2 transmit control data register 1	SITDR1	R/W	H'E6CA0048	16/32
			H'E7CA0048	
			H'FFFA0048	
BBIF2 transmit control data register 2	SITDR2	R/W	H'E6CA004C	16/32
			H'E7CA004C	
			H'FFFA004C	
BBIF2 transmit FIFO data register	SITFDR	W	H'E6CA0050	16/32
			H'E7CA0050	
			H'FFFA0050	
BBIF2 receive control data register 1	SIRDR1	R	H'E6CA0058	16/32
			H'E7CA0058	
			H'FFFA0058	
BBIF2 receive control data register 2	SIRDR2	R	H'E6CA005C	16/32
			H'E7CA005C	
			H'FFFA005C	
BBIF2 receive FIFO data register	SIRFDR	R	H'E6CA0060	16/32
			H'E7CA0060	
			H'FFFA0060	

Note: H'FFFAxxxx and H'E6CAxxxx (or H'E7CAxxxx) are used when making an access from the realtime domain and system domain, respectively.

Table 25.3 Register States in Each Operating Mode

Abbreviation	Power-on Reset	Module Standby
SITMDR1	Initialized	Retained
SITMDR2	Initialized	Retained
SITMDR3	Initialized	Retained
SIRMDR1	Initialized	Retained
SIRMDR2	Initialized	Retained
SIRMDR3	Initialized	Retained
SITSCR	Initialized	Retained
SICTR	Initialized	Retained
SIFCTR	Initialized	Retained
SISTR	Initialized	Retained
SIIER	Initialized	Retained
SITDR1	Initialized	Initialized
SITDR2	Initialized	Initialized
SITFDR	Initialized	Initialized
SIRDR1	Initialized	Initialized
SIRDR2	Initialized	Initialized
SIRFDR	Undefined	Initialized

25.3.1 Transmit Mode Register 1 (SITMDR1)

SITMDR1 is a 32-bit readable/writable register that specifies the BBIF2 transmit mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TRMD	PCON	SYNCMD[1:0]		SYNCCH[1:0]		SYNCA0	BITLSB	—	DTDL[2:0]			—	SYNCDL[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	DIV[3:0]				—	—	—	—	FLD[1:0]		CONT	TXSTP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31	TRMD	1	R/W	Transfer Mode Selects the transfer mode. 0: Slave mode 1: Master mode
30	PCON	0	R/W	Transfer Signal Connection 0: Setting prohibited 1: Uses BBIF2_TSCK and BBIF2_TSYNC for transmission and reception (BBIF2_SCK and BBIF2_SYNC). When value 1 set to the TXRST bit becomes valid, the RXRST bit becomes valid at the same time.
29, 28	SYNCMD [1:0]	00	R/W	SYNC Mode These bits specify the mode for the BBIF2_TSYNC signal. 00: Frame start synchronization pulse 01: 1-bit synchronization pulse for last data in slot 10: Level mode/SPI 11: L/R mode

27, 26	SYNCCH [1:0]	00	R/W	Synchronization Signal Channel Select 00: The frame synchronization signal is output from BBIF2_TSYNC. Other than above: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Descriptions
25	SYNCAC	0	R/W	BBIF2_TSYNC Polarity 0: Active-high signal in synchronization pulse or level mode, or driven high then low in L/R mode 1: Active-low signal in synchronization pulse or level mode, or driven low then high in L/R mode
24	BITLSB	0	R/W	MSB/LSB First 0: MSB first 1: LSB first
23	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
22 to 20	DTDL[2:0]	001	R/W	Data Pin Bit Delay for BBIF2_TSYNC Pin B'1xx is valid only in SPI mode. In SPI mode, these bits should be specified so that the sum of the delays specified through the DTDL[2:0] and SYNCDL[2:0] bits becomes an integer value. 000: No bit delay 001: 1-clock-cycle delay 010: 2-clock-cycle delay 101: 0.5-clock-cycle delay 110: 1.5-clock-cycle delay Other than above: Setting prohibited
19	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
18 to 16	SYNCDL [2:0]	000	R/W	Frame Synchronization Signal Timing Delay These bits extend the transmit frame synchronization signal. This setting is invalid when SYNCMD[1:0] = 01. B'1xx is valid only in SPI mode. In SPI mode, these bits should be specified so that the sum of the delays specified through the DTDL[2:0] and SYNCDL[2:0] bits becomes an integer value. When L/R mode , these bits should always be set to 000. 000: No bit delay 001: 1-clock-cycle delay 010: 2-clock-cycle delay 011: 3-clock-cycle delay 101: 0.5-clock-cycle delay 110: 1.5-clock-cycle delay Other than above: Setting prohibited
15 to 12	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
11 to 8	DIV[3:0]	0000	R/W	Word Division One 32-bit word stored in the transmit FIFO can be transmitted as two separate 16-bit words through two groups. The word count in each group must be set to 1. In this case, data of groups other than word division target groups must be handled as control data. This setting is valid only in LR mode. 0000: Not divided 0001: Upper word in group 1 and lower word in group 2 Other than above: Setting prohibited
7 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
3, 2	FLD[1:0]	00	R/W	Frame Synchronization Signal Interval These bits specify the minimum idle time between frames in the number of serial clock cycles. This setting is valid only in master mode. When Level mode, set the FLD bits in SIRMDR1 for at least 4 cycles of SUBφ. When L/R mode , these bits should always be set to 00. 00: 0-clock-cycle delay 01: 1-clock-cycle delay 10: 2-clock-cycle delay 11: 3-clock-cycle delay
1	CONT	0	R/W	Continuous Frame Transmission Specifies continuous transmission of multiple frames of data within one frame. This setting is valid when SYNCMD[1:0] = 00 or 10. When the TFSE bit in SICTR is set to 0 in master mode, transmission is terminated after one-frame data is transmitted. 0: Does not perform continuous transmission. 1: Performs continuous transmission.

0	TXSTP	0	R/W	Transmission Stop Specifies the processing performed when the remaining number of stages in the transmit FIFO becomes smaller than the total number of words in the transmit frame. This setting is valid only in master mode. When transmission is continued, the value specified with TXDIZ is output as transmit data. If, with TXSTP = 1, the remaining number of stages in the transmit FIFO becomes smaller than the total number of words in the transmit frame, transmission is stopped temporarily. After this, however, transmission is automatically restarted if writing into the transmit FIFO causes the remaining number to become larger than the total number of words in the transmit frame. 0: Continues transmission when the transmit FIFO is empty. (The frame synchronization signal is output.) 1: Temporarily stops transmission when the remaining number of stages in the transmit FIFO becomes smaller than the total number of words in the transmit frame. (The frame synchronization signal is not output.)

25.3.2 Transmit Mode Register 2 (SITMDR2)

SITMDR2 is a 32-bit readable/writable register that specifies the BBIF2 transmit mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GRP[1:0]		—	BITLEN1[4:0]					WDLEN1[7:0]							
Initial value:	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GRPDL1[1:0]		GRPDL3[1:0]		CRDE4	CRDE3	CRDE2	CRDE1	CRDNUM4	CRDNUM3	CRDNUM2	CRDNUM1	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31, 30	GRP[1:0]	00	R/W	Group Count The number of groups is set to the value specified in these bits + 1. When three or more groups are specified, the word size (BITLEN) is set to 16 bits or less.
29	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
28 to 24	BITLEN1[4:0] (BITLEN3)	01111	R/W	Word Size (8 to 32 bits) The word size (bits) of groups 1 and 3 is set to the value specified in these bits + 1 (BITLEN1 = BITLEN3). Eight bits or a larger size should be specified. When three or four groups are used, the word size is set to 16 bits or less. (the highest bit is ignored).
23 to 16	WDLEN1[7:0] (WDLEN1[3:0] WDLEN3[3:0])	H'00	R/W	Word Count (1 to 256 words) The word counts of groups 1 and 3 are set to WDLEN1 + 1 and WDLEN3 + 1 respectively. When one or two groups are used, the 8-bit value is set to WDLEN1. When three or four groups are used, the upper 4-bit value is set to WDLEN1, and the lower 4-bit value is set to WDLEN3.

Bit	Bit Name	Initial Value	R/W	Descriptions
15, 14	GRPDL1[1:0]	00	R/W	Group 1 Data Transmission Delay These bits specify the number of blank bits to be inserted before transmission of group 1. The value specified with TXDIZ in SICTR is output during transmission. 00: 0-clock-cycle delay 01: 1-clock-cycle delay 10: 2-clock-cycle delay 11: 3-clock-cycle delay
13, 12	GRPDL3[1:0]	00	R/W	Group 3 Data Transmission Delay These bits specify the number of blank bits to be inserted before transmission of group 3. The value specified with TXDIZ in SICTR is output during transmission. 00: 0-clock-cycle delay 01: 1-clock-cycle delay 10: 2-clock-cycle delay 11: 3-clock-cycle delay
11	CRDE4	0	R/W	Control Data Enable
10	CRDE3	0	R/W	"x" in CRDEx represents a group. Each of these bits specifies whether the group transmits FIFO data or control data. 0: The specified group transmits FIFO data. 1: The specified group transmits control data.
9	CRDE2	0	R/W	
8	CRDE1	0	R/W	
7	CRDNUM4	0	R/W	Control Data Transmit Count
6	CRDNUM3	0	R/W	"x" in CRDNUMx represents a group. Each of these bits specifies the transmission count of control data when multiple words are set for a control data group. Each bit is valid only when the corresponding CRDE bit is 1. When CRDNUMx = 1, control data is transmitted only for the first word, and the value specified with TXDIZ is output for other words. 0: Transmits control data continuously. 1: Transmits control data only once.
5	CRDNUM2	0	R/W	
4	CRDNUM1	0	R/W	

Bit	Bit Name	Initial Value	R/W	Descriptions
3 to 0	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.

25.3.3 Transmit Mode Register 3 (SITMDR3)

SITMDR3 is a 32-bit readable/writable register that specifies the BBIF2 transmit mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	BITLEN2[4:0]					WDLEN2[7:0]							
Initial value:	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GRPDL2[1:0]		GRPDL4[1:0]		—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 24	BITLEN2[4:0] (BITLEN4)	01111	R/W	Word Size (8 to 32 bits) The word size is set to the value specified in these bits + 1. When three or four groups are used, the word size is set to 16 bits or less (the highest bit is ignored).

Bit	Bit Name	Initial Value	R/W	Descriptions
23 to 16	WDLEN2[7:0] (WDLEN2[3:0] WDLEN4[3:0]	H'00	R/W	Word Count (1 to 256 words) The word counts of groups 2 and 4 are set to WDLEN2 + 1 and WDLEN4 + 1 respectively. When one or two groups are used, the 8-bit value is set to WDLEN2. When three or four groups are used, the upper 4-bit value is set to WDLEN2, and the lower 4-bit value is set to WDLEN4.
15, 14	GRPDL2[1:0]	00	R/W	Group 2 Data Transmission Delay These bits specify the number of blank bits to be inserted before transmission of group 2. The value specified with TXDIZ in SICTR is output during transmission. 00: 0-clock-cycle delay 01: 1-clock-cycle delay 10: 2-clock-cycle delay 11: 3-clock-cycle delay
13, 12	GRPDL4[1:0]	00	R/W	Group 4 Data Transmission Delay These bits specify the number of blank bits to be inserted before transmission of group 4. The value specified with TXDIZ in SICTR is output during transmission. 00: 0-clock-cycle delay 01: 1-clock-cycle delay 10: 2-clock-cycle delay 11: 3-clock-cycle delay
11 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

25.3.4 Receive Mode Register 1 (SIRMDR1)

SIRMDR1 is a 32-bit readable/writable register that specifies the BBIF2 receive mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TRMD	PCON	SYNCMD[1:0]		SYNCCH[1:0]		SYNC AC	BITLSB	—	DTDL[2:0]			—	SYNCDL[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	MRG[3:0]				—	—	—	—	—	—	CONT	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R/W	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31	TRMD	1	R/W	Transfer Mode Selects the transfer mode. Set the PCON bit in SITMDR1 to 1. 0: Slave mode 1: Master mode
30	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
29, 28	SYNCMD [1:0]	00	R/W	SYNC Mode These bits specify the mode for the BBIF2_SYNC signal. Set these bits to the same value as SYNCMD[1:0] in SITMDR1. 00: Frame start synchronization pulse 01: 1-bit synchronization pulse for last data in slot 10: Level mode/SPI 11: L/R mode
27, 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
25	SYNCAC	0	R/W	BBIF2_SYNC Polarity Set this bit to the same value as SYNCAC in SITMDR1. 0: Active-high signal in synchronization pulse or level mode, or driven high then low in L/R mode 1: Active-low signal in synchronization pulse or level mode, or driven low then high in L/R mode
24	BITLSB	0	R/W	MSB/LSB First 0: MSB first 1: LSB first
23	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
22 to 20	DTDL[2:0]	001	R/W	Data Pin Bit Delay for BBIF2_SYNC Pin B'1xx is valid only in SPI mode. In SPI mode, these bits should be specified so that the sum of the delays specified through the DTDL[2:0] and SYNCDL[2:0] bits becomes an integer value. Set these bits to the same value as DTDL in SITMDR1. 000: No bit delay 001: 1-clock-cycle delay 010: 2-clock-cycle delay 101: 0.5-clock-cycle delay 110: 1.5-clock-cycle delay Other than above: Setting prohibited
19	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
18 to 16	SYNCDL [2:0]	000	R/W	BBIF2_SYNC Timing Delay The synchronization signal is extended for the clock cycles specified in these bits. This setting is invalid when SYNCMD[1:0] = 01. B'1xx is valid only in SPI mode. In SPI mode, these bits should be specified so that the sum of the delays specified through the DTDL[2:0] and SYNCDL[2:0] bits becomes an integer value. Set these bits to the same value as SYNCDL in SITMDR1. When L/R mode , these bits should always be set to 000. 000: No bit delay 001: 1-clock-cycle delay 010: 2-clock-cycle delay 011: 3-clock-cycle delay 101: 0.5-clock-cycle delay 110: 1.5-clock-cycle delay Other than above: Setting prohibited
15 to 12	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
11 to 8	MRG[3:0]	0000	R/W	Word Merge The data received as 16-bit words of two groups can be merged into one 32-bit word and the merged data is stored in the receive FIFO. The word count in the groups to be merged must be set to 1. In this case, data of groups other than word merging target groups must be handled as control data. This setting is valid only in LR mode. 0000: Not merged 0001: Upper word in group 1 and lower word in group 2 0100: Upper word in group 2 and lower word in group 1 Other than above: Setting prohibited
7 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
1	CONT	0	R/W	Continuous Frame Reception Specifies continuous reception of multiple frames of data within one frame. This setting is valid when SYNCMD[1:0] =00 or 10. When the RFSE bit in SICTR is set to 0 in master mode, reception is terminated after one-frame data is received. 0: Does not perform continuous reception. 1: Performs continuous reception.
0	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

25.3.5 Receive Mode Register 2 (SIRMDR2)

SIRMDR2 is a 32-bit readable/writable register that specifies the BBIF2 receive mode. Set this register so that the frame size equals the value specified in SITMDR2 and SITMDR3.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GRP[1:0]		—	BITLEN1[4:0]					WDLEN1[7:0]							
Initial value:	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GRPDL1[1:0]		GRPDL3[1:0]		CRDE4	CRDE3	CRDE2	CRDE1	CRDNUM4	CRDNUM3	CRDNUM2	CRDNUM1	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31, 30	GRP[1:0]	00	R/W	Group Count The number of groups is set to the value specified in these bits + 1. When three or more groups are specified, the word size (BITLEN) is set to 16 bits or less. When using transfer signal connection (PCON = 1), set the same value as the GRP bits in SITMDR2.

Bit	Bit Name	Initial Value	R/W	Descriptions
29	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
28 to 24	BITLEN1[4:0] (BITLEN3)	01111	R/W	Word Size (8 to 32 bits) The word size (bits) of groups 1 and 3 is set to the value specified in these bits + 1 (BITLEN1 = BITLEN3). Eight bits or a larger size should be specified. When three or four groups are used, the word size is set to 16 bits or less (the highest bit is ignored). When using transfer signal connection (PCON = 1), set the same value as the BITLEN1 bits in SITMDR2.
23 to 16	WDLEN1[7:0] (WDLEN1[3:0] WDLEN3[3:0])	H'00	R/W	Word Count (1 to 256 words) The word counts of groups 1 and 3 are set to WDLEN1 + 1 and WDLEN3 + 1 respectively. When one or two groups are used, the 8-bit value is set to WDLEN1. When three or four groups are used, the upper 4-bit value is set to WDLEN1, and the lower 4-bit value is set to WDLEN3. When using transfer signal connection (PCON = 1), set the same value as the WDLEN1 bits in SITMDR2.
15, 14	GRPDL1[1:0]	00	R/W	Group 1 Data Reception Delay These bits specify the delay in data reception of group 1. 00: 0-clock-cycle delay 01: 1-clock-cycle delay 10: 2-clock-cycle delay 11: 3-clock-cycle delay When using transfer signal connection (PCON = 1), set the same value as the GRPDL1 bits in SITMDR2.

Bit	Bit Name	Initial Value	R/W	Descriptions
13, 12	GRPDL3[1:0]	00	R/W	Group 3 Data Reception Delay These bits specify the delay in data reception of group 3. 00: 0-clock-cycle delay 01: 1-clock-cycle delay 10: 2-clock-cycle delay 11: 3-clock-cycle delay When using transfer signal connection (PCON = 1), set the same value as the GRPDL3 bits in SITMDR2.
11	CRDE4	0	R/W	Control Data Enable
10	CRDE3	0	R/W	"x" in CRDEx represents a group. Each of these bits specifies whether the group receives FIFO data or control data. 0: The specified group receives FIFO data. 1: The specified group receives control data.
9	CRDE2	0	R/W	
8	CRDE1	0	R/W	
7	CRDNUM4	0	R/W	Control Data Reception Count
6	CRDNUM3	0	R/W	"x" in CRDNUMx represents a group. Each of these bits specifies the reception count of control data when multiple words are set for a control data group. Each bit is valid only when the corresponding CRDE bit is 1. When CRDNUMx = 1, only the first word is received as control data, and the other words are discarded as invalid data. 0: Receives control data continuously. 1: Receives only one word of control data.
5	CRDNUM2	0	R/W	
4	CRDNUM1	0	R/W	
3 to 0	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.

25.3.6 Receive Mode Register 3 (SIRMDR3)

SIRMDR3 is a 32-bit readable/writable register that specifies the BBIF2 receive mode. Set this register so that the frame size equals the value specified in SITMDR2 and SITMDR3.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	BITLEN2[4:0]					WDLEN2[7:0]							
Initial value:	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GRPDL2[1:0]		GRPDL4[1:0]		—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 24	BITLEN2[4:0] (BITLEN4[3:0])	01111	R/W	Word Size (8 to 32 bits) The word size is set to the value specified in these bits + 1. When three or four groups are used, the word size is set to 16 bits or less (the highest bit is ignored). Set the word size to eight bits or more. When using transfer signal connection (PCON = 1), set the same value as the BITLEN2 bits in SITMDR3.
23 to 16	WDLEN2[7:0] (WDLEN4[3:0])	H'00	R/W	Word Count (1 to 256 words) The word counts of groups 2 and 4 are set to WDLEN2 + 1 and WDLEN4 + 1 respectively. When one or two groups are used, the 8-bit value is set to WDLEN2. When three or four groups are used, the upper 4-bit value is set to WDLEN2, and the lower 4-bit value is set to WDLEN4. When using transfer signal connection (PCON = 1), set the same value as the WDLEN2 bits in SITMDR3.

Bit	Bit Name	Initial Value	R/W	Descriptions
15, 14	GRPDL2[1:0]	00	R/W	Group 2 Data Reception Delay These bits specify the delay in data reception of group 2. 00: 0-clock-cycle delay 01: 1-clock-cycle delay 10: 2-clock-cycle delay 11: 3-clock-cycle delay When using transfer signal connection (PCON = 1), set the same value as the GRPDL2 bits in SITMDR3.
13, 12	GRPDL4[1:0]	00	R/W	Group 4 Data Reception Delay These bits specify the delay in data reception of group 4. 00: 0-clock-cycle delay 01: 1-clock-cycle delay 10: 2-clock-cycle delay 11: 3-clock-cycle delay When using transfer signal connection (PCON = 1), set the same value as the GRPDL4 bits in SITMDR3.
11 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

25.3.7 Control Register (SICTR)

SICTR is a 32-bit readable/writable register that specifies the BBIF2 operating state.

The values written to the TXE, RXE, TFSE, and, TSCKE bits become valid (can be read from the bits) several cycles after writing. These bits should not be modified together; modify one bit at a time, check that the new value can be read from the bit, and then modify another bit.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TSCKIZ[1:0]		RSCKIZ[1:0]		TEDG	REDG	—	—	TXDIZ[1:0]		—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TSCKE	TFSE	—	—	—	—	TXE	RXE	—	—	—	—	—	—	TXRST	RXRST
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R	R	R	R/W	R/W	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31, 30	TSCKIZ[1:0]	00	R/W	Transmit Clock Input/Output Polarity Select in SPI Mode When Transmission is Invalid When SPI mode is not used, these bits should always be set to 00. [Master mode] 00: Outputs BBIF2_TSCK when transmission is invalid. 01: Setting prohibited 10: Outputs 0. 11: Outputs 1. [Slave mode] 00: Inputs BBIF2_TSCK when transmission is invalid. 01: Setting prohibited 10: Inputs 0 through BBIF2_TSCK when transmission is invalid. 11: Inputs 1 through BBIF2_TSCK when transmission is invalid.

Bit	Bit Name	Initial Value	R/W	Descriptions
29, 28	RSCKIZ[1:0]	00	R/W	Receive Clock Input Polarity Select in SPI Mode In SPI mode, set these bits to the TSCKIZ value. 00: Inputs BBIF2_SCK when transmission is invalid. 01: Setting prohibited 10: Inputs 0 through BBIF2_SCK when transmission is invalid. 11: Inputs 1 through BBIF2_SCK when transmission is invalid.
27	TEDG	0	R/W	Transmit Timing 0: Outputs transmit data at the rising edge of the clock. 1: Outputs transmit data at the falling edge of the clock.
26	REDG	0	R/W	Receive Timing 0: Samples receive data at the falling edge of the clock. 1: Samples receive data at the rising edge of the clock.
25, 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23, 22	TXDIZ[1:0]	00	R/W	Pin Output When Transmission is Invalid These bits specify the BBIF2_TXD pin output state when transmission is invalid. 00: Outputs 0. 01: Outputs 1. 10: Output is in high-impedance state. 11: Setting prohibited
21 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
15	TSCKE	0	R/W	Transmit Serial Clock Output Enable This bit is valid in master mode. When this bit is set to 1, the BBIF2 initializes the baud rate generator and initiates the operation. At the same time, the BBIF outputs the clock generated by the baud rate generator to the BBIF2_TSCK pin. After the clock is output, 1 can be read. When transmitting data, set this bit to 1 before setting the TFSE and TXE bits. After data transmission, clear the TFSE and TXE bits and then clear this bit to 0. [Write data] 0: Disables the BBIF2_TSCK output. (Outputs the value specified with TSCKIZ.) 1: Enables the BBIF2_TSCK output. [Read data] 0: Does not output BBIF2_TSCK. (Outputs the value specified with TSCKIZ.) 1: Outputs BBIF2_TSCK.
14	TFSE	0	R/W	Transmit Frame Synchronization Signal Output Enable This bit is valid in master mode. When this bit is set to 1, the BBIF2 initializes the frame counter and initiates the operation. After the transmit frame synchronization signal is output, 1 can be read. When 0 is written to this bit, 0 is set after transmission of the frame. [Write data] 0: Disables the BBIF2_TSYNC output. (Outputs the value specified with SYNCAC.) 1: Enables the BBIF2_TSYNC output. [Read data] 0: Does not output BBIF2_TSYNC. (Outputs the value specified with SYNCAC.) 1: Outputs BBIF2_TSYNC.

Bit	Bit Name	Initial Value	R/W	Descriptions
13 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	TXE	0	R/W	Transmit Enable When this bit is set to 1, the BBIF2 starts data transmission from the beginning of the next frame (at the rising edge of the frame synchronization signal). After valid data is output, 1 can be read. When value 1 set to this bit becomes valid, the BBIF2 issues a transmit data transfer request according to the setting of the TFWM bits in SIFCTR. When transmit data is stored in the transmit FIFO, transmission of data from the BBIF2_TXD pin begins. When 0 is written to this bit, 0 is set after transmission of the frame. This bit is initialized upon a transmit reset. [Write data] 0: Disables the BBIF2_TXD output. (Outputs the value specified with TXDIZ.) 1: Enables the BBIF2_TXD output. [Read data] 0: Does not output BBIF2_TXD. (Outputs the value specified with TXDIZ.) 1: Outputs BBIF2_TXD.

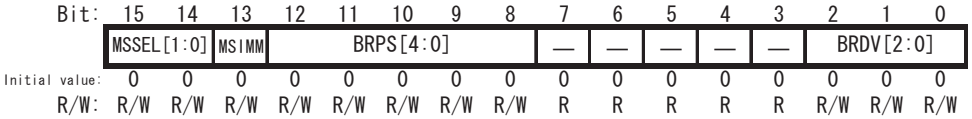
Bit	Bit Name	Initial Value	R/W	Descriptions
8	RXE	0	R/W	Receive Enable When this bit is set to 1, the BBIF2 starts data reception from the beginning of the next frame (at the rising edge of the frame synchronization signal). When value 1 set to this bit becomes valid, the BBIF2 begins reception of data through the BBIF2_RXD pin. When receive data is stored in the receive FIFO, the BBIF issues a receive data transfer request according to the setting of the RFWM bits in SIFCTR. This bit is initialized upon a receive reset. [Write data] 0: Disables data reception through BBIF2_RXD. 1: Enables data reception through BBIF2_RXD. [Read data] 0: Data is not received through BBIF2_RXD. 1: Data can be received through BBIF2_RXD.
7 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
1	TXRST	0	R/W	Transmit Reset When value 1 set to this bit becomes valid, the BBIF2 immediately sets transmit data through the BBIF2_TXD pin to 0, and initializes the transmit data registers and transmit-related status. When value 1 set to this bit becomes valid with PCON = 1, the RXRST bit is also becomes valid. The following registers and bits are initialized. • SITDR1 and SITDR2 • SITFDR • Transmit FIFO write pointer • TCRDY, TFEMP, and TDREQ bits in SISTR • TXE bit This bit is read as 1 until the reset operation is completed for about SUBϕ20 cycles. No data should be written to SICTR or the transmit FIFO during this time period. [Write data] 0: Does not reset transmit operation. 1: Resets transmit operation. [Read data] 0: Transmit operation reset is completed. 1: Transmit operation is being reset.

Bit	Bit Name	Initial Value	R/W	Descriptions
0	RXRST	0	R/W	Receive Reset When value 1 set to this bit becomes valid, the BBIF2 immediately disables reception through the BBIF2_RXD pin, and initializes the receive data registers and receive-related status. The following registers and bits are initialized. • SIRDR1 and SIRDR2 • SIRFDR • Receive FIFO read pointer • RCRDY, RFFUL, and RDREQ bits in SISTR • RXE bit This bit is read as 1 until the reset operation is completed for about SUBϕ20 cycles. No data should be written to SICTR or read the receive FIFO during this time period. [Write data] 0: Does not reset receive operation. 1: Resets receive operation. [Read data] 0: Receive operation reset is completed. 1: Receive operation is being reset.

25.3.8 Transmit Clock Select Register (SITSCR)

SITSCR is a 16-bit readable/writable register that specifies the conditions for generating the transmit serial clock in master mode. SITSCR can be specified when the TRMD bit in SITMDR1 is set to B'1.



Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSSEL[1:0]		MSIMM	BRPS[4:0]					—	—	—	—	—	BRDV[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
15, 14	MSSEL[1:0]	00	R/W	Master Clock Source Select The master clock is the clock input to the baud rate generator. 00: Selects SUBCKϕ as the master clock. 01: Selects FSIϕ as the master clock. 10: Selects FMSOϕ as the master clock. 11: Setting prohibited
13	MSIMM	0	R/W	Master Clock Direct Select 0: Selects the clock output from the baud rate generator as the serial clock. 1: Selects the master clock itself as the serial clock. To set MSIMM = 1, set the master clock source to 24 MHz or less.
12 to 8	BRPS[4:0]	00000	R/W	Prescalar Setting These bits specify the master clock division ratio in the count value of the prescalar in the baud rate generator. The specifiable value is from B'00000 (× 1/1) to B'11111 (× 1/32).
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
2 to 0	BRDV[2:0]	000	R/W	Baud Rate Generator's Division Ratio These bits specify the frequency division ratio for the output stage of the baud rate generator. The final frequency division ratio of the baud rate generator is determined as BRPS × BRDV (1/1024 max.). 000: Prescalar output × 1/2 001: Prescalar output × 1/4 010: Prescalar output × 1/8 011: Prescalar output × 1/16 100: Prescalar output × 1/32 101: Setting prohibited 110: Setting prohibited 111: Prescalar output × 1/1 Note: 111 is valid only when the BRPS[4:0] bits are set to 00000 or 00001.

25.3.9 Transmit Control Data Register 1 (SITDR1)

SITDR1 is a 32-bit readable/writable register that specifies the transmit control data of the BBIF2.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TCRD1[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TCRD2[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 16	TCRD1[15:0]	H'0000	W	• When one or two groups are used: These bits specify the transmit control data for the upper 16 bits of a word in group 1. • When three or four groups are used: These bits specify the transmit control data for a word in group 1.
15 to 0	TCRD2[15:0]	H'0000	W	• When one or two groups are used: These bits specify the transmit control data for the lower 16 bits of a word in group 1 when the word size is larger than 16 bits. • When three or four groups are used: These bits specify the transmit control data for a word in group 3.

25.3.10 Transmit Control Data Register 2 (SITDR2)

SITDR2 is a 32-bit readable/writable register that specifies the transmit control data of the BBIF2.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TCRD3[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TCRD4[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 16	TCRD3[15:0]	H'0000	W	• When one or two groups are used: These bits specify the transmit control data for the upper 16 bits of a word in group 2. • When three or four groups are used: These bits specify the transmit control data for a word in group 2.
15 to 0	TCRD4[15:0]	H'0000	W	• When one or two groups are used: These bits specify the transmit control data for the lower 16 bits of a word in group 2 when the word size is larger than 16 bits. • When three or four groups are used: These bits specify the transmit control data for a word in group 4.

25.3.11 Transmit FIFO Data Register (SITFDR)

SITFDR is a 32-bit write-only register that specifies the transmit FIFO data of the BBIF2.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SITFD1[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SITFD2[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 16	SITFD1[15:0]	H'0000	W	These bits specify the upper 16 bits of the FIFO data to be output through BBIF2_TXD.
15 to 0	SITFD2[15:0]	H'0000	W	These bits specify the lower 16 bits of the FIFO data to be output through BBIF2_TXD.

25.3.12 Receive Control Data Register 1 (SIRDR1)

SIRDR1 is a 32-bit read-only register that stores the receive control data of the BBIF2.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RCRD1[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RCRD2[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 16	RCRD1[15:0]	H'0000	R	• When one or two groups are used: Store the receive control data for the upper 16 bits of a word in group 1. • When three or four groups are used: Store the receive control data for a word in group 1.
15 to 0	RCRD2[15:0]	H'0000	R	• When one or two groups are used: Store the receive control data for the lower 16 bits of a word in group 1 when the word size is larger than 16 bits. • When three or four groups are used: Store the receive control data for a word in group 3.

25.3.13 Receive Control Data Register 2 (SIRDR2)

SIRDR2 is a 32-bit read-only register that stores the receive control data of the BBIF2.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RCRD3[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RCRD4[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 16	RCRD3[15:0]	H'0000	R	• When one or two groups are used: Store the receive control data for the upper 16 bits of a word in group 2. • When three or four groups are used: Store the receive control data for a word in group 2.
15 to 0	RCRD4[15:0]	H'0000	R	• When one or two groups are used: Store the receive control data for the lower 16 bits of a word in group 2 when the word size is larger than 16 bits. • When three or four groups are used: Store the receive control data for a word in group 4.

25.3.14 Receive FIFO Data Register (SIRFDR)

SIRFDR is a 32-bit read-only register that stores the receive FIFO data of the BBIF2.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SIRFD1[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SIRFD2[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 16	SIRFD1[15:0]	H'00	R	Store the upper 16 bits of the FIFO data received through BBIF2_RXD.
15 to 0	SIRFD2[15:0]	H'00	R	Store the lower 16 bits of the FIFO data received through BBIF2_RXD.

25.3.15 Status Register (SISTR)

Each bit in SISTR becomes a BBIF2 interrupt source when the corresponding bit in SIIER is set to 1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	TCRDY	TFEMP	TDREQ	—	—	—	—	TEOF	—	TFSERR	TFOVF	TFUDF	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R	R	R	R	R	R/W	R	R/W	R/W	R/W	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	RCRDY	RFFUL	RDREQ	—	—	—	—	REOF	—	RFSERR	RFUDF	RFOVF	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R	R	R	R	R	R/W	R	R/W	R/W	R/W	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
30	TCRDY	0	R/W	Transmit Control Data Ready If SITDR1 or SITDR2 is written while this bit is cleared to 0, SICTR is overwritten and the previous contents are not output through the BBIF2_TXD pin. This bit is valid when the TXE bit in SICTR is 1. When this bit is set to 1, the content is cleared. Writing 0 to this bit is invalid. If the interrupt request from this bit is enabled, a BBIF2 interrupt is issued. 0: SITDR1 and SITDR2 are not ready to be written. 1: SITDR1 and SITDR2 are ready to be written.

Bit	Bit Name	Initial Value	R/W	Descriptions
29	TFEMP	0	R/W	Transmit FIFO Empty This bit is valid when the TXE bit in SICTR is 1. When this bit is set to 1, the content is cleared. Writing 0 to this bit is invalid. If the interrupt request from this bit is enabled, a BBIF2 interrupt is issued. 0: Transmit FIFO is not empty. 1: Transmit FIFO is empty.
28	TDREQ	0	R	Transmit Data Transfer Request A transmit data transfer request is issued when the empty space in the transmit FIFO exceeds the size specified by the TFWM bits in SIFCTR. When transferring transmit data through the DMAC, this bit is always cleared after one DMAC access. After DMAC access, when the conditions for setting this bit are satisfied, the BBIF2 again sets this bit to 1. This bit is valid when the TXE bit in SICTR is 1. This bit indicates a state; if the size of empty space in the transmit FIFO becomes less than the size specified by the TFWM bits in SIFCTR, the BBIF2 clears this bit. If the interrupt request from this bit is enabled, a BBIF2 interrupt is issued. However, when the TDMAE bit is 1, only a DMAC transfer request is issued. 0: The size of empty space in the transmit FIFO has not exceeded the size specified by the TFWM bits in SIFCTR. 1: The size of empty space in the transmit FIFO has exceeded the size specified by the TFWM bits in SIFCTR.
27 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
23	TEOF	0	R/W	Frame Transmission End The BBIF2 issues the frame transmission end flag upon completion of one-frame data transmission. This bit is valid when the TXE bit in SICTR is 1. When this bit is set to 1, the content is cleared. Writing 0 to this bit is invalid. If the interrupt request from this bit is enabled, a BBIF2 interrupt is issued. 0: One-frame transmission end is not detected. 1: One-frame transmission end is detected.
22	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
21	TFSERR	0	R/W	Transmit Frame Synchronization Error A transmit frame synchronization error occurs when the next transmit frame synchronization timing arrives before the previous data or control data transmission has been completed. If a transmit frame synchronization error occurs, the BBIF2 performs transmission only for the slots that can be transferred. This bit is valid when the TXE bit in SICTR is 1. When 1 is written to this bit, it is cleared. Writing 0 to this bit is invalid. If the interrupt request from this bit is enabled, a BBIF2 interrupt is issued. 0: No transmit frame synchronization error has occurred. 1: A transmit frame synchronization error has occurred.

Bit	Bit Name	Initial Value	R/W	Descriptions
20	TFOVF	0	R/W	Transmit FIFO Overflow A transmit FIFO overflow means that there has been an attempt to write to SITFDR when the transmit FIFO is full. If a transmit FIFO overflow occurs, the BBIF2 ignores the write operation causing the overflow. This bit is valid when the TXE bit in SICTR is 1. When 1 is written to this bit, it is cleared. Writing 0 to this bit is invalid. If the interrupt request from this bit is enabled, a BBIF2 interrupt is issued. 0: No transmit FIFO overflow has occurred. 1: A transmit FIFO overflow has occurred.
19	TFUDF	0	R/W	Transmit FIFO Underflow A transmit FIFO underflow means that loading for transmission has occurred when the transmit FIFO is empty. This bit is valid when the TXE bit in SICTR is 1. When 1 is written to this bit, it is cleared. Writing 0 to this bit is invalid. If the interrupt request from this bit is enabled, a BBIF2 interrupt is issued. 0: No transmit FIFO underflow has occurred. 1: A transmit FIFO underflow has occurred.
18 to 15	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
14	RCRDY	0	R/W	Receive Control Data Ready When data different from the previous data is stored during reception of control data, this bit is set to 1 indicating that valid data was written. When the first data that is not 0 is stored, this bit is set to 1. If valid data is written to SIRDR1 or SIRDR2 when this bit is set to 1, SIRDR1 or SIRDR2 is overwritten with the latest data. This bit is valid when the RXE bit in SICTR is 1. When this bit is set to 1, the content is cleared. Writing 0 to this bit is invalid. If the interrupt request from this bit is enabled, a BBIF2 interrupt is issued. 0: SIRDR1 and SIRDR2 store no valid data. 1: SIRDR1 and SIRDR2 store valid data.
13	RFFUL	0	R/W	Receive FIFO Full This bit is valid when the RXE bit in SICTR is 1. When this bit is set to 1, the content is cleared. Writing 0 to this bit is invalid. If the interrupt request from this bit is enabled, a BBIF2 interrupt is issued. 0: Receive FIFO is not full. 1: Receive FIFO is full.

Bit	Bit Name	Initial Value	R/W	Descriptions
12	RDREQ	0	R	Receive Data Transfer Request A receive data transfer request is issued when the valid data space in the receive FIFO exceeds the size specified by the RFWM bits in SIFCTR. When transferring transmit data through the DMAC, this bit is always cleared by one DMAC access. After DMAC access, when the conditions for setting this bit are satisfied, the BBIF2 again sets this bit to 1. This bit is valid when the RXE bit in SICTR is 1. This bit indicates a state; if the size of valid data space in the receive FIFO becomes less than the size specified by the RFWM bits in SIFCTR, the BBIF2 clears this bit. If the interrupt request from this bit is enabled, a BBIF2 interrupt is issued. However, when the RDMAE bit is 1, only a DMAC transfer request is issued. 0: The size of valid data space in the receive FIFO has not exceeded the size specified by the RFWM bits in SIFCTR. 1: The size of valid data space in the receive FIFO has exceeded the size specified by the RFWM bits in SIFCTR.
11 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	REOF	0	R/W	Frame Reception End The BBIF2 issues the frame reception end flag upon completion of one-frame data reception. This bit is valid when the RXE bit in SICTR is 1. When this bit is set to 1, the content is cleared. Writing 0 to this bit is invalid. If the interrupt request from this bit is enabled, a BBIF2 interrupt is issued. 0: One-frame reception end is not detected. 1: One-frame reception end is detected.

Bit	Bit Name	Initial Value	R/W	Descriptions
6	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
5	RFSERR	0	R/W	Receive Frame Synchronization Error A receive frame synchronization error occurs when the next receive frame synchronization timing arrives before the previous data or control data reception has been completed. If a receive frame synchronization error occurs, the BBIF2 performs reception only for the slots that can be transferred. This bit is valid when the RXE bit in SICTR is 1. When 1 is written to this bit, it is cleared. Writing 0 to this bit is invalid. If the interrupt request from this bit is enabled, a BBIF2 interrupt is issued. 0: No receive frame synchronization error has occurred. 1: A receive frame synchronization error has occurred.
4	RFUDF	0	R/W	Receive FIFO Underflow A receive FIFO underflow means that reading of SIRFDR has occurred when the receive FIFO is empty. If a receive FIFO underflow occurs, the value read from SIRFDR is not guaranteed. This bit is valid when the RXE bit in SICTR is 1. When 1 is written to this bit, it is cleared. Writing 0 to this bit is invalid. If the interrupt request from this bit is enabled, a BBIF2 interrupt is issued. 0: No receive FIFO underflow has occurred. 1: A receive FIFO underflow has occurred.

Bit	Bit Name	Initial Value	R/W	Descriptions
3	RFOVF	0	R/W	Receive FIFO Overflow A receive FIFO overflow means that writing has been caused by receiving operation when the receive FIFO is full. If a receive FIFO overflow occurs, the receive data causing the overflow is lost. This bit is valid when the RXE bit in SICTR is 1. When 1 is written to this bit, it is cleared. Writing 0 to this bit is invalid. If the interrupt request from this bit is enabled, a BBIF2 interrupt is issued. 0: No receive FIFO overflow has occurred. 1: A receive FIFO overflow has occurred.
2 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

25.3.16 Interrupt Enable Register (SIIER)

SIIER is a 32-bit readable/writable register that enables the issue of BBIF2 interrupts. When each bit in this register is set to 1 and the corresponding bit in SISTR is set to 1, the BBIF2 issues an interrupt.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TDMAE	TCRDYE	TFEMPE	TDREQE	—	—	—	—	TEOFE	—	TFSERRE	TFOVFE	TFUDFE	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R	R/W	R/W	R/W	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RDMAE	RCRDYE	RFFULE	RDREQE	—	—	—	—	REOFE	—	RFSERRE	RFUDFE	RFOVFE	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R	R/W	R/W	R/W	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31	TDMAE	0	R/W	Transmit Data DMA Transfer Request Enable Specifies whether to send an interrupt as an interrupt request to the CPU or a transfer request to the DMAC. The TDREQE bit can be set as the request source. 0: Sends an interrupt request to the CPU. 1: Sends a DMA transfer request to the DMAC.
30	TCRDYE	0	R/W	Transmit Control Data Ready Enable 0: Disables interrupts due to transmit control data ready. 1: Enables interrupts due to transmit control data ready.
29	TFEMPE	0	R/W	Transmit FIFO Empty Enable 0: Disables interrupts due to transmit FIFO empty. 1: Enables interrupts due to transmit FIFO empty.
28	TDREQE	0	R/W	Transmit Data Transfer Request Enable 0: Disables interrupts due to transmit data transfer requests. 1: Enables interrupts due to transmit data transfer requests.

Bit	Bit Name	Initial Value	R/W	Descriptions
27 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23	TEOFE	0	R/W	Frame Transmission End Enable 0: Disables a frame transmission end interrupt. 1: Enables a frame transmission end interrupt.
22	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
21	TFSERRE	0	R/W	Transmit Frame Synchronization Error Enable 0: Disables interrupts due to transmit frame synchronization errors. 1: Enables interrupts due to transmit frame synchronization errors.
20	TFOVFE	0	R/W	Transmit FIFO Overflow Enable 0: Disables interrupts due to transmit FIFO overflow 1: Enables interrupts due to transmit FIFO overflow
19	TFUDFE	0	R/W	Transmit FIFO Underflow Enable 0: Disables interrupts due to transmit FIFO underflow. 1: Enables interrupts due to transmit FIFO underflow.
18 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	RDMAE	0	R/W	Receive Data DMA Transfer Request Enable Specifies whether to send an interrupt as an interrupt request to the CPU or a transfer request to the DMAC. The RDREQE bit can be set as the request source. 0: Sends an interrupt request to the CPU. 1: Sends a DMA transfer request to the DMAC.

Bit	Bit Name	Initial Value	R/W	Descriptions
14	RCRDYE	0	R/W	Receive Control Data Ready Enable 0: Disables interrupts due to receive control data ready. 1: Enables interrupts due to receive control data ready.
13	RFFULE	0	R/W	Receive FIFO Full Enable 0: Disables interrupts due to receive FIFO full. 1: Enables interrupts due to receive FIFO full.
12	RDREQE	0	R/W	Receive Data Transfer Request Enable 0: Disables interrupts due to receive data transfer requests. 1: Enables interrupts due to receive data transfer requests.
11 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	REOFE	0	R/W	Frame Reception End Enable 0: Disables a frame reception end interrupt. 1: Enables a frame reception end interrupt.
6	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
5	RFSERRE	0	R/W	Receive Frame Synchronization Error Enable 0: Disables interrupts due to receive frame synchronization errors. 1: Enables interrupts due to receive frame synchronization errors.
4	RFUDFE	0	R/W	Receive FIFO Underflow Enable 0: Disables interrupts due to receive FIFO underflow. 1: Enables interrupts due to receive FIFO underflow.

Bit	Bit Name	Initial Value	R/W	Descriptions
3	RFOVFE	0	R/W	Receive FIFO Overflow Enable 0: Disables interrupts due to receive FIFO overflow. 1: Enables interrupts due to receive FIFO overflow.
2 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

25.3.17 FIFO Control Register (SIFCTR)

SIFCTR is a 32-bit readable/writable register that indicates the area available for the transmit/receive FIFO transfer.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TFWM[2:0]			—	—	TFUA[6:0]							—	—	—	—
Initial value:	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RFWM[2:0]			RFUA[8:0]									—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 29	TFWM[2:0]	0	R/W	Transmit FIFO Watermark A transfer request of the transmit FIFO is issued by the TDREQE bit in SIIER. The transmit FIFO always operates as a 64-stage FIFO regardless of these bit settings. 000: Issues a transfer request when 64 stages of the transmit FIFO are empty. 001: Issues a transfer request when 32 or more stages of the transmit FIFO are empty. 010: Issues a transfer request when 24 or more stages of the transmit FIFO are empty. 011: Issues a transfer request when 16 or more stages of the transmit FIFO are empty. 100: Issues a transfer request when 12 or more stages of the transmit FIFO are empty. 101: Issues a transfer request when 8 or more stages of the transmit FIFO are empty. 110: Issues a transfer request when 4 or more stages of the transmit FIFO are empty. 111: Issues a transfer request when 1 or more stages of transmit FIFO are empty.
28 to 27	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
26 to 20	TFUA[6:0]	H'40	R	Transmit FIFO Usable Area Indicate the number of words that can be transferred by the CPU or DMAC as B'0000000 (full) to B'1000000 (empty).
19 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
15 to 13	RFWM[2:0]	000	R/W	Receive FIFO Watermark A transfer request of the receive FIFO is issued by the RDREQE bit in SIIER. The receive FIFO always operates as a 256-stage FIFO regardless of these bit settings. 000: Issues a transfer request when 1 stage or more of the receive FIFO are valid. 001: Issues a transfer request when 4 or more stages of the receive FIFO are valid. 010: Issues a transfer request when 8 or more stages of the receive FIFO are valid. 011: Issues a transfer request when 16 or more stages of the receive FIFO are valid. 100: Issues a transfer request when 32 or more stages of the receive FIFO are valid. 101: Issues a transfer request when 64 or more stages of the receive FIFO are valid. 110: Issues a transfer request when 128 or more stages of the receive FIFO are valid. 111: Issues a transfer request when 256 stages of the receive FIFO are valid.
12 to 4	RFUA[8:0]	H'000	R	Receive FIFO Usable Area Indicate the number of words that can be transferred by the CPU or DMAC as B'000000000 (empty) to B'100000000 (full).
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

25.4 Operation

25.4.1 Operating Mode

(a) Common Transmit/Receive Mode

BBIF2 uses common clock and frame synchronization signals for transmission and reception.

Master mode: BBIF2_TSCK (BBIF2_SCK) and BBIF2_TSYNC (BBIF2_SYNC) are output.

Slave mode: BBIF2_TSCK (BBIF2_SCK) and BBIF2_TSYNC (BBIF2_SYNC) are input.

25.4.2 Serial Clocks

(a) Clock Output in Master Mode

In master mode, the baud rate generator is used to generate the serial clock. The division ratio is from 1/1 to 1/1024.

(b) Clock Input in Slave Mode

In slave mode, the clock input for transmission and reception is used as the serial clock.

(c) Multiple Channel Function

This module provides the multiple channel function as shown in figure 25.2.

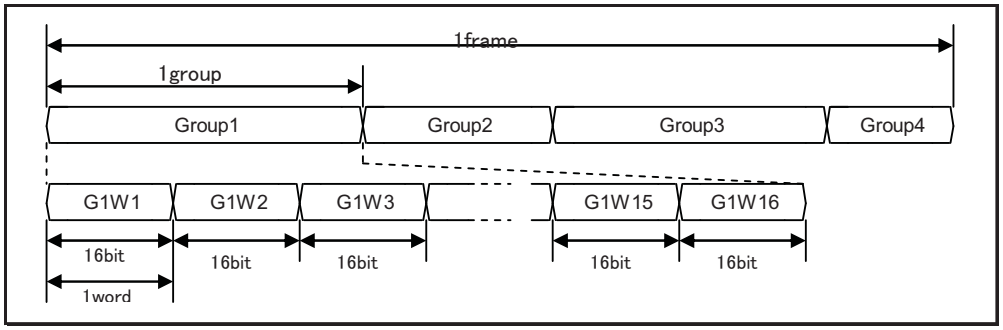


Figure 25.2 Multiple Channel Structure

The following conditions can be specified for the multiple channel function.

- Up to four groups in one frame
- Up to 256 words in one group
- Eight bits to 32 bits in one word
- Up to three blank bits can be inserted between groups

Note the following limitations by the number of groups.

Table 25.4 Maximum Word Size and Group Size Limited by Number of Groups

Number of Groups	Maximum Word Size	Maximum Group Size
One or two	32 bits	256 words
Three or four	16 bits	16 words

25.4.3 Serial Timing

(a) BBIF2_SYNC

The BBIF2_SYNC is a frame synchronization signal. The following four transfer modes are available.

- Frame start synchronization pulse: 1-bit-width pulse indicating the start of a frame
- Last bit synchronization pulse: 1-bit-width pulse indicating the last bit in a word
- Level/SPI: Level signal asserted during frame transmission
- L/R: 1/2-frame-width pulse indicating the first-half groups in a high level and the last-half groups in a low level

Figure 25.3 to 25.6 show the BBIF2_SYNC synchronization timing in these modes.

- Frame Start Synchronization Pulse

The rising edge of the synchronization pulse indicates the start of a frame.

The delay between the rising edge of the synchronization signal and the start of data transmission or reception can be specified with the DTDL bits. The width of the synchronization pulse can be extended through the SYNCDL bit setting.

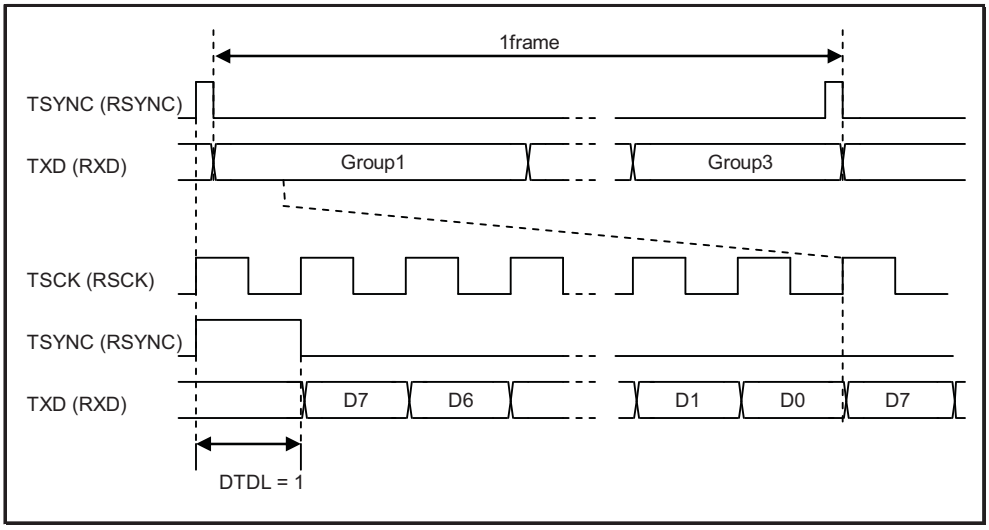


Figure 25.3 Synchronization Timing in Start Frame Synchronization Pulse Mode

- Last Bit Synchronization Pulse

The rising edge of the synchronization pulse indicates the last bit of each word.

The delay between the last bit of a word and the synchronization pulse can be specified with the DTDL bits.

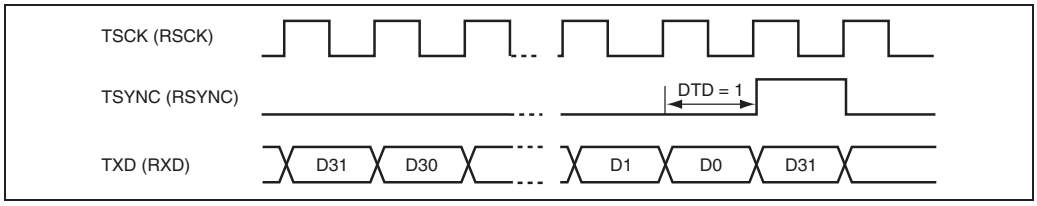


Figure 25.4 Synchronization Timing in Last Bit Synchronization Pulse Mode

- Level Synchronization

The synchronization signal is driven high for the frame length.

The delay between the rising edge of the synchronization signal and the start of transmission or reception can be specified with the DTDL bits and the delay between the end of transmission or reception and the falling edge of the synchronization signal can be specified with the SYNCDL bits (DTDL = 0 to 2 and SYNCDL = 0 to 3). This mode is available for the SPI master or slave operation.

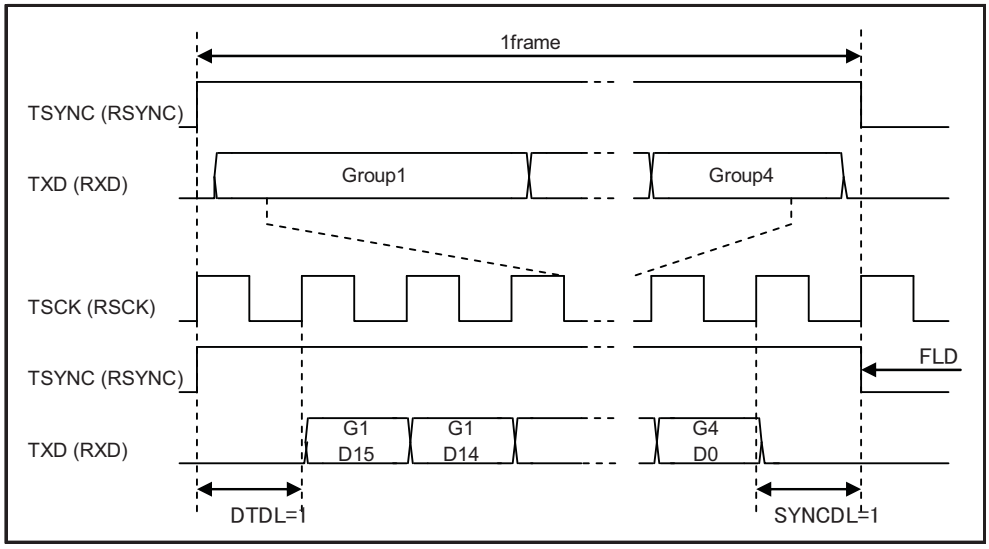


Figure 25.5 Synchronization Timing in Level Synchronization Mode

- L/R Synchronization

A high level in the synchronization signal indicates the first-half groups and a low level indicates the last-half groups.

The delay between the rising or falling edge of the synchronization signal and the start of transmission or reception can be specified with the DTDL bits and the delay between the end of transmission or reception and the rising or falling edge of the synchronization signal can be specified with the SYNCDL bits (DTDL = 0 to 2 and SYNCDL = 0 to 3).

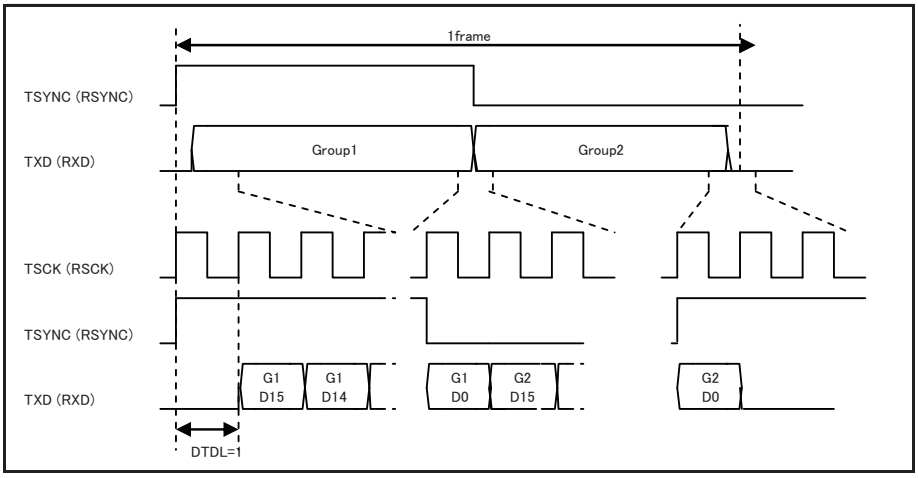


Figure 25.6 Synchronization Timing in L/R Synchronization Mode

(b) Transmit/Receive Timing

The BBIF2_TXD transmit timing and BBIF2_RXD receive timing relative to the BBIF2_TSCK and BBIF2_SCK can be specified as the sampling timing in the following two ways through the TEDG and REDG bits in SIMDR.

- Rising-edge sampling
- Falling-edge sampling

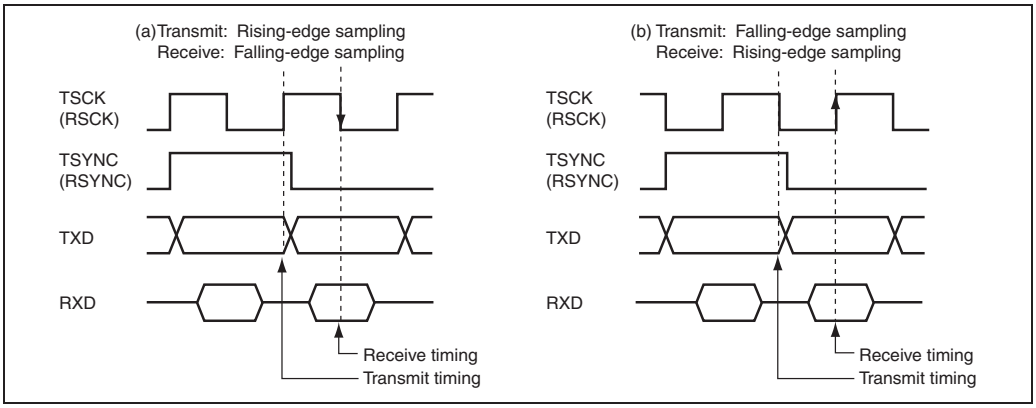


Figure 25.7 Transmit/Receive Timing

25.4.4 Control Data Interface

For the groups specified with the CRDE bits in SITMDR2 and SIRMDR2, data is not stored in the FIFOs but handled as control data to be stored in SITDR1/SITDR2 and SIRDR1/SIRDR2.

Control data is transferred in the following two ways, which can be selected through the CRDNUM bits in SITMDR2 and SIRMDR2, as shown in Figure 25.8.

- Only the first word in the group is transferred as valid data.
- All words in the group is transferred as valid data.

For the invalid data period during transmission, the value specified in the TXDIZ bit is output. The invalid receive data is not stored in SIRDR1 or SIRDR2.

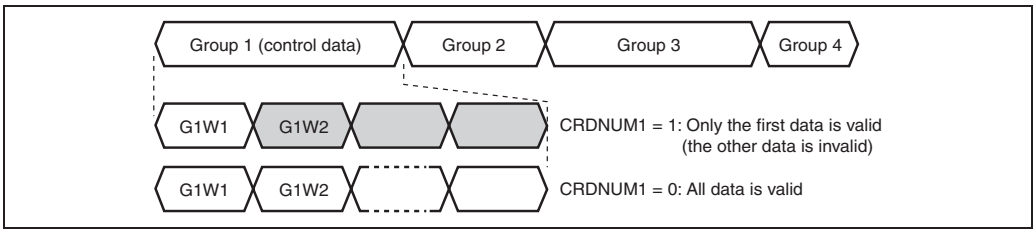


Figure 25.8 Control Data Allocation

25.4.5 Transfer Data Allocation to Registers

(1) Transmit/Receive Data

Transmit/receive data (FIFO data and control data) should be written to or read from the following registers.

- Writing of transmit FIFO data: SITFDR (32/16-bit access)
- Writing of control data: SITDR1 and SITDR2 (32/16-bit access)
- Reading of receive FIFO data: SIRFDR (32/16-bit access)
- Reading of control data: SIRDR1 and SIRDR2 (32/16-bit access)

When making a 16-bit access, only upper 16 bits of FIFO data is accessible. However, both upper 16 bits and lower 16 bits of control data are accessible.

When the word size is smaller than the transmit FIFO data access size, the upper bits are transmitted as valid data. For example, when writing data to the transmit FIFO by 32-bit access and transmitting a16-bit word, the upper 16 bits are transmitted and the lower 16 bits are discarded as invalid data.

In the same way, when the word size is larger than the receive FIFO data access size, the upper bits are received as valid data. For example, when 32-bit data is stored in the receive FIFO and the data is read by 16-bit access, the lower 16 bits are discarded as invalid data.

Figure 25.9 shows the bit alignment of these registers.

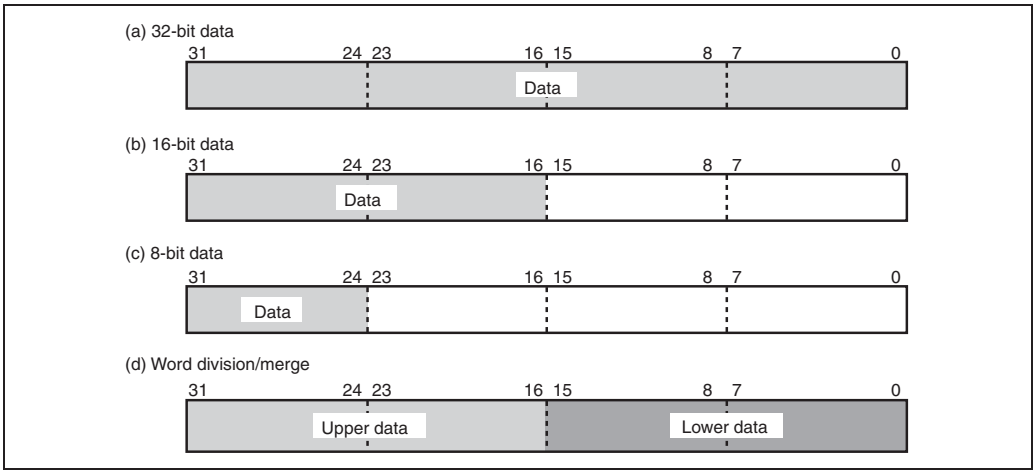


Figure 25.9 Transmit/Receive Data Bit Alignment

25.4.6 FIFO

(a) Overview

The transmit and receive FIFOs of the BBIF2 have the following features.

- 32 bits × 64 stages for transmission and 32 bits × 256 stages for reception
- The FIFO pointer is updated in one read or write cycle regardless of the access size of the CPU or DMAC. (One access cannot be divided into multiple accesses.)

(b) Transfer Request

A request for FIFO data transfer can be issued to the CPU or DMAC as the following interrupt sources.

- FIFO transmit request: TDREQ (interrupt source for transmission)
- FIFO receive request: RDREQ (interrupt source for reception)

The conditions for requesting FIFO data transfer can be specified separately for transmission and reception. The conditions for the transmit FIFO and receive FIFO are specified in the TFWM[2:0] bits and RFWM[2:0] bits in SIFCTR, respectively.

Table 25.5 Condition for Issuing Transmit Request

TFWM[2:0]	Number of Requested Stages	Condition for Transmit Request	Areas Used
000	1	64 stages of empty area	Smallest
001	32	32 or more stages of empty area	
010	40	24 or more stages of empty area	
011	48	16 or more stages of empty area	
100	52	12 or more stages of empty area	
101	56	8 or more stages of empty area	
110	60	4 or more stages of empty area	
111	64	1 or more stages of empty area	Largest

Table 25.6 Condition for Issuing Receive Request

RFWM[2:0]	Number of Requested Stages	Condition for Receive Request	Areas Used
000	1	1 or more stages of valid data	Smallest
001	4	4 or more stages of valid data	
010	8	8 or more stages of valid data	
011	16	16 or more stages of valid data	
100	32	32 or more stages of valid data	
101	64	64 or more stages of valid data	
110	128	128 or more stages of valid data	
111	256	256 stages of valid data	Largest

The maximum FIFO stages are always available even if the data area or empty area exceeds the size specified for the transfer condition. Accordingly, an overflow error or an underflow error occurs if the data area or empty area exceeds the maximum number of FIFO stages.

The FIFO transfer request is canceled when the specified condition is not satisfied even if the FIFO does not become empty or full.

(c) Number of FIFOs

The number of transmit and receive FIFO stages used are indicated by the following registers.

- Transmit FIFO: The number of empty FIFO stages is indicated by the TFUA[6:0] bits in SIFCTR.
- Receive FIFO: The number of valid data stages is indicated by the RFUA[8:0] bits in SIFCTR.

These registers show the number of data stages that can be transferred by the CPU or DMAC.

25.4.7 Transmit and Receive Procedures

(a) Transmission in Master Mode

Figure 25.10 shows an example of settings and operation for transmission in master mode.

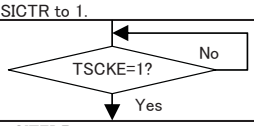
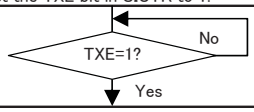
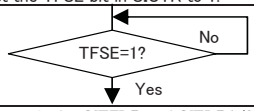
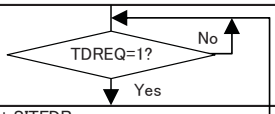
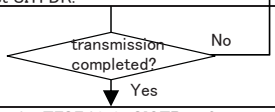
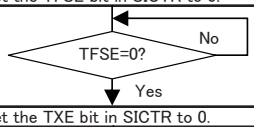
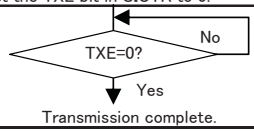
No.	Flow chart	Setting	operation
1	Set SITMDR1/2/3 SITSCR , SIFCTR , and SIIER.	Set the operating mode, serial clock , and FIFO threshold value, and enable interrupts.	
2	Set the TSCKE bit in SICTR to 1.	Set output sampling and start the baud rate generator.	Outputs the serial clock.
3		Read 1 from TSCKE bit in SICTR.	
4	Set SITFDR, SITDR1/2.	Set transmit data.	
5	Set the TXE bit in SICTR to 1.	Enable transmittion.	
6		Read 1 from TXE bit in SICTR.	
7	Set the TFSE bit in SICTR to 1.	Starting output frame of synchronization signal.	Outputs the frame syncronization signal.
8		Read 1 from TFSE bit in SICTR.	
9	Transmit the SITFDR and SITDR1/2 contents through TXD in synchronization with		Transmit data.
10			Assert transmit data transfer request according to the FIFO threshold valu
11	Set SITFDR.	Set transfer data.	
12		Read 1 from TFEMP bit in SICTR.	
13	Set the TFSE bit in SICTR to 0.	Disable output frame of synchronization signal.	
14		Read 0 from TFSE bit in SICTR.	
15	Set the TXE bit in SICTR to 0.	Disable transmit enable.	
16	 Transmission complete.	Read 0 from TXE bit in SICTR.	

Figure 25.10 Example of Transmit Procedure in Master Mode

(b) Transmission in Slave Mode

Figure 25.11 shows an example of settings and operation for transmission in slave mode.

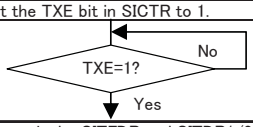
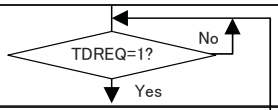
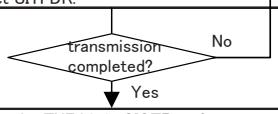
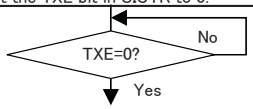
No.	Flow chart	Setting	operation
1	Setting master device polarity	Depend on master device.	Decide SYNC/SCK polarity
2	Set SITMDR1/2/3 SIFCTR and SIIER.	Set operating mode FIFO threshold value and enable interrupts.	
3	Set SITFDR, SITDR1/2.	Set transmit data.	
4	Set the TXE bit in SICTR to 1.	Enable transmittion.	
5		Read 1 from TXE bit in SICTR.	
6	Transmit the SITFDR and SITDR1/2 contents through TXD in synchronization with		Transmit data
7			Assert transmit data transfer request according to the FIFO threshold valu
8	Set SITFDR.	Set transfer data.	
9			
10	Set the TXE bit in SICTR to 0.	Disable transmit enable.	
11	 Transmission complete.	Read 0 from TXE bit in SICTR.	

Figure 25.11 Example of Transmit Procedure in Slave Mode

(c) Reception in Slave Mode

Figure 25.12 shows an example of settings and operation for reception in slave mode.

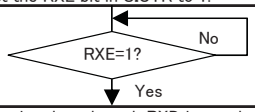
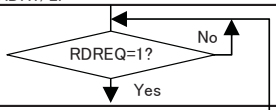
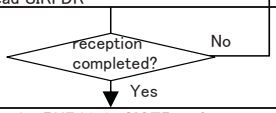
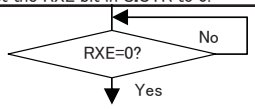
No.	Flow chart	Setting	operation
1	Setting master device polarity	Depend on master device.	Decide SYNC/SCK polarity
2	Set SIRMDR1/2/3 SIFCTR and SIIER.	Set operating mode FIFO threshold value and enable interrupts.	
3	Set the RXE bit in SICTR to 1.	Enable reception.	
4		Read 1 from RXE bit in SICTR.	
5	Receive data through RXD in synchronization with MSIOF_RSYNC and store it in SIRFDR and SIRDR1/2.		Receive data
6			Assert reception data transfer request according to the FIFO threshold valu
7	Read SIRFDR	Read reception data.	
8			
9	Set the RXE bit in SICTR to 0.	Disable reception enable	
10	 Reception complete.	Read 0 from RXE bit in SICTR.	

Figure 25.12 Example of Receive Procedure in Slave Mode

(d) Reset

After a power-on reset is applied, module stop state is canceled, or a reset signal is asserted through the TXRST or RXRST setting in SICTR, it takes about SUBϕ20 cycles to complete the internal reset of the module. During a period from the beginning of reset until the TXRST or RXRST value is read as 0, do not modify the control register or access the FIFOs.

The BBIF2 can separately reset the transmit and receive units by setting the following bits to 1.

- Transmit reset: TXRST bit in SICTR
- Receive reset: RXRST bit in SICTR

Table 25.7 Transmit and Receive Reset

Type	Objects Initialized
Transmit reset	SITDR1, SITDR2, and SITFDR
	Transmit FIFO write pointer
	TCRDY, TFEMP, and TDREQ bits in SISTR
	TXE bit in SICTR
Receive reset	SIRDR1, SIRDR2, and SIRFDR
	Receive FIFO read pointer
	RCRDY, RFFUL, and RDREQ bits in SISTR
	RXE bit in SICTR

(e) Initial Operating Mode

After a power-on reset, both the transmit and receive units are initialized to master mode (0 is output through CLK and SYNC). When using slave mode, keep the connected device outputting 0 until the operating mode setting is completed.

25.4.8 Interrupts

The BBIF2 has one type of interrupt.

(a) Interrupt Sources

Interrupts can be generated by several sources. Each source is shown as a BBIF2 status in SISTR. Table 25.8lists the BBIF2 interrupt sources.

Table 25.8 BBIF2 Interrupt Sources

No.	Classification	Bit Name	Function Name	Description
1	Transmission	TDREQ	Transmit FIFO transfer request	The transmit FIFO has empty space of specified size or more.
2		TFEMP	Transmit FIFO empty	The transmit FIFO is empty.
3		TEOF	Frame transmission end	Transmission of data with a length of one frame is completed.
4	Reception	RDREQ	Receive FIFO transfer request	The receive FIFO stores data of specified size or more.
5		RFFUL	Receive FIFO full	The receive FIFO is full.
6		REOF	Frame reception end	Reception of data with a length of one frame is completed.
7	Control	TCRDY	Transmit control data ready	The transmit control data register is ready to be written.
8		RCRDY	Receive control data ready	The receive control data register stores valid data.
9	Error	TFUDF	Transmit FIFO underflow	Serial data transmit timing has arrived while the transmit FIFO is empty.
10		TFOVF	Transmit FIFO overflow	The transmit FIFO is written to while it is full.
11		RFOVF	Receive FIFO overflow	Serial data is received while the receive FIFO is full.
12		RFUDF	Receive FIFO underflow	The receive FIFO is read while the receive FIFO is empty.
13		TFSERR	Transmit FS error	A transmit frame synchronization signal is input before the specified number of bits has been reached (in slave mode).
14		RFSERR	Receive FS error	A receive frame synchronization signal is input before the specified number of bits has been reached (in slave mode).

Whether an interrupt is issued from an interrupt source is determined by the SIIER settings. If an interrupt source bit is set to 1 and the corresponding bit in SIIER is set to 1, a BBIF2 interrupt is issued.

(b) TDREQ and RDREQ

The transmit FIFO transfer request (TDREQ) and receive FIFO transfer request (RDREQ) are signals indicating the state. If the state changes after TDREQ or RDREQ is set, it is automatically cleared by the BBIF2.

When the DMA transfer is used, a DMA transfer request signal is pulled low for one cycle at the end of DMA transfer.

(c) Processing when Errors Occur

- Transmit FIFO underflow (TFUDF)
  The value specified with TXDIZ in SICTR is output.
- Transmit FIFO overflow (TFOVF)
  The contents of the transmit FIFO are protected, and the write operation causing the overflow is ignored.
- Receive FIFO overflow (RFOVF)
  Data causing the overflow is discarded and lost.
- Receive FIFO underflow (RFUDF)
  An undefined value is output on the bus.
- Transmit FS error (TFSERR)
  The internal counter is reset according to the synchronization signal in which an error occurs.
- Receive FS error (RFSERR)
  The internal counter is reset according to the synchronization signal in which an error occurs.

25.4.9 Transmit and Receive Timing

Examples of the BBIF2 serial transmission and reception are shown in Figure 25.13 and 25.14.

(a) 16-Bit Synchronization Pulse

Synchronization pulse method, one group, one word, 16 bits in a word, no bit delay

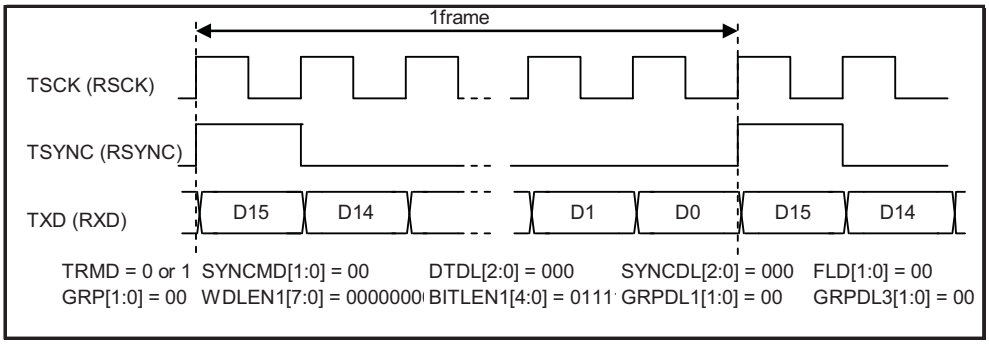


Figure 25.13 Transmit and Receive Timing (16 Bits)

(b) 32-Bit Synchronization Pulse

Synchronization pulse method, one group, 32 words, 32 bits in a word, 1-bit delay

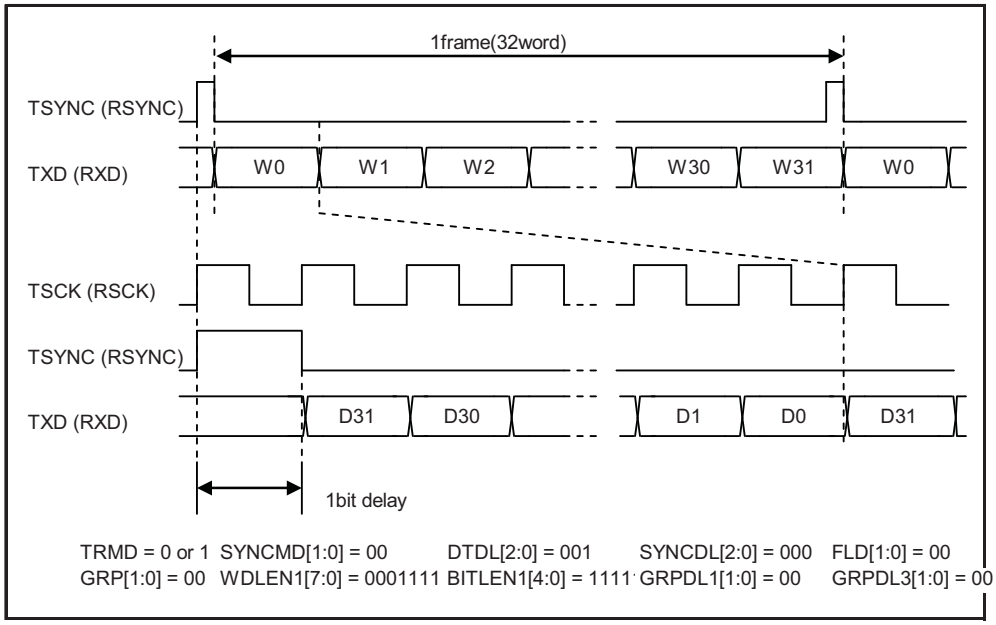


Figure 25.14 Transmit and Receive Timing (32 Bits)

(c) 24-Bit IIS Transmission

L/R mode, 2 groups, 1 word for each group, 24-bit word for each group, 1-bit delay.

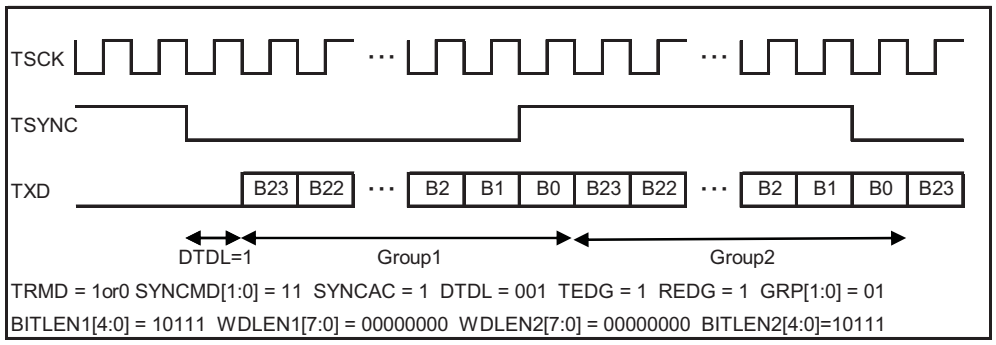


Figure 25.15 Transmit and Receive Timing (24-Bit IIS)

25.4.10 SPI

The BBIF can be used as an SPI device by setting the registers appropriately. Set the following: SITMDR1.PCON = 1'b1, SITMDR1.SYNCMD = 2'b10, and SICTR.TSCKIZ ≠ 2'b00 (for the receiver, SICTR.RSCKIZ ≠ 2'b00).

(a) Example of SPI Device Connection

Figure 25.16 shows an example of connection with an SPI device.

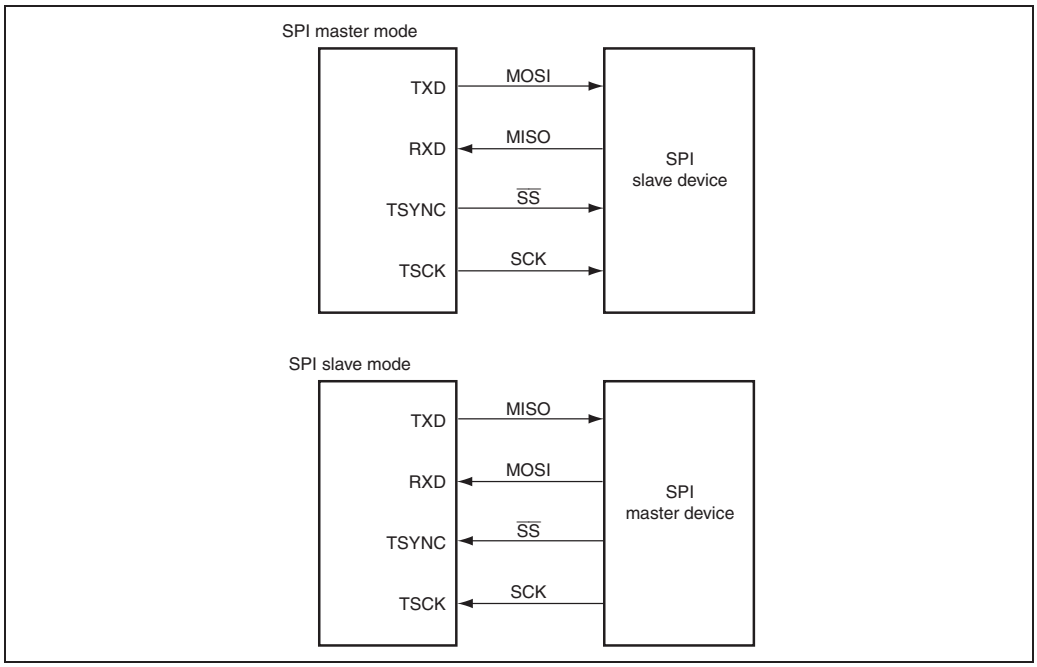


Figure 25.16 Example of SPI Device Connection

(b) SPI Serial Clock Timing

Figure 25.17and 25.18 show the data and clock timing in SPI mode. As shown in the figures, four types of serial transfer formats can be used.

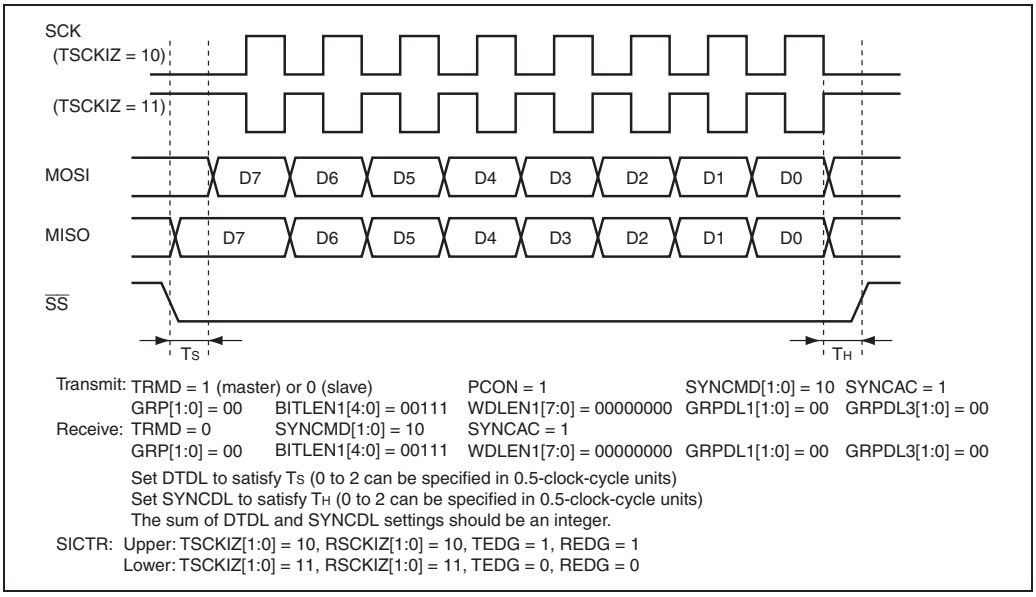


Figure 25.17 SPI Clock and Data Timing 1

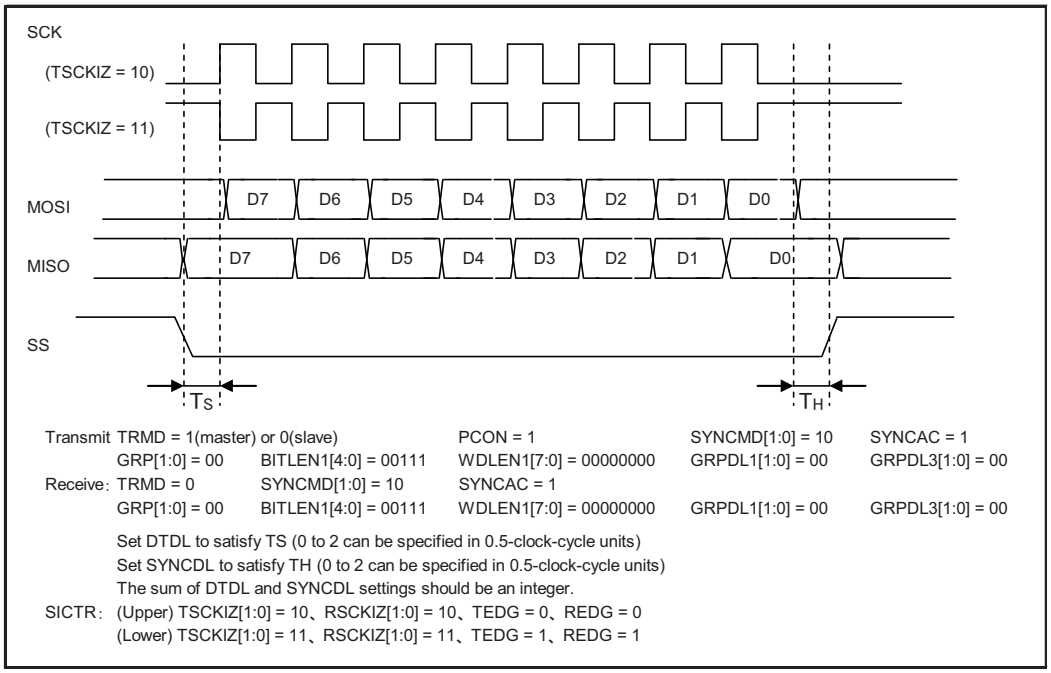


Figure 25.18 SPI Clock and Data Timing 2

25.4.11 Notes for Using SPI Mode

- When the module stop release or software reset is performed in SPI mode, set the control register (SICTR) again with each of the receive-setting bits (RSCKIZ/REDG) being 0.
- When using SPI master mode, set the FLD bits in SITMDR1 to ensure SUBCK4 cycles or more.
- When using SPI slave mode, set SUBCK4 cycles or more for the frame synchronization signal interval.
- For SPI slave mode operation, The setting for data delay should always set 0.
- For SPI slave mode operation, TXDIZ bits work on SS signal invalid state.

25.4.12 IIS

This module can support IIS format with following setting which is shown Figure 25.19 and Figure 25.20.BITLEN1/2 bit will change by usage.

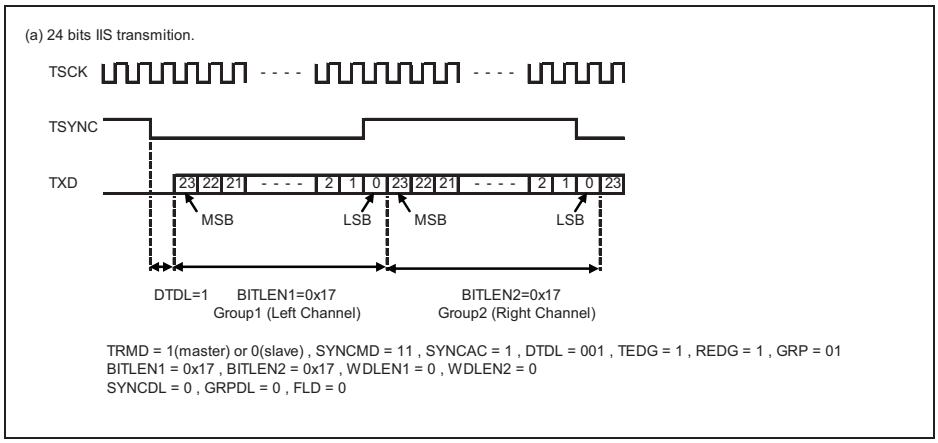


Figure 25.19 24 bits IIS transmition

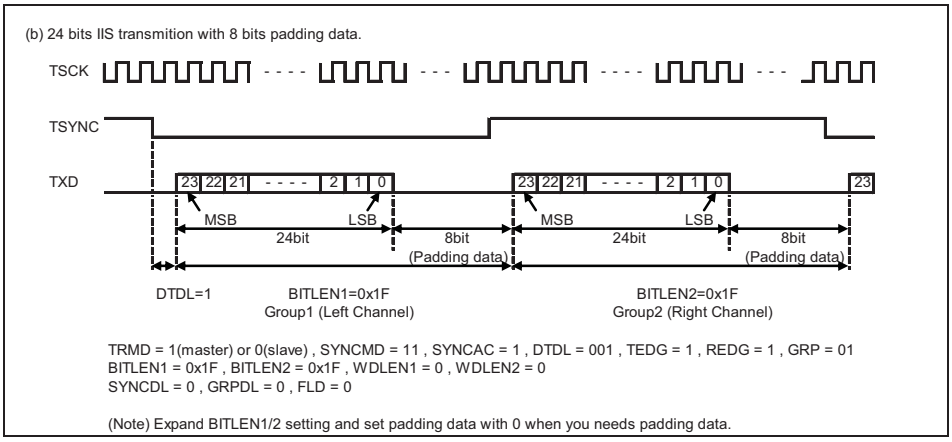


Figure 25.20 24 bits IIS transmition with 8 bits padding data

Section 26 MIPI-HSI

26.1 Features

This LSI circuit incorporates a MIPI-HSI (Mobile Industry Processor Interface–High-speed Sync. Serial Interface) that complies with Version 1.01.00 of the MIPI-HSI specification (30 September 2008).

Features of the HSI are listed below.

- Compliant with Version 1.01.00 of the MIPI-HSI specification (30 September 2008)
- Transmission FIFO with four 64-frame banks
- Reception FIFO with four 64-frame banks
- Automatic attachment of channel IDs to transmitted frames
- Automatic sorting of received frames into banks according to channel IDs
- Reception and transmission at up to 100 Mbps
- Generation of interrupts and DMA requests in response to amounts of data in the reception FIFO and transmission FIFO
- Automatic flow control in response to the reception of break transmission
- CAWAKE and ACWAKE pins
- Detection of tailing bits
- Support for 1.8V I/O interfaces

26.2 Block Diagram

Figure 26.1 is a block diagram of the HSI.

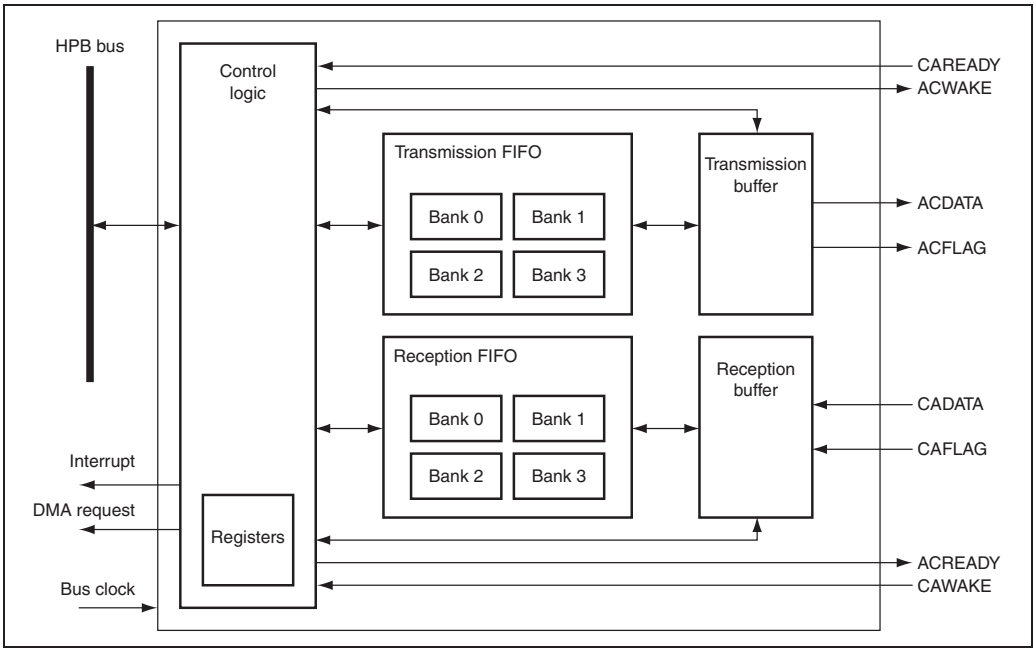


Figure 26.1 Block Diagram of the MIPI-HSI

26.3 Input/Output Pins

Table 26.1 shows the pin configuration of the HSI.

Table 26.1 Pin Configuration

Signal	MIPI Specification	I/O	Function
MP_RX_READY	ACREADY	Output	READY pin in the reception side
GP_RX_WAKE	CAWAKE	Input	WAKE pin in the reception side
GP_RX_FLAG	CAFLAG	Input	FLAG pin in the reception side
GP_RX_DATA	CADATA	Input	DATA pin in the reception side
GP_TX_READY	CAREADY	Input	READY pin in the transmission side
MP_TX_WAKE	ACWAKE	Output	WAKE pin in the transmission side
MP_TX_FLAG	ACFLAG	Output	FLAG pin in the transmission side
MP_TX_DATA	ACDATA	Output	DATA pin in the transmission side

26.4 Register Description

Table 26.2 shows the HSI register configuration.

Table 26.2 Register Configuration

Register Name	Abbreviation	R/W	Address	Initial Value	Access Size
TX control register	HSI_TXCR	R/W	H'E6A40000	H'00000000	32
TX ready negation control register	HSI_TXRNCR	R/W	H'E6A40004	H'00000000	32
TX timeout control register	HSI_TXTOCR	R/W	H'E6A40008	H'00000000	32
TX break control register	HSI_TXBRKCR	R/W	H'E6A4000C	H'00000000	32
TXFIFO status register	HSI_TXFSR	R	H'E6A40020	H'00000000	32
RX control register	HSI_RXCR	R/W	H'E6A40030	H'00000000	32
RX timeout detection time period control register	HSI_RXTOCR	R/W	H'E6A40034	H'00000000	32
RX tailing bit detection time period control register	HSI_RXTLCR	R/W	H'E6A40038	H'00000000	32
Receiver drain timeout detection time period control register	HSI_RXDTOCR	R/W	H'E6A4003C	H'00000000	32
RX burst count constraint register	HSI_RXBCCR	R/W	H'E6A40040	H'00000000	32
RX FIFO status register	HSI_RXFSR	R	H'E6A40050	H'00000000	32
TXDMA control register	HSI_DMATXCR	R/W	H'E6A40060	H'00000000	32
RXDMA control register	HSI_DMARXCR	R/W	H'E6A40064	H'00000000	32
Interrupt control register	HSI_IRQCR	R/W	H'E6A40070	H'00000000	32
Interrupt status register	HSI_IRQSR	R/W	H'E6A40080	H'00000001	32
IO port control register	HSI_IOCR	R/W	H'E6A40090	H'00000000	32
TXCH_ID register (bank 0)	HSI_TX_CH0	W	H'E6A400B0	Undefined	32
TX data window (bank 0)	HSI_TX_DATA0	W	H'E6A400B4	Undefined	32

Register Name	Abbreviation	R/W	Address	Initial Value	Access Size
TXCH_ID register (bank 1)	HSI_TX_CH1	W	H'E6A400B8	Undefined	32
TX data window (bank 1)	HSI_TX_DATA1	W	H'E6A400BC	Undefined	32
TXCH_ID register (bank 2)	HSI_TX_CH2	W	H'E6A400C0	Undefined	32
TX data window (bank 2)	HSI_TX_DATA2	W	H'E6A400C4	Undefined	32
TXCH_ID register (bank 3)	HSI_TX_CH3	W	H'E6A400C8	Undefined	32
TX data window (bank 3)	HSI_TX_DATA3	W	H'E6A400CC	Undefined	32
TXCH_ID status register	HSI_TX_CHSR	R/W	H'E6A400F0	Undefined	32
TXCH_ID/data window (bank 0)	HSI_TX_ CHDATA0	W	H'E6A40100	Undefined	32
TXCH_ID/data window (bank 1)	HSI_TX_ CHDATA1	W	H'E6A40104	Undefined	32
TXCH_ID/data window (bank 2)	HSI_TX_ CHDATA2	W	H'E6A40108	Undefined	32
TXCH_ID/data window (bank 3)	HSI_TX_ CHDATA3	W	H'E6A4010C	Undefined	32
RXCH_ID register (bank 0)	HSI_RX_CH0	R	H'E6A40130	Undefined	32
RX data window (bank 0)	HSI_RX_DATA0	R	H'E6A40134	Undefined	32
RXCH_ID register (bank 1)	HSI_RX_CH1	R	H'E6A40138	Undefined	32
RX data window (bank 1)	HSI_RX_DATA1	R	H'E6A4013C	Undefined	32
RXCH_ID register (bank 2)	HSI_RX_CH2	R	H'E6A40140	Undefined	32
RX data window (bank 2)	HSI_RX_DATA2	R	H'E6A40144	Undefined	32
RXCH_ID register (bank 3)	HSI_RX_CH3	R	H'E6A40148	Undefined	32

Register Name	Abbreviation	R/W	Address	Initial Value	Access Size
RX data window (bank 3)	HSI_RX_DATA3	R	H'E6A4014C	Undefined	32
RXCH_ID status register	HSI_RX_CHSR	R/W	H'E6A40170	Undefined	32
RXCH_ID/data window (bank 0)	HSI_RX_ CHDATA0	R	H'E6A40180	Undefined	32
RXCH_ID/data window (bank 1)	HSI_RX_ CHDATA1	R	H'E6A40184	Undefined	32
RXCH_ID/data window (bank 2)	HSI_RX_ CHDATA2	R	H'E6A40188	Undefined	32
RXCH_ID/data window (bank 3)	HSI_RX_ CHDATA3	R	H'E6A4018C	Undefined	32

26.4.1 TX Control Register (HSI_TXCR)

HSI_TXCR is a 32-bit readable/writable register that carries out setting of the transmitter.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TXBRKLEN								TXRATE							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TXRATEEN	TXCHLEN			—	—	—	TX MODE	—	—	—	TX RESET	—	TXBRK	—	TX START
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R	R/W	R	R	R	R/W	R	R/W	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	TXBRKLEN	All 0	R/W	Sets the length of a break transmission. A value equal to or greater than H'24 should be set to TXBRKLEN. During the break transmission, a break transmission is issued which is of a length that is TXBRKLEN + 1.
23 to 16	TXRATE	All 0	R/W	Transmission transfer rate is set. The allowed range is between H'00 and H'FE when TXRATEEN is enabled. (H'FF is not allowed)

Bit	Bit Name	Initial Value	R/W	Description
15	TXRATEEN	0	R/W	Transmission transfer rate that is set to TXRATE is enabled. 0: Transmitter transmits at 100 MHz. 1: Transmitter transmits at 100/(TXRATE + 2) MHz.
14 to 12	TXCHLEN	All 0	R/W	Number of bits of a channel descriptor is specified. This bit should be set at equal to or less than H'4.
11 to 9	—	All 0	R	Reserved The write value should be the same as the read value.
8	TXMODE	0	R/W	Sets transmission mode. 0: Stream mode 1: Frame mode
7 to 5	—	All 0	R	Reserved The write value should be the same as the read value.
4	TXRESET	0	R/W	When 1 is written to this bit, the transmitter is initialized. Transmission setting and data stored in transmission FIFO are cleared. To cancel initialization, 0 should be written to this bit. The registers to be initialized are as follows: HSI_TXCR (except TXRESET), HSI_TXRNCR, HSI_TXTOCR, HSI_TXBRKCR, HSI_TXFSR, HSI_DMATXCR, HSI_IRQCR.TXOVFEN, HSI_IRQCR.TXF0EN to TXF3EN, HSI_IRQCR.TXRNEN, HSI_IRQCR.TXTOEN, HSI_IRQCR.TXBRKEN, HSI_IRQCR.TXENDEN, HSI_IRQSR.TXOVF, HSI_IRQSR.TXF0 to TXF3, HSI_IRQSR.TXRN, HSI_IRQSR.TXTO, HSI_IRQSR.TXBRK, HSI_IOCR.ACWAKE, HSI_TX_CH0 to HSI_TX_CH3, HSI_TX_DATA0 to HSI_TX_DATA3, HSI_TX_CHSR, HSI_TX_CHDATA0 to HSI_TX_CHDATA3
3	—	0	R	Reserved The write value should be the same as the read value.
2	TXBRK	0	R/W	If 1 is written when TXBRK is 0, the transmitter carries out break transmission at the frame boundary that is being transmitted.
1	—	0	R	Reserved The write value should be the same as the read value.

Bit	Bit Name	Initial Value	R/W	Description
0	TXSTART	0	R/W	If 1 is written when TXSTART is 0, the transmitter takes in the transmission setting and starts transmission. Even if writing is carried out simultaneously to the other fields in HSI_TXCR, it is reflected in the transmission setting. If 0 is written to TXSTART, the transmission is terminated at the frame boundary that is being transmitted.

26.4.2 TX Ready Negation Control Register (HSI_TXRNCR)

HSI_TXRNCR is a 32-bit readable/writable register that carries out setting to measure the time period during which CAREADY is negated and to detect CAREADY negation timeout.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TXRNSTP	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TXRNC															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	TXRNSTP	0	R/W	Sets whether to temporarily terminate transmission at the time of CAREADY negation timeout detection. 0: Transmission is not terminated temporarily at the time of negation timeout detection. 1: Transmission is terminated temporarily at the time of negation timeout detection.
30 to 16	—	All 0	R	Reserved The write value should be the same as the read value.
15 to 0	TXRNC	All 0	R/W	Sets the number of cycles for detecting CAREADY negation timeout. This number of cycles is counted by HPϕ. If CAREADY is negated during the number of cycles that are set by TXRNC, CAREADY negation timeout is detected. To this bit, a value should be set that is equal to or greater than twice the number of cycles necessary for transmitting one frame (for example, if the frame length is 37 bits, the value should be 74 or more). When transmission transfer rate is set, a value should be set that is obtained by multiplying the normal value by the transmission transfer rate.

26.4.3 TX Timeout Control Register (HSI_TXTOCR)

HSI_TXTOCR is a 32-bit readable/writable register that carries out setting to measure the time period during which the frame transmission is terminated when CAREADY is in negated status and to detect transmission timeout.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TXTOSTP	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TXTOC															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	TXTOSTP	0	R/W	Sets operation of the transmitter at the time of transmission timeout detection. 0: Transmission is not terminated at the time of detection. 1: Transmission is terminated at the time of detection.
30 to 16	—	All 0	R	Reserved The write value should be the same as the read value.
15 to 0	TXTOC	All 0	R/W	Sets the number of cycles for detecting transmission timeout. This number of cycles is counted by HPϕ. During the number of cycles that are set by TXTOC, if the transmission is stopped due to CAREADY being negated, transmission timeout is detected. To this bit, a value should be set that is equal to or greater than twice the number of cycles necessary for transmitting one frame (for example, if the frame length is 37 bits, the value should be 74 or more). When the transmission transfer rate is set, a value should be set that is obtained by multiplying the normal value by the transmission transfer rate.

26.4.4 TX Break Control Register (HSI_TXBRKCR)

HSI_TXBRKCR is a 32-bit readable/writable register that carries out setting at the time of break transmission.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TXBRKSTP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved The write value should be the same as the read value.
0	TXBRKSTP	0	R/W	Sets whether to temporarily terminate transmission of the next frame after break transmission. 0: Transmission is not terminated temporarily. 1: Transmission is terminated temporarily.

26.4.5 TXFIFO Status Register (HSI_TXFSR)

HSI_TXFSR is a 32-bit readable/writable register that indicates number of data stored in each bank of transmission FIFO.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	TXFCB3						—	TXFCB2							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	TXFCB1						—	TXFCB0							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	—	0	R	Reserved The write value should be the same as the read value.
30 to 24	TXFCB3	All 0	R	Number of data stored in transmission FIFO bank 3 can be read.
23	—	0	R	Reserved The write value should be the same as the read value.
22 to 16	TXFCB2	All 0	R	Number of data stored in transmission FIFO bank 2 can be read.
15	—	0	R	Reserved The write value should be the same as the read value.
14 to 8	TXFCB1	All 0	R	Number of data stored in transmission FIFO bank 1 can be read.
7	—	0	R	Reserved The write value should be the same as the read value.
6 to 0	TXFCB0	All 0	R	Number of data stored in transmission FIFO bank 0 can be read.

26.4.6 RX Control Register (HSI_RXCR)

HSI_RXCR is a 32-bit readable/writable register that carries out setting of the receiver.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RXBRKLEN								—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	RXCHLEN			RXAFC	RXFLOW		RX MODE	—	—	—	RX RESET	—	—	—	RX START
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	RXBRKLEN	0	R/W	Sets the length of a 0 string, to be recognized as break transmission in frame mode. This bit should be set to equal to or greater than H'25. Set the transmitter of the opposite communication device so that it should transmit two more 0 bits than this set value as the break transmission (when RXBRKLEN = H'25, set the transmitter of the opposite communication device so that it transmits 39 or more bits of 0s as break transmission).
23 to 15	—	0	R	Reserved The write value should be the same as the read value.
14 to 12	RXCHLEN	All 0	R/W	Sets the number of bits of a channel descriptor. This bit should be set at equal to or less than H'4.
11	RXAFC	0	R/W	Enables or disables automatic flow control when receiving break transmission at the time of Receiver Realtime Data Flow in frame mode. 0: Automatic flow control is disabled. 1: Automatic flow control is enabled.
10, 9	RXFLOW	All 0	R/W	Read: Indicates current data flow. Write: Receiving data flow is set. 00: Synchronized Data Flow 01: Pipelined Data Flow 10: Receiver Realtime Data Flow However, transition is made to Synchronized Data Flow if break transmission is detected when RXAFC = 1. 11: Receiver Realtime Data Flow However, transition is made to Pipelined Data Flow if break transmission is detected when RXAFC = 1.
8	RXMODE	0	R/W	Sets receiving mode. 0: Stream mode 1: Frame mode
7 to 5	—	All 0	R	Reserved The write value should be the same as the read value.

Bit	Bit Name	Initial Value	R/W	Description
4	RXRESET	0	R/W	If 1 is written to this bit, the receiver, reception FIFO, and receiver setting registers are initialized. To cancel initialization, 0 should be written to this bit. The registers to be initialized are as follows: HSI_RXCR (except RXRESET), HSI_RXRNCR, HSI_RXTLCR, HSI_RXDTOCR, HSI_RXBCCR, HSI_DMARXCR, HSI_IRQCR.RXOVFEN, HSI_IRQCR.RXUDFEN, HSI_IRQCR.RXF0EN to RXF3EN, HSI_IRQCR.RXDTOEN, HSI_IRQCR.RXTLEN, HSI_IRQCR.RXTOEN, HSI_IRQCR.RXBRKEN, HSI_IRQCR.RXOVF, HSI_IRQSR.RXUDF, HSI_IRQSR.RXF0 to RXF3, HSI_IRQSR.RXDTO, HSI_IRQSR.RXTL, HSI_IRQSR.RXTO, HSI_IRQSR.RXBRK, HSI_IOCR.ACREADY, HSI_RX_CH0 to HSI_RX_CH3, HSI_RX_DATA0 to HSI_RX_DATA3, HSI_RX_CHSR, HSI_RX_CHDATA0 to HSI_RX_CHDATA3
3 to 1	—	All 0	R	Reserved The write value should be the same as the read value.
0	RXSTART	0	R/W	Reception starts when this bit is set to 1. This bit should not be set to 0 when the opposite communication device or the receiver of this HSI is carrying out the reception operation.

26.4.7 RX Timeout Detection Time Period Control Register (HSI_RXTOCR)

HSI_RXTOCR is a 32-bit readable/writable register that sets the number of cycles from the start of the frame reception until timeout. The value of this register can be changed even during the operation of the receiver.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RXTOP															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved The write value should be the same as the read value.
15 to 0	RXTOP	All 0	R/W	Sets the number of timeout cycles of frame reception. This number of cycles is counted by HPϕ. A value should be set that is equal to or greater than the arrival completion time period of the frame to be received.

26.4.8 RX Tailing Bit Detection Time Period Control Register (HSI_RXTLCR)

HSI_RXTLCR is a 32-bit readable/writable register that sets the time period to detect the bit that is received before asserting ACREADY after completion of frame reception. The value of this register can be changed even during the operation of the receiver.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RXTLP															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved The write value should be the same as the read value.
15 to 0	RXTLP	All 0	R/W	Sets the number of cycles, during which the tailing bit is detected. This number of cycles is counted by HPϕ. If the transmission frequency of the opposite communication device is lower, the number of cycles should be set such that the tailing bit detection time period is equal to or greater than the cycle of the transmission frequency.

26.4.9 RX Drain Timeout Detection Time Period Control Register (HSI_RXDTOCR)

HSI_RXDTOCR is a 32-bit readable/writable register that sets the time period until the opposite communication device is considered as terminated while the receiver is in operation due to Receiver Realtime Data Flow. The value of this register can be changed even during the operation of the receiver.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RXDTO															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved The write value should be the same as the read value.
15 to 0	RXDTO	All 0	R/W	Sets the number of cycles until the opposite communication device is considered as terminated. This number of cycles is counted by HPϕ. The number of cycles to be set here should be large enough for considering the transmitter of the opposite communication device as terminated.

26.4.10 RX Burst Count Constraint Register (HSI_RXBCCR)

HSI_RXBCCR is a 32-bit readable/writable register that sets the upper limit of the number of frames that can be received without negating ACREADY in Pipelined Data Flow. The value of this register can be changed even when the receiver is in operation.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	RXBCEN	—	—	—	—	RXBC							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	All 0	R	Reserved The write value should be the same as the read value.
12	RXBCEN	0	R/W	Sets the RX burst count constraint. 0: RX burst count constraint is disabled. 1: RX burst count constraint is enabled.
11 to 8	—	All 0	R	Reserved The write value should be the same as the read value.
7 to 0	RXBC	All 0	R/W	Sets the upper limit of RX burst count.

26.4.11 RXFIFO Status Register (HSI_RXFSR)

HSI_RXFSR is a 32-bit readable/writable register that indicates number of data stored in each bank of reception FIFO.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	RXFCB3							—	RXFCB2						
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	RXFCB1							—	RXFCB0						
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	—	0	R	Reserved The write value should be the same as the read value.
30 to 24	RXFCB3	All 0	R	Number of data stored in reception FIFO bank 3 can be read.
23	—	0	R	Reserved The write value should be the same as the read value.
22 to 16	RXFCB2	All 0	R	Number of data stored in reception FIFO bank 2 can be read.
15	—	0	R	Reserved The write value should be the same as the read value.
14 to 8	RXFCB1	All 0	R	Number of data stored in reception FIFO bank 1 can be read.
7	—	0	R	Reserved The write value should be the same as the read value.
6 to 0	RXFCB0	All 0	R	Number of data stored in reception FIFO bank 0 can be read.

26.4.12 TXDMA Control Register (HSI_DMATXCR)

HSI_DMATXCR is a 32-bit readable/writable register used to carry out DMA transfer setting.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TXD3CHID				TXD3ASNEN	—	TXD3EN		TXD2CHID				TXD2ASNEN	—	TXD2EN	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TXD1CHID				TXD1ASNEN	—	TXD1EN		—	—	—	—	—	—	TXD0EN	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	TXD3CHID	All 0	R/W	The channel ID of the data to be stored in the transmission FIFO bank 3 should be set. The bit count should be the same as that of HSI_TXCR.TXCHLEN.
27	TXD3ASNEN	0	R/W	Enables the channel ID set in TXD3CHID. 0: The channel ID is not allocated to the transmission FIFO bank 3. 1: The channel ID set in TXD3CHID is allocated to the transmission FIFO bank 3. If this bit is set to 1, TXD3CHID is set as the channel ID when data is written to HSI_TXDATA3.
26	—	0	R	Reserved The write value should be the same as the read value.

Bit	Bit Name	Initial Value	R/W	Description
25, 24	TXD3EN	All 0	R/W	Issues a DMA request TX[3] according to the availability of space in the transmission FIFO bank 3. 00: DMA request is not issued (disabled). 01: DMA request is issued if space for one frame or more is available. 10: DMA request is issued if space for two or more frames is available. 11: DMA request is issued if space for eight or more frames is available. This bit should not be enabled when the transmission FIFO bank 3 interrupt is enabled.
23 to 20	TXD2CHID	All 0	R/W	The channel ID of the data to be stored in the transmission FIFO bank 2 should be set. The bit count should be the same as that of HSI_TXCR.TXCHLEN.
19	TXD2ASNEN	0	R/W	Enables the channel ID set in TXD2CHID. 0: The channel ID is not allocated to the transmission FIFO bank 2. 1: The channel ID set in TXD2CHID is allocated to the transmission FIFO bank 2. If this bit is set to 1, TXD2CHID is set as the channel ID when data is written to HSI_TXDATA2.
18	—	0	R	Reserved The write value should be the same as the read value.
17, 16	TXD2EN	All 0	R/W	Issues a DMA request TX[2] according to the availability of space in the transmission FIFO bank 2. 00: DMA request is not issued (disabled). 01: DMA request is issued if space for one frame or more is available. 10: DMA request is issued if space for two or more frames is available. 11: DMA request is issued if space for eight or more frames is available. This bit should not be enabled when the transmission FIFO bank 2 interrupt is enabled.

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	TXD1CHID	All 0	R/W	The channel ID of the data to be stored in the transmission FIFO bank 1 should be set. The bit count should be the same as that of HSI_TXCR.TXCHLEN.
11	TXD1ASNEN	0	R/W	Enables the channel ID set in TXD1CHID. 0: The channel ID is not allocated to the transmission FIFO bank 1. 1: The channel ID set in TXD1CHID is allocated to the transmission FIFO bank 1. If this bit is set to 1, TXD1CHID is set as the channel ID when data is written to HSI_TXDATA1.
10	—	0	R	Reserved The write value should be the same as the read value.
9, 8	TXD1EN	All 0	R/W	Issues a DMA request TX[1] according to the availability of space in the transmission FIFO bank 1. 00: DMA request is not issued (disabled). 01: DMA request is issued if space for one frame or more is available. 10: DMA request is issued if space for two or more frames is available. 11: DMA request is issued if space for eight or more frames is available. This bit should not be enabled when the transmission FIFO bank 1 interrupt is enabled.
7 to 2	—	All 0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
1, 0	TXD0EN	All 0	R/W	Issues a DMA request TX[0] according to the availability of space in the transmission FIFO bank 0. 00: DMA request is not issued (disabled). 01: DMA request is issued if space for one frame or more is available. 10: DMA request is issued if space for two or more frames is available. 11: DMA request is issued if space for eight or more frames is available. This bit should not be enabled when the transmission FIFO bank 0 interrupt is enabled.

26.4.13 RXDMA Control Register (HSI_DMARXCR)

HSI_DMARXCR is a 32-bit readable/writable register used to perform DMA transfer setting.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RXD3CHID				RXD3 ASNEN	—	RXD3EN		RXD2CHID				RXD2 ASNEN	—	RXD2EN	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RXD1CHID				RXD1 ASNEN	—	RXD1EN		—	—	—	—	—	—	RXD0EN	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	RXD3CHID	All 0	R/W	The channel ID of the data to be stored in the reception FIFO bank 3 should be set. The bit count should be the same as that of HSI_RXCR.RXCHLEN. The channel ID allocated to other banks should not be set to this bit.

Bit	Bit Name	Initial Value	R/W	Description
27	RXD3ASNEN	0	R/W	Enables the channel ID set in RXD3CHID. 0: The channel ID is not allocated to the reception FIFO bank 3. 1: The channel ID set in RXD3CHID is allocated to the reception FIFO bank 3. If this bit is set to 1, and if the channel ID of the received frame matches RXD3CHID, the frame is stored in the reception FIFO bank 3.
26	—	0	R	Reserved The write value should be the same as the read value.
25, 24	RXD3EN	All 0	R/W	Issues a DMA request RX[3] if the received data is stored in the reception FIFO bank 3. 00: DMA request is not issued (disabled). 01: DMA request is issued if data of one frame or more is stored. 10: DMA request is issued if data of two or more frames is stored. 11: DMA request is issued if data of eight or more frames is stored. This bit should not be enabled when the reception FIFO bank 3 interrupt is enabled.
23 to 20	RXD2CHID	All 0	R/W	The channel ID of the data to be stored in the reception FIFO bank 2 should be set. The bit count should be the same as that of HSI_RXCR.RXCHLEN. The channel ID allocated to other banks should not be set to this bit.
19	RXD2ASNEN	0	R/W	Enables the channel ID set in RXD2CHID. 0: The channel ID is not allocated to the reception FIFO bank 2. 1: The channel ID set in RXD2CHID is allocated to the reception FIFO bank 2. If this bit is set to 1, and if the channel ID of the received frame matches RXD2CHID, the frame is stored in the reception FIFO bank 2.

Bit	Bit Name	Initial Value	R/W	Description
18	—	0	R	Reserved The write value should be the same as the read value.
17, 16	RXD2EN	All 0	R/W	Issues a DMA request RX[2] if the received data is stored in the reception FIFO bank 2. 00: DMA request is not issued (disabled). 01: DMA request is issued if data of one frame or more is stored. 10: DMA request is issued if data of two or more frames is stored. 11: DMA request is issued if data of eight or more frames is stored. This bit should not be enabled when the reception FIFO bank 2 interrupt is enabled.
15 to 12	RXD1CHID	All 0	R/W	The channel ID of the data to be stored in the reception FIFO bank 1 should be set. The bit count should be the same as that of HSI_RXCR.RXCHLEN. The channel ID allocated to other banks should not be set to this bit.
11	RXD1ASNEN	0	R/W	Enables the channel ID set in RXD1CHID. 0: The channel ID is not allocated to the reception FIFO bank 1. 1: The channel ID set in RXD1CHID is allocated to the reception FIFO bank 1. If this bit is set to 1, and if the channel ID of the received frame matches RXD1CHID, the frame is stored in the reception FIFO bank 1.
10	—	0	R	Reserved The write value should be the same as the read value.

Bit	Bit Name	Initial Value	R/W	Description
9, 8	RXD1EN	All 0	R/W	Issues a DMA request RX[1] if the received data is stored in the reception FIFO bank 1. 00: DMA request is not issued (disabled). 01: DMA request is issued if data of one frame or more is stored. 10: DMA request is issued if data of two or more frames is stored. 11: DMA request is issued if data of eight or more frames is stored. This bit should not be enabled when the reception FIFO bank 1 interrupt is enabled.
7 to 2	—	All 0	R	Reserved This bit is always read as 0. The write value should always be 0.
1, 0	RXD0EN	All 0	R/W	Issues a DMA request RX[0] if the received data is stored in the reception FIFO bank 0. 00: DMA request is not issued (disabled). 01: DMA request is issued if data of one frame or more is stored. 10: DMA request is issued if data of two or more frames is stored. 11: DMA request is issued if data of eight or more frames is stored. This bit should not be enabled when the reception FIFO bank 0 interrupt is enabled.

26.4.14 Interrupt Control Register (HSI_IRQCR)

HSI_IRQCR is a 32-bit readable/writable register that enables or disables interrupts and sets the interrupt conditions.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TX OVFEN	RX OVFEN	RX UDFEN	—	—	—	—	—	RXF3EN		RXF2EN		RXF1EN		RXF0EN	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TXF3EN		TXF2EN		TXF1EN		TXF0EN		TX RNEN	TX TOEN	RX DTOEN	RX TLEN	RX TOEN	RX BRKEN	TX BRKEN	TX ENDEN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	TXOVFEN	0	R/W	Transmission Overflow Interrupt Enable
30	RXOVFEN	0	R/W	Reception Overflow Interrupt Enable
29	RXUDFEN	0	R/W	Reception Underflow Interrupt Enable
28 to 24	—	All 0	R	Reserved The write value should be the same as the read value.
23, 22	RXF3EN	All 0	R/W	Enables the interrupt when received data is stored in the reception FIFO bank 3. 00: The interrupt is not issued (disabled). 01: The interrupt is issued if data of one frame or more is stored. 10: The interrupt is issued if data of 16 or more frames is stored. 11: The interrupt is issued if data of 32 or more frames is stored. This bit should not be enabled when the reception FIFO bank 3 DMA request is enabled.

Bit	Bit Name	Initial Value	R/W	Description
21, 20	RXF2EN	All 0	R/W	Enables the interrupt when received data is stored in the reception FIFO bank 2. 00: The interrupt is not issued (disabled). 01: The interrupt is issued if data of one frame or more is stored. 10: The interrupt is issued if data of 16 or more frames is stored. 11: The interrupt is issued if data of 32 or more frames is stored. This bit should not be enabled when the reception FIFO bank 2 DMA request is enabled.
19, 18	RXF1EN	All 0	R/W	Enables the interrupt when received data is stored in the reception FIFO bank 1. 00: The interrupt is not issued (disabled). 01: The interrupt is issued if data of one frame or more is stored. 10: The interrupt is issued if data of 16 or more frames is stored. 11: The interrupt is issued if data of 32 or more frames is stored. This bit should not be enabled when the reception FIFO bank 1 DMA request is enabled.
17, 16	RXF0EN	All 0	R/W	Enables the interrupt when received data is stored in the reception FIFO bank 0. 00: The interrupt is not issued (disabled). 01: The interrupt is issued if data of one frame or more is stored. 10: The interrupt is issued if data of 16 or more frames is stored. 11: The interrupt is issued if data of 32 or more frames is stored. This bit should not be enabled when the reception FIFO bank 0 DMA request is enabled.

Bit	Bit Name	Initial Value	R/W	Description
15, 14	TXF3EN	All 0	R/W	Enables the interrupt when space is available in the transmission FIFO bank 3. 00: The interrupt is not issued (disabled). 01: The interrupt is issued if space for one frame or more is available. 10: The interrupt is issued if space for 16 or more frames is available. 11: The interrupt is issued if space for 32 or more frames is available. This bit should not be enabled when the transmission FIFO bank 3 DMA request is enabled.
13, 12	TXF2EN	All 0	R/W	Enables the interrupt when space is available in the transmission FIFO bank 2. 00: The interrupt is not issued (disabled). 01: The interrupt is issued if space for one frame or more is available. 10: The interrupt is issued if space for 16 or more frames is available. 11: The interrupt is issued if space for 32 or more frames is available. This bit should not be enabled when the transmission FIFO bank 2 DMA request is enabled.
11, 10	TXF1EN	All 0	R/W	Enables the interrupt when space is available in the transmission FIFO bank 1. 00: The interrupt is not issued (disabled). 01: The interrupt is issued if space for one frame or more is available. 10: The interrupt is issued if space for 16 or more frames is available. 11: The interrupt is issued if space for 32 or more frames is available. This bit should not be enabled when the transmission FIFO bank 1 DMA request is enabled.

Bit	Bit Name	Initial Value	R/W	Description
9, 8	TXF0EN	All 0	R/W	Enables the interrupt when space is available in the transmission FIFO bank 0. 00: The interrupt is not issued (disabled). 01: The interrupt is issued if space for one frame or more is available. 10: The interrupt is issued if space for 16 or more frames is available. 11: The interrupt is issued if space for 32 or more frames is available. This bit should not be enabled when the transmission FIFO bank 0 DMA request is enabled.
7	TXRNEN	0	R/W	Enables the TX ready negation timeout interrupt.
6	TXTOEN	0	R/W	Enables the TX timeout interrupt.
5	RXDTOEN	0	R/W	Enables the RX drain timeout detection interrupt.
4	RXTLEN	0	R/W	Enables the RX tailing bit detection interrupt.
3	RXTOEN	0	R/W	Enables the RX reception timeout interrupt.
2	RXBRKEN	0	R/W	Enables the RX break-transmission reception interrupt. Even if this bit is set to 0, automatic flow control by HSI_RXCR.RXAFC is enabled.
1	TXBRKEN	0	R/W	Enables the TX break-transmission transmission end interrupt.
0	TXENDEN	0	R/W	Enables the TX frame-transmission end interrupt.

26.4.15 Interrupt Status Register (HSI_IRQSR)

HSI_IRQSR is a 32-bit readable/writable register that indicates the source of the generated interrupt.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TXOVF	RXOVF	RXUDF	—	—	—	—	—	—	RXF3	—	RXF2	—	RXF1	—	RXF0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/WC0	R/WC0	R/WC0	R	R	R	R	R	R	R/WC0	R	R/WC0	R	R/WC0	R	R/WC0

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	TXF3	—	TXF2	—	TXF1	—	TXF0	TXRN	TXTO	RXDTO	RXTL	RXTO	RXBRK	TXBRK	TXEND
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/WC0	R	R/WC0	R	R/WC0	R	R/WC0	R/WC0	R/WC0	R/WC0	R/WC0	R/WC0	R/WC0	R/WC0	R

Bit	Bit Name	Initial Value	R/W	Description
31	TXOVF	0	R/WC0	Transmission FIFO overflow was detected. This bit can be cleared by writing 0 to the bit.
30	RXOVF	0	R/WC0	A frame was received when ACREADY was negated. This bit can be cleared by writing 0 to the bit.
29	RXUDF	0	R/WC0	Reception FIFO was read when there was no data. This bit can be cleared by writing 0 to the bit.
28 to 23	—	All 0	R	Reserved The write value should be the same as the read value.
22	RXF3	0	R/WC0	The reception FIFO bank 3 interrupt was generated. This bit can be cleared by writing 0 to the bit.
21	—	0	R	Reserved The write value should be the same as the read value.
20	RXF2	0	R/WC0	The reception FIFO bank 2 interrupt was generated. This bit can be cleared by writing 0 to the bit.
19	—	0	R	Reserved The write value should be the same as the read value.
18	RXF1	0	R/WC0	The reception FIFO bank 1 interrupt was generated. This bit can be cleared by writing 0 to the bit.
17	—	0	R	Reserved The write value should be the same as the read value.
16	RXF0	0	R/WC0	The reception FIFO bank 0 interrupt was generated. This bit can be cleared by writing 0 to the bit.

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved The write value should be the same as the read value.
14	TXF3	0	R/WC0	The transmission FIFO bank 3 interrupt was generated. This bit can be cleared by writing 0 to the bit.
13	—	0	R	Reserved The write value should be the same as the read value.
12	TXF2	0	R/WC0	The transmission FIFO bank 2 interrupt was generated. This bit can be cleared by writing 0 to the bit.
11	—	0	R	Reserved The write value should be the same as the read value.
10	TXF1	0	R/WC0	The transmission FIFO bank 1 interrupt was generated. This bit can be cleared by writing 0 to the bit.
9	—	0	R	Reserved The write value should be the same as the read value.
8	TXF0	0	R/WC0	The transmission FIFO bank 0 interrupt was generated. This bit can be cleared by writing 0 to the bit.
7	TXRN	0	R/WC0	CAREADY negation in the opposite communication device was detected during the set period. This bit can be cleared by writing 0 to the bit. If 1 is set in HSI_TXRNCR.TXRNSTP, transmission is temporarily suspended upon detection. Transmission is resumed when this bit is cleared.
6	TXTO	0	R/WC0	TXFIFO was detected to be nonempty and CAREADY negation in the opposite communication device was detected during the set period. This bit can be cleared by writing 0 to the bit. If 1 is set in HSI_TXTOCR.TXTOSTP, transmission is temporarily suspended upon detection. Transmission is resumed when this bit is cleared.
5	RXDTO	0	R/WC0	Activity suspension of the opposite communication device was detected during the set period. This bit can be cleared by writing 0 to the bit.
4	RXTL	0	R/WC0	The tailing bit was detected after frame reception. This bit can be cleared by writing 0 to the bit.
3	RXTO	0	R/WC0	Timeout occurred during frame reception. This bit can be cleared by writing 0 to the bit.

Bit	Bit Name	Initial Value	R/W	Description
2	RXBRK	0	R/WC0	Break transmission was received. This bit can be cleared by writing 0 to the bit. This bit is set regardless of the value of HSI_IRQCR.RXBRKEN.
1	TXBRK	0	R/WC0	Transmission of break transmission was completed. This bit can be cleared by writing 0 to the bit. This bit is set regardless of the value of HSI_IRQCR.TXBRKEN.
0	TXEND	1	R	Transmission of all the frames stored in TXFIFO and requested break transmission was completed. This bit is set regardless of the value of HSI_IRQCR.TXENDEN.

26.4.16 IO Port Control Register (HSI_IOCR)

HSI_IOCR is a 32-bit readable/writable register that monitors and changes the state of the pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CARDY	—	—	—	ACRDY	—	—	—	CA WAKE	—	—	—	AC WAKE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	All 0	R	Reserved The write value should be the same as the read value.
12	CARDY	0	R	Indicates the CAREADY status.
11 to 9	—	All 0	R	Reserved The write value should be the same as the read value.
8	ACRDY	0	R	Indicates the ACREADY status.

Bit	Bit Name	Initial Value	R/W	Description
7 to 5	—	All 0	R	Reserved The write value should be the same as the read value.
4	CAWAKE	0	R	Indicates the CAWAKE status.
3 to 1	—	All 0	R	Reserved The write value should be the same as the read value.
0	ACWAKE	0	R/W	Changes the ACWAKE status.

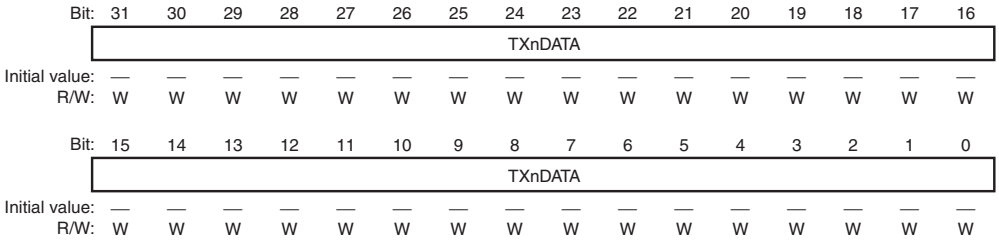
26.4.17 TXCH_ID Register (Banks 0 to 3) (HSI_TX_CH0 to HSI_TX_CH3)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	TXnCHID			
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

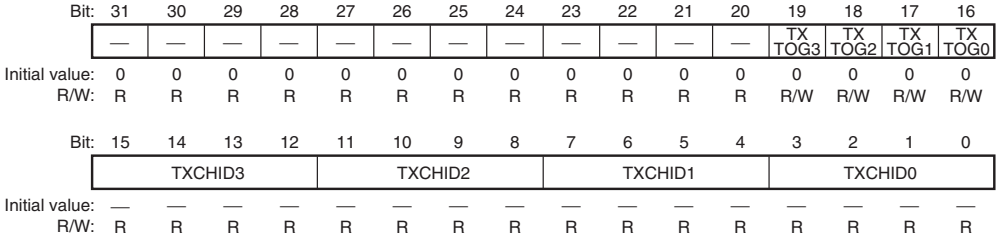
Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	Undefined	W	Reserved The write value should be the same as the read value.
3 to 0	TXnCHID	Undefined	W	The channel ID of the data to be stored in the transmission FIFO bank n should be set. The bit count should be the same as that of HSI_TXCR.TXCHLEN. Data is written to the transmission FIFO simultaneously when data is written to TXnDATA. Writing to TXnCHID does not allow data to be written to the transmission FIFO.

26.4.18 TX Data Window (Banks 0 to 3) (HSI_TX_DATA0 to HSI_TX_DATA3)



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	TXnDATA	Undefined	W	The data in the frame to be stored in the transmission FIFO bank n should be written. The current value of TXnDATA and the value previously set in TXnCHID are stored as a set in the transmission FIFO bank n. When HSI_DMATXCR.TXDnASNEN is enabled, the current value of TXnDATA and the value of HSI_DMATXCR.TXDnCHID are stored as a set in the transmission FIFO bank n.

26.4.19 TXCH_ID Status Register (HSI_TX_CHSR)



Bit	Bit Name	Initial Value	R/W	Description
31 to 20	—	All 0	R	Reserved The write value should be the same as the read value.

Bit	Bit Name	Initial Value	R/W	Description
19	TXTOG3	0	R/W	Sets whether the channel ID or the data is to be written to HSI_TX_CHDATA3. Once HSI_TX_CHDATA3 has been written to, the setting automatically toggles between the channel ID and data. 0: Channel ID is written. 1: Data is written.
18	TXTOG2	0	R/W	Sets whether the channel ID or the data is to be written to HSI_TX_CHDATA2. Once HSI_TX_CHDATA2 has been written to, the setting automatically toggles between the channel ID and data. 0: Channel ID is written. 1: Data is written.
17	TXTOG1	0	R/W	Sets whether the channel ID or the data is to be written to HSI_TX_CHDATA1. Once HSI_TX_CHDATA1 has been written to, the setting automatically toggles between the channel ID and data. 0: Channel ID is written. 1: Data is written.
16	TXTOG0	0	R/W	Sets whether the channel ID or the data is to be written to HSI_TX_CHDATA0. Once HSI_TX_CHDATA0 has been written to, the setting automatically toggles between the channel ID and data. 0: Channel ID is written. 1: Data is written.
15 to 12	TXCHID3	Undefined	R	The value written in HSI_TX_CHID3 is set. When HSI_DMATXCR.TXD3ASNEN is enabled, the value of HSI_DMATXCR.TXD3CHID is set when HSI_TX_DATA3 is written to. When TXTOG3 is 0, the value of TXCHID3 is set to the value of the channel ID written to HSI_TX_CHDATA3.

Bit	Bit Name	Initial Value	R/W	Description
11 to 8	TXCHID2	Undefined	R	The value written in HSI_TX_CHID2 is set. When HSI_DMATXCR.TXD2ASNEN is enabled, the value of HSI_DMATXCR.TXD2CHID is set when HSI_TX_DATA2 is written to. When TXTOG2 is 0, the value of TXCHID2 is set to the value of the channel ID written to HSI_TX_CHDATA2.
7 to 4	TXCHID1	Undefined	R	The value written in HSI_TX_CHID1 is set. When HSI_DMATXCR.TXD1ASNEN is enabled, the value of HSI_DMATXCR.TXD1CHID is set when HSI_TX_DATA1 is written to. When TXTOG1 is 0, the value of TXCHID1 is set to the value of the channel ID written to HSI_TX_CHDATA1.
3 to 0	TXCHID0	Undefined	R	The value written in HSI_TX_CHID0 is set. When TXTOG0 is 0, the value of TXCHID0 is set to the value of the channel ID written to HSI_TX_CHDATA0.

26.4.20 TXCH_ID/Data Window (Banks 0 to 3) (HSI_TX_CHDATA0 to HSI_TX_CHDATA3)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TXnCHDATA															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TXnCHDATA															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	TXnCHDATA	Undefined	W	When HSI_TX_CHSR.TXTOGn is 0, the channel ID of the data to be stored in the transmission FIFO bank n should be set. The bit count should be the same as that of HSI_TXCR.CHLEN. Writing to TXnCHDATA does not allow data to be written to the transmission FIFO. When HSI_TX_CHSR.TXTOGn is 1, the data of the frame to be stored in the transmission FIFO bank n should be written. The current value of TXnCHDATA and the previously set value of TXnCHID are stored as a set in the transmission FIFO bank n.

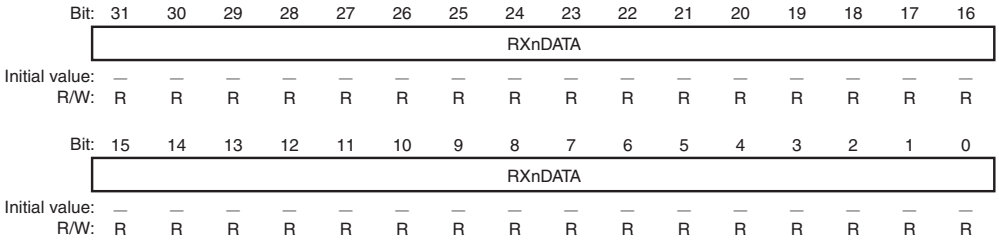
26.4.21 RXCH_ID Register (Banks 0 to 3) (HSI_RX_CH0 to HSI_RX_CH3)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	RXnCHID			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

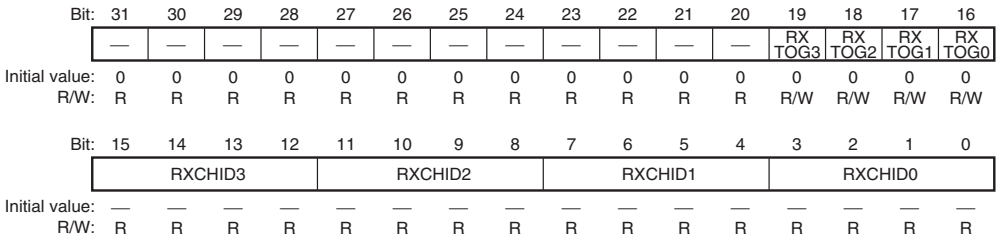
Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R	Reserved The write value should always be 0.
3 to 0	RXnCHID	Undefined	R	The channel ID stored in the reception FIFO bank n is read. Reading RXnCHID does not allow the channel ID of the next frame stored in the reception FIFO bank n to be retrieved.

26.4.22 RX Data Window (Banks 0 to 3) (HSI_RX_DATA0 to HSI_RX_DATA3)



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	RXnDATA	Undefined	R	The data of the frame stored in the reception FIFO bank n is read. When reading RXnDATA, the channel ID of the next frame in the reception FIFO bank n is retrieved to HSI_RX_CHn, and the data of the next frame is retrieved to HSI_RX_DATAn. When frame reception is completed and no frames are stored in the reception FIFO bank n, the channel IDs of the received frames are retrieved to HSI_RX_CHn and the data of the received frames are retrieved to HSI_RX_DATAn.

26.4.23 RXCH_ID Status Register (HSI_RX_CHSR)



Bit	Bit Name	Initial Value	R/W	Description
31 to 20	—	All 0	R	Reserved The write value should be the same as the read value.
19	RXTOG3	0	R/W	Sets whether to read the value of HSI_RX_CHDATA3 as a channel ID or data. Once HSI_RX_CHDATA3 is read, the setting automatically toggles between the channel ID and data. 0: Reads channel ID. 1: Reads data.
18	RXTOG2	0	R/W	Sets whether to read the value of HSI_RX_CHDATA2 as a channel ID or data. Once HSI_RX_CHDATA2 is read, the setting automatically toggles between the channel ID and data. 0: Reads channel ID. 1: Reads data.
17	RXTOG1	0	R/W	Sets whether to read the value of HSI_RX_CHDATA1 as a channel ID or data. Once HSI_RX_CHDATA1 is read, the setting automatically toggles between the channel ID and data. 0: Reads channel ID. 1: Reads data.
16	RXTOG0	0	R/W	Sets whether to read the value of HSI_RX_CHDATA0 as a channel ID or data. Once HSI_RX_CHDATA0 is read, the setting automatically toggles between the channel ID and data. 0: Reads channel ID. 1: Reads data.
15 to 12	RXCHID3	Undefined	R	The value read is the same as the value of HSI_RX_CH3.RX3CHID.
11 to 8	RXCHID2	Undefined	R	The value read is the same as the value of HSI_RX_CH2.RX2CHID.
7 to 4	RXCHID1	Undefined	R	The value read is the same as the value of HSI_RX_CH1.RX1CHID.
3 to 0	RXCHID0	Undefined	R	The value read is the same as the value of HSI_RX_CH0.RX0CHID.

26.4.24 RXCH_ID/Data Window (Banks 0 to 3) (HSI_RX_CHDATA0 to HSI_RX_CHDATA3)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RXnCHDATA															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RXnCHDATA															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	RXnCHDATA	Undefined	R	When HSI_RX_CHSR.RXTOGn is 0, the channel ID stored in the reception FIFO bank n is read. Reading this bit does not allow the channel ID of the next frame stored in the reception FIFO bank n to be retrieved. When HSI_RX_CHSR.RXTOGn is 1, data stored in the reception FIFO bank n is read. When this bit is read, the channel ID of the next frame stored in the reception FIFO bank n is retrieved in this register. When frame reception is completed and no frames are stored in the reception FIFO bank n, the channel IDs of the received frames are retrieved in this register.

26.5 Operation

26.5.1 Transmission Interface

Figure 26.2 is an overview of the transmission interface.

When the ACDATA signal is the same value for two continuous bits, the ACFLAG signal is toggled. Furthermore, the values of the ACDATA and ACFLAG signals last transmitted are maintained in inter-frame.

The CAREADY signal is used in the module after being synchronized with the bus clock.

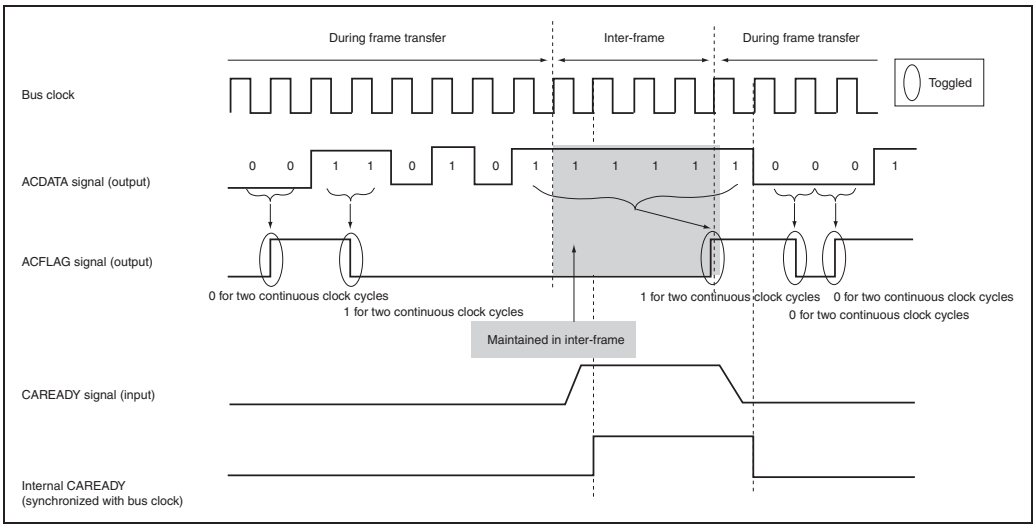


Figure 26.2 Overview of Transmission Interface

26.5.2 Reception Interface

Figure 26.3 is an overview of the reception interface.

Because the values of the CADATA and CAFLAG signals are maintained in inter-frame, the CADATA and CAFLAG signals of the inter-frame are ignored.

The ACREADY signal is output after being synchronized with the bus clock.

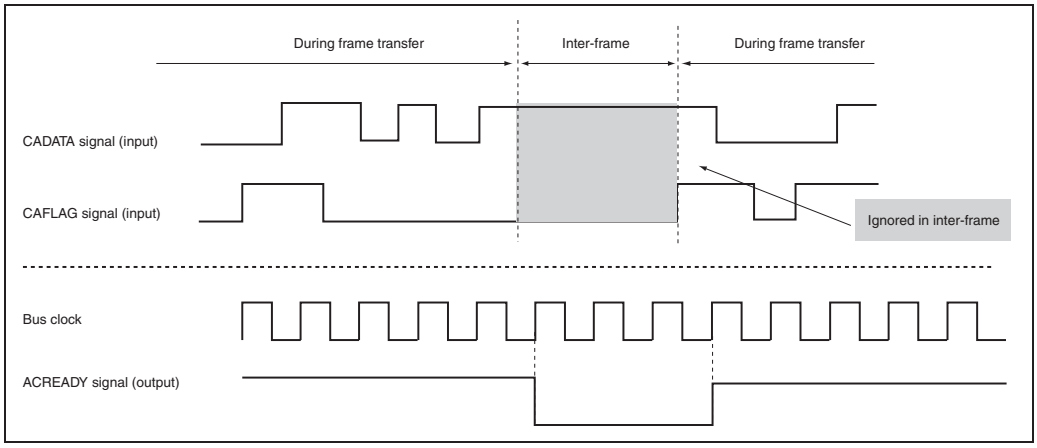


Figure 26.3 Overview of Reception Interface

26.5.3 Transmission FIFO

A transmission FIFO of four 64-frame (4-bit CH, 32-bit data) banks is included (figure 26.4).

An interrupt source or a DMA request can be set for each bank.

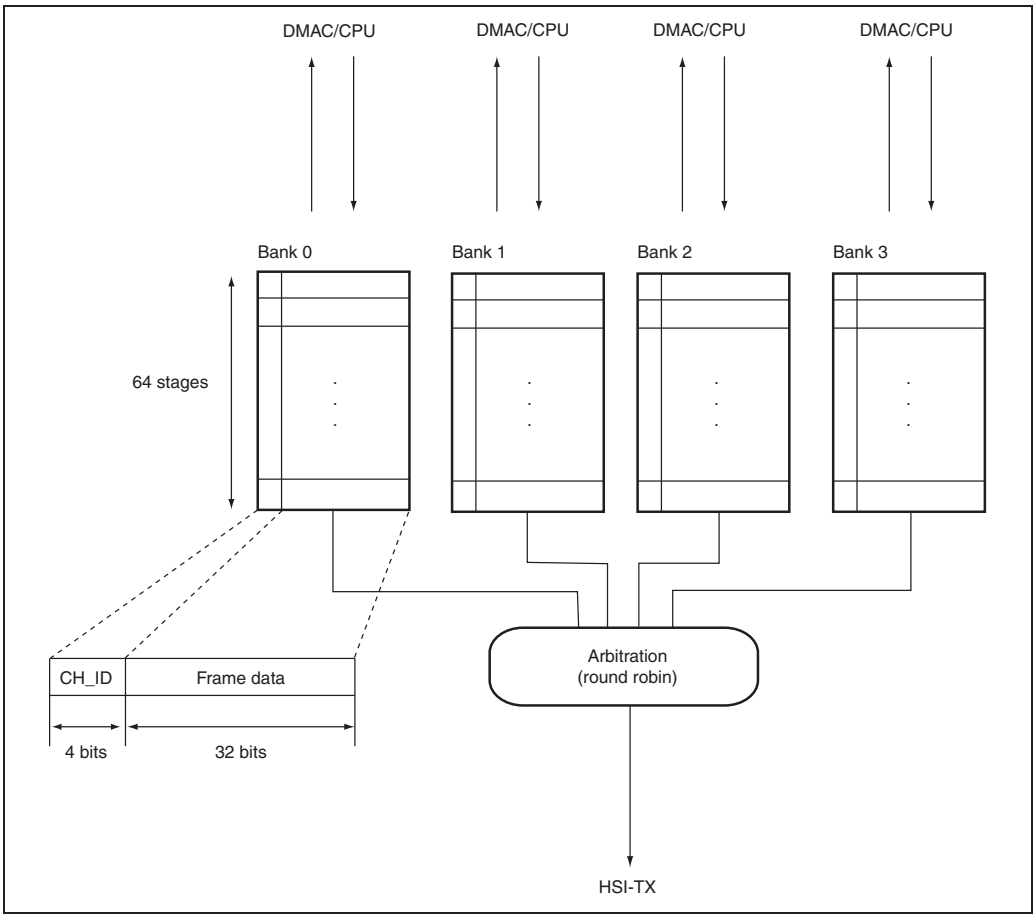


Figure 26.4 Transmission FIFO

26.5.4 Reception FIFO

A reception FIFO of four 64-frame (4-bit CH, 32-bit data) banks is included (figure 26.5).

An interrupt source or a DMA request can be set for each bank.

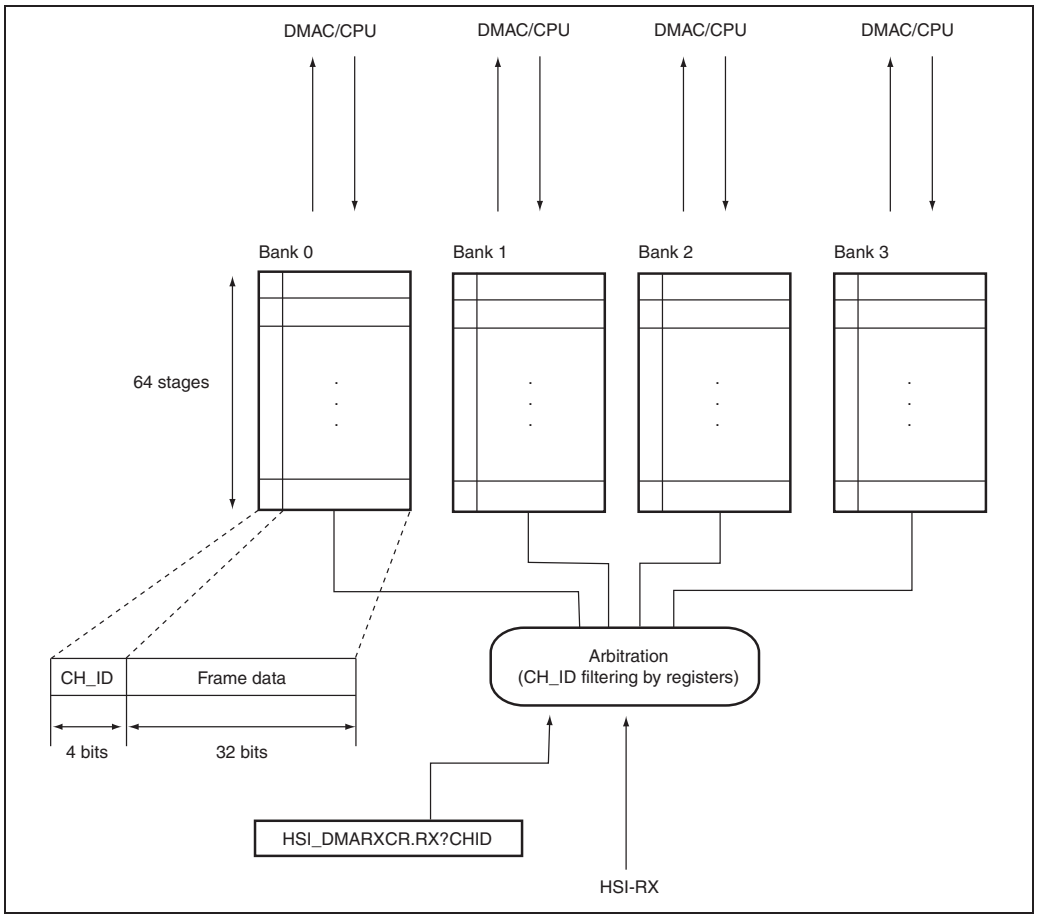


Figure 26.5 Reception FIFO

26.5.5 Transmission Procedure

(1) Transmission System

Transmission FIFO has four banks. Each bank can be operated in parallel and asynchronously.

When multiple banks are to be operated simultaneously, the round robin system is used in which the banks having transmission awaiting frames take turns with transmission each frame.

When transmission sequence is to be confirmed, transmit data using one bank at a time in a sequence.

(2) Preparation of Data to be Transmitted

Data to be transmitted to the memory can be prepared in the form of frame data only and in the form of CH_ID and frame data MIX (figure 26.6).

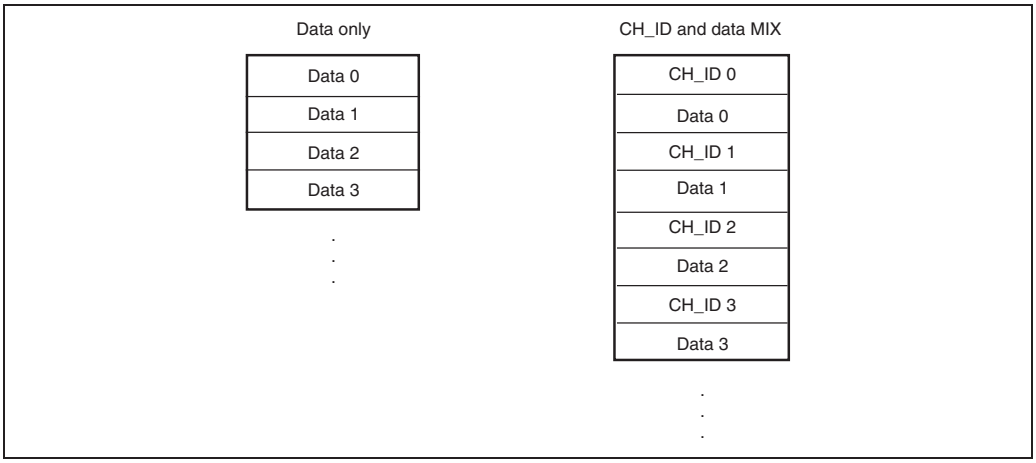


Figure 26.6 Memory Storage Form of Transmit Data

In the form of frame data only, the longword frame data is continuously arranged from the start address of the memory. In the form of CH_ID and frame data MIX, CH_ID that is arranged at the lower position of the longword and the corresponding longword frame data are arranged at alternate positions.

(3) Transmission Start Procedure

Change pin settings and select CAREADY, ACWAKE, ACFLAG, and ACDATA.

Set HSI_IOCR.ACWAKE to 1. Set HSI_TXRNCR, HSI_TXTOCR, HSI_TXBRKCR, and HSI_IRQCR and enable interrupts related to each error.

When carrying out data transfer using multiple banks, HSI_DMATXCR.TXDnASNEN and HSI_DMATXCR.TXDnCHID should also be set. When data is to be transferred through the CPU, HSI_IRQCR.TXFnEN should be set. When data is to be transferred through DMA, HSI_DMATXCR.TXDnEN should be set. For details, see sections 26.5.5 (4) and 26.5.5 (5). HSI_IRQCR.TXFnEN and HSI_DMATXCR.TXDnEN should not be used simultaneously.

When 1 is set to HSI_TXCR.TXSTART after carrying out the above settings, the transmission operation starts according to the settings simultaneously written to HSI_TXCR. Note that TXBRKLEN, TXRATE, TXRATEEN, TXCHLEN, and TXMODE set in HSI_TXCR should not be changed when the transmitter is being operated.

(4) Procedure for Transferring through CPU

(a) Frame Data Only (only banks 1 to 3)

When banks 1 to 3 are to be used, set HSI_DMATXCR.TXDnASNEN to 1 and set CH_ID that is to be assigned to HSI_DMATXCR.TXDnCHID. Check that there is enough space in the transmission FIFO by reading transmission FIFO interrupt or HSI_TXFSR and write frame data to HSI_TX_DATA1 to HSI_TX_DATA3. The transmission operation of HSI starts according to the transmission start procedure. Transmission can be started before or during writing the frame data.

When bank 0 is to be used, transmission in the form of frame data only cannot be carried out.

(b) CH_ID and Frame Data MIX

When bank n is to be used, check that there is enough space in the transmission FIFO by reading transmission FIFO interrupt or HSI_TXFSR, and alternately write the channel ID to HSI_TX_CHn and frame data to HSI_TX_DATAn. The transmission operation of HSI starts according to the transmission start procedure. Transmission can be started before or during writing the frame data.

(5) Procedure for Transferring through DMAC

(a) Frame Data Only

When banks 1 to 3 are to be used, set HSI_DMATXCR.TXDnASNEN to 1 and set CH_ID that is to be assigned to HSI_DMATXCR.TXDnCHID.

The transmission operation of HSI starts according to the transmission start procedure.

In the memory, data is stored in the form of frame data only.

Check that there is enough space in the transmission FIFO by reading transmission FIFO interrupt or HSI_TXFSR.

Specify HSI_TX_DATAn as a transfer destination of the DMAC and set and activate the DMAC.

Set HSI_DMATXCR.TXDnEN to the value other than 0. If the transmission FIFO has more space than specified, the DMA request is output according to the settings of HSI_DMATXCR.TXDnEN.

When transmission is carried out through the DMAC, the value set in HSI_TX_CHn is not used.

When bank 0 is to be used, transmission in the form of frame data only cannot be carried out.

(b) CH_ID and Frame Data MIX

The transmission operation of HSI starts according to the transmission start procedure.

In the memory, the data is stored in the form of CH_ID and frame data MIX.

Check that there is enough space in the transmission FIFO by reading transmission FIFO interrupt or HSI_TXFSR.

Check whether toggle bits of CH_ID and data of TX Ch_ID status register are 0. If any toggle bit is 1, set it to 0.

Specify HSI_TX_CHDATAn as the transfer destination of the DMAC and set and activate the DMAC.

Set HSI_DMATXCR.TXDnEN to the value other than 0. If the transmission FIFO has more space than specified, the DMA request is output according to the settings of HSI_DMATXCR.TXDnEN.

When the transmission is carried out through the DMAC, the value set in HSI_TX_CHn is not used.

(6) Executing Procedure for Break Transmission

If 1 is written to HSI_TXCR.TXBRK when data is being transmitted in the TX transmission start procedure, break transmission is executed at the boundary of the frame that is currently being transmitted. Once transmission is completed, 1 is set to HSI_IRQSR.TXBRK. After issuing the break transmission, 0 should be written to HSI_TXCR.TXBRK.

26.5.6 Reception Procedure

(1) Reception System

Reception FIFO has four banks. By specifying the specific CH_ID in banks 1 to 3, bank 0 and multiple banks can be operated simultaneously. Each bank can be operated in parallel and asynchronously.

When reception sequence is to be confirmed, receive data using one bank at a time.

(2) Memory Storage Method for Received Data

Received data can be stored in the memory in the form of frame data only and in the form of CH_ID and frame data MIX (figure 26.7).

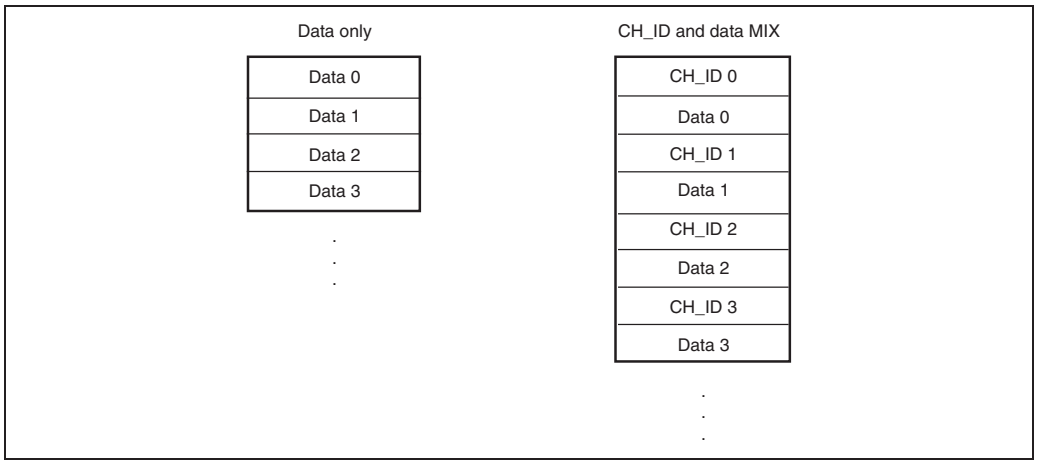


Figure 26.7 Memory Storage Form of Received Data

In the form of frame data only, the longword frame data is continuously arranged from the start address of the memory. In the form of CH_ID and frame data MIX, CH_ID that is arranged at the

lower position of the longword and the corresponding longword frame data are arranged at alternate positions.

(3) Reception Start Procedure

Change pin settings and select ACREADY, CAWAKE, CAFLAG, and CADATA.

Set HSI_RXTOCR, HSI_RXTLCR, HSI_RXDTOCR and HSI_IRQCR and enable interrupts related to each error.

When carrying out data transfer using multiple banks, HSI_DMARXCR.RXDnASNEN and HSI_DMARXCR.RXDnCHID should also be set. When data is to be transferred through the CPU, HSI_IRQCR.RXFnEN should be set. When data is to be transferred through DMA, HSI_DMARXCR.RXDnEN should be set. For details, see sections 26.5.6 (4) and 26.5.6 (5). HSI_IRQCR.RXFnEN and HSI_DMARXCR.RXDnEN should not be used simultaneously.

When 1 is set to HSI_RXCR.RXSTART after carrying out the above settings, the reception operation starts according to the settings simultaneously written to HSI_RXCR. Note that the value set in HSI_RXCR should not be changed when the receiver is being operated. When the transmitter of the opposite communication device is being operated, HSI_RXCR.RXSTART should not be set to 0.

(4) Procedure for Transferring through CPU

(a) Frame Data Only

When banks 1 to 3 are to be used, set HSI_DMARXCR.RXDnASNEN to 1 and set CH-ID that is to be assigned to HSI_DMARXCR.RXDnCHID.

The reception operation of this HSI starts according to the reception start procedure.

Check that the reception FIFO has received data by the reception FIFO frame reception interrupt or reading HSI_RXFSR.

When reading data that is received from bank 0, first, CH_ID is read from HSI_RX_CH0.

Next, the frame data is read from HSI_RX_DATA0.

When banks 1 to 3 are to be used, the CH_ID, which is set in HSI_DMARXCR.RXDnCHID, is used as the CH_ID. When the CH_ID is not necessary, the frame data is read from HSI_RX_DATAn. When the CH_ID is used, similarly as bank 0, the CH_ID is read from HSI_RX_CHn, and next, the frame data is read from HSI_RX_DATAn.

The next data is read from each bank of the reception FIFO by reading HSI_RX_DATAn, not by reading HSI_RX_CHn.

(b) CH_ID and Frame Data Mix

When banks 1 to 3 are to be used, set HSI_DMARXCR.RXDnASNEN to 1 and set CH_ID that is to be assigned to HSI_DMARXCR.RXDnCHID.

Check whether HSI_RX_CHSR.RXTOGn is 0, and if HSI_RX_CHSR.RXTOGn is 1, set it to 0.

The reception operation of this HSI starts according to the reception start procedure.

Check that the reception FIFO has received data by the reception FIFO frame reception interrupt or reading HSI_RXFSR. Data is read from HSI_RX_CHDATAn for each frame in the sequence of CH_ID and frame data.

(5) Procedure for Transferring through DMAC

(a) Frame Data Only

When banks 1 to 3 are to be used, set HSI_DMARXCR.RXDnASNEN to 1 and set CH_ID that is to be assigned to HSI_DMARXCR.RXDnCHID.

Specify HSI_RX_DATAn as the transfer source of the DMAC and set and activate the DMAC.

Set HSI_DMARXCR.RXDnEN to the value other than 0.

The reception operation of HSI starts according to the reception start procedure.

If reception FIFO receives data, the DMA request is output according to the settings of HSI_DMARXCR.RXDnEN.

DMA transfer with HSI_RX_DATA0 as the transfer source is possible even for bank 0. However, if the frames having different CH_ID have been received, the information of CH_ID is lost.

(b) CH_ID and Frame Data MIX

When banks 1 to 3 are to be used, set HSI_DMARXCR.RXDnASNEN to 1 and set CH_ID that is to be assigned to HSI_DMARXCR.RXDnCHID.

Check whether HSI_RX_CHSR.RXTOGn is 0, and if HSI_RX_CHSR.RXTOGn is 1, set it to 0.

Specify HSI_RX_CHDATAn as the transfer source of the DMAC and set and activate the DMAC.

Set HSI_DMARXCR.RXDnEN to the value other than 0. The reception operation of HSI starts according to the reception start procedure.

If reception FIFO receives data, the DMA request is output according to the settings of HSI_DMARXCR.RXDnEN.

26.5.7 Transmission Mode and Data Flow

The following shows the transmission modes and the types of data flow that can be selected. For details on each of the transmission modes and the data flow type, see MIPI-HSI Standards manual.

- Transmission modes: Stream mode, frame mode
- Data flow types: Synchronous data flow, pipelined data flow, receiver realtime data flow

26.5.8 Error and Status Notification

The HSI provides functions for error detection and status notification in both the transmitter and the receiver. This section describes each error source and status and the procedures for recovering from errors. The error detection function and status notification function in the transmitter and receiver work independently.

(1) Transmitter Errors

(a) Error Sources in Transmitter

The transmitter in the HSI can detect the following three types of error.

1. Transmission Overflow

   This error occurs when data is written to a transmission FIFO bank that has already become full. If this error occurs, the written data that caused the error is lost and HSI_IRQSR.TXOVF is set to 1. This error detection function is always enabled.

2. TX Ready Negation Timeout

   This error occurs when the opposite communication device continues negating CAREADY for a specified period. If this error occurs, HSI_IRQSR.TXRN is set. When HSI_TXRNCR.TXRNSTP is set to 1'b1, next frame transmission will not start and transmission will be temporarily suspended even if the opposite communication device asserts CAREADY after this error. In this case, clearing HSI_IRQSR.TXRN restarts transmission. This error detection function is enabled by setting HSI_IRQCR.TXRNEN. The timeout period before detection of this error should be specified in HSI_TXRNCR.TXRNC.

3. TX Timeout

   This error occurs when a valid frame stored in the transmission FIFO enters transmission wait state because the opposite communication device continues negating CAREADY for a specified period. If this error occurs, HSI_IRQSR.TXTO is set. When HSI_TXTOCR.TXTOSTP is set to 1'b1, frame transmission will not restart and temporary suspension of transmission will continue even if the opposite communication device asserts CAREADY after this error. In this case, clearing HSI_IRQSR.TXTO restarts transmission. This error detection function is enabled by setting HSI_IRQCR.TXTOEN to 1'b1. The timeout period before detection of this error should be specified in HSI_TXTOCR.TXTOC.

(b) Issuing Break Transmission

Writing 1'b1 to HSI_TXCR.TXBRK during operation in frame mode issues a break transmission at the frame boundary in the current transmission. The break transmission consists of a sequence of 0s whose length is one bit plus the number of bits specified in HSI_TXCR.TXBRKLEN. After a break transmission is completed, HSI_IRQSR.TXBRK is set to 1. Be sure to write 0 to HSI_TXCR.TXBRK after a break transmission. When HSI_TXBRKCR.TXBRKSTP is set to 1'b1, next frame transmission will not start and transmission will be temporarily suspended even if the opposite communication device asserts CAREADY. In this case, clearing HSI_TXCR.TXBRK restarts transmission.

(c) All Frame Transmission End Notification

When all data written to the transmission FIFO has been transmitted and there is no data waiting for transmission or being transmitted, HSI_IRQSR.TXEND is set to 1'b1; in other cases, it is cleared to 1'b0.

(d) Procedures for Recovering from Transmitter Errors

1. When Transmission Overflow has been Detected

   Some data that had been written by the CPU or DMAC has been lost. Clear HSI_IRQSR.TXOVF and then write the lost data again. HSI_IRQS.TXOVF is cleared by writing 0 when it is set to 1.

2. When TX Ready Negation Timeout or TX Timeout has been Detected

   A TX ready negation timeout or a TX timeout is detected when the opposite communication devices keeps CAREADY in non-asserted state for some reason. When the transmitter is in frame mode, issue a break transmission, and after the transmission, check that CAREADY is asserted. The CAREADY status can be checked through HSI_IOCR.CAREADY. When the opposite communication device keeps CAREADY in non-asserted state, the previous frame transmission might have been unsuccessful and the frame should be transmitted again. If CAREADY is not asserted even after a break transmission or if the transmitter is in stream mode, wait again for a certain period of time; if CAREADY is still in non-asserted state after that, restart the opposite communication device.

(2) Receiver Errors

(a) Error Sources in Receiver

The receiver in the HSI can detect the following five types of error.

1. Reception Overflow

   This error occurs when new frame reception is detected while the receiver negates ACREADY; that is, the receiver is not ready for new frame reception. If this error occurs, the receiver stops operation with ACREADY negated and sets HSI_IRQSR.RXOVF. The frame that caused the error and subsequent frames are not written to the reception FIFO. To restart frame reception, set HSI_RXCR.RXFLOW to 2'b10 or 2'b11 and then clear HSI_IRQSR.RXOVF. This error detection function is enabled by setting HSI_IRQCR.RXOVFEN to 1'b1.

2. Reception Underflow

   This error occurs when the reception FIFO is read when it has no valid frame. If this error occurs, the receiver does not stop operation but sets HSI_IRQSR.RXUDF. The frames received after this error will be written to the reception FIFO. This error detection function is enabled by setting HSI_IRQCR.RXUDFEN to 1'b1.

3. RX Drain Timeout

   This error occurs when the opposite communication device does not send any frame for a specified period while the receiver is in Receiver Realtime Data Flow. If this error occurs, the receiver does not stop operation but sets HSI_IRQSR.RXDTO. The receiver can detect suspension of the opposite communication device operation through this error. If this error is detected, clear HSI_RXCR.RXSTART to 1'b0 to stop the receiver. To restart reception after stopping the receiver, use the reception start procedure described before. This error detection function is enabled by setting HSI_IRQCR.RXDTOEN to 1'b1. The period before the receiver recognizes that the opposite communication device has stopped should be specified in HSI_RXDTOCR.

4. RX Tailing Bit Detection

   This error occurs when frame reception is detected before ACREADY is asserted after frame reception is completed while the receiver is in Synchronized Data Flow or Pipelined Data Flow. In Synchronized Data Flow, this error is detected every time a frame is received, and in Pipelined Data Flow, this error is detected in the state where ACREADY is negated. Note that this error is not detected for a sequence of 0s after reception of the last bit of a frame in frame mode. If this error occurs, the receiver stops operation with ACREADY negated and sets HSI_IRQSR.RXTL. The frame that caused the error and subsequent frames will not be written to the reception FIFO. To restart frame reception, set HSI_RXCR.RXFLOW to 2'b10 or 2'b11 and then clear HSI_IRQSR.RXTL. This error detection function is enabled by setting HSI_IRQCR.RXTLEN to 1'b1. The period before this error is detected (the period between completion of frame reception and reassertion of ACREADY) should be specified in HSI_RXTLCR. During this error detection period, ACREADY is not asserted, so the reception throughput is degraded when a long detection period is specified.

5. RX Reception Timeout

   This error occurs when frame reception is not completed within a specified period while the receiver is in Synchronized Data Flow or Pipelined Data Flow. If this error occurs, the receiver stops operation with ACREADY negated and sets HSI_IRQSR.RXTO. The frame that caused the error and subsequent frames will not be written to the reception FIFO. To restart frame reception, set HSI_RXCR.RXFLOW to 2'b10 or 2'b11 and then clear HSI_IRQSR.RXTO. This error detection function is enabled by setting HSI_IRQCR.RXTOEN to 1'b1. The period before this error is detected (the period between start and completion of frame reception) should be specified in HSI_RXTOCR.

(b) Receiving Break Transmission

The receiver detects a break transmission when receiving a sequence of 0s for the same number or a greater number of bits than specified in HSI_RXCR.RXBRKLEN while the receiver is in frame mode. The receiver detects a break transmission regardless of the HSI_IRQCR.RXBRKEN setting. If the receiver detects a break transmission in Synchronized Data Flow or Pipelined Data Flow, it continues working in Synchronized Data Flow or Pipelined Data Flow. If the receiver detects a break transmission while it is in Receiver Realtime Data Flow with HSI_RXCR.RXAFC set to 1'b1, it automatically enters Synchronized Data Flow when HSI_RXCR.RXFLOW is set to 2'b10 or Pipelined Data Flow when HSI_RXCR.RXFLOW is set to 2'b11. An interrupt can be generated when HSI_IRQCR.RXBRKEN is set to 1'b1. Note that even if the opposite communication device issues break transmissions twice or more in a row, the receiver detects them as a single break transmission. The length of the sequence of 0s sent as a break transmission from the opposite communication device should be two or more bits longer than the length of the sequence of 0s that can be recognized as a break transmission by the receiver in the HSI.

(c) Procedures for Recovering from Receiver Errors

1. When Reception Underflow has been Detected

   The read data includes invalid data. Discard the data and then clear HSI_IRQSR.RXUDF. HSI_IRQSR.RXUDF is cleared by writing 0 when it is set to 1.

2. When Reception Overflow, RX Tailing Bit, or RX Reception Timeout has been Detected (Including RX Drain Timeout Detection)

   Figure 26.8 shows the procedure for recovering from a reception overflow, RX tailing bit detection, or RX reception timeout detection error.

   When a reception overflow, RX tailing bit detection, or RX reception timeout error is detected while the receiver is in Synchronized Data Flow or Pipelined Data Flow, the receiver negates ACREADY, stops reception, and then sends an interrupt request to the CPU. Here, note that part of the data in the reception FIFO may be incorrect because synchronization has failed between the opposite communication device and the receiver. In this state, if a correct frame is received after recovering through the procedure described below, the reception FIFO will include a mixture of correct and incorrect data; to avoid this, read data from the reception FIFO before proceeding to the next step.

After reading data from the reception FIFO, modify HSI_RXCR.RXFLOW. If the receiver was in Synchronized Data Flow when the error was detected, modify HSI_RXCR.RXFLOW to 2'b10: if the receiver was in Pipelined Data Flow, modify HSI_RXCR.RXFLOW to 2'b11. When modifying HSI_RXCR, be careful not to modify any bits other than HSI_RXCR.RXFLOW. After that, clearing all of HSI_IRQSR.RXOVF, HSI_IRQSR.RXTL, and HSI_IRQSR.RXTO restarts reception in Receiver Realtime Data Flow. The HSI_IRQSR.RXOVF, HSI_IRQSR.RXTL, and HSI_IRQSR.RXTO error flags are cleared by writing 0 when they are set to 1. The data received here in Receiver Realtime Data Flow is invalid because it is received in the state where synchronization has failed between the opposite communication device and the receiver, and therefore this data is not written to the reception FIFO.

When data is received in Receiver Realtime Data Flow mode, if HSI_RXCR.RXMODE is 1 (frame mode) and HSI_RXCR.RXAFC is 1, the receiver is automatically recovered to Synchronized Data Flow or Pipelined Data Flow upon detection of a break transmission. In this case, the receiver enters Synchronized Data Flow when HSI_RXCR.RXFLOW is set to 2'b10 or Pipelined Data Flow when HSI_RXCR.RXFLOW is set to 2'b11. After completion of this transition to a new Flow, the frames received after a break transmission are written to the reception FIFO.

Likewise, when data is received in Receiver Realtime Data Flow, if HSI_IRQCR.RXDTOEN is 1, the RX drain timeout detection function is enabled. The RX drain timeout detection function detects the period where the opposite communication device transmits nothing. Through RX drain timeout detection and interrupt generation, suspension of the opposite communication device due to a hang-up or a wait for a handshake can be detected to restart the receiver of the HSI. To restart the receiver, clear HSI_RXCR.RXSTART to 0, make the necessary settings for reception again, and then set HSI_RXCR.RXSTART to 1. When specifying the period before detection of an RX drain timeout, be sure to specify a large enough value in HSI_RXDTOCR to prevent restart of the receiver during operation of the opposite communication device.

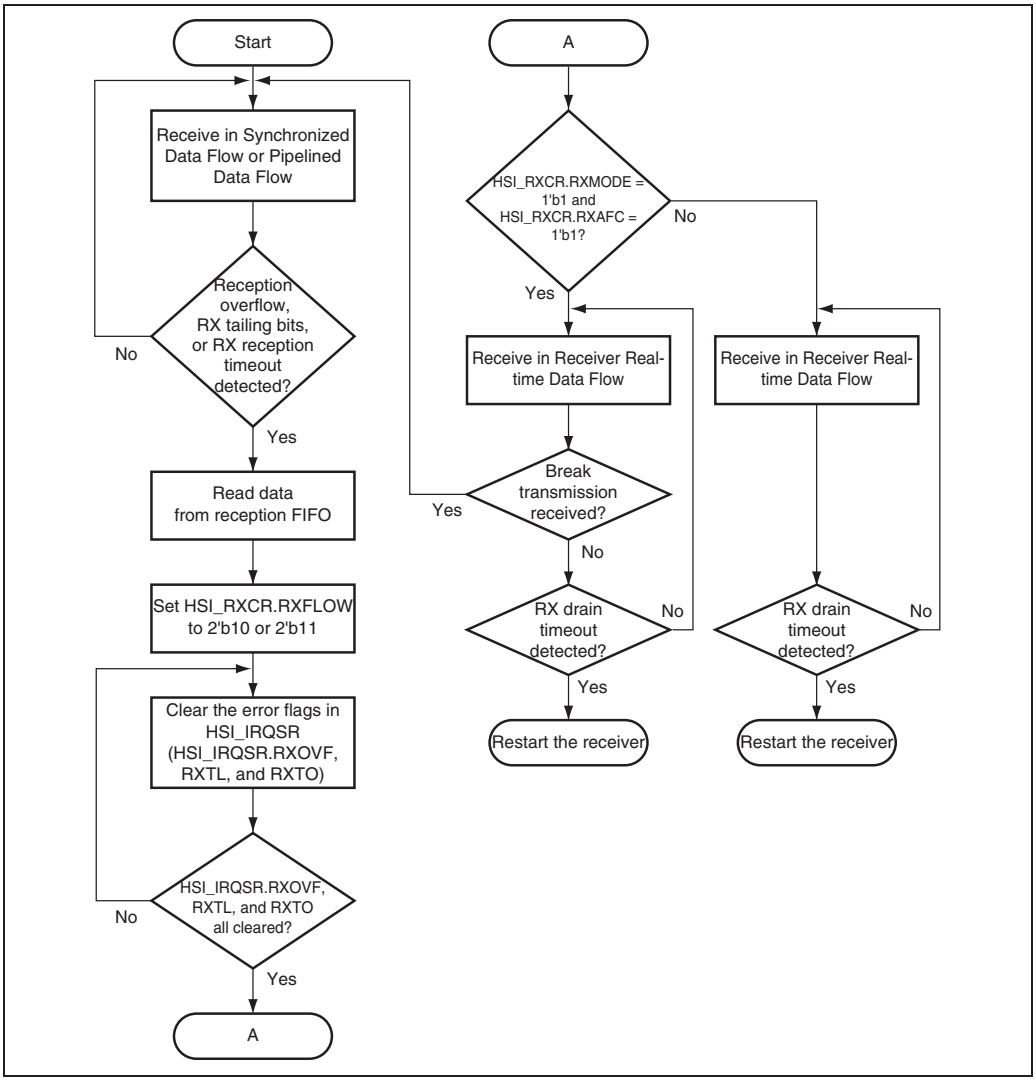


Figure 26.8 Procedure for Recovering from Reception Overflow, RX Tailing Bit Detection, or RX Reception Timeout Detection Error

26.5.9 Interrupts

The following table shows the interrupt sources in this module and the enable bits that enable or disable the interrupt sources. Some interrupt sources can activate the DMAC using the DMA request instead of enabling the interrupt.

Status Bit (HSI_IRQSR)	Enable Bit (HSI_IRQCR)	Content	DMAC Activation
TXOVF	TXOVFEN	Transmission overflow interrupt	Impossible
RXOVF	RXOVFEN	Reception overflow interrupt	Impossible
RXUDF	RXUDFEN	Reception underflow interrupt	Impossible
RXFn	RXFnEN	Reception FIFO bank n interrupt	Possible
TXFn	RXFnEN	Transmission FIFO bank n interrupt	Possible
TXRN	TXRNEN	TX ready negation timeout interrupt	Impossible
TXTO	TXTOEN	TX timeout interrupt	Impossible
RXDTO	RXDTOEN	RX drain timeout detection interrupt	Impossible
RXTL	RXTLEN	RX tailing bit detection interrupt	Impossible
RXTO	RXTOEN	RX reception timeout interrupt	Impossible
RXBRK	RXBRKEN	RX break-transmission reception interrupt	Impossible
TXBRKEND	TXBRKENDEN	TX break-transmission end interrupt	Impossible
TXEND	TXENDEN	TX frame transmission end interrupt	Impossible

Section 27 Multi Media Card Interface (MMCIF)

This module is a host interface supports JEDEC STANDARD JESD84-A43.This module allows connection with Multi Media Card (referred to as MMC hereafter), which is a flash memory card, or HDD that conforms to the Consumer Electronics AT Attachment (CE-ATA) standard, which is an applied version of MMC standard.

27.1 Features

- Supports 1/4/8-bit MMC
- Supports Boot Operation
- MMC clock frequency ≤ 1/2 × bus clock frequency (HPϕ).
- Supports change MMC clock frequency during Boot Operation
- Data buffer : 512 × 2
- Two types of interrupt requests: normal operation and error/timeout.
- DMA transfer requests: buffer write and buffer read
- Supports Command Completion Signal (CCS) and Command Completion Signal Disable (CCSD)

Figure 27.1 shows a block diagram of this module.

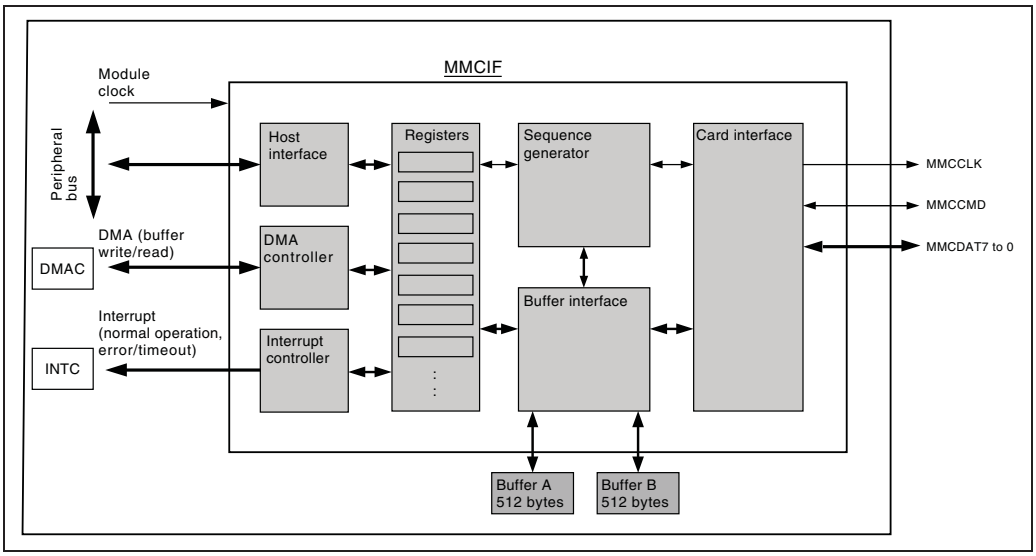


Figure 27.1 Block Diagram of MMCIF

27.2 Input/Output Pins

Table 27.1 shows the pin configuration of the MMCIF.

Table 27.1 Pin Configuration

Pin Name	I/O	Function
MMCCLK	Output	MMC clock
MMCCMD	Input/output	Command/response
MMCDAT[7:0]	Input/output	Transmit/receive data

27.3 Register Descriptions

Table 27.2 shows the register configuration of the MMCIF and Table 27.3 shows the register state in each processing mode.

Table 27.2 Register Configuration

Register Name	Abbreviation	R/W	Address	Access Size
Command setting register	CE_CMD_SET	R/W	H'E6BD0000	16, 32
Argument register	CE_ARG	R/W	H'E6BD0008	16, 32
Argument register for automatically-issued CMD12	CE_ARG_CMD12	R/W	H'E6BD000C	16, 32
Command control register	CE_CMD_CTRL	R/W	H'E6BD0010	16, 32
Transfer block setting register	CE_BLOCK_SET	R/W	H'E6BD0014	16, 32
Clock control register	CE_CLK_CTRL	R/W	H'E6BD0018	16, 32
Buffer access configuration register	CE_BUF_ACC	R/W	H'E6BD001c	16, 32
Response register 3	CE_RESP3	R/W	H'E6BD0020	16, 32
Response register 2	CE_RESP2	R/W	H'E6BD0024	16, 32
Response register 1	CE_RESP1	R/W	H'E6BD0028	16, 32
Response register 0	CE_RESP0	R/W	H'E6BD002C	16, 32
Response register for automatically-issued CMD12	CE_RESP_CMD12	R/W	H'E6BD0030	16, 32
Data register	CE_DATA	R/W	H'E6BD0034	16*, 32
Boot Operation setting register	CE_BOOT	R/W	H'E6BD003C	16, 32
Interrupt flag register	CE_INT	R/W	H'E6BD0040	16, 32
Interrupt enable register	CE_INT_MASK	R/W	H'E6BD0044	16, 32
Status register 1	CE_HOST_STS1	R/W	H'E6BD0048	16, 32
Status register 2	CE_HOST_STS2	R/W	H'E6BD004C	16, 32
Version register	CE_VERSION	R/W	H'E6BD007C	16, 32

Notes: Do not access registers other than those shown above.

* For 16-bit access, H'E6BD0034 is the only address for access.

Table 27.3 Register state in each Processing mode

Abbreviation	Reset *	Module standby
CE_CMD_SET	Initialized	Retained
CE_ARG	Initialized	Retained
CE_ARG_CMD12	Initialized	Retained
CE_CMD_CTRL	Initialized	Retained
CE_BLOCK_SET	Initialized	Retained
CE_CLK_CTRL	Initialized	Retained
CE_BUF_ACC	Initialized	Retained
CE_RESP3	Initialized	Retained
CE_RESP2	Initialized	Retained
CE_RESP1	Initialized	Retained
CE_RESP0	Initialized	Retained
CE_RESP_CMD12	Initialized	Retained
CE_DATA	Initialized	Retained
CE_BOOT	Initialized	Retained
CE_INT	Initialized	Retained
CE_INT_MASK	Initialized	Retained
CE_HOST_STS1	Initialized	Retained
CE_HOST_STS2	Initialized	Retained
CE_VERSION	Initialized	Retained

* For details, refer to section 1-D Overview of reset

27.3.1 Command Setting Register (CE_CMD_SET)

CE_CMD_SET sets a command sequence. The command sequence starts when a command index has been set along with other required settings. If this register is accessed in 16-bit units, the command sequence starts when the settings have been made in bits 31 to 16. Note that writing to CE_CMD_SET is disabled while a command sequence is proceeding (i.e., the value of CMDSEQ in CE_HOST_STS1 is 1). For the setting values of CE_CMD_SET, see section 27.7.17, Setting Values of CE_CMD_SET.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	BOOT	CMD[5:0]						RTYP[1:0]		RBSY	CCSEN	WDAT	DWEN	CMLTE	CMD12EN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RIDXC[1:0]		RCRC7C[1:0]		—	CRC16C	BOOTACK	CRCSTE	TBIT	OPDM	CCSH	—	—	—	DATW[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
30	BOOT	0	R/W	Boot Operation 0: command sequence without Boot Operation 1: command sequence with Boot Operation
29 to 24	CMD[5:0]	All 0	R/W	Command Index Note: Setting a command index in these bits initiates the command sequence.
23, 22	RTYP[1:0]	00	R/W	Response Type 00: No response 01: 6-byte response (R1, R1b, R3, R4, R5) 10: 17-byte response (R2) 11: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Description
21	RBSY	0	R/W	Response Busy Select Selects whether “busy” is involved in response reception. 0: No response busy 1: Response busy involved (R1b)
20	CCSEN	0	R/W	CCS Acceptance 0: Acceptance of CCS disabled 1: Acceptance of CCS enabled
19	WDAT	0	R/W	Presence/Absence of Data 0: No data 1: With data
18	DWEN	0	R/W	Read/Write 0: Read from the card 1: Write to the card
17	CMLTE	0	R/W	Single/Multi Block Transfer Select 0: Single-block transfer 1: Multi-block transfer
16	CMD12EN	0	R/W	Automatic CMD12 Issuance (valid when multi-block transfer is selected) 0: Disables automatic CMD12 issuance 1: Enables automatic CMD12 issuance Note: Set the transfer block size to 512 bytes. Set RBSY bit to 0
15, 14	RIDXC[1:0]	00	R/W	Response Index Check 00: Checks the response index 01: Checks the check bits 10: No checking 11: Setting prohibited
13, 12	RCRC7C [1:0]	00	R/W	Response CRC7 Check 00: Checks CRC7 (set the response type to 01) 01: Checks the check bits (set the response type to 01) 10: Checks internal CRC7 (R2 only) (set the response type to 10) 11: No checking

Bit	Bit Name	Initial Value	R/W	Description
11	—	0	R	Reserved The write value should always be 0.
10	CRC16C	0	R/W	CRC16 Check in Reception 0: Checks CRC16 1: Does not check CRC16 (use when CMD14)
9	BOOTACK	0	R/W	Boot Acknowlege Reception 0:Does not receive Boot Acknowledge 1:Receives Boot Acknowledge
8	CRCSTE	0	R/W	CRC Status Reception 0: Receives CRC status 1: Does not receive CRC status (use when CMD19)
7	TBIT	0	R/W	Transmission Bit Setting 0: Sets the transmission bit to high 1: Sets the transmission bit to low
6	OPDM	0	R/W	Open-Drain Output Mode 0: Normal output 1: Open-drain output Note: This setting is only applied to the MMCCMD line.
5	CCSH	0	R/W	Output High after CCS Reception 0: Outputs a high level at the third cycle after CCS is received 1: Does not output a high level after CCS is received
4 to 2	—	000	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	DATW[1:0]	00	R/W	Data Bus Width Setting 00: 1 bit 01: 4 bits 10: 8 bits 11: Setting prohibited

27.3.2 Argument Register (CE_ARG)

CE_ARG sets the argument for the command to be transmitted. This register must be set before CMD[5:0] in CE_CMD_SET is set.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ARG[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ARG[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	ARG[31:0]	H'00000000	R/W	Set bits 31 to 0 of the argument. Note: Set argument for the automatically-issued CMD12 in CE_ARG_CMD12

27.3.3 Argument Register for Automatically-Issued CMD12 (CE_ARG_CMD12)

CE_ARG_CMD12 is used to set the argument for the automatically-issued CMD12 in multi-block transfer. This register must be set before CMD[5:0] in CE_CMD_SET is set. For automatic issuance of CMD12, see section 27.6.4, Automatic CMD12 Issuance.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	C12ARG[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	C12ARG[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	C12ARG[31:0]	H'00000000	R/W	Set bits 31 to 0 of the argument.

27.3.4 Command Control Register (CE_CMD_CTRL)

CE_CMD_CTRL is used to terminate a command sequence forcibly.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CCSD	BREAK
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	CCSD	1'b0	R/W	CCSD Issuance Writing 1 to this bit while it is 0 issues a CCSD. After making sure that the CCSDE bit in CE_INT has become 1, write 0 to this bit to reset. Note: Before issuing a CCSD, make sure that the value of the CMDSEQ bit in CE_HOST_STS1 is 0.
0	BREAK	1'b0	R/W	Forcible Termination of Command Sequence Writing 1 to this bit while it is 0 and then writing 0 to it discontinues the current command sequence. Note: After this bit is set as described above, check if the value of the CMDSEQ bit in CE_HOST_STS1 has become 0, which indicates that the next processing can be performed.

27.3.5 Transfer Block Setting Register (CE_BLOCK_SET)

CE_BLOCK_SET specifies the size of the block and the number of blocks for the data to be transferred. This register must be set before CMD[5:0] in CE_CMD_SET is set.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	BLKCNT[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BLKSIZ[15:0]															
Initial value:	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	BLKCNT [15:0]	H'0000	R/W	Number of Blocks for Transfer Note: This setting is valid for multi-block transfer.
15 to 0	BLKSIZ [15:0]	H'0200	R/W	Transfer Block Size Note: Transfer block size should be set as follows. • Single-block transfer: 1 to 512 bytes • Multi-block transfer: 512 bytes

27.3.6 Clock Control Register (CE_CLK_CTRL)

CE_CLK_CTRL controls the MMC clock and sets timeout values. Do not change the setting of this register while a command sequence is in progress.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	CLKEN	—	—	—	—	CLKDIV[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	SRSPTO[1:0]		SRBSYTO[3:0]				SRWDTO[3:0]				SCCSTO[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	CLKEN	0	R/W	MMC Clock Output Control 0: Does not output the MMC clock (tied to low level) 1: Outputs the MMC clock
23 to 20	—	00	R	Reserved These bits are always read as 0. The write value should always be 0.
19 to 16	CLKDIV[3:0]	0000	R/W	MMC Clock Frequency Setting 0000: Bus clock/2 0001: Bus clock/2^2 : 0111: Bus clock/2^8 1000: Bus clock/2^9 1001 to 1111: Setting prohibited See section 27.6.5 MMC clock operation during Boot Operation and 27.3.11 Boot Operation register(CE_BOOT) about Boot Operation
15,14	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
13, 12	SRSPTO [1:0]	00	R/W	Response Timeout Setting Specifies the timeout period for the RSPTO bit of CE_INT. 00: 64 MMC clock cycles 01: 128 MMC clock cycles 10: 256 MMC clock cycles 11: Setting prohibited
11 to 8	SRBSYTO [3:0]	0000	R/W	Response Busy Timeout Setting Specifies the timeout period for the RBSYTO bit of CE_INT. 0000: 2^{14} MMC clock cycles 0001: 2^{15} MMC clock cycles : 1110: 2^{28} MMC clock cycles 1111: 2^{29} MMC clock cycles
7 to 4	SRWDTO [3:0]	0000	R/W	Write Data/Read Data Timeout Setting Specifies the timeout period for the WDATTO and RDATTO bits of CE_INT. 0000: 2^{14} MMC clock cycles 0001: 2^{15} MMC clock cycles : 1110: 2^{28} MMC clock cycles 1111: 2^{29} MMC clock cycles
3 to 0	SCCSTO [3:0]	0000	R/W	CCS Timeout Setting Specifies the timeout period for the CCSTO bit of CE_INT. 0000: 2^{14} MMC clock cycles 0001: 2^{15} MMC clock cycles : 1110: 2^{28} MMC clock cycles 1111: 2^{29} MMC clock cycles

27.3.7 Buffer Access Configuration Register (CE_BUF_ACC)

CE_BUF_ACC configures the method of accessing data registers and mode of DMA transfer. This register must be set before CMD[5:0] in CE_CMD_SET is set. For explanation of the buffers, see section 27.6.3, Buffer Structure and Access Buffer.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	DMAWEN	DMAREN	—	—	—	—	—	—	BUSW	ATYP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

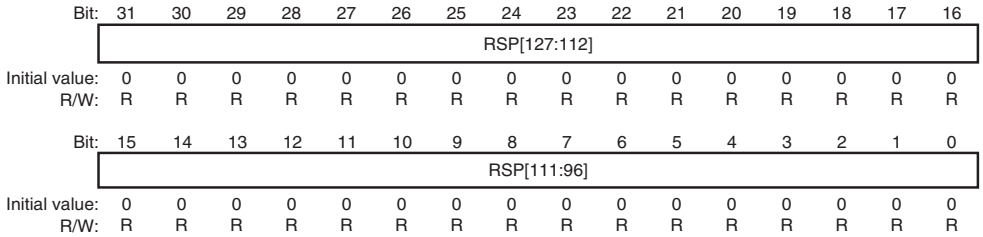
Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25	DMAWEN	0	R/W	Buffer Write DMA Transfer Request Enable 0: Disables DMA transfer request for buffer writing 1: Enables DMA transfer request for buffer writing
24	DMAREN	0	R/W	Buffer Read DMA Transfer Request Enable 0: Disables DMA transfer request for buffer reading 1: Enables DMA transfer request for buffer reading
23 to 18	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
17	BUSW	0	R/W	Data register access size selection 0: When access to CE_DATA in 32-bit. 1: When access to CE_DATA in 16-bit.
16	ATYP	0	R/W	Select access buffer 0: Without swapped byte-wise 1: With swapped byte-wise. Note: See section 27.6.3 Buffer Structure and Access Buffer

Bit	Bit Name	Initial Value	R/W	Description
15 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

27.3.8 Response Registers 3 to 0 (CE_RESP3 to CE_RESP0)

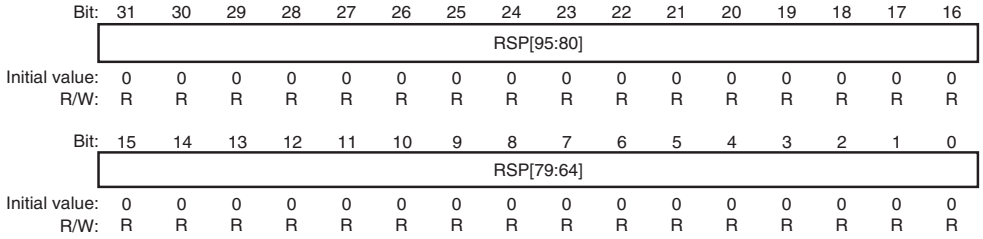
CE_RESP3 to CE_RESP0 are the registers for storing the response that has been received. For the formats of response values, see section 27.6.1, Command/Response Formats.

- CE_RESP3



Bit	Bit Name	Initial Value	R/W	Description (CE_RESP3)
31 to 0	RSP[127:96]	H'00000000	R	R2 response [127:96]

- CE_RESP2



Bit	Bit Name	Initial Value	R/W	Description (CE_RESP2)
31 to 0	RSP[95:64]	H'00000000	R	R2 response [95:64]

- CE_RESP1

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RSP[63:48]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RSP[47:32]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description (CE_RESP1)
31 to 0	RSP[63:32]	H'00000000	R	R2 response [63:32]

- CE_RESP0

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RSP[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RSP[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description (CE_RESP0)
31 to 0	RSP[31:0]	H'00000000	R	Response [31:0] or R2 response [31:0]

27.3.9 Response Register for Automatically-Issued CMD12 (CE_RESP_CMD12)

CE_RESP_CMD12 is the register for storing the response to the automatically-issued CMD12.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RSP12[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RSP12[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	RSP12[31:0]	H'00000000	R	CMD12 response [31:0]

27.3.10 Datta Register (CE_DATA)

CE_DATA is used to access the buffers of this module. In 16-bit access, only DATA[31:16] is accessible. For the write/read data formats, see section 27.6.2, Data Formats.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DATA[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DATA[31:0]	H'00000000	R/W	Buffer write/read data [31:0]

27.3.11 Boot Operation setting Register (CE_BOOT)

CE_BOOT is the register for setting MMC clock frequency and the timeout period for Boot Operation. Do not change the setting of this register while a command sequence is in progress.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	BTCLKDIV[3:0]				SBTACKTO[3:0]				S1STBTDATTO[3:0]				SBTDATTO[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	BTCLKDIV [3:0]	0000	R/W	MMC Clock Frequency Setting for Boot Operation 0000: Bus clock/2 0001: Bus clock/2^2 : 0111: Bus clock/2^8 1000: Bus clock/2^9 1001 to 1111: Setting prohibited Set value less than CE_CLK_CTRL.CLKDIV to BTCLKDIV See section 27.6.5 MMC clock operation during Boot Operation
27 to 24	SBTACKTO [3:0]	0000	R/W	Boot Acknowledge Timeout Setting 0000: 2^{14} MMC clock cycles 0001: 2^{15} MMC clock cycles : 1110: 2^{28} MMC clock cycles 1111: 2^{29} MMC clock cycles

Bit	Bit Name	Initial Value	R/W	Description
23 to 20	S1STBTDATTO[3:0]	0000	R/W	1st Boot Timeout Setting 0000: 2^{14} MMC clock cycles 0001: 2^{15} MMC clock cycles : 1110: 2^{28} MMC clock cycles 1111: 2^{29} MMC clock cycles
19 to 16	SBTDATTO[3:0]	0000	R/W	Boot Interval Timeout Setting 0000: 2^{14} MMC clock cycles 0001: 2^{15} MMC clock cycles : 1110: 2^{28} MMC clock cycles 1111: 2^{29} MMC clock cycles
15 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

27.3.12 Interrupt Flag Register (CE_INT)

CE_INT indicates various statuses during execution of a command sequence. Each bit is set when its setting condition has been met. To clear flag(s), write 0 only to the bit(s) to be cleared and write 1 to the other bits.

For the operation in the case of an error or timeout, see section 27.6.6, Operation in the Case of Error/Timeout.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	CCSDE	—	—	CMD12 DRE	CMD12 RBE	CMD12 CRE	DTRAN E	BUFR E	BUFW EN	BUFR EN	CCS RCV	—	RBSY E	CRSP E
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMD VIO	BUF VIO	—	—	WDAT ERR	RDAT ERR	RIDX ERR	RSP ERR	—	—	CCS TO	CRCS TO	WDAT TO	RDAT TO	RBSY TO	RSP TO
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	00	R	Reserved These bets are always read as 0. The writing value should always be 0.
29	CCSDE	0	R/W*	CCSD Issuance Complete [Setting conditions] CCSD has been issued [Clearing condition] Writing a 0 to this bit
28, 27	—	00	R	Reserved These bets are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
26	CMD12DRE	0	R/W*	Automatic CMD12 Issuance & Buffer Read Complete [Setting conditions] Response busy for automatically-issued CMD12 and buffer reading have been completed. [Clearing condition] Writing a 0 to this bit Note: When CMD12DRE has been set, CMD12RBE, CMD12CRE, and BUFRE have also been set. So, these bits should be cleared as well.
25	CMD12RBE	0	R/W*	Automatic CMD12 Issuance Response Busy Complete [Setting conditions] Reception of the response and response busy for an automatically-issued CMD12 have been completed. [Clearing condition] Writing a 0 to this bit Note: When CMD12RBE has been set, CMD12CRE has also been set. So, this bit should be cleared as well.
24	CMD12CRE	0	R/W*	Automatic CMD12 Response Complete [Setting conditions] The response to an automatically-issued CMD12 has been received. [Clearing condition] Writing a 0 to this bit
23	DTRANE	0	R/W*	Data Transmission Complete [Setting conditions] Transmission of all blocks of data has been completed. • When configured to receive CRC status: Completion of busy (data busy) after reception of CRC status • When configured not to receive CRC status: Completion of data transmission [Clearing condition] Writing a 0 to this bit

Bit	Bit Name	Initial Value	R/W	Description
22	BUFRE	0	R/W*	Buffer Read Complete [Setting conditions] All blocks of data have been received and the data have been read from the buffer [Clearing condition] Writing a 0 to this bit
21	BUFWEN	0	R/W*	Buffer Write Ready [Setting conditions] The buffer has become empty and ready for writing. [Clearing condition] Writing a 0 to this bit Note: This bit is not set when DMA transfer request for buffer writing is enabled.
20	BUFREN	0	R/W*	Buffer Read Ready [Setting conditions] Transfer block size of data have been stored in the buffer and it has become ready for reading [Clearing condition] Writing a 0 to this bit Note: This bit is not set when DMA transfer request for buffer reading is enabled.
19	CCSRCV	0	R/W*	CCS Reception Complete [Setting conditions] CCS has been received. [Clearing condition] Writing a 0 to this bit
18	—	0	R	Reserved This bet is always read as 0.The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
17	RBSYE	0	R/W*	Response Busy Complete [Setting conditions] Reception of a response and response busy have been completed. [Clearing condition] Writing a 0 to this bit Note: When RBSYE has been set, CRSPE has also been set. So, this bit should be cleared as well. Completion of reception of the response and response busy for automatically-issued CMD12 is reflected in CMD12RBE.
16	CRSPE	0	R/W*	Command/Response Complete [Setting conditions] A command has been transmitted or a response has been received • When configured not to receive response: A command has been transmitted • When configured to receive 6- or 17-byte response: A response has been received [Clearing condition] Writing a 0 to this bit Note: Completion of reception of the response to automatically-issued CMD12 is reflected in CMD12CRE.

Bit	Bit Name	Initial Value	R/W	Description
15	CMDVIO	0	R/W*	Command Issuance Error [Setting conditions] Illegal setting has been made in CE_CMD_SET or CE_BLOCK_SET. • During execution of a command sequence: Writing to CMD[5:0] in CE_CMD_SET • At the start of command sequence: Writing to CMD[5:0] in CE_CMD_SET when the registers have been set for one of the following combinations of selection — No response + response busy — No response + with data — No response + acceptance of CCS enabled — No data + automatic CMD12 issuance — With data + single-block transfer + automatic CMD12 issuance — With data + automatic CMD12 issuance + acceptance of CCS enabled — With data + transfer block size = 0 — With data + transfer block size ≥ 513 — With data + multi-block transfer + number of blocks for transfer = 0 [Clearing condition] Writing a 0 to this bit Note: When CMDVIO has been set, the command sequence is not stopped automatically.

Bit	Bit Name	Initial Value	R/W	Description
14	BUFVIO	0	R/W*	Buffer Access Error [Setting conditions] Illegal buffer access has been attempted. • CE_ DATA has been accessed exceeding the block size set in BLKSIZ[15:0] in CE_BLOCK_SET • While data is being read from the card: CE_DATA has been accessed with BUFREN not set (when DMA is used, with no DMA transfer request asserted for buffer reading) • While data is being written to the card: CE_DATA has been accessed with BUFWEN not set (when DMA is used, with no DMA transfer request asserted for buffer writing) [Clearing condition] Writing a 0 to this bit Note: When BUFVIO has been set, the command sequence is not stopped automatically.
13, 12	—	00	R	Reserved These bits are always read as 0. The write value should always be 0.
11	WDATERR	0	R/W*	Write Data Error [Setting conditions] Error is found in the data that has been written. • Error is in the status of the CRC status • Error is in the end bits of the CRC status [Clearing condition] Writing a 0 to this bit Note: When WDATERR has been set, the command sequence is stopped automatically.

Bit	Bit Name	Initial Value	R/W	Description
10	RDATERR	0	R/W*	Read Data Error [Setting conditions] Error is found in the read data. • Error is in CRC16 of the read data • Error is in the end bits of the read data [Clearing condition] Writing a 0 to this bit Note: When RDATERR has been set, the command sequence is stopped automatically.
9	RIDXERR	0	R/W*	Response Index Error [Setting conditions] Error has been found in the index value of the response. • When RIDXC[1:0] in CE_CMD_SET is 2'b00: The index value in the received response does not match that of the transmitted command • When RIDXC[1:0] in CE_CMD_SET is 2'b01: The check bits are not all 1 [Clearing condition] Writing a 0 to this bit Note: When RIDXERR has been set, the command sequence is stopped automatically.

Bit	Bit Name	Initial Value	R/W	Description
8	RSPERR	0	R/W*	Response Error [Setting conditions] Error has been found in the response values of the response. • Transmission bit in the response is high • Error is in the end bits of the response • When RCRC7C[1:0] in CE_CMD_SET is 2'b00: Error is in CRC7 of the response • When RCRC7C [1:0] in CE_CMD_SET is 2'b01: The check bits are not all 0 • When RCRC7C[1:0] in CE_CMD_SET is 2'b10: Error is in internal CRC7 of the response [Clearing condition] Writing a 0 to this bit Note: When RSPERR has been set, the command sequence is stopped automatically.
7, 6	—	00	R	Reserved These bits are always read as 0. The write value should always be 0.
5	CCSTO	0	R/W*	CCS Timeout [Setting conditions] CCS could not be received [Clearing condition] Writing a 0 to this bit Note: The period for timeout detection is set in SCCSTO[3:0] of CE_CLK_CTRL. The command sequence is not stopped even if CCSTO is set.
4	CRCSTO	0	R/W*	CRC Status Timeout [Setting conditions] CRC status could not be received [Clearing condition] Writing a 0 to this bit Note: The command sequence is not stopped even if CRCSTO is set.

Bit	Bit Name	Initial Value	R/W	Description
3	WDATTO	0	R/W*	Write Data Timeout [Setting conditions] Data busy that follows CRC status does not end [Clearing condition] Writing a 0 to this bit Note: The period for timeout detection is set in SRWDTO[3:0] of CE_CLK_CTRL. The command sequence is not stopped even if WDATTO is set.
2	RDATTO	0	R/W*	Read Data Timeout [Setting conditions] Read data could not be received [Clearing condition] Writing a 0 to this bit Note: The period for timeout detection is set in SRWDTO[3:0] of CE_CLK_CTRL. The command sequence is not stopped even if RDATTO is set.
1	RBSYTO	0	R/W*	Response Busy Timeout [Setting conditions] Response busy does not end [Clearing condition] Writing a 0 to this bit Note: The period for timeout detection is set in SRBSYTO[3:0] of CE_CLK_CTRL. The command sequence is not stopped even if RBSYTO is set.
0	RSPTO	0	R/W*	Response Timeout [Setting conditions] Response could not be received [Clearing condition] Writing a 0 to this bit Note: The period for timeout detection is set in SRSPTO[1:0] of CE_CLK_CTRL. The command sequence is not stopped even if RSPTO is set.

Note: * A 0 is the only value that can be written to these bits. Writing a 1 is ignored.

27.3.13 Interrupt Mask Register (CE_INT_MASK)

CE_INT_MASK controls output of the CE_INT-related interrupt signals. If a flag in CE_INT is set to 1 while its corresponding bit in CE_INT_MASK is set to 1, an interrupt request is output. For details on interrupt requests, see section 27.4, Interrupt Requests.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	MCCSDE	—	—	MCMD12DRE	MCMD12RBE	MCMD12CRE	MDTRANE	MBUFRE	MBUFWEN	MBUFREN	MCCSRCV	—	MRBSYE	MCRSPE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MCMDVIO	MBUFVIO	—	—	MWDATERR	MRDATERR	MRIDXERR	MRSPERR	—	—	MCCSTO	MCRCSTO	MWDATTO	MRDATTO	MRBSYTO	MRSPTO
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	00	R*	Reserved These bits are always read as 0. The write value should always be 0.
29	MCCSDE	0	R/W	CCSDE Interrupt Mask 0: Disables interrupt output by the CCSDE flag 1: Enables interrupt output by the CCSDE flag
28, 27	—	00	R*	Reserved These bits are always read as 0. The write value should always be 0.
26	MCMD12DRE	0	R/W	CMD12DRE Interrupt Mask 0: Disables interrupt output by the CMD12DRE flag 1: Enables interrupt output by the CMD12DRE flag
25	MCMD12RBE	0	R/W	CMD12RBE Interrupt Mask 0: Disables interrupt output by the CMD12RBE flag 1: Enables interrupt output by the CMD12RBE flag
24	MCMD12CRE	0	R/W	CMD12CRE Interrupt Mask 0: Disables interrupt output by the CMD12CRE flag 1: Enables interrupt output by the CMD12CRE flag
23	MDTRANE	0	R/W	DTRANE Interrupt Mask 0: Disables interrupt output by the DTRANE flag 1: Enables interrupt output by the DTRANE flag

Bit	Bit Name	Initial Value	R/W	Description
22	MBUFRE	0	R/W	BUFRE Interrupt Mask 0: Disables interrupt output by the BUFRE flag 1: Enables interrupt output by the BUFRE flag
21	MBUFWEN	0	R/W	BUFWEN Interrupt Mask 0: Disables interrupt output by the BUFWEN flag 1: Enables interrupt output by the BUFWEN flag
20	MBUFREN	0	R/W	BUFREN Interrupt Mask 0: Disables interrupt output by the BUFREN flag 1: Enables interrupt output by the BUFREN flag
19	MCCSRCV	0	R/W	CCSRCV Interrupt Mask 0: Disables interrupt output by the CCSRCV flag 1: Enables interrupt output by the CCSRCV flag
18	—	0	R*	Reserved These bits are always read as 0. The write value should always be 0.
17	MRBSYE	0	R/W	RBSYE Interrupt Mask 0: Disables interrupt output by the RBSYE flag 1: Enables interrupt output by the RBSYE flag
16	MCRSPE	0	R/W	CRSPE Interrupt Mask 0: Disables interrupt output by the CRSPE flag 1: Enables interrupt output by the CRSPE flag
15	MCMDVIO	0	R/W	CMDVIO Interrupt Mask 0: Disables interrupt output by the CMDVIO flag 1: Enables interrupt output by the CMDVIO flag
14	MBUFVIO	0	R/W	BUFVIO Interrupt Mask 0: Disables interrupt output by the BUFVIO flag 1: Enables interrupt output by the BUFVIO flag
13, 12	—	00	R*	Reserved These bits are always read as 0. The write value should always be 0.
11	MWDATERR	0	R/W	WDATERR Interrupt Mask 0: Disables interrupt output by the WDATERR flag 1: Enables interrupt output by the WDATERR flag

Bit	Bit Name	Initial Value	R/W	Description
10	MRDATERR	0	R/W	RDATERR Interrupt Mask 0: Disables interrupt output by the RDATERR flag 1: Enables interrupt output by the RDATERR flag
9	MRIDXERR	0	R/W	RIDXERR Interrupt Mask 0: Disables interrupt output by the RIDXERR flag 1: Enables interrupt output by the RIDXERR flag
8	MRSPERR	0	R/W	RSPERR Interrupt Mask 0: Disables interrupt output by the RSPERR flag 1: Enables interrupt output by the RSPERR flag
7, 6	—	00	R*	Reserved These bits are always read as 0. The write value should always be 0.
5	MCCSTO	0	R/W	CCSTO Interrupt Mask 0: Disables interrupt output by the CCSTO flag 1: Enables interrupt output by the CCSTO flag
4	MCRCSTO	0	R/W	CRCSTO Interrupt Mask 0: Disables interrupt output by the CRCSTO flag 1: Enables interrupt output by the CRCSTO flag
3	MWDATTO	0	R/W	WDATTO Interrupt Mask 0: Disables interrupt output by the WDATTO flag 1: Enables interrupt output by the WDATTO flag
2	MRDATTO	0	R/W	RDATTO Interrupt Mask 0: Disables interrupt output by the RDATTO flag 1: Enables interrupt output by the RDATTO flag
1	MRBSYTO	0	R/W	RBSYTO Interrupt Mask 0: Disables interrupt output by the RBSYTO flag 1: Enables interrupt output by the RBSYTO flag
0	MRSPTO	0	R/W	RSPTO Interrupt Mask 0: Disables interrupt output by the RSPTO flag 1: Enables interrupt output by the RSPTO flag

27.3.14 Status Register 1 (CE_HOST_STS1)

CE_HOST _STS1 indicates the number of blocks that have been transferred, the states of the CMD line and DAT lines, the index of the response that has been received, and whether a command sequence is in progress.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CMD SEQ	CMD SIG	RSPIDX[5:0]						DATSIG[7:0]							
Initial value:	0	—	0	0	0	0	0	0	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RCVBLK[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	CMDSEQ	0	R	Command Sequence in Progress 0: Command sequence is in the initial state 1: Command sequence is being executed
30	CMDSIG	Undefined	R	CMD Line Status Indicates the state on the command line.
29 to 24	RSPIDX [5:0]	H'00	R	Response Index Indicate the index of the response that has been received
23 to 16	DATSIG [7:0]	Undefined	R	DAT[7:0] Status Indicate the states on the DAT lines Note:When transfer error or timeout error occur, MMCDAT[0] may be with 1’b0.
15 to 0	RCVBLK [15:0]	H'0000	R	Number of Transferred Blocks Indicate the number blocks that have been transferred. When the DWEN bit in CE_CMD_SET is 0 Number of blocks read from the card When the DWEN bit in CE_CMD_SET is 1 Number of blocks written to the card

27.3.15 Status Register 2 (CE_HOST _STS2)

CE_HOST _STS2 indicates timeout and error statuses.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CRC STE	CRC 16E	AC12 CRCE	RSP CRC7E	CRC STEBE	RDAT EBE	AC12R EBE	RSP EBE	AC12 IDXE	RSP IDXE	BTACK PATE	BTACK EBE	—	CRCST[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CCS TO	RDAT TO	DATBS YTO	CRCST TO	AC12 BSYTO	RSPBS YTO	AC12 RSPTO	RSP TO	BTACK TO	1STBT DATTO	BTDAT TO	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	CRCSTE	0	R	CRC Status Error Set to 1 when an error is found in the CRC status value.
30	CRC16E	0	R	Read Data CRC16 Error Set to 1 when an error is found in CRC16 in the read data.
29	AC12CRCE	0	R	Automatic CMD12 Response CRC7 Error Set to 1 when an error is found in CRC7 of the response to the automatically-issued CMD12.
28	RSPCRC7E	0	R	Command Response CRC7 Error Set to 1 when an error is found in CRC7 of the response.
27	CRCSTEBE	0	R	CRC Status End Bit Error Set to 1 when an error is found in the end bits in CRC status.
26	RDATEBE	0	R	Read Data End Bit Error Set to 1 when an error is found in the end bits in the read data.
25	AC12REBE	0	R	Automatic CMD12 Response End Bit Error Set to 1 when an error is found in the end bits of the response to the automatically-issued CMD12.

Bit	Bit Name	Initial Value	R/W	Description
24	RSPEBE	0	R	Command Response End Bit Error Set to 1 when an error is found in the end bits of the response.
23	AC12IDX	0	R	Automatic CMD12 Response Index Error Set to 1 when an error is found in the index of the response to the automatically-issued CMD12.
22	RSPIDXE	0	R	Command Response Index Error Set to 1 when an error is found in the index of the response.
21	BTACKPATE	0	R	Boot Acknowledge Pattern Error Set to 1 when an error is found in the Pattern in Boot Acknowledge.
20	BTACKEBE	0	R	Boot Acknowledge End Bit Error Set to 1 when an error is found in the end bit in Boot Acknowledge.
19	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
18 to 16	CRCST [2:0]	000	R	CRC Status Indicate the value of the CRC status that has been received.
15	CCSTO	0	R	CCS Timeout Set to 1 if CCS is not received within the period set by the SCCSTO bits in CE_CLK_CTRL.
14	RDATTO	0	R	Read Data Timeout Set to 1 if read data is not received within the period set by the SRWDTO bits in CE_CLK_CTRL.
13	DATBSYTO	0	R	Data Busy Timeout Set to 1 if data busy continues exceeding the period set by the SRWDTO bits in CE_CLK_CTRL.
12	CRCSTTO	0	R	CRC Status Timeout Set to 1 if CRC status could not be received.
11	AC12BSYTO	0	R	Automatic CMD12 Response Busy Timeout Set to 1 if the response busy of the automatically-issued CMD12 continues exceeding the period set by the SRBSYTO bits in CE_CLK_CTRL.

Bit	Bit Name	Initial Value	R/W	Description
10	RSPBSYTO	0	R	Response Busy Timeout Set to 1 if the response busy continues exceeding the period set by the SRBSYTO bits in CE_CLK_CTRL.
9	AC12RSPTO	0	R	Automatic CMD12 Response Timeout Set to 1 if the response to the automatically-issued CMD12 is not received within the period set by the SRSPTO bits in CE_CLK_CTRL.
8	RSPTO	0	R	Response Timeout Set to 1 if the response is not received within the period set by the SRSPTO bits in CE_CLK_CTRL.
7	BTACKTO	0	R	Boot Acknowledge Timeout Set to 1 if the Boot Acknowledge is not received within the period set by the SBTACKTO bits in CE_BOOT when Boot Operation.
6	1STBTDATT	0	R	1st Boot data Timeout Set to 1 if 1st read data is not received within the period set by the S1STBTDATO bits in CE_BOOT when Boot Operation.
5	BTDATO	0	R	Boot Interval Timeout Set to 1 if read data is not received within the period set by the SBTDATTO bits in CE_BOOT after previous read data was received when Boot Operation.
4 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

27.3.16 Version Register (CE_VERSION)

CE_VERSION indicates the version number and controls software reset of this module.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SW RST	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VERSION[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	SWRST	0	R/W	Software Reset 0: Software reset cleared (normal operation) 1: Executes software reset
30 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 0	VERSION [15:0]	H’0002	R	Version Information Indicates the version number of this module.

27.4 Interrupt Requests

This module generates these types of interrupt requests: normal operation and error/timeout. The interrupt flags are accommodated in the CE_INT. When a bit in the flag register is set to 1 and also the corresponding bit in the interrupt mask register is set to 1 (enabled), an interrupt request is generated.

Table 27.4 Specification of the Interrupt Requests

Flag Register	Bit	Mask Register	Bit	Interrupt Request
CE_INT	CCSDE	CE_INT_MASK	MCCSDE	Normal operation interrupt
	CMD12DRE		MCMD12DRE	
	CMD12RBE		MCMD12RBE	
	CMD12CRE		MCMD12CRE	
	DTRANE		MDTRANE	
	BUFRE		MBUFRE	
	BUFWEN		MBUFWEN	
	BUFREN		MBUFREN	
	CCSRCV		MCCSRCV	
	RBSYE		MRBSYE	
	CRSPE		MCRSPE	
	CMDVIO		MCMDVIO	Error/timeout interrupt
	BUFVIO		MBUFVIO	
	WDATERR		MWDATERR	
	RDATERR		MRDATERR	
	RIDXERR		MRIDXERR	
	RSPERR		MRSPERR	
	CCSTO		MCCSTO	
	CRCSTO		MCRCSTO	
	WDATTO		MWDATTO	
	RDATTO		MRDATTO	
	RBSYTO		MRBSYTO	
	RSPTO		MRSPTO	

27.5 DMA Specifications

27.5.1 DMA for Buffer Writing

The DMA transfer request is asserted for buffer writing when the buffer has become empty while the DMAWEN bit in CE_BUF_ACC is set to 1.

The DMA transfer request stays asserted for the amount of data specified by BLKSIZ (the block size set in CE_BLOCK_SET) × BLKCNT (the number of blocks for transfer set in CE_BLOCK_SET), and negated after the last block has been transferred. Note that the BUFWEN bit in CE_INT will not be asserted during DMA transfer.

If an error has occurred during DMA transfer or DMA transfer is forcibly terminated, the command sequence is stopped automatically, which causes the DMA transfer request to be negated.

27.5.2 DMA for Buffer Reading

The DMA transfer request is asserted for buffer reading when the buffer stores data of the block size specified in CE_BLOCK_SET while the DMAREN bit in CE_BUF_ACC is set to 1.

The DMA transfer request stays asserted for the amount of data specified by BLKSIZ (the block size set in CE_BLOCK_SET) × BLKCNT (the number of blocks for transfer set in CE_BLOCK_SET), and negated after the last block has been transferred. Note that the BUFREN bit in CE_INT will not be asserted during DMA transfer.

If an error has occurred during DMA transfer or DMA transfer is forcibly terminated, the command sequence is stopped automatically, which causes the DMA transfer request to be negated.

27.6 Operation

This section describes the formats of the command and response, timing of automatic CMD12 issuance, buffer structures, buffer access select function, and the operation when an error has occurred.

27.6.1 Command/Response Formats

Figure 27.2 shows the format of the command to be transferred. The command index that is set in CMD[5:0] of CE_CMD_SET and the argument set in ARG[31:0] of CE_ARG are reflected in the command.

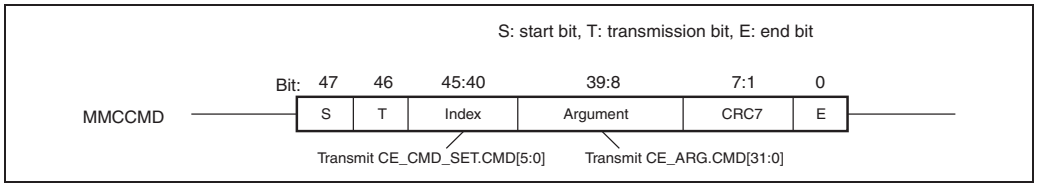


Figure 27.2 Command Format

Figures 27.3 and 27.4 show the formats when a 6-byte response and 17-byte response are received, respectively. The response index is stored in RSPIDX[5:0] of CE_HOST_STS1, and the status value of the response is stored to CE_RESP0 or CE_RESP3 to CE_RESP0.

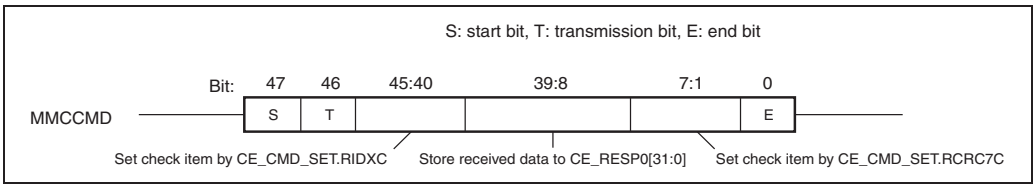


Figure 27.3 Format of 6-Byte Response

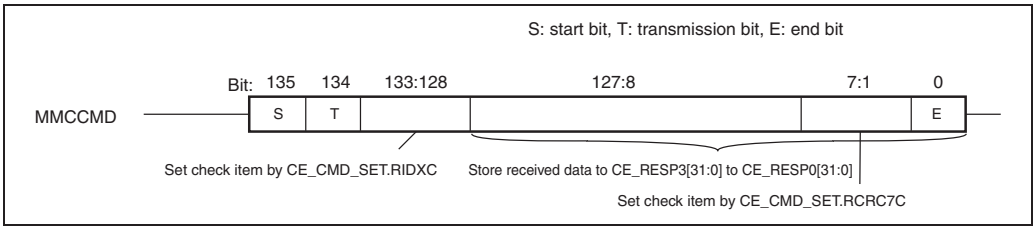


Figure 27.4 Format of 17-Byte Response (R2)

27.6.2 Data Formats

Figures 27.5 to 27.7 show the formats of data. In transmission, the value written to the buffer is reflected on the data lines, and in reception, the value of the received data is stored in the buffer.

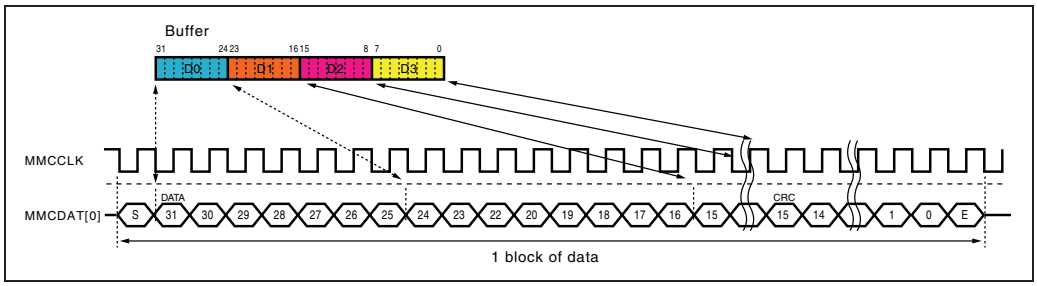


Figure 27.5 Data Format (1-Bit Mode)

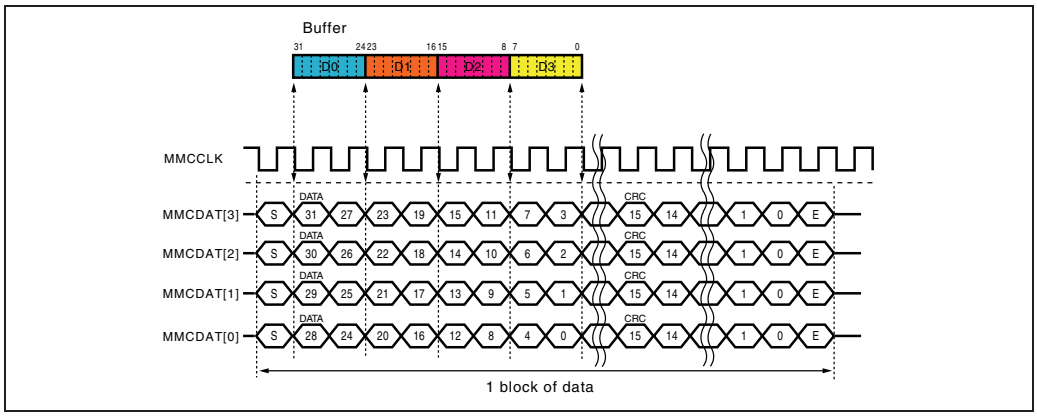


Figure 27.6 Data Format (4-Bit Mode)

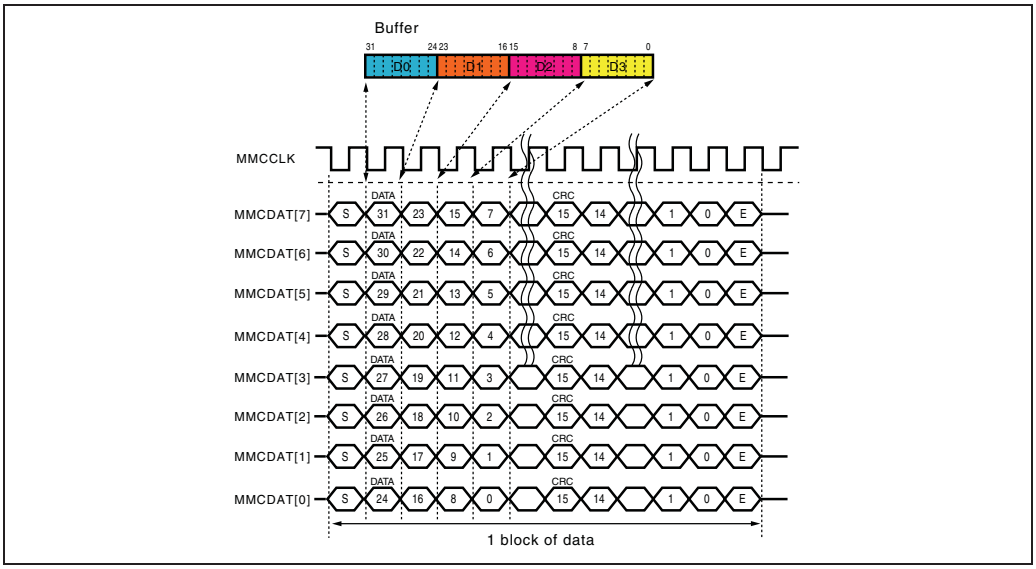


Figure 27.7 Data Format (8-Bit Mode)

27.6.3 Buffer Structure and Buffer Access

This module has two 512-byte RAM units which are used for double buffering. If the transfer block size is set to 4 × n + 1 or 4 × n + 3, access should be made for 4 × n + 2 bytes or 4 × (n + 1) bytes in 16-bit access, and for 4 × (n + 1) bytes in 32-bit access. (n = 0, 1, 2, …, 127)

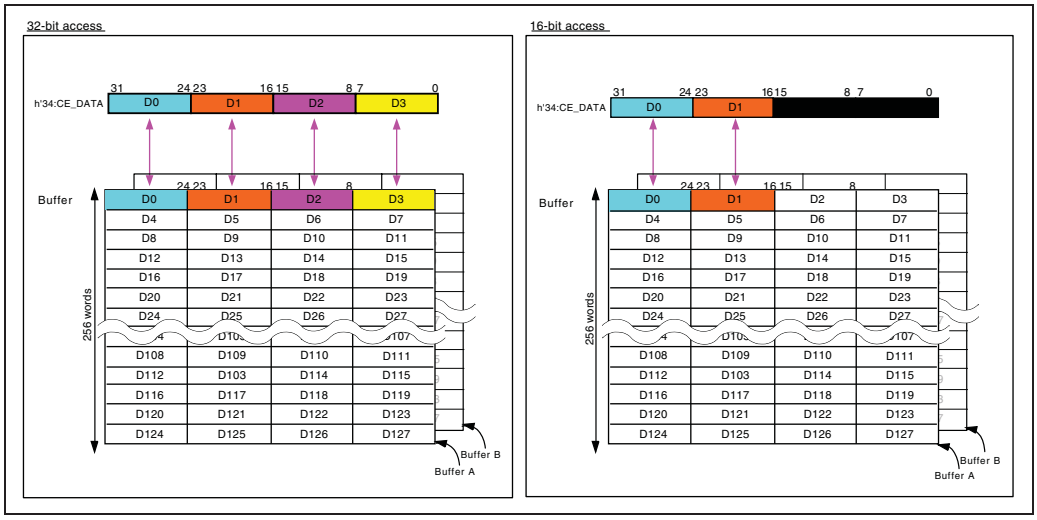


Figure 27.8 Double Buffer Structure

This module has the buffer access select function that allows byte-wise swapping of data when the buffer is accessed by writing to or reading from CE_DATA. This function is enabled by the setting of CE_BUFF_ACC. Figure 27.8 shows the specification of 32-bit and 16-bit accesses.

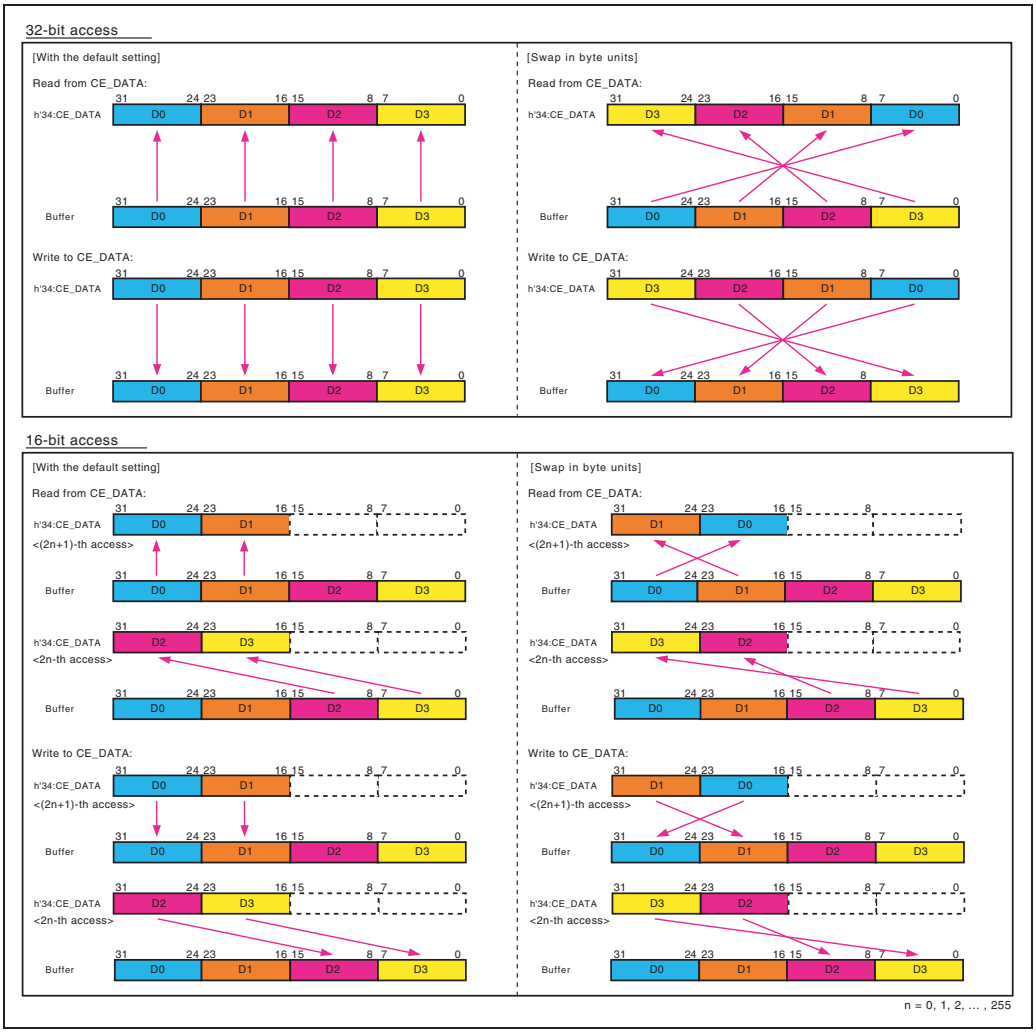


Figure 27.9 Specification of Byte-Swapping in 32/16-Bit Accesses

27.6.4 Automatic CMD12 Issuance

This module has the function that automatically issues CMD12 when multi-block transfer is performed with the CMD12EN in CE_CMD_SET set to 1. Timing of automatic CMD12 issuance is described for the case of multi-block reading and multi-block writing.

Figure 27.10 shows the timing of automatic CMD12 issuance in multi-block read. CMD12 is issued such that the end bit of the command is sent two bits before the end bit of the data during reception of the last block.

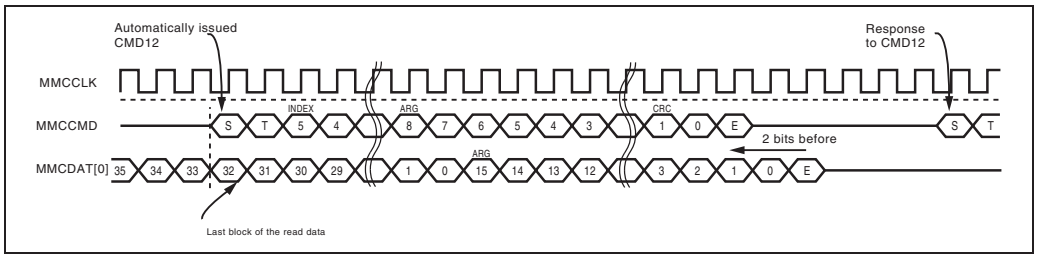


Figure 27.10 Timing of Automatically-Issued CMD12 in Multi-Block Read (1-Bit Mode)

Figure 27.11 shows the timing of automatic CMD12 issuance in multi-block write. CMD12 is issued after the data busy after transmission of the last block has ended.

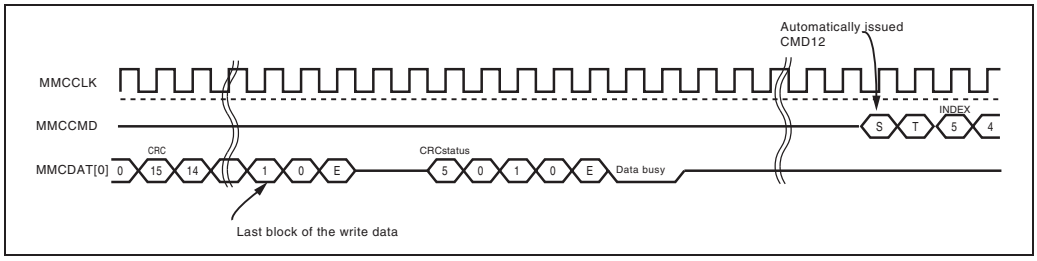


Figure 27.11 Timing of Automatically-Issued CMD12 in Multi-Block Write (1-Bit Mode)

27.6.5 MMC Clock frequency for Boot Operation

Figure 27.12 shows the operation which changes MMC Clock frequency for Boot Operation. After MMCCMD is changed from 1 into 0 and 74 cycles of MMC Clock, it changes into the MMC clock frequency corresponding to CE_BOOT.BTCLKDIV. After MMCCMD is changed from 0 into 1 and 48 cycles of MMC Clock, it changes into the MMC clock frequency corresponding to CE_CLK_CTRL.CLKDIV.

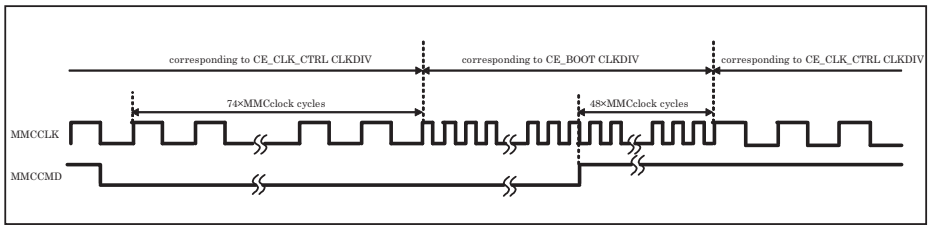


Figure 27.12 MMC Clock frequency for Boot Operation

27.6.6 Operation in the Case of Error/Timeout

This module might not stop when the error has occurred. Execute software reset after terminate the sequence forcibly if the command sequence is still in progress (Confirm it with CMDSEQ of CE_HOST_STS1) when the error has occurred. The data for transmission or received data that had been stored in the buffers at the time of error occurrence are not guaranteed.

This module is not stopped when a timeout has occurred. Issue the next command terminate the sequence forcibly when the next command is issued after a timeout has occurred.

27.6.7 For processing when terminate forcibly

The command sequence might not end in the MMC/CE-ATA host interface according to set timing of the BREAK bit of the CE_CMD_CTRL register when the command sequence terminate forcibly.

Therefore, process it by either of the following two methods when the command sequence terminate forcibly.

(1) When the command sequence terminate forcibly, execute software reset without using the BREAK bit of the CE_CMD_CTRL register.

(2) When the command sequence terminate forcibly in the following after the command of the R1b response is issued, execute software reset without using the BREAK bit of the CE_CMD_CTRL register.

- Busy timeout for response

- Abnormality of response value

27.7 Examples of Setting

This section shows the procedures for executing typical command sequences.

27.7.1 Legends

Figure 27.13 shows the legends for the symbols used in the figures in the following subsections.

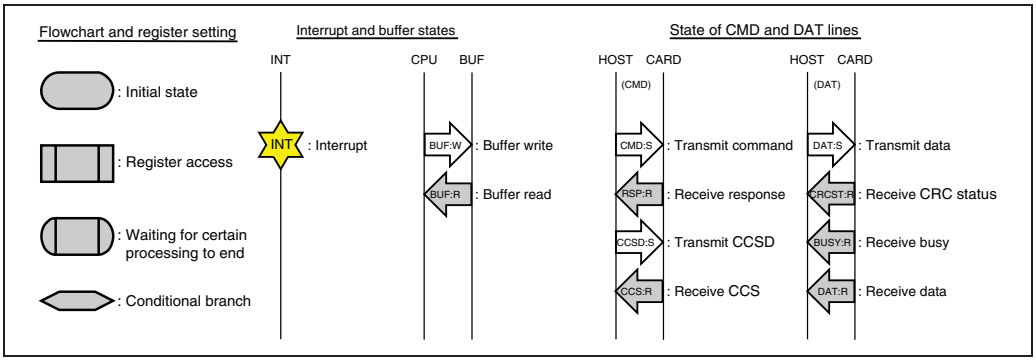


Figure 27.13 Legends for the Symbols Used in the Figures

27.7.2 Command Transmission

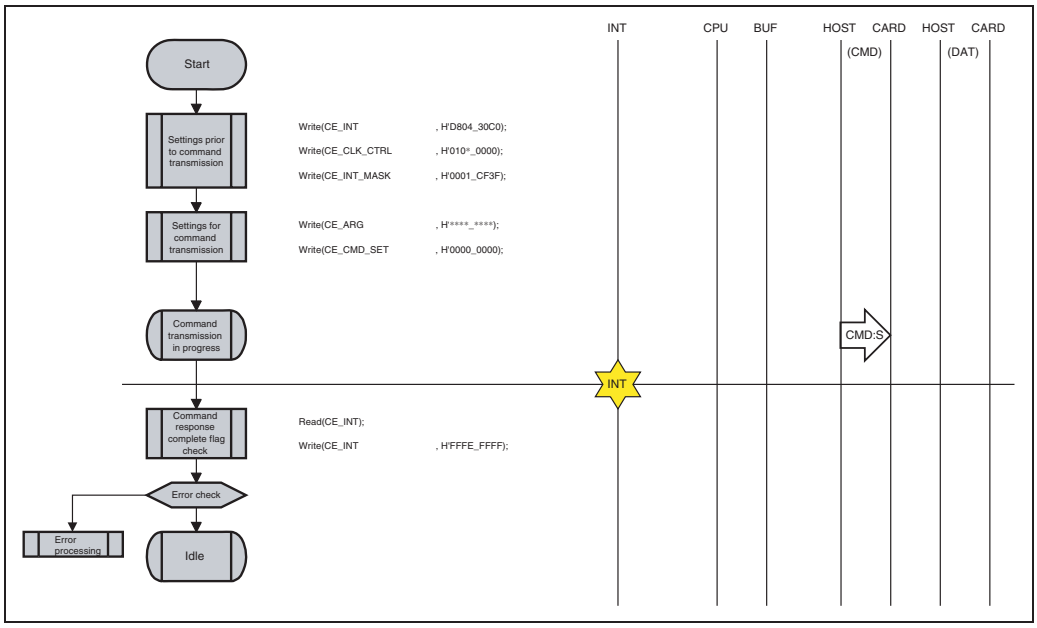


Figure 27.14 Command Transmission (CMD0)

27.7.3 Command Transmission → Response Reception

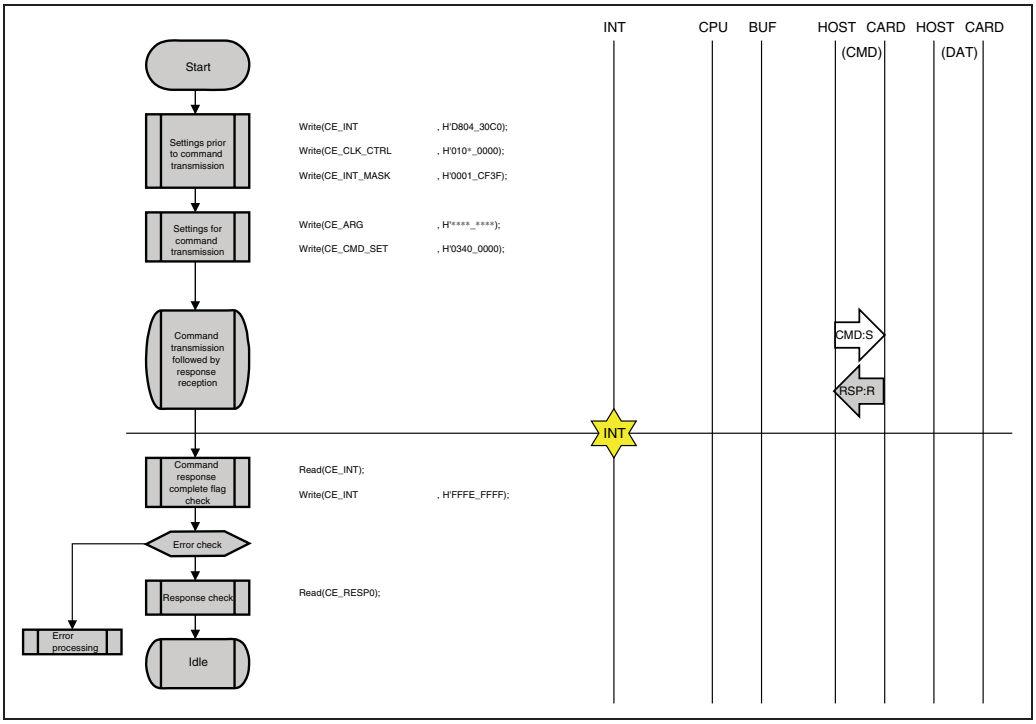


Figure 27.15 Command Transmission → Response Reception (CMD13)

27.7.4 Command Transmission → Response Reception (with Response Busy)

- When busy time is less than setting of CE_CLK_CTRL.SRBSYTO

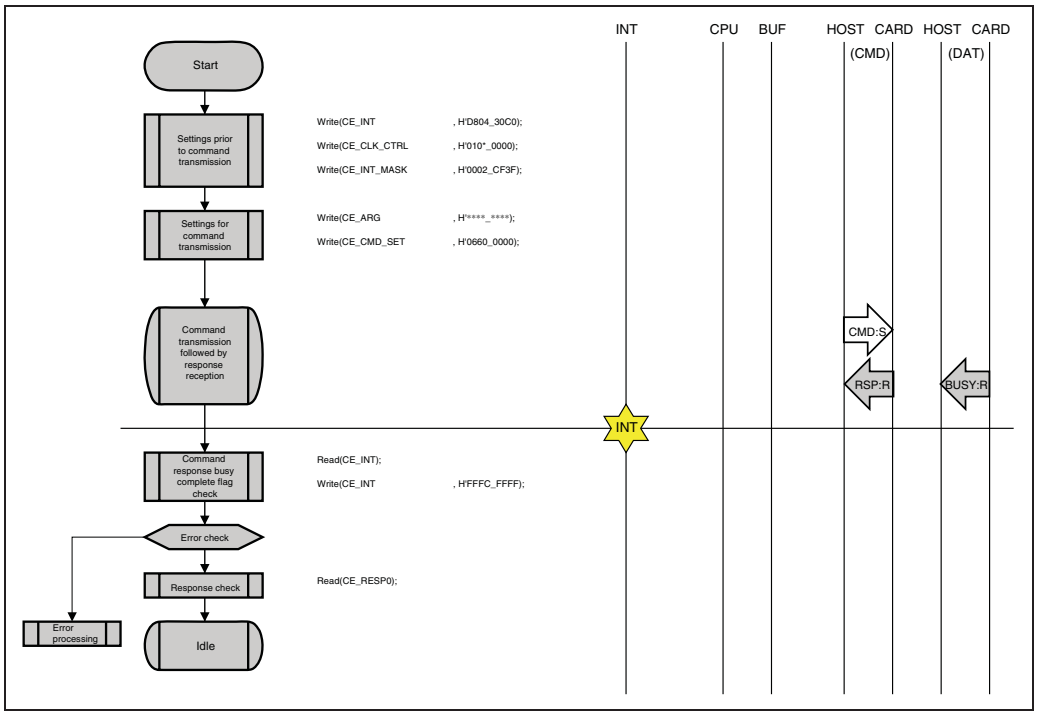


Figure 27.16 Command Transmission → Response Reception (with Response Busy) (CMD6)

- When busy time might become more than the setting of CE_CLK_CTRL.SRBSYTO

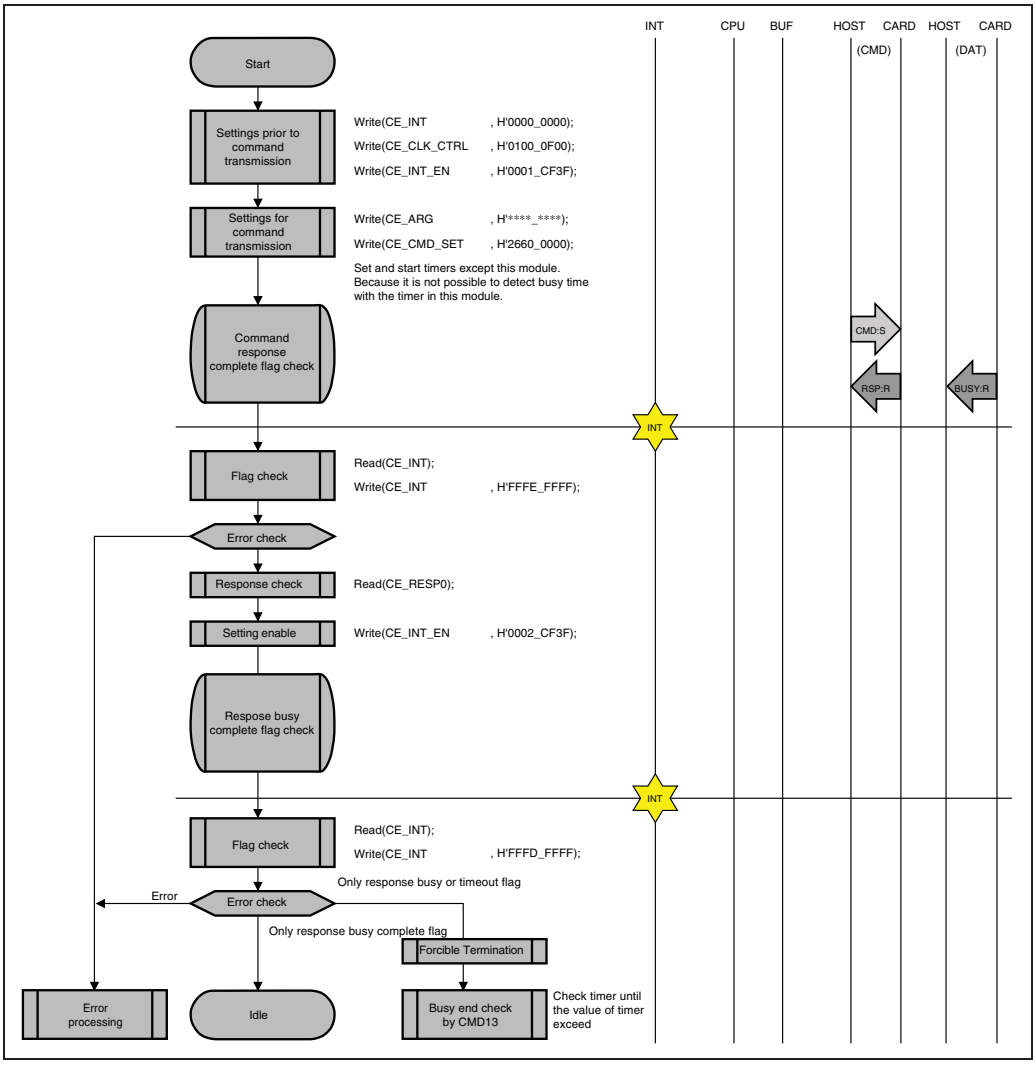


Figure 27.17 Command Transmission → Response Reception (with Response Busy) (CMD38)

27.7.5 Single-Block Read

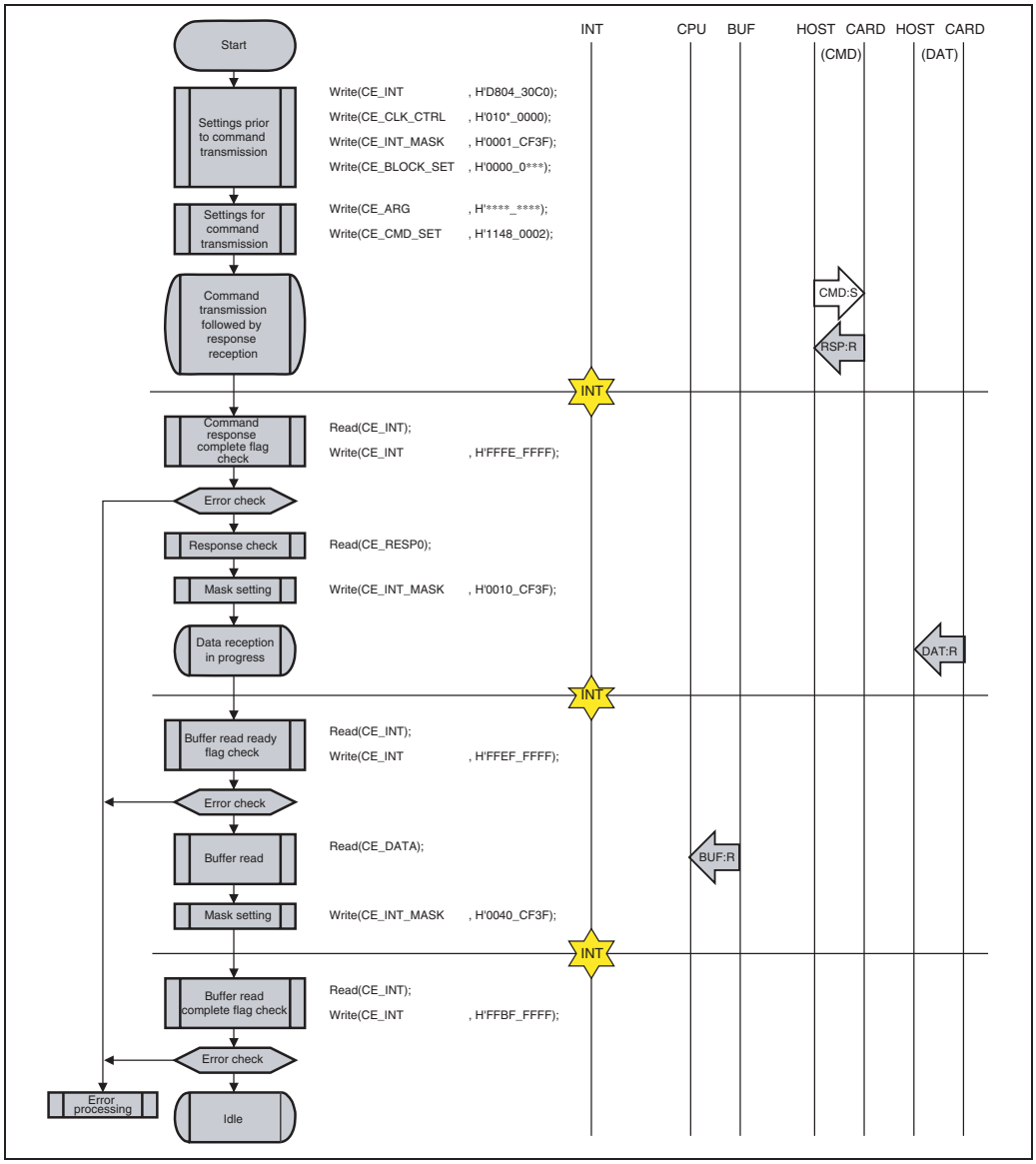


Figure 27.18 Single-Block Read (CMD17)

27.7.6 Multi-Block Read

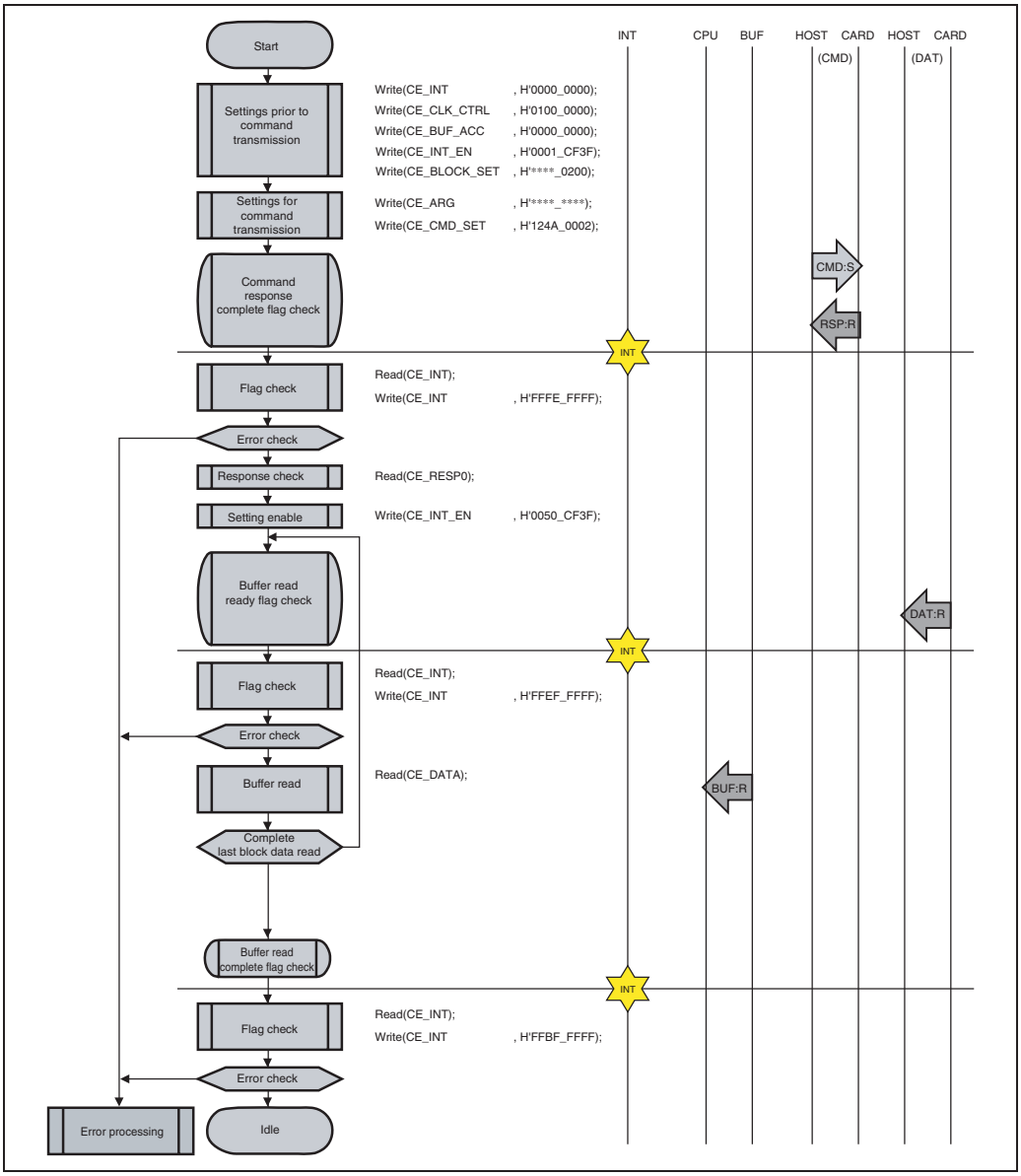


Figure 27.19 Multi-Block Read (CMD18 Pre defined)

27.7.7 Multi-Block Read (with Automatic CMD12 Issuance)

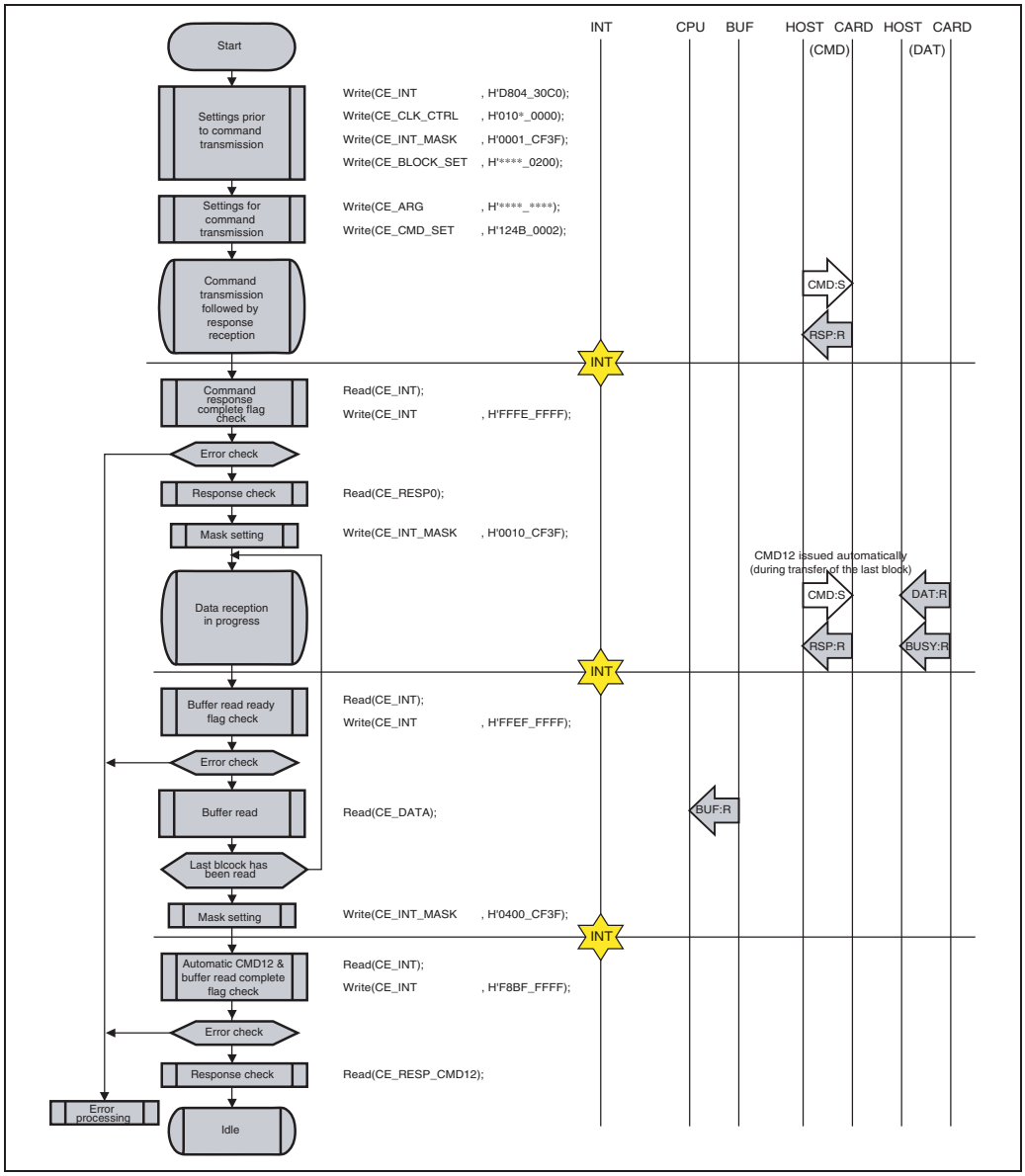


Figure 27.20 Multi-Block Read (with Automatic CMD12 Issuance) (CMD18 Open ended)

27.7.8 Single-Block Write

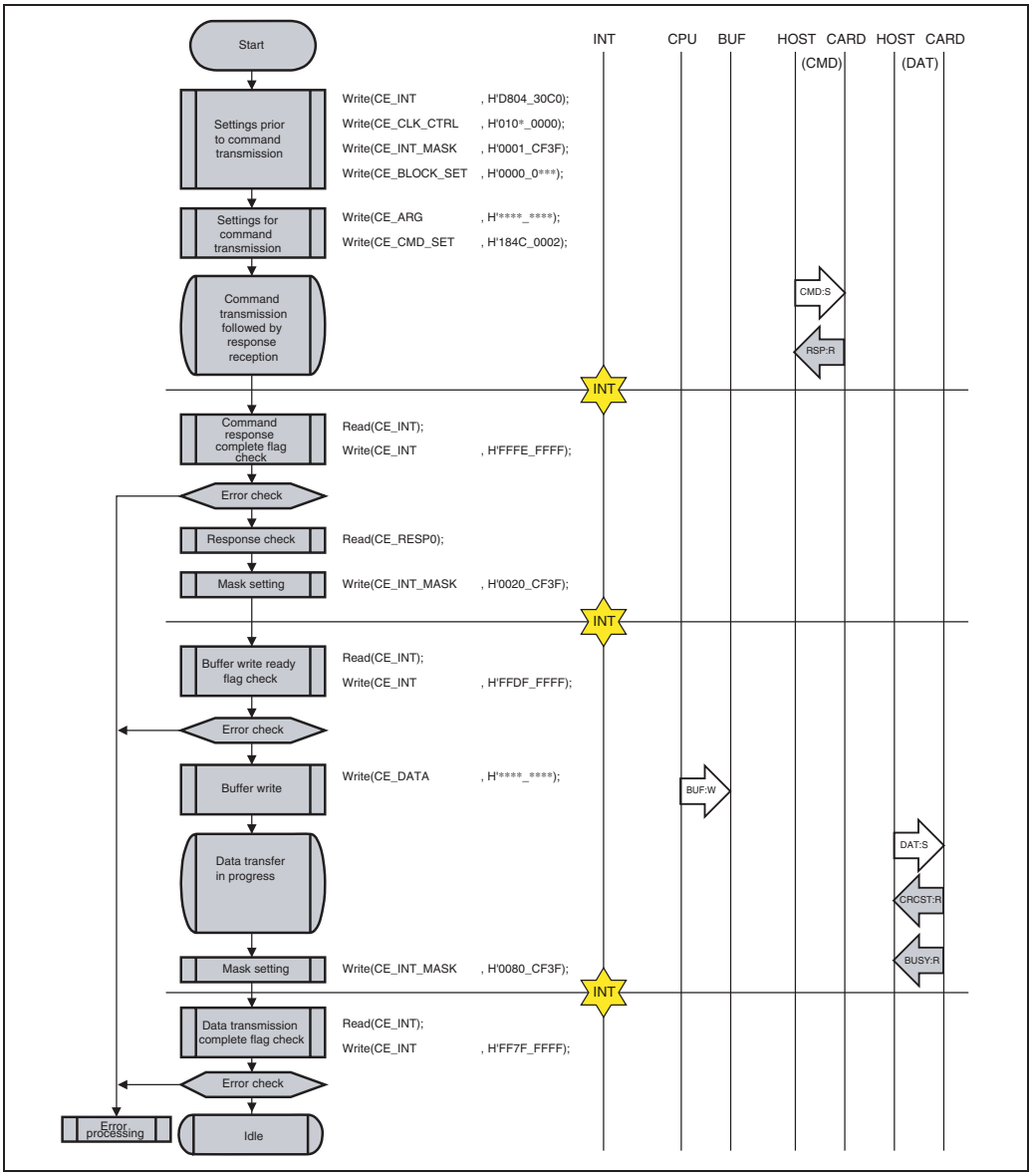


Figure 27.21 Single-Block Write (CMD24)

27.7.9 Multi-Block Write

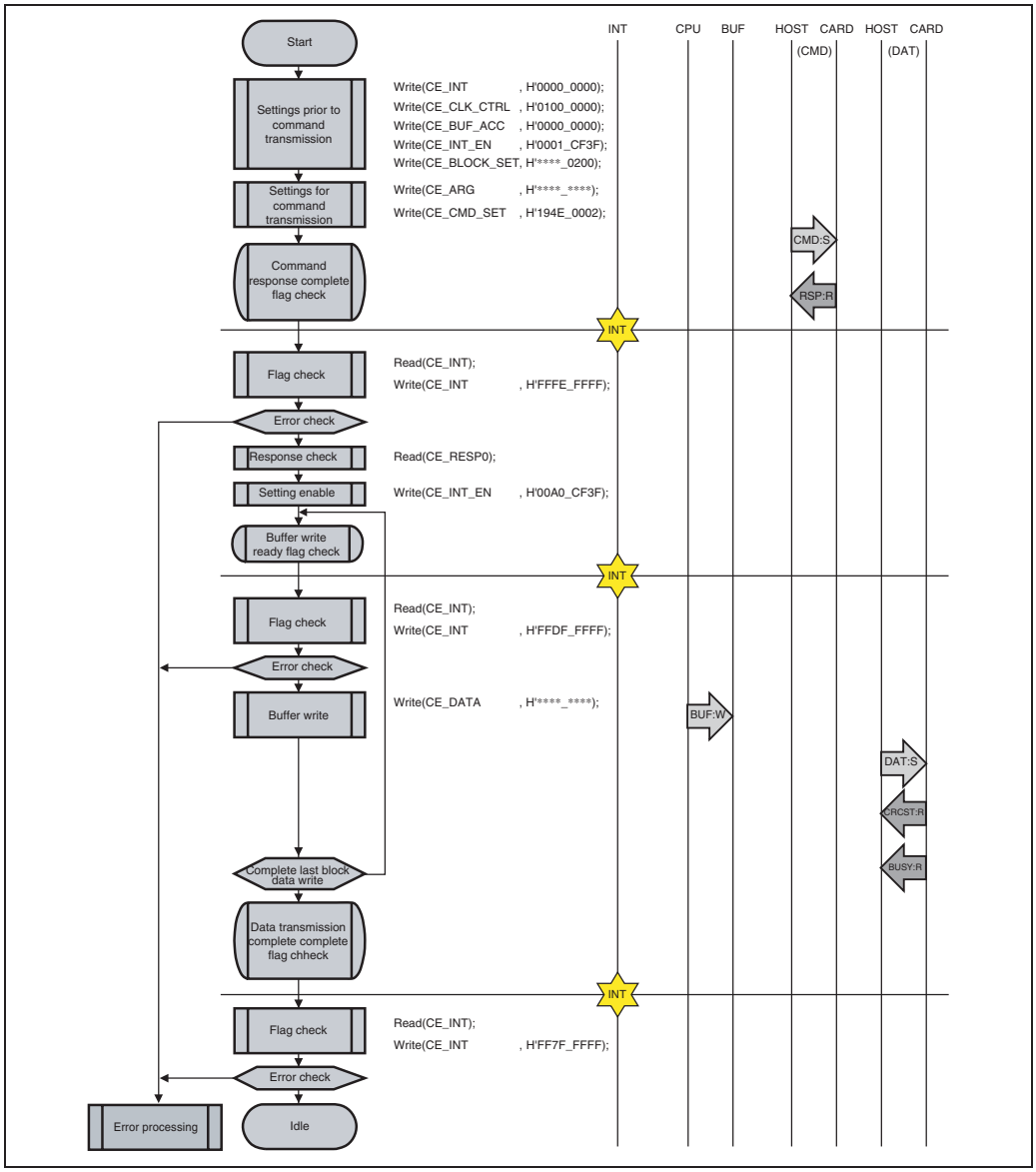


Figure 27.22 Multi-Block Write (CMD25 Pre defined)

27.7.10 Multi-Block Write (with Automatic CMD12 Issuance)

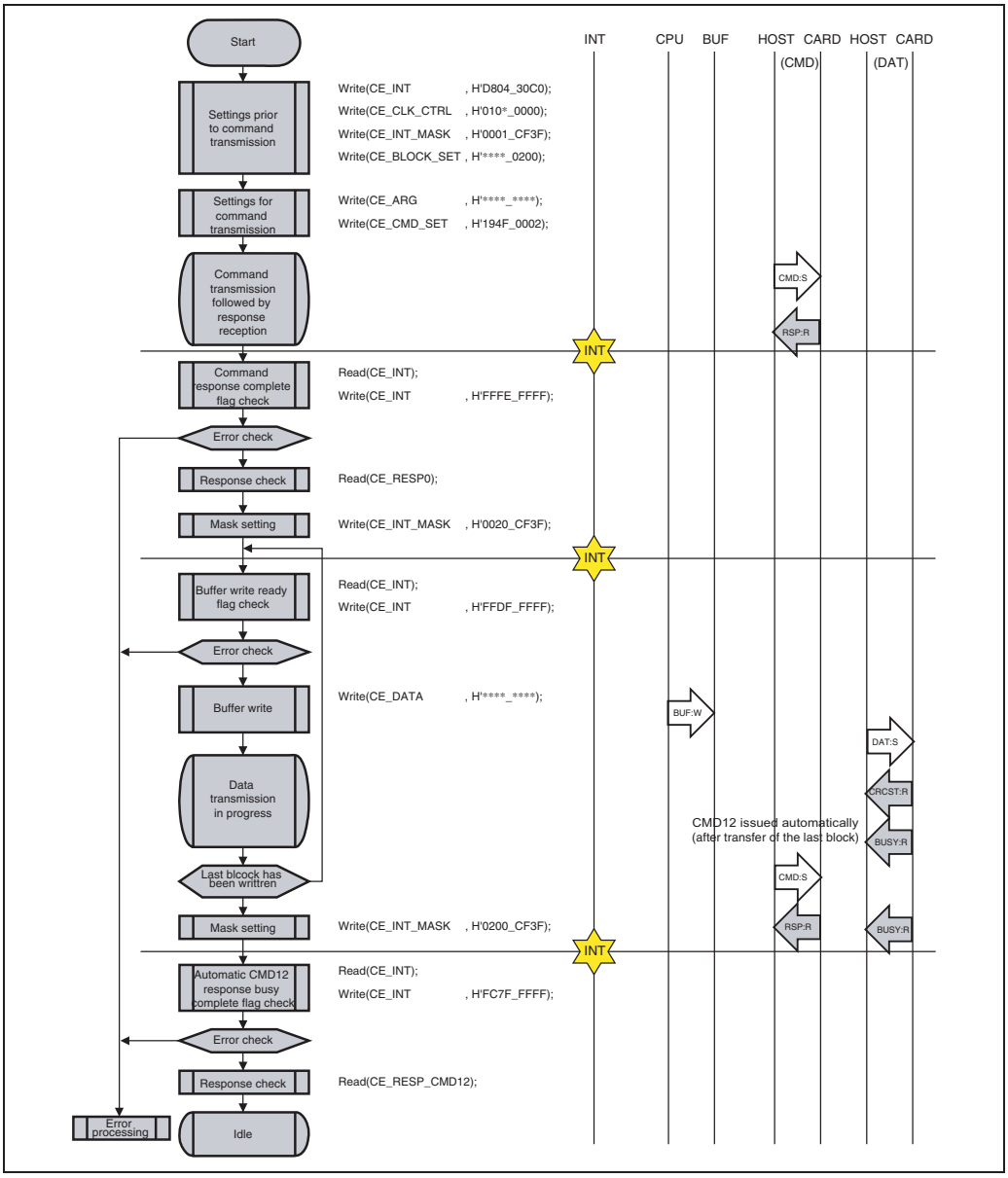


Figure 27.23 Multi-Block Write (with Automatic CMD12 Issuance) (CMD25 Open ended)

27.7.11 Boot Operation

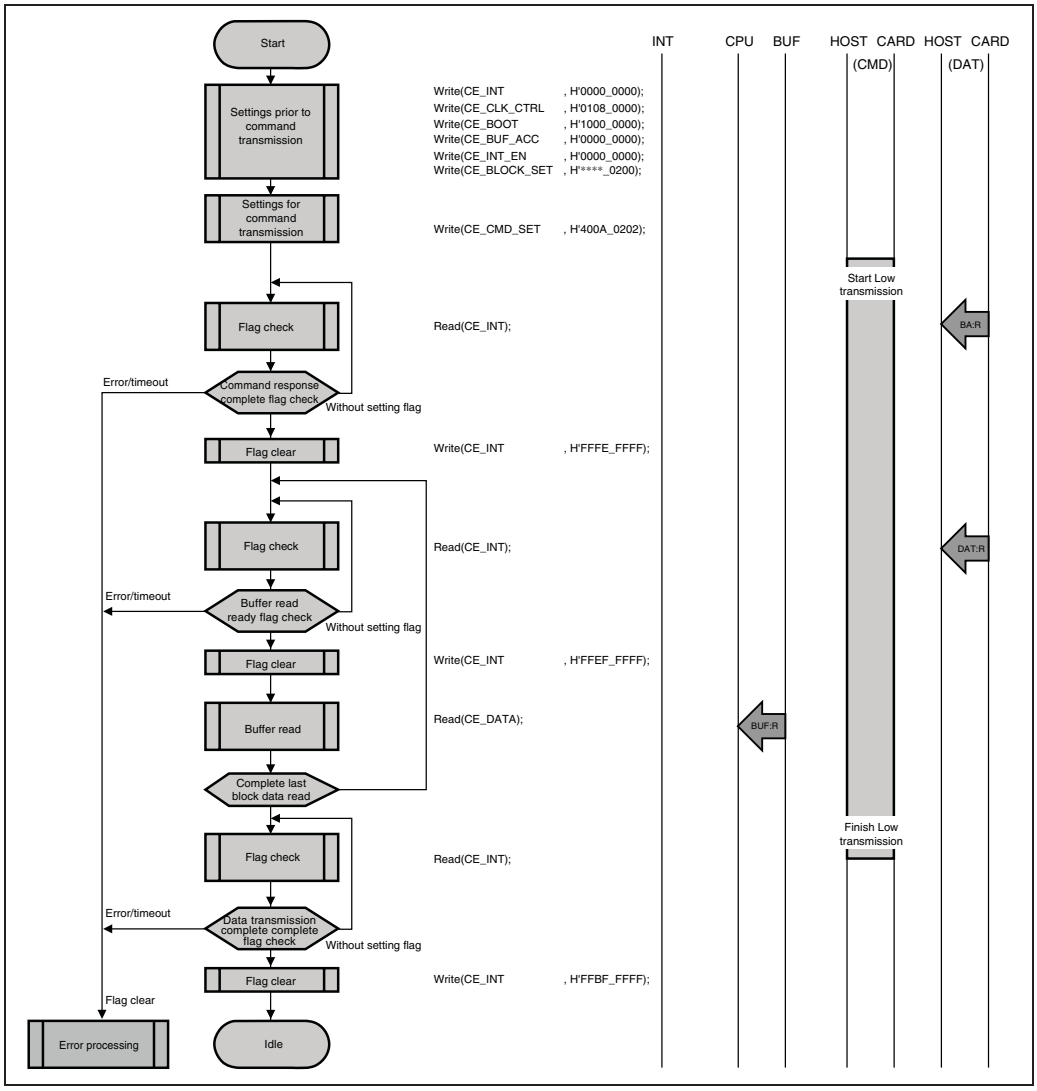


Figure 27.24 Boot Operation (with Boot Acknowledge)

27.7.12 Forcible Termination

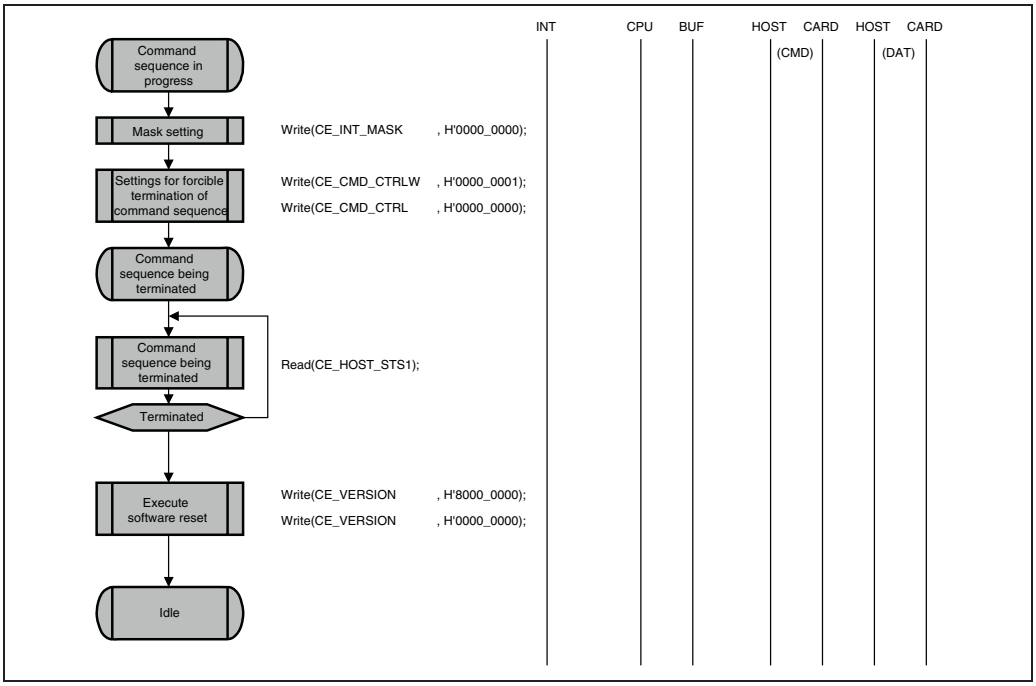


Figure 27.25 Forcible Termination

27.7.13 Command Transmission → Response Reception (with Response Busy and CCS)

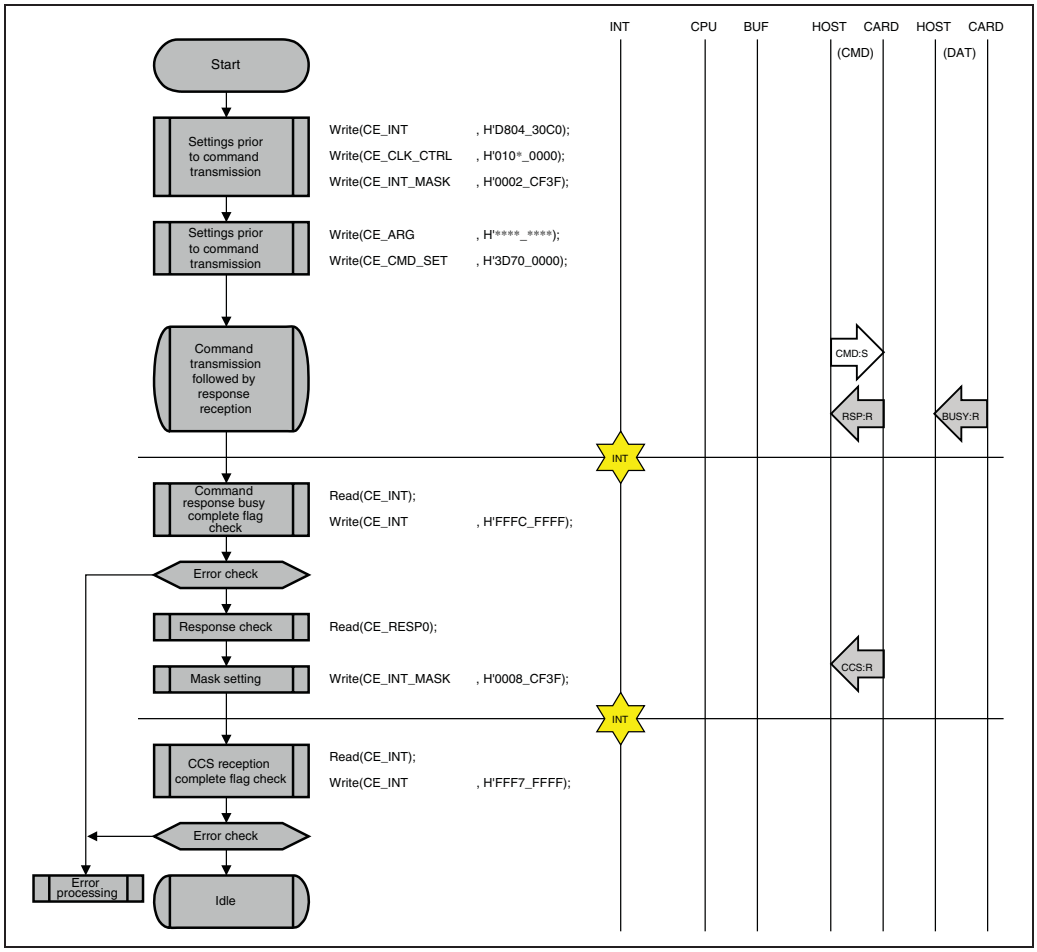


Figure 27.26 Command Transmission → Response Reception (with Response Busy and CCS) (CMD61)

27.7.14 Multi-Block Read (with CCS)

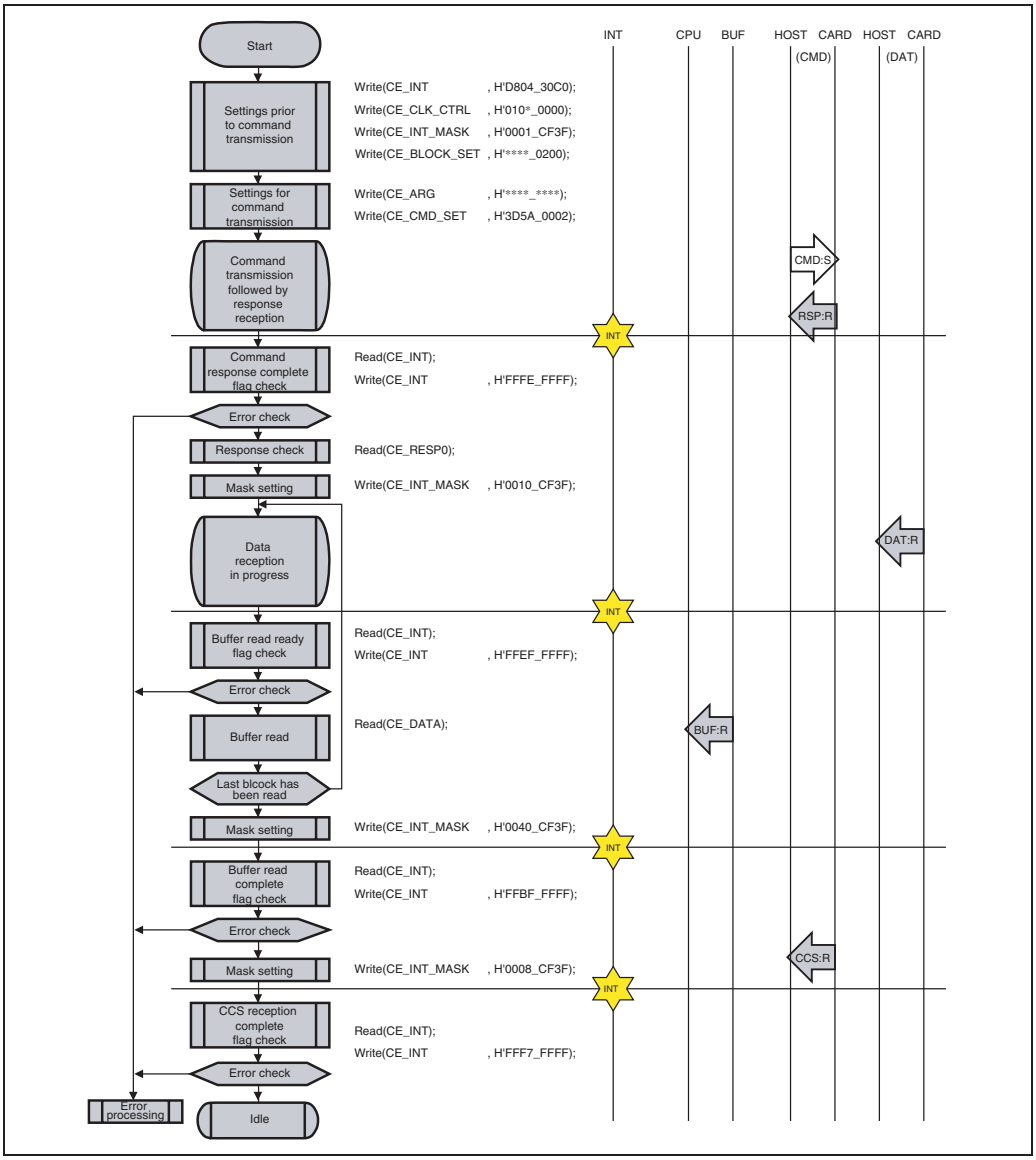


Figure 27.27 Multi-Block Read (with CCS) (CMD61)

27.7.15 Multi-Block Write (with Response Busy and CCS)

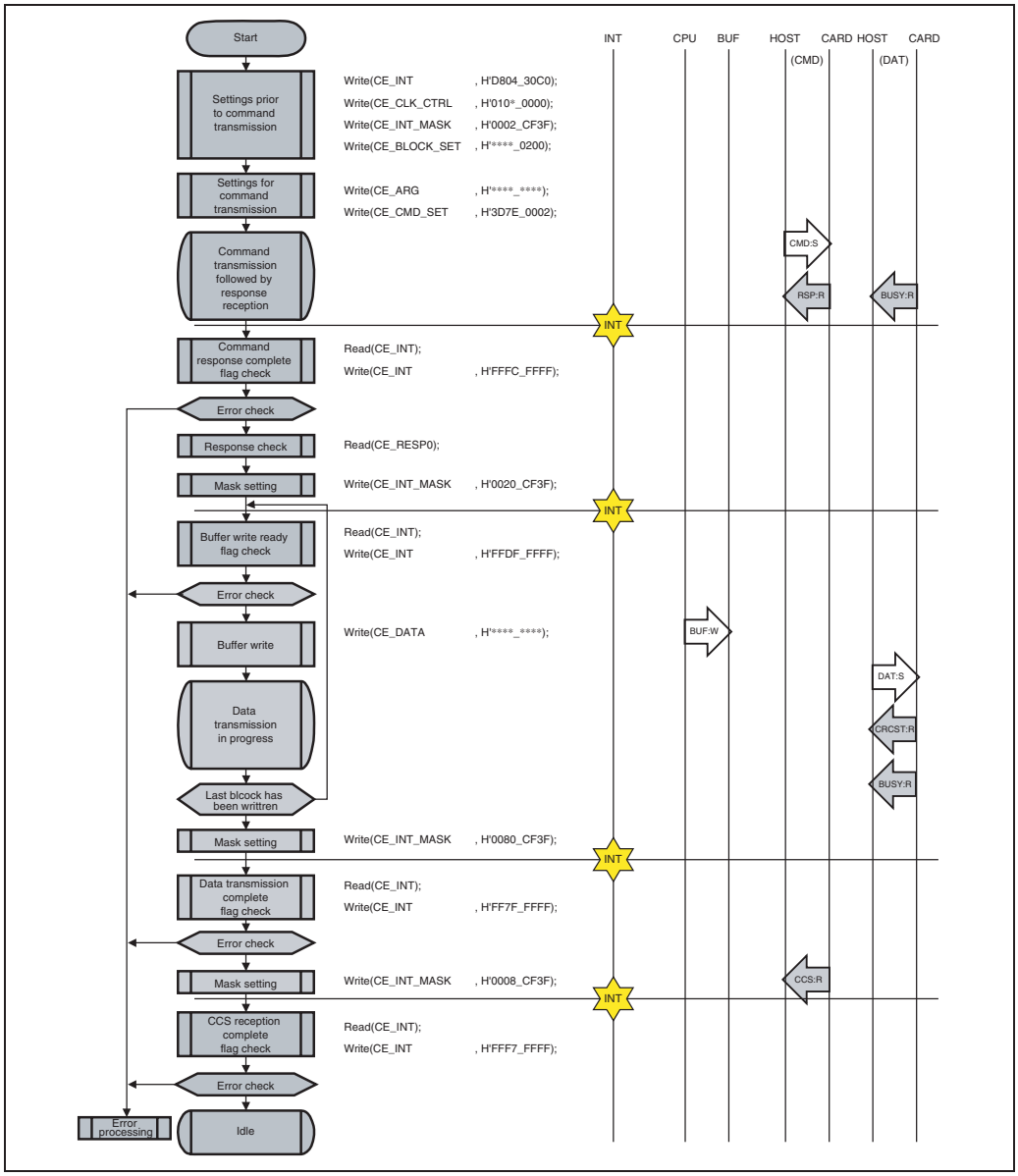


Figure 27.28 Multi-Block Write (with Response Busy and CCS) (CMD61)

27.7.16 Forcible Termination → Transmission of CCSD

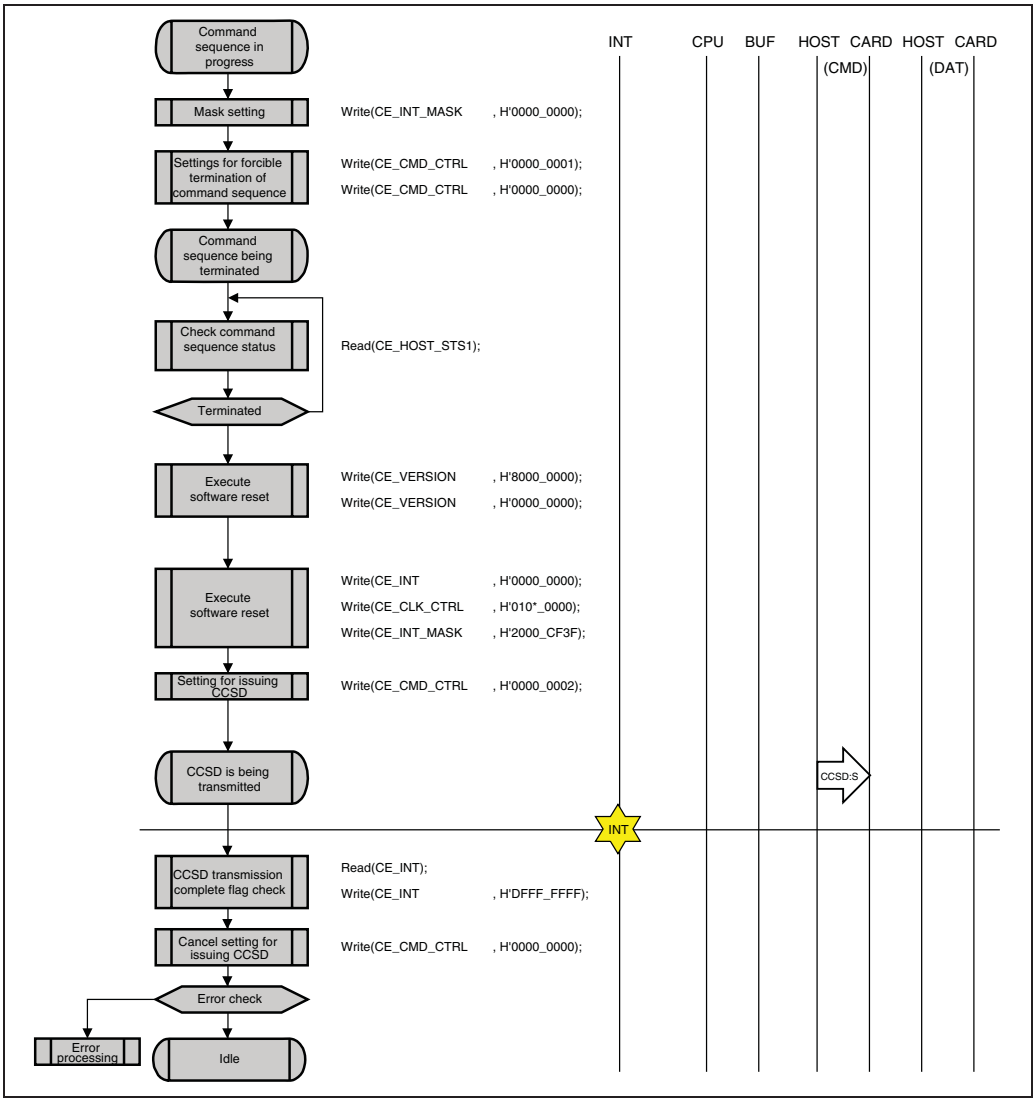


Figure 27.29 Forcible Termination → Transmission of CCSD

27.7.17 Setting Values of CE_CMD_SET

Table 27.5 to 27.7 lists the setting values required to issue commands.

Table 27.5 Setting Values of CE_CMD_SET 1 (sequence without Boot Operation)

Command	Response	CE_CMD_SET																					note
		Reserved	BOOT	CMD[5:0]	RTYP[1:0]	RBSY	CCSEN	WDAT	DWEN	CMLTE	CMD12EN	RIDXC[1:0]	RCRC7C[1:0]	Reserved	CRC16C	BOOTACK	CRCSTE	TBIT	OPDM	CCSH	Reserved[2:0]	DATW[1:0]	
CMD0	—	0	0	000000	00	0	0	0	0	0	0	00	00	0	0	0	0	0	0	0	000	00	
CMD1	R3	0	0	000001	01	0	0	0	0	0	0	01	01	0	0	0	0	0	0	0	000	00	
CMD2	R2	0	0	000010	10	0	0	0	0	0	0	01	10	0	0	0	0	0	0	0	000	00	
CMD3	R1	0	0	000011	01	0	0	0	0	0	0	00	00	0	0	0	0	0	0	0	000	00	
CMD4	—	0	0	000100	00	0	0	0	0	0	0	00	00	0	0	0	0	0	0	0	000	00	
CMD5	R1b	0	0	000101	01	1	0	0	0	0	0	00	00	0	0	0	0	0	0	0	000	00	
CMD6	R1b	0	0	000110	01	1	0	0	0	0	0	00	00	0	0	0	0	0	0	0	000	00	
CMD7	R1	0	0	000111	01	0	0	0	0	0	0	00	00	0	0	0	0	0	0	0	000	00	
	R1b	0	0	000111	01	1	0	0	0	0	0	00	00	0	0	0	0	0	0	0	000	00	
CMD8	R1	0	0	001000	01	0	0	1	0	0	0	00	00	0	0	0	0	0	0	0	000	**	
CMD9	R2	0	0	001001	10	0	0	0	0	0	0	01	10	0	0	0	0	0	0	0	000	00	
CMD10	R2	0	0	001010	10	0	0	0	0	0	0	01	10	0	0	0	0	0	0	0	000	00	
CMD12	R1	0	0	001100	01	0	0	0	0	0	0	00	00	0	0	0	0	0	0	0	000	00	
	R1b	0	0	001100	01	1	0	0	0	0	0	00	00	0	0	0	0	0	0	0	000	00	
CMD13	R1	0	0	001101	01	0	0	0	0	0	0	00	00	0	0	0	0	0	0	0	000	00	
CMD14	R1	0	0	001110	01	0	0	1	0	0	0	00	00	0	1	0	0	0	0	0	000	**	
CMD15	-	0	0	001111	00	0	0	0	0	0	0	00	00	0	0	0	0	0	0	0	000	00	
CMD16	R1	0	0	010000	01	0	0	0	0	0	0	00	00	0	0	0	0	0	0	0	000	00	
CMD17	R1	0	0	010001	01	0	0	1	0	0	0	00	00	0	0	0	0	0	0	0	000	**	
CMD18	R1	0	0	010010	01	0	0	1	0	1	0	00	00	0	0	0	0	0	0	0	000	**	Pre-defined
	R1	0	0	010010	01	0	0	1	0	1	1	00	00	0	0	0	0	0	0	0	000	**	Open-ended
CMD19	R1	0	0	010011	01	0	0	1	1	0	0	00	00	0	0	0	1	0	0	0	000	**	
CMD23	R1	0	0	010111	01	0	0	0	0	0	0	00	00	0	0	0	0	0	0	0	000	00	
CMD24	R1	0	0	011000	01	0	0	1	1	0	0	00	00	0	0	0	0	0	0	0	000	**	
CMD25	R1	0	0	011001	01	0	0	1	1	1	0	00	00	0	0	0	0	0	0	0	000	**	Pre-defined
	R1	0	0	011001	01	0	0	1	1	1	1	00	00	0	0	0	0	0	0	0	000	**	Open-ended
CMD26	R1	0	0	011010	01	0	0	1	1	0	0	00	00	0	0	0	0	0	0	0	000	**	
CMD27	R1	0	0	011011	01	0	0	1	1	0	0	00	00	0	0	0	0	0	0	0	000	**	
CMD28	R1b	0	0	011100	01	1	0	0	0	0	0	00	00	0	0	0	0	0	0	0	000	00	
CMD29	R1b	0	0	011101	01	1	0	0	0	0	0	00	00	0	0	0	0	0	0	0	000	00	
CMD30	R1	0	0	011110	01	0	0	1	0	0	0	00	00	0	0	0	0	0	0	0	000	**	
CMD35	R1	0	0	100011	01	0	0	0	0	0	0	00	00	0	0	0	0	0	0	0	000	00	

Table 27.6 Setting Values of CE_CMD_SET 2 (sequence with Boot Operation)

		CE_CMD_SET																				
	Boot Acknowledge	Reserved	BOOT	CMD[5:0]	RTYP[1:0]	RBSY	CCSEN	WDAT	DWEN	CMLTE	CMD12EN	RIDXC[1:0]	RCRC7C[1:0]	Reserved	CRC16C	BOOTACK	CRCSTE	TBIT	OPDM	CCSH	Reserved[2:0]	DATW[1:0]	note
—	W	0	1	000000	00	0	0	1	0	1	0	00	00	0	0	1	0	0	0	0	000	**	
	W / O	0	1	000000	00	0	0	1	0	1	0	00	00	0	0	0	0	0	0	0	000	**	

Table 27.7 Setting Values of CE_CMD_SET 3 (sequence of CE_ATA)

		CE_CMD_SET																				
Command	Response	Reserved	BOOT	CMD[5:0]	RTYP[1:0]	RBSY	CCSEN	WDAT	DWEN	CMLTE	CMD12EN	RIDXC[1:0]	RCRC7C[1:0]	Reserved	CRC16C	BOOTACK	CRCSTE	TBIT	OPDM	CCSH	Reserved[2:0]	DATW[1:0]	note
CMD60	R1	0	0	111100	01	0	0	1	0	0	0	00	00	0	0	0	0	0	0	0	000	**	Read
	R1b	0	0	111100	01	1	0	1	1	0	0	00	00	0	0	0	0	0	0	0	000	**	Write
CMD61	R1b	0	0	111101	01	1	1	0	0	0	0	00	00	0	0	0	0	0	0	*	000	**	No data
	R1	0	0	111101	01	0	1	1	0	1	0	00	00	0	0	0	0	0	0	*	000	**	Read
	R1b	0	0	111101	01	1	1	1	1	1	0	00	00	0	0	0	0	0	0	*	000	**	Write

Section 28 NAND Flash Memory Controller (FLCTL)

The NAND flash memory controller (FLCTL) provides a memory interface for an external NAND-type flash memory. To take measures for errors specific to flash memory, the FLCTL supports the ECC-code generation function and error detection function. It also supports ×16-bit configuration products. The FLCTL generates ECC code with up to 4 symbols, detects ECC code errors and has an error pattern generation circuit.

28.1 Features

28.1.1 NAND-Type Flash Memory Interface

- Interface directly connectable to NAND-type flash memory
- Read or write in sector units (512 + 16 bytes) and ECC processing executed
- In this manual, an access unit of 512 + 16 bytes, referred to as a sector, is always used. Note, however, that the size of a page is (515 + 16), (1024 + 32), or (2048 + 64) bytes depending on the type of flash memory being connected.
- Read or write in byte units
- Supports addresses of up to 5 bytes

Note: An access unit of 512 + 16bytes is referred to as a page in some datasheets for NAND-type flash memory. In this manual, this access unit of 512 + 16 bytes is always referred to as a sector. Each page of 2048 + 64 bytes is divided into four sectors, each consisting of 512 + 16 bytes. Although each page consists of 1024 + 32 words for 16-bit I/O products, a page is divided into four sectors even for 16-bit products.

28.1.2 Access Modes

The FLCTL can select one of the following two access modes.

- Command access mode: Performs an access by specifying a command to be issued from the FLCTL to flash memory, address, and data size to be input or output. Read, write, or erasure of data without ECC processing can be achieved.
- Sector access mode: Performs a read or write in sector units by specifying a sector address and controls ECC-code generation and check. By specifying the number of sectors, the continuous sectors can be read or written (specify addresses in sector addresses).
- High-speed sector access mode: The following commands are supported to access the flash memory at a high speed. Note that some flash memory products do not support these

commands:
- “Auto Page Program Operation with Data Cache”
- “Read Operation with Read Cache”

28.1.3 Sectors and Control Codes

- A sector is comprised of 512-byte data and 16-byte control code. The 16-byte control code includes 8-byte ECC.
- The control code includes 10-byte ECC when using a 4-symbol ECC circuit.
- The position of the ECC in the control code can be specified in 4-byte units.
- The user can write any data into bytes 0 to 5 in the control code area when using a 4-symbol ECC circuit.
- User information can be written to the control code other than the ECC.

28.1.4 3-symbol ECC

- 8-byte ECC code is generated and error check is performed for a sector (512-byte data + 16-byte control code). (Note that the ECC code generation in the 16-byte control code and the number of bytes to be checked differ depending on the specifications.)
- Error correction capability is up to three errors.
- In a write operation, an ECC code is generated for data and control code prior to the ECC. The control code following the ECC is not considered.
- In a read operation, an ECC error is checked for data and control code prior to the ECC. An ECC on the control code in the FIFO is replaced with the check result by the ECC circuit, not an ECC code read from flash memory.
- An error correction is not performed even when an ECC error occurs. Error corrections must be performed by software.

28.1.5 4-symbol ECC

- 80-bit (10-byte) ECC code is added to a sector (512-byte data + 6-byte control code).
- Error correction and detection capability covers up to four random errors (up to 40 bits).
- In a write operation, an ECC code is generated for data and control code prior to the ECC.
- In a read operation, an ECC error is checked for data and control code prior to the ECC. An ECC on the control code in the FIFO is replaced with the check result by the ECC circuit, not an ECC code read from flash memory.
- The 4-symbol ECC circuit in this FLCTL can generate error correction patterns using the hardware. The error correction pattern generation and checking are performed in sector units.

- The hardware-based error correction outputs addresses indicating the locations of errors and error patterns to correct errors.
- ECC correction algorithm in the 3-symbol ECC circuit and the 4-symbol ECC circuit use Reed-Solomon

28.1.6 Data Error

- When a program error or erase error occurs, the error is reflected on the error source flags. Interrupts for each source can be specified.
- When a read error occurs, an ECC in the control code is other than 0. This read error is reflected on the ECC error source flag.
- When an ECC error occurs, perform an error correction, specify another sector to be replaced, and copy the contents of the block to another sector as required.

28.1.7 Data Transfer FIFO and Data Register

- The 224-byte FLDTFIFO is incorporated for data transfer of flash memory.
- The 32-byte FLECFIFO is incorporated for data transfer of control code.
- The overrun/underrun detection flag is provided for the access from the CPU and DMA.

28.1.8 DMA Transfer

- By individually specifying the destinations of data and control code of flash memory to the DMA controller, data and control code can be sent to different areas.

28.1.9 Access Size

- Registers can be accessed in 32 bits or 8 bits. Registers must be accessed in the specified access size.
- The FIFO is accessed in 32-bit (4-byte) units. If the specified number of bytes for read and write accesses is not a multiple of 4, the fractional bytes are handled as padding bytes.
- The register contents are damaged if the access size is violated.

28.1.10 Access Time

- The operating frequency of the FLCTL pins can be specified by the FCKSEL bit and the QTSEL bit in the common control register (FLCMNCR), regardless of the operating frequency of the peripheral bus. To ensure the setup time, these operating frequencies must be specified within the maximum operating frequency of memory to be connected.

28.1.11 Connection of ×16-Bit Configuration Flash Memory on the External Bus

Before connecting the LSI with a ×16-bit configuration flash memory, observe the following notes.

- The maximum number of bytes that can be continuously written to in sector access mode is that of one page. To write data that exceeds the maximum number of bytes, the address must be specified again.

Figure 28.1 shows a block diagram of the FLCTL.

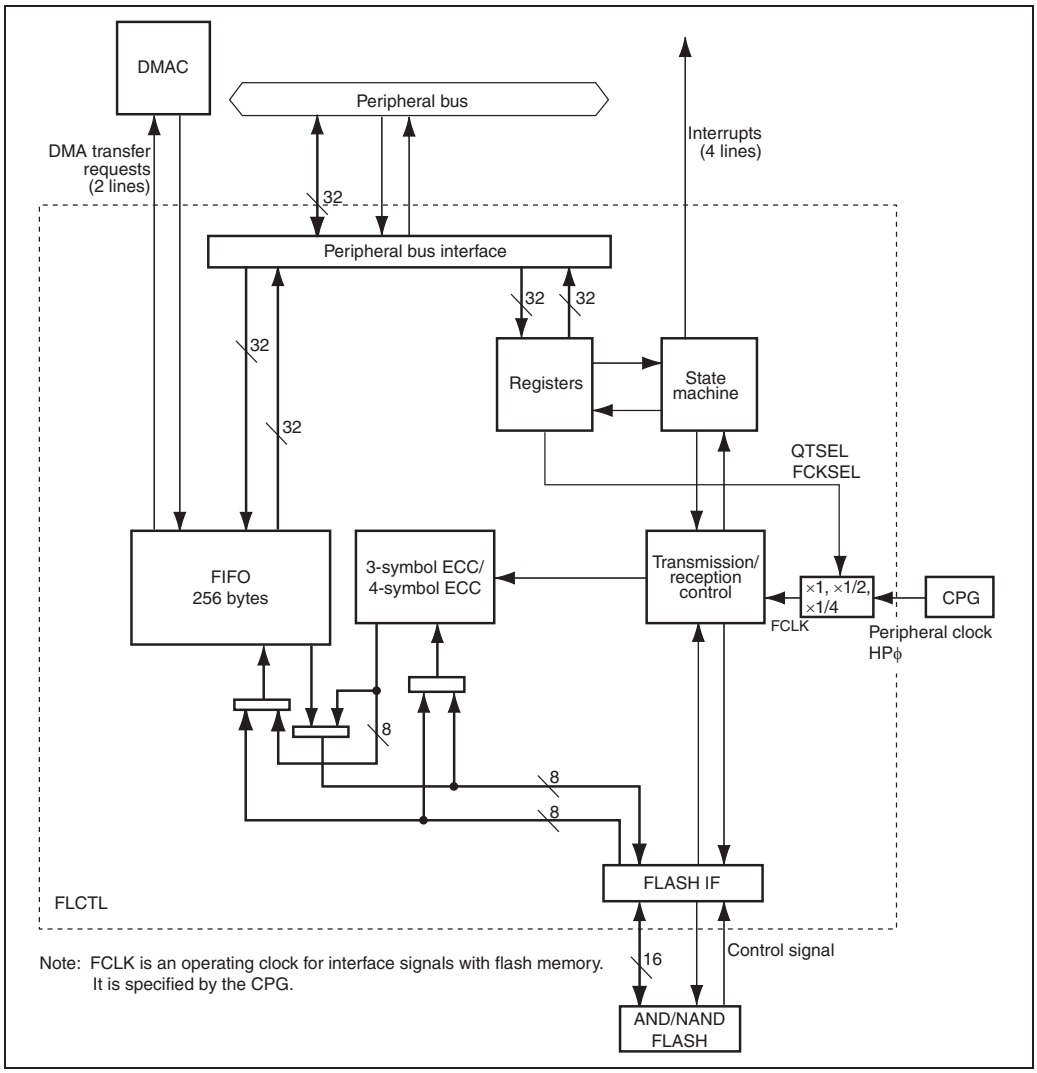


Figure 28.1 FLCTL Block Diagram

28.2 Input/Output Pins

The pin configuration of the FLCTL is listed in table 28.1.

Table 28.1 Pin Configuration

Pin Name	Function	I/O	Corresponding Flash Memory Pin	Description
$\overline{\text{FCE0}}$	Chip enable	Output	$\overline{\text{CE0}}$	Enables flash memory connected to this LSI.
$\overline{\text{FCE1}}$			$\overline{\text{CE1}}$	
NAF15 to NAF0	Data I/O pins	I/O	I/O15 to I/O0	I/O pins for command, address, and data.
FCDE	Command data enable	Output	CLE	Command Latch Enable (CLE) Asserted when a command is output. Command Data Enable ($\overline{\text{CDE}}$) Asserted when a command is output.
FOE	Output enable	Output	ALE	Address Latch Enable (ALE) Asserted when an address is output and negated when data is input or output. Output Enable ($\overline{\text{OE}}$) Asserted when data is input or when a status is read.
FSC	Serial clock	Output	$\overline{\text{RE}}$	Read Enable ($\overline{\text{RE}}$) Reads data at the falling edge of $\overline{\text{RE}}$. Serial Clock (SC) Inputs or outputs data synchronously with the SC.
$\overline{\text{FWE}}$	Write enable	Output	$\overline{\text{WE}}$	Write Enable Flash memory latches a command, address, and data at the rising edge of $\overline{\text{WE}}$.
FRB	Ready/busy	Input	R/$\overline{\text{B}}$	Ready/Busy Indicates ready state at high level; indicates busy state at low level.
—*	—	—	$\overline{\text{WP}}$	Write Protect/Reset When this pin goes low, erroneous erasure or programming at power on or off can be prevented.
—*	—	—	$\overline{\text{SE}}$	Spare Area Enable Used to access spare area. This pin must be fixed at low in sector access mode.

Note: * Not supported in this LSI.

28.3 Register Descriptions

Table 28.2 shows the FLCTL register configuration. Table 28.3 shows the register state in each processing mode.

Table 28.2 Register Configuration of FLCTL

Name	Abbreviation	R/W	Address	Access Size
Common control register	FLCMNCR	R/W	H'E6A3 0000	32
Command control register	FLCMDCR	R/W	H'E6A3 0004	32
Command code register	FLCMCDR	R/W	H'E6A3 0008	32
Address register	FLADR	R/W	H'E6A3 000C	32
Address register 2	FLADR2	R/W	H'E6A3 003C	32
Data register	FLDATAR	R/W	H'E6A3 0010	32
Data counter register	FLDTCNTR	R/W	H'E6A3 0014	32
Interrupt DMA control register	FLINTDMACR	R/W	H'E6A3 0018	32
Ready busy timeout setting register	FLBSYTMR	R/W	H'E6A3 001C	32
Ready busy timeout counter	FLBSYCNT	R	H'E6A3 0020	32
Data FIFO register	FLDTFIFO	R/W	H'E6A3 0024/ H'E6A3 0050	32
Control code FIFO register	FLECFIFO	R/W	H'E6A3 0028/ H'E6A3 0060	32
Transfer control register	FLTRCR	R/W	H'E6A3 002C	8
Bus occupation period setting register	FLHOLDCR	R/W	H'E6A3 0038	32
4-symbol ECCRESULT1	FL4ECCRESULT1	R	H'E6A3 0080	32
4-symbol ECCRESULT2	FL4ECCRESULT2	R	H'E6A3 0084	32
4-symbol ECCRESULT3	FL4ECCRESULT3	R	H'E6A3 0088	32
4-symbol ECCRESULT4	FL4ECCRESULT4	R	H'E6A3 008C	32
4-symbol ECC control register	FL4ECCCR	R/W	H'E6A3 0090	32
ECC error count register	FL4ECCCNT	R/W	H'E6A3 0094	32
Error address indication register	FLERRADR	R/W	H'E6A3 0098	32

Table 28.3 Register State of FLCTL in Each Processing Mode

Register Abbreviation	Reset *	Module Standby
FLCMNCR	Initialized	Retained
FLCMDCR	Initialized	Retained
FLCMCDR	Initialized	Retained
FLADR	Initialized	Retained
FLADR2	Initialized	Retained
FLDATAR	Initialized	Retained
FLDTCNTR	Initialized	Retained
FLINTDMACR	Initialized	Retained
FLBSYTMR	Initialized	Retained
FLBSYCNT	Initialized	Retained
FLDTFIFO	Initialized	Retained
FLECFIFO	Initialized	Retained
FLTRCR	Initialized	Retained
FL4ECCRESULT0	Initialized	Retained
FL4ECCRESULT1	Initialized	Retained
FL4ECCRESULT2	Initialized	Retained
FL4ECCRESULT3	Initialized	Retained
FL4ECCCR	Initialized	Retained
FL4ECCCNT	Initialized	Retained
FLERRADR	Initialized	Retained

Note: * For details, refer to section 1-D Overview of reset.

28.3.1 Common Control Register (FLCMNCR)

FLCMNCR is a 32-bit readable/writable register that specifies the type (NAND) of flash memory, access mode, and $\overline{\text{FCE}}$ pin output.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	PULSE[3]	FLMLC	ECCPOS[2]	4ECCCNTEN	4ECCEN	4ECCCORREC	BUSYON	SHBUSSEL	16BITSEL	SNAND	PULSE[2]	ENDIAN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PULSE[1]	–	ECCPOS[1:0]		ACM[1:0]		PULSE[0]	–	–	–	–	CE1	CE0	–	–	TYPESEL
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
27	PULSE[3]	0	R/W	Use this bit to set the pulse width of each clock (WE and RE) used to access the flash memory. Refer to PULSE[2] for details.
26	FLMLC	0	R/W	Large Block Access Select Selects a data alignment used to access a large-block product. This bit is invalid when the SNAND bit is set to 0. 0: A large block is accessed in 512-byte + 16-byte units. 1: A large block is accessed in 2048-byte + 64-byte units. (A large block is accessed by changing the column address.) Note: When setting PULSE[3:0] to 4'b1000, setting this bit to 1 is prohibited.
25	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
24	4ECCCNTEN	0	R/W	4-Symbol ECC Error Count Outputs the total number of errors included in the read sector and the maximum number of errors in the read sector. 0: Counting is not executed. 1: The 4-symbol ECC circuit is used to output the total number of errors and the maximum number of errors included in the read sector. Note: When setting this bit to 1, set the 4ECCCORRECT bit to 0.
23	4ECCEN	0	R/W	4-Symbol ECC Circuit Enable When this bit is set to 1 in sector access mode, the 4-symbol ECC circuit is enabled. Flash memory can only be read and written. 0: The 3-symbol ECC circuit is enabled. 1: The 4-symbol ECC circuit is enabled.
22	4ECC CORRECT	0	R/W	4-Symbol ECC Correction Information Generation The 4-symbol ECC circuit is used to generate information required for correction for one sector. After finishing reading one sector, set the 4-symbol ECC control register to generate error patterns. For details, see section 28.4, 4-Symbol ECC. 0: Only outputs ECC code, not outputting correction patterns. 1: Stops reading when an ECC error occurs. Resume the operation after reading the error pattern.
21	BUSYON	0	R/W	Busy Select This bit is only enabled when the FLCTL pins are multiplexed with the external bus. Set this bit to select whether or not to release the external bus mastership during a busy period. Note that $\overline{CE}$ must not be negated during a busy period depending on the flash memory in use. 0: Holds bus mastership during a busy period. 1: Releases bus mastership during a busy period. Note: When FLCTL processing is completed, $\overline{CE}$ is negated regardless of the status of ready/busy. For details, see section 28.9, Usage Notes.

Bit	Bit Name	Initial Value	R/W	Description
20	SHBUSSEL	1	R/W	External Bus Connection Set this bit to 1 when the I/O section is multiplexed with the external bus through BSC. 0: When the I/O pins of the flash memory are for exclusive use by the I/O function 1: When the I/O pins of the flash memory are multiplexed with the external bus Note: Set this bit to 1 because the FLCTL pins are multiplexed with the external bus.
19	16BITSEL	0	R	16-Bit I/O Select Set this bit to 1 when flash memory with ×16-bit configuration is specified. 0: When flash memory with ×8-bit configuration is specified 1: When flash memory with ×16-bit configuration is specified
18	SNAND	0	R/W	Large-Capacity NAND Flash Memory Select Set this bit to 1 when using 1-Gbit or larger NAND-type flash memory, in which one page is equal to 2048 + 64 bytes, or 1-Gbit or larger AG-AND-type flash memory. 0: When using flash memory in which one page is equal to 512 + 16 bytes or AND-type flash memory 1: When using NAND-type flash memory, in which one page is equal to 2048 + 64 bytes, or 1-Gbit or larger AG-AND-type flash memory

Bit	Bit Name	Initial Value	R/W	Description
17	PULSE[2]	0	R/W	Flash Clock Select Use this bit to set the pulse width of each clock (WE and RE) used to access the flash memory. • When connecting an 8-bit IO product 000: Low: 1 HPϕ cycle, High: 1 HPϕ cycle 001: Low: 2 HPϕ cycles, High: 2 HPϕ cycles 010: Low: 0.5 HPϕ cycle, High: 0.5 HPϕ cycle 011: Low: 1 HPϕ cycle, High: 1 HPϕ cycle 100: Low: 2 HPϕ cycles, High: 2 HPϕ cycles 101: Low: 4 HPϕ cycles, High: 4 HPϕ cycles 110: Low: 1.5 HPϕ cycle, High: 1.5 HPϕ cycle 111: Low: 3 HPϕ cycles, High: 3 HPϕ cycles • When connecting an 16-bit IO product — RE pulse width ***0: Setting prohibited 0001: Low: 6 HPϕ cycles, High: 2 HPϕ cycles 0011: Setting prohibited 0101: Low: 12 HPϕ cycles, High: 4 HPϕ cycles 0111: Low: 9 HPϕ cycles, High: 3 HPϕ cycles 1000: Low : 6 HPϕ cycles, High: 2 HPϕ cycles Note: When ; page read and setting this bits to 1000,this bits is replaced to 0001 — WE pulse width ***0: Setting prohibited 0001: Low: 2 HPϕ cycles, High: 6 HPϕ cycles 0011: Setting prohibited 0101: Low: 4 HPϕ cycles, High: 12 HPϕ cycles 0111: Low: 3 HPϕ cycles, High: 9 HPϕ cycles

Bit	Bit Name	Initial Value	R/W	Description
16	ENDIAN	0	R/W	FIFO Data Endian Specification 0: Big endian When writing to flash memory the data in FLDTFIFO and FLECFIFO in the FLCTL is output in the order of bits 31 to 24, 23 to 16, 15 to 8, 7 to 0, and then again 31 to 24, and so on. When reading from flash memory, output data from the flash memory is stored in FIFO in the order of: the first data to bits 31 to 24, the second data to 23 to 16, the third data to 15 to 8, the fourth data to 7 to 0, the fifth data to 31 to 22, and so on, in FLDTFIFO and FLECFIFO. 1: Little endian When writing to flash memory the data in FLDTFIFO and FLECFIFO in the FLCTL is output in the order of bits 7 to 0, 15 to 8, 23 to 16, 31 to 24, and then again 7 to 0, and so on. When reading from flash memory, output data from the flash memory is stored in FIFO in the order of: the first data to bits 7 to 0, the second data to 15 to 8, the third data to 23 to 16, the fourth data to 31 to 24, the fifth data to 7 to 0, and so on, in FLDTFIFO and FLECFIFO.
15	PULSE[1]	0	R/W	Flash Clock Select Use this bit to set the pulse width of each clock (WE and RE) used to access the flash memory. For details, see the description for the PULSE[2] bit.
14	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
13, 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11, 10	ACM[1:0]	00	R/W	Access Mode Specification Specifies access mode. 00: Command access mode 01: Sector access mode 10: High-speed sector access mode 11: Setting prohibited. Note: Set the FLMLC bit to 0 in high-speed sector access mode.
9	PULSE[0]	0	R/W	Flash Clock Select Use this bit to set the pulse width of each clock (WE and RE) used to access the flash memory. For details, see the description for the PULSE[2] bit.
8 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
4	CE1	0	R/W	Chip Enable 1 0: Disable (Outputs a high-level signal to the $\overline{\text{FCE1}}$ pin) 1: Enable (Outputs a low-level signal to the $\overline{\text{FCE1}}$ pin)
3	CE0	0	R/W	Chip Enable 0 0: Disable (Outputs a high-level signal to the $\overline{\text{FCE0}}$ pin) 1: Enable (Outputs a low-level signal to the $\overline{\text{FCE0}}$ pin)
2, 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	TYPESEL	0	R/W	Memory Interface Select When this module is used, Write 1 to this bit.

Note: Both the CE0 and CE1 bits should not be enabled at the same time.

28.3.2 Command Control Register (FLCMDCR)

FLCMDCR is a 32-bit readable/writable register that issues a command in command access mode, specifies address issue, and specifies source or destination of data transfer. In sector access mode, FLCMDCR specifies the number of sector transfers.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ADR CNT2	SCTCNT[19:16]				ADR MD	CDS RC	DOSR	—	—	SEL RW	DOA DR	ADRCNT[1:0]		DOC MD2	DOC MD1
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SCTCNT[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	ADRCNT2	0	R	Address Issue Byte Count Specification Specifies the number of bytes for the address data to be issued in address stage. This bit is used together with ADRCNT[1:0]. 0: Issue the address of byte count, specified by ADRCNT[1:0]. 1: Issue 5-byte address. Set the ADRCNT1 and ADRCNT0 bits to B'00.
30 to 27	SCTCNT [19:16]	All 0	R/W	Sector Transfer Count Specification [19:16] These bits are extended bits of the sector transfer count specification [15:0], SCTCNT[15:0]. SCTCNT[19:16] and SCTCNT[15:0] are used together to operate as SCTCNT[19:0], the 20-bit counter.
26	ADRMD	0	R/W	Sector Access Address Specification This bit is invalid in command access mode. This bit is valid only in sector access mode. 0: The value of the address register is handled as a physical sector number. Use this value usually in sector access. 1: The value of the address register is output as the address of flash memory. Note: Clear this bit to 0 in continuous sector access.

Bit	Bit Name	Initial Value	R/W	Description
25	CDSRC	0	R/W	Data Buffer Specification Specifies the data buffer to be read from or written to in the data stage in command access mode. 0: Specifies FLDATAR as the data buffer. 1: Specifies FLDTFIFO as the data buffer.
24	DOSR	0	R/W	Status Read Check Specifies whether or not the status read is performed after the second command has been issued. 0: Performs no status read 1: Performs status read
23, 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
21	SELRW	0	R/W	Data Read/Write Specification Specifies the direction of read or write in data stage. 0: Read 1: Write
20	DOADR	0	R/W	Address Stage Execution Specification Specifies whether or not the address stage is executed in command access mode. 0: Performs no address stage 1: Performs address stage
19, 18	ADRCNT [1:0]	00	R/W	Address Issue Byte Count Specification Specify the number of bytes for the address data to be issued in address stage. 00: Issue 1-byte address 01: Issue 2-byte address 10: Issue 3-byte address 11: Issue 4-byte address
17	DOCMD2	0	R/W	Second Command Stage Execution Specification Specifies whether or not the second command stage is executed in command access mode. 0: Does not execute the second command stage 1: Executes the second command stage

Bit	Bit Name	Initial Value	R/W	Description
16	DOCMD1	0	R/W	First Command Stage Execution Specification Specifies whether or not the first command stage is executed in command access mode. 0: Does not execute the first command stage 1: Executes the first command stage
15 to 0	SCTCNT [15:0]	H'0000	R/W	Sector Transfer Count Specification [15:0] Specify the number of sectors to be read continuously in sector access mode. These bits are counted down for each sector transfer end and stop when they reach 0. These bits are used together with SCTCNT[19:16]. In command access mode, these bits are H'0 0001.

28.3.3 Command Code Register (FLCMCDR)

FLCMCDR is a 32-bit readable/writable register that specifies a command to be issued in command access or sector access.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMD[15:8]								CMD[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

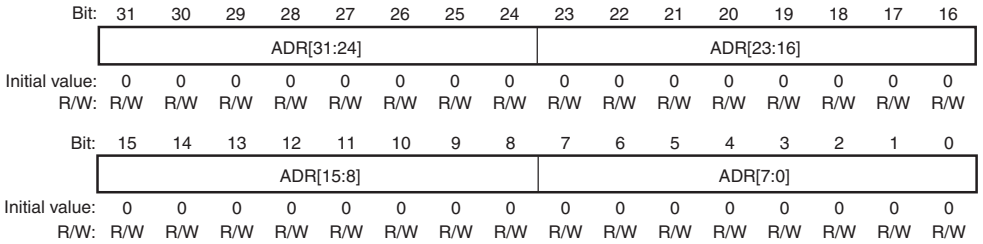
Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 8	CMD[15:8]	H'00	R/W	Specify a command code to be issued in the second command stage.
7 to 0	CMD[7:0]	H'00	R/W	Specify a command code to be issued in the first command stage.

28.3.4 Address Register (FLADR)

FLADR is a 32-bit readable/writable register that specifies an address to be output in command access mode. In sector access mode, a physical sector number specified in the physical sector address bits is converted into an address to be output by setting the ADRMD bit in FLCMDCR to 0.

Specify the start sector address in continuous sector access mode.

(a) ADRMD = 1



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	ADR[31:24]	H'00	R/W	Fourth Address Data Specify 4th data to be output to flash memory as an address in command access mode.
23 to 16	ADR[23:16]	H'00	R/W	Third Address Data Specify 3rd data to be output to flash memory as an address in command access mode.
15 to 8	ADR[15:8]	H'00	R/W	Second Address Data Specify 2nd data to be output to flash memory as an address in command access mode.
7 to 0	ADR[7:0]	H'00	R/W	First Address Data Specify 1st data to be output to flash memory as an address in command access mode.

(b) ADRMD = 0

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	ADR[25:16]									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ADR[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25 to 0	ADR[25:0]	H'000 0000	R/W	Physical Sector Address Specify a physical sector number to be accessed in sector access mode. For a large-block or 16-bit I/O product, a page address can be specified in the ADR25 to ADR2 bits or ADR17 to ADR2 bits, and a sector-based column address can be specified in the ADR1 and ADR0 bits. For a small-block product, only page addresses can be specified. When the ADRCNT2 bit is set to 1, the ADR25 to ADR0 bits are enabled. When the ADRCNT2 bit is set to 0, the ADR17 to ADR0 bits are enabled. • 8-bit I/O product (large-block) ADR[1:0]: B'00 → 0th byte (0 sectors) ADR[1:0]: B'01 → 512+16th byte (1 sector) ADR[1:0]: B'10 → 1024+32nd byte (2 sectors) ADR[1:0]: B'11 → 1536+48th byte (3 sectors) • 16-bit I/O product ADR[1:0]: B'00 → 0th word (0 sectors) ADR[1:0]: B'01 → 512+16th word (2 sectors) For details, see figure 28.3.

28.3.5 Address Register 2 (FLADR2)

FLADR2 is a 32-bit readable/writable register, and is valid when the ADRCNT2 bit in FLCMDCR is set to 1. FLADR2 specifies an address to be output in command access mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	ADR[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	ADR[7:0]	H'00	R/W	Fifth Address Data Specify 5th data to be output to flash memory as an address in command access mode.

28.3.6 Data Counter Register (FLDTCNTR)

FLDTCNTR is a 32-bit readable/writable register that specifies the number of bytes to be read or written in command access mode.

Note: This register is unavailable for reading or writing continuous data of five bytes or more.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ECFLW[7:0]								DTFLW[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	DTCNT[11:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	ECFLW[7:0]	H'00	R	FLECFIFO Access Count Specify the number of longwords in FLECFIFO to be read or written. These bit values are used when the CPU reads from or writes to FLECFIFO. In FLECFIFO read, these bits specify the number of longwords of the data that can be read from FLECFIFO. In FLECFIFO write, these bits specify the number of longwords of unoccupied area that can be written in FLECFIFO.
23 to 16	DTFLW[7:0]	H'00	R	FLDTFIFO Access Count Specify the number of longwords in FLDTFIFO to be read or written. These bit values are used when the CPU reads from or writes to FLDTFIFO. In FLDTFIFO read, these bits specify the number of longwords of the data that can be read from FLDTFIFO. In FLDTFIFO write, these bits specify the number of longwords of unoccupied area that can be written in FLDTFIFO.
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 0	DTCNT[11:0]	H'000	R/W	Data Count Specification Specify the number of bytes of data to be read or written in command access mode. (Up to 2048 + 64 bytes can be specified.)

28.3.7 Data Register (FLDATAR)

FLDATAR is a 32-bit readable/writable register. It stores input/output data used when 0 is written to the CDSRC bit in FLCMDCR in command access mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DT[31:24]								DT[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DT[15:8]								DT[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	DT[31:24]	H'00	R/W	Fourth Data Specify the 4th data to be input or output via the NAF7 to NAF0 pins. In write: Specify write data In read: Store read data
23 to 16	DT[23:16]	H'00	R/W	Third Data Specify the 3rd data to be input or output via the NAF7 to NAF0 pins. In write: Specify write data In read: Store read data
15 to 8	DT[15:8]	H'00	R/W	Second Data Specify the 2nd data to be input or output via the NAF7 to NAF0 pins. In write: Specify write data In read: Store read data
7 to 0	DT[7:0]	H'00	R/W	First Data Specify the 1st data to be input or output via the NAF7 to NAF0 pins. In write: Specify write data In read: Store read data

28.3.8 Interrupt DMA Control Register (FLINTDMACR)

FLINTDMACR is a 32-bit readable/writable register that enables or disables DMA transfer requests or interrupts. A transfer request from the FLCTL to the DMAC is issued after each access mode has been started.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	ECER INTE	—	DMA MULTI	FIFOTRG [1:0]		AC1 CLR	AC0 CLR	DREQ1 EN	DREQ0 EN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	EC ERB	ST ERB	BTO ERB	TRR EQF1	TRR EQF0	STER INTE	RBER INTE	TE INTE	TR INTE1	TR INTE0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	ECERINTE	0	R/W	ECC Error Interrupt Enable 0: Disables an interrupt when an ECC error occurs 1: Enables an interrupt when an ECC error occurs
23	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
22	DMAMULTI	0	R/W	DMA 16-byte Transfer Select 0: When DMA transfer is not used or in DMA longword transfer mode 1: In DMA 16-byte transfer mode

Bit	Bit Name	Initial Value	R/W	Description
21, 20	FIFOTRG [1:0]	00	R/W	FIFO Trigger Setting* Change the condition for the FIFO transfer request. In flash-memory read: 00: Issue an interrupt or a DMA transfer request to the CPU when FLDTFIFO stores 4 bytes of data. 01: Issue an interrupt or a DMA transfer request to the CPU when FLDTFIFO stores 16 bytes of data. 10: Issue an interrupt or a DMA transfer request to the CPU when FLDTFIFO stores 128 bytes of data. 11: Issue an interrupt to the CPU when FLDTFIFO stores 128 bytes of data, or issue a DMA transfer request to the CPU when FLDTFIFO stores 16 bytes of data. In flash-memory programming: 00: Issue an interrupt to the CPU when FLDTFIFO has empty area of 4 bytes or more (do not set DMA transfer). 01: Issue an interrupt or a DMA transfer request to the CPU when FLDTFIFO has empty area of 16 bytes or more. 10: Issue an interrupt to the CPU when FLDTFIFO has empty area of 128 bytes or more (do not set DMA transfer). 11: Issue an interrupt to the CPU when FLDTFIFO has empty area of 128 bytes or more, or issue a DMA transfer request to the CPU when FLDTFIFO has empty area of 16 bytes or more.
19	AC1CLR	0	R/W	FLECFIFO Clear Clears FLECFIFO. 0: Retains the FLECFIFO value. In flash-memory access, this bit should be cleared to 0. 1: Clears FLECFIFO. After FLECFIFO has been cleared, this bit should be cleared to 0.

Bit	Bit Name	Initial Value	R/W	Description
18	AC0CLR	0	R/W	FLDTFIFO Clear Clears FLDTFIFO. 0: Retains the FLDTFIFO value. In flash-memory access, this bit should be cleared to 0. 1: Clears FLDTFIFO. After FLDTFIFO has been cleared, this bit should be cleared to 0.
17	DREQ1EN	0	R/W	FLECFIFODMA Request Enable Enables or disables the DMA transfer request issued from FLECFIFO. 0: Disables the DMA transfer request issued from FLECFIFO 1: Enables the DMA transfer request issued from FLECFIFO
16	DREQ0EN	0	R/W	FLDTFIFODMA Request Enable Enables or disables the DMA transfer request issued from FLDTFIFO. 0: Disables the DMA transfer request issued from the FLDTFIFO 1: Enables the DMA transfer request issued from the FLDTFIFO
15	DTOERB	0	R/W	Data-area FIFO0 Buffer Overrun Detects and indicates an overrun of the FIFO0 address counter. No interrupt occurs even if this bit is set to 1. 1 cannot be written into this flag bit. Only 0 can be written to clear the flag. 0: No overrun has occurred in FLDTFIFO. 1: An overrun has occurred in FLDTFIFO.
14	DTUERB	0	R/W	Data-area FIFO0 Buffer Underrun Detects and indicates an underrun of the FIFO0 address counter. No interrupt occurs even if this bit is set to 1. 1 cannot be written into this flag bit. Only 0 can be written to clear the flag. 0: No underrun has occurred in FLDTFIFO. 1: An underrun has occurred in FLDTFIFO.

Bit	Bit Name	Initial Value	R/W	Description
13	ECOERB	0	R/W	Control code-area FIFO1 Buffer Overrun Detects and indicates an overrun of the FIFO1 address counter. No interrupt occurs even if this bit is set to 1. 1 cannot be written into this flag bit. Only 0 can be written to clear the flag. 0: No overrun has occurred in FLECFIFO. 1: An overrun has occurred in FLECFIFO.
12	ECUERB	0	R/W	Control code-area FIFO1 Buffer Underrun Detects and indicates an underrun of the FIFO1 address counter. No interrupt occurs even if this bit is set to 1. 1 cannot be written into this flag bit. Only 0 can be written to clear the flag. 0: No underrun has occurred in FLECFIFO. 1: An underrun has occurred in FLECFIFO.
11, 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	ECERB	0	R/W	ECC Error Indicates the result of ECC error detection. This bit is set to 1 if an ECC error occurs while flash memory is read in sector access mode. No interrupt occurs even if this bit is set to 1. This bit is a flag. 1 cannot be written to this bit. Only 0 can be written to clear the flag. 0: Indicates that no ECC error occurs (Latched ECC is all 0.) 1: Indicates that an ECC error occurs

Bit	Bit Name	Initial Value	R/W	Description
8	STERB	0	R/W	Status Error Indicates the result of status read. This bit is set to 1 if the specific bit in the bits STAT[7:0] in FLBSYCNT is set to 1 in status read. This bit is a flag. 1 cannot be written to this bit. Only 0 can be written to clear the flag. 0: Indicates that no status error occurs (the specific bit in the bits STAT[7:0] in FLBSYCNT is 0.) 1: Indicates that a status error occurs For details on the specific bit in STAT7 to STAT0 bits, see section 28.4.7, Status Read.
7	BTOERB	0	R/W	Timeout Error This bit is set to 1 if a timeout error occurs (the bits RBTIMCNT[19:0] in FLBSYCNT are decremented to 0). This bit is a flag. 1 cannot be written to this bit. Only 0 can be written to clear the flag. 0: Indicates that no timeout error occurs 1: Indicates that a timeout error occurs
6	TRREQF1	0	R/W	FLECFIFO Transfer Request Flag Indicates that a transfer request is issued from FLECFIFO. This bit is a flag. 1 cannot be written to this bit. Only 0 can be written to clear the flag. 0: Indicates that no transfer request is issued from FLECFIFO 1: Indicates that a transfer request is issued from FLECFIFO
5	TRREQF0	0	R/W	FLDTFIFO Transfer Request Flag Indicates that a transfer request is issued from FLDTFIFO. This bit is a flag. 1 cannot be written to this bit. Only 0 can be written to clear the flag. 0: Indicates that no transfer request is issued from FLDTFIFO 1: Indicates that a transfer request is issued from FLDTFIFO

Bit	Bit Name	Initial Value	R/W	Description
4	STERINTE	0	R/W	Interrupt Enable at Status Error Enables or disables an interrupt request to the CPU when a status error has occurred. 0: Disables the interrupt request to the CPU by a status error 1: Enables the interrupt request to the CPU by a status error
3	RBERINTE	0	RW	Interrupt Enable at Timeout Error Enables or disables an interrupt request to the CPU when a timeout error has occurred. 0: Disables the interrupt request to the CPU by a timeout error 1: Enables the interrupt request to the CPU by a timeout error
2	TEINTE	0	R/W	Transfer End Interrupt Enable Enables or disables an interrupt request to the CPU when a transfer has been ended (TREND bit in FLTRCR). 0: Disables the transfer end interrupt request to the CPU 1: Enables the transfer end interrupt request to the CPU
1	TRINTE1	0	R/W	FLECFIFO Transfer Request Enable to CPU Enables or disables an interrupt request to the CPU by a transfer request issued from FLECFIFO. When the DMA transfer is enabled, this bit should be cleared to 0. 0: Disables an interrupt request to the CPU by a transfer request from FLECFIFO. 1: Enables an interrupt request to the CPU by a transfer request from FLECFIFO.

Bit	Bit Name	Initial Value	R/W	Description
0	TRINTE0	0	R/W	FLDTFIFO Transfer Request Enable to CPU Enables or disables an interrupt request to the CPU by a transfer request issued from FLDTFIFO. When the DMA transfer is enabled, this bit should be cleared to 0. 0: Disables an interrupt request to the CPU by a transfer request from FLDTFIFO 1: Enables an interrupt request to the CPU by a transfer request from FLDTFIFO

28.3.9 Ready Busy Timeout Setting Register (FLBSYTMR)

FLBSYTMR is a 32-bit readable/writable register that specifies the timeout time when the FRB pin is busy.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	RBTMOUT[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RBTMOUT[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	RBTMOUT[23:0]	H'00000	R/W	Ready Busy Timeout Specify timeout time (the number of HPϕ clocks) in busy state. When these bits are set to 0, timeout is not generated.

28.3.10 Ready Busy Timeout Counter (FLBSYCNT)

FLBSYCNT is a 32-bit read-only register.

The status of flash memory obtained by the status read is stored in the bits STAT[7:0].

The timeout time set in the bits RBTMOUT[19:0] in FLBSYTMR is copied to the bits RBTIMCNT[19:0] and counting down is started when the FRB pin is placed in a busy state. When values in the RBTIMCNT[19:0] become 0, 1 is set to the BTOERB bit in FLINTDMACR, thus notifying that a timeout error has occurred. In this case, an FLSTE interrupt request can be issued if an interrupt is enabled by the RBERINTE bit in FLINTDMACR.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	STAT[7:0]								RBTIMCNT[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RBTIMCNT[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	STAT[7:0]	H'00	R	Indicate the flash memory status obtained by the status read.
23 to 0	RBTIMCNT [23:0]	H'00 0000	R	Ready Busy Timeout Counter When the FRB pin is placed in a busy state, the values of the bits RBTMOUT[19:0] in FLBSYTMR are copied to these bits. These bits are counted down while the FRB pin is busy. A timeout error occurs when these bits are decremented to 0.

28.3.11 Data FIFO Register (FLDTFIFO)

FLDTFIFO is used to read or write the data FIFO area.

In DMA transfer, data in this register must be specified as the destination (source).

Note that the direction of read or write specified by the SELRW bit in FLCMDCR must match that specified in this register.

When transferring 16-byte DMA, access FLDTFIFO from the address (H'E6A3 0050) on the 16-byte address boundary.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DTFO[31:24]								DTFO[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DTFO[15:8]								DTFO[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	DTFO[31:24]	H'00	R/W	First Data Specify 1st data to be input or output via the NAF7 to NAF0 pins. In write: Specify write data In read: Store read data Note: The fourth data is input or output if the ENDIAN bit of FLCMNCR is set to 1.
23 to 16	DTFO[23:16]	H'00	R/W	Second Data Specify 2nd data to be input or output via the NAF7 to NAF0 pins. In write: Specify write data In read: Store read data Note: The third data is input or output if the ENDIAN bit of FLCMNCR is set to 1.

Bit	Bit Name	Initial Value	R/W	Description
15 to 8	DTFO[15:8]	H'00	R/W	Third Data Specify 3rd data to be input or output via the NAF7 to NAF0 pins. In write: Specify write data In read: Store read data Note: The second data is input or output if the ENDIAN bit of FLCMNCR is set to 1.
7 to 0	DTFO[7:0]	H'00	R/W	Fourth Data Specify 4th data to be input or output via the NAF7 to NAF0 pins. In write: Specify write data In read: Store read data Note: The first data is input or output if the ENDIAN bit of FLCMNCR is set to 1.

28.3.12 Control Code FIFO Register (FLECFIFO)

FLECFIFO is used to read or write the control code FIFO area.

In DMA transfer, data in this register must be specified as the destination (source).

Note that the direction of read or write specified by the SELRW bit in FLCMDCR must match that specified in this register.

When transferring 16-byte DMA, access FLECFIFO from the address (H'E6A3 0060) on the 16-byte address boundary.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ECFO[31:24]								ECFO[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ECFO[15:8]								ECFO[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	ECFO[31:24]	H'00	R/W	First Data Specify 1st data to be input or output via the NAF7 to NAF0 pins. In write: Specify write data In read: Store read data Note: The fourth data is input or output if the ENDIAN bit of FLCMNCR is set to 1.
23 to 16	ECFO[23:16]	H'00	R/W	Second Data Specify 2nd data to be input or output via the NAF7 to NAF0 pins. In write: Specify write data In read: Store read data Note: The third data is input or output if the ENDIAN bit of FLCMNCR is set to 1.
15 to 8	ECFO[15:8]	H'00	R/W	Third Data Specify 3rd data to be input or output via the NAF7 to NAF0 pins. In write: Specify write data In read: Store read data Note: The second data is input or output if the ENDIAN bit of FLCMNCR is set to 1.
7 to 0	ECFO[7:0]	H'00	R/W	Fourth Data Specify 4th data to be input or output via the NAF7 to NAF0 pins. In write: Specify write data In read: Store read data Note: The first data is input or output if the ENDIAN bit of FLCMNCR is set to 1.

28.3.13 Transfer Control Register (FLTRCR)

Setting the TRSTRT bit to 1 initiates access to flash memory. Access completion can be checked by the TREND bit. During the transfer (from when the TRSTRT bit is set to 1 until the TREND bit is set to 1), the processing should not be forcibly ended (by setting the TRSTRT bit to 0).

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	TRANSTATUS	TREND	TRSTRT
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	TRANSTATUS	0	R	Transfer State Indicates if the bus mastership of the external bus is acquired and the transfer is being performed. When the I/O pins are for exclusive use by the I/O function and not multiplexed with the external bus, the TRSTRT bit is set to 1. This bit, TRANSTATUS, is also set to 1. 0: Transfer is not started 1: Transfer is being performed or completed
1	TREND	0	R/W	Processing End Flag Bit Indicates that the processing performed in the specified access mode has been completed. The write value should always be 0.
0	TRSTRT	0	R/W	Transfer Start By setting this bit from 0 to 1 when the TREND bit is 0, processing in the access mode specified by the access mode specification bits ACM[1:0] is initiated. 0: Stops transfer 1: Starts transfer

28.3.14 Bus Occupancy Period Setting Register (FLHOLDCR)

FLHOLDCR is used to set the release frequency for the external bus of the FLCTL when another module (including the CPU) accesses the memory in the BSC while writing or reading a page to or from NAND-type flash memory. When the HOLDEN bit in this register is set to 0, the FLCTL occupies the external memory during data exchange with flash memory. Note that a deadlock may occur depending on where the program code is stored or how it is used.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	BUSREQ[1:0]		HOLDEN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
2, 1	BUSREQ	All 0	R/W	Bus Occupancy Period Setting Sets the bus occupancy period of the FLCTL. 00: Releases the bus when the FLCTL's FIFO becomes empty or full. 01: Releases the bus if another module accesses the memory in the BSC when the FLCTL is using the external bus exclusively. 10: FLCTL accesses are given priority in the following cases even when another module accesses the memory in the BSC when the FLCTL is using the external bus exclusively. • When writing to flash memory If 128 bytes or more data is stored in the FLCTL's FIFO • When reading from flash memory If 128 bytes or less data is stored in the FLCTL's FIFO 11: Setting prohibited However, note that the bus is not released during the transfer period regardless of the setting of this bet if the HOLDEN bit is set to 0.
0	HOLDEN	0	R/W	Bus Occupancy Enable Releases the external bus when writing or reading a page to or from flash memory. 0: The bus is not released ruing the transfer period. 1: The bus is released when the FIFO becomes empty or full.

28.3.15 4-Symbol ECCRESULT1 (FL4ECCRESULT1)

This register is valid only when the 4ECCEN bit and 4ECCCORRECT bits in FLCMNCR are set to 1 and correction patterns are generated based on 4ECCCR. The error correction pattern for the first error location that the 4-symbol ECC circuit outputs and the error position's address for the first error location are set in this register.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	LOC19	LOC18	LOC17	LOC16	LOC15	LOC14	LOC13	LOC12	LOC11	LOC10
Initial value:	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	PAT19	PAT18	PAT17	PAT16	PAT15	PAT14	PAT13	PAT12	PAT11	PAT10
Initial value:	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25	LOC19	1	R	First Error Address Indicates the first error address of four errors. The initial value is H'3FF. Since each sector contains 528 bytes, the valid addresses are H'000 to H'20F. Each value set in these bits becomes valid only after the 4ECCEND bit in 4ECCCR is set to 1. Note that reading data in the next sector before reading these bits destroys the data.
24	LOC18	1	R	
23	LOC17	1	R	
22	LOC16	1	R	
21	LOC15	1	R	
20	LOC14	1	R	
19	LOC13	1	R	
18	LOC12	1	R	
17	LOC11	1	R	
16	LOC10	1	R	
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
9	PAT19	1	R	First Error Correction Pattern
8	PAT18	1	R	Indicates the correction pattern for the first error of four errors. The initial value is H'3FF. One error location (symbol) consists of eight bits.
7	PAT17	1	R	
6	PAT16	1	R	Each value set in these bits becomes valid only after the 4ECCEND bit in 4ECCCR is set to 1. Note that reading data in the next sector before reading these bits destroys the data.
5	PAT15	1	R	
4	PAT14	1	R	
3	PAT13	1	R	
2	PAT12	1	R	
1	PAT11	1	R	
0	PAT10	1	R	

28.3.16 4-Symbol ECCRESULT2 (FL4ECCRESULT2)

This register is valid only when the 4ECCEN bit and 4ECCCORRECT bits in FLCMNCR are set to 1 and correction patterns are generated based on 4ECCCR. The error correction pattern for the second error location that the 4-symbol ECC circuit outputs and the error position's address for the second error location are set in this register.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	LOC 29	LOC 28	LOC 27	LOC 26	LOC 25	LOC 24	LOC 23	LOC 22	LOC 21	LOC 20
Initial value:	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	PAT 29	PAT 28	PAT 27	PAT 26	PAT 25	PAT 24	PAT 23	PAT 22	PAT 21	PAT 20
Initial value:	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
25	LOC29	1	R	Second Error Address Indicates the second error address of four errors. The initial value is H'3FF. Since each sector contains 528 bytes, the valid addresses are H'000 to H'20F. Each value set in these bits becomes valid only after the 4ECCEND bit in 4ECCCR is set to 1. Note that reading data in the next sector before reading these bits destroys the data.
24	LOC28	1	R	
23	LOC27	1	R	
22	LOC26	1	R	
21	LOC25	1	R	
20	LOC24	1	R	
19	LOC23	1	R	
18	LOC22	1	R	
17	LOC21	1	R	
16	LOC20	1	R	
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	PAT29	1	R	Second Error Correction Pattern Indicates the correction pattern for the second error of four errors. The initial value is H'3FF. One error location (symbol) consists of eight bits. Each value set in these bits becomes valid only after the 4ECCEND bit in 4ECCCR is set to 1. Note that reading data in the next sector before reading these bits destroys the data.
8	PAT28	1	R	
7	PAT27	1	R	
6	PAT26	1	R	
5	PAT25	1	R	
4	PAT24	1	R	
3	PAT23	1	R	
2	PAT22	1	R	
1	PAT21	1	R	
0	PAT20	1	R	

28.3.17 4-Symbol ECCRESULT3 (FL4ECCRESULT3)

This register is valid only when the 4ECCEN bit and 4ECCCORRECT bits in FLCMNCR are set to 1 and correction patterns are generated based on 4ECCCR. The error correction pattern for the third error location that the 4-symbol ECC circuit outputs and the error position's address for the third error location are set in this register.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	LOC 39	LOC 38	LOC 37	LOC 36	LOC 35	LOC 34	LOC 33	LOC 32	LOC 31	LOC 30
Initial value:	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	PAT 39	PAT 38	PAT 37	PAT 36	PAT 35	PAT 34	PAT 33	PAT 32	PAT 31	PAT 30
Initial value:	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25	LOC39	1	R	Third Error Address Indicates the third error address of four errors. The initial value is H'3FF. Since each sector contains 528 bytes, the valid addresses are H'000 to H'20F. Each value set in these bits becomes valid only after the 4ECCEND bit in 4ECCCR is set to 1. Note that reading data in the next sector before reading these bits destroys the data.
24	LOC38	1	R	
23	LOC37	1	R	
22	LOC36	1	R	
21	LOC35	1	R	
20	LOC34	1	R	
19	LOC33	1	R	
18	LOC32	1	R	
17	LOC31	1	R	
16	LOC30	1	R	
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
9	PAT39	1	R	Third Error Correction Pattern
8	PAT38	1	R	Indicates the correction pattern for the third error of four errors. The initial value is H'3FF. One error location (symbol) consists of eight bits.
7	PAT37	1	R	
6	PAT36	1	R	Each value set in these bits becomes valid only after the 4ECCEND bit in 4ECCCR is set to 1. Note that reading data in the next sector before reading these bits destroys the data.
5	PAT35	1	R	
4	PAT34	1	R	
3	PAT33	1	R	
2	PAT32	1	R	
1	PAT31	1	R	
0	PAT30	1	R	

28.3.18 4-Symbol ECCRESULT4 (FL4ECCRESULT4)

This register is valid only when the 4ECCEN bit and 4ECCCORRECT bits in FLCMNCR are set to 1 and correction patterns are generated based on 4ECCCR. The error correction pattern for the fourth error location that the 4-symbol ECC circuit outputs and the error position's address for the fourth error location are set in this register.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	LOC 49	LOC 48	LOC 47	LOC 46	LOC 45	LOC 44	LOC 43	LOC 42	LOC 41	LOC 40
Initial value:	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	PAT 49	PAT 48	PAT 47	PAT 46	PAT 45	PAT 44	PAT 43	PAT 42	PAT 41	PAT 40
Initial value:	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
25	LOC49	1	R	Fourth Error Address Indicates the fourth error address of four errors. The initial value is H'3FF. Since each sector contains 528 bytes, the valid addresses are H'000 to H'20F. Each value set in these bits becomes valid only after the 4ECCEND bit in 4ECCCR is set to 1. Note that reading data in the next sector before reading these bits destroys the data.
24	LOC48	1	R	
23	LOC47	1	R	
22	LOC46	1	R	
21	LOC45	1	R	
20	LOC44	1	R	
19	LOC43	1	R	
18	LOC42	1	R	
17	LOC41	1	R	
16	LOC40	1	R	
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	PAT49	1	R	Fourth Error Correction Pattern Indicates the correction pattern for the fourth error of four errors. The initial value is H'3FF. One error location (symbol) consists of eight bits. Each value set in these bits becomes valid only after the 4ECCEND bit in 4ECCCR is set to 1. Note that reading data in the next sector before reading these bits destroys the data.
8	PAT48	1	R	
7	PAT47	1	R	
6	PAT46	1	R	
5	PAT45	1	R	
4	PAT44	1	R	
3	PAT43	1	R	
2	PAT42	1	R	
1	PAT41	1	R	
0	PAT40	1	R	

28.3.19 4-Symbol ECC Control Register (FL4ECCCR)

This register is valid only when the 4-symbol ECC circuit is enabled and the 4ECCCORRECT bit in FLCMNCR is set to 1. When the 4ECCEXST bit in this register is set to 1, the 4-symbol ECC circuit calculates an error correction pattern and the address of the error location for the read data for one sector. When the 4ECCEND bit is set to 1, this indicates that processing is completed. When the 4ECCFA bit is set to 1, this indicates that there are five or more errors or the errors are uncorrectable error patterns. Only 0 can be written to this register. Writing 0 to this register after the 4ECCEND is set to 1, the read operation to flash memory resumes.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	4ECCFA	4ECCEND	4ECCEXST
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	4ECCFA	0	R/W	4-Symbol ECC Uncorrectable Only 0 can be written to this bit. Five or more errors detected are handled as uncorrectable and this bit is set to 1. 0: Correctable errors 1: Uncorrectable errors
1	4ECCEND	0	R/W	4-Symbol ECC Correction Pattern Generation Completion Only 0 can be written to this bit. When this bit is set to 1, this indicates that processing up to correction pattern generation is completed. When the 4ECCFA bit is set to 1 and this bit is set to 1, processing was aborted without generating a correction pattern since more than five errors have been detected.

Bit	Bit Name	Initial Value	R/W	Description
0	4ECCEXST	0	R/W	4ECC Correction Execution Only 0 can be written to this bit. When 4ECCCORRECT is 1 when an error is detected, error correction patterns are generated for one sector. 0: Error pattern generation stop 1: Correction patterns being generated When setting this bit to 1, do not write 0 to this register until the 4ECCEND bit is set to 1.

28.3.20 Error Address Indication Register (FLERRADR)

FLCTL stops its operation after reading the error sector if a status error or ECC error occurs while a write to or read from flash memory is in process in “Auto Page Program Operation with Data Cache” or “Read Operation with Read Cache” in high-speed sector access mode. This register indicates the address where read operation has stopped with a physical address.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	ECCADR_COL[1:0]		ERRADR_PAGE[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ERRADR_PAGE[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
25, 24	ECCADR_ COL [1:0]	00	R/W	When a status error or ECC error occurred, a column address where the read or write operation has stopped is set. Only 0 can be written. 00: First sector 01: Second sector 10: Third sector 11: Fourth sector Note: These bits are always set to 00 for a small-block product.
23 to 0	ERRADR_ PAGE [23:0]	H'00 0000	R/W	When a status error or ECC error occurred, a page address where the read or write operation has stopped is set. Only 0 can be written.

28.3.21 ECC Error Count Register (FL4ECCCNT)

This register is valid only when the 4ECCCNTEN bit in FLCMNCR is set to 1. FLCTL counts the number of ECC errors included in all the sectors that are read from flash memory. If more than five ECC errors are included in one sector, +5 is always set. This register also indicates the maximum number of errors included in one sector in all the sectors that have been read.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	ERRCNT1[10:0]										
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	ERRMAX[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 27	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
26 to 16	ERRCNT [10:0]	H'000	R/W	Error Count Only 0 can be written to these bits. Indicate the total number of errors included in the sectors that have been read continuously (up to one block: 64 pages × 4 sectors). Even if a sector contains more than five errors, the number of errors is counted as 5.
15 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2 to 0	ERRMAX [2:0]	000	R/W	Maximum Error Count Only 0 can be written to these bits. Indicates the maximum number of errors contained in a sector after comparing the number of errors contained in all the sectors that have been read. 000: The maximum number of errors was 0. 001: The maximum number of errors was 1. 010: The maximum number of errors was 2. 011: The maximum number of errors was 3. 100: The maximum number of errors was 4. 101: The maximum number of errors was 5 or more. 110: Not set. 111: Not set.

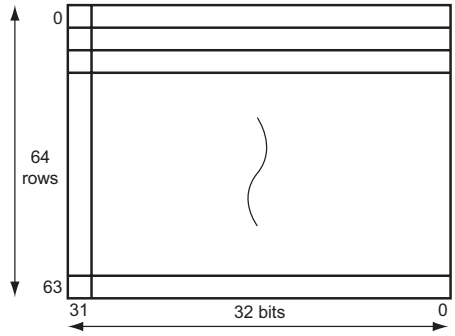
28.3.22 "Auto Page Program Operation with Data Cache" Command Address Specification Memory

This is a memory area to specify an address for the "Auto Page Program Operation with Data Cache" command. Write the page addresses to write from address 0 in the order of pages to be written. If the data written in this area matches H'8*** ****, the "Auto Page Program Operation with Data Cache" command is terminated.

If the ACM1 and ACM0 bits in the common control register (FLCMNCR) are set to B'10, the addresses set in the address register and address register 2 become invalid, and the address specified in this register becomes valid.

Only longword access can be made from the CPU to this memory area. Set the page address in bits 30 to 0 starting from the LSB. Set any unused upper bit to 0.

The address area is H'E6A3 1000 to H'E6A3 1100.



28.4 4-Symbol ECC

28.4.1 Overview of the 4-Symbol ECC Circuit

The former FLCTL used to have information that enables error correction for up to three symbols and the ECC code generation function that makes corrections using software. This FLCTL has information that enables error correction for up to four symbols and the ECC code generation function that can generate error correction patterns using hardware to support multi-level cell (MLC) flash memory. Generation of error correction patterns means generation of information required for error correction, not executing error correction.

Although the 4-symbol ECC circuit included in this FLCTL can correct errors of up to 10 bits per symbol (up to 40 bits in four symbols), it corrects errors of up to 32 bits because 8 bits are counted as one symbol in the data area of flash memory.

The 4-symbol ECC circuit consists of three stages:

1. ECC code generation circuit
2. Error location detection circuit
3. Error correction pattern generation circuit

ECC code can be generated consecutively. An error is determined and an error correction pattern is generated on a per-sector basis.

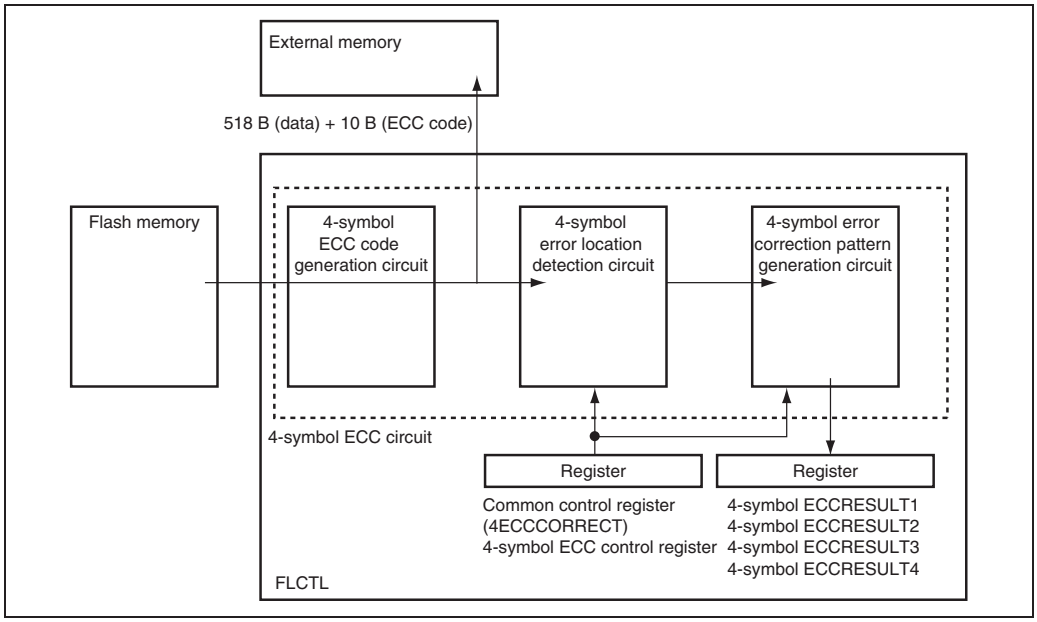


Figure 28.2 4-Symbol ECC Circuit Block Diagram

28.4.2 4-Symbol ECC Operation

Figure 28.3 shows the operation flow when the 4-symbol ECC circuit is used. When the 4ECCEN bit in FLCMNCR is set to 1, the 4-symbol ECC circuit is enabled. Information required for generating correction patterns is stored in the 4-symbol ECC circuit when the 4ECCCORRECT bit in the FLCMNCR is set to 1.

To execute ECC error determination and error correction, set the 4ECCCR register after reading one sector. No error can be corrected if there are five or more errors in one sector. If all of the 4-symbol ECCRESULT1, 4-symbol ECCRESULT2, 4-symbol ECCRESULT3 and 4-symbol ECCRESULT4 are set to the initial values after correction processing, this indicates that there has been no ECC error.

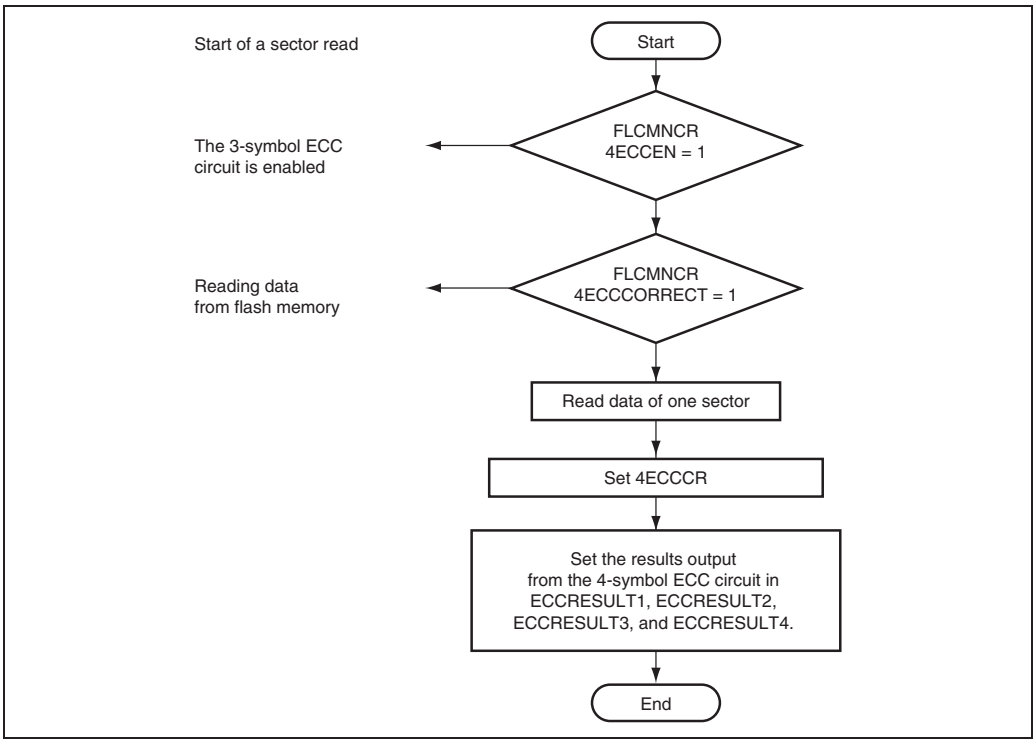


Figure 28.3 4-Symbol ECC Operation Flow

28.4.3 Error Correction Pattern Generation

The 4-symbol ECC circuit contained in this FLCTL can generate error correction patterns using hardware. Correction patterns allow data to be restored to the original correct values. Hardware can only generate error correction patterns. The data should be restored using software.

Error correction patterns are output in the following formats. Since the error bit is set to 1, the restoration data is EOR of the error data and error correction pattern.

Example 1
Original data: B'00000000
Error data: B'11111111
Correction pattern: B'0011111111 (The upper two bits are unnecessary)
Restoration data: B'00000000
(The error pattern and correction pattern are EORed.)

Example 2
Original data: B'10101010
Error data: B'01010101
Correction pattern: B'0011111111 (The upper two bits are unnecessary)
Restoration data: B'10101010
(The error pattern and correction pattern are EORed.)

Example 3
Original data: B'11110000
Error data: B'00000000
Correction pattern: B'0011110000 (The upper two bits are unnecessary)
Restoration data: B'11110000
(The error pattern and correction pattern are EORed.)

28.4.4 Flow when an ECC Error Occurs

figure 28.4 and figure 28.5 shows the flow when an ECC error occurs (when using 4-symbol ECC).

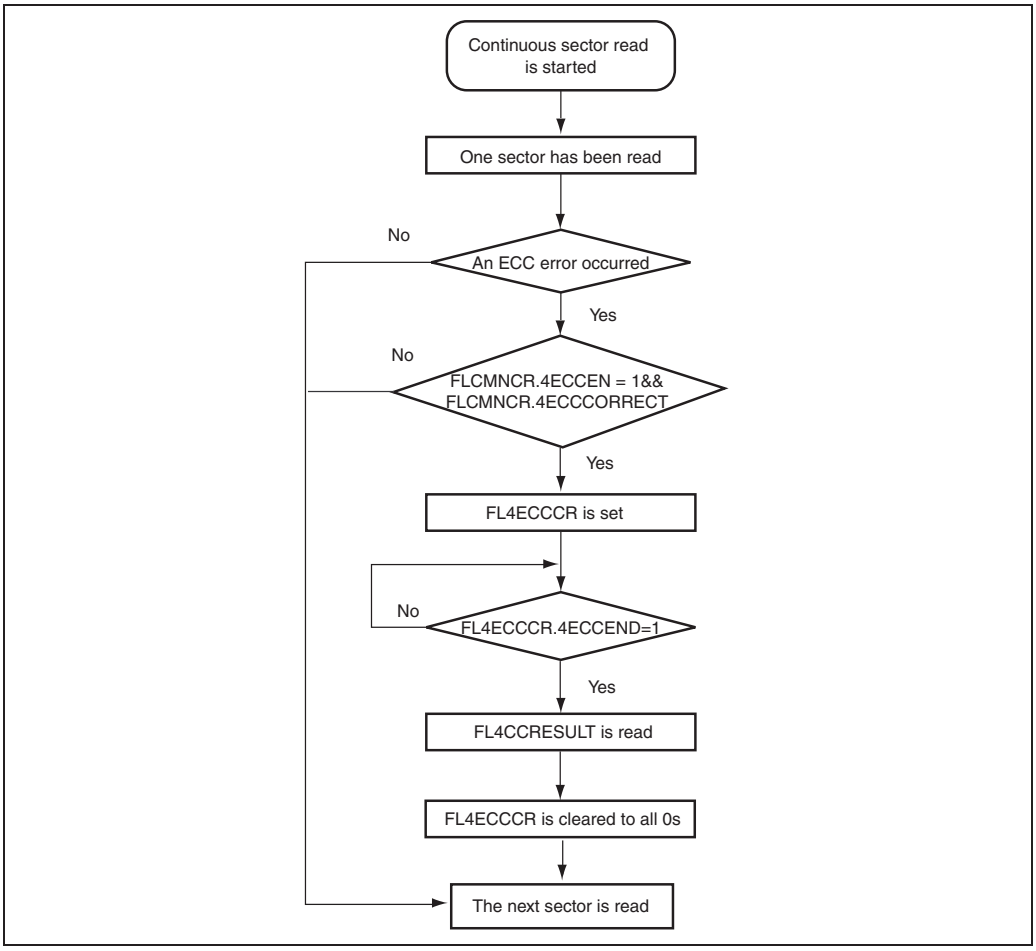


Figure 28.4 Flow when an ECC Error Occurs

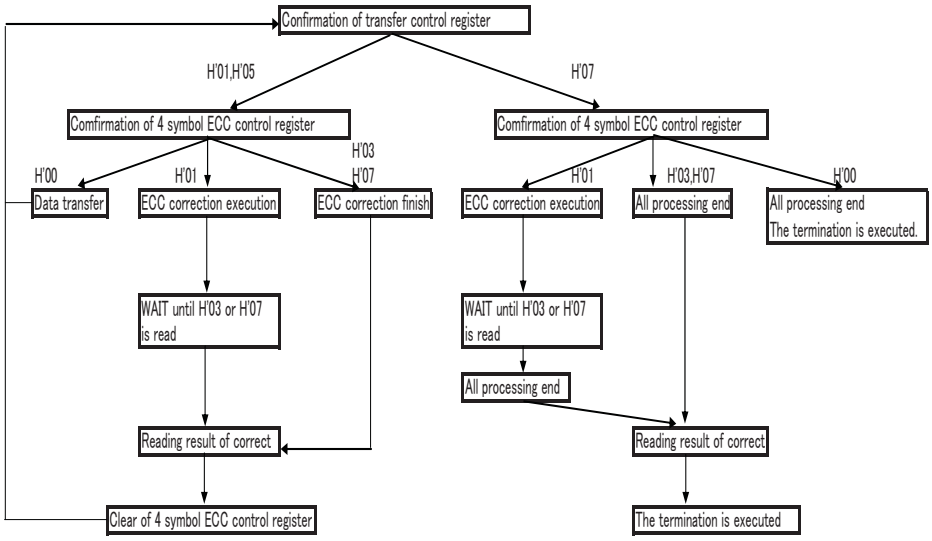


Figure 28.5 process end flow When ECC Error Occurs

28.5 Connection with 16-bit I/O Products

16-bit I/O flash memory can be connected by setting the 16BITSEL bit in FLCMNCR to 1. Set the NANDWF bit in FLCMNCR to 1 when connecting to a 16-bit I/O product.

The basic internal operation of FLCTL is the same as when connecting an 8-bit I/O product. The interface section of FLCTL performs 8- to 16-bit conversion and 16- to 8-bit conversion, and is connected to flash memory as shown in figure 28.6. Figure 28.7 shows an example when using FLDTFIFO with the ENDIAN bit in FLCMNCR set to 0.

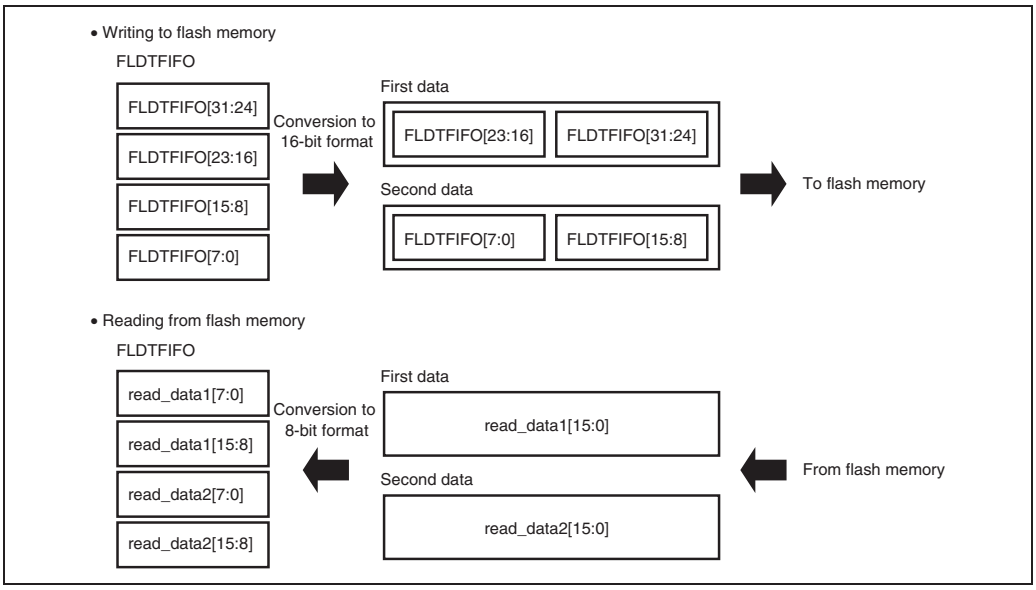


Figure 28.6 Connection with 16-bit I/O Flash Memory

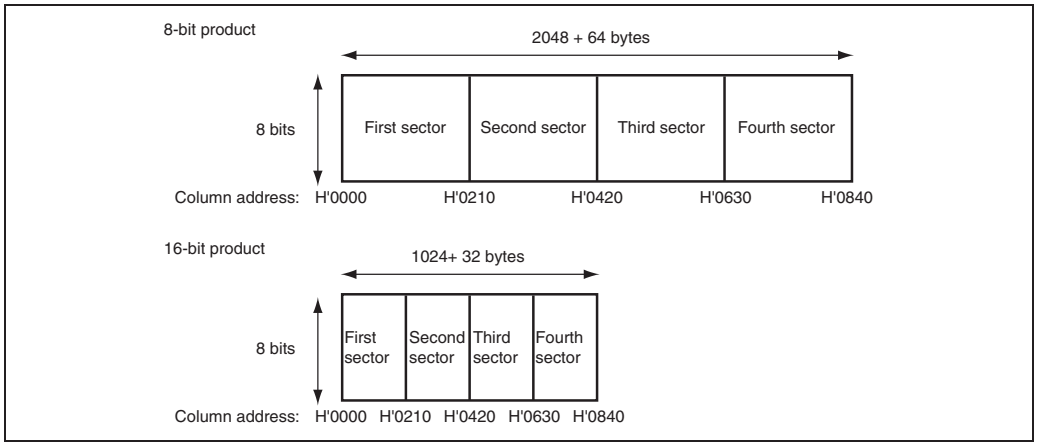


Figure 28.7 Data Allocation

28.6 Operation

28.6.1 Operating Modes

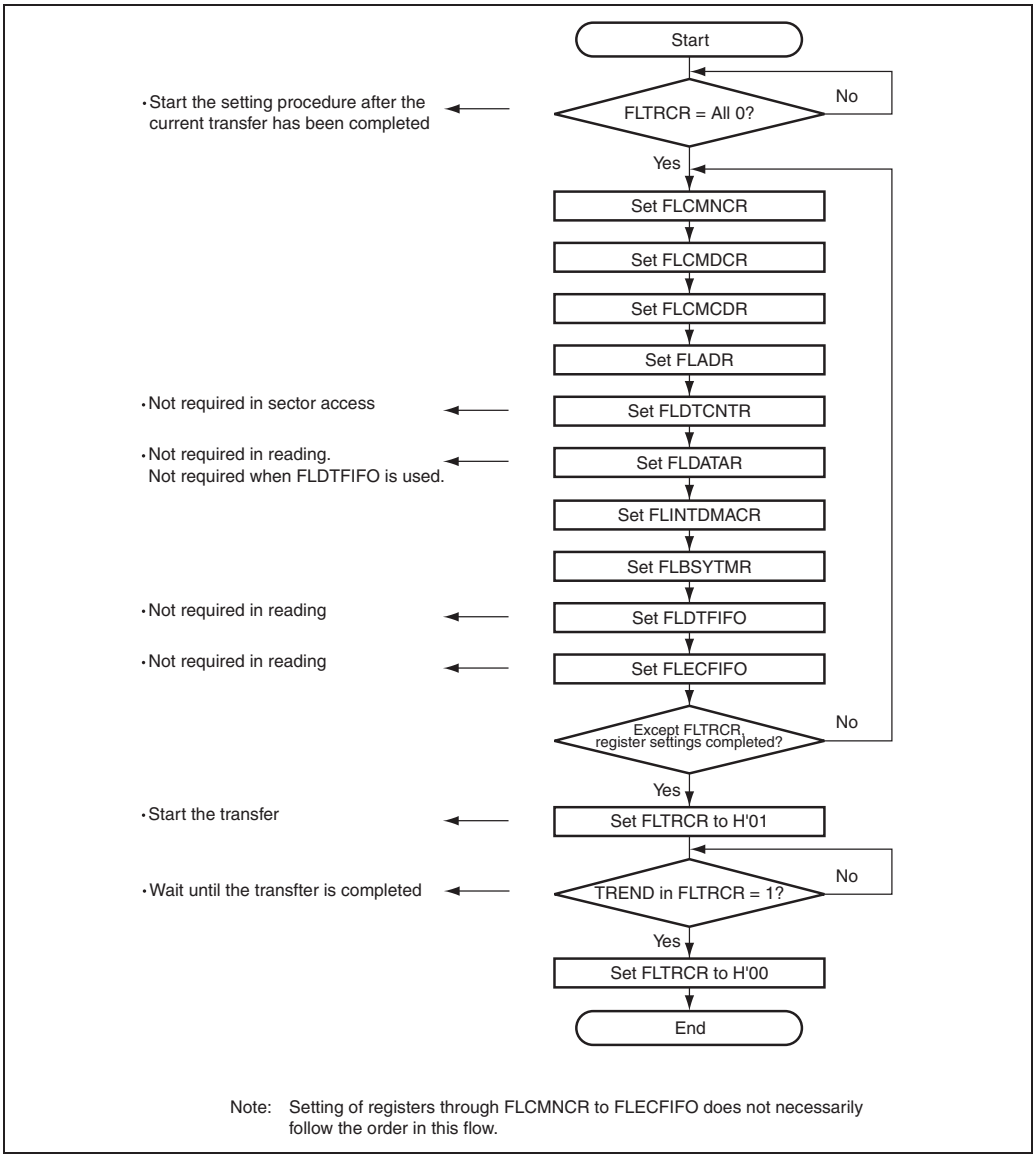
Two operating modes are supported.

- Command access mode
- Sector access mode

The ECC generation and error check are performed in sector access mode.

28.6.2 Register Setting Procedure

Figure 28.8 shows the register setting flow required for accessing to the flash memory.



Note: Setting of registers through FLCMNCR to FLECFIFO does not necessarily follow the order in this flow.

Figure 28.8 Register Setting Flow

28.6.3 Command Access Mode

Command access mode accesses flash memory by specifying a command to be issued to flash memory, address, data, read or write direction, and number of times to the registers. In this mode, I/O data can be transferred by the DMA via FLDTFIFO.

(1) NAND-Type Flash Memory Access

Figure 28.9 shows an example of read operation for NAND-type flash memory. In this example, the first command is specified as H'00, address data length is specified as 3 bytes, and the number of read bytes is specified as 8 bytes in the data counter.

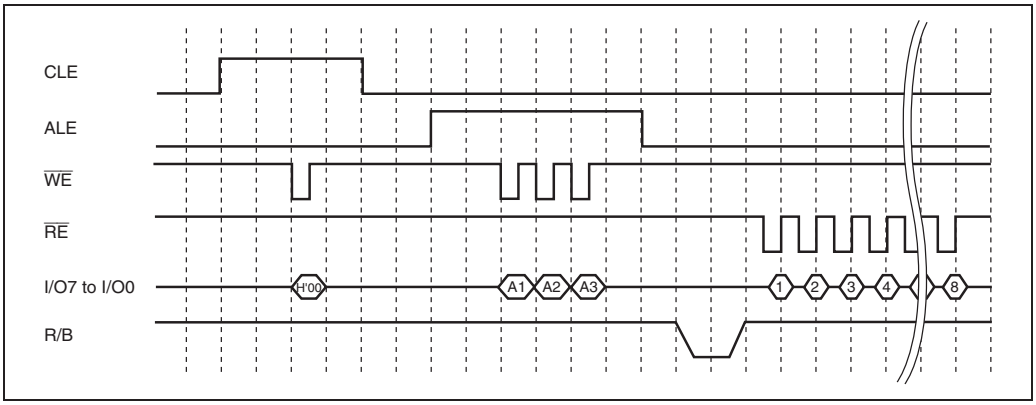


Figure 28.9 Read Operation Timing for NAND-Type Flash Memory (1)

Figures 28.9 and 28.10 show examples of programming operation for NAND-type flash memory.

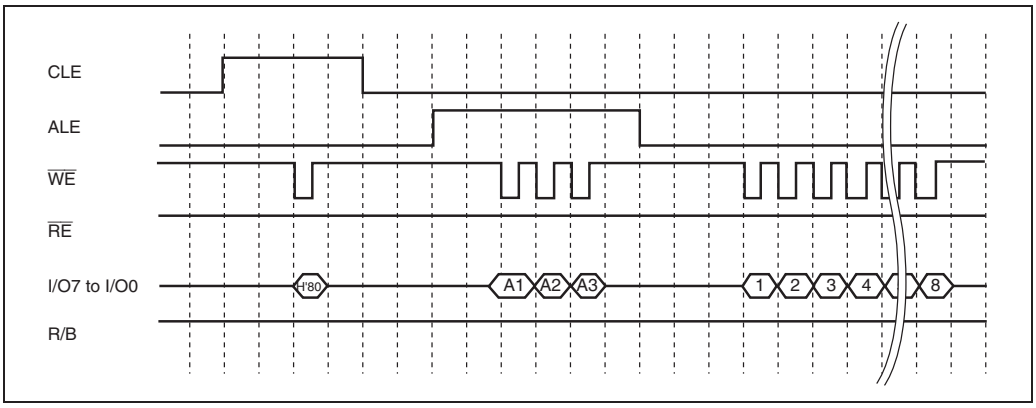


Figure 28.10 Programming Operation Timing for NAND-Type Flash Memory (1)

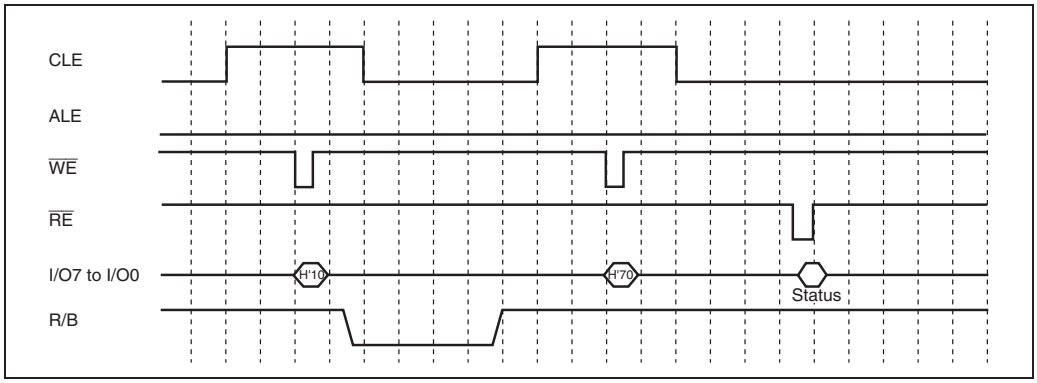


Figure 28.11 Programming Operation Timing for NAND-Type Flash Memory (2)

(2) NAND-Type Flash Memory (2048 + 64 Bytes) Access

Figure 28.12 shows an example of read operation for NAND-type flash memory (2048 + 64 bytes). In this example, the first command is specified as H'00, the second command is specified as H'30, and address data length is specified as 4 bytes. The number of read bytes is specified as 4 bytes in the data counter.

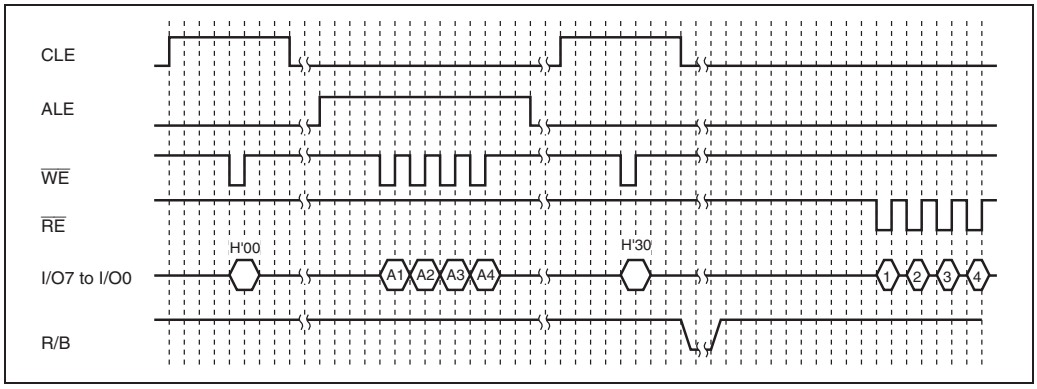


Figure 28.12 Read Operation Timing for NAND-Type Flash Memory

Figures 28.13 and 28.14 show examples of programming operation for NAND-type flash memory (2048 + 64 bytes).

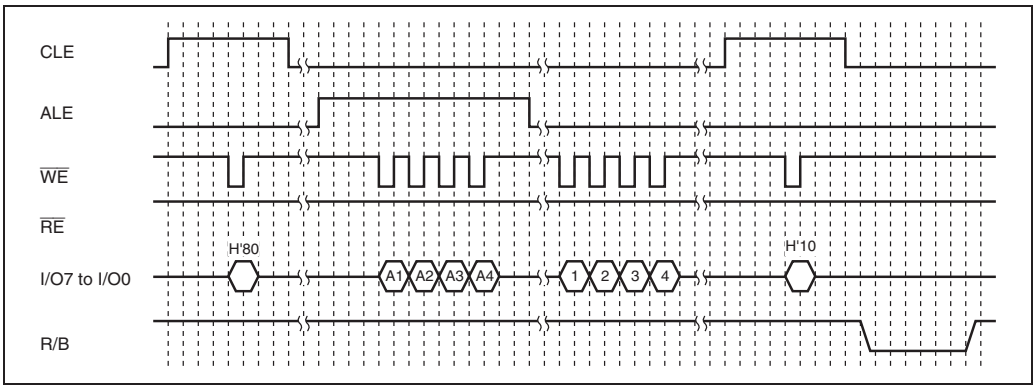


Figure 28.13 Programming Operation Timing for NAND-Type Flash Memory (1)

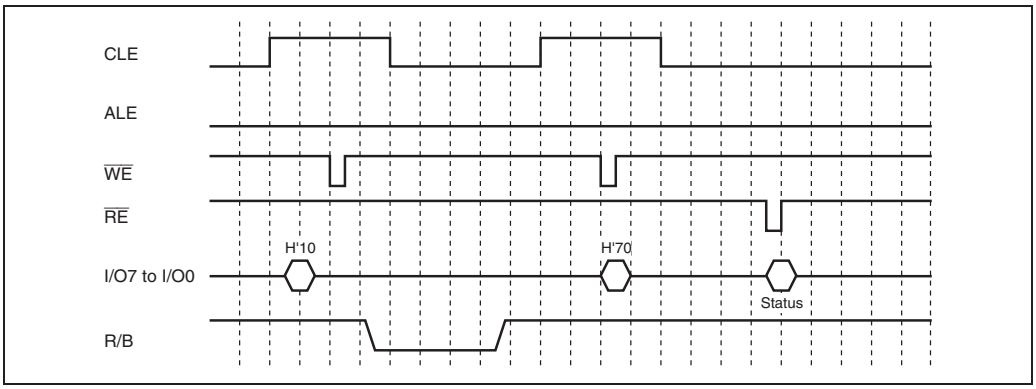


Figure 28.14 Programming Operation Timing for NAND-Type Flash Memory (2)

28.6.4 Sector Access Mode

In sector access mode, flash memory can be read or programmed in sector units by specifying the number of physical sectors to be accessed. In programming, an ECC is added. In read, an ECC error check (detection) is performed.

Since 512-byte data is stored in FLDTFIFO and 16-byte control code is stored in FLECFIFO, the DREQ1EN and DREQ0EN bits in FLINTDMACR can be set to transfer by the DMA.

Figure 28.15 and 28.16 shows the relationship of DMA transfer between sectors in flash memory (data and control code) and memory on the address space.

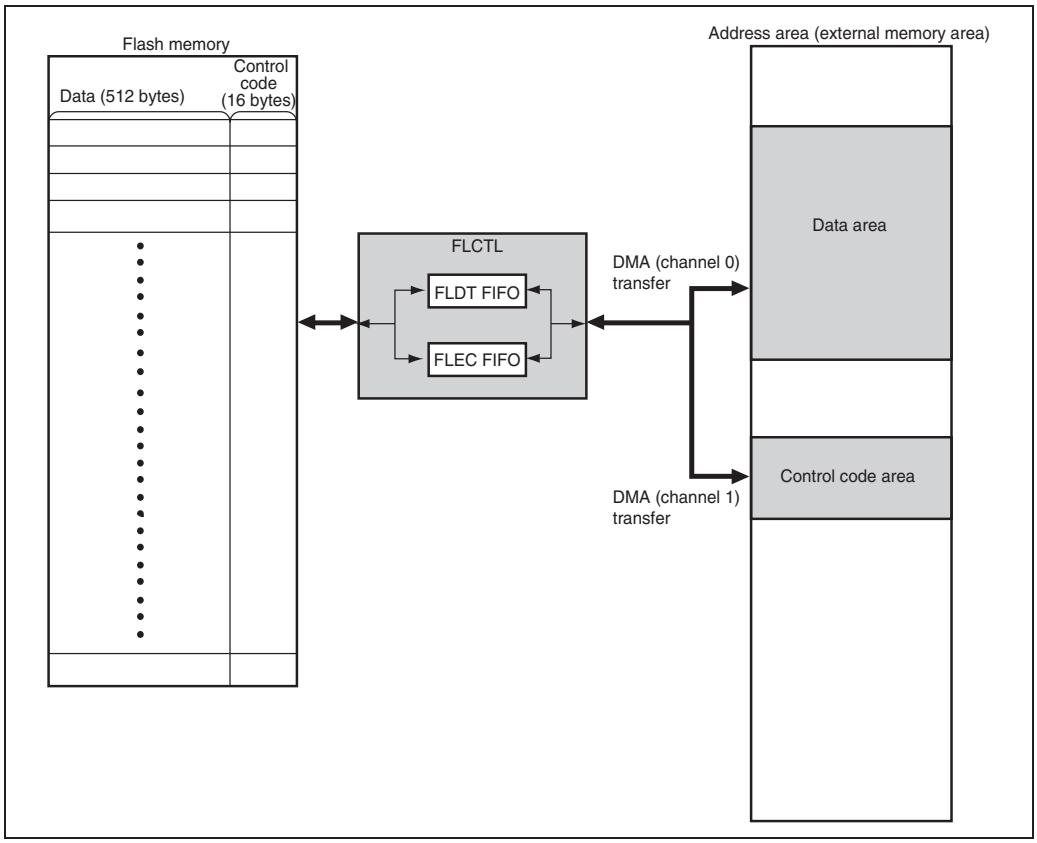


Figure 28.15 Relationship between DMA Transfer and Sector (Data and Control Code), and Memory and DMA Transfer

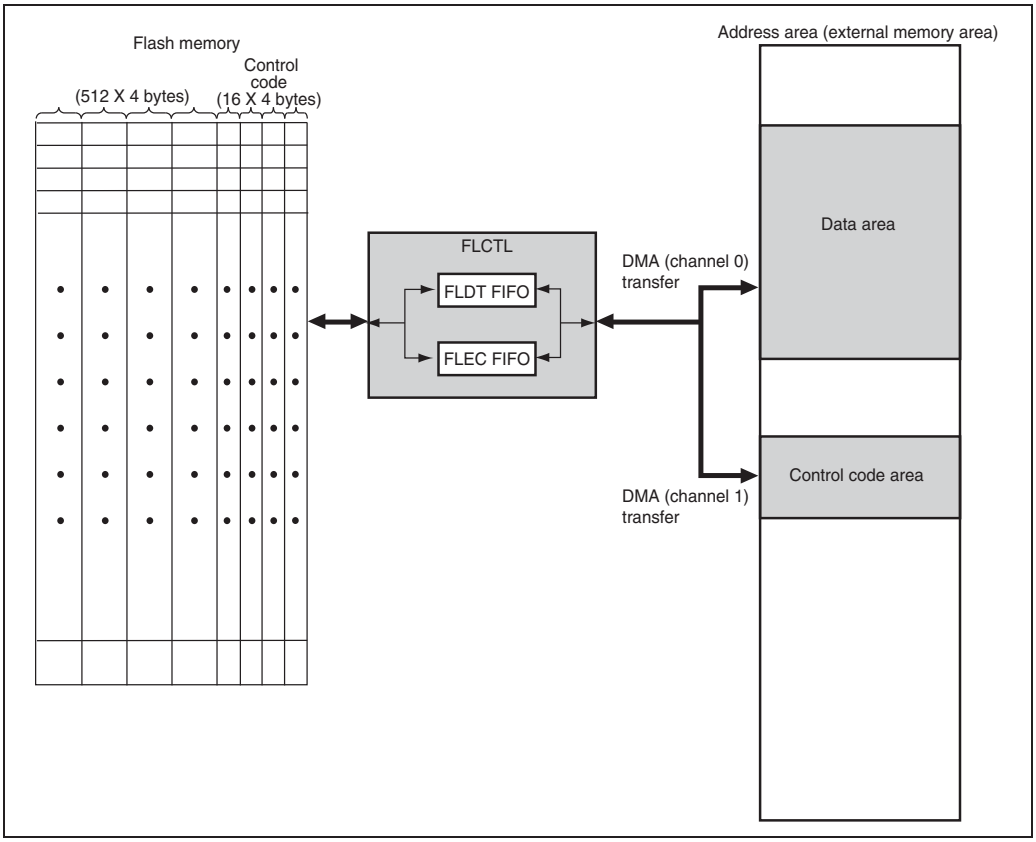


Figure 28.16 Relationship between DMA Transfer and Sector (Data and Control Code), and Memory and DMA Transfer

(1) Physical Sector

Figure 28.17 shows the relationship between the physical sector address of NAND-type flash memory and the address of flash memory.

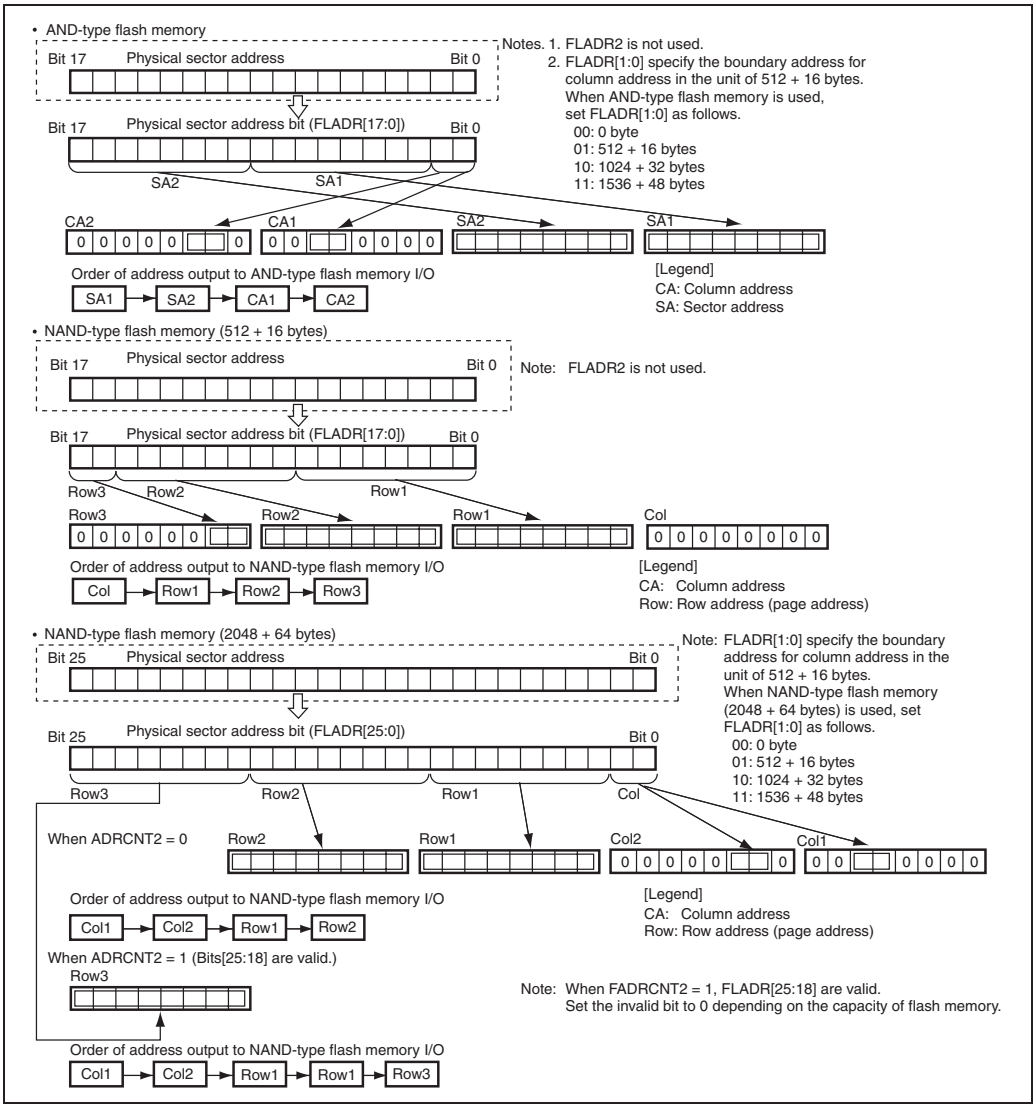


Figure 28.17 Relationship between Sector Number and Address Expansion of NAND-Type Flash Memory (1)

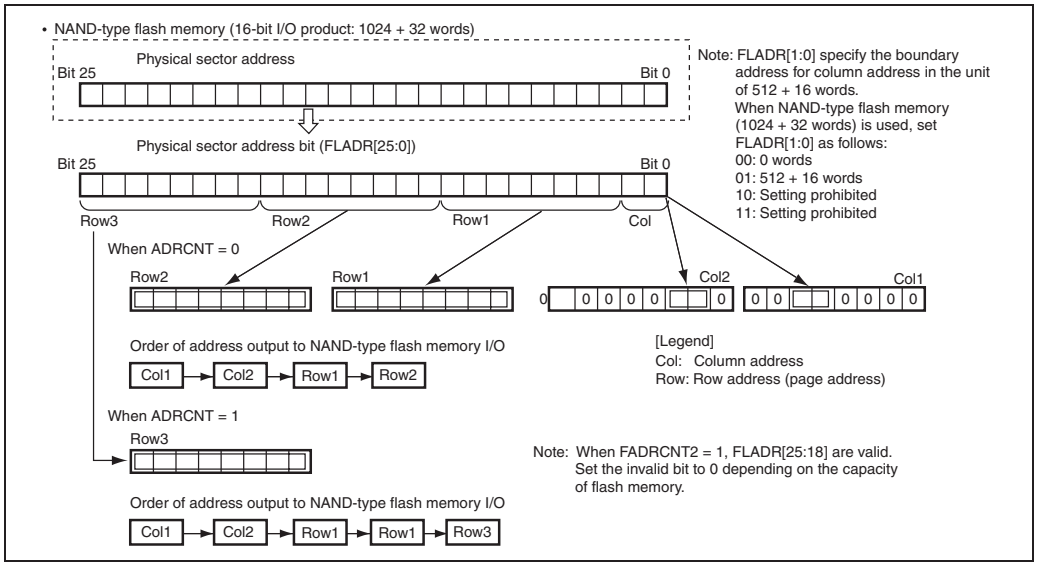


Figure 28.18 Relationship between Sector Number and Address Expansion of NAND-Type Flash Memory (2)

(2) Continuous Sector Access

Continuous physical sectors can be read or written by specifying the start physical sector of NAND-type flash memory and the number of sectors to be transferred. Figure 28.19 shows an example of physical sector specification register and transfer count specification register settings when transferring logical sectors 0 to 40, which are not contiguous because of an unusable sector in NAND-type flash memory.

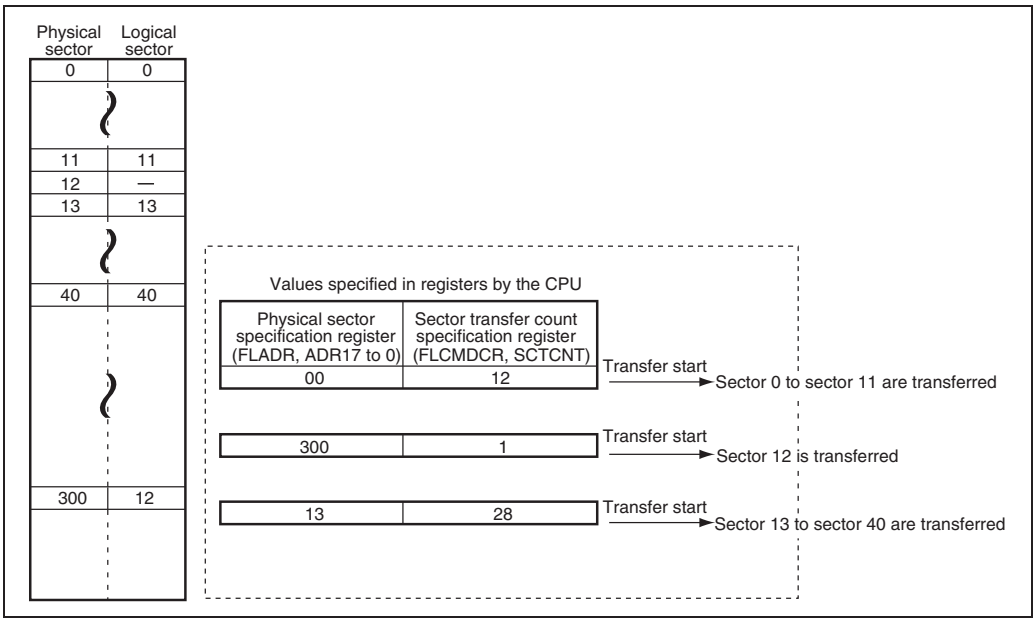


Figure 28.19 Sector Access when Unusable Sector Exists in Continuous Sectors

(3) Flash Memory Access In Sector Access Mode

Figures 28.20 and 28.21 show the waveforms when performing a programming and read operation to NAND-type flash memory in sector access mode.

Figure 28.20 shows the waveform when programming a large-block product whose IO size is 8 bits and memory size is 1 Gbits. A value is programmed into the flash memory in the waveform shown in figure 28.20 for each page (2048 + 64 bytes).

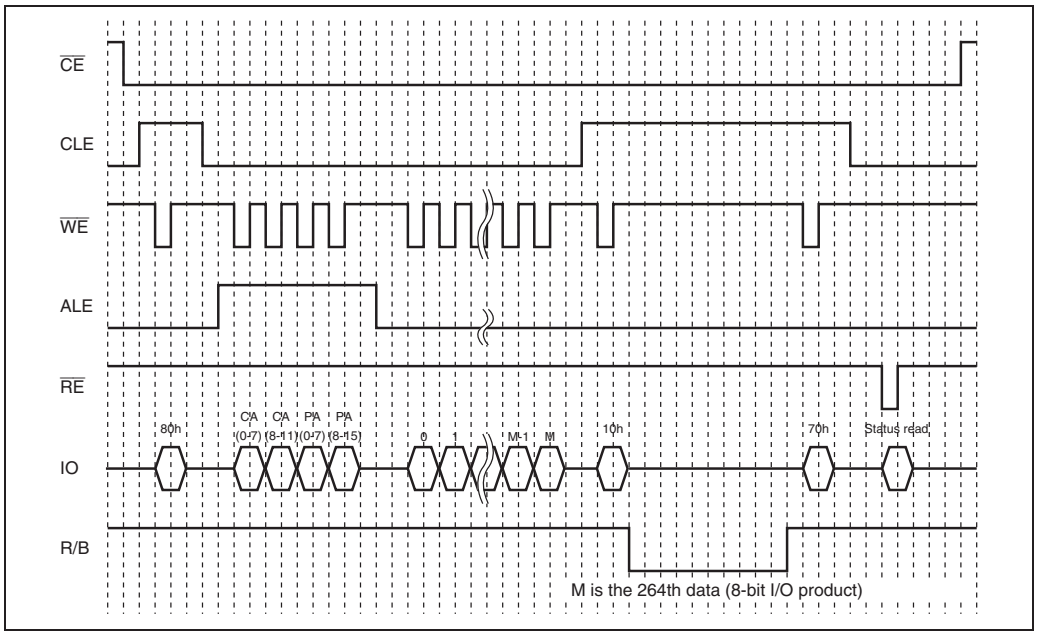


Figure28.20 Programming Operation Timing for NAND-Type Flash Memory (Sector Access Mode)

Figure 28.21 shows the waveform when programming a large-block product whose IO size is 8 bits and memory size is 1 Gbits. A value is programmed into the flash memory in the waveform shown in figure 28.21 for each page (2048 + 64 bytes).

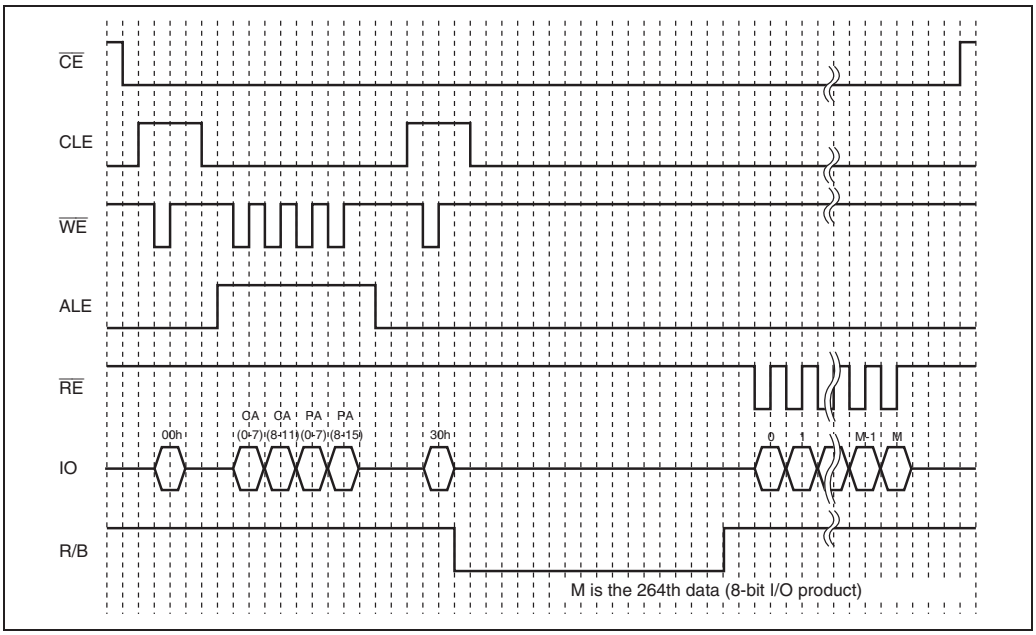


Figure 28.21 Read Operation Timing for NAND-Type Flash Memory (Sector Access Mode)

(4) Flash Memory Access in High-Speed Sector Access Mode

Figures 28.22 to 28.25 show the waveforms when performing a programming and read operation to NAND-type flash memory in high-speed sector access mode. Note that some products do not support high-speed access mode depending on the connected flash memory.

Figures 28.22 and 28.23 show the waveforms when programming in high-speed access mode a large-block product whose IO size is 8 bits and memory size is 1 Gbits. High-speed access mode shortens the busy period.

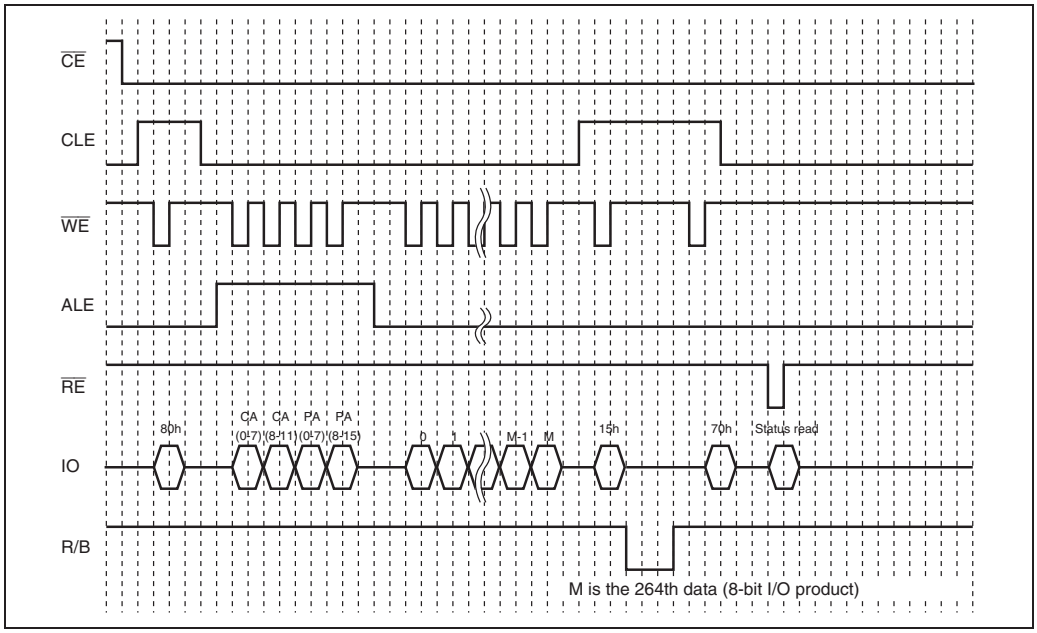


Figure28.22 Programming Operation Timing for NAND-Type Flash Memory (1) (High-speed Sector Access Mode)

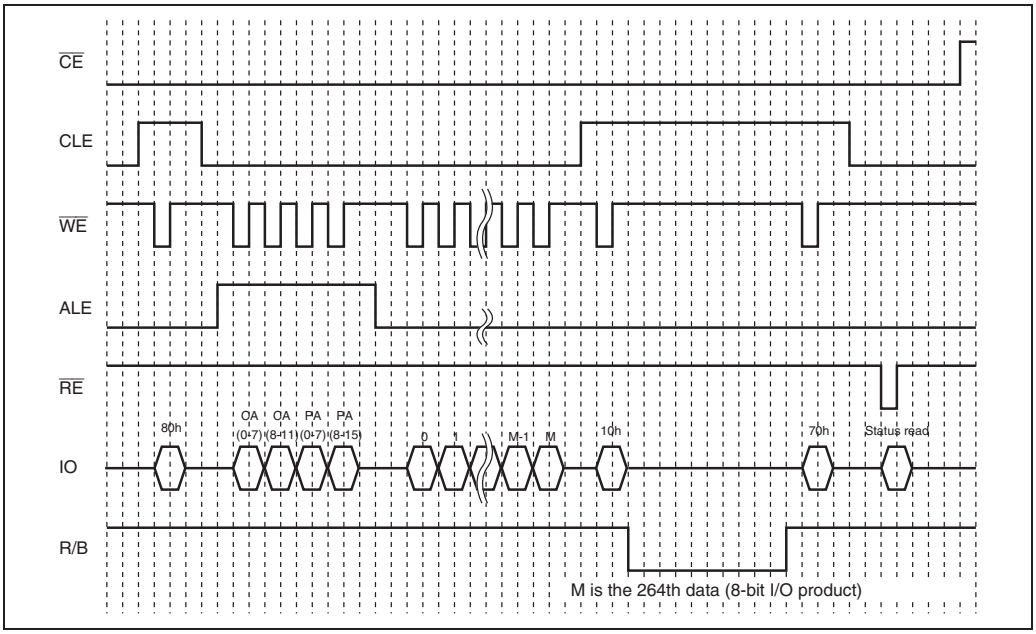


Figure28.23 Programming Operation Timing for NAND-Type Flash Memory (2) (High-speed Sector Access Mode)

Figures 28.24 and 28.25 show the waveforms when reading in high-speed access mode a large-block product whose IO size is 8 bits and memory size is 1 Gbits. High-speed access mode shortens the busy period.

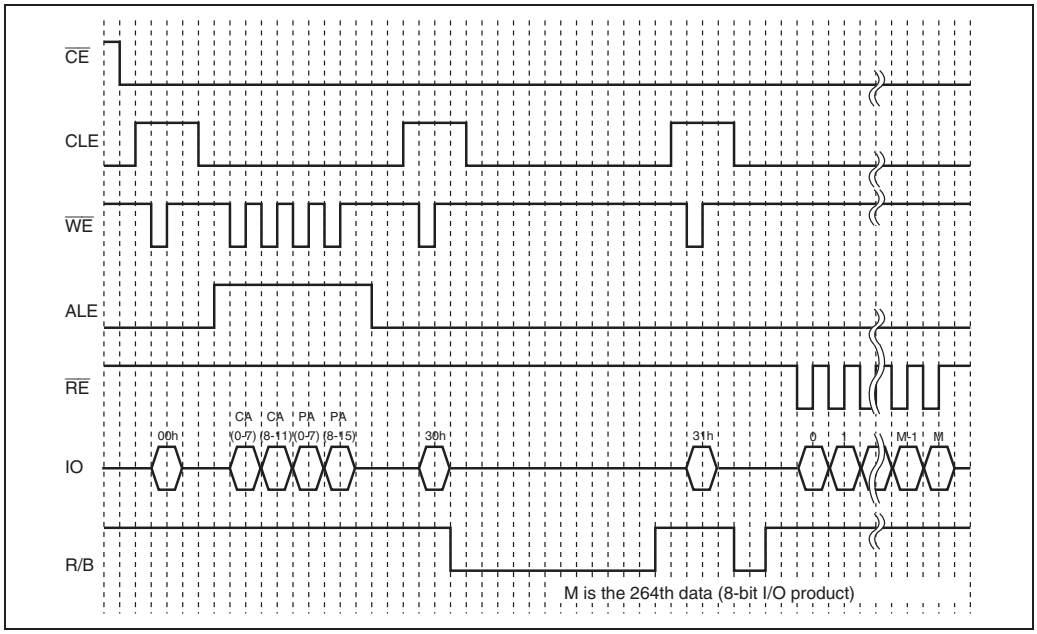


Figure 28.24 Read Operation Timing for NAND-Type Flash Memory (1) (High-speed Sector Access Mode)

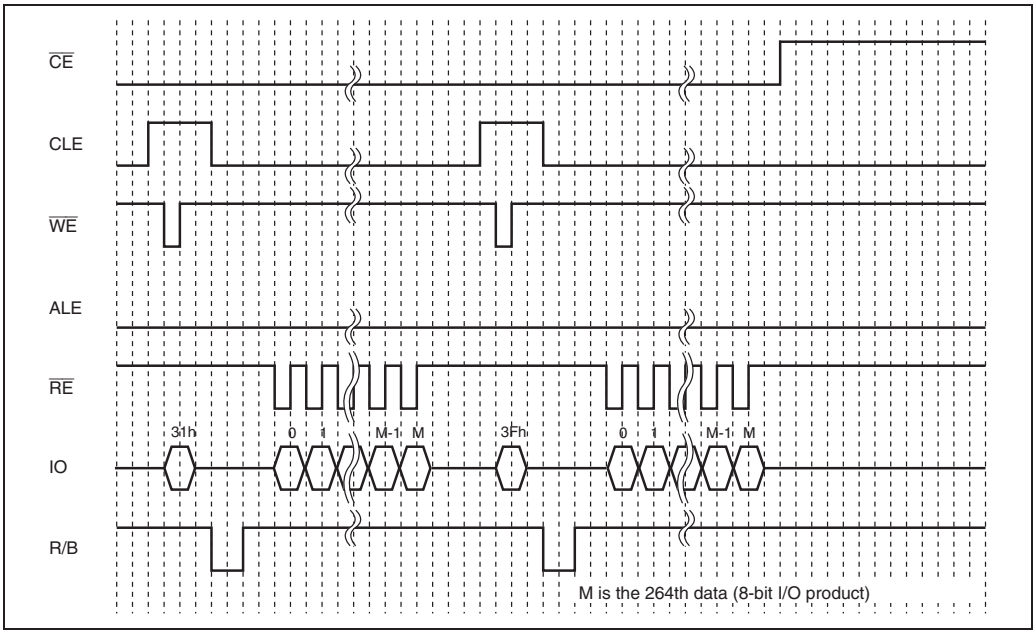


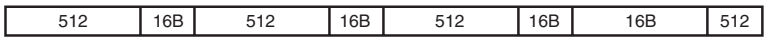
Figure28.25 Read Operation Timing for NAND-Type Flash Memory (2) (High-speed Sector Access Mode)

(5) Large-block Memory Access

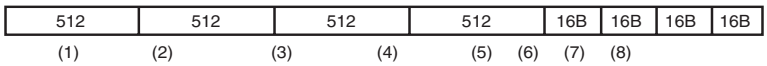
FLCTL accesses large-block memory (2048 + 64 bytes per page) in two ways.

The FLMLC bit (bit 26) in the common control register can be used to switch the access method. The figures below show the data array in flash memory at each access.

a) When FLMLC=0



b) When FLMLC=1



When FLMLC=1, memory is accessed in the following sequence by changing the column address:

1. Access the first sector (sector (1) in the figure above)
2. Change the column address (change the address to control code area (5) in the figure above)
3. Access the control code area (area (5) in the figure above)
4. Change the column address (change the address to second sector (2) in the figure above)
5. Access the second sector (sector (2) in the figure above)
6. Change the column address (change the address to control code area (6) in the figure above)
7. Access the control code area (area (6) in the figure above)
8. Change the column address (change the address to third sector (3) in the figure above)
9. Access the third sector (sector (3) in the figure above)
10. Change the column address (change the address to control code area (7) in the figure above)
11. Access the control code area (area (7) in the figure above)
12. Change the column address (change the address to fourth sector (4) in the figure above)
13. Access the fourth sector (sector (4) in the figure above)

14. Change the column address (change the address to control code area (8) in the figure above)

15. Access the control code area (area (8) in the figure above)

28.6.5 ECC Error Correction

When using the 3-symbol ECC circuit, the FLCTL generates and adds an ECC code during write operation in sector access mode and performs ECC error check during read operation in sector access mode. The FLCTL, however, does not perform error correction. Note that errors must be corrected by software.

When using the 4-symbol ECC circuit, the FLCTL generates and adds an ECC code during write operation in sector access mode, and performs ECC error check during read operation in sector access mode and outputs error correction patterns. The FLCTL, however, does not replace error data. Note that error data must be replaced by software.

28.6.6 Status Read

The FLCTL can read the status register of an NAND-type flash memory. The data in the status register of an NAND-type flash memory is input through the I/O7 to I/O0 pins and stored in the STAT7 to STAT70 bits in FLBSYCNT. The STAT7 to STAT70 bits in FLBSYCNT can be read by the CPU. If a program error or erase error is detected when the status register value is stored in the STAT7 to STAT70 bits in FLBSYCNT, the STERB bit in FLINTDMACR is set to 1 and generates an interrupt to the CPU if the STERINTE bit in FLINTDMACR is enabled.

(1) Status Read of NAND-Type Flash Memory

The status register of NAND-type flash memory can be read by inputting command H'70 to NAND-type flash memory. If programming is executed in command access mode or sector access mode while the DOSR bit in FLCMDCR is set to 1, the FLCTL automatically inputs command H'70 to NAND-type flash memory and reads the status register of NAND-type flash memory. When the status register of NAND-type flash memory is read, the I/O7 to I/O0 pins indicate the following information as described in table 28.4.

Table 28.4 Status Read of NAND-Type Flash Memory

I/O	Status (definition)	Description
I/O7	Program protection	0: Cannot be programmed 1: Can be programmed
I/O6	Ready/busy	0: Busy state 1: Ready state
I/O5 to I/O1	Reserved	—
I/O0	Program/erase	0: Pass 1: Fail

28.7 Interrupt Sources

The FLCTL has six interrupt sources: Status error, ready/busy timeout error, ECC error, transfer end, FIFO0 transfer request, and FIFO1 transfer request. Each of the interrupt sources has its corresponding interrupt flag and the interrupt can be requested independently to the CPU if the interrupt is enabled by the interrupt enable bit. Note that the status error, ready/busy timeout error, and ECC error use the common FLSTE interrupt to the CPU.

Table 28.6 FLCTL Interrupt Requests

Interrupt Source	Interrupt Flag	Enable Bit	Description	Priority
FLSTE interrupt	STERB	STERINTE	Status error	Highest
	BTOERB	RBERINTE	Ready/busy timeout error	
	ECERB	ECERINTE	ECC error	
FLTEND interrupt	TREND	TEINTE	Transfer end	
FLTRQ0 interrupt	TRREQF0	TRINTE0	FIFO0 transfer request	
FLTRQ1 interrupt	TRREQF1	TRINTE1	FIFO1 transfer request	Lowest

Note: Flags for the FIFO0 overrun error/underrun error and FIFO1 overrun error/underrun error also exist. However, no interrupt is requested to the CPU.

28.8 DMA Transfer Specifications

The FLCTL can request DMA transfers separately to the data area FLDTFIFO and control code area FLECFIFO. Table 28.7 summarizes DMA transfer enable or disable states in each access mode.

Table 28.7 DMA Transfer Specifications

	Sector Access Mode	Command Access Mode
FLDTFIFO	DMA transfer enabled	DMA transfer enabled
FLECFIFO	DMA transfer enabled	DMA transfer disabled

In little endian form, these bits should not be used because a 16-byte DMA transfer causes a data replacement in longword units.

Usage Notes

(1) Usage Notes on the BUSYON Bit

The FLCTL negates $\overline{CE}$ when finishing a sequence of operations whether it is busy or ready. Note that $\overline{CE}$ is negated and the bus mastership is released at the same time as FLCTL processing is completed even during a busy period when bit 21 (BUSYON) in the common control register (FLCMNCR) is set to 0. When BUSYON = 0, the bus mastership can be obtained even during the busy period by setting bit 24 (DOSR) in the command control register (FLCMDCR) to 1 and executing a status read.

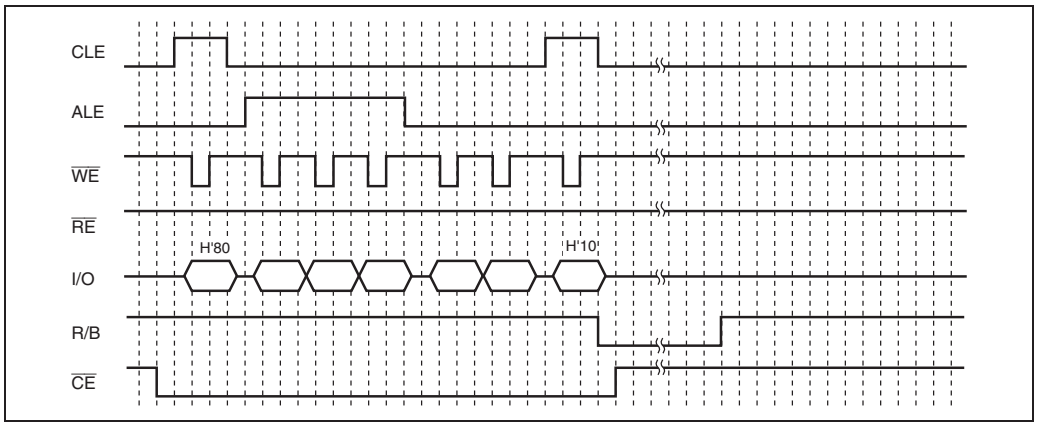


Figure28.26 BUSYON = 0 and DOSR = 0 (Programming to Flash Memory)

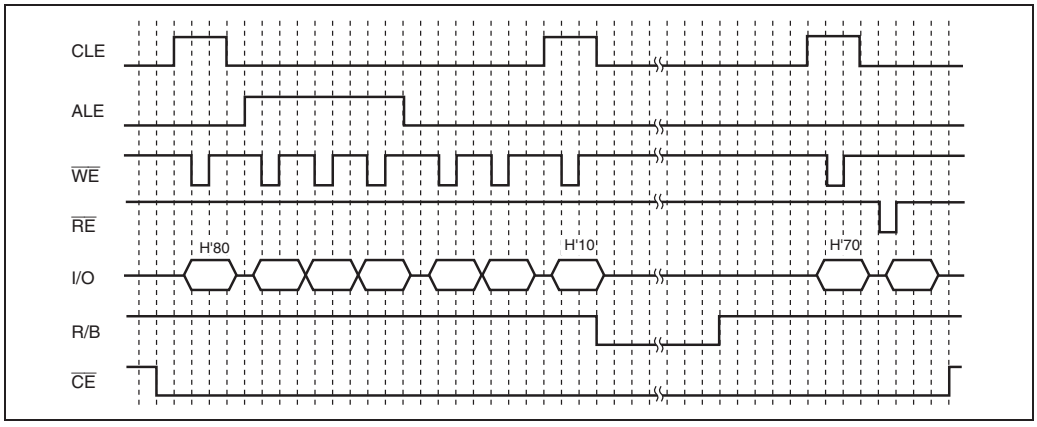


Figure28.27 BUSYON = 0 and DOSR = 1 (Programming to Flash Memory)

(2) Usage Notes on the SNAND Bit

When the SNAND bit of the common control register (FLCMNCR) is set to 1, only the first and second commands are supported regardless of the settings of DOCMD1 and DOCMD2 of the command control register (FLCMDCR).

Set the SNAND bit to 0 when no command is issued or only the first command is issued.

Section 29 Multifunctional Interface (MFI)

The multifunctional interface (MFI) incorporated in this LSI consists of the MFIM, which has an interface of the on-chip ROM, and the MFIS, which has an interface between the SYS domain and the realtime domain (RT domain).

The MFIM allows reading from the on-chip ROM space (MMFROM) for the MFIM, in 32-bit units. The MMFROM is accessible from the SYS domain.

From the SYS domain, the MFIS allows reading from and writing to the on-chip RAM space (SMFRAM) for the MFIS in 32-bit units. The SMFRAM is accessible from both the SYS domain and the RT domain. The MFIS also supports the issuing of interrupts by the SYS domain for the RT domain and interrupts by the RT domain for the SYS domain. The SMFRAM along with these interrupt functions allows software-like data transfer between the SYS domain and the RT domain.

29.1 Features of the MFIM

- The MMFROM space can be read from in 32-bit units.

Figure 29.1 shows a block diagram of the MFIM.

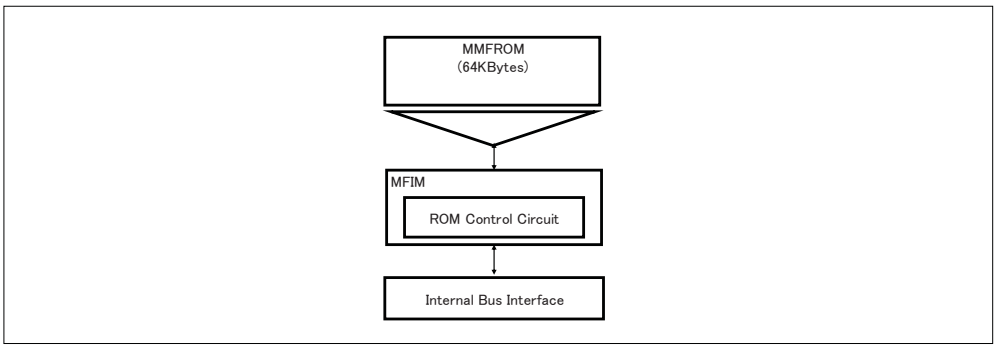


Figure 29.1 MFIM Block Diagram

29.2 Register Descriptions

Table 29.1 shows the MFIM register configuration.

Table 29.1 Register Configuration

Register Name	Abbreviation	R/W	Address	Access Size
MMFROM	MMFROM	R	H'E6B0 0000 to H'E6B0 FFFF	32, 16, 8

29.3 Features of the MFIS

- Provides for reading from and writing to the SMFRAM in 32-bit units.
- Automatic address incrementation and selectable endian.
- By writing to specific bits of the internal registers of the MFIS from the SYS domain, interrupts can be sent to the RT domain. Conversely, interrupts can also be sent from the RT domain to the SYS domain.
- Two seven-bit interrupt sources are provided, one for the BB domain and the other for the SYS domain. As a result, 128 different interrupts can be controlled by software, enabling high-speed data transfer using interrupts.

Figure 29.7 shows a block diagram of the MFIS.

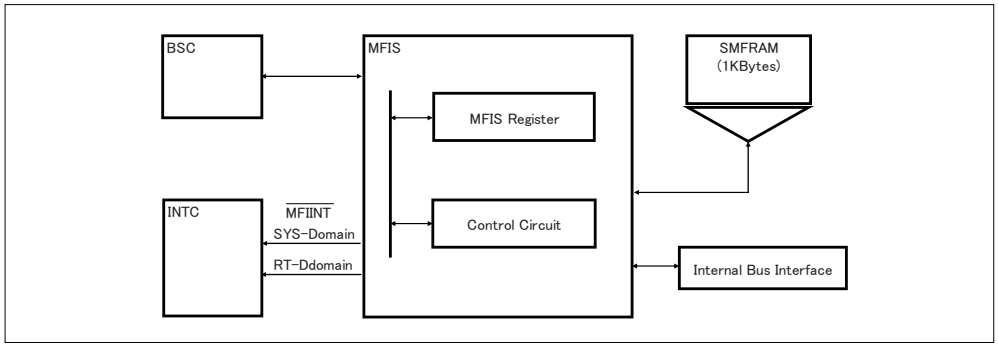


Figure 29.7 MFIS Block Diagram

29.4 Register Descriptions of MFIS

Table 29.5 shows the MFI register configuration. Table 29.6 shows the register states in each operating mode.

Table 29.5 Register Configuration

Register Name	Abbreviation	R/W	Address	Access Size
MFIS index register	MFISIDX	R/W	H'E6A6 0000	32
MFIS general status register	MFISGSR	R/W	H'E6A6 0004	32
MFIS status/control register	MFISSCR	R/W	H'E6A6 0008	32
MFIS memory control register	MFISMCR	R/W	H'E6A6 000C	32
MFIS internal interrupt control register	MFISIICR	R/W	H'E6A6 0010	32
MFIS external interrupt control register	MFISEICR	R/W	H'E6A6 0014	32
MFIS address register	MFISADR	R/W	H'E6A6 0018	32
MFIS data register	MFISDATA	R/W	H'E6A6 001C	32
MFIS semaphore register	MFISSM4	R/W	H'E6A6 0080	32
SMFRAM	SMFRAM	R/W	H'E6A7 0000 to H'E6A7 03FF	32, 16, 8

Table 29.6 Register States in Each Operating Mode

Register Abbreviation	Reset *1	Software Reset	A4S Area Reset	Module Standby
MFISIDX	Initialized	Initialized	Initialized	Retained
MFISGSR	Initialized	Initialized	Retained	Retained
MFISSCR	Initialized	Initialized	Retained	Retained
MFISMCR	Initialized	Initialized	Initialized	Retained
MFISIICR	Initialized	Initialized	Retained	Retained
MFISEICR(*2)	Initialized	Initialized	Retained	Retained
MFISADR	Initialized	Initialized	Initialized	Retained
MFISDATA	Initialized	Initialized	Retained	Retained
MFISSM4	Initialized	Initialized	Retained	Retained
SMFRAM	Undefined	Retained	Retained	Retained

Note: *1 For details, refer to section 1-D Overview of reset.
Note: *2 The bit RSTEND in MFISEICR is off the subject of retained.

29.4.1 MFIS Index Register (MFISIDX)

MFISIDX is a 32-bit register used to specify the register for reading from and writing to the MFI with the second bit (A2) in the address of the bus state controller (BSC) held 0. From the MFI, this register can only be written while the A2 is set to 1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	REG[5:0]						BYTE[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 2	REG[5:0]	000000	R/W*	MFIS Internal Register Select 000000: MFISGSR 000001: MFISSCR 000010: MFISMCR 000011: MFISIICR 000100: MFISEICR 000101: MFISADR 000110: MFISDATA 100000: MFISSM4 Settings other than above are prohibited.

Bit	Bit Name	Initial Value	R/W	Description
1, 0	BYTE[1:0]	00	R/W*	Internal Register Byte Specification These bits specify which 16 bits of the 32-bit register are to be accessed. • MFISSCR.BO = 0 00: Register bits 31 to 16 01: Setting prohibited 10: Register bits 15 to 0 11: Setting prohibited • MFISSCR.BO = 1 00: Register bits 15 to 0 01: Setting prohibited 10: Register bits 31 to 16 11: Setting prohibited However, when MFISDATA is selected using bits REG5 to REG0, each time reading or writing of MFISDATA occurs, bits BYTE1 and BYTE0 change according to the following rules. 16-bit bus: 00 → 10 → 00 → 10... repeated

Note: * These bits can only be written via the MFIS, while the A2 pin is held 1. They cannot be written from the peripheral bus of the RT domain.

29.4.2 MFIS General Status Register (MFISGSR)

MFISGSR is a 32-bit register that can be freely used to indicate the mutual states between the SYS domain and the RT domain. This register is read-only from the MFIS when the A2 pin is held 1. When writing to MFISGSR via the MFIS, writing should be performed with MFISGSR specified in bits REG5 to REG0 in MFISIDX, and with the A2 pin held 0. In this state, MFISGSR can also be read.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	STATUS[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	STATUS [7:0]	H'00	R/W	General Status These bits can be read from or written to by the software or on-chip CPU in the SYS domain. Except upon a reset, they are never overwritten by hardware.

29.4.3 MFIS Status/Control Register (MFISSCR)

MFISSCR is a 32-bit readable/writable register used to control the MFIS mode and state.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EDN	BO
Initial value:	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
5 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	EDN	0	R/W	Endian (for MFRAM access) Specifies the byte positions when accessing the MFRAM from the on-chip CPU. 0: Big endian 1: Little endian
0	BO	0	R/W	Byte Order Specifies the byte position of the MFIS internal registers along with bits MFISIDX1 and MFISIDX0. 0: Big endian (MSB first) 1: Little endian (LSB first)

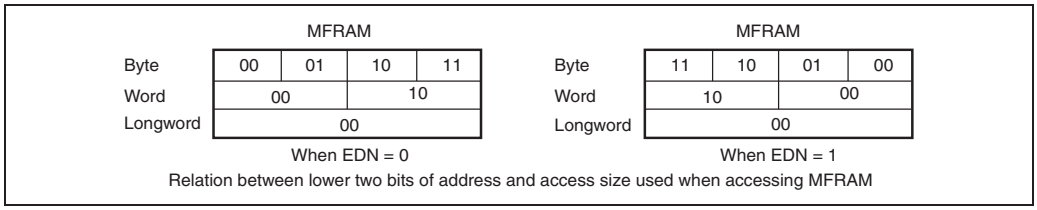


Figure 29.8 Differences in EDN Bit Specifications

29.4.4 MFIS Memory Control Register (MFISMCR)

MFISMCR is a 32-bit register used to control the SMFRAM via the MFIS.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	LOCK	—	WT	—	RD	—	—	AI/AD
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W*1	R	R/W*1	R	R/W*1	R	R	R/W*1

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	LOCK	0	R/W*1	Lock This bit is used to lock read/write operations during continuous access. When 1 is written to the LOCK bit, the values of the RD and WT bits set at that time are held until the LOCK bit is next cleared to 0. By using the LOCK, RD, and WT bits, modes are as follows: LOCK RD WT 1 1 0 : Continuous read mode 1 0 1 : Continuous write mode The RD and WT bits should not both simultaneously be set to 1.

Bit	Bit Name	Initial Value	R/W	Description
6	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
5	WT	0	R/W*[1]	Write When this bit is set to 1, the MFIDATA value is written to the SMFRAM position corresponding to MFISADR.*[2]*[3] If the WT bit and LOCK bit are set to 1 simultaneously, a state of continuous writing to the MFIS is entered, and high-speed data transfer becomes possible. This state is maintained until the WT bit is next cleared to 0, or until the LOCK bit is cleared to 0. If the LOCK bit is not simultaneously set to 1, writing to SMFRAM is performed only once. The value of the WT bit is automatically cleared to 0.
4	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
3	RD	0	R/W*[1]	Read When this bit is set to 1, the SMFRAM data corresponding to MFISADR is read in MFISDATA.*[2]*[3] If the RD bit and LOCK bit are set to 1 simultaneously, a state of continuous reading of the MFIS is entered, and high-speed data transfer becomes possible. This state is maintained until the RD bit is next cleared to 0, or until the LOCK bit is cleared to 0. If the LOCK bit is not simultaneously set to 1, reading of SMFRAM is performed only once. The value of the RD bit is automatically cleared to 0.
2, 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
0	AI/AD	0	R/W*[1]	Address Auto-Increment/Decrement This bit is valid only when the LOCK bit is 1. The value of the MFIADR is automatically incremented by 4 or decremented by 4 according to the setting of this bit each time reading or writing of SMFRAM is performed. 0: Auto-increment mode (+4) 1: Auto-decrement mode (–4)

Notes: 1. This bit can only be written via the MFI. It cannot be written from the peripheral bus of the RT domain.
2. If access of SMFRAM via the BSC and access of SMFRAM from the peripheral bus of the RT domain occur simultaneously, the access via the BSC is executed first.
3. If a single reading or single writing is necessary after continuous reading or continuous writing, it should be performed after the WT bit and RD bit are cleared to 0.

29.4.5 MFIS Internal Interrupt Control Register (MFISIICR)

MFISIICR is used to issue interrupts from the SYS domain to the RT domain.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	IIC[6:0]							IIR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
7 to 1	IIC[6:0]	0000000	R/W	Internal Interrupt Source Bits used to specify the source for interrupts generated by the IIR. These bits can be written from both the BSC and peripheral bus of the RT domain. By using these bits, fast execution of an interrupt handler is possible. These bits are completely under software control, and their values have no effect on the operation of the RT domain.
0	IIR	0	R/W	Internal Interrupt Request While this bit is 1, an interrupt request is issued to the RT domain.

29.4.6 MFIS External Interrupt Control Register (MFISEICR)

MFISEICR is a 32-bit register used to issue interrupts from the RT domain to the SYS domain.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial Value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	RST END	EIC[6:0]							EIR
Initial Value:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	RSTEND	1	R/W	Reset Period End Flag Flag indicating that the reset period has finished. 0: Clears the flag. 1: Retains the previous value.

Bit	Bit Name	Initial Value	R/W	Description
7 to 1	EIC[6:0]	0000000	R/W	External Interrupt Source Bits used to specify the source for interrupts generated by the EIR. These bits can be written from both the BSC and RT domain peripheral bus. By using these bits, fast execution of an interrupt handler is possible. These bits are completely under software control, and their values have no effect on the operation of the RT domain.
0	EIR	0	R/W	External Interrupt Request While this bit is 1, an interrupt request is issued to the SYS domain.

29.4.7 MFIS Address Register (MFISADR)

MFISADR is a 32-bit register that indicates the address in the SMFRAM to be accessed via the BSC.

When using the setting of the LOCK bit in MFISMCR to specify continuous access of the SMFRAM, auto-increment (+4) or auto-decrement (-4) of the address, according to the AI/AD bit setting in MFISMCR, is performed automatically, and the MFISADR is updated. Wrap-around operation is performed if auto-increment or auto-decrement causes an excess of the following valid bits. MFISRCR is writable via the BSC. However, it is read-only and cannot be written from the peripheral bus of the RT domain.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	A[9:2]								—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 2	A[9:2]	H'00	R/W	Address These bits specify the 1-Kbyte memory space of SMFRAM to be accessed via the BSC, with 32-bit boundary.
1, 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

29.4.8 MFIS Data Register (MFISDATA)

MFISDATA is a 32-bit register used to store data for writing to the SMFRAM and data read from the SMFRAM. If MFISDATA is not used when accessing the SMFRAM, it can be used for software data transfer between the SYS domain and the RT domain.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	D[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	D[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	D[31:0]	H'0000 0000	R/W	32-Bit Data

29.4.9 MFIS Semaphore Register (MFISSM4)

MFISSM4 is a dedicated register allowing read modify write to be performed from the SYS domain and from the RT domain. Using MFISSM4 as a semaphore can improve the data transfer efficiency.

In a state where neither the SYS domain nor the RT domain makes a request, MFISSM4 indicates that the bits SM7 and SM6 = B'00. If a request (for read operation to the MFISSM4) from the SYS domain occurs in this state, bits SM7 and SM6 = B'00 is read. Viewing B'00, software can learn the successful acquisition. After this, MFISSM4 changes to the bits SM7 and SM6 = B'01.

Note that any request/access from the SYS domain means an access via the BSC. Any access from the AP-SYS to H’E6A60080 is handled as an access from the RT domain.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	SM[7:6]		INF[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
7, 6	SM[7:6]	00	R/W	Bits for Semaphore If these bits are 00, reading to this register reads B'01 (read from the SYS domain) or B'10 (read from the RT domain). The read value means a value before the change. The change is made only when B'00 is read. 00: Only reading from both the SYS domain and the RT domain is possible. 01: Reading/writing from the SYS domain is possible, and only reading is possible from the RT domain. 10: Only reading is possible from the SYS domain, reading/writing from the RT domain is possible. 11: Setting prohibited.
5 to 0	INF[5:0]	000000	R/W	Reading/writing is allowed according to the semaphore conditions of bits SM7 and SM6. These bits are usually used as information.

Note: If reading from the SYS domain and the RT domain simultaneously occurs for MFISSM4 with the bits SM7 and SM6, = B'00, MFISSM4 returns data of the bits SM7 and SM6 = B'01 to the AP domain, while returns B'00 to the SYS domain.

29.5 Access to MFIS Registers

The MFIS register can be accessed from the SYS domain by accessing the MFIS register space from the SYS domain. Table 29.7 shows the correspondence between the access from the SYS domain and MFIS operations.

Table 29.7 MFIS Operations

A2	Access from SYS domain	Operation
0	Read	Reading of registers specified by the index register (MFISIDX7 to MFISIDX0)
0	Write	Writing of registers specified by the index register (MFISIDX7 to MFISIDX0)
1	Read	Reading of the status register (MFISGSR7 to MFISGSR0)
1	Write	Writing of the index register (MFISIDX7 to MFISIDX0)

29.5.1 Control Signal for Register Access and Access Restrictions

Table 29.8 lists restrictions by control signals and access sources to access to the MFIS register. For details on access restrictions, see the register descriptions.

Table 29.8 Register Access Restrictions

	Access Restriction	
Register Name	**RT domain**	**SYS domain**
MFISIDX	R only	W only
MFISGSR	R/W	R/W
MFISSCR	R/W	R/W
MFISMCR	R only	R/W
MFISIICR	R/W	R/W
MFISEICR	R/W	R/W
MFISADR	R only	R/W
MFISDATA	R/W	R/W
MFISSM4	R/W	R/W

[Legend]
R: Read
W: Write

29.6 Interface

Here the details of the MFIS interface between the SYS domain and the RT domain are described.

The access timing from the SYS domain must be adjusted by the BSC settings. The minimum write signal assert width for the MFIS space is 3 cycles of HPϕ, and the minimum read signal assert width is 4 cycles of HPϕ.

29.6.1 MFISIDX Write/MFISGSR Read

Writing of MFISIDX and reading of MFISGSR are shown in figure 29.9. $\overline{\text{MFIREGCS}}$ is a chip-select signal asserted by the BSC for the MFI when an MFI register is to be accessed.

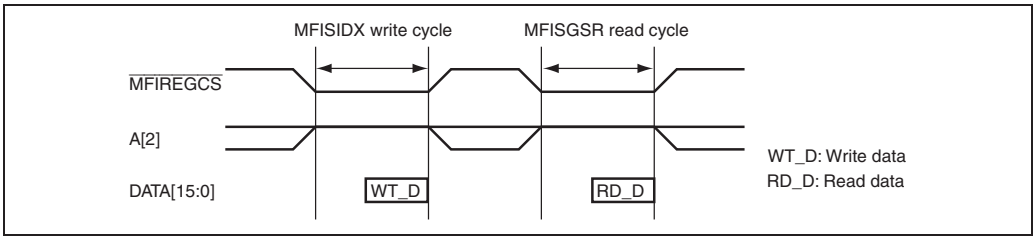


Figure 29.9 MFISIDX Write and MFISGSR Read

29.6.2 MFIS Register Read/Write

As shown in figure 29.10, in reading and writing of MFIS internal registers, first the A2 pin is held 1 and MFISIDX is written in order to select the register and byte position to be accessed. Then set the A2 pin to 0, and access the register selected by MFISIDX.

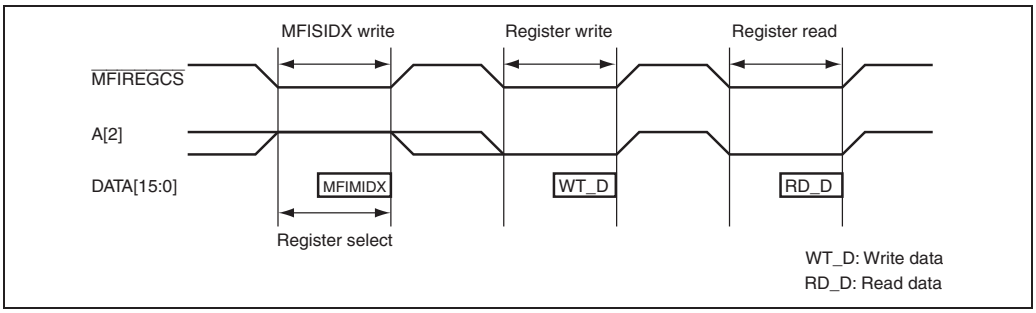


Figure 29.10 MFIS Register Settings

29.6.3 Continuous Data Writing from MFIS to SMFRAM

Figure 29.11 shows the timing chart for continuous data transfer from the MFIS to SMFRAM. As shown in this timing chart, by setting the start address and the data to be written first, continuous data transfer can subsequently be performed. As a result, effective data transfer to the SMFRAM can be performed using DMA transfer or similar methods.

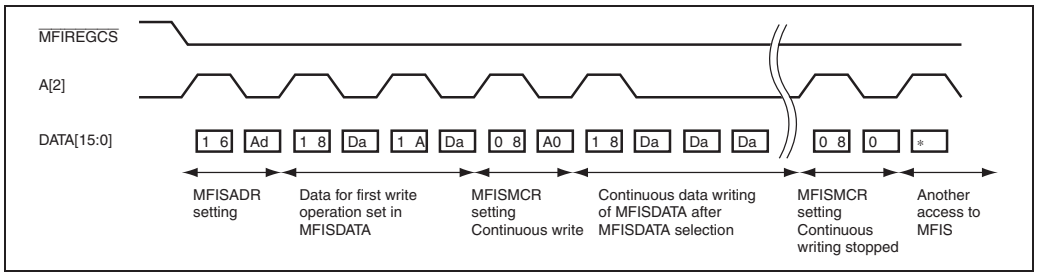


Figure 29.11 Continuous Data Writing to SMFRAM

29.6.4 Continuous Data Reading from SMFRAM through MFIS

Figure 29.12 shows the timing chart for continuous data reading from SMFRAM through the MFIS. As this timing chart indicates, by setting the start address, data can subsequently be read continuously. As a result, effective data transfer to the SMFRAM can be performed using DMA transfer or similar methods.

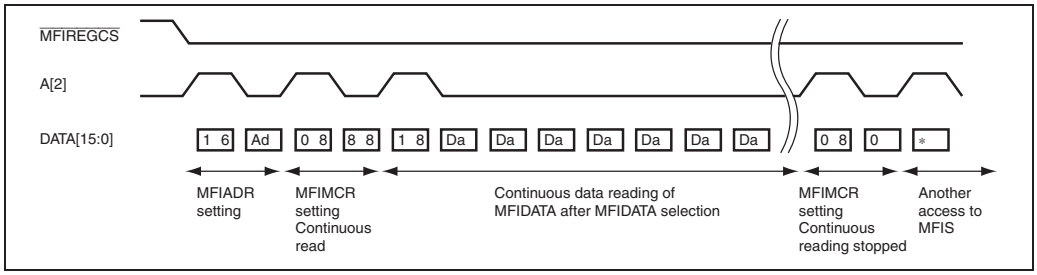


Figure 29.12 Continuous Data Reading from SMFRAM

Section 30 AC Parallel Interface 1 (ACMFI1)

This LSI has a non address-data multiplex type multifunctional interface (AC-MFI1 : AC-Multi Functional Interface 1 Non Address-Data multiplex) for use in high-speed transfer of data to external device, which cannot utilize the system bus.

The ACMFI1 allows external device to read from and write to 64 Kbytes of the on-chip ACMFRAM. This ACMFRAM can be accessed by both the ACMFI1 and on-chip CPU. Interrupts issued to this LSI by the external device, and interrupts sent from this LSI to the external device, are also supported. By using the ACMFRAM and these interrupt function, software-based data transfer between external device and on-chip CPU becomes possible, and connection to external device not releasing bus mastership is enabled.

30.1 Features

- The 64-Kbytes on-chip ACMFRAM can be read from and written to in 32-bit units.
- A 16-bit non address-data multiplex asynchronous interface is supported.
- Endian settings can be done.
- By writing specific bits in the ACMFI1 internal registers from the external device, interrupts can be issued. Conversely, interrupts can be sent from the on-chip CPU to the external device.
- Seven interrupt source bits each for internal interrupts and for external interrupts. As a result, software control of 128 different interrupts is possible, enabling high-speed data transfer using interrupts.
- Internal registers of this LSI (e.g. DMAC registers) can be accessed by using the ACMFI1 internal registers (bus master function).
- Data can be continuously read or written between the external device connected to the ACMFI1 and this LSI via ACMFRAM according to the register settings.

Figure 30.1 shows a block diagram of the ACMFI1.

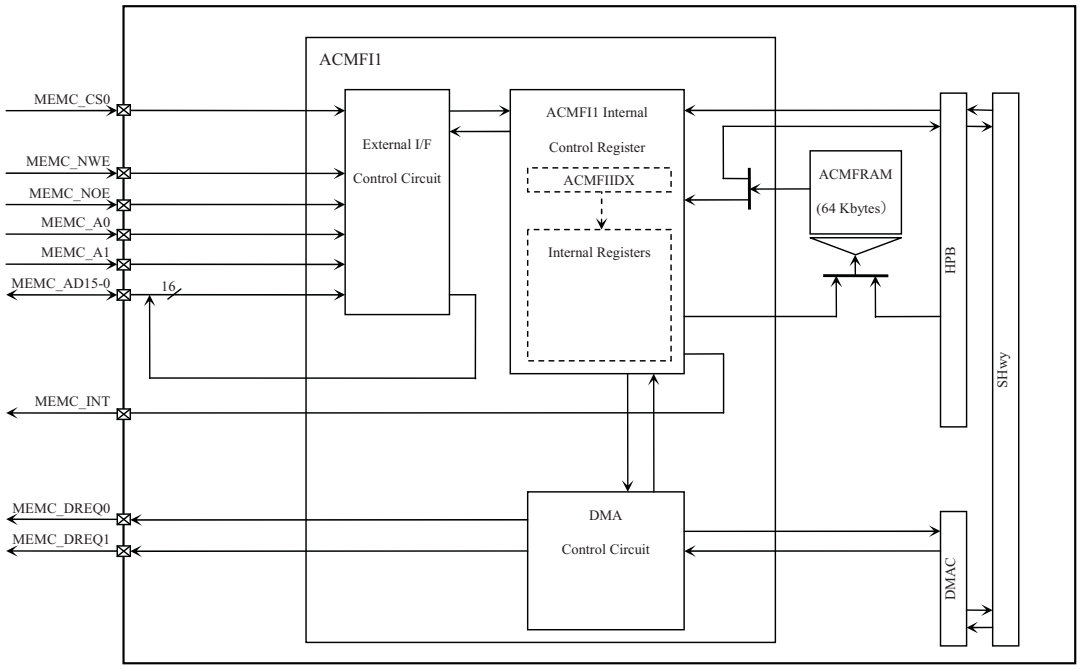


Figure 30.1 ACMFI1 Block Diagram

30.2 Input/Output Pins

The ACMFI1 pin configuration is listed in table 30.1.

Table 30.1 Pin Configuration

Name	Function	I/O	Description
MEMC_AD15 to MEMC_AD0	ACMFI1 data pins	I/O	Input/output to the ACMFI1
MEMC_CS0	ACMFI1chip select	Input	Chip select input to the ACMFI1
MEMC_A0	ACMFI1 register select 0	Input	Switching between ACMFI1 access types 0 L : Access to the register selected by ACMFIIDX H : Access to Index/status register
MEMC_A1	ACMFI1 register select 1	Input	Switching between ACMFI1 access types 1 L : Access in accordance with MEMC_A0 H : Access to ACMFIDATAW or ACMFIDATAR
MEMC_NWE	ACMFI1 write	Input	Write strobe signal; data is written while at low level
MEMC_NOE	ACMFI1 read	Input	Read strobe signal; data is read while at low level
MEMC_INT	ACMFI1 interrupt	Output	Interrupt request to the external device from the ACMFI1
MEMC_DREQ0	External DMA transfer request 0	Output	Output the DMA transfer request from the ACMFI1 to the external device
MEMC_DREQ1	External DMA transfer request 1	Output	Output the DMA transfer request from the ACMFI1 to the external device

30.3 Register Descriptions

Table 30.2 shows the ACMFI1 register configuration. Table 30.3 shows the register states in each operating mode.

Table 30.2 Register Configuration

Register Name	Abbreviation	R/W	Address	Access Size
ACMFI index register	ACMFIIDX	R/W	H'E6B7 0000	32
ACMFI general status register	ACMFIGSR	R/W	H'E6B7 0004	32
ACMFI status/control register	ACMFISCR	R/W	H'E6B7 0008	32
ACMFI memory control register	ACMFIMCR	R/W	H'E6B7 000C	32
ACMFI internal interrupt control register	ACMFIIICR	R/W	H'E6B7 0010	32
ACMFI external interrupt control register	ACMFIEICR	R/W	H'E6B7 0014	32
ACMFI address register	ACMFIADR	R/W	H'E6B7 0018	32
ACMFI data register	ACMFIDATA	R/W	H'E6B7 001C	32
ACMFI register control register	ACMFIRCR	R/W	H'E6B7 0020	32
ACMFI address register (for DMA write)	ACMFIADRW	R/W	H'E6B7 0044	32
ACMFI address register (for DMA read)	ACMFIADRR	R/W	H'E6B7 0048	32
ACMFI data register (for DMA write)	ACMFIDATAW	R/W	H'E6B7 004C	32
ACMFI data register (for DMA read)	ACMFIDATAR	R/W	H'E6B7 0050	32
ACMFI memory control register (for DMA write)	ACMFIMCRW	R/W	H'E6B7 0054	32
ACMFI memory control register (for DMA read)	ACMFIMCRR	R/W	H'E6B7 0058	32
ACMFI transfer number register (for DMA write)	ACMFIDNRW	R	H'E6B7 005C	32
ACMFI transfer number register (for DMA read)	ACMFIDNRR	R	H'E6B7 0060	32
ACMFI transfer size register (for DMA write)	ACMFISIZEW	R/W	H'E6B7 0064	32
ACMFI transfer size register (for DMA read)	ACMFISIZER	R/W	H'E6B7 0068	32
ACMFI semaphore register	ACMFISM4	R/W	H'E6B7 0080	32
ACMFI internal RAM	ACMFRAM	R/W	H'E6B9 0000 to H'E6B9 FFFF	32, 16, 8

[Note] Access size shows access size from on-chip CPU. Access size from external device via AC parallel interface 1 is 16bit.

Table 30.3 Register States in Each Operating Mode

Register Name	Power-On Reset	Power down of A4S area
ACMFIIDX	Initialized	Initialized
ACMFIGSR	Initialized	Initialized
ACMFISCR	Initialized	Initialized
ACMFIMCR	Initialized	Initialized
ACMFIIICR	Initialized	Initialized
ACMFIEICR	Initialized	Initialized
ACMFIADR	Initialized	Initialized
ACMFIDATA	Initialized	Initialized
ACMFIRCR	Initialized	Initialized
ACMFIADRW	Initialized	Initialized
ACMFIADRR	Initialized	Initialized
ACMFIDATAW	Initialized	Initialized
ACMFIDATAR	Initialized	Initialized
ACMFIMCRW	Initialized	Initialized
ACMFIMCRR	Initialized	Initialized
ACMFIDNRW	Initialized	Initialized
ACMFIDNRR	Initialized	Initialized
ACMFISIZEW	Initialized	Initialized
ACMFISIZER	Initialized	Initialized
ACMFISM4	Initialized	Initialized
ACMFRAM	Undefined	Undefined

30.3.1 ACMFI Index Register (ACMFIIDX)

ACMFIIDX is used to specify the register for reading and writing from the ACMFI1 with MEMC_A0 pin held low. From the ACMFI1, this register can only be written while MEMC_A0 pin is set high.

Bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	REG[5:0]						BYTE[1:0]	
Initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 2	REG[5:0]	000000	R/W*	ACMFI1 Internal Register Select 5 to 0 000000 : ACMFIGSR 000001 : ACMFISCR 000010 : ACMFIMCR 000011 : ACMFIIICR 000100 : ACMFIEICR 000101 : ACMFIADR 000110 : ACMFIDATA 000111 : ACMFIRCR 010000 : ACMFIADRW 010001 : ACMFIADRR 010010 : ACMFIDATAW 010011 : ACMFIDATAR 010100 : ACMFIMCRW 010101 : ACMFIMCRR 010110 : ACMFIDNRW 010111 : ACMFIDNRR 011000 : ACMFISIZEW 011001 : ACMFISIZER 100000 : ACMFISM4 Others : Setting prohibited

Bit	Bit Name	Initial Value	R/W	Description
1, 0	BYTE[1:0]	00	R/W*	Internal Register Byte Specification These bits specify of which 16 bits of the 32-bit register are to be accessed. Case of ACMFISCR.BO = 0 00 : Register bits [31:16] 01 : Setting prohibited 10 : Register bits [15:0] 11 : Setting prohibited Case of ACMFISCR.BO = 1 00 : Register bits [15:0] 01 : Setting prohibited 10 : Register bits [31:16] 11 : Setting prohibited However, when ACMFIDATA is selected using bits REG[5:0], each time reading or writing of ACMFIDATA occurs, bits BYTE[1:0] change according to the following rules. 16-bit bus : 00 → 10 → 00 → 10… repeated

[Note] * These bits can only be written via the ACMFI1, while MEMC_A0 pin is set high. They cannot be written by on-chip CPU.

30.3.2 ACMFI General Status Register (ACMFIGSR)

ACMFIGSR can be freely used for mutual display of states between the external device connected to ACMFI1 and the on-chip CPU. When MEMC_A0 pin is set high, this register is read-only from ACMFI1. When writing to the ACMFIGSR via ACMFI1, writing should be performed with ACMFIGSR specified in bits REG[5:0] in ACMFIIDX, and with MEMC_A0 pin set low. In this state, ACMFIGSR can also be read.

Bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	STATUS[7:0]							
Initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	STATUS[7:0]	H'00	R/W	General Status These bits can be read and written by the software of the external device connected to the ACMFI1, and by the on-chip CPU. Except upon a reset, they are never overwritten by hardware.

30.3.3 ACMFI Status/Control Register (ACMFISCR)

ACMFISCR is used to control the ACMFI1 mode and state.

Bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	MDREN	MDRN[2]	MDWN[2]	-	-
Initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
R/W :	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MDRN[1:0]		MDWN[1:0]		MDWEN	-	MDCS	-	-	-	-	-	-	-	EDN	BO
Initial :	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1
R/W :	R/W	R/W	R/W	R/W	R/W	R	R/W	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	MDREN	0	R/W*	Specifies whether MEMC_DREQ1 is output. 0 : MEMC_DREQ1 is not output 1 : MEMC_DREQ1 is output
19	MDRN[2]	0	R/W*	When using ACMFIADRR with MDRN[1:0], specifies the negate timing of MEMC_DREQ1. This negate timing is decided by increment count of ACMFIADRR. 000 : 1 time(for 4byte)、 001 : setting prohibited 010 : 1 time(for 16byte)、 011 : 4 times(for 16byte) 100 : 1 time(for 32byte)、 101 : 8 times(for 32byte) 110 : 1 time(for 64byte)、 111 : 16 times(for 64byte)
18	MDWN[2]	0	R/W*	When using ACMFIADRW with MDWN[1:0], specifies the negate timing of MEMC_DREQ0. This negate timing is decided by increment count of ACMFIADRW. 000 : 1 time(for 4byte)、 001 : setting prohibited 010 : 1 time(for 16byte)、 011 : 4 times(for 16byte) 100 : 1 time(for 32byte)、 101 : 8 times(for 32byte) 110 : 1 time(for 64byte)、 111 : 16 times(for 64byte)
17 to 16	-	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.
15 to 14	MDRN[1:0]	00	R/W*	Refer to MDRN[2] bit.
13 to 12	MDWN[1:0]	00	R/W*	Refer to MDWN[2] bit.
11	MDWEN	0	R/W*	Specifies whether MEMC_DREQ0/MEMC_DREQ1 signal is used. 0 : MEMC_DREQ0/MEMC_DREQ1 signal is not used. 1 : MEMC_DREQ0/MEMC_DREQ1 signal is used.
10	-	0	R	Reserved This bit is always read as 0. The write value should always be 0.
9	MDCS	0	R/W*	MEMC_DREQ Signal Selection Specifies the MEMC_DREQ signal to be used. 0 : Only MEMC_DREQ1 (With this setting, one-side channel is only operable.) 1 : MEMC_DREQ0/MEMC_DREQ1
8 to 7	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6	-	1	R	Reserved This bit is always read as 1. The write value should always be 1.

5 to 2	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	EDN	1	R/W	Endian (for ACMFRAM access) Specifies the byte positions when accessing the ACMFRAM from the on-chip CPU. 0 : Big endian 1 : Little endian
0	BO	1	R/W	Byte Order Specifies the byte position of the ACMFIDATA[31:0] bits corresponding to bits BYTE[1:0] in ACMFIIDX. 0 : Big endian (MSB first) 1 : Little endian (LSB first)

[Note] * This bit can only be written via ACMFI1. It cannot be written by the on-chip CPU.

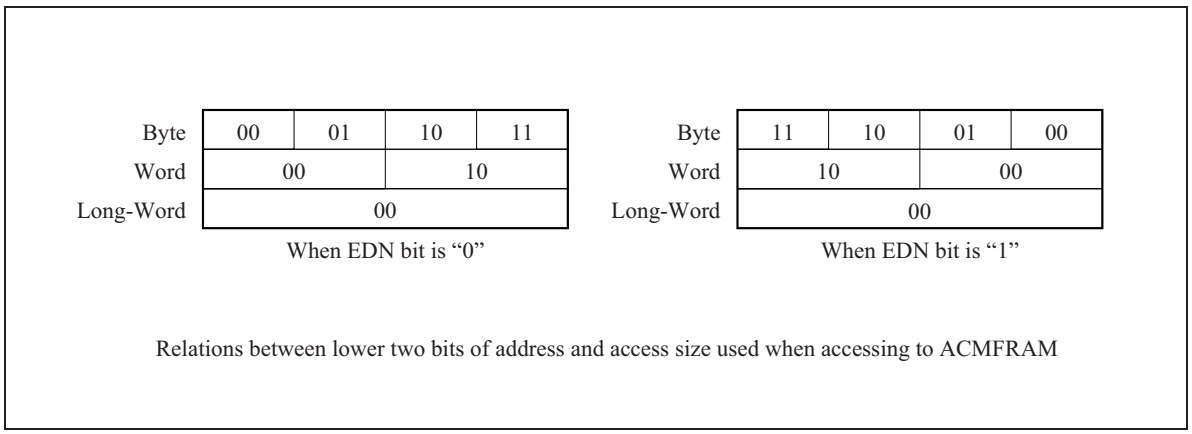


Figure 30.2 Difference in EDN Bit Specifications

30.3.4 ACMFI Memory Control Register (ACMFIMCR)

ACMFIMCR is used to control the ACMFRAM via ACMFI1.

Bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	LOCK	-	WT	-	RD	-	-	AI/AD
Initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R/W	R	R/W	R	R/W	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	LOCK	0	R/W*1	Lock This bit is used to lock read/write operations during continuous access. When “1” is written to the LOCK bit, the values of the RD and WT bits set at that time are held until the LOCK bit is next cleared to “0”. By using the LOCK, RD, and WT bits, modes are as follows : LOCK RD WT 1 1 0 : Continuous read mode 1 0 1 : Continuous write mode The RD and WT bits should be set to “1” simultaneously.
6	-	0	R	Reserved This bit is always read as 0. The write value should always be 0.
5	WT	0	R/W*1	Write When this bit is set to “1”, the ACMFIDATA value is written to ACMFRAM position corresponding to ACMFIADR.*2*3 • If the WT bit and LOCK bit are set to “1” simultaneously, a state of continuous writing to ACMFI1 is entered, and high-speed data transfer becomes possible. This state is maintained until the WT bit is next cleared to “0”, or until the LOCK bit is cleared to “0”. • If the LOCK bit is not simultaneously set to “1”, writing to ACMFRAM is performed only once. The value of the WT bit is automatically cleared to “0”.
4	-	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
3	RD	0	R/W*1	Read When this bit is set to “1”, the ACMFRAM data corresponding to ACMFIADR is read in ACMFIDATA.*2*3*4 • If the RD bit and LOCK bit are set to “1” simultaneously, a state of continuous reading of the ACMFI1 is entered, and high-speed data transfer becomes possible. This state is maintained until the RD bit is next cleared to “0”, or until The LOCK bit is cleared to “0”. • If the LOCK bit is not simultaneously set to “1”, reading of ACMFRAM is performed only once. The value of the RD bit is automatically cleared to “0”.
2 to 1	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	AI/AD	0	R/W*1	Address Auto-Increment/Decrement This bit is valid only when the LOCK bit is “1”. The value of ACMFIADR is automatically incremented by 4 or decremented by 4 according to the setting of this bit each time reading or writing of ACMFRAM is performed. 0 : Auto-increment mode (+4) 1 : Auto-decrement mode (-4)

[Note] 1. This bit can only be written via ACMFI1. It cannot be written by the on-chip CPU.

2. If access of ACMFRAM from the on-chip CPU and access of ACMFRAM via ACMFI1 occur simultaneously, the access via ACMFI1 is executed first.

3. If a single reading or single writing is necessary after continuous reading or continuous writing, it should be performed after the WT bit and RD bit is cleared to “0”.

4. When continuous read with DMA transfer function is executed and this bit is set to “1”, dummy read from this register is executed before previous setting and ACMFI1 Bus Access, Dummy Read and set RD bit to “1” must continue.

30.3.5 ACMFI Internal Interrupt Control Register (ACMFIIICR)

ACMFIIICR is used to issue interrupts from the external device connected to ACMFI1 to the on-chip CPU.

Bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	IIC[6:0]							IIR
Initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 1	IIC[6:0]	All 0	R/W	Internal Interrupt Source These bits used to specify the source for interrupts generated by the IIR. These bits can be written from both external device via ACMFI1 and on-chip CPU. By using these bits, fast execution of an interrupt handler is possible. These bits are completely under software control, and their values have no effect on the operation of the LSI.
0	IIR	0	R/W	Internal Interrupt Request While this bit is “1”, an interrupt request is issued to the on-chip CPU.

30.3.6 ACMFI External Interrupt Control Register (ACMFIEICR)

ACMFIEICR is used to issue interrupts to the external device connected to ACMFI1 from the on-chip CPU.

Bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	WEFE	REFE	-	-	WDFE	-	RDFE	-	-
Initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R/W	R/W	R	R	R/W	R	R/W	R	R

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WEFF	REFF	-	-	WDF	RDF	-	RSTEND	EIC[6:0]							EIR
Initial :	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R	R	R/W	RW	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	WEFE	0	R/W	Register Write End Notification Sets whether to notify, through MEMC_INT pin, when register write operation finishes. 0 : Does not notify the end of register write operation through MEMC_INT pin 1 : Notifies the end of register write operation through MEMC_INT pin.
23	REFE	0	R/W	Register Read End Notification Sets whether to notify, through MEMC_INT pin, when register read operation finishes. 0 : Does not notify the end of register read operation through MEMC_INT pin. 1 : Notifies the end of register read operation through MEMC_INT pin.
22 to 21	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	WDFE	0	R/W	ACMFRAM Overflow Notification Sets whether to notify, through MEMC_INT pin, when ACMFRAM overflows during DMA transfer. 0 : Does not notify an overflow through MEMC_INT pin 1 : Notifies an overflow through MEMC_INT pin
19	-	0	R	Reserved This bit is always read as 0. The write value should always be 0.
18	RDFE	0	R/W	ACMFRAM Read Data Empty Notification Sets whether to notify, through MEM_INT pin, when ACMFRAM becomes empty of read data during DMA transfer. 0 : Does not notify read data empty through MEMC_INT pin 1 : Notifies read data empty through MEMC_INT pin
17 to 16	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

15	WEFF	0	R/W	Register Write End Flag Flag indicating that register write operation has finished. 0 : Clears the flag 1 : Retains the previous value
14	REFF	0	R/W	Register Read End Flag Flag indicating that register read operation has finished. 0 : Clears the flag 1 : Retains the previous value
13 to 12	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11	WDF	0	R/W	ACMFRAM Overflow Flag Flag indicating that ACMFRAM has lost free space during DMA transfer. 0 : Clears the flag 1 : Retains the previous value
10	RDF	0	R/W	ACMFRAM Read Data Empty Flag Flag indicating that no data to be read through ACMFI1 bus exists in ACMFRAM bus during DMA transfer. 0 : Clears the flag 1 : Retains the previous value
9	-	0	R	Reserved This bit is always read as 0. The write value should always be 0.
8	RSTEND	1	R/W	Reset Period End Flag Flag indicating that the reset period has finished. 0 : Clears the flag 1 : Retains the previous value
7 to 1	EIC[6:0]	All 0	R/W	External Interrupt Source These bits used to specify the source for interrupts generated by the EIR. These bits can be written from both external device and on-chip CPU. By using these bits, fast execution of an interrupt handler is possible. These bits are completely under software control, and their values have no effect on the operation of this LSI.
0	EIR	0	R/W	External Interrupt Request While this bit is “1”, the MEMC_INT pin is asserted and an interrupt request is issued to the external device from the LSI.

30.3.7 ACMFI Address Register (ACMFIADR)

ACMFIADR indicates the address in the ACMFRAM to be accessed via ACMFI1.

When using the setting of the LOCK bit in ACMFIMCR to specify continuous access of the ACMFRAM, auto-increment (+4) or auto-decrement (-4) of the address, according to the AI/AD bit setting in ACMFIMCR, is performed automatically, and the ACMFIADR is updated. Wrap-around operation is performed if auto-increment or auto-decrement causes an excess of the following valid bits.

Bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	A[31:16]															
Initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	A[15:2]														-	-
Initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	A[31:2]	All 0	R/W*	Address These bits specify the 64-Kbyte memory space of ACMFRAM to be accessed via ACMFI1, with 32-bit boundary. They also specify the address of an internal register of this LSI to be accessed via ACMFI1. These A[15:2] bits are valid when ACMFRAM is accessed, whereas A[31:10] bits are valid when an internal register of this LSI is accessed.
1 to 0	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

[Note] * These bits can only be written by the external device via ACMFI1. They cannot be written by the on-chip CPU.

30.3.8 ACMFI Data Register (ACMFIDATA)

ACMFIDATA is used to hold data for writing to the ACMFRAM and data read from the ACMFRAM. ACMFIDATA is also used to hold data read from and written to registers which are accessed via ACMFI1. If ACMFIDATA is not used when accessing ACMFRAM, it can be used for LSI software data transfer with the external device connected to the ACMFI1.

Bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	D[31:16]															
Initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	D[15:0]															
Initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	D[31:0]	All 0	R/W	32-Bit Data

30.3.9 ACMFI Register Control Register (ACMFIRCR)

ACMFIRCR is used to access internal registers of this LSI via the ACMFI1.

Bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	AER	-	RWT	RRD	SZ[1:0]		ADR[9:0]									
Initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
15	AER	0	R/W	Address Error If the value set in the ADR bits is not consistent with the register access size, this bit is set to “1”. Read/write operation is canceled when an address error occurs. 0 : Clears the flag 1 : Retains the previous value
14	-	0	R	Reserved This bit is always read as 0. The write value should always be 0.
13	RWT	0	R/W	Register Write Write “1” to this bit when writing to a register. When writing to the register is completed, this bit is cleared to “0”.
12	RRD	0	R/W	Register Read Write “1” to this bit when reading from a register. When reading from the register is completed, this bit is cleared to “0”.
11 to 10	SZ[1:0]	00	R/W	Register Access Size These bits specify the access size for reading from/writing to a register. 00 : Byte 01 : Word 10 : Long-Word 11 : Setting prohibited
9 to 0	ADR[9:0]	All 0	R/W	Register Low-Order Address The address of the register to be accessed is specified in conjunction with ACMFIADR. Address = {ACMFIADR[31:10], ACMFIRCR[9:0]}

[Note] This register can be read and written by the external device via ACMFI1. It cannot be read or written by the on-chip CPU.

30.3.10 ACMFI address Register (for DMA Write) (ACMFIADRW)

ACMFIADRW is a register that indicates low-order address in the ACMFRAM for the write access via the ACMFI1 during DMA transfer. Auto-increment (+4) of the address is performed automatically each time 4 bytes of data are written and then ACMFIADRW is updated. The address is automatically updated to the one specified by ACMFIADRW if auto-increment causes an excess of the DMA transfer range set by ACMFISIZEW.

Bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	A[15:2]														-	-
Initial :	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 2	A[15:2]	H'3800	R/W*	Address These bits specify the lower 16 bits of 64-Kbyte memory space in the ACMFRAM that is for the write access via ACMFI1 during DMA transfer. Address can set only “H’3800”.
1 to 0	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

[Note] * This register can be read and written by the external device via ACMFI1. It cannot be read or written by the on-chip CPU.

30.3.11 ACMFI Address Register (for DMA Read) (ACMFIADRR)

ACMFIADRR is a register that indicates low-order address in the ACMFRAM for the read access via the ACMFI1 during DMA transfer. Auto-increment (+4) of the address is performed automatically each time 4 bytes of data are written and then ACMFIADRR is updated. The address is automatically updated to the one specified by ACMFIADRR if auto-increment causes an excess of the DMA transfer range set by ACMFISIZER.

Bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	A[15:2]														-	-
Initial :	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 2	A[15:2]	H'3C00	R/W*	Address These bits specify the lower 16 bits of 64-Kbyte memory space in the ACMFRAM that is for the read access via ACMFI1 during DMA transfer. Address can set only “H’3C00”.
1 to 0	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

[Note] * This register can be read and written by the external device via ACMFI1. It cannot be read or written by the on-chip CPU.

30.3.12 ACMFI Data Register (for DMA Write) (ACMFIDATAW)

ACMFIDATAW is used to hold data for writing to the ACMFRAM during DMA transfer.

Bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	D[31:16]															
Initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	D[15:0]															
Initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	D[31:0]	All 0	R/W	32-Bit Data

30.3.13 ACMFI Data Register (for DMA Read) (ACMFIDATAR)

ACMFIDATAR is used to hold data for reading from the ACMFRAM during DMA transfer.

Bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	D[31:16]															
Initial :	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	D[15:0]															
Initial :	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	D[31:0]	Undefined	R/W	32-Bit Data

[Note] These bits cannot be written from the on-chip CPU when the MEMC_A1 pin is in high level.

30.3.14 ACMFI Memory Control Register (for DMA Write) (ACMFIMCRW)

ACMFIMCRW is a register that controls the write access to the ACMFRAM via the ACMFI1 during DMA transfer.

Bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	DREQW	DRSW[1:0]		DRW	LOCKW	DWTW	WT	-	-	-	-	-
Initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
R/W :	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11	DREQW	0	R/W*[1]	Specifies whether the MEMC_DREQ0 signal is used for writing to the ACMFRAM. 0 : The MEMC_DREQ0 signal is not used 1 : The MEMC_DREQ0 signal is used
10 to 9	DRSW[1:0]	00	R/W*[1]	When the MEMC_DREQ0 signal is used for writing, if there is free space larger than the one specified by these bits, MEMC_DREQ0 signal is output. 00 : 4Byte 01 : 16Byte 10 : 32Byte 11 : 64Byte
8	DRW	0	R	Write Data Ready This bit is set to "1" when the number of long-word data (transfer pointer) written to the ACMFRAM is 1 or greater.
7	LOCKW	0	R/W*[1]	This bit locks the writing operation for the successive access. When this bit is set to "1", the DWTW bit should also set to "1".
6	DWTW	0	R/W*[1]	Specifies whether the DMA transfer is performed from the ACMFRAM. 0 : DMA transfer is not performed 1 : DMA transfer is performed
5	WT	0	R/W*[1]	When "1" is written to this bit, the value of ACMFIDATAW is written to the area in the ACMFRAM that corresponds to ACMFIADRW.
4 to 3	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2 to 1	-	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.

0	-	0	R	Reserved This bit is always read as 0. The write value should always be 0.

[Note] 1. This register can be read and written by the external device via ACMFI1. It cannot be read or written by the on-chip CPU.

2. When the ACMFRAM access from the on-chip CPU and the ACMFRAM access from the external device via the ACMFI1 occur simultaneously, the access from the external device takes the priority.

3. The writing should be performed after the WT bit is cleared to “0”.

30.3.15 ACMFI Memory Control Register (for DMA Read) (ACMFIMCRR)

ACMFIMCRR is a register that controls the read access from the ACMFRAM via the ACMFI1 during DMA transfer.

Bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	DREQR	DRSR[1:0]		DRR	LOCKR	DWTR	RD	-	-	-	-	-
Initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
R/W :	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11	DREQR	0	R/W*1	Specifies whether the MEMC_DREQ1*2 signal is used for reading from the ACMFRAM. 0 : The MEMC_DREQ1*2 signal is not used 1 : The MEMC_DREQ1*2 signal is used
10 to 9	DRSR[1:0]	00	R/W*1	When the MEMC_DREQ1*2 signal is used for reading, if there is free space lager than the one specified by these bits, the MEMC_DREQ1*2 signal is output. 00 : 4Byte 01 : 16Byte 10 : 32Byte 11 : 64Byte
8	DRR	0	R	Read Data Ready This bit is set to “1” when the number of long-word data (transfer pointer) written to the ACMFRAM is 1 or greater.
7	LOCKR	0	R/W*1	This bit locks the reading operation for the successive access. When this bit is set to “1”, the DWTR bit should also set to “1”.

6	DWTR	0	R/W*[1]	Specifies whether the DMA transfer is performed from the ACMFRAM. 0 : DMA transfer is not performed 1 : DMA transfer is performed
5	RD	0	R/W*[1]	When "1" is written to this bit, the value of ACMFIDATAR is written to the area in the ACMFRAM that corresponds to ACMFIADRR.
4 to 3	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2 to 1	-	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.
0	-	0	R	Reserved These bits are always read as 0. The write value should always be 0.

[Note] 1. This register can be read and written by the external device via ACMFI1. It cannot be read or written by the on-chip CPU.

2. When the MDCS bit in ACMFISCR is cleared to "0", the signal is output from the MEMC_DREQ0 pin.

3. The reading should be performed after the RD bit is cleared to "0".

30.3.16 ACMFI Transfer Number register (for DMA Write) (ACMFIDNRW)

ACMFIDNRW is a register that indicates the valid number of written data (in long-word units) stored in the ACRAM during DMA transfer.

Bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	VDN[9:0]									
Initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 0	VDN[9:0]	All 0	R	Valid Number of ACMFRAM Data These bits indicate the valid number of data (in long-word units) stored in the ACMFRAM.

[Note] This register is a read-only register and cannot be written to from both the on-chip CPU and the external device via the ACMFI1.

30.3.17 ACMFI Transfer Number Register (DMA Read) (ACMFIDNRR)

ACMFIDNRR is a register that indicates the valid number of read data (in long-word units) stored in the ACMFRAM during DMA transfer.

Bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	VDN[9:0]									
Initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 0	VDN[9:0]	All 0	R	Valid Number of ACMFRAM Data These bits indicate the valid number of data (in long-word units) stored in the ACMFRAM.

[Note] This register is a read-only register and cannot be written to from both the on-chip CPU and the external device via the ACMFI1.

30.3.18 ACMFI Transfer Size Register (for DMA Write) (ACMFISIZEW)

ACMFISIZEW is a register that specifies the number of transfer size for writing in long-word units during DMA transfer.

Bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	SIZEW[10:0]										
Initial :	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 11	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 0	SIZEW[10:0]	H'100	R/W	Number of DMA Transfer Size for Writing These bits specify the number of DMA transfer size for writing in long-word units. Transfer size can set only “H’100”.

[Note] Rewriting to this register during DMA transfer is prohibited. If rewritten, the operation is not guaranteed.

30.3.19 ACMFI Transfer Size Register (for DMA Read) (ACMFISIZER)

ACMFISIZER is a register that specifies the number of transfer size for reading in long-word units during DMA transfer.

Bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	SIZER[10:0]										
Initial :	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 11	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 0	SIZER[10:0]	H'100	R/W	Number of DMA Transfer Size for Reading These bits specify the number of DMA Transfer size for reading in long-word units. Transfer size can set only “H’100”.

[Note] Rewriting to this register during DMA transfer is prohibited. If rewritten, the operation is not guaranteed.

30.3.20 ACMFI Semaphore Register (ACMFISM4)

ACMFISM4 is dedicated register allowing read modify write to be performed from the external device via the ACMFI1 and from the on-chip CPU. Using ACMFISM4 as a semaphore can improve the data transfer efficiency.

In a state where neither the external device nor the on-chip CPU makes a request, ACMFISM4 indicates that the SM[7:6] = “00”. If a request (for read operation to the ACMFISM4) from the external device occurs in this state, the SM[7:6] = “00” is read. Viewing the SM[7:6] = “00”, software can learn the successful acquisition. After this, ACMFISM4 changes to the SM[7:6] = “01”.

Bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	SM[7:6]		INF[5:0]					
Initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	-	0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 6	SM[7:6]	00	R/W	Bits for Semaphore If these bits are “00”, reading to this register reads “01” (read from the external device via the ACMFI1) or “10” (read from the on-chip CPU). The read value means a value before the change. The change is made only when “00” is read. 00 : Only reading from both the external device via the ACMFI1 and the on-chip CPU is possible. 01 : Reading/writing from the external device via the ACMFI1 is possible, and only reading is possible from the on-chip CPU. 10 : Only reading from the external device via the ACMFI1 is possible, reading/writing from the on-chip CPU is possible. 11 : Setting prohibited.
5 to 0	INF[5:0]	All 0	R/W	Reading/writing is allowed according to the semaphore conditions of SM[7:6] bits. These bits are usually used as information.

[Note] 1. If reading from the external device via the ACMFI1 and the on-chip CPU simultaneously occurs for ACMFISM4 with the SM[7:6] = “00”, ACMFISM4 returns data of the SM[7:6] = “01” to the on-chip CPU, while returns “00” to the external device.

2. Access from the external device via the ACMFI1 to bits 31 to 16 is prohibited.

30.4 Operation

30.4.1 Access to ACMFI1 Registers

The ACMFI1 can be accessed by combining the MEMC_CS0, MEMC_A0, MEMC_NWE and MEMC_NOE signals. Table 30.4 shows the correspondence between combinations of these signals and ACMFI1 operations.

Table 30.4 ACMFI1 Operations

MEMC_CS0	MEMC_A0	MEMC_A1	MEMC_NWE	MEMC_NOE	Operation
H	X	X	X	X	No operation (NOP)
L	L	L	H	L	Read of register specified by ACMFIIDX[7:0]
L	L	L	L	H	Write of register specified by ACMFIIDX[7:0]
L	H	L	H	L	Read of ACMFIGSR
L	H	L	L	H	Write of ACMFIIDX
L	X	H	H	L	Read of ACMFIDATAR
L	X	H	L	H	Write of ACMFIDATAW
L	X	X	H	H	No operation (NOP)
L	X	X	L	L	Setting prohibited

[Legend]

X : Don't care

L : Low level

H : High level

30.4.2 Control Signal for Register Access and Access Restrictions

Table 30.5 lists restrictions to access to the ACMFI1 register. For details on access restrictions, see the register descriptions.

Table 30.5 Register Access Restrictions

Register Name		Access Restriction	
		On-Chip CPU	ACMFI1 Interface (External Device)
ACMFI1 Register	ACMFIIDX	R only	W only
	ACMFIGSR	R/W	R/W
	ACMFISCR	R/W	R/W
	ACMFIMCR	R only	R/W
	ACMFIIICR	R/W	R/W
	ACMFIEICR	R/W	R/W
	ACMFIADR	R only	R/W
	ACMFIDATA	R/W	R/W
	ACMFIRCR	R only	R/W
	ACMFIADRW	R only	R/W
	ACMFIADRR	R only	R/W
	ACMFIDATAW	R/W	R/W
	ACMFIDATAR	R/W	R/W
	ACMFIMCRW	R only	R/W
	ACMFIMCRR	R only	R/W
	ACMFIDNRW	R only	R only
	ACMFIDNRR	R only	R only
	ACMFISIZEW	R/W	R/W
	ACMFISIZER	R/W	R/W
	ACMFISM4	R/W	R/W

[Legend]

R : Read

W : Write

30.4.3 Memory Map

Table 30.6 shows the memory space in the on-chip ACMFRAM.

Table 30.6 Memory Map

	Start Address	End Address	Memory Size	Classification
Via ACMFI1	H'0000	H'FFFF	64 Kbytes	On-chip ACMFRAM area
Via on-chip CPU	H'E6B9 0000	H'E6B9 FFFF	64 Kbytes	

30.4.4 Connection

When connecting the ACMFI1 to an external device, a method like that shown in figure 30.3 should be used.

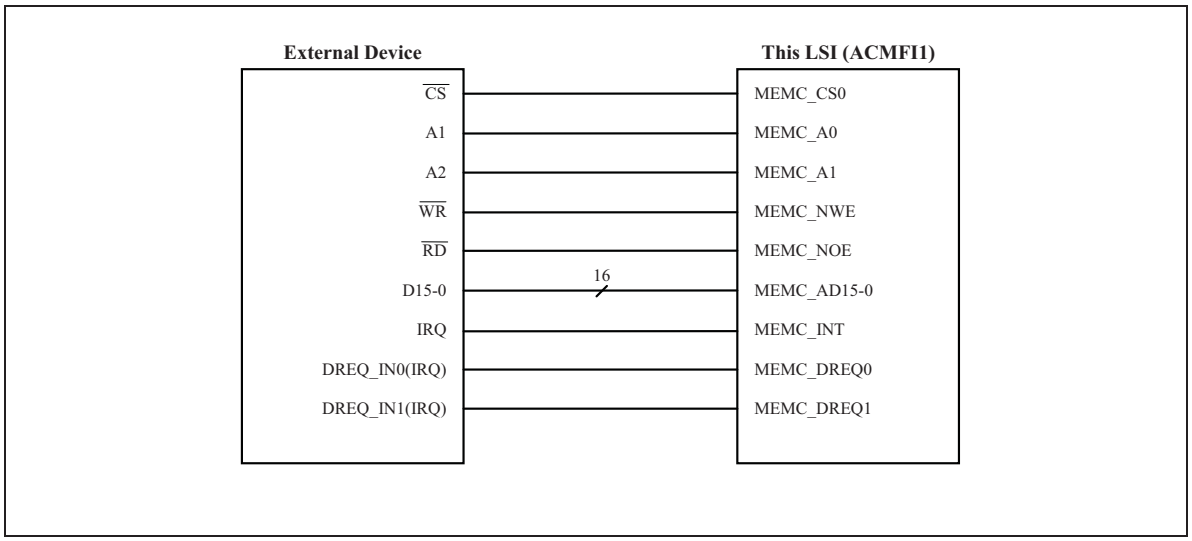


Figure 30.3 Example of ACMFI1 Connection

30.4.5 Access to LSI Internal Registers via the ACMFI1

By using function, on-chip peripheral module registers can be directly accessed from the external device via the ACMFI1. Write to and read from registers with the following procedures.

(1) Register Write Operation

1. Set the address of the register to be written to ACMFIADR and ACMFIRCR, and the data to be written to ACMFIDATA.
2. Setting the RWT bit in ACMFIRCR to “1” writes the data in ACMFIDATA to the address specified by ACMFIADR and ACMFIRCR.
3. When the write operation is completed, the RWT bit is automatically cleared to “0”.

(2) Register Read Operation

1. Set the address of the register to be read to ACMFIADR and ACMFIRCR.
2. Set the RRD bit in ACMFIRCR to “1”.
3. When the read operation is completed, the RRD bit is automatically cleared to “0” (read data is stored in ACMFIDATA）.

The register write operation flow and register read operation flow are shown in figure 30.4.

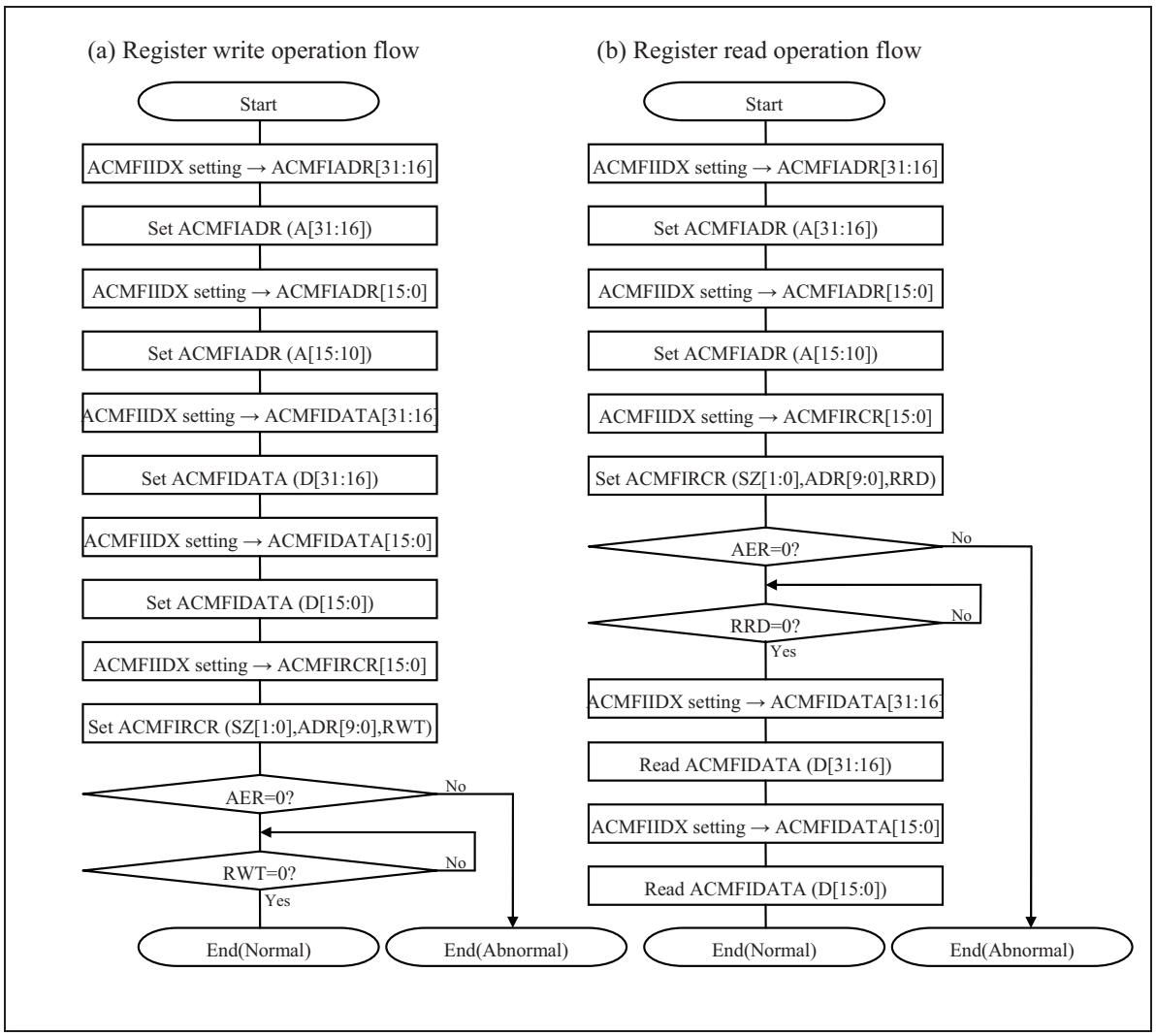


Figure 30.4 Register Write and Read Operation flows

30.4.6 DMA Transfer Request Output

By using this function, successive data read/write via the ACMFRAM is enabled with the reload mode of the DMAC.

First, the following shows the successive reading flow of the data written from the ACMFI1 bus.

1. Set the DMAC register with the reload mode enabled and start it up. At this time, DMA transfer size is 16bytes.
2. Set ACMFIADRW to “H’E000” and set ACMFISIZEW to “H’0100”.
3. Set the MDWN bit in ACMFISCR any value. This transfer unit must be corresponding to the transfer units of DRSW bit in ACMFIMCRW.
4. Set the LOCKW, DWTW and WT bits in ACMFIMCRW to “1”, respectively.
5. Drive the MEMC_A1 pin to high level and write data from the ACMFI1 bus.
6. The DMA transfers the valid data on the ACMFRAM.
7. When data write from the ACMFI1 bus is completed and number of transfers reaches the one specified in the DMAC, a DMA transfer end interrupt occurs.
8. After the interrupt source is handled in the interrupt handling routine, clear the LOCKW, DWTW and WT bits in ACMFIMCRW to “0”, respectively.

Then, the following shows the reading flow of the data that is successively written to the ACMFRAM by the DMAC from the ACMFI1 bus.

1. Set the DMAC register with the reload mode enabled and start it up. At this time, DMA transfer size is 16bytes.
2. Set ACMFIADRR to “H’F000” and set ACMFISIZER “H’0100”.
3. Set the MDRN bit in ACMFISCR any value. This transfer unit must be corresponding to the transfer units of DRSR bit in ACMFIMCRR.
4. Set the LOCKR and DWDR bits in ACMFIMCRR to “1”, respectively.
5. Wait until ACMFIDNRR is larger than transfer unit set by the above-mentioned “3.” or MEMC_DREQ* is asserted.
6. Set the RD bit in ACMFIMCRR to “1”.
7. Read ACMFIMCRR until the RD bit in ACMFIMCRR is “1”.
8. Drive the MEMC_A1 pin to high level and read data from the ACMFI1 bus.
9. When the DMA transfer is completed, a DMA transfer end interrupt occurs.
10. After the interrupt source is handled in the interrupt handling routine, clear the LOCKR, DWDR and RD bits in ACMFIMCRR to “0”, respectively.

Though successive read/write is enabled after the processing described above, caution should be paid to the following.

- The number of writing data from ACMFI1 bus is multiples of 16bytes when successive write is executed.
- The number of data transferred by DMAC is multiples of transfer unit of DRSR bits in ACMFIMCRR when successive read is executed.
- Set it again from the above flow “1.” when successive transfer is executed again.
- Please consider the response time of MEMC_INT pin when MEMC_INT pin is used and controlled during data transfer.
- Use any channels of DMAC as needed.

30.5 Interface (Basic)

The parallel interface using the ACMFI1 is described below. Access via the ACMFI1 is completed within a fixed time.

Figure 30.5 shows the basic read/write sequence.

Read operations are specified in the overlap period during which both the MEMC_NOE and MEMC_CS0 signals go low. Write operations are specified in the overlap period during which both the MEMC_NWE and MEMC_CS0 signals go low.

When the MEMC_A0 is low, the type is normal access, and when high, index/status registers access.

For details on the timing, refer to section **.*, AC characteristics.

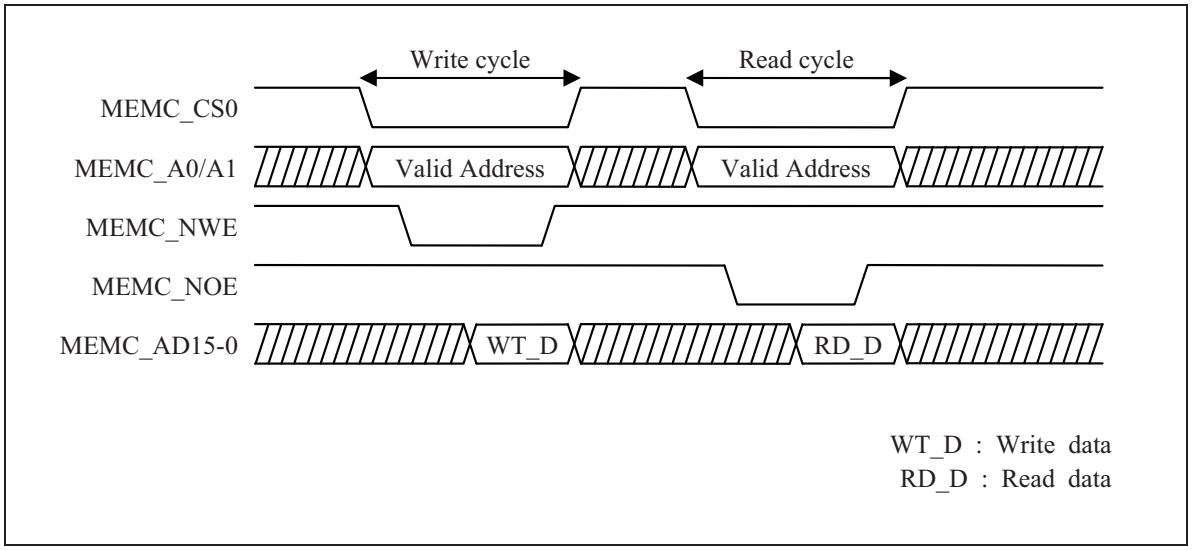


Figure 30.5 Basic Timing for ACMFI1 Interface

30.6 Interface (Details)

Here the details of the interface are described.

30.6.1 ACMFIIDX Write/ACMFIGSR Read

Writing of ACMFIIDX and reading of ACMFIGSR is shown in figure 30.6.

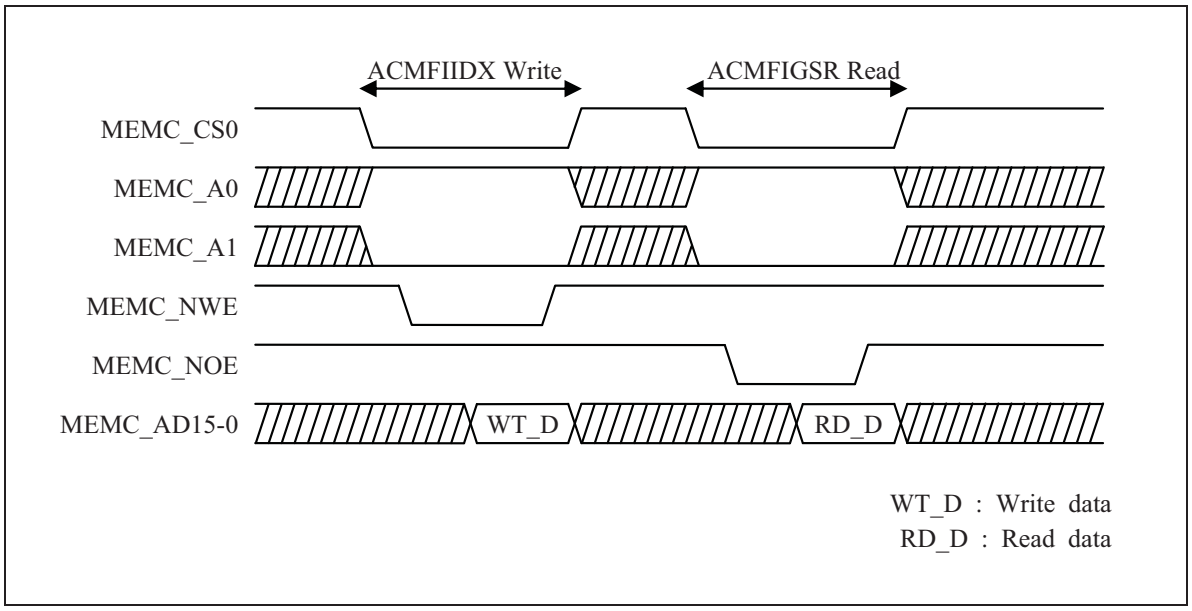


Figure 30.6 ACMFIIDX Write and ACMFIGSR Read

30.6.2 ACMFI1 Register Read/Write

As shown in figure 30.7, in reading and writing of ACMFI1 internal registers, first the MEMC_A0 signal is held high level and ACMFIIDX is written in order to select the register and byte position to be accessed. Then the MEMC_A0 signal is held low level and reading or writing of the register selected using ACMFIIDX is performed.

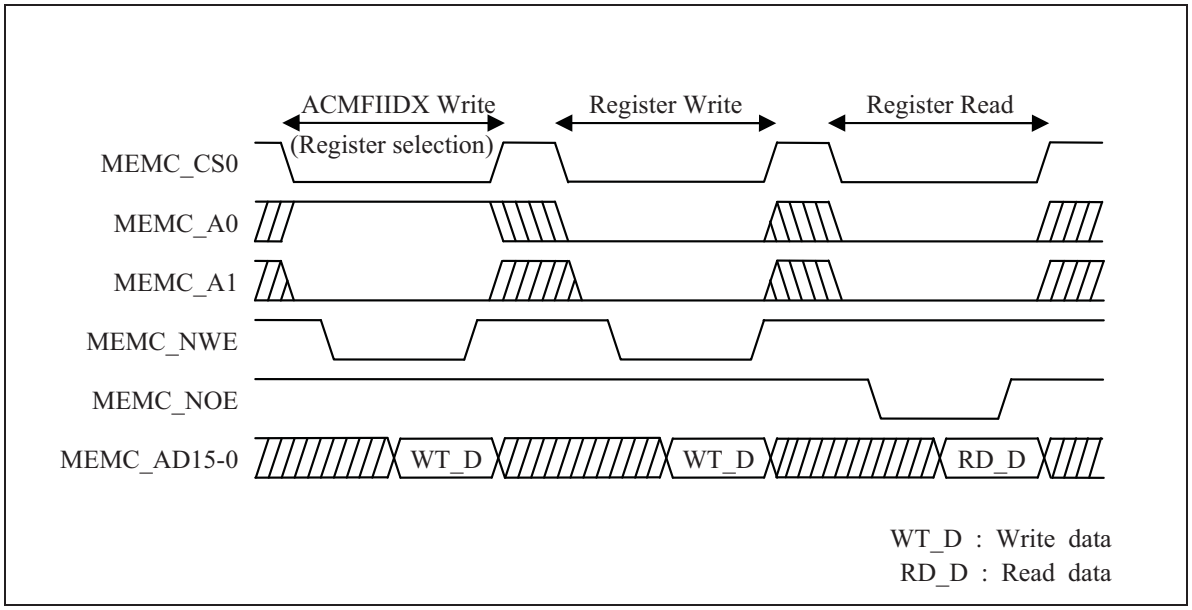


Figure 30.7 ACMFI1 Register Settings

Figure 30.8 shows the data drive timing at ACMFI1 bus read. MEMC_AD drive is controlled by the falling or rising edges of the MEMC_NOE signal.

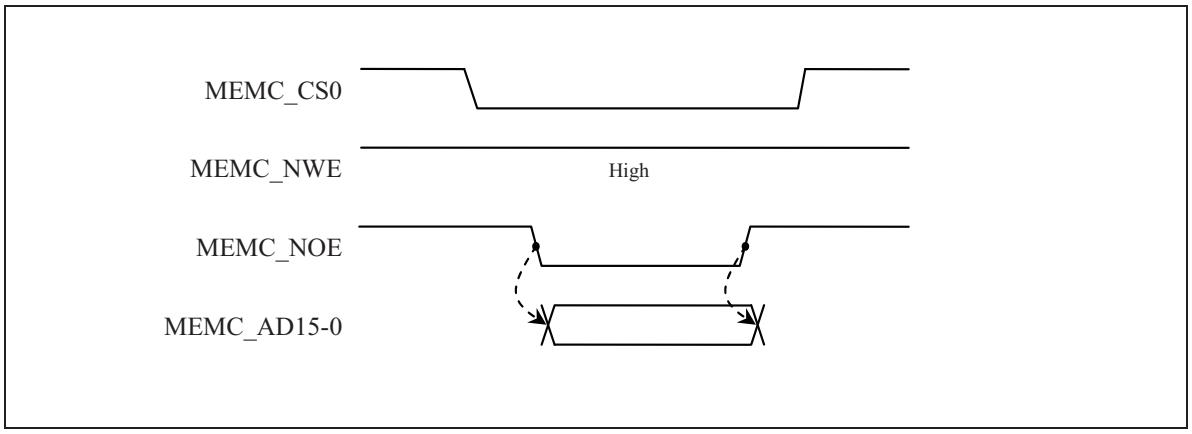


Figure 30.8 Data Drive Timing at ACMFI1 Bus Read

30.6.3 Continuous Data Writing from ACMFI1 to ACMFRAM

Figure 30.9 shows the timing chart for continuous data transfer from the ACMFI1 to ACMFRAM. As shown in this timing chart, by setting the start address and the data to be written first, continuous data transfer can subsequently be performed. As a result, effective data transfer to this LSI can be performed using DMA transfer or similar methods.

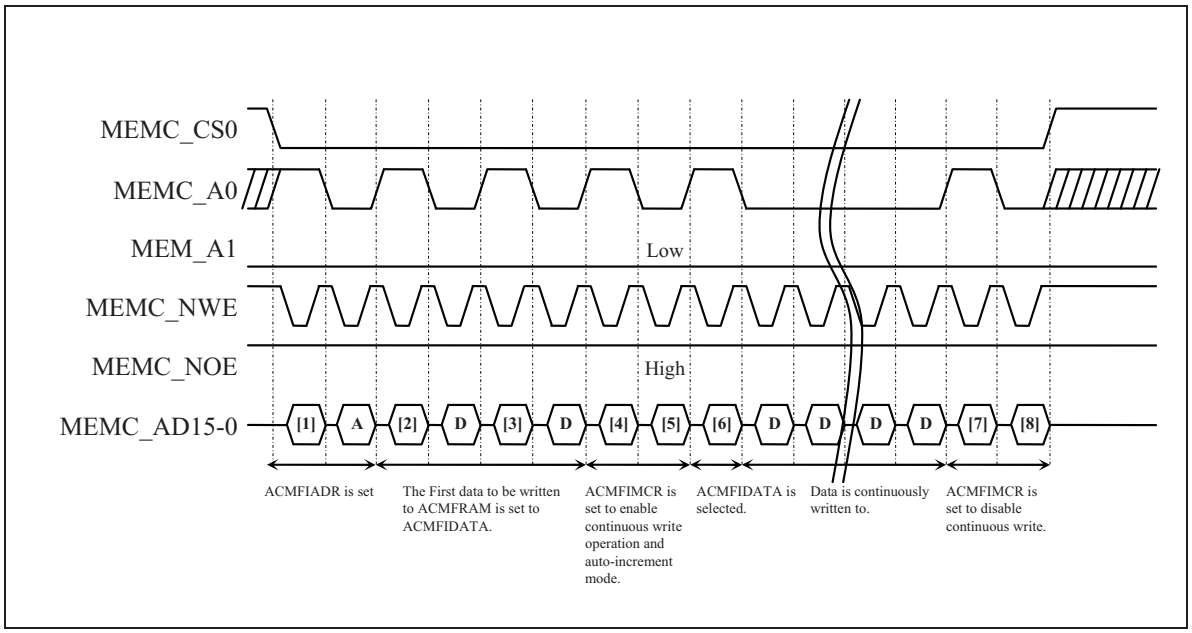


Figure 30.9 Continuous Data Writing to ACMFRAM

[Note] Details of symbols in figure are shown below.

A : The start address value of continuous write

D : The data value to be written to ACMFRAM

[1] : Index value in which ACMFIADR is selected (H'0014 or H'0016)

[2] : Index value in which ACMFIDATA is selected (H'0018 or H'001A)

[3] : Index value in which ACMFIDATA is selected (H'001A or H'0018)

[4] : Index value in which ACMFIMCR is selected (H'0008 or H'000A)

[5] : Set value of continuous write and auto-increment (H'00A0)

[6] : Index value in which ACMFIDATA is selected (H'0018 or H'001A)

[7] : Index value in which ACMFIMCR is selected (H'0008 or H'000A)

[8] : The value in which the continuous write and auto-increment are released (H'0000)

30.6.4 Continuous Data Reading from ACMFRAM

Figure 30.10 shows the timing chart for continuous data reading from ACMFRAM through the ACMFI1. As shown in this timing chart, by setting the start address, data can subsequently be read continuously. As a result, effective data transfer to this LSI can be performed using DMA transfer or similar methods.

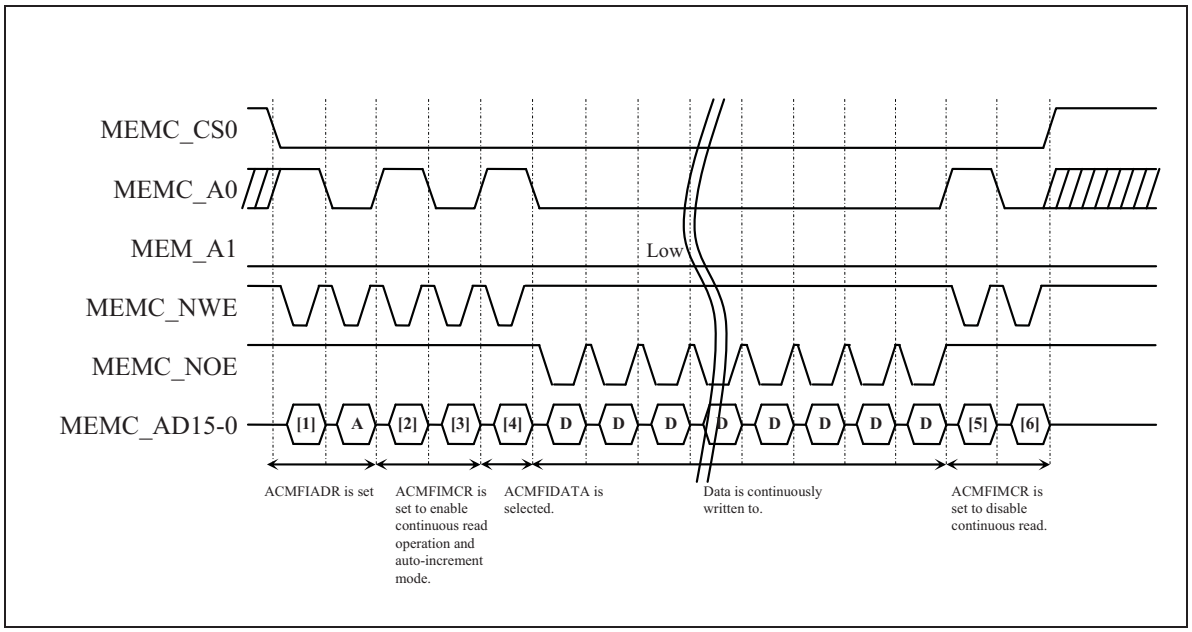


Figure 30.10 Continuous Data Reading from ACMFRAM

[Note] Details of symbols in figure are shown below.

A : The start address value of continuous read

D : The data value to be read by continuous read

[1] : Index value in which ACMFIADR is selected (H'0014 or H'0016)

[2] : Index value in which ACMFIMCR is selected (H'0008 or H'000A)

[3] : Set value of continuous read and auto-increment (H'0088)

[4] : Index value in which ACMFIDATA is selected (H'0018 or H'001A)

[5] : Index value in which ACMFIMCR is selected (H'0008 or H'000A)

[6] : The value in which the continuous read and auto-increment are released (H'0000)

Section 31 AC Parallel Interface 2 (ACMFI2)

This LSI has an address-data multiplex type multifunctional interface (AC-MFI2 : AC-Multi Functional Interface 2 Address-Data Multiplex) which realizes direct access from external device by 16bit parallel interface to the resource in this LSI. ACMFI2 has an asynchronous interface (MEMC_CS0) and a synchronous interface (MEMC_CS1), and high-speed access is possible to SDRAM connected to this LSI from external device.

31.1 Features

- This LSI has asynchronous interface chip select (MEMC_CS0) and synchronous interface chip select (MEMC_CS1).
- Both a synchronous interface and an asynchronous interface are an address-data multiplex.
- For an asynchronous interface, 16bit-read/write is possible for 64 K bytes of on-chip RAM, and ACMFI2 registers.
- High-speed burst access is possible to SDRAM connected to this LSI by the synchronous interface.
- The burst access size in a synchronous interface is unrestricted. (within target capacity)
- The input clock for a synchronous interface supports a maximum of 50MHz.
  (Conditions : Input clock frequency < internal clock frequency)
- It is possible to apply interrupt from external device to on-chip CPU or from on-chip CPU to external device.
- This LSI has an address complement register and it is possible to complement a certain specific address bit.
- This LSI has an address protective register and it is possible to restrict access for each address space.
- This LSI has an address auto increment function and high-speed continuous burst access is possible to SDRAM.
- This LSI has semaphore register and the communication can be assisted between external device and on-chip CPU.

The block diagram of ACMFI2 is shown in Fig.31.1.

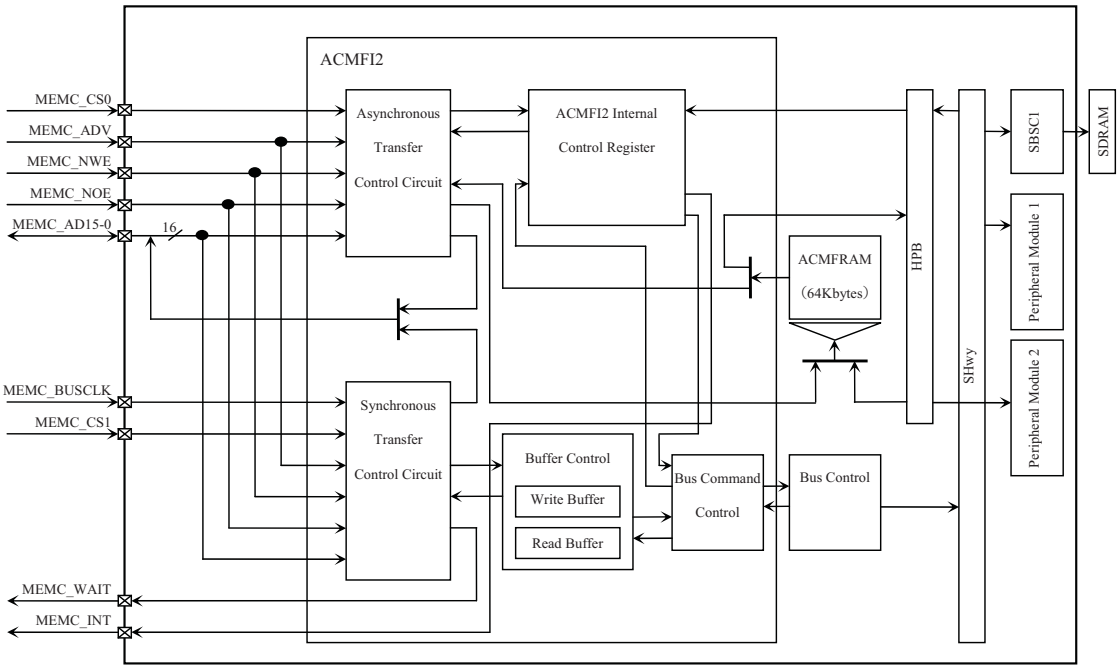


Figure 31.1 ACMFI2 block diagram

31.2 Input/Output Pins

The ACMFI2 pin configuration is listed in Table 31.1.

Table 31.1 Pin Configuration

Name	Function	I/O	Description
MEMC_CS0	Asynchronous interface chip select	Input	Chip select input to the ACMFI2 in asynchronous transfer.
MEMC_CS1	Synchronous interface chip select	Input	Chip select input to the ACMFI2 in synchronous transfer.
MEMC_BUSCLK	Synchronous interface input clock	Input	Clock input to the ACMFI2 in synchronous transfer.
MEMC_ADV	Address valid	Input	Address-valid input to the ACMFI2 in both synchronous and asynchronous transfer.
MEMC_NWE	Write strobe	Input	Write strobe input to the ACMFI2 in both synchronous and asynchronous transfer.
MEMC_NOE	Read strobe	Input	Read strobe input to the ACMFI2 in both synchronous and asynchronous transfer.
MEMC_AD15-AD0	Address/Data	I/O	Address/Data multiplex input-output in both synchronous and asynchronous transfer.
MEMC_WAIT	Access wait	Output	The Access wait output for a synchronous interface.
MEMC_INT	Interrupt	Output	Interrupt request to external device from the ACMFI2. (Low Active signal)

31.3 Register Descriptions

Table 31.2 shows the ACMFI2 register configuration of access from on-chip CPU. Table 31.3 shows the ACMFI2 register configuration of access from external device. Moreover, Table 31.4 shows the state of register in each operating mode.

Table 31.2 Register Configuration of access from on-chip CPU

Register Name	Abbreviation	R/W	Address	Access Size
ACMFI general status register	ACMFIGSR	R/W	H'E6B80000	32
ACMFI semaphore register	ACMFISM4	R/W	H'E6B80004	32
ACMFI internal interrupt control register	ACMFIIICR	R/W	H'E6B80008	32
ACMFI external interrupt control register 0	ACMFIEICR0	R/W	H'E6B8000C	32
ACMFI indirect access control register	ACMFIIDACR	R	H'E6B80010	32
ACMFI indirect access address register	ACMFIIDAA	R	H'E6B80014	32
ACMFI indirect access data register	ACMFIIDAD	R	H'E6B80018	32
(Reserve)		R	H'E6B8001C	32
ACMFI synchronous transfer control register	ACMFISYNC	R	H'E6B80020	32
ACMFI synchronous transfer address register	ACMFISYNCA	R	H'E6B80024	32
ACMFI synchronous transfer status register	ACMFISYNCS	R	H'E6B80028	32
ACMFI synchronous transfer status mask register	ACMFISYNCMASK	R/W	H'E6B8002C	32
ACMFI address protection register	ACMFIPTCR	R/W	H'E6B80030	32
ACMFI protection error address register	ACMFIPTCERA	R	H'E6B80034	32
ACMFRAM protection register	ACRAMPTCR	R/W	H'E6B80038	32
ACMFI external interrupt control register 1	ACMFIEICR1	R/W	H'E6B8003C	32
ACMFI internal RAM	ACMFRAM	R/W	H'E6B90000 to H'E6B9FFFF	32, 16, 8

Table 31.3 Register Configuration of access from external device

Register Name	Abbreviation	R/W	Address(*)	Access Size
ACMFI general status register	ACMFIGSR	R/W	H'00000	16
ACMFI semaphore register	ACMFISM4	R/W	H'00004	16
ACMFI internal interrupt control register	ACMFIIICR	R/W	H'00008	16
ACMFI external interrupt control register 0	ACMFIEICR0	R/W	H'0000C	16
ACMFI indirect access control register	ACMFIIDACR	R/W	H'00010	16
ACMFI indirect access address register	ACMFIIDAA	R/W	H'00014	16
ACMFI indirect access data register	ACMFIIDAD	R/W	H'00018	16
(Reserve)		R	H'0001C	16
ACMFI synchronous transfer control register	ACMFISYNC	R/W	H'00020	16
ACMFI synchronous transfer address register	ACMFISYNCA	R/W	H'00024	16
ACMFI synchronous transfer status register	ACMFISYNCS	R/W	H'00028	16
ACMFI synchronous transfer status mask register	ACMFISYNCMASK	R/W	H'0002C	16
ACMFI address protection register	ACMFIPTCR	R	H'00030	16
ACMFI protection error address register	ACMFIPTCERA	R	H'00034	16
ACMFRAM protection register	ACRAMPTCR	R	H'00038	16
ACMFI external interrupt control register 1	ACMFIEICR1	R/W	H'0003C	16
ACMFI internal RAM	ACMFRAM	R/W	H'10000 to H'1 FFFF	16

[Note] * Access from external device to the above-mentioned register group is possible only in case of asynchronous access (MEMC_CS0 use). Note that the external input address is 2-byte boundary. 1bit right shift of the above-mentioned address is fundamentally equivalent to the external address PIN. An example is indicated below.

(Example)

Access destination register (internal address)	Access bit	MEMC_AD[15:0] (external pin)
ACMFIPTCERA(H'0000034)	Bit15-0	b'0000000000011010
ACMFIPTCERA(H'0000034)	Bit31-16	b'0000000000011011
ACMFRAM(H'0010008)	Bit15-0	b'1000000000000100

Table 31.4 Register States in Each Operating Mode

Register Abbreviation	Power-On Reset	Power down of A4S area
ACMFIGSR	Initialized	Initialized
ACMFISM4	Initialized	Retained
ACMFIIICR	Initialized	Initialized
ACMFIEICR0	Initialized	Initialized
ACMFIIDACR	Initialized	Initialized
ACMFIIDAA	Initialized	Initialized
ACMFIIDAD	Initialized	Initialized
ACMFISYNC	Initialized	Retained
ACMFISYNCA	Initialized	Retained
ACMFISYNCS	Initialized	Initialized
ACMFISYNCMASK	Initialized	Retained
ACMFIPTCR	Initialized	Retained
ACMFIPTCERA	Initialized	Initialized
ACRAMPTCR	Initialized	Retained
ACMFIEICR1	Initialized	Retained
ACMFRAM	Undefined	Undefined

31.3.1 ACMFI General Status Register (ACMFIGSR)

ACMFIGSR can be freely used for mutual display of status between external device connected to the ACMFI2 and on-chip CPU.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	STATUS[15:0]															
Initial:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 0	STATUS[15:0]	All 0	R/W	General Status These bits can be read and written by the software of external device connected to the ACMFI2, and by on-chip CPU. Except upon a reset, they are never overwritten by hardware.

31.3.2 ACMFI Semaphore Register (ACMFISM4)

ACMFISM4 is a dedicated register allowing read modify write to be performed from external device connected to the ACMFI2 and from on-chip CPU. Using ACMFISM4 as a semaphore can improve the data transfer efficiency.

When the bits SM[1:0] = 00 is read, software can learn the successful acquisition.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	SM[1:0]		INF[7:0]							
Initial:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 8	SM[1:0]	00	R/W	Bits for Semaphore If these bits are “00”, reading to this register reads “01” (read from external device connected to ACMFI2) or “10” (read from on-chip CPU). The read value means a value before the change. The change is made only when “00” is read. As for these bits, only writing “00” is possible. When values other than “00” are written, the value does not change. It is possible to write this register by the following condition. 00 : Only reading from both external device and on-chip CPU is possible. 01 : Reading/writing from the external device is possible, and only reading is possible from on-chip CPU. 10 : Only reading is possible from the external device, reading/writing from on-chip CPU is possible. 11 : Setting prohibited.
7 to 0	INF[7:0]	All 0	R/W	Bits for Information Reading/writing is allowed according to the semaphore conditions of bits SM[1:0]. These bits are usually used as information.

[Note] If reading from external device and on-chip CPU simultaneously occurs for ACMFISM4 with the bits SM[1:0] = “00”, ACMFISM4 returns data of the bits SM[1:0] = “01” to on-chip CPU, while returns “00” to external device.

31.3.3 ACMFI Internal Interrupt Control Register (ACMFIIICR)

ACMFIIICR is used to issue interrupts from external device connected to the ACMFI2 to on-chip CPU.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	IIC[6:0]							IIR
Initial:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 1	IIC[6:0]	All 0	R/W	Internal Interrupt Source Bits used to specify the source for interrupts generated by the IIR. These bits can be written from both external device and on-chip CPU. By using these bits, fast execution of an interrupt handler is possible. These bits are completely under software control, and their values have no effect on the operation of the LSI.
0	IIR	0	R/W	Internal Interrupt Request While this bit is “1”, an interrupt request is issued to on-chip CPU.

31.3.4 ACMFI External Interrupt Control Register 0（ACMFIEICR0）

ACMFIEICR0 is used to issue interrupts from on-chip CPU to external device connected to the ACMFI2.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ERR3	ERR2	ERR1	ERR0	-	-	-	-	EIC[6:0]							EIR
Initial:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	ERR3	0	R	Internal Bus Error Interrupt Notification This bit is set to “1” when an error occurs in this LSI internal bus during access to this LSI via ACMFI2. This bit is cleared by setting SRST of ACMFISYNCS to “1”. This bit cannot be cleared by on-chip CPU.
14	ERR2	0	R	Synchronous Transfer Write Error Interrupt Notification This bit is set to “1” when a synchronous transfer write is issued in the unexpected access size. This bit is cleared by setting SRST of ACMFISYNCS to “1”. This bit cannot be cleared by on-chip CPU.
13	ERR1	0	R	ACMFRAM Access Error Interrupt Notification This bit is set to “1” when access to the access protection area in ACRAMPTCR occurs. This bit is cleared by setting ERST of ACRAMPTCR to “1”. This bit cannot be cleared by on-chip CPU.
12	ERR0	0	R	Access Error Interrupt Notification This bit is set to “1” when access to the access protection area in ACMFIPTCR occurs. This bit is cleared by setting ERST of ACMFIPTCR to “1”. This bit cannot be cleared by on-chip CPU.
11 to 8	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 1	EIC[6:0]	All 0	R/W	External Interrupt Source These bits are used to specify the source for interrupts generated by the EIR. These bits can be written from both external device and on-chip CPU. By using these bits, fast execution of interrupt handler is possible. These bits are completely under software control, and their values have no effect on the operation of the LSI.
0	EIR	0	R/W	External Interrupt Request While this bit is “1”, the MEMC_INT pin is asserted and an interrupt request is issued to the external device from this LSI.

31.3.5 ACMFI Indirect Access Control Register (ACMFIIDACR)

ACMFIIDACR is used when access to the internal registers of this LSI by using this register, ACMFIDAA and ACMFIDAD.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	AERR	-	-	-	-	-	-	RWT	-	-	-	RRD	-	-	SZ[1:0]	
Initial:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R/W	R	R	R	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial	R/W	Description
31 to 16	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	AERR	0	R/W	Address Error This bit is set to “1” when the value set in the ADR bits is not consistent with the register access size. Read/write operation is canceled when an address error occurs. <Read> 0 : With No Error 1 : Error Occurred <Write> 0 : Clears the Error 1 : Retains the previous value
14 to 9	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	RWT	0	R/W	Register Write Write “1” to this bit when writing to the register. When writing to the register is completed, this bit is cleared to “0”.
7 to 5	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	RRD	0	R/W	Register Read Write “1” to this bit when reading from the register. When reading from the register is completed, this bit is cleared to “0”.
3 to 2	-	0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial	R/W	Description
1 to 0	SZ[1:0]	All 0	R/W	Register Access Size These bits specify the access size for reading from/writing to the register. 00 : Byte 01 : Word 10 : Long-Word 11 : Setting prohibited

[Note] This register can be read and written by external device via ACMFI2. It cannot be written though can be read by the on-chip CPU.

31.3.6 ACMFI Indirect Access Address Register (ACMFIIDAA)

ACMFIIDAA is used to store an accessed address, when accessing to the register in this LSI via the register of ACMFI2.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ADR[31:16]															
Initial:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ADR[15:0]															
Initial:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Vale	R/W	Description
31 to 0	ADR[31:0]	All 0	R/W	Address The accessed address in accessing registers of this LSI via the register of ACMFI2 is specified.

[Note] This register can be read and written by external device via ACMFI2. It cannot be written though can be read by the on-chip CPU.

31.3.7 ACMFI Indirect Access Data Register (ACMFIIDAD)

ACMFIIDAD is used when access to the internal registers of this LSI. ACMFIDAD is used to hold data read from and written to register which are accessed by external device.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DATA[31:16]															
Initial:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[15:0]															
Initial:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Vale	R/W	Description
31 to 0	DATA[31:0]	All 0	R/W	Data In case of accessing to the register in this LSI via ACMFI2 registers, the write data is stored in this register in writing, and the read data is stored in reading.

[Note] This register can be read and written by external device via ACMFI2. It cannot be written though can be read by the on-chip CPU.

31.3.8 ACMFI Synchronous Transfer Control Register (ACMFISYNC)

ACMFISYNC is used to specify the function setting associated with the synchronous transfer.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	RDW	-	-	WTW[1:0]	
Initial:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	INCS[1:0]		-	-	-	-	RDO[1:0]		-	-	WDO[1:0]		-	WBV
Initial:	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R	R	R	R/W	R/W	R	R	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	RDW	0	R/W	Read Data Wait (Refer to 31.4.4(6) for details) 0 : Read data output no delay (Default) 1 : Read data output 1cycle delay mode
19 to 18	-	00	R	Reserved These bits are always read as 0. The write value should always be 0.
17 to 16	WTW[1:0]	00	R/W	Write Data Wait (Refer to 31.4.4(6) for details) 00 : Write Data input no delay (Default) 01 : Write Data input 1cycle delay mode 10 : Write Data input 2cycle delay mode 11 : Write Data input 3cycle delay mode
15 to 14	-	00	R	Reserved These bits are always read as 0. The write value should always be 0.
13 to 12	INCS[1:0]	00	R/W	Address Auto Increment Mode (Refer to 31.4.4(4) for details) 00:Address auto increment mode OFF 01:16Byte address auto increment mode ON 10:32Byte address auto increment mode ON 11 : Setting prohibited
11 to 10	-	00	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 8	-	11	R	Reserved These bits are always read as 1. The write value should always be 1.

Bit	Bit Name	Initial Value	R/W	Description
7 to 6	RDO[1:0]	00	R/W	Read Data Swapping 00 : No swapping 01 : Byte-wise swapping 10 : Word-wise swapping 11 : Both byte-wise and word-wise swapping
5 to 4	-	00	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 2	WDO[1:0]	00	R/W	Write Data Swapping 00 : No swapping 01 : Byte-wise swapping 10 : Word-wise swapping 11 : Both byte-wise and word-wise swapping
1	-	0	R	Reserved This bit is always read as 0. The write value should always be 0.
0	WBV	0	R	Indicates whether or not data remains in the write buffer. 0 : No data remains in the write buffer (the write operation complete). 1 : Data remains in the write buffer (the write operation is in progress).

[Note] Rewriting the value of this register during synchronous transfer is prohibited. Operation is not guaranteed if the value is rewritten.

Before rewriting the bits of ACMFISYNC, check to ensure that the WBV bit is “0”.

31.3.9 ACMFI Synchronous Transfer Address Register (ACMFISYNCA)

ACMFISYNCA is a register which can complement the access address in synchronous transfer.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SYNCA[14:0]															-
Initial:	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	SYNCA[14:0]	H'2000	R/W	Offset Address Set the higher-order address bits [31:17] for use in synchronous transfer, i.e. specify the area for access. The initial value is SDRAM space.
16 to 0	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

[Note] Rewriting the value of this register during synchronous transfer is prohibited. Operation is not guaranteed if the value is rewritten.

Before rewriting the bits of ACMFISYNC, check to ensure that the WBV bit is "0".

31.3.10 ACMFI Synchronous Transfer Status Register (ACMFISYNCS)

ACMFISYNCS is a register which stores the status in using synchronous interface. (Indirect access in asynchronous interface is included)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	SRST
Initial:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	INCRERR	INCWERR	-	-	-	BERR	-	-	WERR1	WERR0
Initial:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	SRST	0	W	Status Reset 0 : Invalid setting 1 : Status reset (ACMFISYNCS[15:0] are all cleared and ACMFIEICR0[15:14] are cleared.)
15 to 10	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	INCRERR	0	R	Address Increment Read Error This bit is set to “1” when an illegal synchronous read is issued when value of INCS[1:0](ACMFISYNC) is “01” or “10”.
8	INCWERR	0	R	Address Increment Write Error This bit is set to “1” when an illegal synchronous write is issued when value of INCS[1:0](ACMFISYNC) is “01” or “10”.
7 to 5	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	BERR	0	R	Internal Bus Error This bit is set to “1” when an internal bus error occurs.
3 to 2	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	WERR1	0	R	Write Access Size Over Error This bit is set to “1” when larger access than 2-burst access size (4byte) occurs in a synchronous write.

Bit	Bit Name	Initial Value	R/W	Description
0	WERR0	0	R	Write Access Size Under Error This bit is set to "1" when smaller access than 2-burst access size (4byte) occurs in a synchronous write.

31.3.11 ACMFI Synchronous Transfer Status Mask Register (ACMFISYNCMASK)

ACMFISYNCMASK is a register which external interrupt by error bit of ACMFISYNCS masked is possible. (Except BERR bit of ACMFISYNCS)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	MSK3	MSK2	-	-	-	-	-	-	MSK1	MSK0
Initial:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	MSK3	0	R/W	Address Increment Read Error Mask When this bit is set to "1", external interrupt by INCRERR bit of ACMFISYNCS is masked.
8	MSK2	0	R/W	Address Increment Write Error Mask When this bit is set to "1", external interrupt by INCWERR bit of ACMFISYNCS is masked.
7 to 2	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	MSK1	0	R/W	Write Access Size Over Error Mask When this bit is set to "1", external interrupt by WERR1 bit of ACMFISYNCS is masked.
0	MSK0	0	R/W	Write Access Size Under Error Mask When this bit is set to "1", external interrupt by WERR0 bit of ACMFISYNCS is masked.

31.3.12 ACMFI Address Protection Register (ACMFIPTCR)

ACMFIPTCR is a register which restrict access area in access from external device to inside of this LSI. In case of access to restricted area, the access becomes invalid.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PTCERR	-	ERST	ETC	-	-	PT4	-	-	-	-	-	-	-	PT1	PT0
Initial:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	W	R/W	R	R	R/W	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	PTCERR	0	R	Protection Error 0 : No error 1 : Error (Access to protection area)
14	-	0	R	Reserved This bit is always read as 0. The write value should always be 0.
13	ERST	0	W	Error Log Reset (Refer to 31.4.4(5) for details) 0 : Invalid setting 1 : Clears the error log
12	ETC	0	R/W	Other Area Protection All access restrictions are performed except area of PT0, PT1 and PT4 in this register. 0 : No access permitted 1 : Access permitted
11 to 10	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	PT4	0	R/W	CPG and SYSC Area Protection 0 : No access permitted 1 : Access permitted
8 to 2	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	PT1	0	R/W	BSC Area Protection 0 : No access permitted 1 : Access permitted

Bit	Bit Name	Initial Value	R/W	Description
0	PT0	0	R/W	SDRAM Area Protection 0 : No access permitted 1 : Access permitted

[Note] This register can be read and written by on-chip CUP. It cannot be written though can be read by external device via ACMFI2. Exceptionally, only ERST bit can be written by external device via ACMFI2.

31.3.13 ACMFI Protection Error Address Register (ACMFIPTCERA)

ACMFIPTCERA is a register to store the invalid accessed address when accessing to restricted area.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ERRADR[31:16]															
Initial:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ERRADR[15:0]															
Initial:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	ERRADR[31:0]	All 0	R	Error Address Log Error address is stored in this register when accessing to protection area.

31.3.14 ACMFRAM Protection Register (ACRAMPTCR)

ACRAMPTCR is a register to restrict access by every 8KB for ACMFRAM area when accessing from external device to ACMFRAM. In case of access to the restrict area, this access becomes invalid.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RAMERRADR[15:0]															
Initial:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ERR	-	-	ERST	-	-	-	-	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0
Initial:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	RAMERRADR [15:0]	All 0	R	ACMFRAM Error Address Log Error Address is stored in these bits when accessing to protection area of ACMFRAM.
15	ERR	0	R	ACMFRAM Protection Error 0 : No error 1 : Error (access to protection area of ACMFRAM)
14 to 13	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	ERST	0	W	Error Log Reset (Refer to 31.4.4(5) for details) 0 : Invalid setting 1 : Clears the error log
11 to 8	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	AR7	0	R/W	ACMFRAM Protection Area 7 (address : H'E000 to H'FFFF) 0 : No access permitted 1 : Access permitted
6	AR6	0	R/W	ACMFRAM Protection Area 6 (address : H'C000 to H'DFFF) 0 : No access permitted 1 : Access permitted
5	AR5	0	R/W	ACMFRAM Protection Area 5 (address : H'A000 to H'BFFF) 0 : No access permitted 1 : Access permitted

Bit	Bit Name	Initial Value	R/W	Description
4	AR4	0	R/W	ACMFRAM Protection Area 4 (address : H'8000 to H'9FFF) 0 : No access permitted 1 : Access permitted
3	AR3	0	R/W	ACMFRAM Protection Area 3 (address : H'6000 to H'8FFF) 0 : No access permitted 1 : Access permitted
2	AR2	0	R/W	ACMFRAM Protection Area 2 (address : H'4000 to H'5FFF) 0 : No access permitted 1 : Access permitted
1	AR1	0	R/W	ACMFRAM Protection Area 1 (address : H'2000 to H'3FFF) 0 : No access permitted 1 : Access permitted
0	AR0	0	R/W	ACMFRAM Protection Area 0 (address : H'0000 to H'1FFF) 0 : No access permitted 1 : Access permitted

[Note] This register can be read and written by on-chip CUP. It cannot be written though can be read by external device via ACMFI2. Exceptionally, only ERST bit can be written by external device via ACMFI2.

31.3.15 ACMFI External Interrupt Control Register 1 (ACMFIEICR1)

ACMFIEICR1 is a register which interrupt notified external device can be notified also to on-chip CUP. And this register can prevent external interrupt by hardware source.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EMSK3	EMSK2	EMSK1	EMSK0	-	-	-	-	-	-	-	-	-	-	-	CINT
Initial:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
15	EMSK3	0	R/W	External Interrupt Mask by ERR3 bit of ACMFIEICR0 0 : No masked 1 : Masks
14	EMSK2	0	R/W	External Interrupt Mask by ERR2 bit of ACMFIEICR0 0 : No masked 1 : Masks
13	EMSK1	0	R/W	External Interrupt Mask by ERR1 bit of ACMFIEICR0 0 : No masked 1 : Masks
12	EMSK0	0	R/W	External Interrupt Mask by ERR0 bit of ACMFIEICR0 0 : No masked 1 : Masks
11 to 1	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	CINT	0	R/W	External Interrupt Control When this bit is set to “1”, external interrupt transferred to MEMC_INT pin is also informed to on-chip CPU.

31.4 Operation

31.4.1 Access to ACMFI2 Registers

External access method which can access to ACMFI2 registers is an access only via asynchronous interface with MEMC_CS0. Please note that access to ACMFI2 registers via synchronous interface with MEMC_CS1 is invalid.

31.4.2 Memory Map

The memory space of on-chip ACMFRAM is shown in Table 31.5.

Table 31.5 ACMFI2 memory map

	Start address	End address	Memory size	Classification
Via ACMFI2 (external device)	H'10000	H'1FFFF	64K bytes	On-chip ACMFRAM area
Via on-chip CPU (this LSI)	H'E6B90000	H'E6B9FFFF	64K bytes	

31.4.3 Access to Internal Registers of this LSI via ACMFI2

By using this function, on-chip peripheral module registers can be directly accessed via asynchronous interface with MEMC_CS0. Write to and read from registers with the following procedures.

(1) Register Write Operation

1. Set the address of the register to be written to ACMFIIDAA.
2. Set the data of the register to be written to ACMFIIDAD.
3. Write access to the address set to ACMFIIDAA with the data set to ACMFIIDAD is executed by setting these SZ bits in ACMFIIDACR to access size and by setting the RWT bit in ACMFIIDACR to “1”. (Check the AERR bit in ACMFIIDACR is not set to “1”)
4. When the write operation is completed, the RWT bit is automatically cleared to “0”.

(2) Register Read Operation

1. Set the address of the register to be read to ACMFIIDAA.
2. Read access from the address set to ACMFIDAA is executed by setting these SZ bits in ACMFIIDACR to access size and by setting the RRD bit in ACMFIIDACR to “1”. (Check the AERR bit in ACMFIIDACR is not set to “1”)
3. When the read operation is completed, the RRD bit is automatically cleared to “0” and read data is stored in ACMFIIDAD.

When you access this LSI via ACMFI2 registers as mentioned above, please start these operations after checking that the WBV bit in ACMFISYNC is “0”.

31.4.4 Synchronous Transfer Mode

This function makes direct addressing and high-speed access to the memory device connected to this LSI via ACMFI2 by the synchronous interface.

(1) SDRAM Access

SDRAM connected to this LSI can be accessed in a direct address with the synchronous interface. Details are shown below.

- No limitation applies to the burst length. Write/read is executed until CS is negated.
- We recommended the 32-byte boundaries for burst access.
- Write/read buffers are incorporated in ACMFI2 and high-speed burst access is possible.

The higher-order address bits [31:17] for use in SDRAM access are provided by ACMFISYNCA. Please check the WBV bit in ACMFISYNC is “0” when you change the complemented address. (Refer to (3) Higher-order address change flow for details)

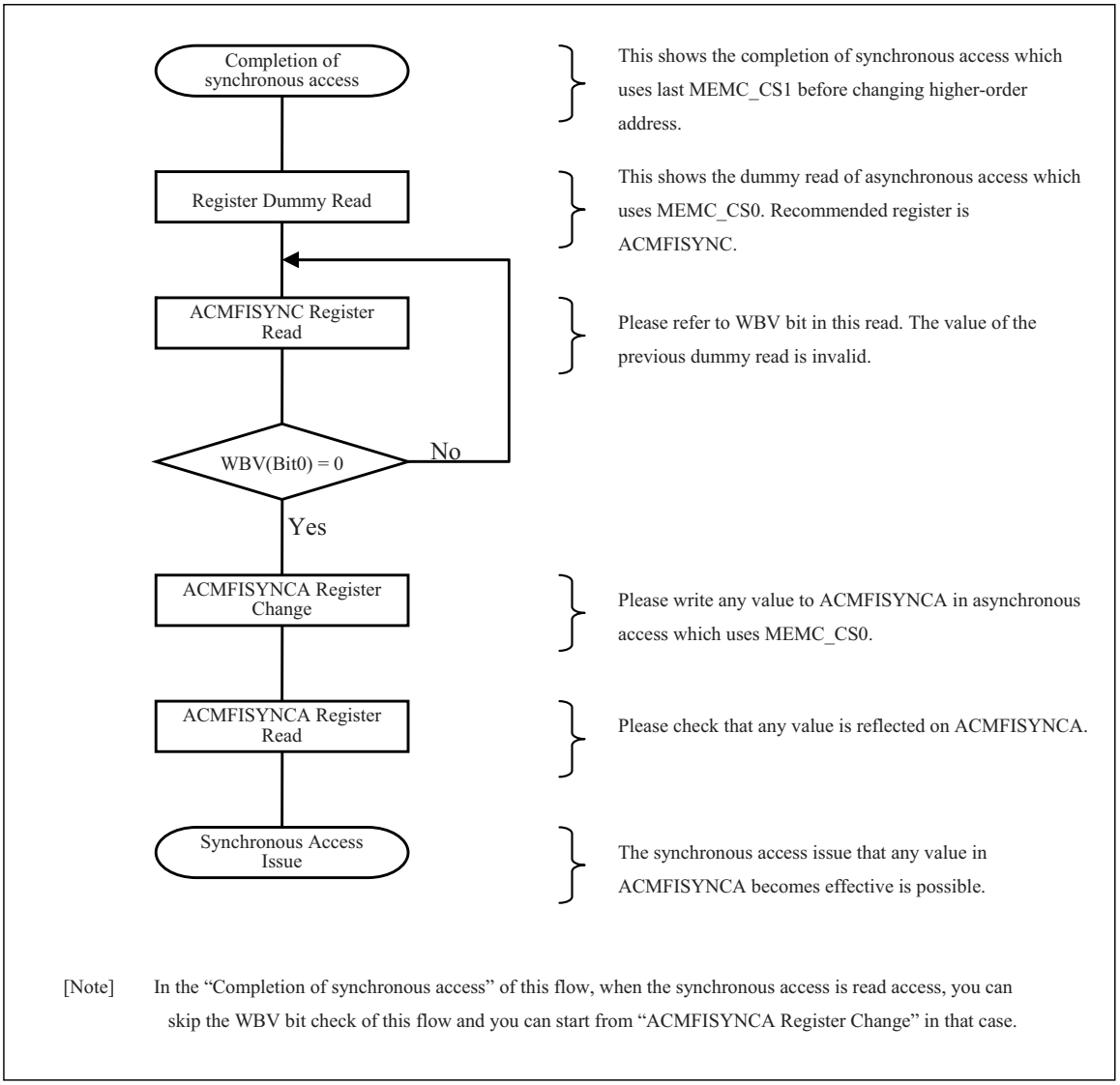
(2) Peripheral Module Access

Access to peripheral modules in this LSI is possible by using the synchronous interface. When you access to peripheral modules, please make sure of 4byte (2-burst) access. When access size is not 4Byte, operation is not guaranteed.

As SDRAM Access, the higher-order address bits [31:17] for use in SDRAM access are provided by ACMFISYNCA. Please check the WBV bit in ACMFISYNC is “0” when you change the complemented address. (Refer to (3) Higher-order address change flow for details)

(3) Higher-order Address Change Flow

ACMFI2 provides the function which complements higher-order address with ACMFISYNCA in the synchronous access. This function is available by the following flow.



[Note] In the “Completion of synchronous access” of this flow, when the synchronous access is read access, you can skip the WBV bit check of this flow and you can start from “ACMFISYNCA Register Change” in that case.

Figure 31.2 Higher-order address change flow

(4) Address Auto Increment Mode

Details of INCS[1:0] bits in ACMFISYNC are shown below.

[1] Automatic increment object area

Basically, only SDRAM area is an automatic increment object area.

[2] 16-byte/32-byte boundary increment setting

Please issue the 8-burst access (16byte) in the synchronous interface when INCS[1:0] bits are “01”. And only 16-byte boundary address must issue, and the access must issue continuous. When unexpected access is issued, MEMC_INT is asserted by internal error. The operation is not guaranteed at this time.

Also, please issue the 16-burst access (32byte) in the synchronous interface when INCS[1:0] bits are “10”. And only 32-byte boundary address must issue, and the access must issue continuous.

[3] Automatic address increment setting flow

Please set it according to the same procedure as “Higher-order Address Change Flow”. The mark of “ACMFISYNCA Register” in Fig.31.2 is replaced with “ACMFISYNC Register” and please refers.

[4] Notes

When the address increment setting is valid, SYNC[14:0] bits in ACMFISYNCA is changed for auto increment value. If you issue the access to other target in synchronous interface, please set ACMFISYNCA to higher-order address of the target after completion of auto increment access

(5) Error Reset Function

Details of ERST bit in ACMFIPTCR and ERST bit in ACRAMPTCR are shown below.

[1] About object of clear bits when ERST bit in ACMFIPTCR is set to “1”

Register Name. Bit Name	When the on-chip CPU writes "1" to ERST		When the external device writes "1" to ERST	
	Read from on-chip CPU	Read from external device	Read from on-chip CPU	Read from external device
ACMFIEICR0. ERR0	X	X	O	O
ACMFIPTCR. PTCERR	O	O	X	O
ACMFIPTCERA. ERRADR	X	X	O	O

[Note] “O” in above-mentioned table shows that it is cleared and “X” in above-mentioned table shows that it is not cleared.

[2] About object of clear bits when ERST bit in ACRAMPTCR is set to “1”

Register Name. Bit Name	When the on-chip CPU writes "1" to ERST		When the external device writes "1" to ERST	
	Read from on-chip CPU	Read from external device	Read from on-chip CPU	Read from external device
ACMFIEICR0. ERR1	X	X	O	O
ACRAMPTCR. ERR	O	X	X	O
ACRAMPTCR. RAMERRADR	X	X	O	O

[Note] “O” in above-mentioned table shows that it is cleared and “X” in above-mentioned table shows that it is not cleared.

(6) Variable Timing of Input/Output Data in Synchronous Interface

Details of RDW bit and WTD[1:0] bits in ACMFISYNC are shown below.

[1] About WTD[1:0] bits setting

The cycle time from MEMC_WAIT negate output timing to input write data can be changed by changing these bits.

Details of timing are shown below for every setting.

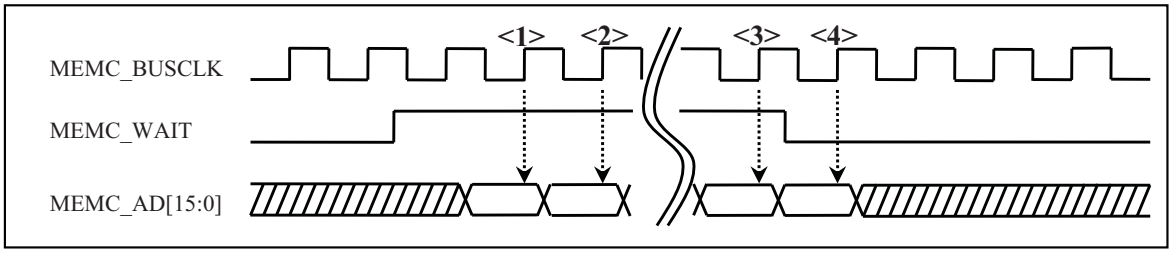


Figure 31.3 Valid timing of write data when WTD[1:0] bits in ACMFISYNC is “00”

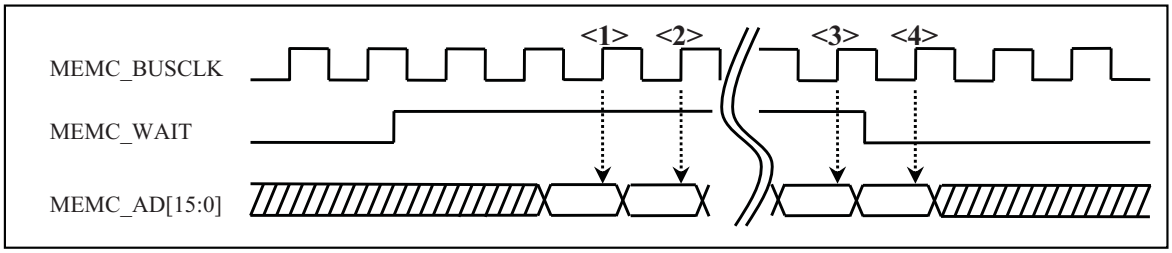


Figure 31.4 Valid timing of write data when WTD[1:0] bits in ACMFISYNC is “01”

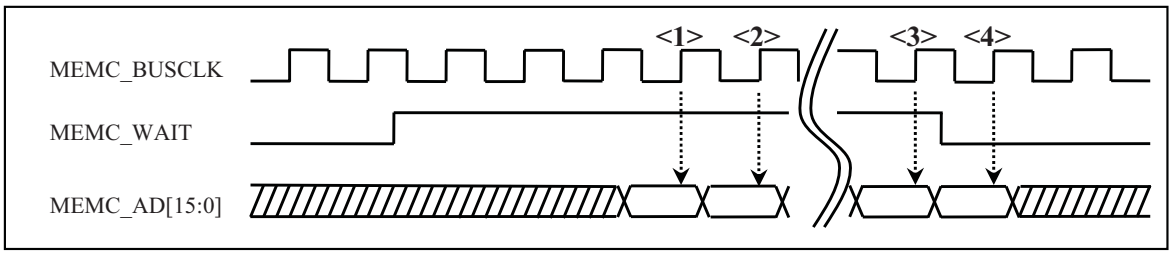


Figure 31.5 Valid timing of write data when WTD[1:0] bits in ACMFISYNC is “10”

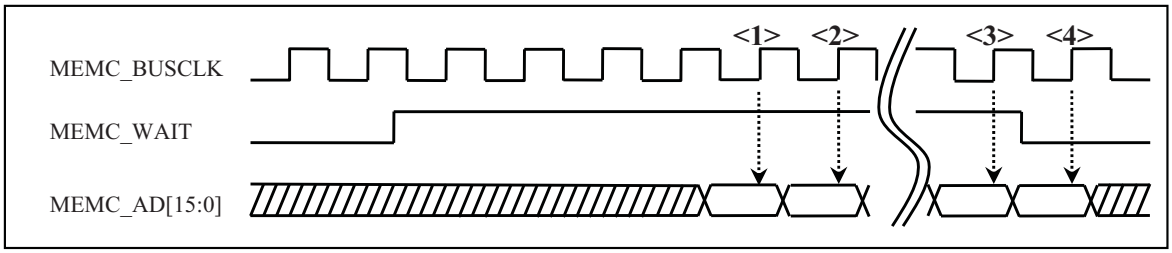


Figure 31.6 Valid timing of write data when WTD[1:0] bits in ACMFISYNC is “11”

• ”<1>” in the above figure is shown clock edge which retrieves the first write data after MEMC_WAIT negated, and “<2>” is shown the next write data. “<3>” and “<4>” is clock edge which retrieves the write data at MEMC_WAIT

asserted, and this timing is basically invariable at MEMC_WAIT asserted.

[2] About RDW bit setting

The cycle time from MEMC_WAIT negate output timing to output read data can be changed by setting "1" to this bit. Details of timing are shown below for every setting.

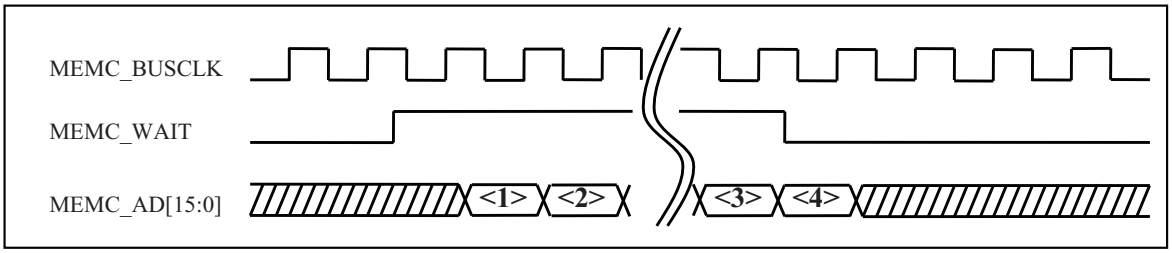


Figure 31.7 Valid timing of read data when RDW bit in ACMFISYNC is "0"

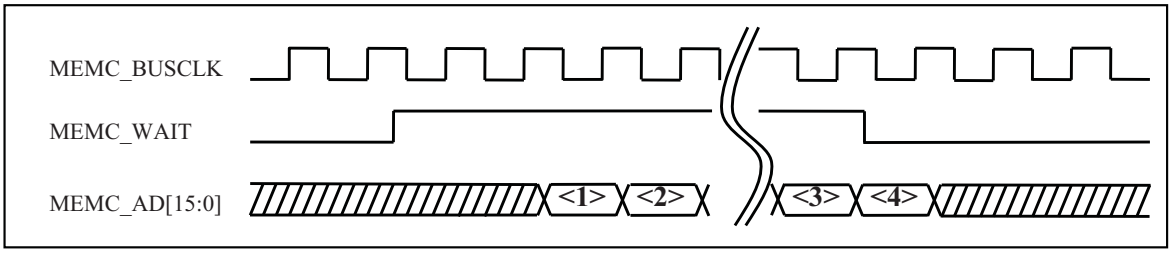


Figure 31.8 Valid timing of read data when RDW bit in ACMFISYNC is "1"

- "<1>" in the above figure is shown the first valid read data after MEMC_WAIT negated, and "<2>" is the next valid read data. "<3>" and "<4>" are the valid data output at MEMC_WIAT asserted, and this output timing is invariable at MEMC_WAIT asserted.

[3] Input/output data timing setting flow

Please set it according to the same procedure as "Higher-order Address Change Flow". The mark of "ACMFISYNCA Register" in Fig.31.2 is replaced with "ACMFISYNC Register" and please refers.

31.5 Interface

The parallel interface with ACMFI2 is described. ACMFI2 interface supports asynchronous interface and synchronous interface with MEMC_BUSCLK.

31.5.1 Asynchronous Interface

The basic write sequence of the asynchronous interface is shown in Fig.31.9 and the basic read sequence of the asynchronous interface shown in Fig.31.10. The Address/data multiplex is applied and the external address is 2-byte boundary.

Please refer to [***AC Characteristic] for detailed timing.

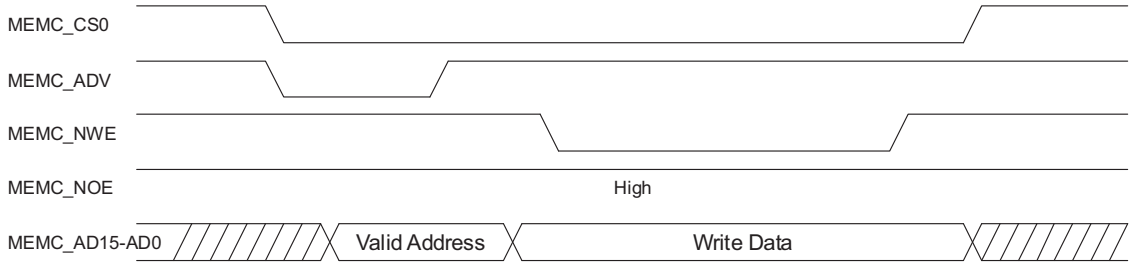


Figure 31.9 Write basic timing of asynchronous interface

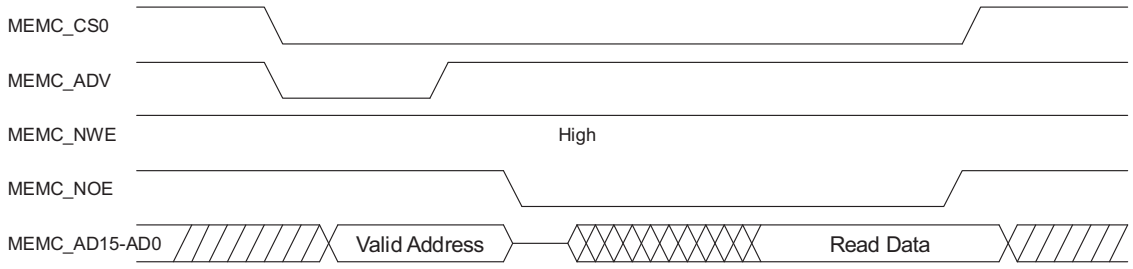


Figure 31.10 Read basic timing of asynchronous interface

31.5.2 Synchronous Interface

The basic write sequence of the synchronous interface is shown in Fig.31.11 and the basic read sequence of the synchronous interface shown in Fig.31.12. The Address/data multiplex is applied and the external address is 2-byte boundary.

Please refer to [***AC Characteristic] for detailed timing.

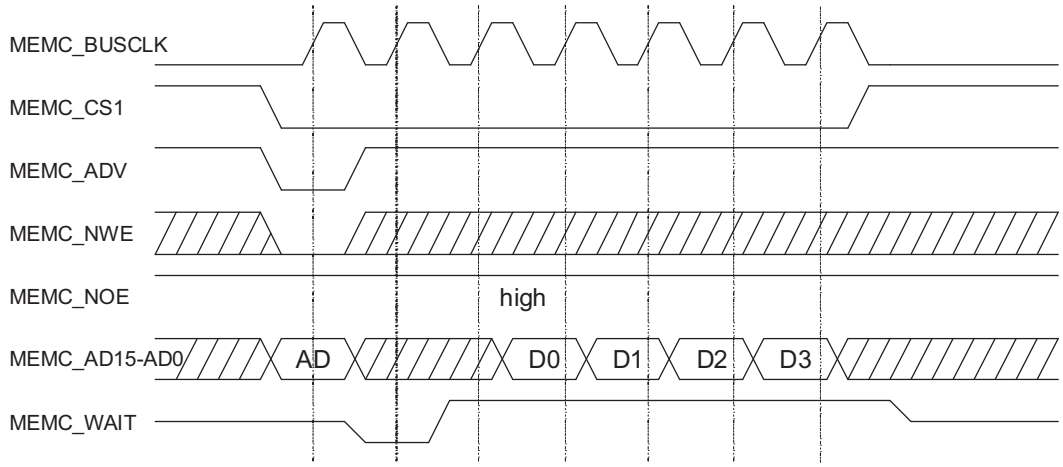


Figure 31.11 Write basic timing of synchronous interface

[Note] The asserting period of MEMC_WAIT is not constant and figure above is example.

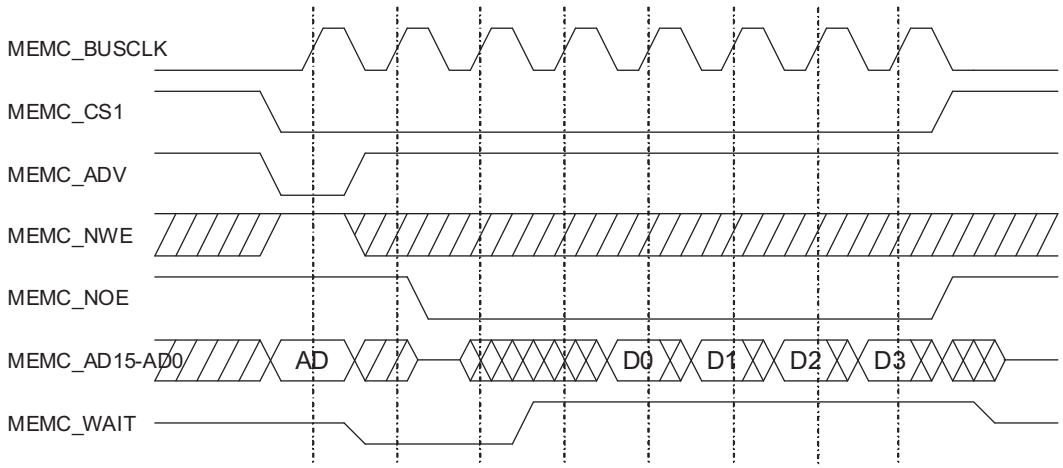


Figure 31.12 Read basic timing of synchronous interface

[Note] The asserting period of MEMC_WAIT is not constant and figure above is example.

The long burst (64bytes) write sequence is shown in Fig.31.13 and the long burst (64bytes) read sequence is shown in Fig.31.14. Continuous access is applied in long burst access, and address is incremented automatically, and access is continued while MEMC_CS1 is asserted. In the following figure, address of the burst access is issued by 32-byte boundary.

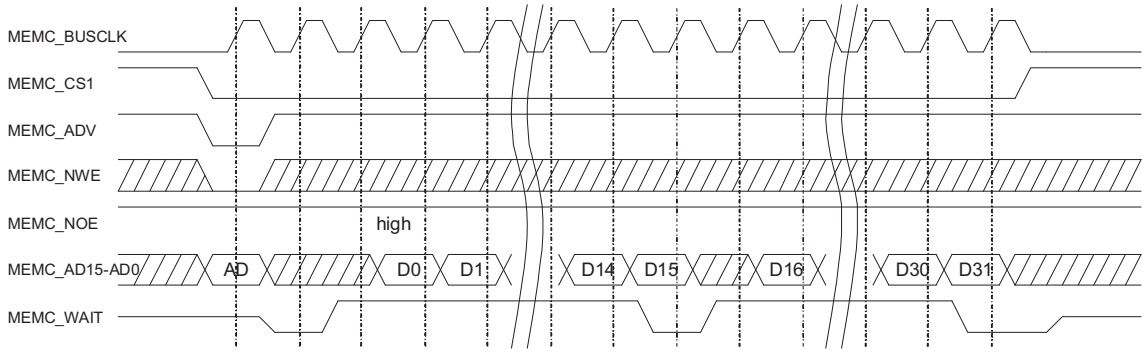


Figure 31.13 64byte-burst write timing of synchronous interface

[Note] The asserting period of MEMC_WAIT is not constant. One or more cycles of MEMC_WAIT is asserted by every 32byte write.

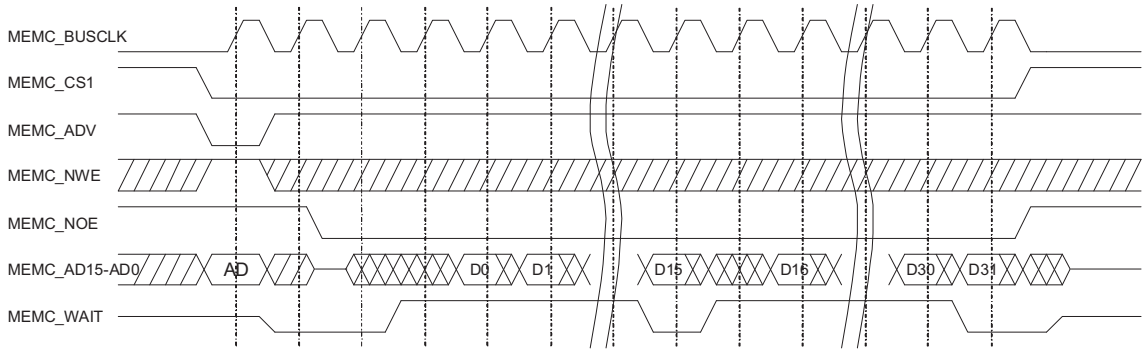


Figure 31.14 64byte-burst read timing of synchronous interface

[Note] The asserting period of MEMC_WAIT is not constant. One or more cycles of MEMC_WAIT is asserted by every 32byte write.

Section 32 USB High-Speed 0 Module (USBHS0)

This module is a USB controller provided with the USB host controller function and the function controller function. When the host controller function is selected, high-speed transfer, full-speed transfer, and low-speed transfer conforming to the USB (universal serial bus) Specification 2.0 are available. When the function controller function is selected, high-speed transfer and full-speed transfer are available. Provided with an on-chip USB transceiver, this module also supports all transfer types defined by the USB Specification.

This module can use up to ten pipes with an on-chip 16-Kbyte buffer memory for data transfer. Furthermore, for pipes 1 to 9, arbitrary endpoint numbers can be allocated according to peripheral devices to be communicated and user systems.

32.1 Features

(1) Incorporates a host controller and a function controller conforming to USB High Speed.

- On-chip USB host controller and function controller
- The USB host controller function and the function controller function are selectable by register setting.
- On-chip USB transceiver

(2) Achieves space-saving mount with less external elements.

- Direct connection of the VBUS0_0 and VBUS1_0 signal to the input pin of this module
- On-chip D+ pull-up resistor (function operation mode)
- On-chip D+/D- pull-down resistors (host operation mode)
- On-chip D+/D- terminating resistors (high-speed operation mode)
- On-chip D+/D- output resistors (full-speed operation mode)

(3) Supports all data transfer types for USB communication.

- Control transfer
- Bulk transfer
- Interrupt transfer (except for high bandwidth)
- Isochronous transfer (except for high bandwidth)

(4) Dedicated DMA interface

- On-chip 2-channel DMA interface

(5) Pipe configuration

- On-chip 16-Kbyte buffer memory for USB communication
- Up to ten pipes are selectable (including the default control pipe)
- Programmable pipe configuration
- Arbitrary endpoint numbers can be allocated to pipes 1 to 9.
- Settable transfer conditions for each pipe are as follows:

  Pipe 0: A pipe only for control transfer with a 64-byte (fixed) single buffer

  Pipes 1 and 2: Pipes that can select bulk transfer or isochronous transfer (Continuous transfer mode and buffer size are programmable.) (Double buffer can be specified with up to 2 Kbytes.)

  Pipes 3 to 5: Pipes only for bulk transfer (Continuous transfer mode and buffer size are programmable.) (Double buffer can be specified with up to 2 Kbytes.)

  Pipes 6 to 9: Pipes only for interrupt transfer with a 64-byte (fixed) single buffer

(6) Features with host controller function

- Supports high-speed transfer (480 Mbps), full-speed transfer (12 Mbps), and low-speed transfer (1.5 Mbps).
- Allows communication with multiple peripheral devices through a hub.
- Reset handshake auto-response
- Automated SOF/packet transmission schedule
- Isochronous transfer/interrupt transfer interval setting function

(7) Features with function controller function

- Supports high-speed transfer (480 Mbps) and full-speed transfer (12 Mbps).
- High-speed or full-speed automatic recognition of operation using the reset handshake auto-response function
- Control transfer stage management function
- Device state management function
- Auto-response to the SET_ADDRESS request
- NAK response interrupt function (NRDY)
- SOF interpolation function

(8) Other functions

- Transfer terminating function using transaction count
- SOF pulse output function
- BRDY interrupt event notification timing change function (BFRE)
- Buffer memory auto-clear function (DCLRM) after reading data of the pipe specified by the DnFIFO (n = 0, 1) port
- NAK setting function (SHTNAK) for the response PID due to the transfer end
- Supports data line pulsing as an OTG function.
- Supports the MAX3355E (OTG external device) interface.

32.2 Input/Output Pins

Table 32.1 lists the input and output pins of the USB.

Table 32.1 Pin Configuration of USB

Classification	Pin Name	Name	I/O	Description
USB bus interface	DP_0	USB D+ data	I/O	D+ Input/output of the On-chip Transceiver Connect this pin to the D+ pin of the USB bus.
	DM_0	USB D- data	I/O	D- Input/output of the On-chip Transceiver Connect this pin to the D- pin of the USB bus.
VBUS monitoring input	VBUS0_0	VBUS input 0	Input	USB Cable Connection Monitoring Pin For link. Connect this pin directly to VBUS of the USB bus. This pin is used to detect VBUS connection or disconnection. When not connecting to VBUS of the USB 0 bus, fix this pin to +5V. Also supply +5V to this pin when the host controller function is selected. However, VBUS cannot be supplied to devices to be connected.
	VBUS1_0	VBUS input 1	Input	USB Cable Connection Monitoring Pin for PHY. Connect this pin directly to VBUS of the USB bus. This pin is used to detect VBUS connection or disconnection. When not connecting to VBUS of the USB 0 bus, fix this pin to +5V. Also supply +5V to this pin when the host controller function is selected. However, VBUS cannot be supplied to devices to be connected.
Reference resistance	REFRIN_0	Reference input	Input	Reference Resistance Connecting Pin Connect this pin to the ground through a 5.6 kΩ ±1% resistor.

Classification	Pin Name	Name	I/O	Description
OTG external device interface	PWEN_0	Power enable	Output	VBUS0_0 and VBUS1_0 Supply ON/OFF Control Pin When using MAX3355E as an OTG external device, connect this pin directly to the OFFVBUS0_0 and VBUS1_0 pin of the MAX3355E.
	EXTLP_0	OTG external device low power	Output	External Device Power Shutdown Control Pin When using MAX3355E as an OTG external device, connect this pin directly to the SHDN pin of the MAX3355E.
	OVCN_0	Overcurrent detection	Input	Overcurrent Status Monitoring Pin When using MAX3355E as an OTG external device, connect this pin directly to the STATUS1 pin of the MAX3355E.
	OVCN2_0	Overcurrent detection 2	Input	Overcurrent Status Monitoring Pin When using MAX3355E as an OTG external device, connect this pin directly to the STATUS2 pin of the MAX3355E.
	IDIN_0	Device ID	Input	Device ID Monitoring Pin When using MAX3355E as an OTG external device, connect this pin directly to the ID_OUT pin of the MAX3355E.

32.3 Register Descriptions

Table 32.2 lists the registers used in this module. Table 32.3 list the register states in each processing mode.

Table 32.2 Register Configuration

Register Name	Abbreviation	R/W	Address	Access Size
System configuration control register	SYSCFG	R/W	H'E689 0000	16
CPU bus wait register	BUSWAIT	R/W	H'E689 0002	16
System configuration status register	SYSSTS	R	H'E689 0004	16
Device state control register	DVSTCTR	R/W	H'E689 0008	16
Test mode register	TESTMODE	R/W	H'E689 000C	16
CFIFO port register	CFIFO	R/W	H'E689 0014	32
CFIFO port select register	CFIFOSEL	R/W	H'E689 0020	16
CFIFO port control register	CFIFOCTR	R/W	H'E689 0022	16
D0FIFO port select register	D0FIFOSEL	R/W	H'E689 0028	16
D0FIFO port control register	D0FIFOCTR	R/W	H'E689 002A	16
D1FIFO port select register	D1FIFOSEL	R/W	H'E689 002C	16
D1FIFO port control register	D1FIFOCTR	R/W	H'E689 002E	16
Interrupt enable register 0	INTENB0	R/W	H'E689 0030	16
Interrupt enable register 1	INTENB1	R/W	H'E689 0032	16
BRDY interrupt enable register	BRDYENB	R/W	H'E689 0036	16
NRDY interrupt enable register	NRDYENB	R/W	H'E689 0038	16
BEMP interrupt enable register	BEMPENB	R/W	H'E689 003A	16
SOF output configuration register	SOFCFG	R/W	H'E689 003C	16
Interrupt status register 0	INTSTS0	R/W	H'E689 0040	16
Interrupt status register 1	INTSTS1	R/W	H'E689 0042	16
BRDY interrupt status register	BRDYSTS	R/W	H'E689 0046	16
NRDY interrupt status register	NRDYSTS	R/W	H'E689 0048	16
BEMP interrupt status register	BEMPSTS	R/W	H'E689 004A	16
Frame number register	FRMNUM	R/W	H'E689 004C	16
μ frame number register	UFRMNUM	R/W	H'E689 004E	16
USB address register	USBADDR	R	H'E689 0050	16

Register Name	Abbreviation	R/W	Address	Access Size
USB request type register	USBREQ	R	H'E689 0054	16
USB request value register	USBVAL	R	H'E689 0056	16
USB request index register	USBINDX	R	H'E689 0058	16
USB request length register	USBLENG	R	H'E689 005A	16
DCP configuration register	DCPCFG	R/W	H'E689 005C	16
DCP maximum packet size register	DCPMAXP	R/W	H'E689 005E	16
DCP control register	DCPCTR	R/W	H'E689 0060	16
Pipe window select register	PIPESEL	R/W	H'E689 0064	16
Pipe configuration register	PIPECFG	R/W	H'E689 0068	16
Pipe buffer register	PIPEBUF	R/W	H'E689 006A	16
Pipe maximum packet size register	PIPEMAXP	R/W	H'E689 006C	16
Pipe cycle control register	PIPEPERI	R/W	H'E689 006E	16
Pipe 1 control register	PIPE1CTR	R/W	H'E689 0070	16
Pipe 2 control register	PIPE2CTR	R/W	H'E689 0072	16
Pipe 3 control register	PIPE3CTR	R/W	H'E689 0074	16
Pipe 4 control register	PIPE4CTR	R/W	H'E689 0076	16
Pipe 5 control register	PIPE5CTR	R/W	H'E689 0078	16
Pipe 6 control register	PIPE6CTR	R/W	H'E689 007A	16
Pipe 7 control register	PIPE7CTR	R/W	H'E689 007C	16
Pipe 8 control register	PIPE8CTR	R/W	H'E689 007E	16
Pipe 9 control register	PIPE9CTR	R/W	H'E689 0080	16
Pipe 1 transaction counter enable register	PIPE1TRE	R/W	H'E689 0090	16
Pipe 1 transaction counter register	PIPE1TRN	R/W	H'E689 0092	16
Pipe 2 transaction counter enable register	PIPE2TRE	R/W	H'E689 0094	16
Pipe 2 transaction counter register	PIPE2TRN	R/W	H'E689 0096	16
Pipe 3 transaction counter enable register	PIPE3TRE	R/W	H'E689 0098	16
Pipe 3 transaction counter register	PIPE3TRN	R/W	H'E689 009A	16
Pipe 4 transaction counter enable register	PIPE4TRE	R/W	H'E689 009C	16
Pipe 4 transaction counter register	PIPE4TRN	R/W	H'E689 009E	16
Pipe 5 transaction counter enable register	PIPE5TRE	R/W	H'E689 00A0	16
Pipe 5 transaction counter register	PIPE5TRN	R/W	H'E689 00A2	16

Register Name	Abbreviation	R/W	Address	Access Size
Device address 0 configuration register	DEVADD0	R/W	H'E689 00D0	16
Device address 1 configuration register	DEVADD1	R/W	H'E689 00D2	16
Device address 2 configuration register	DEVADD2	R/W	H'E689 00D4	16
Device address 3 configuration register	DEVADD3	R/W	H'E689 00D6	16
Device address 4 configuration register	DEVADD4	R/W	H'E689 00D8	16
Device address 5 configuration register	DEVADD5	R/W	H'E689 00DA	16
Device address 6 configuration register	DEVADD6	R/W	H'E689 00DC	16
Device address 7 configuration register	DEVADD7	R/W	H'E689 00DE	16
Device address 8 configuration register	DEVADD8	R/W	H'E689 00E0	16
Device address 9 configuration register	DEVADD9	R/W	H'E689 00E2	16
Device address A configuration register	DEVADDA	R/W	H'E689 00E4	16

Table 32.3 Register States in Each Processing Mode

Register Abbreviation	Power-On Reset	Software Standby	Module Standby	Sleep
SYSCFG	Initialized	Retained	Retained	Retained
BUSWAIT	Initialized	Retained	Retained	Retained
SYSSTS	Initialized	Retained	Retained	Retained
DVSTCTR	Initialized	Retained	Retained	Retained
TESTMODE	Initialized	Retained	Retained	Retained
CFIFO	Initialized	Retained	Retained	Retained
CFIFOSEL	Initialized	Retained	Retained	Retained
CFIFOCTR	Initialized	Retained	Retained	Retained
D0FIFOSEL	Initialized	Retained	Retained	Retained
D0FIFOCTR	Initialized	Retained	Retained	Retained
D1FIFOSEL	Initialized	Retained	Retained	Retained
D1FIFOCTR	Initialized	Retained	Retained	Retained
INTENB0	Initialized	Retained	Retained	Retained
INTENB1	Initialized	Retained	Retained	Retained
BRDYENB	Initialized	Retained	Retained	Retained
NRDYENB	Initialized	Retained	Retained	Retained

Register Abbreviation	Power-On Reset	Software Standby	Module Standby	Sleep
BEMPENB	Initialized	Retained	Retained	Retained
SOFCFG	Initialized	Retained	Retained	Retained
INTSTS0	Initialized	Retained	Retained	Retained
INTSTS1	Initialized	Retained	Retained	Retained
BRDYSTS	Initialized	Retained	Retained	Retained
NRDYSTS	Initialized	Retained	Retained	Retained
BEMPSTS	Initialized	Retained	Retained	Retained
FRMNUM	Initialized	Retained	Retained	Retained
UFRMNUM	Initialized	Retained	Retained	Retained
USBADDR	Initialized	Retained	Retained	Retained
USBREQ	Initialized	Retained	Retained	Retained
USBVAL	Initialized	Retained	Retained	Retained
USBINDX	Initialized	Retained	Retained	Retained
USBLENG	Initialized	Retained	Retained	Retained
DCPCFG	Initialized	Retained	Retained	Retained
DCPMAXP	Initialized	Retained	Retained	Retained
DCPCTR	Initialized	Retained	Retained	Retained
PIPESEL	Initialized	Retained	Retained	Retained
PIPECFG	Initialized	Retained	Retained	Retained
PIPEBUF	Initialized	Retained	Retained	Retained
PIPEMAXP	Initialized	Retained	Retained	Retained
PIPEPERI	Initialized	Retained	Retained	Retained
PIPE1CTR	Initialized	Retained	Retained	Retained
PIPE2CTR	Initialized	Retained	Retained	Retained
PIPE3CTR	Initialized	Retained	Retained	Retained
PIPE4CTR	Initialized	Retained	Retained	Retained
PIPE5CTR	Initialized	Retained	Retained	Retained
PIPE6CTR	Initialized	Retained	Retained	Retained
PIPE7CTR	Initialized	Retained	Retained	Retained
PIPE8CTR	Initialized	Retained	Retained	Retained
PIPE9CTR	Initialized	Retained	Retained	Retained

Register Abbreviation	Power-On Reset	Software Standby	Module Standby	Sleep
PIPE1TRE	Initialized	Retained	Retained	Retained
PIPE1TRN	Initialized	Retained	Retained	Retained
PIPE2TRE	Initialized	Retained	Retained	Retained
PIPE2TRN	Initialized	Retained	Retained	Retained
PIPE3TRE	Initialized	Retained	Retained	Retained
PIPE3TRN	Initialized	Retained	Retained	Retained
PIPE4TRE	Initialized	Retained	Retained	Retained
PIPE4TRN	Initialized	Retained	Retained	Retained
PIPE5TRE	Initialized	Retained	Retained	Retained
PIPE5TRN	Initialized	Retained	Retained	Retained
DEVADD0	Initialized	Retained	Retained	Retained
DEVADD1	Initialized	Retained	Retained	Retained
DEVADD2	Initialized	Retained	Retained	Retained
DEVADD3	Initialized	Retained	Retained	Retained
DEVADD4	Initialized	Retained	Retained	Retained
DEVADD5	Initialized	Retained	Retained	Retained
DEVADD6	Initialized	Retained	Retained	Retained
DEVADD7	Initialized	Retained	Retained	Retained
DEVADD8	Initialized	Retained	Retained	Retained
DEVADD9	Initialized	Retained	Retained	Retained
DEVADDA	Initialized	Retained	Retained	Retained

32.3.1 System Configuration Control Register (SYSCFG)

SYSCFG enables or disables high-speed operation, selects the host controller function or function controller function, controls DP_0 and DM_0 pins, and enables or disables the operation of this module.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	SCKE	—	—	HSE	DCFM	DRPD	DPRPU	—	—	—	USBE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R	R	R/W	R/W	R/W	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10	SCKE	0	R/W	USB Module Clock Enable Enables or halts the supply of the 48-MHz clock to this module. 0: The clock supply to the USB module is halted. 1: The clock supply to the USB module is enabled. When this bit is 0, only this register and BUSWAIT are readable and writable. Other registers in the USB module are readable but not writable.
9, 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
7	HSE	0	R/W	High-Speed Operation Enable 0: High-speed operation is disabled. When the function controller function is selected: Full-speed operation only When host controller function is selected: Full-speed or low-speed operation 1: High-speed operation is enabled. (This module detects the transmission rate.) (1) When the host controller function is selected When HSE is 0, the USB port performs low-speed or full-speed operation. If the USB detects that a low-speed peripheral device is attached to the USB port, be sure to set the HSE bit to 0. When HSE is 1, this module executes the reset handshake protocol, and according to the result, the USB port is automatically driven to high-speed or full-speed operation mode. Change this bit after the ATTCH interrupt is detected and before resetting the USB bus (before setting USBRESET to 1). (2) When the function controller function is selected When HSE is 0, this module performs full-speed operation. When HSE is 1, this module executes the reset handshake protocol, and according to the result, this module automatically performs high-speed or full-speed operation. Change this bit while the DPRPU bit is 0.
6	DCFM	0	R/W	Controller Function Select Selects the function of this module. 0: The function controller function is selected. 1: The host controller function is selected. Change this bit while the DPRPU and DRPD bits are 0. During the HNP processing, however, this bit can be set according to the processing sequence.

Bit	Bit Name	Initial Value	R/W	Description
5	DRPD	0	R/W	D+ Line/D- Line Resistance Control Enables or disables pull-down of the D+ and D- lines when the host controller function is selected. 0: Pull-down is disabled. 1: Pull-down is enabled. Set this bit to 1 when the host controller function is selected. During the HNP processing, however, this bit can be set according to the processing sequence. Set this bit to 0 when the function controller function is selected.
4	DPRPU	0	R/W	D+ Line Resistance Control Enables or disables pull-up of the D+ line when the function controller function is selected. 0: Pull-up is disabled. 1: Pull-up is enabled. When this bit is set to 1 with the function controller function selected, this module pulls up the D+ line at 3.3V, and informs the USB host of ATTACH. Clearing this bit to 0 cancels the pull-up of the D+ line, and informs the USB host of DETACH. Set this bit to 1 when the function controller function is selected. During the HNP processing, however, this bit can be set according to the processing sequence. Set this bit to 0 when the host controller function is selected.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
0	USBE	0	R/W	USB Module Operation Enable Enables or disables the USB module operation. 0: The USB module operation is disabled. 1: The USB module operation is enabled. Tables 32.4 and 32.5 list the registers and bit names initialized when this bit is cleared to 0. Change this bit while the SCKE bit is 1. When the host controller function is selected, set the DPRD bit to 1, eliminate chattering with the LNST bit, confirm that the USB bus is stable, and then set this bit to 1.

Table 32.4 Registers Initialized by Writing 0 in the USBE Bit (When the function controller function is selected)

Register Name	Bit Name	Remarks
SYSSTS	LNST	The value is retained when the host controller function is selected.
DVSTCTR	RHST	
INTSTS0	DVSQ	The value is retained when the host controller function is selected.
USBADDR	USBADDR	The value is retained when the host controller function is selected.
USEREQ	BRequest, bmRequestType	The value is retained when the host controller function is selected.
USBVAL	wValue	The value is retained when the host controller function is selected.
USBINDX	wIndex	The value is retained when the host controller function is selected.
USBLENG	wLength	The value is retained when the host controller function is selected.

Table 32.5 Registers Initialized by Writing 0 in the USBE Bit (When the host controller function is selected)

Register Name	Bit Name	Remarks
DVSTCTR	RHST	
FRMNUM	FRNM	The value is retained when the function controller function is selected.
UFRMNUM	UFRNM	The value is retained when the function controller function is selected.

32.3.2 CPU Bus Wait Register (BUSWAIT)

BUSWAIT specifies the number of access waits from the CPU to this module.

This register is writable even if the SCKE bit in SYSCFG is 0.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	BWAIT[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
3 to 0	BWAIT[3:0]	1111	R/W	CPU Bus Wait Specify the number of access waits to this module. 0000: 0 waits (2 access cycles) 0001: 1 wait (3 access cycles) 0010 to 1110: 2 to 14 waits (4 to 16 access cycles) 1111: 15 waits (17 access cycles) initial value The following restriction is provided for access cycles to the registers of addresses beginning with H'04 of this controller. Restriction for wait: The cycle of continuous accesses to the registers of this controller must be 80 ns or more. To satisfy this restriction, control waits using the frequency of system clock HPϕ. Choose the best value within the initial value of 17 clock cycles (maximum). This setting is the same as the waits in accesses to the FIFO port register. The maximum speed of accesses to the FIFO port is as follows: MBW = 10 (32-bit width) : Max. 48 Mbytes/s MBW = 01 (16-bit width) : Max. 24 Mbytes/s MBW = 00 (8-bit width) : Max. 12 Mbytes/s

32.3.3 System Configuration Status Register (SYSSTS)

SYSSTS monitors the USB data bus line status (D+ and D- lines).

This register is initialized by a power-on reset or a USB reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OVCMON[1:0]		—	—	—	—	—	—	—	HTACT	—	—	—	ID MON	LNST[1:0]	
Initial value:	—*	—*	0	0	0	1	0	0	0	0	0	0	0	—*	—*	—*
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15, 14	OVCMON [1:0]	Undefined*	R	OVCN_0/OVCN2_0 Pin Monitor Indicate the input state of the OVCN_0 and OVCN2_0 pins. 00: OVCN_0 = Low, OVCN2 = Low 01: OVCN_0 = Low, OVCN2 = High 10: OVCN_0 = High, OVCN2 = Low 11: OVCN_0 = High, OVCN2 = High Connection of an external device to the OVCN_0 and OVCN2 pins allows SRP as an OTG function.
13 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
9 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6	HTACT	0	R	Indicates that this module is processing when the host controller function is selected. 0: Idle state 1: Processing
5 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
2	IDMON	Undefined*	R	Indicates the input state of the IDIN pin. 0: IDIN = Low 1: IDIN = High Connection of an external device to the IDIN pin allows a device ID as an OTG function to be reflected in this bit.
1, 0	LNST[1:0]	Undefined*	R	USB Data Line Status Monitor Indicate the USB data bus line (D+ and D- lines) status. Table 32.6 shows the USB data bus line status. Read these bits after the attach processing (DPRPU = 1) when the function controller function is selected or read them after enabling pull-down of the D+ and D- lines (DRPD = 1) when the host controller function is selected.

Note: * These bits depend on the state of the DP_0, DM_0, OVCN_0, OVCN2, and IDIN pins.

Table 32.6 USB Data Bus Line Status

LNST[1]	LNST[0]	Low-Speed Operation (only when host controller function is selected)	Full-Speed Operation	High-Speed Operation	Chirp Operation
0	0	SE0	SE0	Squelch	Squelch
0	1	K-State	J-State	UnSquelch	Chirp J
1	0	J-State	K-State	Invalid	Chirp K
1	1	SE1	SE1	Invalid	Invalid

Legend:

Chirp: The reset handshake protocol (RHSP) is being executed with high-speed operation is enabled (HSE = 1 in SYSCFG).
Squelch: SE0 or idle state
UnSquelch: High-speed J-State or high-speed K-State
Chirp J: Chirp J-State
Chirp K: Chirp K-State
Invalid: Invalid

32.3.4 Device State Control Register (DVSTCTR)

DVSTCTR controls and monitors the USB data bus state.

This register is initialized by a power-on reset. The WKUP bit is initialized and the RESUME bit becomes undefined by a USB bus reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	HNP BTOA	EXT LP	PWEN	WKUP	RWU PE	USB RST	RES UME	UACT	—	RHST[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W*	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11	HNPBTOA	0	R/W	Switches HNP (Host Negotiation Protocol) From B (Device) to A (Host). This bit is used to switch the function controller function (device B) to the host controller function (device A) when the OTG uses the HNP. 0: Normal operation 1: Switching OTG B to A is enabled. When this bit is 1, the internal function controller remains suspended until the HNP processing finishes even when DPRPU = 0 or DCFM = 1. Furthermore, even if the falling edge of the D+ signal is detected, the resume (RESM) interrupt is not generated. When the HOST ATTACH (pull-up at the other side) is detected or the HNP processing timeout occurs, write 0 in this bit. Write 1 in this bit only in the suspended state with the function controller function selected.
10	EXTLP_0	0	R/W	Controls the EXTLP_0 pin output state. 0: EXTLP0 Low output 1: EXTLP0 High output
9	PWEN_0	0	R/W	Controls the PWEN_0 pin output state. 0: PWEN_0 Low output 1: PWEN_0 High output

Bit	Bit Name	Initial Value	R/W	Description
8	WKUP	0	R/W*	Wakeup Output Enables or disables the remote wakeup (resume signal output) to the USB bus when the function controller function is selected. 0: The remote wakeup signal is not output. 1: The remote wakeup signal is output. This module controls the remote wakeup signal output time. When this bit is set to 1, this module outputs 10 ms K-State and then clears this bit. The USB Specification requires the USB bus idle state to be maintained for at least 5 ms before transmitting the remote wakeup signal. For this reason, this module outputs K-State after waiting for 2 ms even if 1 is written in this bit immediately after the suspended state is detected. Write 1 in this bit only when the device is in the suspended state (DVSQ = 1xx in INTSTS0) and remote wakeup is enabled by the USB host. When setting this bit to 1, do not stop the internal clock even in the suspended state (Write 1 in this bit with SCKE set to 1). Write 0 in this bit when the host controller function is selected.
7	RWUPE	0	R/W	Wakeup Detection Enable Enables or disables remote wakeup (resume signal output) for the peripheral device of the down port when the host controller function is selected. 0: Remote wakeup output to the down port is disabled. 1: Remote wakeup output to the down port is enabled. When the remote wakeup signal is detected while this bit is 1, this module detects the resume signal (2.5 μs K-State) for the down port and performs resume processing to drive K-State. When this bit is set to 0, the remote wakeup signal (K-State) from the peripheral device connected to the selected port is ignored even if it is detected by this module. While this bit is 1, do not halt any internal clocks even in the suspended state (keep SCKE = 1). Also do not reset the USB bus from the suspended state by writing 1 in the USBRST bit. This is prohibited by USB Specification 2.0. Set this bit to 0 when the function controller function is selected.

Bit	Bit Name	Initial Value	R/W	Description
6	USBRST	0	R/W	Bus Reset Output Controls the USB bus reset signal output when the host controller function is selected. 0: The USB bus reset signal is not output. 1: The USB bus reset signal is output. When this bit is set to 1 with the host controller function selected, this module drives SE0 of the USB port to perform the USB bus reset processing. When the HSE bit is 1 at this time, this module executes the reset handshake protocol. While USBRST is 1 (until the software writes 0 in this bit), this module continues the SE0 output. Secure the time specified in the USB Specification 2.0 for the USB bus reset time period (USBRST = 1). If 1 is written in this bit during communication (UACT = 1) or during resume (RESUME = 1), this module does not reset the USB bus until the UACT and RESUME bits are cleared to 0. Immediately after this bit is cleared to cancel a USB bus reset, write 1 in the UACT bit. Set this bit to 0 when the function controller function is selected.
5	RESUME	0	R/W	Resume Output Controls the resume signal output when the host controller function is selected. 0: The resume signal is not output. 1: The resume signal is output. When this bit is set to 1, this module drives the port into K-State to output the resume signal. While RESUME is 1 (until the software writes 0 in this bit), this module continues the K-State output. Secure the time specified in the USB Specification 2.0 for the resume time period (RESUME = 1). Write 1 in this bit only in the suspended state. Immediately after this bit is cleared to cancel the resume, write 1 in the UACT bit. Set this bit to 0 when the function controller function is selected.

Bit	Bit Name	Initial Value	R/W	Description
4	UACT	0	R/W	USB Bus Enable Enables or disables the USB bus operation (output control of the SOF or μSOF packet to the USB bus) when the host controller function is selected. 0: Down port operation is disabled. (SOF/μSOF packets are not sent.) 1: Down port operation is enabled. (SOF/μSOF packets are sent.) When this bit is set to 1, this module drives the USB port into the USB bus enable state, sends the SOF packet, and performs data communication. The SOF or μSOF packet is sent within one (micro) frame time period after the software writes 1 in this bit. When this bit is set to 0, this module enters the idle state after the SOF or μSOF packet is sent. This module sets this bit to 0 in the following cases: When the DTCH interrupt is detected during communication (UACT = 1) When the EOFERR interrupt is detected during communication (UACT = 1) Write 1 in this bit at the end of USB reset processing (clearing the USBRST bit) or at the end of resume processing from the suspended state (clearing the RESUME bit). Set this bit to 0 when the function controller function is selected.
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
2 to 0	RHST[2:0]	000	R	Reset Handshake Indicate the reset handshake state. (1) When the host controller function is selected: 000: Transmission rate is undefined (when powered or not connected). 1xx: The reset handshake processing is in progress. 001: Low-speed connection 010: Full-speed connection 011: High-speed connection After the software writes 1 in USBRST, these bits become 100. When HSE is set to 1 for the port, these bits become 111 when this module detects ChirpK from the peripheral device. When the software writes 0 in USBRST of the selected port and this module finishes driving SE0, this module determines the value of the RHST bits. (2) When the function controller function is selected: 000: Transmission rate is undefined. 100: The reset handshake processing is in progress. 010: Full-speed connection 011: High-speed connection When this module detects a USB bus reset with the HSE bit set to 1 for the port, these bits become 100. After that, when this module outputs ChirpK and detects ChirpJK from the USB host three times, these bits become 011. Unless high-speed mode is fixed within 2.5 ms after the ChirpK output, these bits become 010. When this module detects a USB bus reset with the HSE bit set to 0 for the port, these bits become 010. When the RHST bits are fixed to 010 or 011 after this module detected a USB bus reset, the DVST interrupt occurs.

32.3.5 Test Mode Register (TESTMODE)

TESTMODE controls the USB test signal output in high-speed operation mode.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	UTST[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
7 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
3 to 0	UTST[3:0]	0000	R/W	Test Mode Table 32.7 shows the test mode operation of this module. Control the USB test signal output in high-speed operation mode. These bits are valid only in high-speed operation mode. Use this test mode when the RHST bits in DVSTCTR are 011. Since bit 3 (UTST3) of these bits depends on the DCFM bit (controller function select), set these bits according to the DCFM bit. Furthermore, after the test with these bits, cancel this test mode by a power-on reset. When the host controller function is selected: Set these bits after setting DRPD to 1. This module outputs waveforms to the USB port for which DRPD = 1 and UACT = 1 are set. This module also performs high-speed termination for the USB port. Set the UTST bits using the following steps. 1. System reset 2. Clock initiation 3. DCFM = 1, DPRD = 1 (Setting HSE to 1 is not needed.) 4. USBE = 1 5. Set the UTST bits to a value according to the test content. 6. Set the UACT bit to 1.

Bit	Bit Name	Initial Value	R/W	Description
3 to 0	UTST[3:0]	0000	R/W	Change the UTST bits using the following steps. 1. UACT = 0, USBE = 0 2. USBE = 1 3. Set the UTST bits to a value according to the test content. 4. Set the UACT bit to 1. When Test_SE0_NAK (1011) is set, this module does not output the SOF packet to the port for which UACT is set to 1. When Test_Force_Enable (1101) is set, this module outputs the SOF packet to the port for which UACT is set to 1. Furthermore in this test mode, even if this module detects a high-speed disconnection (DTCH interrupt), this module does not control the hardware related to the detection. Before setting the UTST bits, set the PID bit of all pipes to NAK. When performing normal USB communication after setting test mode, issue a system reset. When the function controller function is selected: Set these bits according to the SetFeature request from the USB host during high-speed communication. While these bits are 0001 to 0100, this module does not enter the suspended state.

Table 32.7 Test Mode Operation

	UTST Bits Setting	
Test Mode	**When function controller function is selected**	**When host controller function is selected**
Normal operation	0000	0000
Test_J	0001	1001
Test_K	0010	1010
Test_SE0_NAK	0011	1011
Test_Packet	0100	1100
Test_Force_Enable	—	1101
Reserved	0101 to 0111	1110 to 1111

32.3.6 CFIFO Port Register

CFIFO is a port register to read data from or write data to the FIFO buffer memory.

Each FIFO port consists of this register (CFIFO) for data read/write from/to the FIFO buffer memory, the select registers (CFIFOSEL, D0FIFOSEL, and D1FIFOSEL) to select pipes to be allocated to a FIFO port, and the control registers (CFIFOCTR, D0FIFOCTR, and D1FIFOCTR).

Each FIFO port provides the following features.

- Make accesses to the FIFO buffer for DCP through the CFIFO port.
- Make accesses to the FIFO buffer with DMA transfers through the DMAC module for USB high-speed only.
- When using a function specific to FIFO ports (DMA transfer function, etc.), the pipe number (selected pipe) specified by the CURPIPE bits cannot be changed.
- Register groups of a FIFO port do not affect other FIFO ports.
- Do not allocate the same pipe number to different FIFO ports.
- There are two FIFO buffer states where the access mastership is on the CPU side and on the SIE side. When the FIFO buffer access mastership is on the SIE side, the CPU cannot make an access to the FIFO buffer.

This register is initialized by a power-on reset.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	FIFOPORT[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FIFOPORT[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	FIFOPORT [31:0]	All 0	R/W	FIFO Port Read receive data from the FIFO buffer or write transmit data to the FIFO buffer using these bits. Access to this register is enabled only when the FRDY bit in each control register (CFIFOCTR, D0FIFOCTR, or D1FIFOCTR) is set to 1. Valid bits in this register vary with the value of the MBW bits. Table 32.8 shows the valid bits in this register.

Table 32.8 Operation of This Register when Accessed

Access Size	Bits 31 to 24	Bits 23 to 16	Bits 15 to 8	Bits 7 to 0
32 bits	N + 3 address	N + 2 address	N + 1 address	N + 0 address
16 bits	Write: Invalid, Read: Prohibited*		N + 1 address	N + 0 address
8 bits	Write: Invalid, Read: Prohibited*			N + 0 address

Note: * Reading an invalid register with word access or byte access is prohibited.

32.3.7 FIFO Port Select Registers (CFIFOSEL, D0FIFOSEL, D1FIFOSEL)

CFIFOSEL, D0FIFOSEL, and D1FIFOSEL select pipes to be allocated to FIFO ports and control accesses to each FIFO port.

Do not specify the same pipe number for the CURPIPE bits in CFIFOSEL, D0FIFOSEL, and D1FIFOSEL. When the CURPIPE bits in D0FIFOSEL and D1FIFOSEL are set to B'000, no pipe is specified.

Do not change any pipe number when DMA transfer is enabled.

This register is initialized by a power-on reset.

(1) CFIFOSEL

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RCNT	REW	—	—	MBW[1:0]		—	—	—	—	ISEL	—	CURPIPE[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R	R/W	R/W	R	R	R	R	R/W	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	RCNT	0	R/W	Read Count Mode Specifies read mode of the DTLN bits in CFIFOCTR. 0: Clears the DTLN bits after reading all receive data in the CFIFO (or after reading receive data of one side of the double buffer). 1: Counts down the DTLN bits at each reading of CFIFO receive data.
14	REW	0	R/W	Buffer Pointer Rewind Specifies whether to rewind the buffer pointer or not. 0: The buffer pointer is not rewound. 1: The buffer pointer is rewound. When the selected pipe is in the receive direction and this bit is set to 1 during FIFO buffer reading, the FIFO buffer can be read from the first data. (In the case of a double buffer, the first data of one side that is being read can be read again.) Do not set this bit to 1 concurrently with the CURPIPE setting change. Be sure to confirm that the FRDY bit is 1 when setting this bit to 1. To rewrite the FIFO buffer data from the first data for a pipe in the transmit direction, use the BCLR bit.
13, 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
11, 10	MBW[1:0]	00	R/W	CFIFO Port Access Bit Width Specify the bit width for accesses to the CFIFO port. 00: 8 bits 01: 16 bits 10: 32 bits 11: Setting prohibited When the selected pipe is in the receive direction and data read is started after these bits are set, do not change these bits until all data is completely read. When the selected pipe is in the receive direction, set the CURPIPE and MBW bits at the same time. When the selected pipe is in the transmit direction, no bit width can be changed (from 8 bits to 16/32 bits or from 16 bits to 32 bits) during data write to the buffer memory. When 8-bit width or 16-bit width is selected, data of odd bytes can also be written by controlling the byte access.
9 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	ISEL	0	R/W	CFIFO Port Access Direction when DCP is Selected 0: Buffer memory read is selected. 1: Buffer memory write is selected. To change this bit when the selected pipe is DCP, write 1 or 0 in this bit, read the value of this bit, confirm that the write value equals the read value, and then proceed with the next processing. If this bit is changed in the middle of access to the FIFO buffer, accesses made before that time are retained, the value of this bit is rewritten, and then further access is enabled. Set this bit concurrently with the CURPIPE bits.

Bit	Bit Name	Initial Value	R/W	Description
4	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
3 to 0	CURPIPE [3:0]	0000	R/W	CFIFO Port Access Pipe Select Set the number of pipe to be used for data read or write through the CFIFO port. 0000: DCP 0001: Pipe 1 0010: Pipe 2 0011: Pipe 3 0100: Pipe 4 0101: Pipe 5 0110: Pipe 6 0111: Pipe 7 1000: Pipe 8 1001: Pipe 9 Other than above: Setting prohibited To change these bits, write a value in these bits, read the value of these bits, confirm that the write value equals the read value, and then proceed with the next processing. Do not write the same pipe number in the CURPIPE bits in CFIFOSEL, D0FIFOSEL, and D1FIFOSEL. If these bits are changed in the middle of access to the FIFO buffer, accesses made before that time are retained, the value of these bits is rewritten, and then further access is enabled.

Note: * Only reading 0 is enabled.

(2) D0FIFOSEL, D1FIFOSEL

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RCNT	REW	DCLRM	DREQE	MBW[1:0]		—	—	DEZPM	—	—	—	CURPIPE[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W*	R/W	R/W	R/W	R/W	R	R	R/W	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	RCNT	0	R/W	Read Count Mode Specifies read mode of the DTLN bits in DnFIFOCTR. 0: Clears the DTLN bits after reading all receive data in the DnFIFO (or after reading receive data of one side of the double buffer). 1: Counts down the DTLN bits at each reading of DnFIFO receive data. When making an access to the DnFIFO with the BFRE bit set to 1, set this bit to 0.
14	REW	0	R/W*	Buffer Pointer Rewind Specifies whether to rewind the buffer pointer or not. 0: The buffer pointer is not rewound. 1: The buffer pointer is rewound. When the selected pipe is in the receive direction and this bit is set to 1 during FIFO buffer reading, the FIFO buffer can be read from the first data. (In the case of a double buffer, the first data of one side that is being read can be read again.) Do not set this bit to 1 concurrently with the CURPIPE setting change. Be sure to confirm that the FRDY bit is 1 when setting this bit to 1. When making an access to the DnFIFO with the BFRE bit set to 1, do not set this bit to 1 when the short packet data is completely read. To rewrite the FIFO buffer data from the first data for a pipe in the transmit direction, use the BCLR bit.

Bit	Bit Name	Initial Value	R/W	Description
13	DCLRM	0	R/W	Buffer Memory Auto-Clear Mode after Reading Data of Selected Pipe Enables or disables buffer memory auto-clear mode after reading data of the selected pipe. 0: Buffer memory auto-clear mode is disabled. 1: Buffer memory auto-clear mode is enabled. When this bit is 1 and a Zero-Length packet is received while the FIFO buffer allocated to the selected pipe is empty or when a short packet is received with the BFRE bit set to 1 and the packet data is completely read, this module performs buffer clear (BCLR = 1 processing) of the FIFO buffer. When using this module with the BRDYM bit set to 1, be sure to set this bit to 0.
12	DREQE	0	R/W	DMA Transfer Request Enable Enables or disables making a DMA transfer request. 0: DMA transfer request is disabled. 1: DMA transfer request is enabled. To enable a DMA transfer request, set the CURPIPE bits and then set this bit to 1. Set this bit to 0 before changing the CURPIPE setting.
11, 10	MBW[1:0]	00	R/W	FIFO Port Access Bit Width Specify the bit width for accesses to the DnFIFO port. 00: 8 bits 01: 16 bits 10: 32 bits 11: Setting prohibited When the selected pipe is in the receive direction and data read is started after these bits are set, do not change these bits until all data is completely read. When the selected pipe is in the receive direction, set the CURPIPE and MBW bits at the same time. When the selected pipe is in the transmit direction, no bit width can be changed (from 8 bits to 16/32 bits or from 16 bits to 32 bits) during data write to the buffer memory. When 8-bit width or 16-bit width is selected, data of odd bytes can also be written by controlling the byte access.

Bit	Bit Name	Initial Value	R/W	Description
9 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	DEZPM	0	R/W	DEZPM: Zero-Length Packet Addition Mode If the DMA transfer size that is set for the the USBHS-DMAC modules is an integral multiple of the maximum packet size, a null packet is added after all of the data has been sent. 0: Disables addition of packets. 1: Enables addition of packets. This bit is applied to pipes used to write to the FIFO buffer. DEZPM must be set before starting DMA transfers. If the DEZPM bit is set after DMA transfers complete, no null packets are added. Note : This mode depends on the buffer size(PIPEBUF.BUFSIZE[4:0]). A null packet is added after transferring data up to buffer size which is defined by PIPEBUF.BUFSIZE[4:0]. When transfer data size is over 2Kbytes, this mode must not be used because max size of buffer is 2Kbytes. In that case, please add the null packet by SW with BVAL bit of FIFO Port Control Registers.
6 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
3 to 0	CURPIPE [3:0]	0000	R/W	FIFO Port Access Pipe Select Set the number of pipe to be used for data read or write through the D0FIFO and D1FIFO ports. 0000: No pipe 0001: Pipe 1 0010: Pipe 2 0011: Pipe 3 0100: Pipe 4 0101: Pipe 5 0110: Pipe 6 0111: Pipe 7 1000: Pipe 8 1001: Pipe 9 Other than above: Setting prohibited To change these bits, write a value in these bits, read the value of these bits, confirm that the write value equals the read value, and then proceed with the next processing. Do not write the same pipe number in the CURPIPE bits in CFIFOSEL, D0FIFOSEL, and D1FIFOSEL. If these bits are changed in the middle of access to the FIFO buffer, accesses made before that time are retained, the value of these bits is rewritten, and then further access is enabled.

Note: * Only reading 0 is enabled.

32.3.8 FIFO Port Control Registers (CFIFOCTR, D0FIFOCTR, D1FIFOCTR)

CFIFOCTR, D0FIFOCTR, and D1FIFOCTR specify buffer memory write end and CPU buffer clear, as well as indicate whether the FIFO port is accessible or not. These registers correspond to each FIFO port.

These registers are initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BVAL	BCLR	FRDY	—	DTLN[11:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W*1	R/W*2	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	BVAL	0	R/W*1	Buffer Memory Enable Flag This flag is set to 1 upon completion of data write in the FIFO buffer of the CPU of the pipe selected by the CURPIPE bits. 0: Invalid 1: Write end When the selected pipe is in the transmit direction, set this bit to 1 in the following cases. This module sets the FIFO buffer of the CPU to the SIE side to enable data transmission. To send a short packet, set this bit to 1 upon completion of data write. To send a Zero-Length packet, set this bit to 1 before writing data to the FIFO buffer. For pipes of continuous transfer mode, set this bit to 1 after writing data that is a positive integer multiple of MaxPacketSize and less than the BufferSize value. When data with the size specified by MaxPacketSize is written to a pipe of continuous transfer mode, this module writes 1 in this bit and sets the FIFO buffer of the CPU to the SIE side to enable data transmission. Set this bit to 1 when this module shows FRDY = 1. When the selected pipe is in the receive direction, do not set this bit to 1.

Bit	Bit Name	Initial Value	R/W	Description
14	BCLR	0	R/W*[2]	CPU buffer clear Clears the CPU side FIFO buffer of the selected pipe. 0: Invalid 1: Clears the CPU side FIFO buffer. When the FIFO buffer assigned to the selected pipe is set to a double buffer, and even when both sides of the buffer are readable, this module clears only one side of the FIFO buffer. When the selected pipe is DCP, this module clears the FIFO buffer when this bit is set to 1 irrespective of whether the FIFO buffer is on the CPU side or SIE side. When clearing the SIE side FIFO buffer, be sure to set the PID bits in DCP to NAK and then set the BCLR bit to 1. When the selected pipe is in the transmit direction, and if 1 is written in the BVAL and BCLR bits at the same time, this module clears the previously written data, and makes a Zero-Length packet transmittable. When the selected pipe is not DCP, write 1 in this bit while the FRDY flag indicates 1.
13	FRDY	0	R	FIFO Port Ready Indicates whether the CPU (DMAC) can access the FIFO port. 0: The FIFO port is not accessible. 1: The FIFO port is accessible. This module indicates FRDY = 1 in the following cases. However, since there is no data to read, no data can be read from the FIFO port. In these cases, set the BCLR bit to 1 to clear the FIFO buffer to make transmission/reception of the next data available. When a Zero-Length packet is received with the FIFO buffer assigned to the selected pipe empty When a short packet is received with BFRE set to 1 and the packet data is completely read
12	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
11 to 0	DTLN[11:0]	H'000	R	Receive Data Length Indicate the receive data length. The value of these bits during FIFO buffer reading varies as follows depending on the setting of the RCNT bit. When RCNT = 0: This module indicates the reecive data length with these bits until the CPU (DMAC) finishes reading one side of the FIFO buffer. When BFRE is 1, this module retains the reecive data length until the BCLR bit is set to 1 after the FIFO buffer read is completed. When RCNT = 1: This module decrements the value of the DTLN bits in each read cycle (-1 when MBW = 0, and -2 when MBW = 1) When reading out from a single FIFO buffer is complete, DTLN = 0 for this module. However, the behavior is different when double-buffering has been specified. If reading out of data from one side is not finished before the other side is full of received data, when all data have been read out from the first side, the DTLN bits reflect the amount of data received in the other side. When reading these bits during FIFO buffer reading while the RCNT bit is 1, note that this module updates the value in these bits within 150 ns after each FIFO port read cycle.

Notes: 1. Only writing 1 is enabled.
2. Only reading 0 and writing 1 are enabled.

32.3.9 Interrupt Enable Register 0 (INTENB0)

INTENB0 specifies masking of each interrupt. When this module detects an interrupt for which 1 is written in the corresponding bit in this register by the software, this module generates a USB interrupt.

When interrupt source detection conditions are satisfied irrespective of the register setting (interrupt enable/disable), this module sets the corresponding status bit in INTSTS0 to 1.

When the software changes an interrupt enable bit (0 to 1) whose interrupt source status bit in INTSTS0 is set to 1, this module generates a USB interrupt.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VBSE	RSME	SOFE	DVSE	CTRE	BEMPE	NRDYE	BRDYE	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	VBSE	0	R/W	VBUS0_0 and VBUS1_0 Interrupt Enable Enables or disables USB interrupt outputs when the VBINT interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
14	RSME	0	R/W	Resume Interrupt Enable Enables or disables USB interrupt outputs when the RESM interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
13	SOFE	0	R/W	Frame Number Update Interrupt Enable Enables or disables USB interrupt outputs when the SOFR interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

Bit	Bit Name	Initial Value	R/W	Description
12	DVSE	0	R/W	Device State Transition Interrupt Enable* Enables or disables USB interrupt outputs when the DVST interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
11	CTRE	0	R/W	Control Transfer Stage Transition Interrupt Enable* Enables or disables USB interrupt outputs when the CTRT interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
10	BEMPE	0	R/W	Buffer Empty Interrupt Enable Enables or disables USB interrupt outputs when the BEMP interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
9	NRDYE	0	R/W	Buffer Not Ready Response Interrupt Enable Enables or disables USB interrupt outputs when the NRDY interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
8	BRDYE	0	R/W	Buffer Ready Interrupt Enable Enables or disables USB interrupt outputs when the BRDY interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Note: * The RSME, DVSE, and CTRE bits can be set to 1 only when the function controller function is selected. Do not enable interrupts of these bits when the host controller function is selected.

32.3.10 Interrupt Enable Register 1 (INTENB1)

INTENB1 specifies masking of each interrupt when the host controller function is selected. When this module detects an interrupt for which 1 is written in the corresponding bit in this register by the software, this module generates a USB interrupt.

When interrupt source detection conditions are satisfied irrespective of the register setting (interrupt enable/disable), this module sets the corresponding status bit in INTSTS1 to 1.

When the software changes an interrupt enable bit (0 to 1) whose interrupt source status bit in INTSTS1 is set to 1, this module outputs a USB interrupt.

When the function controller function is selected, do not allow any interrupt.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OVRCRE	BCHGE	—	DTCHE	ATTCHE	—	—	—	—	EOFERRE	SIGNE	SACKE	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	OVRCRE	0	R/W	OVRCR Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
14	BCHGE	0	R/W	USB Bus Change Interrupt Enable Enables or disables USB interrupt outputs when the BCHG interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
13	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
12	DTCHE	0	R/W	Disconnection Detect Interrupt Enable Enables or disables USB interrupt outputs when the DTCH interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

Bit	Bit Name	Initial Value	R/W	Description
11	ATTCHE	0	R/W	Connection Detect Interrupt Enable Enables or disables USB interrupt outputs when the ATTCH interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
10 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6	EOFERRE	0	R/W	EOF Error Detect Interrupt Enable Enables or disables USB interrupt outputs when the EOFERR interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
5	SIGNE	0	R/W	Setup Transaction Error Interrupt Enable Enables or disables USB interrupt outputs when the SIGN interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
4	SACKE	0	R/W	Setup Transaction ACK Interrupt Enable Enables or disables USB interrupt outputs when the SACK interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

32.3.11 BRDY Interrupt Enable Register (BRDYENB)

BRDYENB enables or disables the BRDY bit to be set to 1 when the BRDY interrupt of a pipe is detected.

When this module detects the BRDY interrupt of a pipe for which the software sets the corresponding bit in this register to 1, this module sets the PIPEBRDY bit of the pipe in BRDYSTS and also sets the BRDY bit in INTSTS0 to 1 and generates the BRDY interrupt.

When one or more PIPEBRDY bits in BRDYSTS are 1 and the software changes the corresponding interrupt enable bit(s) in this register from 0 to 1, this module generates the BRDY interrupt.

This register is initialized by a power-on reset.

ビット：	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	PIPE9 BRDYE	PIPE8 BRDYE	PIPE7 BRDYE	PIPE6 BRDYE	PIPE5 BRDYE	PIPE4 BRDYE	PIPE3 BRDYE	PIPE2 BRDYE	PIPE1 BRDYE	PIPE0 BRDYE
初期値：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W：	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	PIPE9 BRDYE	0	R/W	Pipe 9 BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
8	PIPE8 BRDYE	0	R/W	Pipe 8 BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
7	PIPE7 BRDYE	0	R/W	Pipe 7 BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
6	PIPE6 BRDYE	0	R/W	Pipe 6 BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

Bit	Bit Name	Initial Value	R/W	Description
5	PIPE5 BRDYE	0	R/W	Pipe 5 BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
4	PIPE4 BRDYE	0	R/W	Pipe 4 BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
3	PIPE3 BRDYE	0	R/W	Pipe 3 BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
2	PIPE2 BRDYE	0	R/W	Pipe 2 BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
1	PIPE1 BRDYE	0	R/W	Pipe 1 BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
0	PIPE0 BRDYE	0	R/W	Pipe 0 BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

32.3.12 NRDY Interrupt Enable Register (NRDYENB)

NRDYENB enables or disables the NRDY bit to be set to 1 when the NRDY interrupt of a pipe is detected.

When this module detects the NRDY interrupt of a pipe for which the software sets the corresponding bit in this register to 1, this module sets the PIPENRDY bit of the pipe in NRDYSTS and also sets the NRDY bit in INTSTS0 to 1 and generates an NRDY interrupt.

When one or more PIPENRDY bits in NRDYSTS are 1 and the software changes the corresponding interrupt enable bit(s) in this register from 0 to 1, this module generates an NRDY interrupt.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	PIPE9 NRDYE	PIPE8 NRDYE	PIPE7 NRDYE	PIPE6 NRDYE	PIPE5 NRDYE	PIPE4 NRDYE	PIPE3 NRDYE	PIPE2 NRDYE	PIPE1 NRDYE	PIPE0 NRDYE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	PIPE9 NRDYE	0	R/W	Pipe 9 NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
8	PIPE8 NRDYE	0	R/W	Pipe 8 NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
7	PIPE7 NRDYE	0	R/W	Pipe 7 NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
6	PIPE6 NRDYE	0	R/W	Pipe 6 NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

Bit	Bit Name	Initial Value	R/W	Description
5	PIPE5 NRDYE	0	R/W	Pipe 5 NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
4	PIPE4 NRDYE	0	R/W	Pipe 4 NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
3	PIPE3 NRDYE	0	R/W	Pipe 3 NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
2	PIPE2 NRDYE	0	R/W	Pipe 2 NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
1	PIPE1 NRDYE	0	R/W	Pipe 1 NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
0	PIPE0 NRDYE	0	R/W	Pipe 0 NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

32.3.13 BEMP Interrupt Enable Register (BEMPENB)

BEMPENB enables or disables the BEMP bit to be set to 1 when the BEMP interrupt of a pipe is detected.

When this module detects the BEMP interrupt of a pipe for which the software sets the corresponding bit in this register to 1, this module sets the PIPEBEMP bit of the pipe in BEMPSTS and the BEMP bit in INTSTS0 to 1 and generates the BEMP interrupt.

When one or more PIPEBEMP bits in BEMPSTS are 1 and the software changes the corresponding interrupt enable bit(s) in this register from 0 to 1, this module generates the BEMP interrupt.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	PIPE9 BEMPE	PIPE8 BEMPE	PIPE7 BEMPE	PIPE6 BEMPE	PIPE5 BEMPE	PIPE4 BEMPE	PIPE3 BEMPE	PIPE2 BEMPE	PIPE1 BEMPE	PIPE0 BEMPE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	PIPE9 BEMPE	0	R/W	Pipe 9 BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
8	PIPE8 BEMPE	0	R/W	Pipe 8 BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
7	PIPE7 BEMPE	0	R/W	Pipe 7 BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
6	PIPE6 BEMPE	0	R/W	Pipe 6 BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

Bit	Bit Name	Initial Value	R/W	Description
5	PIPE5 BEMPE	0	R/W	Pipe 5 BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
4	PIPE4 BEMPE	0	R/W	Pipe 4 BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
3	PIPE3 BEMPE	0	R/W	Pipe 3 BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
2	PIPE2 BEMPE	0	R/W	Pipe 2 BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
1	PIPE1 BEMPE	0	R/W	Pipe 1 BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
0	PIPE0 BEMPE	0	R/W	Pipe 0 BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

32.3.14 SOF Output Configuration Register (SOFCFG)

SOFCFG specifies an effective period of transactions, the BRDY interrupt status clear timing, and others.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	TRNENSEL	—	BRDYM	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R/W	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	TRNENSEL	0	R/W	Transaction Effective Period Switching Specifies a transaction effective period where this module sends a token in one frame in a port in full-speed or low-speed communication. 0: Low-speed is not supported. 1: Low-speed is supported. This bit is valid only when the host controller function is selected. This bit does not affect the high-speed transaction effective period even when the host controller function is selected. Set this bit to 0 when the function controller function is selected.
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6	BRDYM	0	R/W	Status Clear Timing of Each Pipe BRDY Interrupt Specifies the timing to clear the BRDY interrupt status of each pipe. 0: The software clears the status. 1: This module clears the status by reading or writing the FIFO buffer.

Bit	Bit Name	Initial Value	R/W	Description
5	—	0	R	Reserved This bit is reserved. Write the value that was read immediately before. Note: The initial value of this bit is 0 immediately after a power-on reset. Be sure to set this bit to 1 during the initialization routine of this module.
4 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

32.3.15 Interrupt Status Register 0 (INTSTS0)

INTSTS0 indicates the status of detected interrupts.

This register is initialized by a power-on reset. The DVSQ2 to DVSQ0 bits are also initialized by a USB bus reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VBINT	RESM	SOFR	DVST	CTRT	BEMP	NRDY	BRDY	VBSTS	DVSQ[2:0]			VALID	CTSQ[2:0]		
Initial value:	0	0	0	*1	0	0	0	0	*3	*2	*2	*2	0	0	0	0
R/W:	R/W*7	R/W*7	R/W*7	R/W*7	R/W*7	R	R	R	R	R	R	R	R/W*7	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	VBINT	0	R/W*7	VBUS0_0 and VBUS1_0 Interrupt Status*4*5 0: No VBUS0_0 and VBUS1_0 interrupt is generated. 1: A VBUS0_0 and VBUS1_0 interrupt is generated. This bit indicates 1 when this module detects a change in the VBUS0_0 and VBUS1_0 pin input level (high to low or low to high level). This module indicates the VBUS0_0 and VBUS1_0 pin input value using the VBSTS bit. When a VBINT interrupt occurs, read the VBSTS bit several times by the software and confirm that the read value is equal each time to eliminate chattering.
14	RESM	0	R/W*7	Resume Interrupt Status*4*5*6 0: No resume interrupt is generated. 1: A resume interrupt is generated. This bit indicates 1 when this module detects a falling of the DP pin level in the suspended state (DVSQ = 1XX) with the function controller function selected. The read value is invalid when the host controller function is selected.

Bit	Bit Name	Initial Value	R/W	Description
13	SOFR	0	R/W*7	Frame Number Update Interrupt Status*4 0: No SOF interrupt is generated. 1: An SOF interrupt is generated. (1) When the host controller function is selected When the UACT bit is set to 1 by the software, this bit is set to 1 at the frame number update timing. (This interrupt is detected every millisecond.) (2) When the function controller function is selected This module indicates SOFR = 1 at the frame number update timing. (This interrupt is detected every millisecond.) Even when an SOF packet from the USB host is corrupted, this module detects an SOFR interrupt using the internal interpolation.
12	DVST	0/1*1	R/W*7	Device State Transition Interrupt Status*4*6 0: No device state transition interrupt is generated. 1: A device state transition interrupt is generated. When this module detects a change in device state with the function controller function selected, this module updates the DVSQ value and set this bit to 1. When this interrupt occurred, clear the status before this module detects the next device state transition. The read value is invalid when the host controller function is selected.
11	CTRT	0	R/W*7	Control Transfer Stage Transition Interrupt Status*4*6 0: No control transfer stage transition interrupt is generated. 1: A control transfer stage transition interrupt is generated. When this module detects a control transfer stage transition with the function controller function selected, this module updates the CTSQ value and set this bit to 1. When this interrupt occurred, clear the status before this module detects the next stage transition in control transfers. The read value is invalid when the host controller function is selected.

Bit	Bit Name	Initial Value	R/W	Description
10	BEMP	0	R	Buffer Empty Interrupt Status 0: No BEMP interrupt is generated. 1: A BEMP interrupt is generated. This module indicates BEMP = 1 when at least one of the PIPEBEMP bits in BEMPSTS corresponding to the pipes for which 1 is set in the PIPEBEMPE bits in BEMPENB is set to 1 (when this module detects a BEMP interrupt of one or more pipes for which BEMP interrupts are enabled by the software). For PIPEBEMP status assertion conditions, see section 32.4.2 (3), BEMP Interrupt. When the software writes 0 to all PIPEBEMP bits corresponding to the pipes for which interrupts are enabled by the PIPEBEMPE bits, this module clears this bit to 0. This bit cannot be cleared to 0 by writing 0 by the software.
9	NRDY	0	R	Buffer Not Ready Interrupt Status 0: No NRDY interrupt is generated. 1: An NRDY interrupt is generated. This module indicates NRDY = 1 when at least one of the PIPENRDY bits in NRDYSTS corresponding to the pipes for which 1 is set in the PIPENRDYE bits in NRDYENB is set to 1 (when this module detects an NRDY interrupt of one or more pipes for which NRDY interrupts are enabled by the software). For PIPENRDY status assertion conditions, see section 32.4.2 (2), NRDY Interrupt. When the software writes 0 to all PIPENRDY bits corresponding to the pipes for which interrupts are enabled by the PIPENRDYE bits, this module clears this bit to 0. This bit cannot be cleared to 0 by writing 0 by the software.

Bit	Bit Name	Initial Value	R/W	Description
8	BRDY	0	R	Buffer Ready Interrupt Status Indicates the BRDY interrupt status. 0: No BRDY interrupt is generated. 1: A BRDY interrupt is generated. This module indicates BRDY = 1 when at least one of the PIPEBRDY bits in BRDYSTS corresponding to the pipes for which 1 is set in the PIPEBRDYE bits in BRDYENB is set to 1 (when this module detects a BRDY interrupt of one or more pipes for which BRDY interrupts are enabled by the software). For PIPEBRDY status assertion conditions, see section 32.4.2 (1), BRDY Interrupt. When the software writes 0 to all PIPEBRDY bits corresponding to the pipes for which interrupts are enabled by the PIPEBRDYE bits, this module clears this bit to 0. This bit cannot be cleared to 0 by writing 0 by the software.
7	VBSTS	0/1*[3]	R	VBUS Input Status 0: The VBUS0_0 and VBUS1_0 pin is low level. 1: The VBUS0_0 and VBUS1_0 pin is high level.
6 to 4	DVSQ[2:0]	000/001*[2]	R	Device State 000: Powered state 001: Default state 010: Address state 011: Configuration state 1xx: Suspended state The read value is invalid when the host controller function is selected.
3	VALID	0	R/W*[7]	USB Request Receive 0: Not detected 1: A setup packet is received. The read value is invalid when the host controller function is selected.

Bit	Bit Name	Initial Value	R/W	Description
2 to 0	CTSQ[2:0]	000	R	Control Transfer Stage 000: Idle stage or setup stage 001: Control read data stage 010: Control read status stage 011: Control write data stage 100: Control write status stage 101: Control write (NoData) status stage 110: Control transfer sequence error 111: Setting prohibited The read value is invalid when the host controller function is selected.

Notes:
1. The initial value is B'0 after a power-on reset, and B'1 after a USB bus reset.
2. The initial value is B'000 after a power-on reset, and B'001 after a USB bus reset.
3. The initial value is 1 when the VBUS0_0 and VBUS1_0 pin is high level, and is 0 when the VBUS0_0 and VBUS1_0 pin is low level.
4. To clear the VBINT, RESM, SOFR, DVST, or CTRT bit, write 0 only to bits to be cleared and write 1 to the other bits. Do not write 0 to status bits that indicate 0.
5. When a status change shown in the VBINT or RESM bit is detected while the clock is halted (SCKE = 0) and the corresponding interrupt is enabled, the interrupt is output. Clear the interrupt status of these bits by the software after the clock is enabled.
6. A status change of the RESM, DVST, or CTRT bit occurs only when the function controller function is selected. When the function controller function is selected, disable the corresponding interrupt enable bits to 0 (disabled).
7. Only writing 0 is enabled.

32.3.16 Interrupt Status Register 1 (INTSTS1)

INTSTS1 monitors the status of each interrupt.

By using INTSTS0 when the function controller function is selected or INTSTS1 when the host controller function is selected, occurrence of interrupts can be monitored with either of these registers.

Enable interrupts generated due to a status change shown by each bit in this register only when the host controller function is selected.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OVRCR	BCHG	—	DTCH	ATTCH	—	—	—	—	EOFERR	SIGN	SACK	—	—	—	—
Initial value:	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W*1	R	R/W*1	R/W*1	R	R	R	R	R/W*1	R/W*1	R/W*1	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	OVRCR	Undefined	R/W	OVRCR Interrupt Status This interrupt is generated when the OVCN_0 or OVCN2 pin input status changes. 0: No OVRCR interrupt is generated. 1: An OVRCR interrupt is generated.

Bit	Bit Name	Initial Value	R/W	Description
14	BCHG	0	R/W*[1]	USB Bus Change Interrupt Status Indicates the USB bus change interrupt status. 0: No BCHG interrupt is generated. 1: A BCHG interrupt is generated. When a full-speed or low-speed signal level change occurs in the USB port (from J-State, K-State, or SE0 to J-State, K-State, or SE0), this module detects a BCHG interrupt and indicates BCHG = 1. At this time, when the corresponding interrupt enable bit is set to 1 by the software, this module generates an interrupt. The current input state of the USB port is indicated by the LNST bits in SYSSTS. When a BCHG interrupt occurs, read the LNST bits several times by the software and confirm that the read value is equal each time to eliminate chattering. A USB bus change can also be detected while the internal clock is halted. The read value is invalid when the function controller function is selected.
13	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
12	DTCH	0	R/W*[1]	USB Disconnection Detect Interrupt Status Indicates the USB disconnection detect interrupt status when the host controller function is selected. 0: No DTCH interrupt is generated. 1: A DTCH interrupt is generated. When a USB bus disconnection is detected, this module detects a DTCH interrupt and indicates DTCH = 1. At this time, when the corresponding interrupt enable bit is set to 1 by the software, this module generates an interrupt. This module detects a USB bus disconnection based on the USB 2.0 Specification. After detecting a DTCH interrupt, this module performs the following hardware control irrespective of the setting of the corresponding interrupt enable bit. The software must terminate communication of all pipes with the USB port and drives this module into a state of waiting for ATTACH to the USB port (an ATTCH interrupt is generated). Clears the UACT bit of the port in which a DTCH interrupt is detected to 0 and indicates the UACT bit. Drives the port in which a DTCH interrupt is detected into the idle state. The read value is invalid when the function controller function is selected.

Bit	Bit Name	Initial Value	R/W	Description
11	ATTCH	0	R/W*[1]	ATTCH Interrupt Status Indicates the ATTCH interrupt status when the host controller function is selected. 0: No ATTCH interrupt is generated. 1: An ATTCH interrupt is generated. When this module detects J-State or K-State of full-speed or low-speed signal level for 2.5 μs in the USB port, this module detects an ATTCH interrupt and indicates ATTCH = 1. At this time, when the corresponding interrupt enable bit is set to 1 by the software, this module generates an interrupt. Conditions for this module to detect an ATTCH interrupt are as follows: When K-State, SE0 or SE1 changes to J-State and then J-State continues for 2.5 μs When J-State, SE0 or SE1 changes to K-State and then K-State continues for 2.5 μs The read value is invalid when the function controller function is selected.
10 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
6	EOFERR	0	R/W*[1]	EOF Error Detect Interrupt Status Indicates the EOFERR interrupt status when the host controller function is selected. 0: No EOFERR interrupt is generated. 1: An EOFERR interrupt is generated. When this module detects that communication is not completed at the EOF2 timing specified in the USB 2.0 Specification, this module detects an EOFERR interrupt and indicates EOFERR = 1. At this time, when the corresponding interrupt enable bit is set to 1 by the software, this module generates an EOFERR interrupt. After detecting an EOFERR interrupt, this module performs the following hardware control irrespective of the setting of the corresponding interrupt enable bit. The software must terminate communication of all pipes with the USB port and perform reenumeration for the USB port. Clears the UACT bit of the port in which an EOFERR interrupt is detected to 0 and indicates the UACT bit. Drives the port in which an EOFERR interrupt is detected into the idle state. The read value is invalid when the function controller function is selected.

Bit	Bit Name	Initial Value	R/W	Description
5	SIGN	0	R/W*[1]	Setup Transaction Error Interrupt Status Indicates the setup transaction error interrupt status when the host controller function is selected. 0: No SIGN interrupt is generated. 1: A SIGN interrupt is generated. When a peripheral device does not send an ACK response three times in a row in the SETUP transaction issued by this module, this module detects a SIGN interrupt and indicates SIGN = 1. At this time, when the corresponding interrupt enable bit is set to 1 by the software, this module generates a SIGN interrupt. This module detects a SIGN interrupt when any of the following response is generated to SETUP transactions (three times in a row). When the peripheral device sends no response and therefore this module detects a timeout When the ACK packet is corrupted When a handshake signal (NAK, NYET, or STALL) other than ACK is received The read value is invalid when the function controller function is selected.

Bit	Bit Name	Initial Value	R/W	Description
4	SACK	0	R/W*[1]	Setup Transaction ACK Response Interrupt Status Indicates the setup transaction ACK response interrupt status when the host controller function is selected. 0: No SACK interrupt is generated. 1: A SACK interrupt is generated. When this module receives an ACK response from a peripheral device in the SETUP transaction issued by this module, this module detects a SACK interrupt and indicates SACK = 1. At this time, when the corresponding interrupt enable bit is set to 1 by the software, this module generates a SACK interrupt.
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Notes: 1. To clear the status of each bit in this register, write 0 only to bits to be cleared and write 1 to the other bits.

2. When a status change shown in the BCHG bit is detected while the clock is halted (SCKE = 0) and the corresponding interrupt is enabled, the interrupt is output. Clear the BCHG interrupt status by the software after the clock is enabled.

   Any interrupts other than the BCHG bit are not detected while the clock is halted (SCKE = 0).

32.3.17 BRDY Interrupt Status Register (BRDYSTS)

BRDYSTS indicates the BRDY interrupt status of each pipe.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	PIPE9 BRDY	PIPE8 BRDY	PIPE7 BRDY	PIPE6 BRDY	PIPE5 BRDY	PIPE4 BRDY	PIPE3 BRDY	PIPE2 BRDY	PIPE1 BRDY	PIPE0 BRDY
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	PIPE9BRDY	0	R/W*1	Pipe 9 BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.
8	PIPE8BRDY	0	R/W*1	Pipe 8 BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.
7	PIPE7BRDY	0	R/W*1	Pipe 7 BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.
6	PIPE6BRDY	0	R/W*1	Pipe 6 BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.
5	PIPE5BRDY	0	R/W*1	Pipe 5 BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.
4	PIPE4BRDY	0	R/W*1	Pipe 4 BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.

Bit	Bit Name	Initial Value	R/W	Description
3	PIPE3BRDY	0	R/W*[1]	Pipe 3 BRDY Interrupt Status*[2] 0: No interrupt is generated. 1: An interrupt is generated.
2	PIPE2BRDY	0	R/W*[1]	Pipe 2 BRDY Interrupt Status*[2] 0: No interrupt is generated. 1: An interrupt is generated.
1	PIPE1BRDY	0	R/W*[1]	Pipe 1 BRDY Interrupt Status*[2] 0: No interrupt is generated. 1: An interrupt is generated.
0	PIPE0BRDY	0	R/W*[1]	Pipe 0 BRDY Interrupt Status*[2] 0: No interrupt is generated. 1: An interrupt is generated.

Notes: 1. To clear the status of each bit in this register when BRDYM is 0, write 0 only to bits to be cleared and write 1 to the other bits.
2. When BRDYM is 0, be sure to clear this interrupt before making an access to the FIFO.

32.3.18 NRDY Interrupt Status Register (NRDYSTS)

NRDYSTS indicates the NRDY interrupt status of each pipe.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	PIPE9 NRDY	PIPE8 NRDY	PIPE7 NRDY	PIPE6 NRDY	PIPE5 NRDY	PIPE4 NRDY	PIPE3 NRDY	PIPE2 NRDY	PIPE1 NRDY	PIPE0 NRDY
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	PIPE9NRDY	0	R/W*	Pipe 9 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
8	PIPE8NRDY	0	R/W*	Pipe 8 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
7	PIPE7NRDY	0	R/W*	Pipe 7 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
6	PIPE6NRDY	0	R/W*	Pipe 6 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
5	PIPE5NRDY	0	R/W*	Pipe 5 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
4	PIPE4NRDY	0	R/W*	Pipe 4 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.

Bit	Bit Name	Initial Value	R/W	Description
3	PIPE3NRDY	0	R/W*	Pipe 3 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
2	PIPE2NRDY	0	R/W*	Pipe 2 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
1	PIPE1NRDY	0	R/W*	Pipe 1 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
0	PIPE0NRDY	0	R/W*	Pipe 0 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.

Note: * To clear the status of each bit in this register, write 0 only to bits to be cleared and write 1 to the other bits.

32.3.19 BEMP Interrupt Status Register (BEMPSTS)

BEMPSTS indicates the BEMP interrupt status of each pipe.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	PIPE9 BEMP	PIPE8 BEMP	PIPE7 BEMP	PIPE6 BEMP	PIPE5 BEMP	PIPE4 BEMP	PIPE3 BEMP	PIPE2 BEMP	PIPE1 BEMP	PIPE0 BEMP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	PIPE9BEMP	0	R/W*	Pipe 9 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
8	PIPE8BEMP	0	R/W*	Pipe 8 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
7	PIPE7BEMP	0	R/W*	Pipe 7 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
6	PIPE6BEMP	0	R/W*	Pipe 6 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
5	PIPE5BEMP	0	R/W*	Pipe 5 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
4	PIPE4BEMP	0	R/W*	Pipe 4 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.

Bit	Bit Name	Initial Value	R/W	Description
3	PIPE3BEMP	0	R/W*	Pipe 3 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
2	PIPE2BEMP	0	R/W*	Pipe 2 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
1	PIPE1BEMP	0	R/W*	Pipe 1 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
0	PIPE0BEMP	0	R/W*	Pipe 0 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.

Note: * To clear the status of each bit in this register, write 0 only to bits to be cleared and write 1 to the other bits.

32.3.20 Frame Number Register (FRMNUM)

FRMNUM indicates the sources of isochronous errors and a frame number.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OVRN	CRCE	—	—	—	FRNM[10:0]										
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W*	R/W*	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	OVRN	0	R/W*	Overrun/Underrun Detect Status Indicates whether an overrun or underrun error is detected or not in a pipe that is performing isochronous transfer. 0: No error is detected. 1: An error is detected. Writing 0 to this bit by the software clears this bit to 0. At this time, write 1 to the other bits in this register. (1) When the host controller function is selected This module indicates OVRN =1 in any of the following cases. When the OUT token transmit timing comes when transmit data write to the FIFO buffer is not completed in a transmit direction pipe of isochronous transfer type When the IN token transmit timing comes with no side of the FIFO buffer empty in a receive direction pipe of isochronous transfer type (2) When the function controller function is selected This module indicates OVRN =1 in any of the following cases. When the IN token is received when transmit data write to the FIFO buffer is not completed in a transmit direction pipe of isochronous transfer type When the OUT token is received with no side of the FIFO buffer empty in a receive direction pipe of isochronous transfer type

Bit	Bit Name	Initial Value	R/W	Description
14	CRCE	0	R/W*	Receive Data Error Indicates whether a CRC error or bit stuffing error is detected or not in a pipe that is performing isochronous transfer. 0: No error is detected. 1: An error is detected. Writing 0 to this bit by the software clears this bit to 0. At this time, write 1 to the other bits in this register. (1) When the host controller function is selected When a CRC error is detected, this module generates an internal NRDY interrupt request. (2) When the function controller function is selected When a CRC error is detected, this module does not generate an internal NRDY interrupt request.
13 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 0	FRNM [10:0]	H'000	R	Frame Number This module modifies this bit at the SOF transmit timing (every 1 ms) or when an SOF is received and indicates the latest frame number. Read these bits twice and confirm that the read value is equal each time.

Note: * Only writing 0 is enabled.

32.3.21 μ Frame Number Register (UFRMNUM)

UFRMNUM indicates a μ frame number.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	UFRNM[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2 to 0	UFRNM[2:0]	000	R	μ Frame Indicate a μ frame number. In high-speed operating mode, these bits indicate a μ frame number. In other operating modes, these bits indicate B'000. Read these bits twice and confirm that the read value is equal each time.

32.3.22 USB Address Register (USBADDR)

USBADDR indicates a USB address.

This register is valid only when the function controller function is selected. To set the address of a peripheral device when the host controller function is selected, use the DEVSEL bits in PIPEMAXP.

This register is initialized by a power-on reset or USB bus reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	USBADDR[6:0]						
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6 to 0	USBADDR[6:0]	H'00	R	USB Address Indicate the USB address allocated by the host when the SET_ADRESS request is successfully processed with the function controller function selected. When this module detects a USB reset, these bits indicate H'00. When the host controller function is selected, these bits are invalid.

32.3.23 USB Request Type Register (USBREQ)

USBREQ stores the setup request for control transfers.

When the function controller function is selected, USBREQ stores the values of received bRequest and bmRequestType. When the host controller function is selected, USBREQ sets the values of bRequest and bmRequestType to be sent.

This register is initialized by a power-on reset or USB bus reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BREQUEST[7:0]								BMREQUESTTYPE[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*

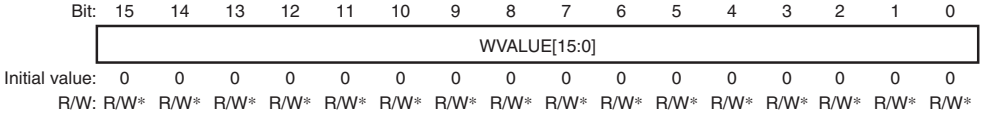
Bit	Bit Name	Initial Value	R/W	Description
15 to 8	BREQUEST [7:0]	H'00	R/W*	Request Store the value of USB request bRequest. (1) When the host controller function is selected Set the value of USB request data of the SETUP transaction to be sent. Do not modify these bits when the SUREQ bit is 1. (2) When the function controller function is selected Indicate the USB request data received in the SETUP transaction. These bits cannot be modified.
7 to 0	BMREQUEST TYPE[7:0]	H'00	R/W*	Request Type Store the value of USB request bmRequestType. (1) When the host controller function is selected: Set the value of USB request data of the SETUP transaction to be sent. Do not modify these bits when the SUREQ bit is 1. (2) When the function controller function is selected: Indicate the USB request data received in the SETUP transaction. These bits cannot be modified.

Note: * When the function controller function is selected, these are read-only bits and cannot be modified. When the host controller function is selected, these are readable/writable bits.

32.3.24 USB Request Value Register (USBVAL)

When the function controller function is selected, USBVAL stores the value of received wValue. When the host controller function is selected, USBVAL sets the value of wValue to be sent.

This register is initialized by a power-on reset or USB bus reset.



Bit	Bit Name	Initial Value	R/W	Description
15 to 0	WVALUE [15:0]	H'0000	R/W*	Value Store the value of USB request wValue. (1) When the host controller function is selected Set the value of USB request wValue of the SETUP transaction to be sent. Do not modify these bits when the SUREQ bit is 1. (2) When the function controller function is selected Indicate the value of USB request wValue received in the SETUP transaction. These bits cannot be modified.

Note: * When the function controller function is selected, these are read-only bits and cannot be modified. When the host controller function is selected, these are readable/writable bits.

32.3.25 USB Request Index Register (USBINDX)

USBINDX stores the setup request for control transfers.

When the function controller function is selected, USBINDX stores the value of received wIndex. When the host controller function is selected, USBINDX sets the value of wIndex to be sent.

This register is initialized by a power-on reset or USB bus reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WINDEX[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*

Bit	Bit Name	Initial Value	R/W	Description
15 to 0	WINDEX [15:0]	H'0000	R/W*	Index Store the value of USB request wIndex. (1) When the host controller function is selected Set the value of USB request wIndex of the SETUP transaction to be sent. Do not modify these bits when the SUREQ bit is 1. (2) When the function controller function is selected Indicate the value of USB request wIndex received in the SETUP transaction. These bits cannot be modified.

Note: * When the function controller function is selected, these are read-only bits and cannot be modified. When the host controller function is selected, these are readable/writable bits.

32.3.26 USB Request Length Register (USBLENG)

USBLENG stores the setup request of control transfers.

When the function controller function is selected, USBLENG stores the value of received wLength. When the host controller function is selected, USBLENG sets the value of wLength to be sent.

This register is initialized by a power-on reset or USB bus reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WLENGTH[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*

Bit	Bit Name	Initial Value	R/W	Description
15 to 0	WLENGTH [15:0]	H'0000	R/W*	Length Store the value of USB request wLength. (1) When the host controller function is selected Set the value of USB request wLength of the SETUP transaction to be sent. Do not modify these bits when the SUREQ bit is 1. (2) When the function controller function is selected Indicate the value of USB request wLength received in the SETUP transaction. These bits cannot be modified.

Note: * When the function controller function is selected, these are read-only bits and cannot be modified. When the host controller function is selected, these are readable/writable bits.

32.3.27 DCP Configuration Register (DCPCFG)

DCPCFG specifies the data transfer direction of the default control pipe (DCP).

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	DIR	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	DIR	0	R/W	Transfer Direction Specifies the data stage and status stage transfer direction of control transfers when the host controller function is selected. 0: Data receive direction 1: Data transmit direction When the function controller function is selected, set this bit to 0.
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

32.3.28 DCP Maximum Packet Size Register (DCPMAXP)

DCPMAXP specifies the maximum packet size of the DCP.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DEVSEL[3:0]				—	—	—	—	—	MXPS[6:0]						
Initial value:	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	DEVSEL [3:0]	0000	R/W	Device Select Specify the address of the peripheral device that is a remote party for control transfers when the host controller function is selected. 0000: Address 0000 0001: Address 0001 : : 1001: Address 1001 1010: Address 1010 Other than above: Setting prohibited Set DEVADDn corresponding to the value of these bits, and then set these bits. When setting DEVSEL = 0010, for example, set the address in DEVADD2. Set these bits when CSSTS = 0, PID = NAK, and the SUREQ bit is 0. To change these bits after changing the PID bits in DCP from BUF to NAK, check CSSTS = 0 and PBUSY = 0 and then change these bits. However, the software does not have to check the PBUSY bit when this module changed the PID bit to NAK. When the function controller function is selected, set these bits to B'0000.
11 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
6 to 0	MXPS [6:0]	H'40	R/W	Maximum Packet Size Set the payload of DCP data (maximum DCP packet size) in these bits. The initial value of these bits is H'40 (64 bytes). Set a value in the MXPS bits based on the USB Specification. Set the MXPS bits when CSSTS = 0, PID = NAK, and the CURPIPE bits are not set. When setting these bits to 1 after changing the PID bits for the pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK. Do not write the FIFO buffer when the MXPS bits are 0 or set the PID bits to BUF.

32.3.29 DCP Control Register (DCPCTR)

DCPCTR is used to monitor the buffer memory status, change/check the data PID sequence bit, and set the response PID for a DCP.

This register is initialized by a power-on reset. The PID2 to PID0 bits in CCPL are also initialized by a USB bus reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BSTS	SUREQ	CSCLR	CSSTS	SUREQCLR	—	—	SQCLR	SQSET	SQMON	PBUSY	PINGE	—	CCPL	PID[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
R/W:	R	R/W*2	R/W*1	R	R/W*1	R	R	R/W*1	R/W*1	R	R	R/W	R	R/W*1	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	BSTS	0	R	Buffer Status Indicates whether the DCP FIFO buffer is accessible or not. 0: The buffer is not accessible. 1: The buffer is accessible. This bit indicates as follows depending on the ISEL value. When ISEL = 0, this bit indicates whether the buffer is ready to read receive data. When ISEL = 1, this bit indicates whether the buffer is ready to write transmit data.

Bit	Bit Name	Initial Value	R/W	Description
14	SUREQ	0	R/W*[2]	Sending SETUP Token When the host controller function is selected, a setup packet is sent by writing 1 to this bit. 0: Invalid 1: A setup packet is sent. After processing the SETUP transaction, this module generates a SACK interrupt or SIGN interrupt and clears this bit to 0. When the SUREQCLR bit is set to 1 by the software, this module clears this bit to 0. Set this bit to 1 after setting the USB request to be sent in the SETUP transaction in the DEVSEL bits, USBREQ, USBVAL, USBINDX, and USBLENG registers. Check that PID bits in DCP are set to NAK before setting the SUREQ bit to 1. Furthermore, do not change the values of the DEVSEL bits, USBREQ, USBVAL, USBINDX, and USBLENG registers after setting this bit to 1 until the SETUP transaction is completed (while SUREQ = 1). Set this bit to 1 only when sending a SETUP token. In other cases, be sure to set this bit to 0. When the function controller function is selected, be sure to set this bit to 0.

Bit	Bit Name	Initial Value	R/W	Description
13	CSCLR	0	R/W*[1]	Split Transactions C-SPLIT Status Clear When the host controller function is selected, the CSSTS bit can be cleared to 0 by writing 1 to this bit for data transfer using split transactions. In this case, the next transfer of DCP restarts with S-SPLIT. 0: Invalid 1: Clears the CSSTS bit to 0. When this bit is set to 1 by the software, this module clears the CSSTS bit to 0. To forcibly restart the next transfer with S-SPLIT in data transfer using split transactions, set this bit to 1 by the software. Since this module automatically clears the CSSTS bit to 0 at the end of C-SPLIT in normal split transactions, the software needs not clear the CSSTS bit. Control the CSSTS bit with this bit while communication is halted by clearing the UACT bit or when it is clarified that no data transfer is performed by detection of DETACH. Even if this bit is set to 1 when CSSTS is 0, CSSTS remains 0. When the function controller function is selected, be sure to set this bit to 0.
12	CSSTS	0	R	Split Transactions COMPLETE SPLIT (C-SPLIT) Status When the host controller function is selected, the C-SPLIT status of split transactions is indicated. 0: START-SPLIT (S-SPLIT) transaction is being processed or a device that is not used in split transactions is being processed. 1: C-SPLIT transaction is being processed. This module sets this bit to 1 when starting C-SPLIT, and clears this bit to 0 when C-SPLIT end is detected. When the function controller function is selected, the read value of this bit is invalid.

Bit	Bit Name	Initial Value	R/W	Description
11	SUREQCLR	0	R/W*[1]	SUREQ Bit Clear When the host controller function is selected, the SUREQ bit can be cleared to 0 by writing 1 to this bit. 0: Invalid 1: Clears the SUREQ bit. This bit always indicates 0. When communication is halted with the SUREQ bit set to 1 in the SETUP transaction, set this bit to 1 by the software. Since this module automatically clears the SUREQ bit to 0 at the end of normal SETUP transaction, the software needs not clear the SUREQ bit. Control the SUREQ bit with this bit while communication is halted by clearing the UACT bit or when it is clarified that no data transfer is performed by detection of DETACH. When the function controller function is selected, be sure to set this bit to 0.
10, 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	SQCLR	0	R/W*[1]	Toggle Bit Clear The expected value of the sequence toggle bit for the next transaction in DCP transfer can be set in DATA0. 0: Invalid 1: The expected value is set in DATA0. This bit always indicates 0. Do not set the SQCLR and SQSET bits to 1 at the same time. Set this bit to 1 when CSCTS = 0, PID = NAK, and the CURPIPE bits are not set. When setting this bit to 1 after changing the PID bits for the pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.

Bit	Bit Name	Initial Value	R/W	Description
7	SQSET	0	R/W*[1]	Toggle Bit Set The expected value of the sequence toggle bit for the next transaction in DCP transfer can be set in DATA1. 0: Invalid 1: The expected value is set in DATA1. Do not set the SQCLR and SQSET bits to 1 at the same time. Set this bit to 1 when CSCTS = 0, PID = NAK, and the CURPIPE bits are not set. When setting this bit to 1 after changing the PID bits for the pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.
6	SQMON	1	R	Sequence Toggle Bit Monitor Indicates the expected value of the sequence toggle bit for the next transaction in DCP transfer. 0: DATA0 1: DATA1 When the transaction is successfully completed, this module toggles this bit. However, when a DATA-PID mismatch occurs in the receive direction transfer, this bit is not toggled. When the function controller function is selected, this module sets this bit to 1 (sets the expected value in DATA1) when the setup packet is successfully received. When the function controller function is selected, this module does not read this bit in IN transactions or OUT transactions in the status stage.

Bit	Bit Name	Initial Value	R/W	Description
5	PBUSY	0	R	Pipe Busy Indicates whether the DCP communication state is shifted to the NAK state or not when the DCP changed the PID bits from BUF to NAK. 0: Transition to the NAC state is not completed. 1: Transition to the NAC state is completed. When this module starts the USB transaction for the corresponding pipe, this module sets this bit to 1. This module clears this bit to 0 upon completion of each transaction. After the software sets PID = NAK, read this bit to check whether changing the pipe setting is enabled or not.
4	PINGE	0	R/W	PING Token Output Enable When this bit is set to 1 with the host controller function selected, this module sends the PING token in the transmit direction transfer. The transmit direction transfer is started with the PING transaction. 0: Sending the PING token is disabled. 1: Normal PING operation When an ACK handshake is detected in the PING transaction, this module executes an OUT transaction for the next transaction. When a NAK handshake is detected in an OUT transaction, this module executes a PING transaction for the next transaction. When the software sets this bit to 0 with the host controller function selected, this module does not send the PING token in the transmit direction transfer. The transmit direction transfer is always performed in OUT transactions. Change this bit when CSSTS = 0 and PID = NAK. When setting this bit to 1 after changing the PID bits for the pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK. When the function controller function is selected, be sure to set this bit to 0.

Bit	Bit Name	Initial Value	R/W	Description
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2	CCPL	0	R/W*[1]	Control Transfer End Enable Enables the status stage end of control transfers when the function controller function is selected. 0: Invalid 1: The control transfer end is enabled. When the software sets this bit to 1 while the corresponding PID bits are set to BUF, this module finishes the control transfer stage. That is, this module sends an ACK handshake in response to OUT transactions from the USB host in the control read transfer, and sends a Zero-Length packet in response to IN transactions from the USB host in control write and no-data control transfers. However, a SET_ADDRESS request is detected, this module automatically sends responses from the SETUP stage until the end of the status stage irrespective of the setting of this bit. When this module receives the next setup packet, this module clears this bit to 0. When VALID = 1, the software cannot write 1 to this bit. When the host controller function is selected, be sure to set this bit to 0.

Bit	Bit Name	Initial Value	R/W	Description
1, 0	PID[1:0]	00	R/W	Response PID Control responses of this module in control transfers. 00: NAK response 01: BUF response (depending on buffer state) 10: STALL response 11: STALL response (1) When the host controller function is selected Change these bits from NAK to BUF. When transmit direction is set Write all transmit data to the FIFO buffer when UACT = 1 and PID = NAK, and then set the PID bits to BUF. After BUF is set, this module executes OUT transactions (or PING transactions). When receive direction is set Check that the FIFO buffer is empty (or make it empty) when UACT = 1 and PID = NAK, and then set the PID bits to BUF. After BUF is set, this module executes IN transactions. This module modifies these bits in the following cases. When this module receives data with a size exceeding the MaxPacketSize value while these bits are set to BUF by the software, this module indicates PID = STALL (11). When this module detects a CRC error or another receive error three times in a row, this module indicates PID = NAK. When this module receives a STALL handshake, this module indicates PID = STALL (11). After this module sends S-SPLIT of split transactions for the selected pipe (indicating CSSTS = 1), this module executes the transaction until C-SPLIT is completed even if the software changed these bits to NAK. When C-SPLIT is completed, this module indicates PID = NAK.

Bit	Bit Name	Initial Value	R/W	Description
1, 0	PID[1:0]	00	R/W	(2) When the function controller function is selected This module modifies these bits in the following cases. This module changes these bits to NAK upon receiving a SETUP packet. At this time, this module indicates VALID = 1. The software cannot modify these bits until the software sets VALID = 0. When this module receives data with a size exceeding the MaxPacketSize value while these bits are set to BUF by the software, this module indicates PID = STALL (11). When this module detects a control transfer sequence error, this module indicates PID = STALL (1x). When this module detects a USB bus reset, this module indicates PID = NAK. This module does not read the value of these bits during the SET_ADDRESS request processing (auto processing).

Notes: 1. These bits are always read as 0. Only writing 1 is enabled.
2. Only writing 1 is enabled.

32.3.30 Pipe Window Select Register (PIPESEL)

Make settings for pipes 1 to 9 using PIPESEL, PIPECFG, PIPEBUF, PIPEMAXP, PIPEPERI, PIPEnCTR, PIPEnTRE, and PIPEnTRN.

Specify a pipe to be used with PIPESEL, and then make function settings for each pipe in PIPECFG, PIPEBUF, PIPEMAXP, and PIPEPERI. The PIPEnCTR, PIPnTRE, and PIPnTRN registers can be set independently from pipe selection using PIPESEL.

Not only the selected pipe but also the corresponding bits in registers for all pipes are initialized by a power-on reset or USB bus reset.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	PIPESEL[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
3 to 0	PIPESEL [3:0]	0000	R/W	Pipe Window Select Specify a pipe number corresponding to PIPECFG, PIPEBUF, PIPEMAXP, and PIPEPERI to be read or written. 0000: No pipe is selected. 0001: Pipe 1 0010: Pipe 2 0011: Pipe 3 0100: Pipe 4 0101: Pipe 5 0110: Pipe 6 0111: Pipe 7 1000: Pipe 8 1001: Pipe 9 Other than above: Setting prohibited PIPECFG, PIPEBUF, PIPEMAXP, and PIPEPERI corresponding to the pipe number specified by these bits can be read and written. When these bits are set to 0000, all bits in PIPECFG, PIPEBUF, PIPEMAXP, and PIPEPERI are read as 0 and cannot be modified.

32.3.31 Pipe Configuration Register (PIPECFG)

PIPECFG specifies the transfer type, buffer memory access direction, and endpoint number for pipes 1 to 9, selects continuous transfer mode or discontinuous transfer mode, and single buffer or double buffer, and also specifies whether to disable the operation of each pipe when data transfer finishes.

This register is initialized by a power-on reset. The TYPE1 and TYPE0 bits are also initialized by a USB bus reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TYPE[1:0]		—	—	—	BFRE	DBLB	CNT MD	SHT NAK	—	—	DIR	EPNUM[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15, 14	TYPE[1:0]	00	R/W	Transfer Type Select the transfer type of the pipe specified by the PIPESEL bits (selected pipe). Pipes 1 and 2 00: No pipe is used. 01: Bulk transfer 10: Setting prohibited 11: Isochronous transfer Pipes 3 to 5 00: No pipe is used. 01: Bulk transfer 10: Setting prohibited 11: Setting prohibited Pipes 6 to 9 00: No pipe is used. 01: Setting prohibited 10: Interrupt transfer 11: Setting prohibited Before setting the selected pipe for PID = BUF (before starting USB communication using the selected pipe), be sure to set these bits to a value other than 00. Modify these bits when the PID bits of the selected pipe are set to NAK. When changing the setting of these bits after changing the PID bits for the selected pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.
13 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
10	BFRE	0	R/W	BRDY Interrupt Operation Specifies the BRDY interrupt output timing from this module to the CPU for the selected pipe. 0: At a BRDY interrupt timing during data transmission or reception 1: At a BRDY interrupt timing after reading data When this bit is set to 1 by the software and the selected pipe is used in the receive direction, this module detects the transfer end and outputs a BRDY interrupt when the packet is completely read. When a BRDY interrupt occurs with this setting, the software must set BCLR = 1. Unless BCLR = 1 is set, the FIFO buffer allocated to the selected pipe does not enter the receive ready state. When this bit is set to 1 by the software and the selected pipe is used in the transmit direction, this module generates no BRDY interrupt. For details, see section 32.4.2 (1), BRDY Interrupt. Modify this bit when CSSTS = 0, PID = NAK, and no pipe number is specified by the CURPIPE bits. Furthermore, when changing the setting of this bit after USB communication using the selected pipe, set the ACLRM bit to 1 and clear it to 0 continuously by the software to clear the FIFO buffer allocated to the selected pipe, in addition to the three register states above. When changing the setting of this bit after changing the PID bits for the selected pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.

Bit	Bit Name	Initial Value	R/W	Description
9	DBLB	0	R/W	Double Buffer Mode Specifies a single buffer or double buffer for the FIFO buffer used in the selected pipe. 0: Single buffer 1: Double buffer This bit is valid when pipes 1 to 5 are selected. When this bit is set to 1 by the software, this module allocates the FIFO buffer size specified by the BUFSIZE bits in PIPEBUF to the selected pipe for two sides. Thus the size of the FIFO buffer that this module allocates to the selected pipe is as follows: (BUFSIZE + 1) * 64 * (DBLB + 1) [bytes] When this bit is set to 1 by the software and the selected pipe is used in the transmit direction, this module generates no BRDY interrupt. For details, see section 32.4.2 (1), BRDY Interrupt. Modify this bit when CSSTS = 0, PID = NAK, and no pipe number is specified by the CURPIPE bits. Furthermore, when changing the setting of this bit after USB communication using the selected pipe, set the ACLRM bit to 1 and clear it to 0 continuously by the software to clear the FIFO buffer allocated to the selected pipe, in addition to the three register states above. When changing the setting of this bit after changing the PID bits for the selected pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.

Bit	Bit Name	Initial Value	R/W	Description
8	CNTMD	0	R/W	Continuous Transfer Mode Selects continuous transfer mode or discontinuous transfer mode to be used in communication for the selected pipe. 0: Discontinuous transfer mode 1: Continuous transfer mode This bit is valid when pipes 1 to 5 are selected by the PIPESEL bits and bulk transfer is selected (TYPE = 01). Modify this bit when CSSTS = 0, PID = NAK, and no pipe number is specified by the CURPIPE bits. Furthermore, when changing the setting of this bit after USB communication using the selected pipe, set the ACLRM bit to 1 and clear it to 0 continuously by the software to clear the FIFO buffer allocated to the selected pipe, in addition to the three register states above. When changing the setting of this bit after changing the PID bits for the selected pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.

Bit	Bit Name	Initial Value	R/W	Description
7	SHTNAK	0	R/W	Pipe Disable at the Time of Transfer End Specifies whether to change the setting of the PID bits to NAK at the end of transfer when the selected pipe is in the receive direction. 0: The pipe is continued at the end of transfer. 1: The pipe is disabled at the end of transfer. This bit is valid when the selected pipe is either of pipes 1 to 5 and is in the receive direction. When the software sets this bit to 1 for a receive direction pipe, this module changes the setting of the PID bits corresponding to the selected pipe to NAK for the selected pipe when this module determines the transfer end. When the following conditions are satisfied, this module determines the transfer end. When short packet data (including a Zero-Length packet) is correctly received. When the transaction counter is used and packets with a size of the transaction counter are correctly received. Modify this bit when CSSTS = 0 and PID = NAK. When changing the setting of this bit after changing the PID bits for the selected pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK. For transmit direction pipes, set this bit to 0.
6, 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
4	DIR	0	R/W	Transfer Direction Selects the transfer direction of the selected pipe. 0: Receive direction 1: Transmit direction When this bit is set to 0 by the software, this module uses the selected pipe in the receive direction. When this bit is set to 1, this module uses the selected pipe in the transmit direction. Modify this bit when CSSTS = 0, PID = NAK, and no pipe number is specified by the CURPIPE bits. Furthermore, when changing the setting of this bit after USB communication using the selected pipe, set the ACLRM bit to 1 and clear it to 0 continuously by the software to clear the FIFO buffer allocated to the selected pipe, in addition to the three register states above. When changing the setting of this bit after changing the PID bits for the selected pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.
3 to 0	EPNUM[3:0]	0000	R/W	Endpoint Number Specify the endpoint number of the selected pipe. The setting of 0000 means an unused pipe. Modify these bits when CSSTS = 0 and PID = NAK. When changing the setting of these bits after changing the PID bits for the selected pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK. Set these bits so that the combination of the DIR setting and the EPNUM setting does not overlap the setting of other pipes (EPNUM = 0000 is allowed in this case.)

32.3.32 Pipe Buffer Register (PIPEBUF)

PIPEBUF specifies the buffer size and buffer number for pipes 1 to 9.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	BUFSIZE[4:0]					—	—	BUFNMB[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
14 to 10	BUFSIZE [4:0]	H'00	R/W	Buffer Size Specify the buffer size of the pipe specified by the PIPESEL bits (selected pipe) in units of blocks. One block is 64 bytes. 00000 (H'00): 64 bytes 00001 (H'01): 128 bytes : : 11111 (H'1F): 2 Kbytes When DBLB = 1 is set by the software, this module allocates the FIFO buffer size specified by these bits to the selected pipe for two sides. Thus the size of the FIFO buffer that this module allocates to the selected pipe is as follows: (BUFSIZE + 1) * 64 * (DBLB + 1) [bytes] A value that can be set in these bits varies depending on pipes selected. For pipes 1 to 5: Set BUFSIZE to H'00 to H'1F. For pipes 6 to 9: Set BUFSIZE to H'00. When using the buffer with CNTMD = 1, set a value in multiples of MaxPacketSize in these bits. Modify these bits when CSSTS = 0, PID = NAK, and no pipe number is specified by the CURPIPE bits. When changing the setting of this bit after changing the PID bits for the selected pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.
9, 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	BUFNMB [7:0]	H'00	R/W	Buffer Number Specify the FIFO buffer number of the selected pipe with a value from H'04 to H'87. When the selected pipe is either of pipes 1 to 5, these bits can be set to a value according to user systems. Set BUFNMB to H'06 to H'4F. BUFNMB = 0 to 3 are for DCP only. BUFNMB = 4 is for pipe 6 only. However, when pipe 6 is not used, this is available for other pipes. When pipe 6 is selected, these bits cannot be modified and this module automatically allocates BUFNMB = 4. BUFNMB = 5 is for pipe 7 only. However, when pipe 7 is not used, this is available for other pipes. When pipe 7 is selected, these bits cannot be modified and this module automatically allocates BUFNMB = 5. BUFNMB = 6 is for pipe 8 only. However, when pipe 8 is not used, this is available for other pipes. When pipe 8 is selected, these bits cannot be modified and this module automatically allocates BUFNMB = 6. BUFNMB = 7 is for pipe 9 only. However, when pipe 9 is not used, this is available for other pipes. When pipe 9 is selected, these bits cannot be modified and this module automatically allocates BUFNMB = 7. Modify these bits when CSSTS = 0, PID = NAK, and no pipe number is set in the CURPIPE bits. When changing the setting of these bits after changing the PID bits for the selected pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.

32.3.33 Pipe Maximum Packet Size Register (PIPEMAXP)

PIPEMAXP specifies the maximum packet size for pipes 1 to 9.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DEVSEL[3:0]				—	MXPS[10:0]										
Initial value:	0	0	0	0	0	*	*	*	*	*	*	*	*	*	*	*
R/W:	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	DEVSEL[3:0]	00	R/W	Device Select Specify the USB device address of the peripheral device that is a remote party for communication when the host controller function is selected. 0000: Address 0000 0001: Address 0001 0010: Address 0010 : : 1010: Address 1010 Other than above: Setting prohibited Set these bits after setting DEVADDn (n = 0 to A) corresponding to the value of these bits. When setting DEVSEL = 0010, for example, set the address in DEVADD2. To change these bits after changing the PID bits in DCP from BUF to NAK, check CSSTS = 0 and PBUSY = 0 and then change these bits. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK. When the function controller function is selected, set these bits to B'0000.
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
10 to 0	MXPS[10:0]	*	R/W	Maximum Packet Size Specify the payload of data (maximum packet size) of the selected pipe. The settable value range for each pipe is as follows: Pipes 1 and 2: 1 byte (H'001) to 1024 bytes (H'400) Pipes 3 to 5: 8 (H'008), 16 (H'010), 32 (H'020), 64 (H'040), or 512 bytes (H'200) (MXPS2 to MXPS0 bits are not provided.) Pipes 6 to 9: 1 byte (H'001) to 64 bytes (H'040) Set a value in the MXPS bits based on the USB Specification for each transfer type. To transmit an isochronous pipe in split transactions, set a value of 188 bytes or less in the MXPS bits. When changing the setting of this bit after changing the PID bits for the selected pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK. Do not write the FIFO buffer when the MXPS = 0 or set the PID bits to BUF.

Note: * The initial value is H'000 (when no pipe is selected by the PIPESEL bits in PIPESEL) or H'040 (when a pipe is selected).

32.3.34 Pipe Cycle Control Register (PIPEPERI)

PIPEPERI specifies whether to activate the buffer flush function or not at the time of an interval error during the isochronous IN transfer, and also specifies the interval error detection interval for pipes 1 to 9.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	IFIS	—	—	—	—	—	—	—	—	—	IITV[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	IFIS	0	R/W	Isochronous IN Buffer Flush Specifies whether to flush the FIFO buffer when the pipe specified by the PIPESEL bits (selected pipe) is isochronous IN transfer type. 0: The FIFO buffer is not flushed. 1: The FIFO buffer is flushed. Buffer flush is a function that this module automatically clears the FIFO buffer when this module does not receive IN-Token from the USB host in a (μ) frame for each interval specified in the IITV bits when the function controller function is selected and the selected pipe is isochronous IN transfer type. When double buffer is selected (DBLB = 1), this module clears data of only the older side. The FIFO buffer is cleared when an SOF packet is received immediately after the (μ) frame where IN-Token is to be received. Even if the SOF packet is corrupted, the FIFO buffer is cleared at the time when the SOF packet is to be received using the internal interpolation. When the host controller function is selected, set this bit to 0. When the selected pipe is not isochronous transfer type, set this bit to 0.

Bit	Bit Name	Initial Value	R/W	Description
11 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2 to 0	IITV[2:0]	000	R/W	Interval Error Detection Interval Specify the interval error detection interval of the selected pipe with a value of 2's n-th power of the frame timing. This function differs in detail between host controller function and function controller function as described later. Set these bits when CSSTS = 0, PID = NAK, and no pipe number is specified by the CURPIPE bits. When changing the setting of these bits after changing the PID bits for the selected pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK. To change the setting of these bits after USB communication, set PID = NAK and then set ACLRM = 1 to initialize the interval timer. These bits are not provided for pipes 3 to 5. Set 000 in the position of these bits corresponding to pipes 3 to 5.

32.3.35 Pipe n Control Register (PIPEnCTR) (n = 1 to 9)

PIPEnCTR monitors the buffer memory status, changes/checks the data PID sequence bits, selects whether to use auto-response mode and buffer auto-clear mode, and specifies a response PID for pipes 1 to 9. This register can be set independently of the pipe selection using PIPESEL.

This register is initialized by a power-on reset. The PID1 and PID0 bits are also initialized by a USB bus reset.

(1) PIPEnCTR (n = 1 to 5)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BSTS	INBUFM	CSCLR	CSSTS	—	ATREPM	ACLRM	SQCLR	SQSET	SQMON	PBUSY	—	—	—	PID[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W*2	R	R	R/W	R/W	R/W*1	R/W*1	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	BSTS	0	R	Buffer Status Indicates the FIFO buffer status of the pipe. 0: The buffer is not accessible from the CPU. 1: The buffer is accessible from the CPU. The meaning of this bit differs depending on the settings of the DIR, BFRE, and DCLRM bits as shown in Table 32.9.
14	INBUFM	0	R	Transmit Buffer Monitor Indicates the FIFO buffer status of the selected pipe in the transmit direction. 0: The buffer memory contains no transmittable data. 1: The buffer memory contains transmittable data. When transmit direction (DIR = 1) is set for the pipe, this module sets this bit to 1 when the software (or DMAC) finishes writing data to the FIFO buffer for at least one register set. When this module finishes sending all data on the register set (writing is completed) of the FIFO buffer, this bit indicates 0. In the case of a double buffer (DBLB = 1), when this module finishes sending all data on both register sets and the software (or DMAC) has not completed writing of data for one register set, this bit indicates 0. When receive direction (DIR = 0) is set for the selected pipe, this bit indicates the same value as the BSTS bit.

Bit	Bit Name	Initial Value	R/W	Description
13	CSCLR	0	R/W*2	CSPLIT Status Clear When the software sets this bit to 1 with the host controller function selected, this module clears the CSSTS bit to 0. 0: Invalid 1: Clears the CSSTS bit to 0. To forcibly restart the next transfer with S-SPLIT in data transfer using split transactions, set this bit to 1 by the software. Since this module automatically clears the CSSTS bit to 0 at the end of C-SPLIT in normal split transactions, the software needs not clear the CSSTS bit. Clear the CSSTS bit with this bit while communication is halted by clearing the UACT bit or when it is clarified that no data transfer is performed by detection of Detach mode. Even if this bit is set to 1 when CSSTS is 0, CSSTS remains 0. When the function controller function is selected, be sure to set this bit to 0.
12	CSSTS	0	R	CSSTS Status When the host controller function is selected, this bit indicates the C-SPLIT status of split transactions. 0: START-SPLIT (S-SPLIT) transaction is being processed or no split transaction is used. 1: C-SPLIT transaction is being processed. This module sets this bit to 1 when starting C-SPLIT, and clears this bit to 0 when C-SPLIT end is detected. The value of this bit is valid only when the host controller function is selected.
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
10	ATREPM	0	R/W	Auto-Response Mode Enables or disables auto-response for the selected pipe. 0: Auto-response is disabled. 1: Auto-response is enabled. When the function controller function is selected and the transfer type of the selected pipe is set to bulk transfer, this bit can be set to 1. When this bit is 1, this module sends responses to tokens from the USB host as follows: (1) When the selected pipe is set for Bulk-IN transfer (TYPE = 01 and DIR = 1) When ATREPM = 1 and PID = BUF, this module sends a Zero-Length packet in response to the IN-Token. Each time this module receives ACK from the USB host (flow of one transaction: receiving IN-Token -> sending Zero Length packet -> receiving ACK), this module updates the sequence toggle bit (DATA-PID) by toggling it. No BRDY interrupt or BEMP interrupt is generated. (2) When the selected pipe is set for Bulk-OUT transfer (TYPE = 01 and DIR = 0) When ATREPM = 1 and PID = BUF, this module sends NAK in response to the OUT-Token (or PING-Token) and generates an NRDY interrupt. Modify this bit when CSSTS = 0 and PID = NAK. When setting this bit to 1 after changing the PID bits for the pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK. Be sure to set this bit to 1 for USB communication when the FIFO buffer is empty. Do not write data to the FIFO buffer during USB communication with this bit set to 1. When the selected pipe is set for isochronous transfer, be sure to set this bit to 0. When the host controller function is selected, be sure to set this bit to 0.

Bit	Bit Name	Initial Value	R/W	Description
9	ACLRM	0	R/W	Buffer Auto-Clear Mode Enables or disables buffer auto-clear mode for the selected pipe. 0: Buffer auto-clear mode is disabled. 1: Buffer auto-clear mode is enabled. (All buffers are initialized.) To completely delete the data in the FIFO buffer allocated to the pipe, write 1 and then 0 continuously to the ACLRM bit. Table 32.10 shows data cleared by this module when this bit is set to 1 and then 0 and cases where such data is cleared. Modify this bit when CSSTS = 0 and PID = NAK. When setting this bit to 1 after changing the PID bits for the pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.
8	SQCLR	0	R/W*[1]	Toggle Bit Clear Set this bit to 1 to clear the expected value (in DATA0) of the sequence toggle bit for the next transaction of the selected pipe. 0: Invalid 1: The expected value is cleared in DATA0. When the software sets this bit to 1, this module sets the expected value of the sequence toggle bit of the pipe in DATA0. This module always indicates SQCLR = 0. When this bit is set to 1 for a Bulk-Out transfer pipe with the host controller function selected, this module starts the next transfer with the PING-token for the pipe. Set the SQCLR bit to 1 when CSCTS = 0 and PID = NAK. When setting this bit to 1 after changing the PID bits for the selected pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.

Bit	Bit Name	Initial Value	R/W	Description
7	SQSET	0	R/W*[1]	Toggle Bit Set Set this bit to 1 to set the expected value of the sequence toggle bit for the next transaction of the selected pipe. 0: Invalid 1: The expected value is set in DATA1. When the software sets this bit to 1, this module sets the expected value of the sequence toggle bit of the pipe in DATA1. This module always indicates SQSET = 0. Set the SQSET bit to 1 when CSCTS = 0 and PID = NAK. When setting this bit to 1 after changing the PID bits for the pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.
6	SQMON	0	R	Toggle Bit Check Indicates the expected value of the sequence toggle bit for the next transaction of the selected pipe. 0: DATA0 1: DATA1 If the pipe is not the isochronous transfer type, when a transaction is successfully processed, this module toggles this bit. However, when a DATA-PID mismatch occurs in the receive direction transfer, this bit is not toggled.
5	PBUSY	0	R	Pipe Busy Indicates whether the pipe is currently used in the USB bus or not. 0: The selected pipe is not used in the USB bus. 1: The selected pipe is being used in the USB bus. When this module starts the USB transaction for the selected pipe, this module sets this bit to 1. This module clears this bit to 0 upon completion of each transaction. After the software sets PID = NAK, read this bit to see if changing the pipe setting is enabled or not.
4 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
1, 0	PID[1:0]	00	R/W	Response PID Specify a response used in the next transaction for the selected pipe. 00: NAK response 01: BUF response (depending on buffer state) 10: STALL response 11: STALL response These bits are set to NAK by default. To perform USB transfer with the selected pipe, change the setting of these bits to BUF. Tables 32.11 and 32.12 show the basic operation (with no error in packets) of this module in each setting of the PID bits. When changing these bits from BUF to NAK by the software while the pipe is in USB communication, write 00 (NAK) to these bits and then check PBUSY = 1 to confirm that the USB transfer of the pipe entered the NAK state. However, when this module changed these bits to NAK, the software does not have to check the PBUSY bit. This module modifies these bits in the following cases. • When the pipe is in the receive direction and the software sets the SHTNAK bit of the selected pipe to 1, this module indicates PID = NAK when this module recognizes the transfer end. • When this module receives data with a payload exceeding the MaxPacketSize value for the pipe, this module indicates PID = STALL (11). • When this module detects a USB bus reset with the function control function selected, this module indicates PID = NAK. • When this module detects a CRC error or another receive error three times in a row with the host control function selected, this module indicates PID = NAK. • When this module receives a STALL handshake with the host control function selected, this module indicates PID = STALL (11). Set these bits as follows: • To change the state from NAK (00) to STALL, write 10. • To change the state from BUF (01) to STALL, write 11. • To change the state from STALL (11) to NAK, write 10 then 00. • To change the state from STALL to BUF, set these bits to NAK and then to BUF.

Notes: 1. Only reading 0 and writing 1 are enabled.
2. Only writing 1 is enabled.

Table 32.9 Operations of BSTS Bit

DIR Bit	BFRE Bit	DCLRM Bit	Meaning of BSTS Bit
0	0	0	Indicates 1 when the FIFO buffer becomes ready to read receive data from the buffer, and indicates 0 upon completion of the data read.
		1	Setting prohibited
	1	0	Indicates 1 when the FIFO buffer becomes ready to read receive data from the buffer, and indicates 0 when the software sets BCLR = 1 after the buffer data read.
		1	Indicates 1 when the FIFO buffer becomes ready to read receive data from the buffer, and indicates 0 upon completion of the data read.
1	0	0	Indicates 1 when the FIFO buffer becomes ready to write transmit data to the buffer, and indicates 0 upon completion of the data write.
		1	Setting prohibited
	1	0	Setting prohibited
		1	Setting prohibited

Table 32.10 Data Cleared by This Module when ACLRM = 1

No.	Data Cleared by the ACLRM Bit	Clearing Timing
1	All data in the FIFO buffer (both sides for double FIFO buffer) allocated to the pipe	
2	Interval count value when the pipe is isochronous transfer type	When resetting the interval count value
3	Internal flags related to the BFRE bit	When changing the BFRE setting
4	FIFO buffer toggle control	When changing the DBLB setting
5	Internal flags related to the transaction count	When forcibly terminating the transaction count function

Table 32.11 Operations of This Module in Each Setting of PID Bits (when the Host Controller Function is Selected)

PID Bits	Transfer Type	Transfer Direction (DIR Bit)	Operation of This Module
00 (NAK)	Independent of the setting	Independent of the setting	Issues no token.
01 (BUF)	Bulk or interrupt	Independent of the setting	Issues tokens when UACT = 1 is set and the FIFO buffer for the pipe is ready to receive/transmit. Issues no token when UACT = 0 is set or the FIFO buffer is not ready to receive/transmit.
	Isochronous	Independent of the setting	Issues tokens irrespective of the state of the FIFO buffer for the pipe.
10 (STALL) or 11 (STALL)	Independent of the setting	Independent of the setting	Issues no token.

Table 32.12 Operations of This Module in Each Setting of PID Bits (when the Function Controller Function is Selected)

PID Bits	Transfer Type	Transfer Direction (DIR Bit)	Operation of This Module
00 (NAK)	Bulk or interrupt	Independent of the setting	Sends a NAK response to a token from the USB host. However, for the operation of this module when ATREPM = 1, see the description on the ATREPM bit.
	Isochronous	Independent of the setting	Sends no response to a token from the USB host.
01 (BUF)	Bulk	Receive direction (DIR = 0)	Receives data and sends an ACK response to the OUT token from the USB host when the FIFO buffer for the pipe is ready to receive. Otherwise, sends a NAK response. Sends an ACK response to the PING token from the USB host when the FIFO buffer for the selected pipe is ready to receive. Otherwise, sends a NYET response.
	Interrupt	Receive direction (DIR = 0)	Receives data and sends an ACK response to the OUT token from the USB host when the FIFO buffer for the pipe is ready to receive. Otherwise, sends a NAK response.
	Bulk or interrupt	Transmit direction (DIR = 1)	Sends data in response to a token from the USB host when the FIFO buffer for the pipe is ready to transmit. Otherwise, sends a NAK response.
	Isochronous	Receive direction (DIR = 0)	Receives data in response to the OUT token from the USB host when the FIFO buffer for the pipe is ready to receive. Otherwise, ignores the data.
		Transmit direction (DIR = 1)	Sends data in response to a token from the USB host when the FIFO buffer for the pipe is ready to transmit. Otherwise, sends a Zero-Length packet.
10 (STALL) or	Bulk or interrupt	Independent of the setting	Sends a STALL response to a token from the USB host.
11 (STALL)	Isochronous	Independent of the setting	Sends no response to a token from the USB host.

(2) PIPEnCTR (n = 6 to 9)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BSTS	—	CSCLR	CSSTS	—	—	ACLRM	SQCLR	SQSET	SQMON	PBUSY	—	—	—	PID[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W*1	R/W	R	R	R/W	R/W*1	R/W*1	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	BSTS	0	R	Buffer Status Indicates the state of the FIFO buffer of the selected pipe. 0: The buffer is not accessible. 1: The buffer is accessible. The meaning of this bit differs as shown in Table 32.9 depending on the settings of the DIR, BFRE, and DCLRM bits.
14	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
13	CSCLR	0	R/W*1	CSPLIT Status Clear Setting this bit to 1 clears the CSSTS bit of the selected pipe. 0: Invalid 1: Clears the CSSTS bit. To forcibly restart the next transfer with S-SPLIT in data transfer using split transactions, set this bit to 1 by the software. Since this module automatically clears the CSSTS bit to 0 at the end of C-SPLIT in normal split transactions, the software does not have to clear the CSSTS bit. Control the CSSTS bit with this bit while communication is halted by clearing the UACT bit or when it is clarified that no data transfer is performed by detection of Detach mode. Even if this bit is set to 1 when CSSTS is 0, CSSTS remains 0. When the function controller function is selected, be sure to set this bit to 0.

Bit	Bit Name	Initial Value	R/W	Description
12	CSSTS	0	R/W	When the host controller function is selected, this bit indicates the C-SPLIT status of split transactions. 0: START-SPLIT (S-SPLIT) transaction is being processed or the transaction is transferred without split transaction. 1: C-SPLIT transaction is being processed. This module sets this bit to 1 when starting C-SPLIT, and clears this bit to 0 when C-SPLIT end is detected. When the function controller function is selected, the read value of this bit is invalid. This bit is valid only when the host controller function is selected.
11, 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	ACLRM	0	R/W	Buffer Auto-Clear Mode*3*4 Enables or disables buffer auto-clear mode for the selected pipe. 0: Buffer auto-clear mode is disabled. 1: Buffer auto-clear mode is enabled. (All buffers are initialized.) To completely delete the data in the FIFO buffer allocated to the pipe, write 1 and then 0 continuously to the ACLRM bit. Table 32.13 shows data cleared by this module when this bit is set to 1 and then 0 and cases where such data is cleared. Modify this bit when CSSTS = 0, PID = NAK, and the pipe is not set in the CURPIPE bits. When setting this bit to 1 after changing the PID bits for the pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.

Bit	Bit Name	Initial Value	R/W	Description
8	SQCLR	0	R/W*[1]	Toggle Bit Clear*[3]*[4] Set this bit to 1 to clear the expected value (in DATA0) of the sequence toggle bit for the next transaction of the selected pipe. 0: Invalid 1: The expected value is cleared in DATA0. When the software sets this bit to 1, this module sets the expected value of the sequence toggle bit of the pipe in DATA0. This module always indicates SQCLR = 0. When this bit is set to 1 for a Bulk-Out transfer pipe with the host controller function selected, this module starts the next transfer with the PING-token for the pipe. Set the SQCLR bit to 1 when CSCTS = 0 and PID = NAK. When setting this bit to 1 after changing the PID bits for the pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.
7	SQSET	0	R/W*[1]	Toggle Bit Set*[3]*[4] Set this bit to 1 to set the expected value of the sequence toggle bit for the next transaction of the selected pipe. 0: Invalid 1: The expected value is set in DATA1. When the software sets this bit to 1, this module sets the expected value of the sequence toggle bit of the selected pipe in DATA1. This module always indicates SQSET = 0. Set the SQSET bit to 1 when CSCTS = 0 and PID = NAK. When setting this bit to 1 after changing the PID bits for the selected pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.

Bit	Bit Name	Initial Value	R/W	Description
6	SQMON	0	R	Toggle Bit Check Indicates the expected value of the sequence toggle bit for the next transaction of the pipe. 0: DATA0 1: DATA1 If the selected pipe that is not the isochronous transfer type, when a transaction is successfully processed, this module toggles this bit. However, when a DATA-PID mismatch occurs in the receive direction transfer, this bit is not toggled.
5	PBUSY	0	R	Pipe Busy Indicates whether the selected pipe is currently used in the USB bus or not. 0: The selected pipe is not used in the USB bus. 1: The selected pipe is being used in the USB bus. When this module starts the USB transaction for the selected pipe, this module sets this bit to 1. This module clears this bit to 0 upon completion of each transaction. After the software sets PID = NAK, read this bit to see if changing the pipe setting is enabled or not.
4 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
1, 0	PID[1:0]	00	R/W	Response PID Specify a response used in the next transaction for the selected pipe. 00: NAK response 01: BUF response (depending on buffer state) 10: STALL response 11: STALL response These bits are set to NAK by default. To perform USB transfer with the selected pipe, change the setting of these bits to BUF. Tables 32.13 and 32.14 show the basic operation (with no error in packets) of this module in each setting of the PID bits. When changing these bits from BUF to NAK by the software while the pipe is in USB communication, write 00 (NAK) to these bits and then check PBUSY = 1 to confirm that the USB transfer of the selected pipe entered the NAK state. However, when this module changed these bits to NAK, the software needs not check the PBUSY bit. This module modifies these bits in the following cases. • When the selected pipe is in the receive direction and the software sets the SHTNAK bit of the selected pipe to 1, this module indicates PID = NAK when this module recognizes the transfer end. • When this module receives data with a payload exceeding the MaxPacketSize value for the pipe, this module indicates PID = STALL (11). • When this module detects a USB bus reset with the function control function selected, this module indicates PID = NAK. • When this module detects a CRC error or another receive error three times in a row with the host control function selected, this module indicates PID = NAK. • When this module receives a STALL handshake with the host control function selected, this module indicates PID = STALL (11). Set these bits as follows: • To change the state from NAK (00) to STALL, write 10. • To change the state from BUF (01) to STALL, write 11. • To change the state from STALL (11) to NAK, write 10 then 00. • To change the state from STALL to BUF, set these bits to NAK and then to BUF.

Notes: 1. Only reading 0 and writing 1 are enabled.
2. Only writing 1 is enabled.
3. Set the ACLRM, SQCLR, or SQSET bit when CSSTS = 0, PID = NAK, and the selected pipe is not set in the CURPIPE bits.
4. When setting the ACLRM, SQCLR, or SQSET bit after changing the PID bits from BUF to NAK, check that CSSTS = 0 and PBUSY = 0 for the pipe. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.

Table 32.13 Data Cleared by This Module when ACLRM = 1

No.	Data Cleared by the ACLRM Bit	Clearing Timing
1	All data in the FIFO buffer allocated to the selected pipe	
2	Interval count value when the host controller function is selected and the selected pipe is interrupt transfer type	When resetting the interval count value
3	Internal flags related to the BFRE bit	When changing the BFRE setting
4	Internal flags related to the transaction count	When forcibly terminating the transaction count function

32.3.36 Pipe n Transaction Counter Enable Register (PIPnTRE) (n = 1 to 5)

PIPnTRE enables or disables the transaction counter function and clears the counter for pipes 1 to 5.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	TRENB	TRCLR	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
9	TRENB	0	R/W	Transaction Counter Enable Enables or disables the transaction counter function. 0: The transaction counter function is disabled. 1: The transaction counter function is enabled. When the software sets the number of total packets in the TRNCNT bits in PIPEnTRN for the receive pipe and then sets this bit to 1, this module controls the following when it received the same number of packets as the setting of the TRNCNT bits. When continuous communication mode is used (CNTMD = 1), this module toggles the received data to the CPU even if the FIFO buffer is not full at the end of reception. When SHTNAK = 1, this module changes the PID bits for the corresponding pipe to NAK when this module received the same number of packets as the setting of the TRNCNT bits. When BFRE = 1, this module asserts the BRDY interrupt when this module received the same number of packets as the setting of the TRNCNT bits and read the receeive data completely. For transmit pipes, set this bit to 0. When the transaction counter function is not used, set this bit to 0. When using the transaction counter function, set the TRNCNT bits and then set this bit to 1. Furthermore, set this bit to 1 before receiving the first packet that is included in the transaction count range.
8	TRCLR	0	R/W	Transaction Counter Clear Clears the current count value of the transaction counter for the pipe and indicates TRCLR = 0. 0: Invalid 1: The current count value is cleared.
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Note: Change the bits in this register when CSSTS = 0 and PID = NAK.
When changing the bits in this register after changing the PID bits for the pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.

32.3.37 Pipe n Transaction Counter Register (PIPEnTRN) (n = 1 to 5)

PIPnTRE is a transaction counter for pipes 1 to 5.

This register is initialized by a power-on reset, but the setting of this register is retained through a USB bus reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TRNCNT[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 0	TRNCNT [15:0]	All 0	R/W	Transaction Counter Writing: Specify the number of transactions of DMA transfer. Reading: When TRENB = 0, the set number of transactions is indicated. When TRENB = 1, the number of current transactions is indicated. This module increments (+1) the value of these bits when the following conditions are all satisfied. TRENB = 1 TRCNT value ≠ current count value +1 when a packet is received. The payload of the received packet equals the value of the MXPS bits. This module clears these bits to 0 when any of the following is satisfied. When the following conditions are all satisfied - TRENB = 1 - TRCNT value = current count value +1 when a packet is received. - The payload of the received packet equals the value of the MXPS bits. When the following conditions are all satisfied - TRENB = 1 - A short packet is received. When the following conditions are all satisfied - TRENB = 1 - The software sets the TRCLR bit to 1.

Bit	Bit Name	Initial Value	R/W	Description
15 to 0	TRNCNT [15:0]	All 0	R/W	For transmit pipes, set these bits to all 0. When the transaction counter function is not used, set these bits to all 0. Change these bits when CSSTS = 0, PID = NAK, and TRENB = 0. When setting these bits to 1 after changing the PID bits for the pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK. When changing these bits, set TRCNT = 1 and then set TRENB = 1.

32.3.38 Device Address n Configuration Register (DEVADDn) (n = 0 to A)

DEVADDn specifies the address and port number of the HUB connected to a peripheral device as a communication target, as well as the transfer rate of the peripheral device, for pipes 0 to A.

When the host controller function is selected, be sure to set the bits in this register before starting communication for each pipe.

Change the bits in this register when there is no valid pipe that uses the setting of these bits. A valid pipe is defined as a pipe that meets the following two conditions.

1. The setting of the DEVSEL bits specifies this register.
2. The PID bits for the selected pipe are set to BUF or the selected pipe is the DCP with SUREQ = 1

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	UPPHUB[3:0]				HUBPORT[2:0]			USBSPD[1:0]		—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14 to 11	UPPHUB [3:0]	0000	R/W	HUB Register Specify the USB address of the HUB connected to the peripheral device as a communication target. 0000: The peripheral device is connected directly to the port of this LSI. 0001 to 1010: USB address of the HUB 1011 to 1111: Setting prohibited When the host controller function is selected, this module reads these bits to generate packets when executing split transactions. When the function controller function is selected, set these bits to 0000.

Bit	Bit Name	Initial Value	R/W	Description
10 to 8	HUBPORT [2:0]	000	R/W	HUB Port for Communication Target Device Specify the port number of the HUB connected to the peripheral device as a communication target. 000: The peripheral device is connected directly to the port of this LSI. 001 to 111: Port number of the HUB When the host controller function is selected, this module reads these bits to generate packets when executing split transactions. When the function controller function is selected, set these bits to 000.
7, 6	USBSPD [1:0]	00	R/W	Communication Target Device Transfer Rate Specify the USB transfer rate of the peripheral device as a communication target. 00: DEVADDn is not used. 01: Low speed 10: Full speed 11: High speed When the host controller function is selected, this module reads these bits to generate packets. When the function controller function is selected, set these bits to 00.
5 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

32.4 Operation

32.4.1 System Control and Oscillation Control

This section describes register operations required for the initial settings of this module and the registers required for the power consumption control.

(1) Reset

Table 32.14 lists the reset types of this module. For initialization states of registers after each reset, see section 32.3, Register Descriptions.

Table 32.14 Reset Types

Reset Name	Operation
Power-on reset	RESETP pin
AP system reset	RESETA pin
Power area reset	Register in the SYSC
Software reset	Register in the CPGA

(2) Setting Selection of Controller Functions

This module can select the host controller function or the function controller function. Select either of these functions by the DCFM bit in SYSCFG. Set the DCFM bit during the initial setting immediately after a power-on reset or in the D+ pull-up disabled state (DPRPU = 0) and D+/D- pull-down disabled state (DRPD = 0).

(3) Enabling High-Speed Operation

This module can set the USB transmission rate (communication bit rate) by the software.

When the host controller function is selected, high-speed operation or full-speed/low-speed operation is selectable. When the function controller function is selected, high-speed operation or full-speed operation is selectable. To enable high-speed operation with this module, set the HSE bit in SYSCFG to 1. When high-speed operation is enabled, this module executes the reset handshake protocol and automatically sets the USB transmission rate. The reset handshake result can be checked by the RHST bits in DVSTCTR.

When high-speed operation is disabled, this module operates in full speed or low speed when the host controller function is selected, and operates only in full speed when the function controller function is selected.

When the host controller function is selected, change the HSE bit during a period from ATTACH detection until a bus reset. When the host controller function is selected, change the HSE bit in the D+ pull-up disabled state (DPRPU = 0).

(4) USB Data Bus Resistor Control

Figure 32.1 shows the connection between this module and the USB connector.

This module incorporates a pull-up resistor of the D+ signal and pull-down resistors of the D+ and D- signals. Specify pull-up and pull-down for each signal using the DPRPU and DRPD bits in SYSCFG.

Furthermore, this module controls the terminating resistors of the D+ and D- signals in high-speed operation, and the output resistors in full-speed operation. This module automatically switches the on-chip resistors after connection to the host controller or the peripheral device upon detecting a reset handshake, suspended state, or resume.

When the function controller function is selected and the DPRPU bit in SYSCFG is set to 0 during communication with the host controller, this module disables the pull-up resistors (or terminating resistors) of the USB data line. Therefore, the USB host can be notified of a disconnection from the device.

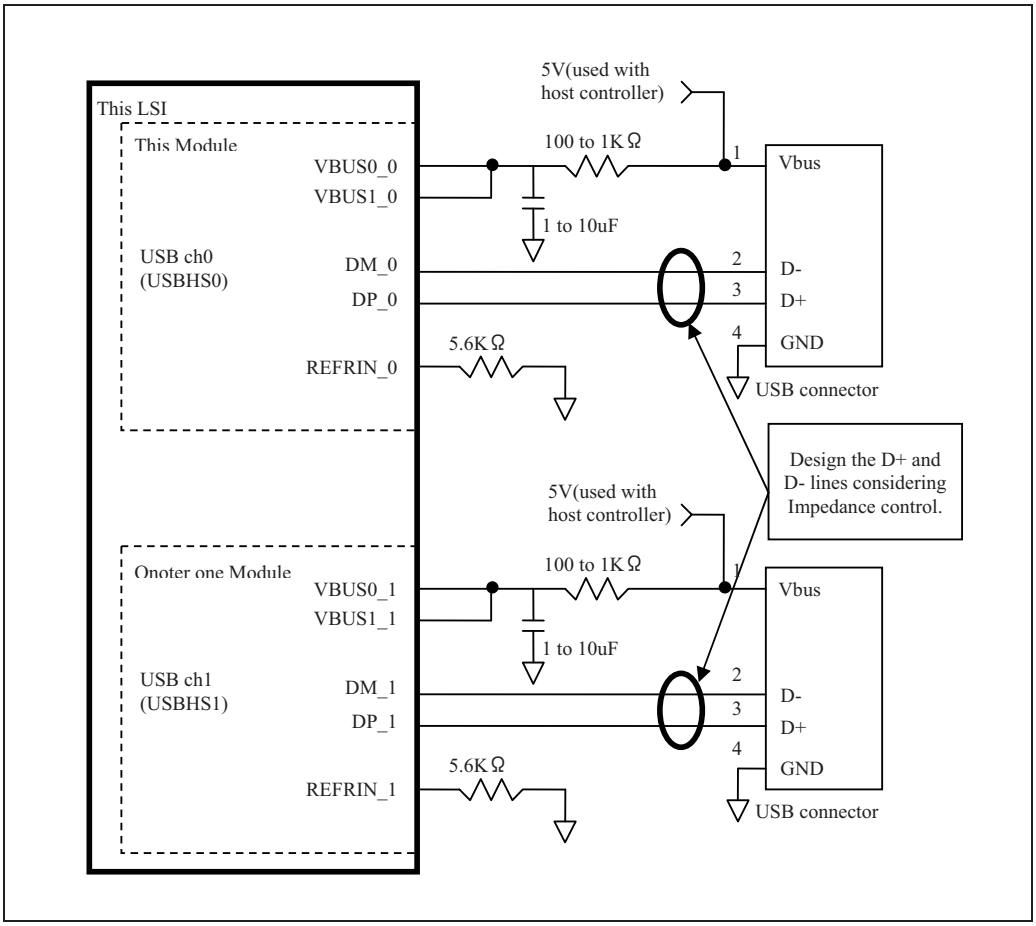


Figure 32.1 Connection to the USB Connector

(5) Software reset when the USB disconnection is detected

Issue a software reset of the USBHS module when the USB disconnection is detected. If the DMA interface is being used, issue a software reset of the USBHS-DMAC module as well. A software reset can be issued via a register in the CPGA.

Whether or not the USB disconnection is detected can be determined by the VBSTS in the INTSTS0 register when the function controller function is selected or the DTCH bit in the INTSTS1 register when the host controller function is selected.

32.4.2 Interrupt Function

Table 32.15 lists the interrupt generating conditions of this module.

When any of the following interrupt generating conditions are satisfied and the interrupt output is enabled by the corresponding interrupt enable register, this module outputs a USB interrupt request to the interrupt controller (INTC).

Table 32.15 Interrupt Generating Conditions

Bit	Interrupt Name	Interrupt Generating Conditions	Function	Related Status
VBINT	VBUS interrupt	When VBUS0_0 and VBUS1_0 input pin state change is detected (both L to H and H to L)	Host and function controller functions	VBSTS
RESM	Resume interrupt	When a USB bus state change is detected in the suspended state (J-State to K-State or J-State to SE0)	Function	—
SOFR	Frame number update interrupt	[When the host controller function is selected] When an SOF packet with a different frame number is sent [When the function controller function is selected] SOFRM = 0: When an SOF packet with a different frame number is received SOFRM = 1: When an SOF packet with a μ frame number of 0 cannot be received due to damage, etc.	Host and function controller functions	—
DVST	Device state transition interrupt	When a device state transition is detected USB bus reset detected Suspended state detected SET_ADDRESS request received SET_CONFIGURATION request received	Function	DVSQ

Bit	Interrupt Name	Interrupt Generating Conditions	Function	Related Status
CTRT	Control transfer stage transition interrupt	When a control transfer stage transition is detected Setup stage completed Control write transfer status stage shifted Control read transfer status stage shifted Control transfer completed Control transfer sequence error occurred	Function	CTSQ
BEMP	Buffer empty interrupt	When the buffer becomes empty after sending all buffer memory data When a packet with a size exceeding the maximum packet size is received	Host and function controller functions	BEMPSTS.PIPEBEMP
NRDY	Buffer not ready interrupt	[When the host controller function is selected] When STALL from the peripheral device in response to the issued token is received When a response from the peripheral device in response to the issued token cannot be received successfully (no response three times in a row or a packet receive error three times in a row) When an overrun or underrun error occurred during isochronous transfer [When the function controller function is selected] When NAK is sent in response to IN token, OUTtoken, or PING token When a CRC error or bit stuffing error occurred during data reception in isochronous transfer When an overrun or underrun error occurred during data reception in isochronous transfer	Host and function controller functions	NRDYSTS.PIPENRDY

Bit	Interrupt Name	Interrupt Generating Conditions	Function	Related Status
BRDY	Buffer ready interrupt	When the buffer becomes ready for reading or writing	Host and function controller functions	BRDYSTS. PIPEBRDY
OVRCR	OVRCR interrupt	When an OVCN_0/OVCN2 input pin state change is detected	Host and function controller functions	OVCMON
BCHG	Bus change interrupt	When a USB bus state change is detected	Host and function controller functions	—
DTCH	Disconnection in full-speed operation	When a disconnection from the peripheral device is detected during full-speed operation	Host controller function	—
ATTCH	Device connection	When J-STATE or K-STATE where USB bus state continues for 2.5 μs is detected This interrupt is available for detection of connection to a peripheral device.	Host controller function	—
EOFERR	EOF error	When an EOF error of the peripheral device is detected	Host controller function	—
SACK	SETUP	When an ACK response to the setup transaction is received	Host controller function	—
SIGN	SETUP error	When an error (no response or ACK packet damage) is detected three times in a row in the setup transaction	Host controller function	—

Note: These bits in this table are those of INTSTS0 if any register's name is not indicated.

Figure 32.2 shows a block diagram of the interrupt circuit of this module.

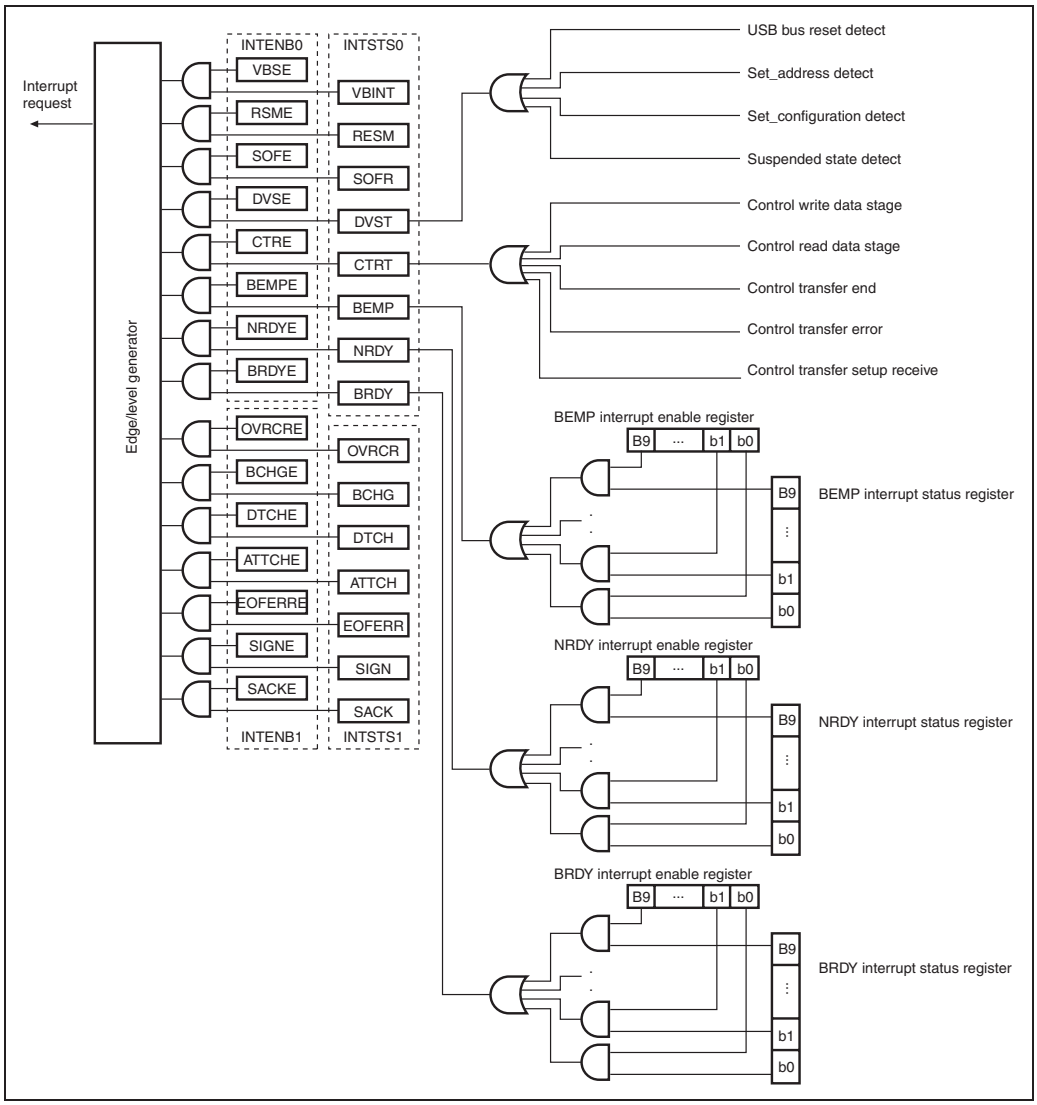


Figure 32.2 Block Diagram of Interrupt Circuit

(1) BRDY Interrupt

A BRDY interrupt can be generated when either of the host controller function and function controller functions is selected. When the following conditions in each pipe are satisfied, this module sets the corresponding bit in BRDYSTS to 1. At this time, when the PIPEBRDYE bit for the pipe in BRDYENB is set to 1 and the BRDYE bit in INTENB0 is set to 1 by the software, this module generates a BRDY interrupt.

BRDY interrupt generating conditions and clearing method depend on the settings of the BRDYM bit and the BFRE bit for each pipe.

(a) When BRDY interrupt disable (BRDYM = 0) and BRDY interrupt output enable (BFRE = 0) at data reception/transmission are specified

With this setting, a BRDY interrupt indicates that the FIFO port is accessible.

This module generates an internal BRDY interrupt request trigger when the following conditions are satisfied, and sets the PIPEBRDY bit corresponding to the request trigger pipe to 1.

1. Pipes set for the transmit direction

- When the software changes the DIR bit from 0 to 1
- When this module finishes sending a packet of the pipe while data write from the CPU to the FIFO buffer allocated to the pipe is disabled (BSTS = 0)

  When continuous communication mode is selected, this module generates a BRDY interrupt request trigger upon completion of sending data for one side of the FIFO buffer.
- When a double FIFO buffer is specified and one side of the FIFO buffer is empty when data write to the other side of the FIFO buffer is completed

  Even if one side of the FIFO buffer becomes empty while the other side is in data write processing, no BRDY interrupt is generated until the ongoing data write finishes.
- When this module generates a buffer flush for a pipe of isochronous transfer type
- When the FIFO buffer becomes write enable state by writing 1 to the ACLRM bit

No BRDY interrupt request trigger is generated for the DCP (in data transmission of control transfer).

2. Pipes set for the receive direction

- When this module receives a packet successfully and the FIFO buffer becomes ready for reading while data read access from the CPU to the FIFO buffer allocated to the pipe is disabled (BSTS = 0)

  No BRDY interrupt request trigger is generated in transactions with incorrect data PID.

  When continuous communication mode is selected, no BRDY interrupt request trigger is generated for packets with a MaxPacketSize data size and when the FIFO buffer still has available space.

  When this module receives a short packet, this module generates a BRDY interrupt request trigger even if the buffer has available space.

  When a transaction counter is used, this module generates a BRDY interrupt request trigger when this module receives a packet with a size of the set value even if the FIFO buffer still has available space.

  When a double FIFO buffer is specified and one side of the FIFO buffer is ready for reading when data read from the other side of the FIFO buffer is completed

  Even if data read for one side of the FIFO buffer is completed while the other side is undergoing data read, no BRDY interrupt request trigger is generated until the ongoing data read finishes.

This interrupt is not generated in communication in the control transfer status stage when the function controller function is selected.

The software can clear the PIPEBRDY interrupt status of the pipe by writing 0 to the PIPEBRDY bit for the pipe in BRDYSTS. At this time, write 1 to the bits corresponding to other pipes.

Be sure to clear the BRDY interrupt status before accessing the FIFO buffer.

(b) When BRDY interrupt disable (BRDYM = 0) and BRDY interrupt output enable (BFRE = 1) at the end of data read are specified

With this setting, this module determines that a **BRDY** interrupt is generated upon completion of reading all data of one transfer in a receive pipe, and sets the bit for the pipe in this register to 1.

This module determines that the last data of a transfer was received in either of the following cases.

- A Zero-Length packet or another short packet is received.
- A transaction counter (TRNCNT bits) is used and a packet with a size of the value of the TRNCNT bits is received.

When either of these conditions is satisfied and the data read is completed, this module determines that reading all data for one transfer is completed.

When this module receives a Zero-Length packet with the FIFO buffer empty, this module determines that reading all data for one transfer is completed when the Zero-Length packet data is toggled to the CPU. In this case, write 1 to the BCLR bit in the corresponding FIFOCTR register by the software to start the next transfer.

With this setting, this module generates no BRDY interrupt for transmit pipes.

The software can clear the PIPEBRDY interrupt status of the pipe to 0 by writing 0 to the PIPEBRDY bit for the pipe. At this time, write 1 to the bits corresponding to other pipes.

When using this mode, do not change the BFRE setting until the processing for one transfer is completed.

To change the BFRE bit during processing, clear all FIFO buffers for the pipe by the ACLRM bit.

(c) When BRDY interrupt enable (BRDYM = 1) and BRDY interrupt output enable (BFRE = 0) at data reception/transmission are specified

With this setting, the value of the PIPEBRDY bit varies with the value of the **BSTS** bit for each pipe. That is, this module indicates 1 or 0 of the BRDY interrupt status according to the FIFO buffer status.

1. Pipes set for the transmit direction

   When the FIFO port is ready to write data, the PIPEBRDY bit indicates 1. When the FIFO port is not ready to write data, the PIPEBRDY bit indicates 0.

   However, even if the transmit pipe of the DCP is ready to write data, no BRDY interrupt is asserted.
2. Pipes set for the receive direction

   When the FIFO port is ready to read data, the PIPEBRDY bit indicates 1. When all data is read from the FIFO port (reading disabled), the PIPEBRDY bit indicates 0.

   When this module receives a Zero-Length packet with the FIFO buffer empty, this module indicates 1 with the corresponding bit until 1 is written to BCLR by the software, and continues to assert the BRDY interrupt.

   With this setting, the software cannot clear the PIPEBRDY bit to 0.

   When BRDYM = 1, set the BFRE bit to 0 for all pipes.

Figure 32.3 shows the BRDY interrupt generation timing.

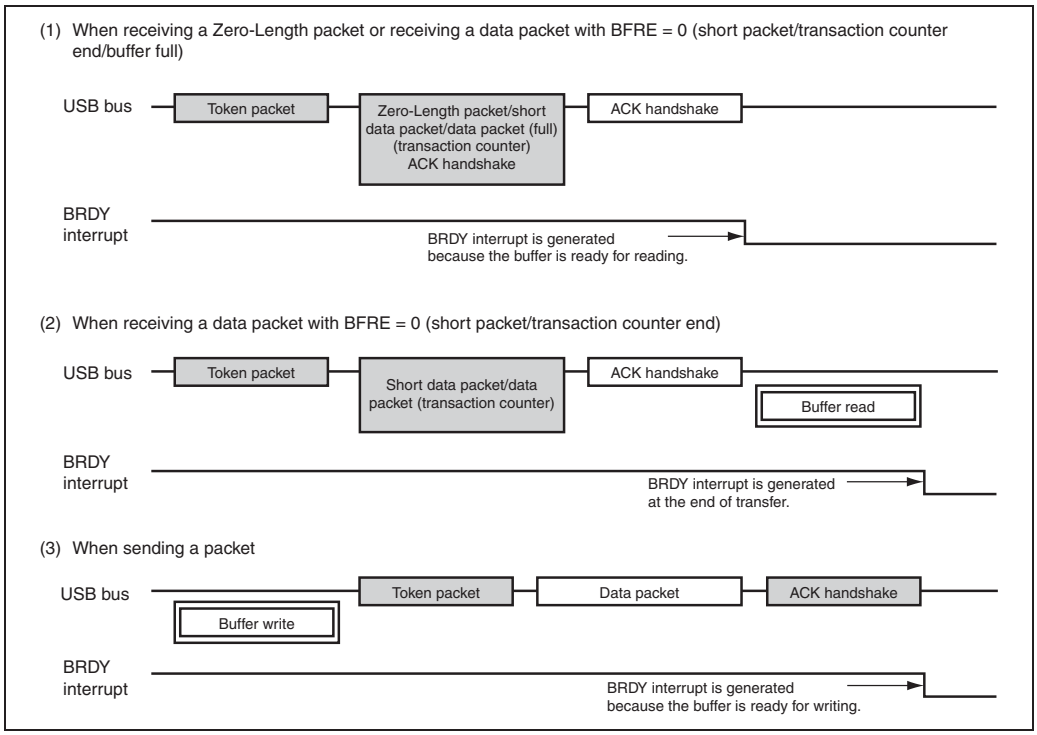


Figure 32.3 BRDY Interrupt Generation Timing

(2) NRDY Interrupt

When this module generates an internal NRDY interrupt request for the pipe in which PID = BUF is set by the software, this module indicates PIPENRDY = 1 for the pipe in NRDYSTS. At this time, when 1 is set in the corresponding bit in NRDYENB by the software, this module indicates NRDY = 1 in INTSTS0 and generates a USB interrupt.

The following shows the conditions for this module to generate an internal NRDY interrupt request for a pipe.

However, the execution of the SETUP transaction when the host controller function is selected is excluded from the following interrupt generation conditions. In the SETUP transaction when the host controller function is selected, this module detects an SACK interrupt or SIGN interrupt.

Furthermore, when executing the control transfer status stage with the function controller function selected, this module generates no interrupt request.

(a) When the host controller function is selected and no split transaction occurs

1. Pipes in the transmit direction

   This module detects an NRDY interrupt when either of the following conditions is satisfied.

   — When the OUT token transmit timing comes with no transmit data in the FIFO buffer in an isochronous transfer-type pipe

   At this time, this module sends a Zero-Length packet following the OUT token, and then indicates PIPENRDY = 1 for the pipe and OVRN = 1.

   — In communication other than SETUP transaction for a pipe of other than isochronous transfer type, when no response from the peripheral device (timeout is detected without detecting a handshake packet from the peripheral device) or an error in a packet from the peripheral device occurred three times in a row in an arbitrary combination

   At this time, this module indicates PIPENRDY = 1 for the pipe and changes the PID bits for the pipe to NAK.

   — When this module receives a STALL handshake from the peripheral device in communication other than the SETUP transaction (including STALL to PING as well as STALL to OUT)

   At this time, this module indicates PIPENRDY = 1 for the pipe and changes the PID bits for the pipe to STALL (11).

2. Pipes in the receive direction
   — When the IN token transmit timing comes with the FIFO buffer occupied in an isochronous transfer-type pipe

     At this time, this module ignores the receive data in response to the IN Token and indicates PIPENRDY = 1 for the pipe and OVRN = 1.

     Furthermore, when a packet error is detected in the receive data in response to the IN Token, this module also indicates CRCE = 1.

     In communication for a pipe of other than isochronous transfer type, when no response from the peripheral device to the IN token sent from this module (timeout is detected without detecting a data packet from the peripheral device) or an error in a packet from the peripheral device occurred three times in a row in an arbitrary combination

     At this time, this module indicates PIPENRDY = 1 for the pipe and changes the PID bits for the pipe to NAK.

     In communication for an isochronous transfer-type pipe, when this module receives no response from the peripheral device to the IN token sent from this module (timeout is detected without detecting a data packet from the peripheral device) or an error in a packet from the peripheral device is detected

     At this time, this module indicates PIPENRDY = 1 for the pipe but does not change the PID bits for the pipe.
   — In communication for an isochronous transfer-type pipe, when a CRC error or a bit stuffing error is detected in the received data packet

     At this time, this module indicates PIPENRDY = 1 for the pipe and CRCE = 1.
   — When this module receives a STALL handshake

     At this time, this module indicates PIPENRDY = 1 for the pipe and changes the PID bits for the pipe to STALL.

(b) When the host controller function is selected and split transactions occur

1. Pipes in the transmit direction
   — When the OUT token transmit timing comes with no transmit data in the FIFO buffer in an isochronous transfer-type pipe

     At this time, this module indicates PIPENRDY = 1 for the pipe and OVRN = 1 when it sends the Start-Split transaction (S-SPLIT). This module also sends a Zero-Length packet following the OUT token.
   — In the S-SPLIT or Complete-Sprit transaction (C-SPLIT) for a pipe of other than isochronous transfer type, when no response from the HUB (timeout is detected without detecting a handshake packet from the HUB) or an error in a packet from the HUB occurred three times in a row in an arbitrary combination

At this time, this module indicates PIPENRDY = 1 for the pipe and changes the PID bits for the pipe to NAK.

When this module detects an NRDY interrupt when sending C-SPLIT, this module clears the CSSTS bit to 0.

— When this module receives a STALL handshake in response to C-SPLIT

At this time, this module indicates PIPENRDY = 1 for the pipe and changes the PID bits for the pipe to STALL (11). This module also clears the CSSTS bit to 0.

However, this interrupt is not detected in the SETUP transaction.

— When this module receives NYET in response to C-SPLIT with microFrame = 4 in an interrupt transfer-type pipe

— At this time, this module indicates PIPENRDY = 1 for the pipe and clears the CSSTS bit to 0 but does not change the PID bits for the pipe.

2. Pipes in the receive direction

— When the IN token transmit timing comes with the FIFO buffer occupied in an isochronous transfer-type pipe

At this time, this module indicates PIPENRDY = 1 for the pipe and OVRN = 1 when it sends S-SPLIT. This module also ignores the receive data in response to the IN token.

— In a transfer for a bulk transfer-type pipe or in a transfer other than the SETUP transaction of the DCP, when no response from the HUB in response to the IN token from this module when sending S-SPLIT or C-SPLIT (timeout is detected without detecting a handshake packet from the HUB) or an error in a packet from the HUB occurred three times in a row in an arbitrary combination

At this time, this module indicates PIPENRDY = 1 for the pipe and changes the PID bits for the pipe to NAK. When this condition is generated in the C-SPLIT transaction, this module clears the CSSTS bit to 0.

— In the C-SPLIT transaction for a pipe of isochronous or interrupt type, when no response from the HUB in response to the IN token from this module (timeout is detected without detecting a data packet from the HUB) or an error in a packet from the HUB occurred three times in a row in an arbitrary combination

When this condition is generated in an interrupt transfer-type pipe, this module indicates PIPENRDY = 1 for the pipe, changes the PID bits for the pipe to NAK, and clears the CSSTS bit to 0.

When this condition is generated in an isochronous transfer-type pipe, this module indicates PIPENRDY = 1 for the pipe and CRCE = 1 and clears the CSSTS to 0, bit to 0 but does not change the PID bits for the pipe.

— When this module receives a STALL handshake response during the C-SPLIT transaction in a pipe of other than isochronous transfer type

At this time, this module indicates PIPENRDY = 1 for the pipe, changes the PID bits for the pipe to STALL (11), and clears the CSSTS bit to 0.

— When this module receives a NYET in response to C-SPLIT with microFrame = 4 in a pipe of isochronous or interrupt transfer type

At this time, this module indicates PIPENRDY = 1 for the pipe and CRCE = 1 and clears the CSSTS bit to 0, but does not change the PID bits for the pipe.

(c) When the function controller function is selected

1. Pipes in the transmit direction

— When this module receives an IN token with no transmit data in the FIFO buffer

This module generates an NRDY interrupt request and indicates PIPENRDY = 1.

When the pipe in which the interrupt is generated is isochronous transfer type, this module sends a Zero-Length packet and indicates OVRN = 1.

2. Pipes in the receive direction pipe

— When this module receives an OUT token with the FIFO buffer occupied

When the pipe in which the interrupt is generated is isochronous transfer type, this module generates an NRDY interrupt request when this module receives an OUT token, and indicates PIPENRDY = 1 and OVRN = 1.

When the pipe in which the interrupt is generated is not isochroous transfer type, this module generates an NRDY interrupt request when this module sends an NAK handshake response after receiving data following the OUT token, and indicates PIPENRDY = 1.

However, this module generates no NRDY interrupt when resending data (in the case of DATA-PID mismatch) or when an error occurs in a data packet.

— When this module receives a PING token with the FIFO buffer occupied

This module generates an NRDY interrupt request when this module receives a PING token and indicates PIPENRDY = 1.

— When a packet is not received correctly within the interval frame in an isochroous transfer-type pipe

This module generates an NRDY interrupt request when this module receives SOF and indicates PIPENRDY = 1.

Figure 32.4 shows the NRDY interrupt generation timing when the function controller function is selected.

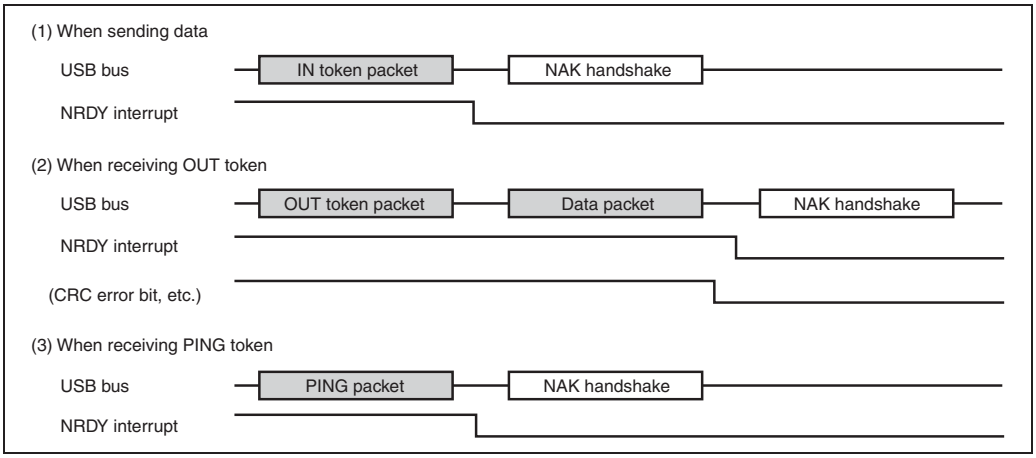


Figure 32.4 NRDY Interrupt Generation Timing when the Function Controller Function is Selected

(3) BEMP Interrupt

When this module detects a BEMP interrupt for the pipe in which PID = BUF is set by the software, this module indicates PIPEBEMP = 1 for the pipe in BEMPSTS. At this time, when 1 is set in the corresponding bit in BEMPENB by the software, this module indicates BEMP = 1 in INTSTS0 and generates a USB interrupt.

This module generates an internal BEMP interrupt request in the following cases.

1. Transmit direction pipes

   When the FIFO buffer for the pipe is empty at the end of transmission (including transmission of a Zero-Length packet)

   When single buffer is set for the FIFO buffer, this module generates an internal BEMP interrupt request concurrently with a BRDY interrupt for pipes other than DCP.
   However, this module generates no internal BEMP interrupt request in the following cases.

   — In the case of double buffer, when the software (DMAC) already started writing data to the FIFO buffer of the CPU at the end of transmission for one-side data
   — When the buffer is cleared (empty) by writing 1 to the ACLRM or BCLR bit.
   — When sending a Zero-Length packet (IN transfer) of the control transfer status stage when the function controller function is selected

2. Receive direction pipes

   When this module receives a packet with a data size exceeding the MaxPacketSize value

   In this case, this module generates a BEMP interrupt request and indicates the PIPEBEMP = 1 for the pipe, ignores the received data, and changes the PID bits for the pipe to STALL (11).

   At this time, this module sends no response when the host controller function is selected, and sends a STALL response when the function controller function is selected.

   However, this module generates no BEMP interrupt request in the following cases.

   — When this module detects a CRC error or bit stuffing error in the receive data

   — When executing the SETUP transaction

   Writing 0 to the PIPEBEMP bits clears the status.

   Writing 0 to the PIPEBEMP bits has no effect on the operation of this module.

Figure 32.5 shows the BEMP interrupt generation timing when the function controller function is selected.

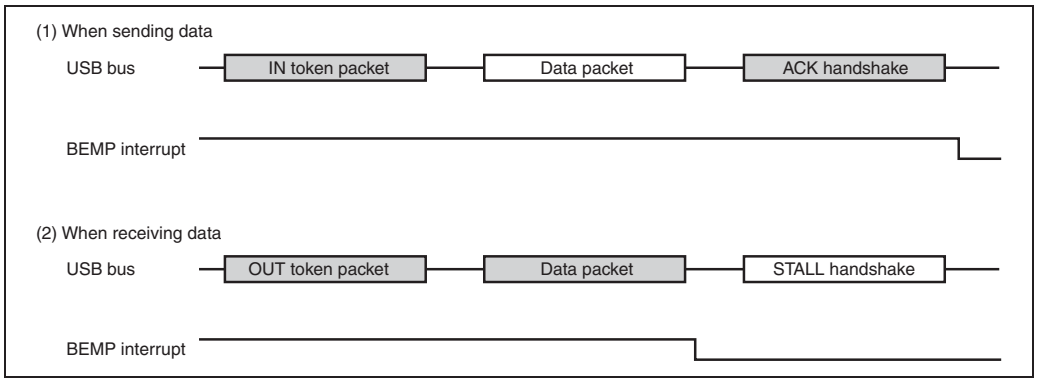


Figure 32.5 BEMP Interrupt Generation Timing when the Function Controller Function is Selected

(4) Device State Transition Interrupt

Figure 32.6 shows the device state transitions of this module. This module controls device states and generates device state transition interrupts. However, when returning from the suspended state (detecting the resume signal), this module detects the transition with a resume interrupt. The device state transition interrupt is enabled or disabled by setting INTENB0. The current device state can be monitored using the DVSQ bits in INTSTS0.

When this module shifts to the default state, a device state transition interrupt occurs after executing the reset handshake protocol.

This module controls the device states only when the function controller function is selected. In addition, device state transition interrupts are generated only when the function controller function is selected.

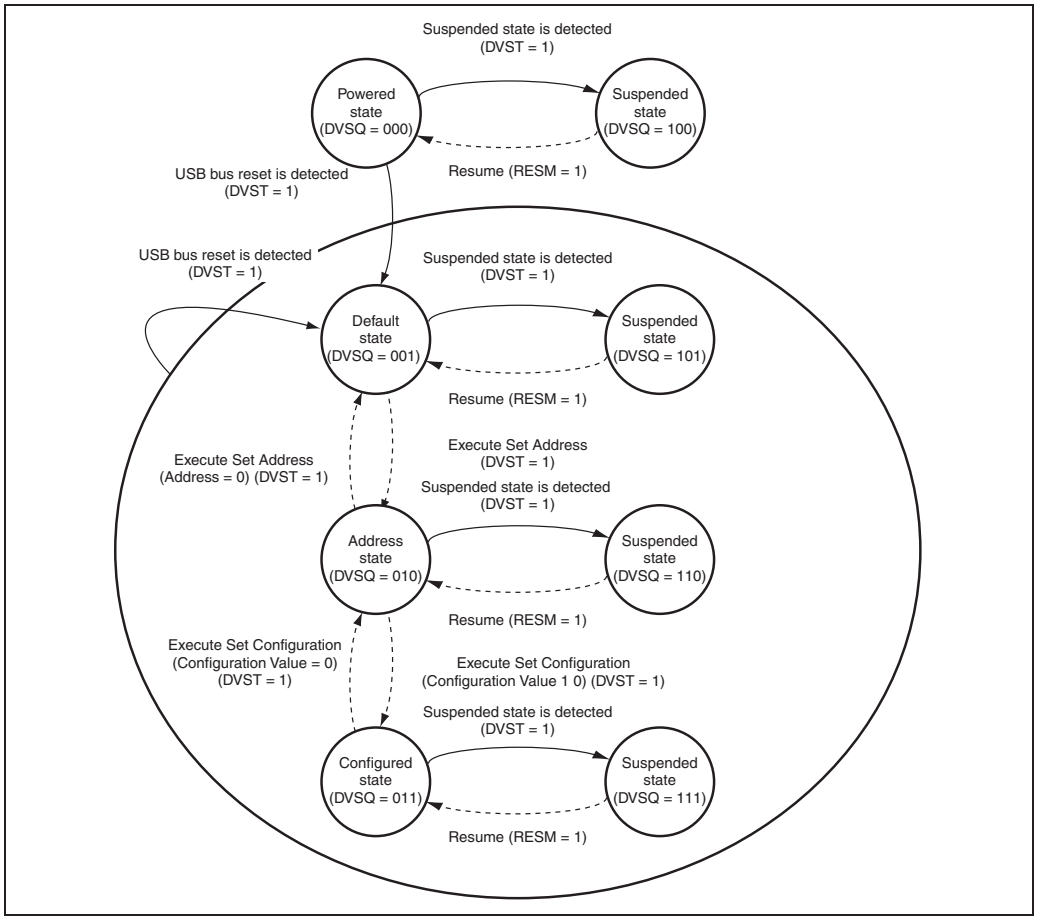


Figure 32.6 Device State Transitions

(5) Control Transfer Stage Transition Interrupt

Figure 32.7 shows control transfer stage transitions of this module. This module manages the sequence of control transfers and generates control transfer stage transition interrupts. Enabling or disabling each control transfer stage transition interrupt can be set by INTENB0. The current transfer stage after transition can be checked by the CTSQ bits in INTSTS0.

Control transfer stage transition interrupts are generated only when the function controller function is selected.

The following describes control transfer sequence errors. When an error occurs, the PID bits in DCPCTR indicate B'1x (STALL response).

1. Control read transfer
   - This module receives an OUT or PING token in response to the IN token in the data stage before starting data transfer.
   - This module receives an IN token in the status stage.
   - This module receives a packet with a data packet of DATAPID = DATA0 in the status stage.
2. Control write transfer
   - This module receives an IN token in response to the OUT token in the data stage before sending an ACK response.
   - This module receives a packet with the first data packet of DATAPID = DATA0.
   - This module receives an OUT or PING token in the status stage.
3. Control write no-data control transfer
   - This module receives an OUT or PING token in the status stage.

If the size of the receive data exceeds the wLength value of the USB request in the control write transfer data stage, this is not treated as a control transfer sequence error. This module sends ACK for normal end in response to a packet other than Zero-Length packet in the control read transfer status stage.

When a CTRT interrupt is generated (SERR = 1) due to a sequence error, CTSQ = 110 is retained until the interrupt status is cleared (CTRT = 0) by the system. For this reason, while CTSQ = 110, even if a new USB request is received, a CTRT interrupt at the end of the setup stage is not generated. (This module retains the setup stage end status and generates a setup stage end interrupt after the interrupt status is cleared by the software.)

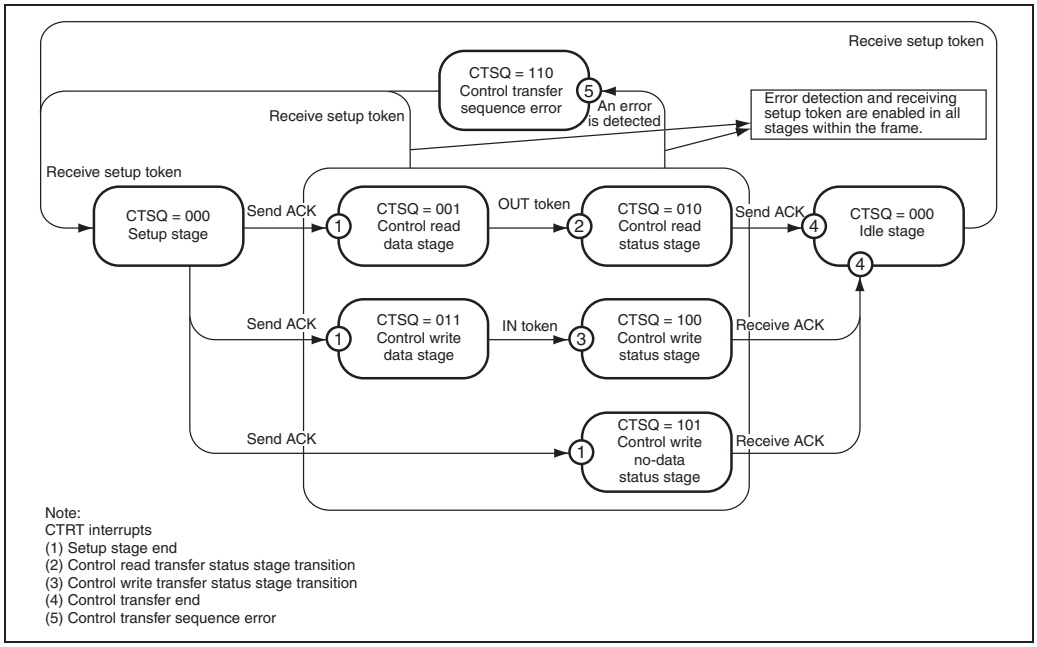


Figure 32.7 Control Transfer Stage Transitions

(6) Frame Update Interrupt

Figure 32.8 shows an example of the SOFR interrupt output timing of this module.

When the host controller function is selected, an SOFR interrupt is generated at the frame number update timing. When the function controller function is selected, an SOFR interrupt is generated immediately after the frame number is updated.

When this module detects a new SOF packet during the full-speed operation with the function controller function selected, this module updates the frame number and generates an SOFR interrupt. In the high-speed operation, however, the frame number is not updated or no SOFR interrupt is generated unless the module enters the μ SOF lock state. Furthermore, the SOF interpolation function is not activated. The μ SOF lock state occurs when this module receives a μ SOF packet twice in a row with different frame numbers without an error.

The μ SOF lock monitoring start and stop conditions are as follows:

1. µ SOF lock monitoring start conditions
   USBE = 1
2. µ SOF lock monitoring stop conditions
   USBE = 0, receiving USB bus reset, or detection of suspended state

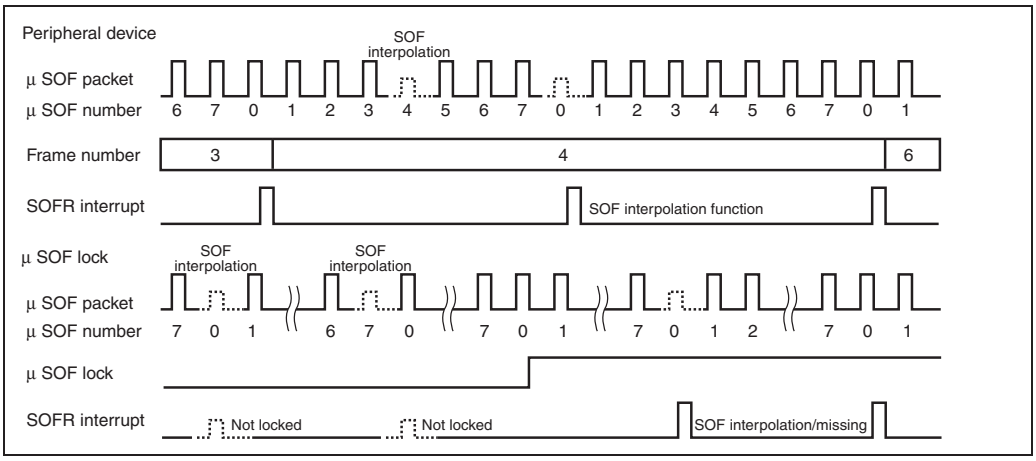


Figure 32.8 Example of SOFR Interrupt Output Timing

(7) VBUS Interrupt

When the VBUS pin state changes, a VBUS interrupt is generated. The VBUS pin level can be checked by the VBSTS bit in INTSTS0. The VBUS interrupt is used to check connection or disconnection to/from the host controller. However, when the system starts up with the host controller connected, the VBUS pin state remains unchanged, and therefore the first VBUS interrupt is not generated.

(8) Resume Interrupt

When the function controller function is selected and the USB bus state changes (J-State to K-State or J-State to SE0) with the device state suspended, a resume interrupt is generated. The resume interrupt is used to detect the return from the suspended state.

When the host controller function is selected, no resume interrupt is generated. Use the BCHG interrupt to detect a change in the USB bus state.

(9) BCHG Interrupt

When the USB bus state changes, a BCHG interrupt is generated. This interrupt is used to detect connection to a peripheral device and to detect remote wakeup when the host controller function is selected. This interrupt occurs when either of the host controller function or function controller function is selected.

(10) DTCH Interrupt

When a disconnection of the USB bus is detected with the host controller function selected, a DTCH interrupt is generated. This module detects a bus disconnection conforming to the USB Specification 2.0.

After detecting a DTCH interrupt, this module performs the following hardware control irrespective of the setting of the corresponding interrupt enable bit. The software must terminate the communication of all pipes with the port and drive this module into the state of waiting for connection to the port (ATTCH interrupt is generated).

- Change the UACT bit of the port that detected the DTCH interrupt to 0 and indicate UACT.
- Drive the port where the DTCH interrupt occurred into the idle state.

(11) SACK Interrupt

When this module receives ACK from the peripheral device in response to the transmitted setup packet with the host controller function selected, a SACK interrupt is generated. This interrupt indicates that a setup transaction is successfully completed.

(12) SIGN Interrupt

When this module cannot receive ACK successfully from the peripheral device in response to the transmitted setup packet three times in a row with the host controller function selected, a SIGN interrupt is generated. This interrupt is used to detect no ACK response from the peripheral device or ACK packet damage.

(13) ATTCH Interrupt

When J-State or K-State of the full-speed/low-speed signal level is detected for 2.5 μs in the USB port with the host controller function selected, an ATTCH interrupt is generated. This interrupt is detected in either of the following cases.

- When the signal level changed from K-State, SE0 or SE1 to J-State, and remains in J-State for 2.5 μs
- When the signal level changed from J-State, SE0 or SE1 to K-State, and remains in K-State for 2.5 μs

(14) EOFERR Interrupt

When this module detects that communication is not completed at the EOF2 timing specified in the USB Specification 2.0, an EOFERR interrupt is generated.

After detecting an EOFERR interrupt, this module performs the following hardware control irrespective of the setting of the corresponding interrupt enable bit. The software must terminate the communication of all pipes with the port and perform reenumeration for the port.

- Change the UACT bit of the port that detected the EOFERR interrupt to 0 and indicate UACT.
- Drive the port where the EOFERR interrupt occurred into the idle state.

32.4.3 Pipe Control

Table 32.16 lists the pipe settings of this module. In the USB data transfer, data must be transmitted or received using virtual pipes called “endpoint.” This module is provided with ten pipes for data transfer. Set each pipe according to system specifications.

Table 32.16 Pipe Settings

Register Name	Bit Name	Setting	Remarks
DCPCFG	TYPE	Transfer type	Pipes 1 to 9: Setting allowed
PIPECFG	BFRE	BRDY interrupt mode	Pipes 1 to 5: Setting allowed
	DBLB	Double buffer	Pipes 1 to 5: Setting allowed
	CNTMD	Continuous transfer or discontinuous transfer	Pipes 1, 2: Setting allowed only when bulk transfer is selected Pipes 3 to 5: Setting allowed
	DIR	Transfer direction	IN or OUT selectable
	EPNUM	Endpoint number	Pipes 1 to 9: Setting allowed Set a value other than 0000 when using pipes
	SHTNAK	Disabling pipes at the end of transfer	Pipes 1, 2: Setting allowed only when bulk transfer is selected Pipes 3 to 5: Setting allowed
PIPEBUF	BUFSIZE	Buffer memory size	DCP: Setting disallowed (256 bytes fixed) Pipes 1 to 5: Setting allowed (up to 2 Kbytes) Pipes 6 to 9: Setting disallowed (64 bytes fixed)
	BUFNMB	Buffer memory number	DCP: Setting disallowed (H'0 to H'3 fixed) Pipes 1 to 5: Setting allowed (H'8 to H'7F) Pipes 6 to 9: Setting disallowed (H'4 to H'7 fixed)
DCPMAXP PIPEMAXP	DEVSEL	Device select	Checked only when the host controller functions selected.
	MXPS	Maximum packet size	Setting conforming to the USB Specification

Register Name	Bit Name	Setting	Remarks
PIPEPERI	IFIS	Buffer flush	Pipes 1, 2: Setting allowed only when isochronous transfer is selected Pipes 3 to 5: Setting disallowed Pipes 6 to 9: Setting allowed only when the host control function is selected
	IITV	Interval counter	Pipes 1, 2: Setting allowed only when isochronous transfer is selected Pipes 3 to 5: Setting disallowed Pipes 6 to 9: Setting allowed only when the host control function is selected
DCPCTR PIPEnCTR	BSTS	Buffer status	For DCP, receive buffer status and transmit buffer status are switched by the ISEL bit.
	INBUFM	IN buffer monitor	Provided only for pipes 3 to 5.
	SUREQ	SETUP request	Setting allowed for DCP only Controlled only when the host controller function is selected.
	SUREQCLR	SUREQ clear	Setting allowed for DCP only Controlled only when the host controller function is selected.
	CSCLR	CSSTS clear	Controlled only when the host controller function is selected.
	CSSTS	SPLIT status	Monitored only when the host controller function is selected.
	ATREPM	Auto-response mode	Pipes 1 to 5: Setting allowed only when the function controller function is selected.
	ACLRM	Buffer auto-clear	Pipes 1 to 9: Setting allowed
	SQCLR	Sequence clear	Data toggle bit clear
	SQSET	Sequence setting	Data toggle bit setting
	SQMON	Sequence check	Data toggle bit check
	PBUSY	Pipe busy check	
	PID	Response PID	See section 32.4.3 (6), Response PID.

Register Name	Bit Name	Setting	Remarks
PIPEnTRE	TRENB	Transaction count enable	Pipes 1 to 5: Setting allowed
	TRCLR	Current transaction counter clear	Pipes 1 to 5: Setting allowed
PIPEnTRN	TRNCNT	Transaction counter	Pipes 1 to 5: Setting allowed

(1) Pipe Control Registers Switching Procedure

The following bits in the pipe control registers can be modified only when USB communication is set to disabled (PID = NAK).

Bits/registers that cannot be modified when USB communication is set to enabled (PID = BUF)

- Each bit in DCPCFG and DCPMAXP
- SQCLR and SQSET bits in DCPCTR
- Each bit in PIPECFG, PIPEBUF, PIPEMAXP, and PIPEPERI
- ATREPM, ACLRM, SQCLR, and SQSET bits in PIPExCTR
- Each bit in PIPExTRE and PIPExTRN

When changing these bits from the state where USB communication is enabled (PID = BUF), follow the steps below.

1. Generate a pipe control register bit change request.
2. Change the PID bits for the pipe to NAK.
3. Wait until the CSSTS bit for the pipe is cleared to 0 (only when the host controller function is selected).
4. Wait until the PBUSY bit for the pipe is cleared to 0.
5. Change the bits in the pipe control registers.

The following bits in the pipe control registers can be modified only for pipe information that is not set in any of the CURPIPE bits in CFIFOSEL, D0FIFOSEL, and D1FIFOSEL.

Bits/registers that cannot be modified while the CURPIPE bits in FIFO-PORT are being set

- Each bit in DCPCFG and DCPMAXP
- Each bit in PIPECFG, PIPEBUF, PIPEMAXP, and PIPEPERI

Before changing the pipe information, set the CURPIPE bits to a pipe other than that to be changed. For the DCP, clear the buffer by the BCLR bit after modifying the pipe information.

(2) Transfer Type

Specify the transfer type of each pipe by the TYPE bits in PIPEPCFG as follows:

- DCP: Setting is not required (fixed to control transfer).
- Pipes 1, 2: Set bulk transfer or isochronous transfer.
- Pipes 3 to 5: Set bulk transfer.
- Pipes 6 to 9: Set interrupt transfer.

(3) Endpoint Number

Specify the endpoint number of each pipe by the EPNUM bits in PIPEPCFG. The endpoint number of the DCP is always 0. For other pipes, endpoint 1 to endpoint 15 are selectable.

- DCP: Setting is not required (fixed to endpoint 0).
- Pipes 1 to 9: Set an endpoint number by selecting a number 1 to 15.
  However, set an endpoint number so that combinations of the DIR bit and the EPNUM bits do not overlap.

(4) Maximum Packet Size

Specify the maximum packet size of each pipe by the MXPS bits in DCPMAXP and PIPEMAXP. For the DCP and pipes 1 to 5, any of the maximum packet sizes defined in the USB Specification can be set. For pipes 6 to 9, a maximum packet size up to 64 bytes can be set. Specify a maximum packet size as follows before starting transfer (PID = BUF):

- DCP: Set 64 for high-speed operation.
- DCP: Set 8, 16, 32, or 64 for full-speed operation.
- Pipes 1 to 5: Set 512 for high-speed bulk transfer.
- Pipes 1 to 5: Set 8, 16, 32, or 64 for full-speed bulk transfer.
- Pipes 1, 2: Set a value from 1 to 1024 for high-speed isochronous transfer.
- Pipes 1, 2: Set a value from 1 to 1023 for full-speed isochronous transfer.
- Pipes 6 to 9: Set a value from 1 to 64.

High Bandwidth in interrupt and isochronous transfers is not supported.

(5) Transaction Counter (Pipes 1 to 5: Read Direction)

When the specified number of transactions with data packet in the receive direction are completed, this module recognizes this as a transfer end. The transaction counter works when the pipe selected for the D0FIFO and D1FIFO ports is set for the data read (from the buffer memory) direction. The transaction counter is provided with the TRNCNT register to specify the number of transactions and the current counter to count transactions internally. When the current counter reaches the specified value, the buffer memory becomes ready for reading. The current counter of the transaction counter function can be initialized by the TRCLR bit to count transactions again from the beginning. The TRNCNT read data varies depending on the TRENB setting.

- TRENB = 0: The set transaction counter value is read.
- TRENB = 1: The internally counted current counter value is read.
- Change the CURPIPE bits according to the following.
- Do not change the CURPIPE bits until the transaction for the specified pipe finishes.
- Change the CURPIPE bits when the current counter is cleared.
- Control the TRCLR bit according to the following.
- Do not clear the current counter during transaction count and PID = BUF.
- Do not clear the current counter while data is remaining in the buffer.

(6) Response PID

Specify the response PID for each pipe by the PID bits in DCPCTR and PIPEnCTR.

This module operates as follows according to the response PID setting.

1. Setting the response PID when the host controller function is selected
   The response PID specifies the execution of transactions.
   — NAK setting: Pipes are disabled and no transaction is executed.
   — BUF setting: Transactions are executed according to the buffer memory status.
   When the buffer memory contains transmit data in the OUT direction, this module sends an OUT token.
   When the buffer memory has available space and is ready to receive data in the IN direction, this module sends an IN token.
   — STALL setting: Pipes are disabled and no transaction is executed.

Note: The DCP setup transaction is set by the SUREQ bit.

2. Setting the response PID when the function controller function is selected
   The response PID specifies a response to transactions from the host.
   — NAK setting: NAK is always sent in response to a transaction.
   — BUF setting: A response is sent to a transaction according to the buffer memory status.
   — STALL setting: STALL is always sent in response to a transaction.

Note: This module always sends ACK in response to a setup transaction irrespective of the PID setting, and stores a USB request in the register.

This module modifies the PID bits in the following cases depending on transaction results.

3. When the response PID is set by the hardware with the host controller function selected
   — NAK setting: This module sets PID = NAK and automatically stops sending tokens.

- When an NRDY interrupt is generated in a transfer other than isochronous transfer
- (For details, see 32.4.2(2) NRDY Interrupt.)
- When this module receives a short packet with the SHTNAK bit in PIPECFG set to 1 in the bulk transfer
- When the SHTNAK bit is set to 1 in the bulk transfer and the transaction counter stops counting
  — BUF setting: This module does not set the PID bits to BUF.
  — STALL setting: This module sets PID = STALL in the following cases and automatically stops sending tokens.
- When this module receives STALL in response to the transmitted token
- When the size of the received data packet is larger than the maximum packet size

4. When the response PID is set by the hardware with the function controller function selected
   — NAK setting: This module sets PID to NAK in the following cases and always sends NAK in response to a transaction.

- When a SETUP token is successfully received (DCP only)
- When the SHTNAK bit in PIPECFG is set to 1 in a bulk transfer and the transaction counter stops counting or this module receives a short packet
  — BUF setting: This module does not set the PID bits to BUF.
  — STALL setting: This module sets PID to STALL in the following cases and always sends STALL in response to a transaction.
- When a maximum packet size exceeded error is detected in a receive data packet
- When a control transfer sequence error is detected (DCP only)

(7) Data PID Sequence Bit

When data is successfully transferred in the control transfer data stage, bulk transfer, or interrupt transfer, this module automatically toggles the data PID sequence bit. The sequence bit of the data PID transmitted next can be monitored by the SQMON bit in DCPCTR and PIPEnCTR. In a data transmission period, the sequence bit switches at the ACK handshake receive timing. In a data reception period, the sequence bit switches at the ACK handshake transmit timing. The data PID sequence bit can also be changed by the SQCLR and SQSET bits in DCPCTR and PIPEnCTR.

In control transfers when the function controller function is selected, this module automatically sets the sequence bit during a stage transition. DATA0 is indicated at the end of the setup stage, and DATA1 is used for responses in the status stage. This does not require the setting of the sequence bit by the software. In control transfers when the host controller function is selected, the software must set the sequence bit during a stage transition.

Note that, when the host controller function or function controller function is selected, the software must also set the data PID sequence bit when sending or receiving a ClearFeature request.

The sequence bit cannot be modified by the SQSET bit for isochronous transfer pipes.

(8) Response PID = NAK Function

This module has a function to disable the pipe operation (Response PID = NAK) at the last data packet receive timing in a transfer (this module automatically identifies the last data packet receive timing at the short packet receive timing or using the transaction counter) by setting the SHTNAK bit in PIPECFG to 1.

This function allows reception of data packets in transfer units when the buffer memory is used as a double buffer. Furthermore, when the pipe operation is disabled, the software must set the response PID to BUF to enable the pipe operation.

This function is available only for bulk transfers.

(9) Auto-Response Mode

When the ATREPM bit in PIPEnCTR is set to 1 in a bulk transfer pipe (pipes 1 to 5), this module enters auto-response mode: OUT-NAK mode in OUT transfers (DIR = 0) or null auto-response mode in IN transfers (DIR = 1).

1. OUT-NAK mode

   When the ATREPM bit is set to 1 in a bulk OUT transfer pipe, this module sends NAK in response to an OUT token or PING token and outputs an NRDY interrupt. To change response mode from normal mode to OUT-NAK mode, specify OUT-NAK mode with the pipe operation disabled (Response PID = NAK), and then enable the pipe operation (Response PID = BUF). After that, OUT-NAK mode is enabled. However, if an OUT token is received immediately before the pipe operation is disabled, this module receives the data of the token correctly and sends ACK to the host.

   To change response mode from OUT-NAK mode to normal mode, reset OUT-NAK mode with the pipe operation disabled (Response PID = NAK), and then enable the pipe operation (Response PID = BUF). In normal mode, this module can receive OUT data and sends ACK in response to a PING token when the buffer is ready for receiving.

2. Null auto-response mode

   When the ATREPM bit is set to 1 in a bulk IN transfer pipe, this module continues to send Zero-Length packets. To change response mode from normal mode to null auto-response mode, specify null auto-response mode with the pipe operation disabled (Response PID = NAK), and then enable the pipe operation (Response PID = BUF). After that, null auto-response mode is enabled. However, specify null auto-response mode while the buffer is empty. Verify this by checking INBUFM = 0. Since INBUFM = 1 indicates that the buffer contains data, clear the buffer by setting the ACLRM bit. Do not write data to the buffer from the FIFO port during setting to null auto-response mode.

To change response mode from null auto-response mode to normal mode, delay the pipe operation disabled state (Response PID = NAK) for a time period for sending a Zero-Length packet (full-speed: 10 μs, high-speed: 3 μs), and then reset null auto-response mode. Normal mode allows writing from the FIFO port, and also allows sending packets to the host by enabling the pipe operation (Response PID = BUF).

32.4.4 FIFO Buffer Memory

(1) Allocating FIFO Buffer Memory

Figure 32.9 shows an example of the FIFO buffer memory map of this module. The FIFO buffer memory is an area shared by the CPU and this module. There are two FIFO buffer memory states where the access right is given to the system (CPU) or to this module (SIE).

The FIFO buffer memory provides independent areas for each pipe. A memory area is set with the block start number and the number of blocks (BUFNMB and BUFSIZE bits in PIPEBUF) in 64-byte units as one block.

When continuous transfer mode is selected by the CNTMD bit in PIPEnCFG, be sure to set the BUFSIZE bits to a value in integral multiples of the maximum packet size. When double buffer is selected by the DBLB bit in PIPEnCFG, two sides of the memory area specified by the BUFSIZE bits in PIPEBUF are provided for the same pipe.

Furthermore, three FIFO ports are used for accesses (data read/write) to the buffer memory. The number of a pipe to be allocated to the FIFO ports is specified by the CURPIPE bits in CFIFOSEL and DnFIFOSEL.

The buffer status of each pipe can be monitored by the BSTS and INBUFM bits in DCPCTR and PIPEnCTR. The access right to the FIFO ports can be checked by the FRDY bit in CFIFOCTR and DnFIFOCTR.

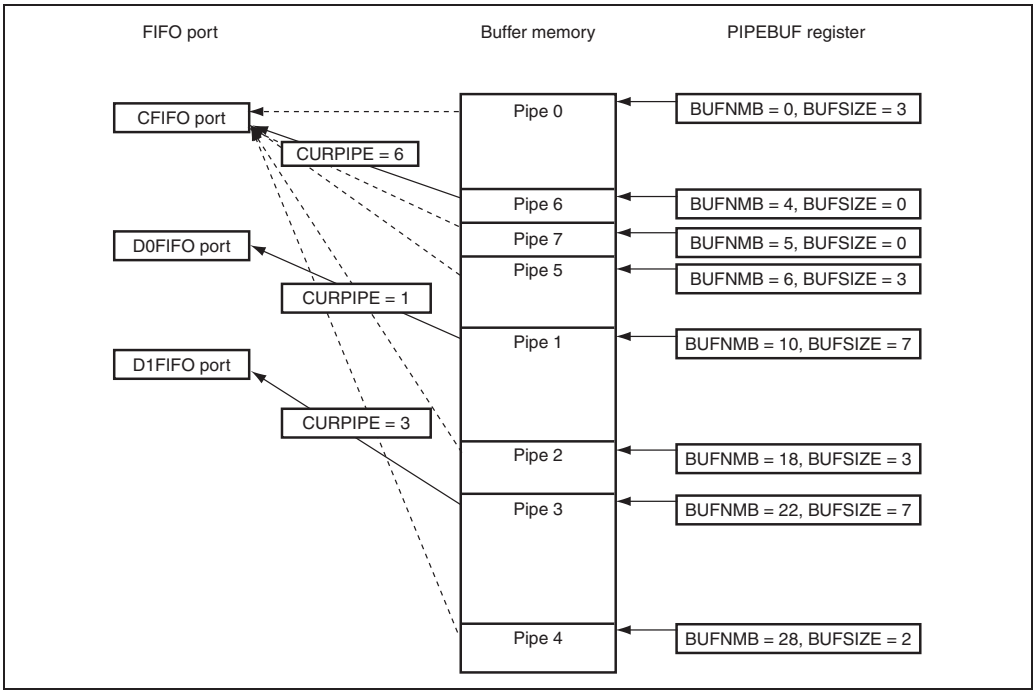


Figure 32.9 Example of Buffer Memory Map

- Buffer status

  Tables 32.17 and 32.18 show the buffer memory status of this module. The buffer memory status can be monitored by the BSTS bit in DCPCTR and the INBUFM bit in PIPEnCTR. The buffer memory access direction is specified by the DIR bit in PIPEnCFG or the ISEL bit in CFIFOSEL (when DCP is selected).

  The INBUFM bit is valid only for pipes 1 to 5 in the transmit direction.

  When a transfer pipe in the transmit direction is set to double buffer, the BSTS bit is used to monitor the buffer status on the CPU side, and the INBUFM bit is used to monitor the buffer status on the SIE side. When data write to the FIFO port by the CPU (DMAC) takes time and buffer empty cannot be checked by the BEMP interrupt, the INBUFM bit is available to check completion of transmission.

Table 32.17 Buffer Memory Status That Varies Depending on the BSTS Bit

ISEL or DIR	BSTS	Buffer Memory Status
0 (receive direction)	0	No receive data in the buffer memory or data is being received. Data cannot be read from the FIFO port.
0 (receive direction)	1	Receive data in the buffer memory or a Zero-Length packet is received. Data can be read from the FIFO port. However, the buffer must be cleared because the FIFO port cannot be read when this module receives a Zero-Length packet.
1 (transmit direction)	0	Transmission of data is not completed. Data cannot be written to the FIFO port.
1 (transmit direction)	1	Transmission of data is completed. The CPU can write data to the buffer memory.

Table 32.18 Buffer Memory Status That Varies Depending on the INBUFM Bit

DIR	INBUFM	Buffer Memory Status
0 (receive direction)	Invalid	Invalid
1 (transmit direction)	0	Transmittable data is completely sent. No transmittable data is in the buffer memory.
1 (transmit direction)	1	Transmittable data is written from the FIFO port. The buffer memory contains transmittable data.

- FIFO buffer clear

  Table 32.19 shows clearing of the FIFO buffer memory of this module. The buffer memory can be cleared by the BCLR, DCLRM, and ACLRM bits.

Table 32.19 Buffer Clear

Bit Name	BCLR	DCLRM	ACLRM
Register	CFIFOCTR DnFIFOCTR	DnFIFOSEL	PIPEnCTR
Function	Clears the buffer memory of the CPU.	Automatically clears the buffer memory after reading data of the specified pipe.	Automatically clears the buffer memory by ignoring all received packets.
Clearing method	Writing 1 to this bit clears the buffer memory.	1: This mode is enabled. 0: This mode is disabled.	1: This mode is enabled. 0: This mode is disabled.

- Buffer area

  Table 32.20 shows a buffer memory map of this module. The buffer memory includes a dedicated areas reserved beforehand for pipes and user areas provided for user settings.

  The buffer for DCP is a dedicated area commonly used in control read transfers and control write transfers.

  Areas for pipes 6 to 9 are allocated respectively in advance. However, when none of pipes 6 to 9 is used, the areas are available for pipes 1 to 5 as user areas.

  Allocate different areas of the buffer memory to each pipe. Note that, when double buffer is specified, the size of an area is twice of the set value.

  Do not set the buffer size to a value smaller than the maximum packet size.

Table 32.20 Buffer Memory Map

Buffer Memory Number	Buffer Size	Pipe Setting	Remarks
H'0	64 bytes	Fixed only for DCP	Single buffer
H'1 to H'3	—	Unavailable	—
H'4	64 bytes	Fixed only for pipe 6	Single buffer
H'5	64 bytes	Fixed only for pipe 7	Single buffer
H'6	64 bytes	Fixed only for pipe 8	Single buffer
H'7	64 bytes	Fixed only for pipe 9	Single buffer
H'8 to H'7F	Max. 7616 bytes	User area for pipes 1 to 5	Double buffer and continuous transfer can be set

- Buffer auto-clear mode function

  When the ACLRM bit PIPEnCTR is set to 1, this module discards all data packets received. However, when this module receives a data packet successfully, it sends ACK to the host controller. This function is available only for the buffer memory read direction.

  Writing 1 and then 0 continuously to the ACLRM bit clears the buffer memory of the selected pipe irrespective of the access direction.

  Take at least 100 ns between writing 1 and writing 0 for the sequence execution time of the hardware.

- Buffer memory specifications (single buffer/double buffer setting)

  Single buffer or double buffer is selectable for pipes 1 to 5 with the DBLB bit in PIPEnCFG. Double buffer is a function to provide two sides of the memory area specified by the BUFSIZE bits in PIPEBUF for the same pipe. Figure 32.10 shows an example of setting for the buffer memory of this module.

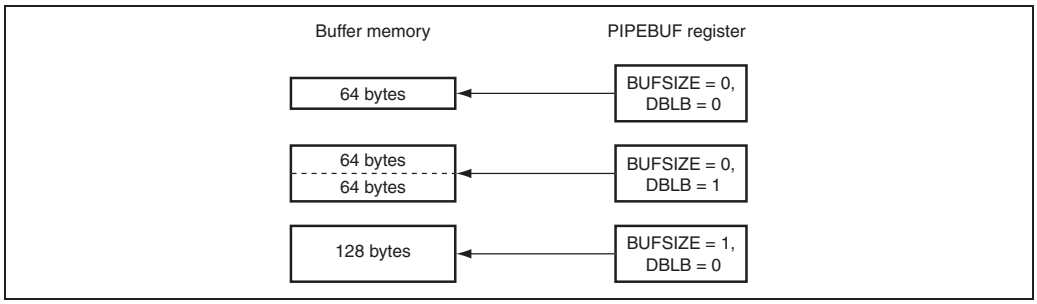


Figure 32.10 Example of Buffer Memory Setting

- Buffer memory operation (continuous transfer setting)

  Continuous transfer mode or discontinuous transfer mode is selectable with the CNTMD bit in PIPEnCFG. This selection is enabled for pipes 1 to 5.

  The continuous transfer mode function allows continuous transmission/reception of multiple transactions. When continuous transfer mode is selected, data up to the buffer size allocated to each pipe can be transferred without outputting an interrupt to the CPU.

  In continuous transmission mode, data in the buffer is divided by the maximum packet size and is then transmitted. To send data less than the buffer size (a short packet or a packet with a size of integral multiples of the maximum packet size and less than the buffer size), set BVAL = 1 after writing transmit data to the buffer.

  In continuous reception mode, no interrupt is generated until this module receives packets to the buffer size, the transaction count ends, or this module receives a short packet.

Table 32.21 shows the relationship between the CNTMD setting and determination of transmission/reception end of the FIFO buffer.

Table 32.21 Relationship between CNTMD Setting and Determination of Transmission/Reception End of FIFO Buffer

Transfer Mode	Determination of Buffer Readable State and Data Transmittable State
Discontinuous transfer (CNTMD = 0)	Conditions for FIFO buffer readable state when data receive direction is selected (DIR = 0):
	When this module receives one packet
	Conditions for FIFO buffer data transmittable state when data transmit direction is selected (DIR = 1):
	Any of the following cases:
	The software (or DMAC) writes data of the maximum packet size to the FIFO buffer.
	The software (or DMAC) writes data of a short packet (including 0 bytes) to the FIFO buffer, and then sets BVAL = 1.
Continuous transfer (CNTMD = 1)	Conditions for FIFO buffer readable state when data receive direction is selected (DIR = 0):
	When the bytes of data received in the FIFO buffer for the selected pipe equals the allocated bytes ((BUFSIZE + 1) * 64)
	When this module receives a short packet other than a Zero-Length packet
	When this module receives a Zero-Length packet when data is already stored in the FIFO buffer for the selected pipe
	When this module receives packets as large as the transaction counter value specified for the selected pipe by the software
	Conditions for FIFO buffer data transmittable state when data transmit direction is selected (DIR = 1):
	Any of the following cases:
	The volume of data written by the software (or DMAC) equals the size of one side of the FIFO buffer for the selected pipe.
	The software (or DMAC) writes data less than the size of one side of the FIFO buffer for the selected pipe to the FIFO buffer, and then sets BVAL = 1.

Figure 32.11 shows an example of buffer memory operation of this module.

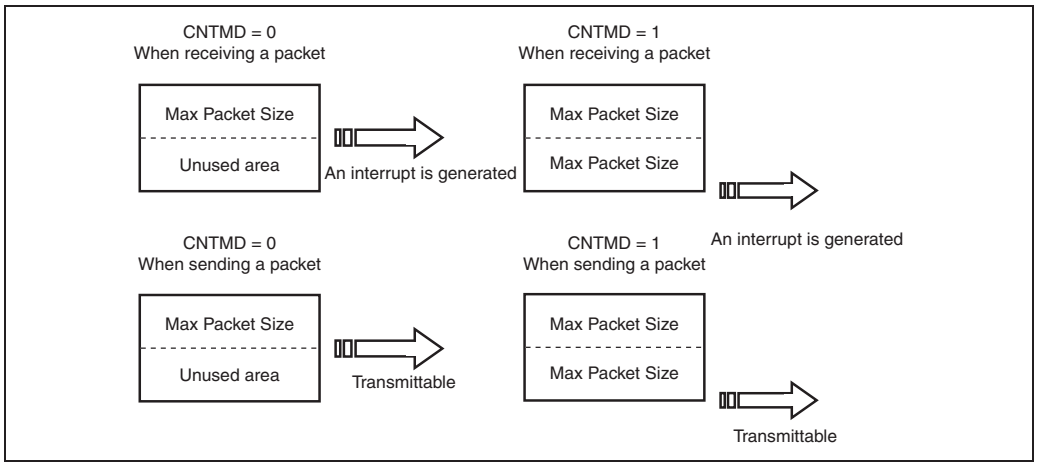


Figure 32.11 Example of Buffer Memory Operation

(2) FIFO Port Function

Table 32.22 lists the settings for the FIFO port functions of this module. During a data write access, when data up to buffer full (or up to the maximum packet size in discontinuous transfer) is written, the FIFO port automatically enters the data transmittable state. To make data less than buffer full (or the maximum packet size in discontinuous transfer) transmittable, set the BVAL bit in CFIFOCTR and DnFIFOCTR to 1 to set write end. For transmission of a Zero-Length packet, clear the buffer using the BCLR bit in these registers and then set the BVAL bit to 1.

During a data read access, when all data is read, the FIFO port automatically enters the new packet receivable state. However, when receiving a Zero-Length packet (DTLN = 0), no data can be read. Therefore, clear the buffer using the BCLR bit in these registers. The receive data length can be checked by the DTLN bits in CFIFOCTR and DnFIFOCTR.

Table 32.22 FIFO Port Function Settings

Register Name	Bit Name	Function	Remarks
CFIFOSEL	RCNT	Selects DTLN read mode.	
DnFIFOSEL	REW	Rewinds the buffer memory (reread/rewrite).	
	DCLRM	Reads and clears receive data of the specified pipe.	DnFIFO only
	DREQE	Enables DMA transfer.	DnFIFO only
	MBW	Specify FIFO port access bit width.	
	BIGEND	Selects FIFO port endian.	
	ISEL	Selects FIFO port access direction.	DCP only
	CURPIPE	Select the current pipe.	
CFIFOCTR	BVAL	Specifies buffer memory write end.	
DnFIFOCTR	BCLR	Clears the buffer memory of the CPU.	
	DTLN	Check receive data length.	

(a) FIFO Port Selection

Table 32.23 shows pipes that can be selected in each FIFO port. Select a pipe to be accessed by the CURPIPE bits in CFIFOSEL and DnFIFOSEL. After selecting a pipe, confirm that the set CURPIPE value is read correctly, check FRDY = 1, and then make an access to the FIFO port. (If the previous pipe number is read, this controller is changing a pipe.)

Also select the bus width to be accessed by the MBW bits. The buffer memory access direction is specified by the DIR bit in PIPEnCFG. However, only the access direction of DCP is determined by the ISEL bit.

Table 32.23 FIFO Port Access

Pipe	Access	Available port
DCP	CPU access	CFIFO port register
Pipes 1 to 9	CPU access	CFIFO port register
	DMA access	D0FIFO port, D1FIFO port

(b) REW Bit

The current access to a pipe can be suspended temporarily, and it is also possible to make an access to another pipe to continue the ongoing pipe processing. This processing is allowed by using the REW bit in CFIFOSEL and DnFIFOSEL.

When the REW bit is set to 1 together with the CURPIPE bits in CFIFOSEL and DnFIFOSEL and a pipe is selected, the reading or writing pointer of the buffer memory is reset, which allows reading or writing data from the first byte. Furthermore, when a pipe is selected with the REW bit set to 0, data can be read or written following the data at the previous selection without resetting the reading or writing pointer of the buffer memory.

To make accesses to the FIFO port, select a pipe and check FRDY = 1.

(3) DMA Transfer (Dedicated DMA Interface)

(a) Overview of DMA Transfer

The FIFO port can be accessed by the DMAC for pipes 1 to 9. When the buffer of a pipe specified for DMA transfer becomes accessible, this module outputs a DMA transfer request.

Specify the data transfer unit to the FIFO port by the MBW bits in DnFIFOSEL, and select a pipe used for DMA transfer by the CURPIPE bits in DnFIFOSEL. Do not change the selected pipe during a DMA transfer.

(b) DMA Transfer End Auto-Recognition

This module can terminate writing of data by DMA transfer to the FIFO buffer by controlling the DMA transfer end signal input. After sampling the transfer end signal, this module drives the buffer memory into the transmittable state (same state as BVAL = 1).

(c) DnFIFO Auto-Clear Mode (D0FIFO/D1FIFO Port Read Direction)

By setting the DCLRM bit in DnFIFOSEL to 1, this module automatically clears the buffer memory for the selected pipe upon completion of data read from the buffer memory.

Table 32.24 shows the relationship between packet reception and buffer memory clear by the software. As shown in the table, buffer clearing conditions vary with the BFRE setting. However, in any state that needs clearing, using the DCLRM bit makes buffer clearing by the software unnecessary. Thus DMA transfer is enabled without requiring any software control.

- This function is available only for the buffer memory read direction.

Table 32.24 Relationship between Packet Reception and Buffer Memory Clear by the Software

Register Setting / Buffer Status When Receiving a Packet	DCLRM = 0		DCLRM = 1	
	BFRE = 0	BFRE = 1	BFRE = 0	BFRE = 1
Buffer full	Clearing not required	Clearing not required	Clearing not required	Clearing not required
Zero-Length packet reception	Clearing required	Clearing required	Clearing not required	Clearing not required
Normal short packet reception	Clearing not required	Clearing required	Clearing not required	Clearing not required
Transaction count end	Clearing not required	Clearing required	Clearing not required	Clearing not required

32.4.5 Control Transfer (DCP)

The default control pipe (DCP) is used for data transfer in the control transfer data stage. The buffer memory for the DCP is a 256-byte single buffer of a fixed area used for both control read and control write. The buffer memory can be accessed only by the CFIFO ports.

(1) Control Transfer when the Host Controller Function is Selected

(a) Setup Stage

USBREQ, USBVAL, USBINDX, and USBLENG are registers used to send USB requests in setup transactions. The specified data is sent as a setup transaction by writing the setup packet data in the register and writing 1 to the SUREQ bit in DCPCTR. The SUREQ bit is cleared to 0 when a transaction ends. Do not access the USB request registers while SUREQ = 1. The device address for a setup transaction is specified by the DEVSEL bits in DCPMAXP.

An interrupt is generated upon receiving a response from the peripheral device in response to the transmitted transaction (SIGN and SACK bits in INTSTS1). The setup transaction result can be checked at the timing of this interrupt request.

For data packets in setup transactions, a DATA0 data packet (USB request) is always sent irrespective of the SQMON setting in DCPCTR.

(b) Data Stage

This module transfers data using the DCP buffer memory in the data stage.

Specify the direction of accesses to the DCP buffer memory by the ISEL bit in CFIFOSEL. Also specify the transfer direction by the DIR bit in DCPCFG.

Transmit the first data packet in the data stage with data PID as DATA1. Set data PID = DATA1 by the SQSET bit in DCPCFG, and set PID = BUF to execute transactions. The completion of data transfer is detected by a BRDY interrupt and a BEMP interrupt.

In a control write transfer, when the transmit data is integral multiples of the maximum packet size, send a Zero-Length packet at the last by the software.

(c) Status Stage

In the status stage, data transfer of Zero-Length packets is performed in the reverse direction of the data stage. The same DCP buffer memory as in the data stage is used for data transfer. Transactions are executed using the same procedure as the data stage.

Send data packets in the data stage with data PID as DATA1. Set data PID = DATA1 by the SQSET bit in DCPCFG.

Furthermore, check the receive data length of a Zero-Length packet by the DTLN bits in CFIFOCTR after a BRDY interrupt is generated, and then clear the buffer memory by the BCLR bit.

(2) Control Transfer when the Function Controller Function is Selected

(a) Setup Stage

1. This module always sends ACK in response to a normal setup packet to this module. The following describes the operation of this module in the setup stage.
   When this module receives a new setup packet, this module sets the following bits.
   — The VALID bit in INTSTS0 to 1
   — The PID bits in DCPCTR to NAK
   — The CCPL bit in DCPCTR to 0
2. When this module receives a data packet following a setup packet, this module stores the USB request parameters in USBREQ, USBVAL, USBINDX, and USBLENG.

Be sure to process responses to control transfers while VALID = 0. The PID bits cannot be set to BUF when VALID = 1, and therefore the data stage cannot be completed.

With the VALID bit function, this module can suspend the ongoing request processing if this module receives a new USB request during a control transfer, and send a response to the latest request.

This module also determines the direction bit (bit 8 of bmRequestType) of the received USB request and the request data length (wLength), identifies a control read transfer, control write transfer, and control write no-data transfer, and controls stage transitions. For an incorrect sequence, a sequence error of the control transfer stage transition interrupt occurs, and the error is reported to the software. For the stage control of this module, see Figure 32.7.

(b) Data Stage

Transfer data in response to the received USB request using the DCP. Before making an access to the DCP buffer memory, specify the access direction by the ISEL bit in CFIFOSEL.

When the transfer data size is larger than the DCP buffer memory size, use a BRDY interrupt for control write transfers and a BEMP interrupt for control read transfers.

In the high-speed control write transfer, this module sends responses using the NYET handshake according to the buffer memory status.

(c) Status Stage

Setting the CCPL bit to 1 with the PID bits in DCPCTR set to BUF finishes a control transfer.

After these settings, this module executes the status stage as follows according to the data transfer direction determined in the setup stage:

- Control read transfer
  This module sends a Zero-Length packet and receives an ACK response from the USB host.
- Control write transfer, no-data control transfer
  This module receives a Zero-Length packet from the USB host and sends an ACK response.

(d) Control Transfer Auto-Response Function

This module automatically responds to a correct SET_ADDRESS request. If any of the following errors occurs in the SET_ADDRESS request, the software must respond to the error.

- Other than control read transfer: bmRequestType ≠ H'00
- Request errors: wIndex ≠ H'00
- Other than no-data control transfer: wLength ≠ H'00
- Request errors: wValue > H'7F

- Control transfer of device state errors: DVSQ = 011 (Configured)

All requests other than SET_ADDRESS require a response made by the software.

32.4.6 Bulk Transfer (Pipes 1 to 5)

The buffer memory usage (single buffer/double buffer setting or continuous/discontinuous transfer mode setting) can be selected for bulk transfers. The buffer memory size can be set to up to 2 Kbytes. This module manages the buffer memory status and automatically responds to a PING packet and an NYET handshake.

(1) PING Packet Control when the Host Controller Function is Selected

This module automatically sends a PING packet in the OUT direction.

As described below, this module sends an OUT packet upon receiving an ACK handshake with the initial state where a PING packet was transmitted. When this module receives NAK or NYET, it returns to the PING transmission state. This control is also effective for the control transfer data stage and status stage.

1. Set OUT data transmission.
2. Send a PING packet.
3. Receive an ACK handshake.
4. Send an OUT data packet.
5. Receive an ACK handshake.
   (Repeat steps 4 and 5.)
6. Send an OUT data packet.
7. Receive a NAK/NYET handshake.
8. Send a PING packet.

This module returns to the PING packet transmission state at the time of a power-on reset, receiving NYET/NAK handshake, setting the sequence toggle bit, setting clear (SQSET, SQCLR), and setting buffer clear (ACLRM).

(2) NYET Handshake Control when the Function Controller Function is Selected

Table 32.25 lists NYET handshake responses of this module. This module sends a NYET response under the following conditions. However, when this module receives a short packet, this module sends ACK instead of NYET. The same is true of the control write transfer data stage.

Table 32.25 NYET Handshake Responses

Setting of PID Bits in DCPCTR	Buffer Memory Status	Token	Response	Remarks
NAK/STALL	—	SETUP	ACK	—
	—	IN/OUT/PING	NAK/STALL	—
BUF	—	SETUP	ACK	—
	RCV-BRDY1	OUT/PING	ACK	Receives a data packet when receiving an OUT token.
	RCV-BRDY2	OUT	NYET	Receives a data packet. Sends a “reception disable” response.
	RCV-BRDY2	OUT (Short)	ACK	Receives a data packet. Sends a “reception enable” response.
	RCV-BRDY2	PING	ACK	Sends a “reception enable” response.
	RCV-NRDY	OUT/PING	NAK	Sends a “reception disable” response.
	TRN-BRDY	IN	DATA0/1	Sends a data packet.
	TRN-NRDY	IN	NAK	TRN-NRDY

[Legend]

RCV-BRDY1: The buffer memory has available space for two packets or more when receiving an OUT or PING token.

RCV-BRDY2: The buffer memory has available space for only one packet when receiving an OUT token.

RCV-NRDY: The buffer memory is occupied when receiving an PING token.

TRN-BRDY: The buffer memory contains transmit data when receiving an IN token.

TRN-NRDY: The buffer memory contains no transmit data when receiving an IN token.

32.4.7 Interrupt Transfer (Pipes 6 to 9)

When the function controller function is selected, this module performs interrupt transfer following the cycles controlled by the host controller. In interrupt transfers, this module ignores PING packets (no response), sends no NYET handshake, and sends ACK, NAK, and STALL responses.

When the host controller function is selected, the token output timing can be set using the interval counter. This module sends no PING token, but sends OUT tokens even in the OUT direction transfer.

This module does not support the High-Bandwidth interrupt transfer.

(1) Interval Counter in Interrupt Transfer when the Host Controller Function is Selected

To perform an interrupt transfer, set a transaction interval by the IITV bits in PIPEPERI. This controller sends tokens in the interrupt transfer at the specified intervals.

(a) Counter initialization

This controller initializes the interval counter under the following conditions.

- Power-on reset:
  The IITV bits are initialized.
- Buffer memory initialization by ACLRM
  The IITV bits are not initialized but the counter is initialized. The IITV value is counted from the beginning by clearing the ACLRM bit to 0.

Note that the interval counter is not initialized in the following cases.

- USB bus reset or USB suspended
  The IITV bits are not initialized. Setting the UACT bit to 1 causes the interval counter to start counting from the value before the USB bus reset or USB suspended state.

(b) Operation when this module cannot send/receive tokens at the token generation timing

This module generates no token in the following cases even at the token generation timing. In these cases, this module tries to execute the transaction in the next interval.

- When PID = NAK or STALL is set
- When the buffer memory is occupied at the token transmit timing in the IN direction (reception) transfer

- When the buffer memory contains no transmit data at the token transmit timing in the OUT direction (transmission) transfer

32.4.8 Isochronous Transfer (Pipes 1, 2)

This module is provided with the following functions for isochronous transfers.

- Reporting isochronous transfer error information
- Interval counter (IITV bits)
- Isochronous IN transfer data setup control (IDLY function)
- Isochronous IN transfer buffer flush function (IFIS bit)

This module does not support the isochronous High-Bandwidth transfer.

(1) Isochronous Transfer Error Detection

This module is provided with a function to detect the following error information so that the software can manage isochronous transfer errors. Tables 32.26 and 32.27 show the error detection priority of this module and interrupts generated as a result of error detection.

1. PID error
   — When the PID in a receive packet is invalid
2. CRC error, bit stuffing error
   — When a CRC error is found in a receive packet or bit stuffing is invalid
3. Maximum packet size exceeded error
   — When the data size of a receive packet is over the maximum packet size setting
4. Overrun/underrun error
   — When the host controller function is selected
   When the buffer memory is occupied at the token transmit timing in the IN direction (reception) transfer
   When the buffer memory contains no transmit data at the token transmit timing in the OUT direction (transmission) transfer
   — When the function controller function is selected
   When the buffer memory contains no data when this module receives an IN token in the IN direction (transmission) transfer
   When the buffer memory is occupied when this module receives an OUT token in the OUT direction (reception) transfer

5. Interval error

   When the function controller function is selected, this module generates an interval error in the following cases.

   — When no IN token can be received in interval frames in the isochronous IN transfer

   — When this module receives an OUT token other than interval frames in the isochronous OUT transfer

Table 32.26 Error Detection when Receiving Tokens

Priority for Error Detection	Error	Interrupt and Status
1	PID error	This module generates no interrupt (ignores as a damaged packet) when either of the host controller function or function controller function is selected.
2	CRC error, bit stuffing error	This module generates no interrupt (ignores as a damaged packet) when either of the host controller function or function controller function is selected.
3	Overrun error, underrun error	This module generates an NRDY interrupt and sets the OVRN bit when either of the host controller function or function controller function is selected. When the host controller function is selected, this module sends no token. When the function controller function is selected, this module sends a Zero-Length packet in response to the IN token. This module receives no data packet in response to the OUT token.
4	Interval error	When the function controller function is selected, this module generates an NRDY interrupt. When the host controller function is selected, this module generates no interrupt.

Table 32.27 Error Detection when Receiving Data Packets

Priority for Error Detection	Error	Interrupt and Status
1	PID error	This module generates no interrupt (ignores as a damaged packet).
2	CRC error, bit stuffing error	This module generates an NRDY interrupt and sets the CRCE bit when either of the host controller function or function controller function is selected.
3	Maximum packet size exceeded error	This module generates a BEMP interrupt and sets the PID bits to STALL when either of the host controller function or function controller function is selected.

(2) DATA-PID

This module does not support the High-Bandwidth transfer. The following lists responses to received PIDs when the function controller function is selected.

1. IN direction
   - DATA0: Sent correctly as the PID of data packet.
   - DATA1: Not sent
   - DATA2: Not sent
   - mDATA: Not sent
2. OUT direction (full-speed operation)
   - DATA0: Received correctly as the PID of a data packet.
   - DATA1: Received correctly as the PID of a data packet.
   - DATA2: The packet is ignored.
   - mDATA: The packet is ignored.
3. OUT direction (high-speed operation)
   - DATA0: Received correctly as the PID of a data packet.
   - DATA1: Received correctly as the PID of a data packet.
   - DATA2: Received correctly as the PID of a data packet.
   - mDATA: Received correctly as the PID of a data packet.

(3) Interval Counter

Intervals for isochronous transfers can be set by the IITV bits in PIPEPERI. When the function controller function is selected, the functions shown in Table 32.28 are made available with the interval counter. When the host controller function is selected, the interval counter generates the token transmit timing. When the host controller function is selected, the interval counter works in the same way as in the interrupt transfer.

Table 32.28 Interval Counter Functions when the Function Controller Function is Selected

Transfer Direction	Function	Detection Conditions
IN	Transmit buffer flush	No IN token can be successfully received in the interval frame during the isochronous IN transfer.
OUT	Reporting reception of no token	No OUT token can be successfully received in the interval frame during the isochronous OUT transfer.

Since the interval counter is counted upon receiving an SOF or using the interpolated SOF, the isochronism can be maintained even if the SOF is damaged. The specifiable frame interval is 2^{IITV} frames or 2^{IITV} μ frames.

(a) Counter initialization when the function controller function is selected

This module initializes the interval counter as follows:

- Power-on reset
  The IITV bits are initialized.
- Initializing buffer memory by ACLRM
  The IITV bits are not initialized but the interval counter is initialized. Clearing the ACLRM bit to 0 causes the counter to start counting from the set IITV value.

After the interval counter is initialized, the interval counter starts counting in either of the following cases after a packet is correctly transferred.

1. When this module receives an SOF after sending data in response to the IN token with PID = BUF
2. When this module receives an SOF after receiving the OUT token data with PID = BUF

The interval counter is not initialized under the following conditions.

1. When PID = NAK or STALL
   The interval timer does not stop. Try to execute the transaction in the next interval.
2. USB bus reset and USB suspended
   The IITV bits are not initialized. When this module receives an SOF, the interval counter starts counting from the value before receiving the SOF.

(b) Interval count and transfer control when the host controller function is selected

This module controls the token transmission intervals using the set IITV value. This module sends a token for the selected pipe once every 2^IITV times of (μ) frames.

This module counts the interval at every 1-ms frame for the pipe used for communication with the full-speed/low-speed peripheral device connected to the high-speed HUB.

This module starts counting the token transmission interval from the next (μ) frame where PID = BUF is specified by the software.

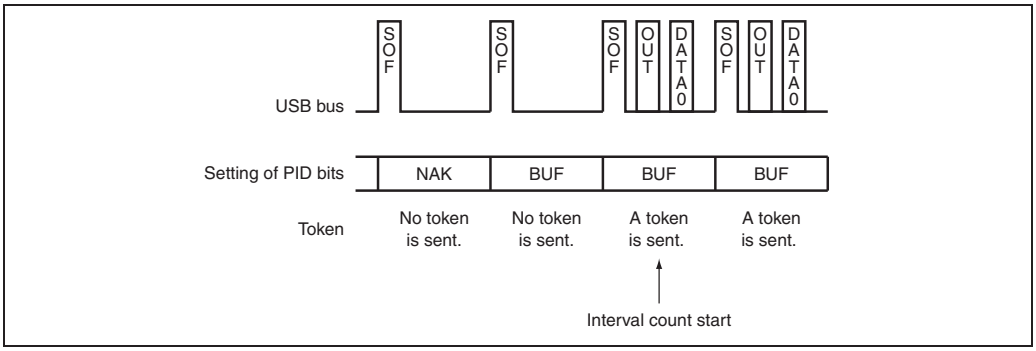


Figure 32.12 Transmission of Tokens when IITV = 0

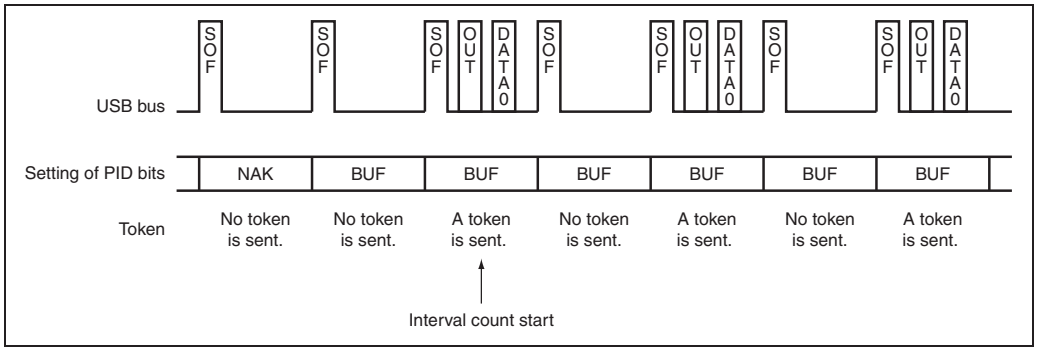


Figure 32.13 Transmission of Tokens when IITV = 1

When the selected pipe is isochronous transfer type, this module performs the following operations in connection with the token transmission interval control. Even if the NRDY interrupt generation conditions are satisfied, this module sends tokens.

1. When the selected pipe is Isochronous-IN transfer pipe

   This module sends an In-Token. When this module does not successfully receive a packet from the peripheral device (including no response and a packet error), this module generates an NRDY interrupt.

   When the IN-Token transmit timing comes before receiving data caused by the FIFO buffer full (due to a delay of reading data from the FIFO buffer by the software or DMAC), this module indicates OVRN = 1 and generates an NRDY interrupt.
2. When the selected pipe is Isochronous-OUT transfer pipe

   When the OUT-Token transmit timing comes with no transmittable data in the FIFO buffer (due to a delay of writing data to the FIFO buffer by the software or DMAC), this module indicates OVRN = 1, generates an NRDY interrupt, and sends a Zero-Length packet.

   The token transmission interval is reset in the following cases.

   — When this module is reset by the hardware (The set IITV value is also cleared to 0.)

   — When ACLRM is set to 1 by the software

(c) Interval count and transfer control when the function controller function is selected

1. When the selected pipe is Isochronous-OUT transfer pipe

   When this module receives no data packet in (μ) frames at the intervals specified by the IITV bits, this controller generates an NRDY interrupt.

   When this module cannot receive data due to a CRC error in the data packet, FIFO buffer full, or other reasons, this module also generates an NRDY interrupt.

   An NRDY interrupt is generated at the SOF packet receive timing. Even if the SOF packet is damaged, this module generates an NRDY interrupt at the SOF packet receive timing using the internal interpolation function.

   When IITV ≠ 0, however, this module generates an NRDY interrupt at the SOF packet receive timing in each interval after the interval count starts.

   When PID = NAK is set by the software after the interval timer is activated, this module generates no NRDY interrupt even when this module receives an SOF packet.

   The interval count start conditions vary with the set IITV value.

   — When IITV = 0: The interval count starts from the next (μ) frame where the PID bits for the selected pipe is changed to BUF.

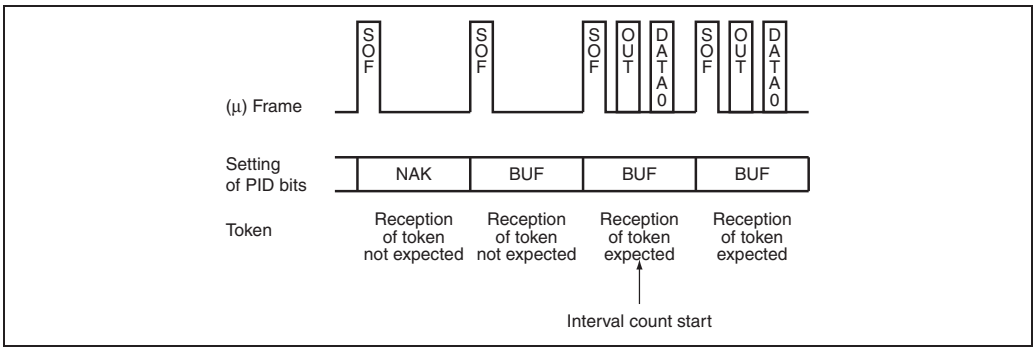


Figure 32.14 (μ) Frames and Expectation of Receiving a Token when IITV = 0

- When IITV ≠ 0: The interval count starts from the time when this module successfully receives the first data packet after the PID bits for the selected pipe is changed to BUF.

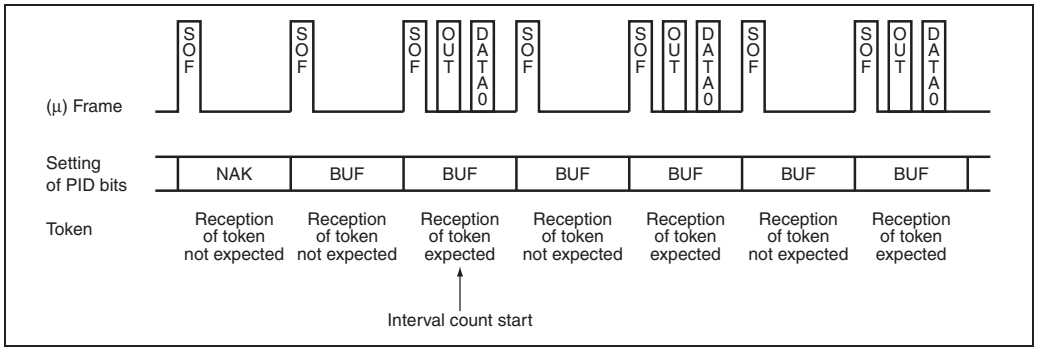


Figure 32.15 (μ) Frames and Expectation of Receiving a Token when IITV ≠ 0

2. When the selected pipe is Isochronous-IN transfer pipe

   Use the selected pipe by combining with the setting of IFIS = 1. When IFIS = 0, this module sends data packets in response to received tokens irrespective of the IITV value.

   When this module receives no IN-Token in (μ) frames at the intervals specified by the IITV bits with transmittable data stored in the FIFO buffer with IFIS = 1, this module clears the FIFO buffer.

   When this module cannot receive data due to a CRC error or another bus error in the IN-Token, this module also clears the FIFO buffer.

   The FIFO buffer is cleared at the SOF packet receive timing. Even if the SOF packet is damaged, this module clears the FIFO buffer at the SOF packet receive timing using the internal interpolation function.

   The interval count start conditions vary with the set IITV value (same as Isochronous-OUT transfer).

   When the function controller function is selected, the interval count start conditions are as follows:

   — When this module is reset by the hardware (The set IITV value is also cleared to 0.)
   — When ACLRM is set to 1 by the software
   — When this module detects a USB reset

(4) Transmit Data Setup in Isochronous Transfer when the Function Controller Function is Selected

In isochronous data transmission when the function controller function is selected, this module can send a data packet in the next frame after this module detects an SOF packet after writing data to the buffer. This function is referred to as the isochronous transfer transmit data setup function. With this function, the frame that started data transmission can be identified.

When the buffer memory is used as a double buffer, even if writing data to both buffers is completed, only one side that finished writing earlier becomes transferable. For this reason, even if multiple IN tokens are received in the same frame, only one packet of the buffer memory is sent.

When the buffer memory is ready for transmission in the IN token reception cycle, this module sends data and an ACK response. However, when the buffer memory is not ready for transmission, this module sends a Zero-Length packet and generates an underrun error.

Figure 32.16 shows an example of transmission using the isochronous transfer transmit data setup function of this module when IITV = 0 (each frame). Transmission of a Zero-Length packet is indicated as hatched “Null” in the figure.

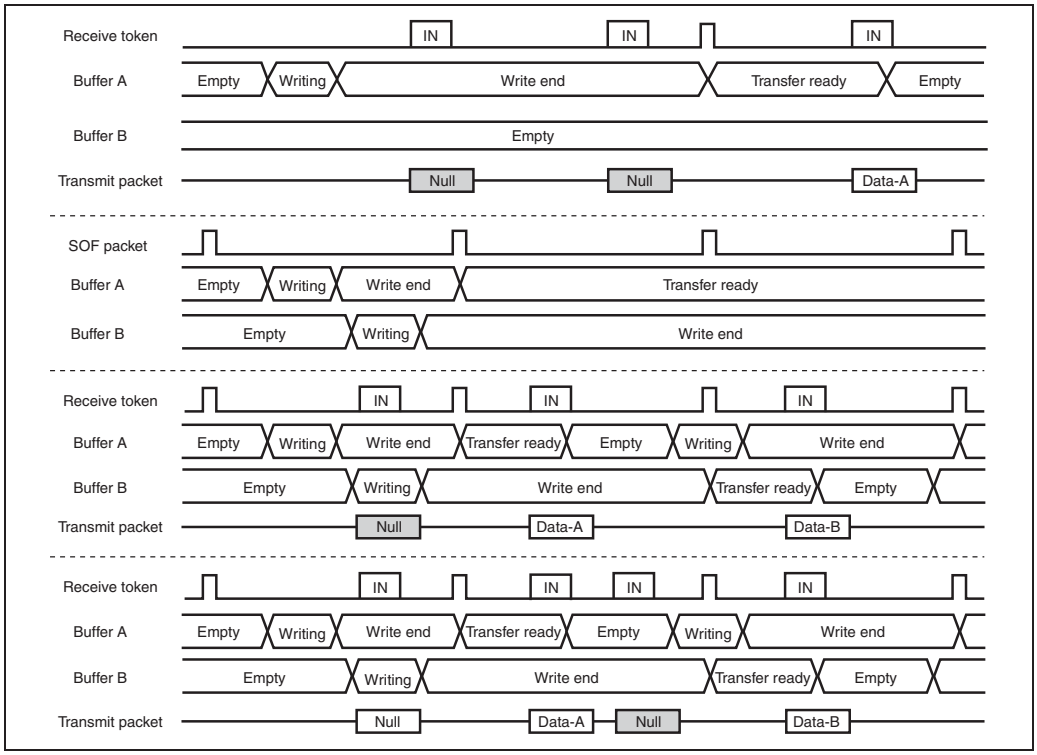


Figure 32.16 Example of Transmit Data Setup Function

(5) Transmit Buffer Flush in Isochronous Transfer when the Function Controller Function is Selected

In isochronous data transmission when the function controller function is selected, this module receives no IN token in the interval frame. When this module receives the SOF or μ SOF packet of the next frame, this module regards the IN token as damaged and clears the buffer that is ready for transmission to make it writable.

At this time, when the buffer memory is used as a double buffer and writing data to both buffers is completed, this module regards the discarded buffer memory data as transmitted in the same interval frame, and drives the buffer memory that is not discarded due to the reception of an SOF or μ SOF packet into the transmission ready state.

The buffer flush function activation timing varies depending on the IITV value.

- When IITV = 0
  This module activates the buffer flush function from the next frame after the pipe is enabled.
- When IITV ≠ 0
  This module activates the buffer flush function from the first normal transaction.

Figure 32.17 shows an example of the buffer flush function of this module. For tokens before the interval frame (outside the specified interval), however, this module sends the data stored in the buffer according to the data setup state or sends a Zero-Length packet as an underrun error.

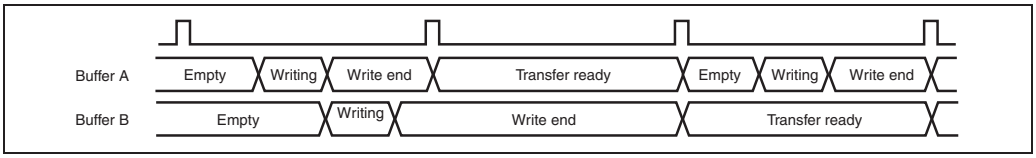


Figure 32.17 Example of Buffer Flush Function

Figure 32.18 shows an example of an interval error of this module. Interval errors are the following five. An interval error occurs at timing [1] in the figure, and the buffer flush function is activated.

When an interval error occurs, the buffer flush function is activated in the IN transfer and an NRDY interrupt occurs in the OUT transfer.

Discriminate an NRDY interrupt (including a receive packet error) from an overrun error with the OVRN bit.

This module sends a response to the hatched tokens in the figure according to the buffer memory status.

1. IN direction
   — When the buffer is ready to transmit data, this module sends the data and an ACK response.
   — When the buffer is not ready to transmit data, this module sends a Zero-Length packet and generates an underrun error.
2. OUT direction
   — When the buffer is ready to receive data, this module receives data and sends an ACK response.
   — When the buffer is not ready to receive data, this module discards the data and generates an overrun error.

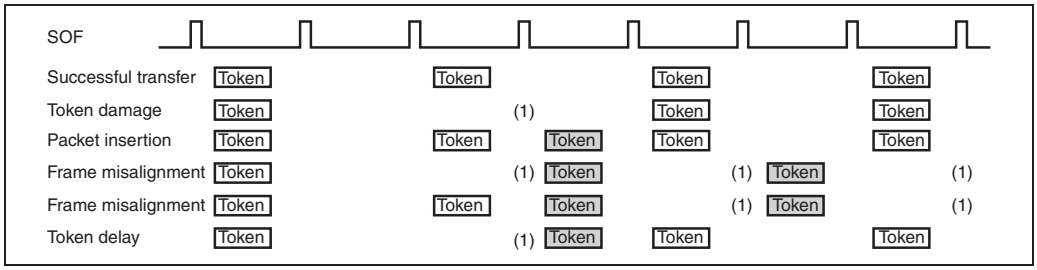


Figure 32.18 Example of Interval Error when IITV = 1

32.4.9 SOF Interpolation Function

When the function controller function is selected, in case this module cannot receive SOF packets at intervals of 1 ms (full-speed operation) or 125 μs (high-speed operation) due to damage or missing of SOF packets, this module interpolates the SOF. The SOF interpolation starts functioning when SYSCFG.USBE = 1, SYSCFG.SCKE = 1, and at the SOF packet receive timing. Furthermore, the interpolation function is initialized in the following cases.

- Power-on reset
- USB bus reset
- When the suspended state is detected

The SOF interpolation functions with the following specifications.

- The frame intervals (125 μs or 1 ms) conform to the result of the reset handshake protocol.
- The SOF interpolation does not function until this module receives an SOF packet.
- After receiving the first SOF packet, 125 μs or 1 ms is counted by the internal 48-MHz clock to interpolate the SOF.
- After receiving the second SOF packet or a following packet, the SOF is interpolated using the previous receive intervals.
- The SOF interpolation does not function in the suspended state and during a USB bus reset. (When this module enters the suspended state in high-speed operation, the SOF interpolation continues for 3 ms from the final packet.)

This module activates the following functions based on the reception of SOF packets. When one or more SOF packets are lost, normal operation can be continued to perform the SOF interpolation.

- Updating frame numbers and μ frame numbers
- SOFR interrupt timing and μ SOF lock

- Isochronous transfer interval count

When one or more SOF packets are lost in full-speed operation, the FRNM bits in FRMNUM are not updated. When one or more μ SOF packets are lost in high-speed operation, the FRNM bits are updated. However, when a μ SOF packet with UFRNM = 000 is lost, the FRNM bits are not updated even if following μ SOF packets with UFRNM ≠ 000 are successfully received.

32.4.10 Pipe Schedule

(1) Transaction Issuing Conditions

When the host controller function is selected, this module issues transactions after setting UACT = 1 according to the conditions in Table 32.29.

Table 32.29 Transaction Issuing Conditions

	Issuing Conditions				
Transaction	**DIR**	**PID**	**IITV0**	**Buffer Status**	**SUREQ**
Setup	—*1	—*1	—*1	—*1	Set to 1
Control transfer data stage, status stage, bulk transfer	IN	BUF	Disabled	Data receive area remaining	—*1
	OUT	BUF	Disabled	Transmit data stored	—*1
Interrupt transfer	IN	BUF	Enabled	Data receive area remaining	—*1
	OUT	BUF	Enabled	Transmit data stored	—*1
Isochronous transfer	IN	BUF	Enabled	*2	—*1
	OUT	BUF	Enabled	*3	—*1

Notes: 1. "—" means that the condition is not related to issuing tokens. "Enabled" shows that transactions are issued only in transfer frames by the interval counter in interrupt transfers and isochronous transfers. "Disabled" shows that transactions are issued irrespective of the interval counter.

2. Transactions are issued irrespective of whether the buffer has a data receive area or not. However, when the buffer has no data receive area, the receive data is discarded.

3. Transactions are issued irrespective of whether the buffer contains transmit data or not. However, when the buffer contains no transmit data, this module sends a Zero-Length packet.

(2) Transfer Schedule

The following describes the within-the-frame transfer scheduling of this module. This module transfers packets in the following procedure after sending the SOF.

1. Execute periodic transfer
   This module searches pipes in the order of pipe 1 -> pipe 2 -> pipe 6 -> pipe 7 -> pipe 8 -> pipe 9. When transactions can be issued in any of these pipes in isochronous transfers or interrupt transfers, this module issues transactions.
2. Control transfer setup transaction
   When the DCP indicates that the setup transaction is enabled, this module sends it.
3. Execute bulk transfer/control transfer data stage and status stage
   This module searches pipes in the order of pipe 1 -> pipe 2 -> pipe 3 -> pipe 4 -> pipe 5. When transactions can be issued in any of these pipes in the bulk transfer/control transfer data stage and control transfer status stage, this module executes transactions.
   When this module issued a transaction and received ACK or NAK from the peripheral device, this module shifts to the transactions for the next pipe. When there is time for transfer within the frame, this module repeats the operation in step 3.

(3) Enabling USB Communication

Setting the UACT bit in DVSTCTR to 1 starts transmission of an SOF or µ SOF, and issuing of transactions is enabled.

Setting the UACT bit to 0 stops transmission of an SOF or µ SOF, and issuing of transactions is suspended. When the UACT bit is changed from 1 to 0, the USB communication is halted after the next SOF or µ SOF is transmitted.

32.5 OTG Function

(1) Example of OTG Connection

The following shows an example of connection when MAX3355E is used as an OTG external device.

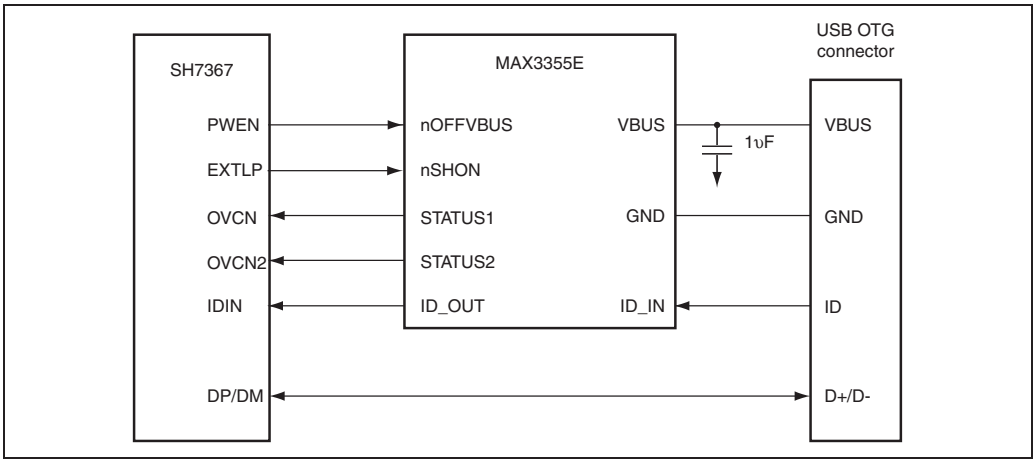


Figure 32.19 Example of OTG Connection

(2) Identifying Device ID

This module identifies either of the host controller function (device A) or function controller function (device B) using the IDMON bit. The IDIN pin state can be monitored with the IDMON bit. For the device ID specifications, see the OTG External Device Manual.

(3) HNP

The following shows a software processing flow for two transitions: (1) from the function controller function (device B) to the host controller function (device A), and (2) from the host controller function (device A) to the function controller function (device B).

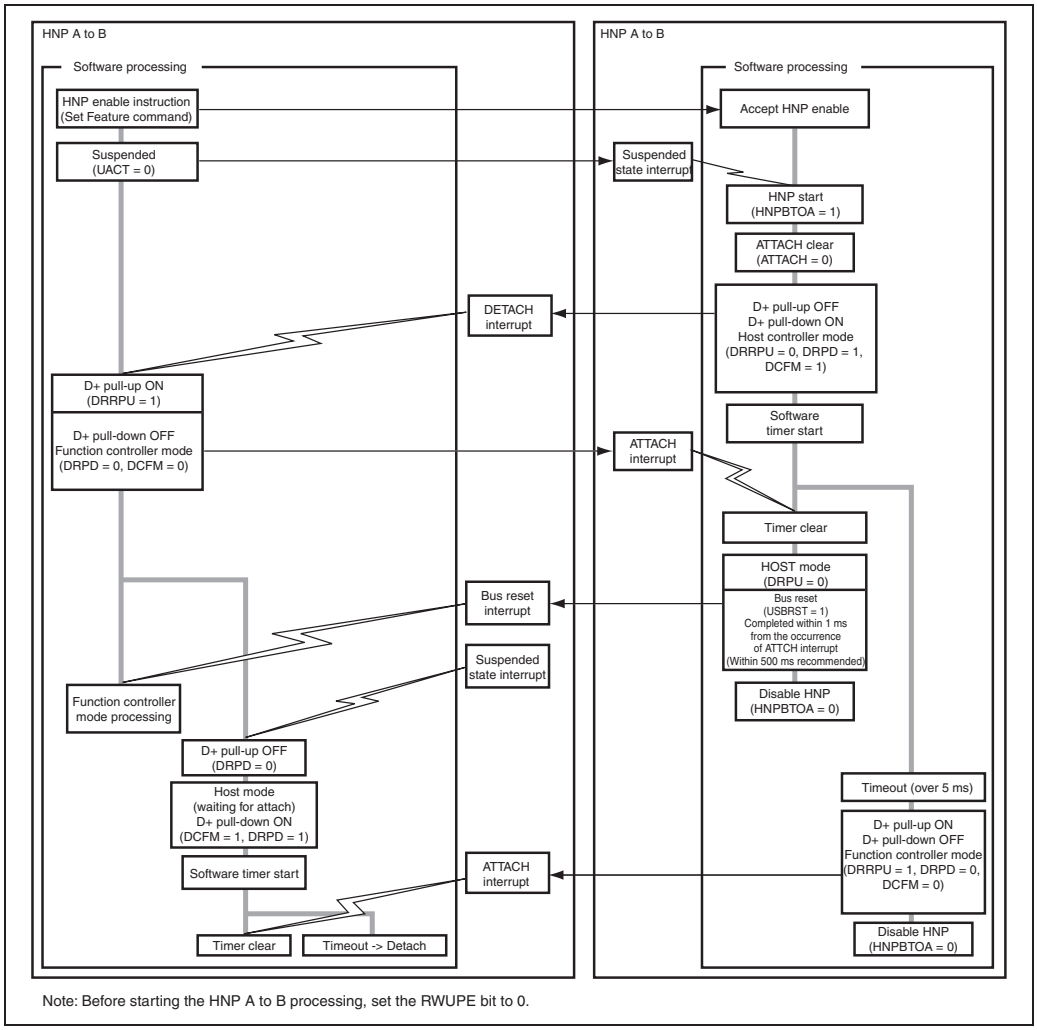


Figure 32.20 HNP Processing Flow

(4) SRP

The VBUS pin level can be sensed by the OVCMON1 and OVCMON0 bits. The values that are input to the OVCN_0 pin and OVCN2 pin are read from the OVCMON1 and OVCMON0 bits. For the VBUS level specifications, see the OTG External Device Manual.

32.6 Guidelines for Designing USB2.0 Hi-Speed Boards

32.6.1 USB Transmission Line

The USB transmission line indicates the pattern that connects the USB connector and this LSI's on-chip USB transceiver.

The USB2.0 has three communication modes: Hi-Speed, Full-Speed and Low-Speed modes. The transmission speed in the Hi-Speed mode is 480 Mbps. Therefore, the USB transmission line must be designed as a high-frequency circuit. Impedance control is required for the USB transmission line.

- The characteristic impedance required for the USB Hi-Speed transmission line is differential impedance 90Ω (±15%).
- The pattern width and pattern pitch for impedance control vary depending on the board thickness, material and layer configuration. For details, consult the board manufacturer.
- A maximum delay of 1 ns is allowed from the USB connector to this LSI. Therefore it is recommended that the pattern length from the USB device to the USB connector is less than 50 mm and the difference between the pattern lengths for D+ and D– is less than 2.5 mm for a generic PCB.
- The lower layer of the USB transmission line must be a solid ground plane. The ground must be wider than the USB transmission line by 2 mm or more. The power supply for a solid ground plane is DG33.
- Do not allocate other signal lines near to the USB transmission line. In particular, lines carrying widely fluctuating signals, such as clock and data bus lines, must be assigned far from the USB transmission line. Furthermore, layout of the USB transmission lines must be such that they do not cross with other signal lines.
- Locate the USB transmission line on the same layer without passing it through a through-hole. Do not create stubs.
- Place the USB transmission lines so that they are equally spaced from each other.
- Locate the USB transmission line as far as possible from the oscillator, power supply circuit, and other I/O connectors.
- Try to avoid bending the USB transmission line as far as possible. If it is absolutely necessary to bend it, do not bend it at acute or right angles. Bend it moderately, at not more than 45 degrees, or bend it into an arc.
- It is recommended to guard ring the clock, reset, read, write and chip select signals with grounds.

When a resistance is connected to the USB transmission line, locate it near to the USB transmission line. The connecting wire must be as short as possible.

32.6.2 Power Supply and Ground Pattern

Analog power supply: AV12 (1.2V), AV33 (3.3V)

Digital power supply: UV12 (1.2V), DV12 (1.2V), DV33 (3.3V)

Analog ground: AG12, AG33

Digital ground: UG12, DG12, DG33

- It is recommended to separate power supplies and ground patterns into digital and analog.
- Connect the power supplies and grounds firmly on wide areas.
- Tantalum solid electrolytic capacitors or ceramic capacitors having excellent high-frequency characteristics are recommended as capacitors for power supplies.
- Aluminum electrolytic capacitors affect the jitter value during measurement of EYE diagram. Use the capacitors after adequately designing and testing them.
- It is recommended to place decoupling capacitors with values of 0.1uF, 0.01uF, and 0.001uF as close as possible to the USB power supply.

32.6.3 Oscillation

- Provide an oscillation circuit near the clock input pin for USB (EXTAL2). It is recommended to guard ring EXTAL2 with a ground.
- When using a crystal resonator, consult its manufacturer to determine the circuit constant.

32.6.4 VBUS

- When this LSI is used as a host controller, it must supply the VBUS power. To do this it is recommended to use a power switch IC with an overcurrent limiter for the USB power bus (hereafter called USB power swtich IC). Current limits should be deteremined on the basis of the current values of the system power supply and the USB peripheral devices to be communicated with. For details on circuits, see the datasheet of your USB power switch IC. Input VBUS (5V) to the VBUS1_0 pin of this LSI. Provide the VBUS1_0 pin with a capacitance of 1uF and a resistance of 100Ω to 1000Ω (never exceeding 1000Ω) as a filter circuit. The potential of the VBUS is normally 5.0V, but when a cable is connected, overshoot may occur as a result of a reflection due to impedance mismatch between the VBUS power IC

and the VBUS in the cable. This overshoot can damage elements. For this reason, the element shown in Figure 32.1, Connection to the USB Connector, should be connected between the VBUS1_0 pin and the connector as a filter circuit.

32.6.5 REFRIN_0 Pin

- Provide a resistor (hereafter called reference resistor) of 5.6 kΩ ±1%, between the REFRIN_0 pin and AG33.
- Locate the reference resistor as close as possible to this LSI.
- The REFRIN_0 pin, the reference resistor and AG33 should be wired on wide areas and the shortest length.
- Use a wiring pattern for and only for the reference resistor and AG33. The pattern should be connected to the analog ground. The pattern should be designed avoiding the possibility for common impedance between REFRIN_0 and other signals.
- To prevent cross talk, very-frequently switched signals such as DP, DM, clocks, and control signals for addresses and data, should not be placed near to the reference resistor, and their patterns should neither get across nor go parallel to the wiring pattern between the reference resistor and the REFRIN_0 pin.

It is recommended to guard ring the reference resistor and its wiring pattern with ground.

Section 33 USB High-Speed 1 Module (USBHS1)

This module is a USB controller provided with the USB host controller function and the function controller function. When the host controller function is selected, high-speed transfer, full-speed transfer, and low-speed transfer conforming to the USB (universal serial bus) Specification 2.0 are available. When the function controller function is selected, high-speed transfer and full-speed transfer are available. Provided with an on-chip USB transceiver, this module also supports all transfer types defined by the USB Specification.

This module can use up to sixteen pipes when the function controller is selected. Furthermore, for pipes 1 to F(Pipe A to Pipe F are effective only when the function controller function is selected), arbitrary endpoint numbers can be allocated according to peripheral devices to be communicated and user systems.

33.1 Features

(1) Incorporates a host controller and a function controller conforming to USB High Speed. But, because the function when the function controller is selected is enhanced, this module is recommended to be selected as a function controller.

- On-chip USB host controller and function controller
- The USB host controller function and the function controller function are selectable by register setting.
- On-chip USB transceiver

(2) Achieves space-saving mount with less external elements.

- Direct connection of the VBUS0_1 and VBUS1_1 signal to the input pin of this module
- On-chip D+ pull-up resistor (function operation mode)
- On-chip D+/D- pull-down resistors (host operation mode)
- On-chip D+/D- terminating resistors (high-speed operation mode)
- On-chip D+/D- output resistors (full-speed operation mode)

(3) Supports all data transfer types for USB communication.

- Control transfer
- Bulk transfer
- Interrupt transfer (except for high bandwidth)
- Isochronous transfer (except for high bandwidth)

(4) Dedicated DMA interface

- On-chip 2-channel DMA interface

(5) Pipe configuration

- Up to twelve pipes are selectable (including the default control pipe)
- Programmable pipe configuration
- Arbitrary endpoint numbers can be allocated to pipes 1 to 9 when host controller function is selected. Arbitrary endpoint numbers can be allocated to pipes 1 to F when function controller function is selected.
- Settable transfer conditions for each pipe are as follows:

  Pipe 0: A pipe only for control transfer with a 64-byte (fixed) single buffer

  Pipes 1 and 2: Pipes that can select bulk transfer or isochronous transfer (Continuous transfer mode and buffer size are programmable.) (Double buffer can be specified with up to 2 Kbytes.)

  - When host controller function is selected:

  Pipes 3 to 5: Pipes only for bulk transfer (Continuous transfer mode and buffer size are programmable.) (Double buffer can be specified with up to 2 Kbytes.)

  Pipes 6 to 9: Pipes only for interrupt transfer with a 64-byte (fixed) single buffer

  - When function controller function is selected:

  Pipes 3 to 5 and 9 to F: Pipes only for bulk transfer (Continuous transfer mode and buffer size are programmable.) (Double buffer can be specified with up to 2 Kbytes.)

  Pipes 6 to 8: Pipes only for interrupt transfer with a 64-byte (fixed) single buffer

(6) Features with host controller function

- Supports high-speed transfer (480 Mbps), full-speed transfer (12 Mbps), and low-speed transfer (1.5 Mbps).
- Allows communication with multiple peripheral devices through a hub.
- Reset handshake auto-response
- Automated SOF/packet transmission schedule
- Isochronous transfer/interrupt transfer interval setting function

(7) Features with function controller function

- Supports high-speed transfer (480 Mbps) and full-speed transfer (12 Mbps).
- High-speed or full-speed automatic recognition of operation using the reset handshake auto-response function

- Control transfer stage management function
- Device state management function
- Auto-response to the SET_ADDRESS request
- NAK response interrupt function (NRDY)
- SOF interpolation function

(8) Other functions

- Transfer terminating function using transaction count
- SOF pulse output function
- BRDY interrupt event notification timing change function (BFRE)
- Buffer memory auto-clear function (DCLRM) after reading data of the pipe specified by the DnFIFO (n = 0, 1) port
- NAK setting function (SHTNAK) for the response PID due to the transfer end

33.2 Input/Output Pins

Table 33.1 lists the input and output pins of the USB.

Table 33.1 Pin Configuration of USB

Classification	Pin Name	Name	I/O	Description
USB bus interface	DP_1	USB D+ data	I/O	D+ Input/output of the On-chip Transceiver Connect this pin to the D+ pin of the USB bus.
	DM_1	USB D- data	I/O	D- Input/output of the On-chip Transceiver Connect this pin to the D- pin of the USB bus.
VBUS monitoring input	VBUS0_1	VBUS input	Input	USB Cable Connection Monitoring Pin Connect this pin directly to VBUS of the USB bus. This pin is used to detect VBUS connection or disconnection. When not connecting to VBUS of the USB bus, fix this pin to +5V. Also supply +5V to this pin when the host controller function is selected. However, VBUS cannot be supplied to devices to be connected.
	VBUS1_1	VBUS input	Input	USB Cable Connection Monitoring Pin Connect this pin directly to VBUS of the USB bus. This pin is used to detect VBUS connection or disconnection. When not connecting to VBUS of the USB bus, fix this pin to +5V. Also supply +5V to this pin when the host controller function is selected. However, VBUS cannot be supplied to devices to be connected.
Reference resistance	REFRIN_1	Reference input	Input	Reference Resistance Connecting Pin Connect this pin to the ground through a 5.6 kΩ ±1% resistor.

Classification	Pin Name	Name	I/O	Description
external device interface	PWEN_1	Power enable	Output	VBUS Supply ON/OFF Control Pin When using MAX3355E as an external device, connect this pin directly to the OFFVBUS0_1 and VBUS1_1 pin of the MAX3355E.
	EXTLP_1	external device low power	Output	External Device Power Shutdown Control Pin When using MAX3355E as an external device, connect this pin directly to the SHDN pin of the MAX3355E.
	OVCN_1	Overcurrent detection	Input	Overcurrent Status Monitoring Pin When using MAX3355E as an external device, connect this pin directly to the STATUS1 pin of the MAX3355E.
	OVCN2_1	Overcurrent detection 2	Input	Overcurrent Status Monitoring Pin When using MAX3355E as an external device, connect this pin directly to the STATUS2 pin of the MAX3355E.
	IDIN_1	Device ID	Input	Device ID Monitoring Pin When using MAX3355E as an external device, connect this pin directly to the ID_OUT pin of the MAX3355E.

33.3 Register Descriptions

Table 33.2 lists the registers used in this module. Table 33.3 list the register states in each processing mode.

Table 33.2 Register Configuration

Register Name	Abbreviation	R/W	Address	Access Size
System configuration control register	SYSCFG	R/W	H'E68B 0000	16
CPU bus wait register	BUSWAIT	R/W	H'E68B 0002	16
System configuration status register	SYSSTS	R	H'E68B 0004	16
Device state control register	DVSTCTR	R/W	H'E68B 0008	16
Test mode register	TESTMODE	R/W	H'E68B 000C	16
CFIFO port register	CFIFO	R/W	H'E68B 0014	32
CFIFO port select register	CFIFOSEL	R/W	H'E68B 0020	16
CFIFO port control register	CFIFOCTR	R/W	H'E68B 0022	16
D0FIFO port select register	D0FIFOSEL	R/W	H'E68B 0028	16
D0FIFO port control register	D0FIFOCTR	R/W	H'E68B 002A	16
D1FIFO port select register	D1FIFOSEL	R/W	H'E68B 002C	16
D1FIFO port control register	D1FIFOCTR	R/W	H'E68B 002E	16
Interrupt enable register 0	INTENB0	R/W	H'E68B 0030	16
Interrupt enable register 1	INTENB1	R/W	H'E68B 0032	16
BRDY interrupt enable register	BRDYENB	R/W	H'E68B 0036	16
NRDY interrupt enable register	NRDYENB	R/W	H'E68B 0038	16
BEMP interrupt enable register	BEMPENB	R/W	H'E68B 003A	16
SOF output configuration register	SOFCFG	R/W	H'E68B 003C	16
Interrupt status register 0	INTSTS0	R/W	H'E68B 0040	16
Interrupt status register 1	INTSTS1	R/W	H'E68B 0042	16
BRDY interrupt status register	BRDYSTS	R/W	H'E68B 0046	16
NRDY interrupt status register	NRDYSTS	R/W	H'E68B 0048	16
BEMP interrupt status register	BEMPSTS	R/W	H'E68B 004A	16
Frame number register	FRMNUM	R/W	H'E68B 004C	16
μ frame number register	UFRMNUM	R/W	H'E68B 004E	16
USB address register	USBADDR	R	H'E68B 0050	16

Register Name	Abbreviation	R/W	Address	Access Size
USB request type register	USBREQ	R	H'E68B 0054	16
USB request value register	USBVAL	R	H'E68B 0056	16
USB request index register	USBINDX	R	H'E68B 0058	16
USB request length register	USBLENG	R	H'E68B 005A	16
DCP configuration register	DCPCFG	R/W	H'E68B 005C	16
DCP maximum packet size register	DCPMAXP	R/W	H'E68B 005E	16
DCP control register	DCPCTR	R/W	H'E68B 0060	16
Pipe window select register	PIPESEL	R/W	H'E68B 0064	16
Pipe configuration register	PIPECFG	R/W	H'E68B 0068	16
Pipe buffer register	PIPEBUF	R/W	H'E68B 006A	16
Pipe maximum packet size register	PIPEMAXP	R/W	H'E68B 006C	16
Pipe cycle control register	PIPEPERI	R/W	H'E68B 006E	16
Pipe 1 control register	PIPE1CTR	R/W	H'E68B 0070	16
Pipe 2 control register	PIPE2CTR	R/W	H'E68B 0072	16
Pipe 3 control register	PIPE3CTR	R/W	H'E68B 0074	16
Pipe 4 control register	PIPE4CTR	R/W	H'E68B 0076	16
Pipe 5 control register	PIPE5CTR	R/W	H'E68B 0078	16
Pipe 6 control register	PIPE6CTR	R/W	H'E68B 007A	16
Pipe 7 control register	PIPE7CTR	R/W	H'E68B 007C	16
Pipe 8 control register	PIPE8CTR	R/W	H'E68B 007E	16
Pipe 9 control register	PIPE9CTR	R/W	H'E68B 0080	16
Pipe A control register	PIPEACTR*	R/W	H'E68B 0082	16
Pipe B control register	PIPEBCTR*	R/W	H'E68B 0084	16
Pipe C control register	PIPECCTR*	R/W	H'E68B 0086	16
Pipe D control register	PIPEDCTR*	R/W	H'E68B 0088	16
Pipe E control register	PIPEECTR*	R/W	H'E68B 008A	16
Pipe F control register	PIPEFCTR*	R/W	H'E68B 008C	16
Pipe 1 transaction counter enable register	PIPE1TRE	R/W	H'E68B 0090	16
Pipe 1 transaction counter register	PIPE1TRN	R/W	H'E68B 0092	16
Pipe 2 transaction counter enable register	PIPE2TRE	R/W	H'E68B 0094	16
Pipe 2 transaction counter register	PIPE2TRN	R/W	H'E68B 0096	16
Pipe 3 transaction counter enable register	PIPE3TRE	R/W	H'E68B 0098	16

Register Name	Abbreviation	R/W	Address	Access Size
Pipe 3 transaction counter register	PIPE3TRN	R/W	H'E68B 009A	16
Pipe 4 transaction counter enable register	PIPE4TRE	R/W	H'E68B 009C	16
Pipe 4 transaction counter register	PIPE4TRN	R/W	H'E68B 009E	16
Pipe 5 transaction counter enable register	PIPE5TRE	R/W	H'E68B 00A0	16
Pipe 5 transaction counter register	PIPE5TRN	R/W	H'E68B 00A2	16
Pipe B transaction counter enable register	PIPEBTRE*	R/W	H'E68B 00A4	16
Pipe B transaction counter register	PIPEBTRN*	R/W	H'E68B 00A6	16
Pipe C transaction counter enable register	PIPECTRE*	R/W	H'E68B 00A8	16
Pipe C transaction counter register	PIPECTRN*	R/W	H'E68B 00AA	16
Pipe D transaction counter enable register	PIPEDTRE*	R/W	H'E68B 00AC	16
Pipe D transaction counter register	PIPEDTRN*	R/W	H'E68B 00AE	16
Pipe E transaction counter enable register	PIPEETRE*	R/W	H'E68B 00B0	16
Pipe E transaction counter register	PIPEETRN*	R/W	H'E68B 00B2	16
Pipe F transaction counter enable register	PIPEFTRE*	R/W	H'E68B 00B4	16
Pipe F transaction counter register	PIPEFTRN*	R/W	H'E68B 00B6	16
Pipe 9 transaction counter enable register	PIPE9TRE	R/W	H'E68B 00B8	16
Pipe 9 transaction counter register	PIPE9TRN	R/W	H'E68B 00BA	16
Pipe A transaction counter enable register	PIPEATRE*	R/W	H'E68B 00BC	16
Pipe A transaction counter register	PIPEATRN*	R/W	H'E68B 00BE	16
Device address 0 configuration register	DEVADD0	R/W	H'E68B 00D0	16
Device address 1 configuration register	DEVADD1	R/W	H'E68B 00D2	16
Device address 2 configuration register	DEVADD2	R/W	H'E68B 00D4	16
Device address 3 configuration register	DEVADD3	R/W	H'E68B 00D6	16
Device address 4 configuration register	DEVADD4	R/W	H'E68B 00D8	16
Device address 5 configuration register	DEVADD5	R/W	H'E68B 00DA	16
Device address 6 configuration register	DEVADD6	R/W	H'E68B 00DC	16
Device address 7 configuration register	DEVADD7	R/W	H'E68B 00DE	16
Device address 8 configuration register	DEVADD8	R/W	H'E68B 00E0	16
Device address 9 configuration register	DEVADD9	R/W	H'E68B 00E2	16
Device address A configuration register	DEVADDA	R/W	H'E68B 00E4	16

note: PIPEA to PIPEF are effective only when the function controller function is selected.

Table 33.3 Register States in Each Processing Mode

Register Abbreviation	Power-On Reset	Software Standby	Module Standby	Sleep
SYSCFG	Initialized	Retained	Retained	Retained
BUSWAIT	Initialized	Retained	Retained	Retained
SYSSTS	Initialized	Retained	Retained	Retained
DVSTCTR	Initialized	Retained	Retained	Retained
TESTMODE	Initialized	Retained	Retained	Retained
CFIFO	Initialized	Retained	Retained	Retained
CFIFOSEL	Initialized	Retained	Retained	Retained
CFIFOCTR	Initialized	Retained	Retained	Retained
D0FIFOSEL	Initialized	Retained	Retained	Retained
D0FIFOCTR	Initialized	Retained	Retained	Retained
D1FIFOSEL	Initialized	Retained	Retained	Retained
D1FIFOCTR	Initialized	Retained	Retained	Retained
INTENB0	Initialized	Retained	Retained	Retained
INTENB1	Initialized	Retained	Retained	Retained
BRDYENB	Initialized	Retained	Retained	Retained
NRDYENB	Initialized	Retained	Retained	Retained
BEMPENB	Initialized	Retained	Retained	Retained
SOFCFG	Initialized	Retained	Retained	Retained
INTSTS0	Initialized	Retained	Retained	Retained
INTSTS1	Initialized	Retained	Retained	Retained
BRDYSTS	Initialized	Retained	Retained	Retained
NRDYSTS	Initialized	Retained	Retained	Retained
BEMPSTS	Initialized	Retained	Retained	Retained
FRMNUM	Initialized	Retained	Retained	Retained
UFRMNUM	Initialized	Retained	Retained	Retained
USBADDR	Initialized	Retained	Retained	Retained

Register Abbreviation	Power-On Reset	Software Standby	Module Standby	Sleep
USBREQ	Initialized	Retained	Retained	Retained
USBVAL	Initialized	Retained	Retained	Retained
USBINDX	Initialized	Retained	Retained	Retained
USBLENG	Initialized	Retained	Retained	Retained
DCPCFG	Initialized	Retained	Retained	Retained
DCPMAXP	Initialized	Retained	Retained	Retained
DCPCTR	Initialized	Retained	Retained	Retained
PIPESEL	Initialized	Retained	Retained	Retained
PIPECFG	Initialized	Retained	Retained	Retained
PIPEBUF	Initialized	Retained	Retained	Retained
PIPEMAXP	Initialized	Retained	Retained	Retained
PIPEPERI	Initialized	Retained	Retained	Retained
PIPE1CTR	Initialized	Retained	Retained	Retained
PIPE2CTR	Initialized	Retained	Retained	Retained
PIPE3CTR	Initialized	Retained	Retained	Retained
PIPE4CTR	Initialized	Retained	Retained	Retained
PIPE5CTR	Initialized	Retained	Retained	Retained
PIPE6CTR	Initialized	Retained	Retained	Retained
PIPE7CTR	Initialized	Retained	Retained	Retained
PIPE8CTR	Initialized	Retained	Retained	Retained
PIPE9CTR	Initialized	Retained	Retained	Retained
PIPEACTR*	Initialized	Retained	Retained	Retained
PIPEBCTR*	Initialized	Retained	Retained	Retained
PIPECCTR*	Initialized	Retained	Retained	Retained
PIPEDCTR*	Initialized	Retained	Retained	Retained
PIPEECTR*	Initialized	Retained	Retained	Retained
PIPEFCTR*	Initialized	Retained	Retained	Retained
PIPE1TRE	Initialized	Retained	Retained	Retained
PIPE1TRN	Initialized	Retained	Retained	Retained
PIPE2TRE	Initialized	Retained	Retained	Retained
PIPE2TRN	Initialized	Retained	Retained	Retained

Register Abbreviation	Power-On Reset	Software Standby	Module Standby	Sleep
PIPE3TRE	Initialized	Retained	Retained	Retained
PIPE3TRN	Initialized	Retained	Retained	Retained
PIPE4TRE	Initialized	Retained	Retained	Retained
PIPE4TRN	Initialized	Retained	Retained	Retained
PIPE5TRE	Initialized	Retained	Retained	Retained
PIPE5TRN	Initialized	Retained	Retained	Retained
PIPEBTRE*	Initialized	Retained	Retained	Retained
PIPEBTRN*	Initialized	Retained	Retained	Retained
PIPECTRE*	Initialized	Retained	Retained	Retained
PIPECTRN*	Initialized	Retained	Retained	Retained
PIPEDTRE*	Initialized	Retained	Retained	Retained
PIPEDTRN*	Initialized	Retained	Retained	Retained
PIPEETRE*	Initialized	Retained	Retained	Retained
PIPEETRN*	Initialized	Retained	Retained	Retained
PIPEFTRE*	Initialized	Retained	Retained	Retained
PIPEFTRN*	Initialized	Retained	Retained	Retained
PIPE9TRE	Initialized	Retained	Retained	Retained
PIPE9TRN	Initialized	Retained	Retained	Retained
PIPEATRE*	Initialized	Retained	Retained	Retained
PIPEATRN*	Initialized	Retained	Retained	Retained
DEVADD0	Initialized	Retained	Retained	Retained
DEVADD1	Initialized	Retained	Retained	Retained
DEVADD2	Initialized	Retained	Retained	Retained
DEVADD3	Initialized	Retained	Retained	Retained
DEVADD4	Initialized	Retained	Retained	Retained
DEVADD5	Initialized	Retained	Retained	Retained
DEVADD6	Initialized	Retained	Retained	Retained
DEVADD7	Initialized	Retained	Retained	Retained
DEVADD8	Initialized	Retained	Retained	Retained
DEVADD9	Initialized	Retained	Retained	Retained
DEVADDA	Initialized	Retained	Retained	Retained

note: PIPEA to PIPEF are effective only when the function controller function is selected.

33.3.1 System Configuration Control Register (SYSCFG)

SYSCFG enables or disables high-speed operation, selects the host controller function or function controller function, controls DP_1 and DM pins, and enables or disables the operation of this module.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	SCKE	—	—	HSE	DCFM	DRPD	DPR PU	—	—	—	USBE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R	R	R/W	R/W	R/W	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10	SCKE	0	R/W	USB Module Clock Enable Enables or halts the supply of the 48-MHz clock to this module. 0: The clock supply to the USB module is halted. 1: The clock supply to the USB module is enabled. When this bit is 0, only this register and BUSWAIT are readable and writable. Other registers in the USB module are readable but not writable.
9, 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
7	HSE	0	R/W	High-Speed Operation Enable 0: High-speed operation is disabled. When the function controller function is selected: Full-speed operation only When host controller function is selected: Full-speed or low-speed operation 1: High-speed operation is enabled. (This module detects the transmission rate.) (1) When the host controller function is selected When HSE is 0, the USB port performs low-speed or full-speed operation. If the USB detects that a low-speed peripheral device is attached to the USB port, be sure to set the HSE bit to 0. When HSE is 1, this module executes the reset handshake protocol, and according to the result, the USB port is automatically driven to high-speed or full-speed operation mode. Change this bit after the ATTCH interrupt is detected and before resetting the USB bus (before setting USBRESET to 1). (2) When the function controller function is selected When HSE is 0, this module performs full-speed operation. When HSE is 1, this module executes the reset handshake protocol, and according to the result, this module automatically performs high-speed or full-speed operation. Change this bit while the DPRPU bit is 0.
6	DCFM	0	R/W	Controller Function Select Selects the function of this module. 0: The function controller function is selected. 1: The host controller function is selected. Change this bit while the DPRPU and DRPD bits are 0. During the HNP processing, however, this bit can be set according to the processing sequence.

Bit	Bit Name	Initial Value	R/W	Description
5	DRPD	0	R/W	D+ Line/D- Line Resistance Control Enables or disables pull-down of the D+ and D- lines when the host controller function is selected. 0: Pull-down is disabled. 1: Pull-down is enabled. Set this bit to 1 when the host controller function is selected. During the HNP processing, however, this bit can be set according to the processing sequence. Set this bit to 0 when the function controller function is selected.
4	DPRPU	0	R/W	D+ Line Resistance Control Enables or disables pull-up of the D+ line when the function controller function is selected. 0: Pull-up is disabled. 1: Pull-up is enabled. When this bit is set to 1 with the function controller function selected, this module pulls up the D+ line at 3.3V, and informs the USB host of ATTACH. Clearing this bit to 0 cancels the pull-up of the D+ line, and informs the USB host of DETACH. Set this bit to 1 when the function controller function is selected. During the HNP processing, however, this bit can be set according to the processing sequence. Set this bit to 0 when the host controller function is selected.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
0	USBE	0	R/W	USB Module Operation Enable Enables or disables the USB module operation. 0: The USB module operation is disabled. 1: The USB module operation is enabled. Tables 33.4 and 33.5 list the registers and bit names initialized when this bit is cleared to 0. Change this bit while the SCKE bit is 1. When the host controller function is selected, set the DPRD bit to 1, eliminate chattering with the LNST bit, confirm that the USB bus is stable, and then set this bit to 1.

Table 33.4 Registers Initialized by Writing 0 in the USBE Bit (When the function controller function is selected)

Register Name	Bit Name	Remarks
SYSSTS	LNST	The value is retained when the host controller function is selected.
DVSTCTR	RHST	
INTSTS0	DVSQ	The value is retained when the host controller function is selected.
USBADDR	USBADDR	The value is retained when the host controller function is selected.
USEREQ	BRequest, bmRequestType	The value is retained when the host controller function is selected.
USBVAL	wValue	The value is retained when the host controller function is selected.
USBINDX	wIndex	The value is retained when the host controller function is selected.
USBLENG	wLength	The value is retained when the host controller function is selected.

Table 33.5 Registers Initialized by Writing 0 in the USBE Bit (When the host controller function is selected)

Register Name	Bit Name	Remarks
DVSTCTR	RHST	
FRMNUM	FRNM	The value is retained when the function controller function is selected.
UFRMNUM	UFRNM	The value is retained when the function controller function is selected.

33.3.2 CPU Bus Wait Register (BUSWAIT)

BUSWAIT specifies the number of access waits from the CPU to this module.

This register is writable even if the SCKE bit in SYSCFG is 0.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	BWAIT[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
3 to 0	BWAIT[3:0]	1111	R/W	CPU Bus Wait Specify the number of access waits to this module. 0000: 0 waits (2 access cycles) 0001: 1 wait (3 access cycles) 0010 to 1110: 2 to 14 waits (4 to 16 access cycles) 1111: 15 waits (17 access cycles) initial value The following restriction is provided for access cycles to the registers of addresses beginning with H'04 of this controller. Restriction for wait: The cycle of continuous accesses to the registers of this controller must be 80 ns or more. To satisfy this restriction, control waits using the frequency of system clock HPϕ. Choose the best value within the initial value of 17 clock cycles (maximum). This setting is the same as the waits in accesses to the FIFO port register. The maximum speed of accesses to the FIFO port is as follows: MBW = 10 (32-bit width) : Max. 48 Mbytes/s MBW = 01 (16-bit width) : Max. 24 Mbytes/s MBW = 00 (8-bit width) : Max. 12 Mbytes/s

33.3.3 System Configuration Status Register (SYSSTS)

SYSSTS monitors the USB data bus line status (D+ and D- lines).

This register is initialized by a power-on reset or a USB reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OVCMON[1:0]		—	—	—	—	—	—	—	HTACT	—	—	—	ID MON	LNST[1:0]	
Initial value:	—*	—*	0	0	0	1	0	0	0	0	0	0	0	—*	—*	—*
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15, 14	OVCMON [1:0]	Undefined*	R	OVCN_1/OVCN2_1 Pin Monitor Indicate the input state of the OVCN_1 and OVCN2_1 pins. 00: OVCN_1 = Low, OVCN2_1 = Low 01: OVCN_1 = Low, OVCN2_1 = High 10: OVCN_1 = High, OVCN2_1 = Low 11: OVCN_1 = High, OVCN2_1 = High Connection of an external device to the OVCN_1 and OVCN2_1 pins allows SRP.
13 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
9 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6	HTACT	0	R	Indicates that this module is processing when the host controller function is selected. 0: Idle state 1: Processing
5 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
2	IDMON	Undefined*	R	Indicates the input state of the IDIN_1 pin. 0: IDIN_1 = Low 1: IDIN_1 = High Connection of an external device to the IDIN_1 pin allows a device ID to be reflected in this bit.
1, 0	LNST[1:0]	Undefined*	R	USB Data Line Status Monitor Indicate the USB data bus line (D+ and D- lines) status. Table 33.6 shows the USB data bus line status. Read these bits after the attach processing (DPRPU = 1) when the function controller function is selected or read them after enabling pull-down of the D+ and D- lines (DRPD = 1) when the host controller function is selected.

Note: * These bits depend on the state of the DP_1, DM_1, OVCN_1, OVCN2_1, and IDIN_1 pins.

Table 33.6 USB Data Bus Line Status

LNST[1]	LNST[0]	Low-Speed Operation (only when host controller function is selected)	Full-Speed Operation	High-Speed Operation	Chirp Operation
0	0	SE0	SE0	Squelch	Squelch
0	1	K-State	J-State	UnSquelch	Chirp J
1	0	J-State	K-State	Invalid	Chirp K
1	1	SE1	SE1	Invalid	Invalid

Legend:

Chirp: The reset handshake protocol (RHSP) is being executed with high-speed operation is enabled (HSE = 1 in SYSCFG).
Squelch: SE0 or idle state
UnSquelch: High-speed J-State or high-speed K-State
Chirp J: Chirp J-State
Chirp K: Chirp K-State
Invalid: Invalid

33.3.4 Device State Control Register (DVSTCTR)

DVSTCTR controls and monitors the USB data bus state.

This register is initialized by a power-on reset. The WKUP bit is initialized and the RESUME bit becomes undefined by a USB bus reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	HNP BTOA	EXT LP	PWEN	WKUP	RWU PE	USB RST	RES UME	UACT	—	RHST[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W*	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11	HNPBTOA	0	R/W	Switches HNP (Host Negotiation Protocol) From B (Device) to A (Host). This bit is used to switch the function controller function (device B) to the host controller function (device A) the HNP. 0: Normal operation 1: Switching B to A is enabled. When this bit is 1, the internal function controller remains suspended until the HNP processing finishes even when DPRPU = 0 or DCFM = 1. Furthermore, even if the falling edge of the D+ signal is detected, the resume (RESM) interrupt is not generated. When the HOST ATTACH (pull-up at the other side) is detected or the HNP processing timeout occurs, write 0 in this bit. Write 1 in this bit only in the suspended state with the function controller function selected.
10	EXTLP_1	0	R/W	Controls the EXTLP_1 pin output state. 0: EXTLP_1 Low output 1: EXTLP_1 High output
9	PWEN_1	0	R/W	Controls the PWEN_1 pin output state. 0: PWEN_1 Low output 1: PWEN_1 High output

Bit	Bit Name	Initial Value	R/W	Description
8	WKUP	0	R/W*	Wakeup Output Enables or disables the remote wakeup (resume signal output) to the USB bus when the function controller function is selected. 0: The remote wakeup signal is not output. 1: The remote wakeup signal is output. This module controls the remote wakeup signal output time. When this bit is set to 1, this module outputs 10 ms K-State and then clears this bit. The USB Specification requires the USB bus idle state to be maintained for at least 5 ms before transmitting the remote wakeup signal. For this reason, this module outputs K-State after waiting for 2 ms even if 1 is written in this bit immediately after the suspended state is detected. Write 1 in this bit only when the device is in the suspended state (DVSQ = 1xx in INTSTS0) and remote wakeup is enabled by the USB host. When setting this bit to 1, do not stop the internal clock even in the suspended state (Write 1 in this bit with SCKE set to 1). Write 0 in this bit when the host controller function is selected.
7	RWUPE	0	R/W	Wakeup Detection Enable Enables or disables remote wakeup (resume signal output) for the peripheral device of the down port when the host controller function is selected. 0: Remote wakeup output to the down port is disabled. 1: Remote wakeup output to the down port is enabled. When the remote wakeup signal is detected while this bit is 1, this module detects the resume signal (2.5 μs K-State) for the down port and performs resume processing to drive K-State. When this bit is set to 0, the remote wakeup signal (K-State) from the peripheral device connected to the selected port is ignored even if it is detected by this module. While this bit is 1, do not halt any internal clocks even in the suspended state (keep SCKE = 1). Also do not reset the USB bus from the suspended state by writing 1 in the USBRST bit. This is prohibited by USB Specification 2.0. Set this bit to 0 when the function controller function is selected.

Bit	Bit Name	Initial Value	R/W	Description
6	USBRST	0	R/W	Bus Reset Output Controls the USB bus reset signal output when the host controller function is selected. 0: The USB bus reset signal is not output. 1: The USB bus reset signal is output. When this bit is set to 1 with the host controller function selected, this module drives SE0 of the USB port to perform the USB bus reset processing. When the HSE bit is 1 at this time, this module executes the reset handshake protocol. While USBRST is 1 (until the software writes 0 in this bit), this module continues the SE0 output. Secure the time specified in the USB Specification 2.0 for the USB bus reset time period (USBRST = 1). If 1 is written in this bit during communication (UACT = 1) or during resume (RESUME = 1), this module does not reset the USB bus until the UACT and RESUME bits are cleared to 0. Immediately after this bit is cleared to cancel a USB bus reset, write 1 in the UACT bit. Set this bit to 0 when the function controller function is selected.
5	RESUME	0	R/W	Resume Output Controls the resume signal output when the host controller function is selected. 0: The resume signal is not output. 1: The resume signal is output. When this bit is set to 1, this module drives the port into K-State to output the resume signal. While RESUME is 1 (until the software writes 0 in this bit), this module continues the K-State output. Secure the time specified in the USB Specification 2.0 for the resume time period (RESUME = 1). Write 1 in this bit only in the suspended state. Immediately after this bit is cleared to cancel the resume, write 1 in the UACT bit. Set this bit to 0 when the function controller function is selected.

Bit	Bit Name	Initial Value	R/W	Description
4	UACT	0	R/W	USB Bus Enable Enables or disables the USB bus operation (output control of the SOF or μSOF packet to the USB bus) when the host controller function is selected. 0: Down port operation is disabled. (SOF/μSOF packets are not sent.) 1: Down port operation is enabled. (SOF/μSOF packets are sent.) When this bit is set to 1, this module drives the USB port into the USB bus enable state, sends the SOF packet, and performs data communication. The SOF or μSOF packet is sent within one (micro) frame time period after the software writes 1 in this bit. When this bit is set to 0, this module enters the idle state after the SOF or μSOF packet is sent. This module sets this bit to 0 in the following cases: When the DTCH interrupt is detected during communication (UACT = 1) When the EOFERR interrupt is detected during communication (UACT = 1) Write 1 in this bit at the end of USB reset processing (clearing the USBRST bit) or at the end of resume processing from the suspended state (clearing the RESUME bit). Set this bit to 0 when the function controller function is selected.
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
2 to 0	RHST[2:0]	000	R	Reset Handshake Indicate the reset handshake state. (1) When the host controller function is selected: 000: Transmission rate is undefined (when powered or not connected). 1xx: The reset handshake processing is in progress. 001: Low-speed connection 010: Full-speed connection 011: High-speed connection After the software writes 1 in USBRST, these bits become 100. When HSE is set to 1 for the port, these bits become 111 when this module detects ChirpK from the peripheral device. When the software writes 0 in USBRST of the selected port and this module finishes driving SE0, this module determines the value of the RHST bits. (2) When the function controller function is selected: 000: Transmission rate is undefined. 100: The reset handshake processing is in progress. 010: Full-speed connection 011: High-speed connection When this module detects a USB bus reset with the HSE bit set to 1 for the port, these bits become 100. After that, when this module outputs ChirpK and detects ChirpJK from the USB host three times, these bits become 011. Unless high-speed mode is fixed within 2.5 ms after the ChirpK output, these bits become 010. When this module detects a USB bus reset with the HSE bit set to 0 for the port, these bits become 010. When the RHST bits are fixed to 010 or 011 after this module detected a USB bus reset, the DVST interrupt occurs.

33.3.5 Test Mode Register (TESTMODE)

TESTMODE controls the USB test signal output in high-speed operation mode.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	UTST[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
7 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
3 to 0	UTST[3:0]	0000	R/W	Test Mode Table 33.7 shows the test mode operation of this module. Control the USB test signal output in high-speed operation mode. These bits are valid only in high-speed operation mode. Use this test mode when the RHST bits in DVSTCTR are 011. Since bit 3 (UTST3) of these bits depends on the DCFM bit (controller function select), set these bits according to the DCFM bit. Furthermore, after the test with these bits, cancel this test mode by a power-on reset. When the host controller function is selected: Set these bits after setting DRPD to 1. This module outputs waveforms to the USB port for which DRPD = 1 and UACT = 1 are set. This module also performs high-speed termination for the USB port. Set the UTST bits using the following steps. 1. System reset 2. Clock initiation 3. DCFM = 1, DPRD = 1 (Setting HSE to 1 is not needed.) 4. USBE = 1 5. Set the UTST bits to a value according to the test content. 6. Set the UACT bit to 1.

Bit	Bit Name	Initial Value	R/W	Description
3 to 0	UTST[3:0]	0000	R/W	Change the UTST bits using the following steps. 1. UACT = 0, USBE = 0 2. USBE = 1 3. Set the UTST bits to a value according to the test content. 4. Set the UACT bit to 1. When Test_SE0_NAK (1011) is set, this module does not output the SOF packet to the port for which UACT is set to 1. When Test_Force_Enable (1101) is set, this module outputs the SOF packet to the port for which UACT is set to 1. Furthermore in this test mode, even if this module detects a high-speed disconnection (DTCH interrupt), this module does not control the hardware related to the detection. Before setting the UTST bits, set the PID bit of all pipes to NAK. When performing normal USB communication after setting test mode, issue a system reset. When the function controller function is selected: Set these bits according to the SetFeature request from the USB host during high-speed communication. While these bits are 0001 to 0100, this module does not enter the suspended state.

Table 33.7 Test Mode Operation

	UTST Bits Setting	
Test Mode	**When function controller function is selected**	**When host controller function is selected**
Normal operation	0000	0000
Test_J	0001	1001
Test_K	0010	1010
Test_SE0_NAK	0011	1011
Test_Packet	0100	1100
Test_Force_Enable	—	1101
Reserved	0101 to 0111	1110 to 1111

33.3.6 CFIFO Port Register

CFIFO is a port register to read data from or write data to the FIFO buffer memory.

Each FIFO port consists of this register (CFIFO) for data read/write from/to the FIFO buffer memory, the select registers (CFIFOSEL, D0FIFOSEL, and D1FIFOSEL) to select pipes to be allocated to a FIFO port, and the control registers (CFIFOCTR, D0FIFOCTR, and D1FIFOCTR).

Each FIFO port provides the following features.

- Make accesses to the FIFO buffer for DCP through the CFIFO port.
- Make accesses to the FIFO buffer with DMA transfers through the DMAC module for USB high-speed only.
- When using a function specific to FIFO ports (DMA transfer function, etc.), the pipe number (selected pipe) specified by the CURPIPE bits cannot be changed.
- Register groups of a FIFO port do not affect other FIFO ports.
- Do not allocate the same pipe number to different FIFO ports.
- There are two FIFO buffer states where the access mastership is on the CPU side and on the SIE side. When the FIFO buffer access mastership is on the SIE side, the CPU cannot make an access to the FIFO buffer.

This register is initialized by a power-on reset.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	FIFOPORT[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FIFOPORT[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	FIFOPORT [31:0]	All 0	R/W	FIFO Port Read receive data from the FIFO buffer or write transmit data to the FIFO buffer using these bits. Access to this register is enabled only when the FRDY bit in each control register (CFIFOCTR, D0FIFOCTR, or D1FIFOCTR) is set to 1. Valid bits in this register vary with the value of the MBW bits. Table 33.8 shows the valid bits in this register.

Table 33.8 Operation of This Register when Accessed

Access Size	Bits 31 to 24	Bits 23 to 16	Bits 15 to 8	Bits 7 to 0
32 bits	N + 3 address	N + 2 address	N + 1 address	N + 0 address
16 bits	Write: Invalid, Read: Prohibited*		N + 1 address	N + 0 address
8 bits	Write: Invalid, Read: Prohibited*			N + 0 address

Note: * Reading an invalid register with word access or byte access is prohibited.

33.3.7 FIFO Port Select Registers (CFIFOSEL, D0FIFOSEL, D1FIFOSEL)

CFIFOSEL, D0FIFOSEL, and D1FIFOSEL select pipes to be allocated to FIFO ports and control accesses to each FIFO port.

Do not specify the same pipe number for the CURPIPE bits in CFIFOSEL, D0FIFOSEL, and D1FIFOSEL. When the CURPIPE bits in D0FIFOSEL and D1FIFOSEL are set to B'000, no pipe is specified.

Do not change any pipe number when DMA transfer is enabled.

This register is initialized by a power-on reset.

(1) CFIFOSEL

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RCNT	REW	—	—	MBW[1:0]		—	—	—	—	ISEL	—	CURPIPE[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R	R/W	R/W	R	R	R	R	R/W	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	RCNT	0	R/W	Read Count Mode Specifies read mode of the DTLN bits in CFIFOCTR. 0: Clears the DTLN bits after reading all receive data in the CFIFO (or after reading receive data of one side of the double buffer). 1: Counts down the DTLN bits at each reading of CFIFO receive data.
14	REW	0	R/W	Buffer Pointer Rewind Specifies whether to rewind the buffer pointer or not. 0: The buffer pointer is not rewound. 1: The buffer pointer is rewound. When the selected pipe is in the receive direction and this bit is set to 1 during FIFO buffer reading, the FIFO buffer can be read from the first data. (In the case of a double buffer, the first data of one side that is being read can be read again.) Do not set this bit to 1 concurrently with the CURPIPE setting change. Be sure to confirm that the FRDY bit is 1 when setting this bit to 1. To rewrite the FIFO buffer data from the first data for a pipe in the transmit direction, use the BCLR bit.
13, 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
11, 10	MBW[1:0]	00	R/W	CFIFO Port Access Bit Width Specify the bit width for accesses to the CFIFO port. 00: 8 bits 01: 16 bits 10: 32 bits 11: Setting prohibited When the selected pipe is in the receive direction and data read is started after these bits are set, do not change these bits until all data is completely read. When the selected pipe is in the receive direction, set the CURPIPE and MBW bits at the same time. When the selected pipe is in the transmit direction, no bit width can be changed (from 8 bits to 16/32 bits or from 16 bits to 32 bits) during data write to the buffer memory. When 8-bit width or 16-bit width is selected, data of odd bytes can also be written by controlling the byte access.
9 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	ISEL	0	R/W	CFIFO Port Access Direction when DCP is Selected 0: Buffer memory read is selected. 1: Buffer memory write is selected. To change this bit when the selected pipe is DCP, write 1 or 0 in this bit, read the value of this bit, confirm that the write value equals the read value, and then proceed with the next processing. If this bit is changed in the middle of access to the FIFO buffer, accesses made before that time are retained, the value of this bit is rewritten, and then further access is enabled. Set this bit concurrently with the CURPIPE bits.

Bit	Bit Name	Initial Value	R/W	Description
4	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
3 to 0	CURPIPE [3:0]	0000	R/W	CFIFO Port Access Pipe Select Set the number of pipe to be used for data read or write through the CFIFO port. 0000: DCP 0001: Pipe 1 0010: Pipe 2 0011: Pipe 3 0100: Pipe 4 0101: Pipe 5 0110: Pipe 6 0111: Pipe 7 1000: Pipe 8 1001: Pipe 9 1010: Pipe A*2 1011: Pipe B*2 1100: Pipe C*2 1101: Pipe D*2 1110: Pipe E*2 1111: Pipe F*2 To change these bits, write a value in these bits, read the value of these bits, confirm that the write value equals the read value, and then proceed with the next processing. Do not write the same pipe number in the CURPIPE bits in CFIFOSEL, D0FIFOSEL, and D1FIFOSEL. If these bits are changed in the middle of access to the FIFO buffer, accesses made before that time are retained, the value of these bits is rewritten, and then further access is enabled.

Note: * Only reading 0 is enabled.
*2 Pipe A to Pipe F are effective only when the function controller function is selected.

(2) D0FIFOSEL, D1FIFOSEL

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RCNT	REW	DCLRM	DREQE	MBW[1:0]		—	—	DEZPM	—	—	—	CURPIPE[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W*	R/W	R/W	R/W	R/W	R	R	R/W	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	RCNT	0	R/W	Read Count Mode Specifies read mode of the DTLN bits in DnFIFOCTR. 0: Clears the DTLN bits after reading all receive data in the DnFIFO (or after reading receive data of one side of the double buffer). 1: Counts down the DTLN bits at each reading of DnFIFO receive data. When making an access to the DnFIFO with the BFRE bit set to 1, set this bit to 0.
14	REW	0	R/W*	Buffer Pointer Rewind Specifies whether to rewind the buffer pointer or not. 0: The buffer pointer is not rewound. 1: The buffer pointer is rewound. When the selected pipe is in the receive direction and this bit is set to 1 during FIFO buffer reading, the FIFO buffer can be read from the first data. (In the case of a double buffer, the first data of one side that is being read can be read again.) Do not set this bit to 1 concurrently with the CURPIPE setting change. Be sure to confirm that the FRDY bit is 1 when setting this bit to 1. When making an access to the DnFIFO with the BFRE bit set to 1, do not set this bit to 1 when the short packet data is completely read. To rewrite the FIFO buffer data from the first data for a pipe in the transmit direction, use the BCLR bit.

Bit	Bit Name	Initial Value	R/W	Description
13	DCLRM	0	R/W	Buffer Memory Auto-Clear Mode after Reading Data of Selected Pipe Enables or disables buffer memory auto-clear mode after reading data of the selected pipe. 0: Buffer memory auto-clear mode is disabled. 1: Buffer memory auto-clear mode is enabled. When this bit is 1 and a Zero-Length packet is received while the FIFO buffer allocated to the selected pipe is empty or when a short packet is received with the BFRE bit set to 1 and the packet data is completely read, this module performs buffer clear (BCLR = 1 processing) of the FIFO buffer. When using this module with the BRDYM bit set to 1, be sure to set this bit to 0.
12	DREQE	0	R/W	DMA Transfer Request Enable Enables or disables making a DMA transfer request. 0: DMA transfer request is disabled. 1: DMA transfer request is enabled. To enable a DMA transfer request, set the CURPIPE bits and then set this bit to 1. Set this bit to 0 before changing the CURPIPE setting.
11, 10	MBW[1:0]	00	R/W	FIFO Port Access Bit Width Specify the bit width for accesses to the DnFIFO port. 00: 8 bits 01: 16 bits 10: 32 bits 11: Setting prohibited When the selected pipe is in the receive direction and data read is started after these bits are set, do not change these bits until all data is completely read. When the selected pipe is in the receive direction, set the CURPIPE and MBW bits at the same time. When the selected pipe is in the transmit direction, no bit width can be changed (from 8 bits to 16/32 bits or from 16 bits to 32 bits) during data write to the buffer memory. When 8-bit width or 16-bit width is selected, data of odd bytes can also be written by controlling the byte access.

Bit	Bit Name	Initial Value	R/W	Description
9 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	DEZPM	0	R/W	DEZPM: Zero-Length Packet Addition Mode If the DMA transfer size that is set for the the USBHS-DMAC modules is an integral multiple of the maximum packet size, a null packet is added after all of the data has been sent. 0: Disables addition of packets. 1: Enables addition of packets. This bit is applied to pipes used to write to the FIFO buffer. DEZPM must be set before starting DMA transfers. If the DEZPM bit is set after DMA transfers complete, no null packets are added. Note : This mode depends on the buffer size(PIPEBUF.BUFSIZE[4:0]). A null packet is added after transferring data up to buffer size which is defined by PIPEBUF.BUFSIZE[4:0]. When transfer data size is over 2Kbytes, this mode must not be used because max size of buffer is 2Kbytes. In that case, please add the null packet by SW with BVAL bit of FIFO Port Control Registers.
6 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
3 to 0	CURPIPE [3:0]	0000	R/W	FIFO Port Access Pipe Select Set the number of pipe to be used for data read or write through the D0FIFO and D1FIFO ports. 0000: No pipe 0001: Pipe 1 0010: Pipe 2 0011: Pipe 3 0100: Pipe 4 0101: Pipe 5 0110: Pipe 6 0111: Pipe 7 1000: Pipe 8 1001: Pipe 9 1010: Pipe A*2 1011: Pipe B*2 1100: Pipe C*2 1101: Pipe D*2 1110: Pipe E*2 1111: Pipe F*2 To change these bits, write a value in these bits, read the value of these bits, confirm that the write value equals the read value, and then proceed with the next processing. Do not write the same pipe number in the CURPIPE bits in CFIFOSEL, D0FIFOSEL, and D1FIFOSEL. If these bits are changed in the middle of access to the FIFO buffer, accesses made before that time are retained, the value of these bits is rewritten, and then further access is enabled.

Note: * Only reading 0 is enabled.
*2 Pipe A to Pipe F are effective only when the function controller function is selected.

33.3.8 FIFO Port Control Registers (CFIFOCTR, D0FIFOCTR, D1FIFOCTR)

CFIFOCTR, D0FIFOCTR, and D1FIFOCTR specify buffer memory write end and CPU buffer clear, as well as indicate whether the FIFO port is accessible or not. These registers correspond to each FIFO port.

These registers are initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BVAL	BCLR	FRDY	—	DTLN[11:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W*1	R/W*2	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	BVAL	0	R/W*1	Buffer Memory Enable Flag This flag is set to 1 upon completion of data write in the FIFO buffer of the CPU of the pipe selected by the CURPIPE bits. 0: Invalid 1: Write end When the selected pipe is in the transmit direction, set this bit to 1 in the following cases. This module sets the FIFO buffer of the CPU to the SIE side to enable data transmission. To send a short packet, set this bit to 1 upon completion of data write. To send a Zero-Length packet, set this bit to 1 before writing data to the FIFO buffer. For pipes of continuous transfer mode, set this bit to 1 after writing data that is a positive integer multiple of MaxPacketSize and less than the BufferSize value. When data with the size specified by MaxPacketSize is written to a pipe of continuous transfer mode, this module writes 1 in this bit and sets the FIFO buffer of the CPU to the SIE side to enable data transmission. Set this bit to 1 when this module shows FRDY = 1. When the selected pipe is in the receive direction, do not set this bit to 1.

Bit	Bit Name	Initial Value	R/W	Description
14	BCLR	0	R/W*2	CPU buffer clear Clears the CPU side FIFO buffer of the selected pipe. 0: Invalid 1: Clears the CPU side FIFO buffer. When the FIFO buffer assigned to the selected pipe is set to a double buffer, and even when both sides of the buffer are readable, this module clears only one side of the FIFO buffer. When the selected pipe is DCP, this module clears the FIFO buffer when this bit is set to 1 irrespective of whether the FIFO buffer is on the CPU side or SIE side. When clearing the SIE side FIFO buffer, be sure to set the PID bits in DCP to NAK and then set the BCLR bit to 1. When the selected pipe is in the transmit direction, and if 1 is written in the BVAL and BCLR bits at the same time, this module clears the previously written data, and makes a Zero-Length packet transmittable. When the selected pipe is not DCP, write 1 in this bit while the FRDY flag indicates 1.
13	FRDY	0	R	FIFO Port Ready Indicates whether the CPU (DMAC) can access the FIFO port. 0: The FIFO port is not accessible. 1: The FIFO port is accessible. This module indicates FRDY = 1 in the following cases. However, since there is no data to read, no data can be read from the FIFO port. In these cases, set the BCLR bit to 1 to clear the FIFO buffer to make transmission/reception of the next data available. When a Zero-Length packet is received with the FIFO buffer assigned to the selected pipe empty When a short packet is received with BFRE set to 1 and the packet data is completely read
12	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
11 to 0	DTLN[11:0]	H'000	R	Receive Data Length Indicate the receive data length. The value of these bits during FIFO buffer reading varies as follows depending on the setting of the RCNT bit. When RCNT = 0: This module indicates the reecive data length with these bits until the CPU (DMAC) finishes reading one side of the FIFO buffer. When BFRE is 1, this module retains the reecive data length until the BCLR bit is set to 1 after the FIFO buffer read is completed. When RCNT = 1: This module decrements the value of the DTLN bits in each read cycle (-1 when MBW = 0, and -2 when MBW = 1) When reading out from a single FIFO buffer is complete, DTLN = 0 for this module. However, the behavior is different when double-buffering has been specified. If reading out of data from one side is not finished before the other side is full of received data, when all data have been read out from the first side, the DTLN bits reflect the amount of data received in the other side. When reading these bits during FIFO buffer reading while the RCNT bit is 1, note that this module updates the value in these bits within 150 ns after each FIFO port read cycle.

Notes: 1. Only writing 1 is enabled.
2. Only reading 0 and writing 1 are enabled.

33.3.9 Interrupt Enable Register 0 (INTENB0)

INTENB0 specifies masking of each interrupt when selection for function controller. When this module detects an interrupt for which 1 is written in the corresponding bit in this register by the software, this module generates a USB interrupt.

When interrupt source detection conditions are satisfied irrespective of the register setting (interrupt enable/disable), this module sets the corresponding status bit in INTSTS0 to 1.

When the software changes an interrupt enable bit (0 to 1) whose interrupt source status bit in INTSTS0 is set to 1, this module generates a USB interrupt. Only when the function controller is selected, the interrupt permission by INTENB0 register can be set. Please do not permit when you select the host controller.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VBSE	RSME	SOFE	DVSE	CTRE	BEMPE	NRDYE	BRDYE	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	VBSE	0	R/W	VBUS0_1 and VBUS1_1 Interrupt Enable Enables or disables USB interrupt outputs when the VBINT interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
14	RSME	0	R/W	Resume Interrupt Enable Enables or disables USB interrupt outputs when the RESM interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
13	SOFE	0	R/W	Frame Number Update Interrupt Enable Enables or disables USB interrupt outputs when the SOFR interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

Bit	Bit Name	Initial Value	R/W	Description
12	DVSE	0	R/W	Device State Transition Interrupt Enable* Enables or disables USB interrupt outputs when the DVST interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
11	CTRE	0	R/W	Control Transfer Stage Transition Interrupt Enable* Enables or disables USB interrupt outputs when the CTRT interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
10	BEMPE	0	R/W	Buffer Empty Interrupt Enable Enables or disables USB interrupt outputs when the BEMP interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
9	NRDYE	0	R/W	Buffer Not Ready Response Interrupt Enable Enables or disables USB interrupt outputs when the NRDY interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
8	BRDYE	0	R/W	Buffer Ready Interrupt Enable Enables or disables USB interrupt outputs when the BRDY interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Note: * The RSME, DVSE, and CTRE bits can be set to 1 only when the function controller function is selected. Do not enable interrupts of these bits when the host controller function is selected.

33.3.10 Interrupt Enable Register 1 (INTENB1)

INTENB1 specifies masking of each interrupt when the host controller function is selected. When this module detects an interrupt for which 1 is written in the corresponding bit in this register by the software, this module generates a USB interrupt.

When interrupt source detection conditions are satisfied irrespective of the register setting (interrupt enable/disable), this module sets the corresponding status bit in INTSTS1 to 1.

When the software changes an interrupt enable bit (0 to 1) whose interrupt source status bit in INTSTS1 is set to 1, this module outputs a USB interrupt.

When the function controller function is selected, do not allow any interrupt.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OVRCRE	BCHGE	—	DTCHE	ATTCHE	—	—	—	—	EOFERRE	SIGNE	SACKE	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	OVRCRE	0	R/W	OVRCR Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
14	BCHGE	0	R/W	USB Bus Change Interrupt Enable Enables or disables USB interrupt outputs when the BCHG interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
13	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
12	DTCHE	0	R/W	Disconnection Detect Interrupt Enable Enables or disables USB interrupt outputs when the DTCH interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

Bit	Bit Name	Initial Value	R/W	Description
11	ATTCHE	0	R/W	Connection Detect Interrupt Enable Enables or disables USB interrupt outputs when the ATTCH interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
10 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6	EOFERRE	0	R/W	EOF Error Detect Interrupt Enable Enables or disables USB interrupt outputs when the EOFERR interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
5	SIGNE	0	R/W	Setup Transaction Error Interrupt Enable Enables or disables USB interrupt outputs when the SIGN interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
4	SACKE	0	R/W	Setup Transaction ACK Interrupt Enable Enables or disables USB interrupt outputs when the SACK interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

33.3.11 BRDY Interrupt Enable Register (BRDYENB)

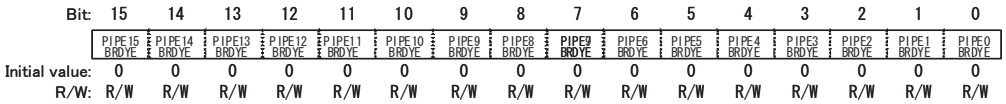
BRDYENB enables or disables the BRDY bit to be set to 1 when the BRDY interrupt of a pipe is detected.

When this module detects the BRDY interrupt of a pipe for which the software sets the corresponding bit in this register to 1, this module sets the PIPEBRDY bit of the pipe in BRDYSTS and also sets the BRDY bit in INTSTS0 to 1 and generates the BRDY interrupt.

When one or more PIPEBRDY bits in BRDYSTS are 1 and the software changes the corresponding interrupt enable bit(s) in this register from 0 to 1, this module generates the BRDY interrupt.

This register is initialized by a power-on reset.

Pipe A to Pipe F are effective only when the function controller function is selected.



Bit	Bit Name	Initial Value	R/W	Description
15	PIPEF BRDYE	0	R/W	Pipe F BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
14	PIPEE BRDYE	0	R/W	Pipe E BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
13	PIPED BRDYE	0	R/W	Pipe D BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
12	PIPEC BRDYE	0	R/W	Pipe C BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
11	PIPEB BRDYE	0	R/W	Pipe B BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

Bit	Bit Name	Initial Value	R/W	Description
10	PIPEA BRDYE	0	R/W	Pipe A BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
9	PIPE9 BRDYE	0	R/W	Pipe 9 BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
8	PIPE8 BRDYE	0	R/W	Pipe 8 BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
7	PIPE7 BRDYE	0	R/W	Pipe 7 BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
6	PIPE6 BRDYE	0	R/W	Pipe 6 BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
5	PIPE5 BRDYE	0	R/W	Pipe 5 BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
4	PIPE4 BRDYE	0	R/W	Pipe 4 BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
3	PIPE3 BRDYE	0	R/W	Pipe 3 BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
2	PIPE2 BRDYE	0	R/W	Pipe 2 BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
1	PIPE1 BRDYE	0	R/W	Pipe 1 BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

Bit	Bit Name	Initial Value	R/W	Description
0	PIPE0 BRDYE	0	R/W	Pipe 0 BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

33.3.12 NRDY Interrupt Enable Register (NRDYENB)

NRDYENB enables or disables the NRDY bit to be set to 1 when the NRDY interrupt of a pipe is detected.

When this module detects the NRDY interrupt of a pipe for which the software sets the corresponding bit in this register to 1, this module sets the PIPENRDY bit of the pipe in NRDYSTS and also sets the NRDY bit in INTSTS0 to 1 and generates an NRDY interrupt.

When one or more PIPENRDY bits in NRDYSTS are 1 and the software changes the corresponding interrupt enable bit(s) in this register from 0 to 1, this module generates an NRDY interrupt.

This register is initialized by a power-on reset.

Pipe A to Pipe F are effective only when the function controller function is selected.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PIPE15 NRDYE	PIPE14 NRDYE	PIPE13 NRDYE	PIPE12 NRDYE	PIPE11 NRDYE	PIPE10 NRDYE	PIPE9 NRDYE	PIPE8 NRDYE	PIPE9 NRDYE	PIPE6 NRDYE	PIPE5 NRDYE	PIPE4 NRDYE	PIPE3 NRDYE	PIPE2 NRDYE	PIPE1 NRDYE	PIPE0 NRDYE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	PIPEF NRDYE	0	R/W	Pipe F NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
14	PIPEE NRDYE	0	R/W	Pipe E NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
13	PIPED NRDYE	0	R/W	Pipe D NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
12	PIPEC NRDYE	0	R/W	Pipe C NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
11	PIPEB NRDYE	0	R/W	Pipe B NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

Bit	Bit Name	Initial Value	R/W	Description
10	PIPEA NRDYE	0	R/W	Pipe A NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
9	PIPE9 NRDYE	0	R/W	Pipe 9 NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
8	PIPE8 NRDYE	0	R/W	Pipe 8 NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
7	PIPE7 NRDYE	0	R/W	Pipe 7 NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
6	PIPE6 NRDYE	0	R/W	Pipe 6 NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
5	PIPE5 NRDYE	0	R/W	Pipe 5 NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
4	PIPE4 NRDYE	0	R/W	Pipe 4 NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
3	PIPE3 NRDYE	0	R/W	Pipe 3 NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
2	PIPE2 NRDYE	0	R/W	Pipe 2 NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
1	PIPE1 NRDYE	0	R/W	Pipe 1 NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

Bit	Bit Name	Initial Value	R/W	Description
0	PIPE0 NRDYE	0	R/W	Pipe 0 NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

33.3.13 BEMP Interrupt Enable Register (BEMPENB)

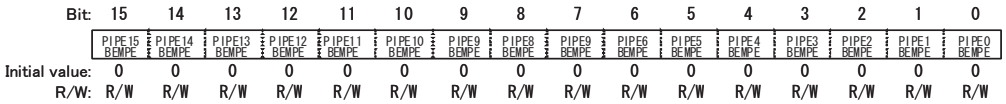
BEMPENB enables or disables the BEMP bit to be set to 1 when the BEMP interrupt of a pipe is detected.

When this module detects the BEMP interrupt of a pipe for which the software sets the corresponding bit in this register to 1, this module sets the PIPEBEMP bit of the pipe in BEMPSTS and the BEMP bit in INTSTS0 to 1 and generates the BEMP interrupt.

When one or more PIPEBEMP bits in BEMPSTS are 1 and the software changes the corresponding interrupt enable bit(s) in this register from 0 to 1, this module generates the BEMP interrupt.

This register is initialized by a power-on reset.

Pipe A to Pipe F are effective only when the function controller function is selected.



Bit	Bit Name	Initial Value	R/W	Description
15	PIPEF BEMPE	0	R/W	Pipe F BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
14	PIPEE BEMPE	0	R/W	Pipe E BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
13	PIPED BEMPE	0	R/W	Pipe D BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
12	PIPEC BEMPE	0	R/W	Pipe C BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
11	PIPEB BEMPE	0	R/W	Pipe B BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

Bit	Bit Name	Initial Value	R/W	Description
10	PIPEA BEMPE	0	R/W	Pipe A BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
9	PIPE9 BEMPE	0	R/W	Pipe 9 BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
8	PIPE8 BEMPE	0	R/W	Pipe 8 BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
7	PIPE7 BEMPE	0	R/W	Pipe 7 BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
6	PIPE6 BEMPE	0	R/W	Pipe 6 BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
5	PIPE5 BEMPE	0	R/W	Pipe 5 BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
4	PIPE4 BEMPE	0	R/W	Pipe 4 BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
3	PIPE3 BEMPE	0	R/W	Pipe 3 BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
2	PIPE2 BEMPE	0	R/W	Pipe 2 BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
1	PIPE1 BEMPE	0	R/W	Pipe 1 BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

Bit	Bit Name	Initial Value	R/W	Description
0	PIPE0 BEMPE	0	R/W	Pipe 0 BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

33.3.14 SOF Output Configuration Register (SOFCFG)

SOFCFG specifies an effective period of transactions, the BRDY interrupt status clear timing, and others.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	TRNENSEL	—	BRDYM	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R/W	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	TRNENSEL	0	R/W	Transaction Effective Period Switching Specifies a transaction effective period where this module sends a token in one frame in a port in full-speed or low-speed communication. 0: Low-speed is not supported. 1: Low-speed is supported. This bit is valid only when the host controller function is selected. This bit does not affect the high-speed transaction effective period even when the host controller function is selected. Set this bit to 0 when the function controller function is selected.
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6	BRDYM	0	R/W	Status Clear Timing of Each Pipe BRDY Interrupt Specifies the timing to clear the BRDY interrupt status of each pipe. 0: The software clears the status. 1: This module clears the status by reading or writing the FIFO buffer.

Bit	Bit Name	Initial Value	R/W	Description
5	—	0	R	Reserved This bit is reserved. Write the value that was read immediately before. Note: The initial value of this bit is 0 immediately after a power-on reset. Be sure to set this bit to 1 during the initialization routine of this module.
4 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

33.3.15 Interrupt Status Register 0 (INTSTS0)

INTSTS0 can know the interrupt generation by referring to the register when the function controller is selected.

Please permit interrupt by the status change that each bit of this register shows only when you select the function.

This register is initialized by a power-on reset. The DVSQ2 to DVSQ0 bits are also initialized by a USB bus reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VBINT	RESM	SOFR	DVST	CTRT	BEMP	NRDY	BRDY	VBSTS	DVSQ[2:0]			VALID	CTSQ[2:0]		
Initial value:	0	0	0	*1	0	0	0	0	*3	*2	*2	*2	0	0	0	0
R/W:	R/W*7	R/W*7	R/W*7	R/W*7	R/W*7	R	R	R	R	R	R	R	R/W*7	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	VBINT	0	R/W*7	VBUS0_1 and VBUS1_1 Interrupt Status*4*5 0: No VBUS0_1 and VBUS1_1 interrupt is generated. 1: A VBUS0_1 and VBUS1_1 interrupt is generated. This bit indicates 1 when this module detects a change in the VBUS0_1 and VBUS1_1 pin input level (high to low or low to high level). This module indicates the VBUS0_1 and VBUS1_1 pin input value using the VBSTS bit. When a VBINT interrupt occurs, read the VBSTS bit several times by the software and confirm that the read value is equal each time to eliminate chattering.
14	RESM	0	R/W*7	Resume Interrupt Status*4*5*6 0: No resume interrupt is generated. 1: A resume interrupt is generated. This bit indicates 1 when this module detects a falling of the DP pin level in the suspended state (DVSQ = 1XX) with the function controller function selected. The read value is invalid when the host controller function is selected.

Bit	Bit Name	Initial Value	R/W	Description
13	SOFR	0	R/W*7	Frame Number Update Interrupt Status*4 0: No SOF interrupt is generated. 1: An SOF interrupt is generated. (1) When the host controller function is selected When the UACT bit is set to 1 by the software, this bit is set to 1 at the frame number update timing. (This interrupt is detected every millisecond.) (2) When the function controller function is selected This module indicates SOFR = 1 at the frame number update timing. (This interrupt is detected every millisecond.) Even when an SOF packet from the USB host is corrupted, this module detects an SOFR interrupt using the internal interpolation.
12	DVST	0/1*1	R/W*7	Device State Transition Interrupt Status*4*6 0: No device state transition interrupt is generated. 1: A device state transition interrupt is generated. When this module detects a change in device state with the function controller function selected, this module updates the DVSQ value and set this bit to 1. When this interrupt occurred, clear the status before this module detects the next device state transition. The read value is invalid when the host controller function is selected.
11	CTRT	0	R/W*7	Control Transfer Stage Transition Interrupt Status*4*6 0: No control transfer stage transition interrupt is generated. 1: A control transfer stage transition interrupt is generated. When this module detects a control transfer stage transition with the function controller function selected, this module updates the CTSQ value and set this bit to 1. When this interrupt occurred, clear the status before this module detects the next stage transition in control transfers. The read value is invalid when the host controller function is selected.

Bit	Bit Name	Initial Value	R/W	Description
10	BEMP	0	R	Buffer Empty Interrupt Status 0: No BEMP interrupt is generated. 1: A BEMP interrupt is generated. This module indicates BEMP = 1 when at least one of the PIPEBEMP bits in BEMPSTS corresponding to the pipes for which 1 is set in the PIPEBEMPE bits in BEMPENB is set to 1 (when this module detects a BEMP interrupt of one or more pipes for which BEMP interrupts are enabled by the software). For PIPEBEMP status assertion conditions, see section 33.4.2 (3), BEMP Interrupt. When the software writes 0 to all PIPEBEMP bits corresponding to the pipes for which interrupts are enabled by the PIPEBEMPE bits, this module clears this bit to 0. This bit cannot be cleared to 0 by writing 0 by the software.
9	NRDY	0	R	Buffer Not Ready Interrupt Status 0: No NRDY interrupt is generated. 1: An NRDY interrupt is generated. This module indicates NRDY = 1 when at least one of the PIPENRDY bits in NRDYSTS corresponding to the pipes for which 1 is set in the PIPENRDYE bits in NRDYENB is set to 1 (when this module detects an NRDY interrupt of one or more pipes for which NRDY interrupts are enabled by the software). For PIPENRDY status assertion conditions, see section 33.4.2 (2), NRDY Interrupt. When the software writes 0 to all PIPENRDY bits corresponding to the pipes for which interrupts are enabled by the PIPENRDYE bits, this module clears this bit to 0. This bit cannot be cleared to 0 by writing 0 by the software.

Bit	Bit Name	Initial Value	R/W	Description
8	BRDY	0	R	Buffer Ready Interrupt Status Indicates the BRDY interrupt status. 0: No BRDY interrupt is generated. 1: A BRDY interrupt is generated. This module indicates BRDY = 1 when at least one of the PIPEBRDY bits in BRDYSTS corresponding to the pipes for which 1 is set in the PIPEBRDYE bits in BRDYENB is set to 1 (when this module detects a BRDY interrupt of one or more pipes for which BRDY interrupts are enabled by the software). For PIPEBRDY status assertion conditions, see section 33.4.2 (1), BRDY Interrupt. When the software writes 0 to all PIPEBRDY bits corresponding to the pipes for which interrupts are enabled by the PIPEBRDYE bits, this module clears this bit to 0. This bit cannot be cleared to 0 by writing 0 by the software.
7	VBSTS	0/1*[3]	R	VBUS0_1 and VBUS1_1 Input Status 0: The VBUS0_1 and VBUS1_1 pin is low level. 1: The VBUS0_1 and VBUS1_1 pin is high level.
6 to 4	DVSQ[2:0]	000/001*[2]	R	Device State 000: Powered state 001: Default state 010: Address state 011: Configuration state 1xx: Suspended state The read value is invalid when the host controller function is selected.
3	VALID	0	R/W*[7]	USB Request Receive 0: Not detected 1: A setup packet is received. The read value is invalid when the host controller function is selected.

Bit	Bit Name	Initial Value	R/W	Description
2 to 0	CTSQ[2:0]	000	R	Control Transfer Stage 000: Idle stage or setup stage 001: Control read data stage 010: Control read status stage 011: Control write data stage 100: Control write status stage 101: Control write (NoData) status stage 110: Control transfer sequence error 111: Setting prohibited The read value is invalid when the host controller function is selected.

Notes:
1. The initial value is B'0 after a power-on reset, and B'1 after a USB bus reset.
2. The initial value is B'000 after a power-on reset, and B'001 after a USB bus reset.
3. The initial value is 1 when the VBUS0_1 and VBUS1_1 pin is high level, and is 0 when the VBUS0_1 and VBUS1_1 pin is low level.
4. To clear the VBINT, RESM, SOFR, DVST, or CTRT bit, write 0 only to bits to be cleared and write 1 to the other bits. Do not write 0 to status bits that indicate 0.
5. When a status change shown in the VBINT or RESM bit is detected while the clock is halted (SCKE = 0) and the corresponding interrupt is enabled, the interrupt is output. Clear the interrupt status of these bits by the software after the clock is enabled.
6. A status change of the RESM, DVST, or CTRT bit occurs only when the function controller function is selected. When the function controller function is selected, disable the corresponding interrupt enable bits to 0 (disabled).
7. Only writing 0 is enabled.

33.3.16 Interrupt Status Register 1 (INTSTS1)

INTSTS1 can know the interrupt generation by referring to the register when the host controller is selected.

By using INTSTS0 when the function controller function is selected or INTSTS1 when the host controller function is selected, occurrence of interrupts can be monitored with either of these registers.

Enable interrupts generated due to a status change shown by each bit in this register only when the host controller function is selected.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OVRCR	BCHG	—	DTCH	ATTCH	—	—	—	—	EOFERR	SIGN	SACK	—	—	—	—
Initial value:	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W*1	R	R/W*1	R/W*1	R	R	R	R	R/W*1	R/W*1	R/W*1	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	OVRCR	Undefined	R/W	OVRCR Interrupt Status This interrupt is generated when the OVCN_1 or OVCN2_1 pin input status changes. 0: No OVRCR interrupt is generated. 1: An OVRCR interrupt is generated.

Bit	Bit Name	Initial Value	R/W	Description
14	BCHG	0	R/W*[1]	USB Bus Change Interrupt Status Indicates the USB bus change interrupt status. 0: No BCHG interrupt is generated. 1: A BCHG interrupt is generated. When a full-speed or low-speed signal level change occurs in the USB port (from J-State, K-State, or SE0 to J-State, K-State, or SE0), this module detects a BCHG interrupt and indicates BCHG = 1. At this time, when the corresponding interrupt enable bit is set to 1 by the software, this module generates an interrupt. The current input state of the USB port is indicated by the LNST bits in SYSSTS. When a BCHG interrupt occurs, read the LNST bits several times by the software and confirm that the read value is equal each time to eliminate chattering. A USB bus change can also be detected while the internal clock is halted. The read value is invalid when the function controller function is selected.
13	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
12	DTCH	0	R/W*[1]	USB Disconnection Detect Interrupt Status Indicates the USB disconnection detect interrupt status when the host controller function is selected. 0: No DTCH interrupt is generated. 1: A DTCH interrupt is generated. When a USB bus disconnection is detected, this module detects a DTCH interrupt and indicates DTCH = 1. At this time, when the corresponding interrupt enable bit is set to 1 by the software, this module generates an interrupt. This module detects a USB bus disconnection based on the USB 2.0 Specification. After detecting a DTCH interrupt, this module performs the following hardware control irrespective of the setting of the corresponding interrupt enable bit. The software must terminate communication of all pipes with the USB port and drives this module into a state of waiting for ATTACH to the USB port (an ATTCH interrupt is generated). Clears the UACT bit of the port in which a DTCH interrupt is detected to 0 and indicates the UACT bit. Drives the port in which a DTCH interrupt is detected into the idle state. The read value is invalid when the function controller function is selected.

Bit	Bit Name	Initial Value	R/W	Description
11	ATTCH	0	R/W*[1]	ATTCH Interrupt Status Indicates the ATTCH interrupt status when the host controller function is selected. 0: No ATTCH interrupt is generated. 1: An ATTCH interrupt is generated. When this module detects J-State or K-State of full-speed or low-speed signal level for 2.5 μs in the USB port, this module detects an ATTCH interrupt and indicates ATTCH = 1. At this time, when the corresponding interrupt enable bit is set to 1 by the software, this module generates an interrupt. Conditions for this module to detect an ATTCH interrupt are as follows: When K-State, SE0 or SE1 changes to J-State and then J-State continues for 2.5 μs When J-State, SE0 or SE1 changes to K-State and then K-State continues for 2.5 μs The read value is invalid when the function controller function is selected.
10 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
6	EOFERR	0	R/W*[1]	EOF Error Detect Interrupt Status Indicates the EOFERR interrupt status when the host controller function is selected. 0: No EOFERR interrupt is generated. 1: An EOFERR interrupt is generated. When this module detects that communication is not completed at the EOF2 timing specified in the USB 2.0 Specification, this module detects an EOFERR interrupt and indicates EOFERR = 1. At this time, when the corresponding interrupt enable bit is set to 1 by the software, this module generates an EOFERR interrupt. After detecting an EOFERR interrupt, this module performs the following hardware control irrespective of the setting of the corresponding interrupt enable bit. The software must terminate communication of all pipes with the USB port and perform reenumeration for the USB port. Clears the UACT bit of the port in which an EOFERR interrupt is detected to 0 and indicates the UACT bit. Drives the port in which an EOFERR interrupt is detected into the idle state. The read value is invalid when the function controller function is selected.

Bit	Bit Name	Initial Value	R/W	Description
5	SIGN	0	R/W*[1]	Setup Transaction Error Interrupt Status Indicates the setup transaction error interrupt status when the host controller function is selected. 0: No SIGN interrupt is generated. 1: A SIGN interrupt is generated. When a peripheral device does not send an ACK response three times in a row in the SETUP transaction issued by this module, this module detects a SIGN interrupt and indicates SIGN = 1. At this time, when the corresponding interrupt enable bit is set to 1 by the software, this module generates a SIGN interrupt. This module detects a SIGN interrupt when any of the following response is generated to SETUP transactions (three times in a row). When the peripheral device sends no response and therefore this module detects a timeout When the ACK packet is corrupted When a handshake signal (NAK, NYET, or STALL) other than ACK is received The read value is invalid when the function controller function is selected.

Bit	Bit Name	Initial Value	R/W	Description
4	SACK	0	R/W*[1]	Setup Transaction ACK Response Interrupt Status Indicates the setup transaction ACK response interrupt status when the host controller function is selected. 0: No SACK interrupt is generated. 1: A SACK interrupt is generated. When this module receives an ACK response from a peripheral device in the SETUP transaction issued by this module, this module detects a SACK interrupt and indicates SACK = 1. At this time, when the corresponding interrupt enable bit is set to 1 by the software, this module generates a SACK interrupt.
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Notes: 1. To clear the status of each bit in this register, write 0 only to bits to be cleared and write 1 to the other bits.

2. When a status change shown in the BCHG bit is detected while the clock is halted (SCKE = 0) and the corresponding interrupt is enabled, the interrupt is output. Clear the BCHG interrupt status by the software after the clock is enabled.

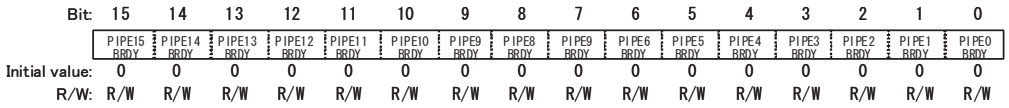
   Any interrupts other than the BCHG bit are not detected while the clock is halted (SCKE = 0).

33.3.17 BRDY Interrupt Status Register (BRDYSTS)

BRDYSTS indicates the BRDY interrupt status of each pipe.

This register is initialized by a power-on reset.

Pipe A to Pipe F are effective only when the function controller function is selected.



Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PIPE15 BRDY	PIPE14 BRDY	PIPE13 BRDY	PIPE12 BRDY	PIPE11 BRDY	PIPE10 BRDY	PIPE9 BRDY	PIPE8 BRDY	PIPE9 BRDY	PIPE6 BRDY	PIPE5 BRDY	PIPE4 BRDY	PIPE3 BRDY	PIPE2 BRDY	PIPE1 BRDY	PIPE0 BRDY
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	PIPEFBRDY	0	R/W*1	Pipe A BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.
14	PIPEEBRDY	0	R/W*1	Pipe A BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.
13	PIPEDBRDY	0	R/W*1	Pipe A BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.
12	PIPECBRDY	0	R/W*1	Pipe A BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.
11	PIPEBBRDY	0	R/W*1	Pipe A BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.
10	PIPEABRDY	0	R/W*1	Pipe A BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.
9	PIPE9BRDY	0	R/W*1	Pipe 9 BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.

Bit	Bit Name	Initial Value	R/W	Description
8	PIPE8BRDY	0	R/W*[1]	Pipe 8 BRDY Interrupt Status*[2] 0: No interrupt is generated. 1: An interrupt is generated.
7	PIPE7BRDY	0	R/W*[1]	Pipe 7 BRDY Interrupt Status*[2] 0: No interrupt is generated. 1: An interrupt is generated.
6	PIPE6BRDY	0	R/W*[1]	Pipe 6 BRDY Interrupt Status*[2] 0: No interrupt is generated. 1: An interrupt is generated.
5	PIPE5BRDY	0	R/W*[1]	Pipe 5 BRDY Interrupt Status*[2] 0: No interrupt is generated. 1: An interrupt is generated.
4	PIPE4BRDY	0	R/W*[1]	Pipe 4 BRDY Interrupt Status*[2] 0: No interrupt is generated. 1: An interrupt is generated.
3	PIPE3BRDY	0	R/W*[1]	Pipe 3 BRDY Interrupt Status*[2] 0: No interrupt is generated. 1: An interrupt is generated.
2	PIPE2BRDY	0	R/W*[1]	Pipe 2 BRDY Interrupt Status*[2] 0: No interrupt is generated. 1: An interrupt is generated.
1	PIPE1BRDY	0	R/W*[1]	Pipe 1 BRDY Interrupt Status*[2] 0: No interrupt is generated. 1: An interrupt is generated.
0	PIPE0BRDY	0	R/W*[1]	Pipe 0 BRDY Interrupt Status*[2] 0: No interrupt is generated. 1: An interrupt is generated.

Notes: 1. To clear the status of each bit in this register when BRDYM is 0, write 0 only to bits to be cleared and write 1 to the other bits.
2. When BRDYM is 0, be sure to clear this interrupt before making an access to the FIFO.

33.3.18 NRDY Interrupt Status Register (NRDYSTS)

NRDYSTS indicates the NRDY interrupt status of each pipe.

This register is initialized by a power-on reset.

Pipe A to Pipe F are effective only when the function controller function is selected.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PIPE15 NRDY	PIPE14 NRDY	PIPE13 NRDY	PIPE12 NRDY	PIPE11 NRDY	PIPE10 NRDY	PIPE9 NRDY	PIPE8 NRDY	PIPE9 NRDY	PIPE6 NRDY	PIPE5 NRDY	PIPE4 NRDY	PIPE3 NRDY	PIPE2 NRDY	PIPE1 NRDY	PIPE0 NRDY
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	PIPEFNRDY	0	R/W*	Pipe F NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
14	PIPEENRDY	0	R/W*	Pipe E NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
13	PIPEDNRDY	0	R/W*	Pipe D NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
12	PIPECNRDY	0	R/W*	Pipe C NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
11	PIPEBNRDY	0	R/W*	Pipe B NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
10	PIPEANRDY	0	R/W*	Pipe A NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
9	PIPE9NRDY	0	R/W*	Pipe 9 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.

Bit	Bit Name	Initial Value	R/W	Description
8	PIPE8NRDY	0	R/W*	Pipe 8 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
7	PIPE7NRDY	0	R/W*	Pipe 7 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
6	PIPE6NRDY	0	R/W*	Pipe 6 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
5	PIPE5NRDY	0	R/W*	Pipe 5 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
4	PIPE4NRDY	0	R/W*	Pipe 4 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
3	PIPE3NRDY	0	R/W*	Pipe 3 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
2	PIPE2NRDY	0	R/W*	Pipe 2 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
1	PIPE1NRDY	0	R/W*	Pipe 1 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
0	PIPE0NRDY	0	R/W*	Pipe 0 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.

Note: * To clear the status of each bit in this register, write 0 only to bits to be cleared and write 1 to the other bits.

33.3.19 BEMP Interrupt Status Register (BEMPSTS)

BEMPSTS indicates the BEMP interrupt status of each pipe.

This register is initialized by a power-on reset.

Pipe A to Pipe F are effective only when the function controller function is selected.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PIPE15 BEMP	PIPE14 BEMP	PIPE13 BEMP	PIPE12 BEMP	PIPE11 BEMP	PIPE10 BEMP	PIPE9 BEMP	PIPE8 BEMP	PIPE9 BEMP	PIPE6 BEMP	PIPE5 BEMP	PIPE4 BEMP	PIPE3 BEMP	PIPE2 BEMP	PIPE1 BEMP	PIPE0 BEMP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	PIPEFBEMP	0	R/W*	Pipe F BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
14	PIPEEBEMP	0	R/W*	Pipe E BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
13	PIPEDBEMP	0	R/W*	Pipe D BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
12	PIPECBEMP	0	R/W*	Pipe C BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
11	PIPEBBEMP	0	R/W*	Pipe B BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
10	PIPEABEMP	0	R/W*	Pipe A BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
9	PIPE9BEMP	0	R/W*	Pipe 9 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.

Bit	Bit Name	Initial Value	R/W	Description
8	PIPE8BEMP	0	R/W*	Pipe 8 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
7	PIPE7BEMP	0	R/W*	Pipe 7 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
6	PIPE6BEMP	0	R/W*	Pipe 6 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
5	PIPE5BEMP	0	R/W*	Pipe 5 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
4	PIPE4BEMP	0	R/W*	Pipe 4 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
3	PIPE3BEMP	0	R/W*	Pipe 3 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
2	PIPE2BEMP	0	R/W*	Pipe 2 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
1	PIPE1BEMP	0	R/W*	Pipe 1 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
0	PIPE0BEMP	0	R/W*	Pipe 0 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.

Note: * To clear the status of each bit in this register, write 0 only to bits to be cleared and write 1 to the other bits.

33.3.20 Frame Number Register (FRMNUM)

FRMNUM indicates the sources of isochronous errors and a frame number.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OVRN	CRCE	—	—	—	FRNM[10:0]										
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W*	R/W*	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	OVRN	0	R/W*	Overrun/Underrun Detect Status Indicates whether an overrun or underrun error is detected or not in a pipe that is performing isochronous transfer. 0: No error is detected. 1: An error is detected. Writing 0 to this bit by the software clears this bit to 0. At this time, write 1 to the other bits in this register. (1) When the host controller function is selected This module indicates OVRN =1 in any of the following cases. When the OUT token transmit timing comes when transmit data write to the FIFO buffer is not completed in a transmit direction pipe of isochronous transfer type When the IN token transmit timing comes with no side of the FIFO buffer empty in a receive direction pipe of isochronous transfer type (2) When the function controller function is selected This module indicates OVRN =1 in any of the following cases. When the IN token is received when transmit data write to the FIFO buffer is not completed in a transmit direction pipe of isochronous transfer type When the OUT token is received with no side of the FIFO buffer empty in a receive direction pipe of isochronous transfer type

Bit	Bit Name	Initial Value	R/W	Description
14	CRCE	0	R/W*	Receive Data Error Indicates whether a CRC error or bit stuffing error is detected or not in a pipe that is performing isochronous transfer. 0: No error is detected. 1: An error is detected. Writing 0 to this bit by the software clears this bit to 0. At this time, write 1 to the other bits in this register. (1) When the host controller function is selected When a CRC error is detected, this module generates an internal NRDY interrupt request. (2) When the function controller function is selected When a CRC error is detected, this module does not generate an internal NRDY interrupt request.
13 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 0	FRNM [10:0]	H'000	R	Frame Number This module modifies this bit at the SOF transmit timing (every 1 ms) or when an SOF is received and indicates the latest frame number. Read these bits twice and confirm that the read value is equal each time.

Note: * Only writing 0 is enabled.

33.3.21 μ Frame Number Register (UFRMNUM)

UFRMNUM indicates a μ frame number.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	UFRNM[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2 to 0	UFRNM[2:0]	000	R	μ Frame Indicate a μ frame number. In high-speed operating mode, these bits indicate a μ frame number. In other operating modes, these bits indicate B'000. Read these bits twice and confirm that the read value is equal each time.

33.3.22 USB Address Register (USBADDR)

USBADDR indicates a USB address.

This register is valid only when the function controller function is selected. To set the address of a peripheral device when the host controller function is selected, use the DEVSEL bits in PIPEMAXP.

This register is initialized by a power-on reset or USB bus reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	USBADDR[6:0]						
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6 to 0	USBADDR[6:0]	H'00	R	USB Address Indicate the USB address allocated by the host when the SET_ADRESS request is successfully processed with the function controller function selected. When this module detects a USB reset, these bits indicate H'00. When the host controller function is selected, these bits are invalid.

33.3.23 USB Request Type Register (USBREQ)

USBREQ stores the setup request for control transfers.

When the function controller function is selected, USBREQ stores the values of received bRequest and bmRequestType. When the host controller function is selected, USBREQ sets the values of bRequest and bmRequestType to be sent.

This register is initialized by a power-on reset or USB bus reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BREQUEST[7:0]								BMREQUESTTYPE[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*

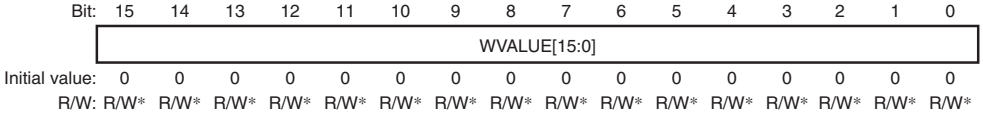
Bit	Bit Name	Initial Value	R/W	Description
15 to 8	BREQUEST [7:0]	H'00	R/W*	Request Store the value of USB request bRequest. (1) When the host controller function is selected Set the value of USB request data of the SETUP transaction to be sent. Do not modify these bits when the SUREQ bit is 1. (2) When the function controller function is selected Indicate the USB request data received in the SETUP transaction. These bits cannot be modified.
7 to 0	BMREQUEST TYPE[7:0]	H'00	R/W*	Request Type Store the value of USB request bmRequestType. (1) When the host controller function is selected: Set the value of USB request data of the SETUP transaction to be sent. Do not modify these bits when the SUREQ bit is 1. (2) When the function controller function is selected: Indicate the USB request data received in the SETUP transaction. These bits cannot be modified.

Note: * When the function controller function is selected, these are read-only bits and cannot be modified. When the host controller function is selected, these are readable/writable bits.

33.3.24 USB Request Value Register (USBVAL)

When the function controller function is selected, USBVAL stores the value of received wValue. When the host controller function is selected, USBVAL sets the value of wValue to be sent.

This register is initialized by a power-on reset or USB bus reset.



Bit	Bit Name	Initial Value	R/W	Description
15 to 0	WVALUE [15:0]	H'0000	R/W*	Value Store the value of USB request wValue. (1) When the host controller function is selected Set the value of USB request wValue of the SETUP transaction to be sent. Do not modify these bits when the SUREQ bit is 1. (2) When the function controller function is selected Indicate the value of USB request wValue received in the SETUP transaction. These bits cannot be modified.

Note: * When the function controller function is selected, these are read-only bits and cannot be modified. When the host controller function is selected, these are readable/writable bits.

33.3.25 USB Request Index Register (USBINDX)

USBINDX stores the setup request for control transfers.

When the function controller function is selected, USBINDX stores the value of received wIndex. When the host controller function is selected, USBINDX sets the value of wIndex to be sent.

This register is initialized by a power-on reset or USB bus reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WINDEX[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*

Bit	Bit Name	Initial Value	R/W	Description
15 to 0	WINDEX [15:0]	H'0000	R/W*	Index Store the value of USB request wIndex. (1) When the host controller function is selected Set the value of USB request wIndex of the SETUP transaction to be sent. Do not modify these bits when the SUREQ bit is 1. (2) When the function controller function is selected Indicate the value of USB request wIndex received in the SETUP transaction. These bits cannot be modified.

Note: * When the function controller function is selected, these are read-only bits and cannot be modified. When the host controller function is selected, these are readable/writable bits.

33.3.26 USB Request Length Register (USBLENG)

USBLENG stores the setup request of control transfers.

When the function controller function is selected, USBLENG stores the value of received wLength. When the host controller function is selected, USBLENG sets the value of wLength to be sent.

This register is initialized by a power-on reset or USB bus reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WLENGTH[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*

Bit	Bit Name	Initial Value	R/W	Description
15 to 0	WLENGTH [15:0]	H'0000	R/W*	Length Store the value of USB request wLength. (1) When the host controller function is selected Set the value of USB request wLength of the SETUP transaction to be sent. Do not modify these bits when the SUREQ bit is 1. (2) When the function controller function is selected Indicate the value of USB request wLength received in the SETUP transaction. These bits cannot be modified.

Note: * When the function controller function is selected, these are read-only bits and cannot be modified. When the host controller function is selected, these are readable/writable bits.

33.3.27 DCP Configuration Register (DCPCFG)

DCPCFG specifies the data transfer direction of the default control pipe (DCP).

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	DIR	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	DIR	0	R/W	Transfer Direction Specifies the data stage and status stage transfer direction of control transfers when the host controller function is selected. 0: Data receive direction 1: Data transmit direction When the function controller function is selected, set this bit to 0.
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

33.3.28 DCP Maximum Packet Size Register (DCPMAXP)

DCPMAXP specifies the maximum packet size of the DCP.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DEVSEL[3:0]				—	—	—	—	—	MXPS[6:0]						
Initial value:	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	DEVSEL [3:0]	0000	R/W	Device Select Specify the address of the peripheral device that is a remote party for control transfers when the host controller function is selected. 0000: Address 0000 0001: Address 0001 : : 1001: Address 1001 1010: Address 1010 Other than above: Setting prohibited Set DEVADDn corresponding to the value of these bits, and then set these bits. When setting DEVSEL = 0010, for example, set the address in DEVADD2. Set these bits when CSSTS = 0, PID = NAK, and the SUREQ bit is 0. To change these bits after changing the PID bits in DCP from BUF to NAK, check CSSTS = 0 and PBUSY = 0 and then change these bits. However, the software does not have to check the PBUSY bit when this module changed the PID bit to NAK. When the function controller function is selected, set these bits to B'0000.
11 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
6 to 0	MXPS [6:0]	H'40	R/W	Maximum Packet Size Set the payload of DCP data (maximum DCP packet size) in these bits. The initial value of these bits is H'40 (64 bytes). Set a value in the MXPS bits based on the USB Specification. Set the MXPS bits when CSSTS = 0, PID = NAK, and the CURPIPE bits are not set. When setting these bits to 1 after changing the PID bits for the pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK. Do not write the FIFO buffer when the MXPS bits are 0 or set the PID bits to BUF.

33.3.29 DCP Control Register (DCPCTR)

DCPCTR is used to monitor the buffer memory status, change/check the data PID sequence bit, and set the response PID for a DCP.

This register is initialized by a power-on reset. The PID2 to PID0 bits in CCPL are also initialized by a USB bus reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BSTS	SUREQ	CSCLR	CSSTS	SUREQCLR	—	—	SQCLR	SQSET	SQMON	PBUSY	PINGE	—	CCPL	PID[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
R/W:	R	R/W*2	R/W*1	R	R/W*1	R	R	R/W*1	R/W*1	R	R	R/W	R	R/W*1	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	BSTS	0	R	Buffer Status Indicates whether the DCP FIFO buffer is accessible or not. 0: The buffer is not accessible. 1: The buffer is accessible. This bit indicates as follows depending on the ISEL value. When ISEL = 0, this bit indicates whether the buffer is ready to read receive data. When ISEL = 1, this bit indicates whether the buffer is ready to write transmit data.

Bit	Bit Name	Initial Value	R/W	Description
14	SUREQ	0	R/W*[2]	Sending SETUP Token When the host controller function is selected, a setup packet is sent by writing 1 to this bit. 0: Invalid 1: A setup packet is sent. After processing the SETUP transaction, this module generates a SACK interrupt or SIGN interrupt and clears this bit to 0. When the SUREQCLR bit is set to 1 by the software, this module clears this bit to 0. Set this bit to 1 after setting the USB request to be sent in the SETUP transaction in the DEVSEL bits, USBREQ, USBVAL, USBINDX, and USBLENG registers. Check that PID bits in DCP are set to NAK before setting the SUREQ bit to 1. Furthermore, do not change the values of the DEVSEL bits, USBREQ, USBVAL, USBINDX, and USBLENG registers after setting this bit to 1 until the SETUP transaction is completed (while SUREQ = 1). Set this bit to 1 only when sending a SETUP token. In other cases, be sure to set this bit to 0. When the function controller function is selected, be sure to set this bit to 0.

Bit	Bit Name	Initial Value	R/W	Description
13	CSCLR	0	R/W*[1]	Split Transactions C-SPLIT Status Clear When the host controller function is selected, the CSSTS bit can be cleared to 0 by writing 1 to this bit for data transfer using split transactions. In this case, the next transfer of DCP restarts with S-SPLIT. 0: Invalid 1: Clears the CSSTS bit to 0. When this bit is set to 1 by the software, this module clears the CSSTS bit to 0. To forcibly restart the next transfer with S-SPLIT in data transfer using split transactions, set this bit to 1 by the software. Since this module automatically clears the CSSTS bit to 0 at the end of C-SPLIT in normal split transactions, the software needs not clear the CSSTS bit. Control the CSSTS bit with this bit while communication is halted by clearing the UACT bit or when it is clarified that no data transfer is performed by detection of DETACH. Even if this bit is set to 1 when CSSTS is 0, CSSTS remains 0. When the function controller function is selected, be sure to set this bit to 0.
12	CSSTS	0	R	Split Transactions COMPLETE SPLIT (C-SPLIT) Status When the host controller function is selected, the C-SPLIT status of split transactions is indicated. 0: START-SPLIT (S-SPLIT) transaction is being processed or a device that is not used in split transactions is being processed. 1: C-SPLIT transaction is being processed. This module sets this bit to 1 when starting C-SPLIT, and clears this bit to 0 when C-SPLIT end is detected. When the function controller function is selected, the read value of this bit is invalid.

Bit	Bit Name	Initial Value	R/W	Description
11	SUREQCLR	0	R/W*[1]	SUREQ Bit Clear When the host controller function is selected, the SUREQ bit can be cleared to 0 by writing 1 to this bit. 0: Invalid 1: Clears the SUREQ bit. This bit always indicates 0. When communication is halted with the SUREQ bit set to 1 in the SETUP transaction, set this bit to 1 by the software. Since this module automatically clears the SUREQ bit to 0 at the end of normal SETUP transaction, the software needs not clear the SUREQ bit. Control the SUREQ bit with this bit while communication is halted by clearing the UACT bit or when it is clarified that no data transfer is performed by detection of DETACH. When the function controller function is selected, be sure to set this bit to 0.
10, 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	SQCLR	0	R/W*[1]	Toggle Bit Clear The expected value of the sequence toggle bit for the next transaction in DCP transfer can be set in DATA0. 0: Invalid 1: The expected value is set in DATA0. This bit always indicates 0. Do not set the SQCLR and SQSET bits to 1 at the same time. Set this bit to 1 when CSCTS = 0, PID = NAK, and the CURPIPE bits are not set. When setting this bit to 1 after changing the PID bits for the pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.

Bit	Bit Name	Initial Value	R/W	Description
7	SQSET	0	R/W*[1]	Toggle Bit Set The expected value of the sequence toggle bit for the next transaction in DCP transfer can be set in DATA1. 0: Invalid 1: The expected value is set in DATA1. Do not set the SQCLR and SQSET bits to 1 at the same time. Set this bit to 1 when CSCTS = 0, PID = NAK, and the CURPIPE bits are not set. When setting this bit to 1 after changing the PID bits for the pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.
6	SQMON	1	R	Sequence Toggle Bit Monitor Indicates the expected value of the sequence toggle bit for the next transaction in DCP transfer. 0: DATA0 1: DATA1 When the transaction is successfully completed, this module toggles this bit. However, when a DATA-PID mismatch occurs in the receive direction transfer, this bit is not toggled. When the function controller function is selected, this module sets this bit to 1 (sets the expected value in DATA1) when the setup packet is successfully received. When the function controller function is selected, this module does not read this bit in IN transactions or OUT transactions in the status stage.

Bit	Bit Name	Initial Value	R/W	Description
5	PBUSY	0	R	Pipe Busy Indicates whether the DCP communication state is shifted to the NAK state or not when the DCP changed the PID bits from BUF to NAK. 0: Transition to the NAC state is not completed. 1: Transition to the NAC state is completed. When this module starts the USB transaction for the corresponding pipe, this module sets this bit to 1. This module clears this bit to 0 upon completion of each transaction. After the software sets PID = NAK, read this bit to check whether changing the pipe setting is enabled or not.
4	PINGE	0	R/W	PING Token Output Enable When this bit is set to 1 with the host controller function selected, this module sends the PING token in the transmit direction transfer. The transmit direction transfer is started with the PING transaction. 0: Sending the PING token is disabled. 1: Normal PING operation When an ACK handshake is detected in the PING transaction, this module executes an OUT transaction for the next transaction. When a NAK handshake is detected in an OUT transaction, this module executes a PING transaction for the next transaction. When the software sets this bit to 0 with the host controller function selected, this module does not send the PING token in the transmit direction transfer. The transmit direction transfer is always performed in OUT transactions. Change this bit when CSSTS = 0 and PID = NAK. When setting this bit to 1 after changing the PID bits for the pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK. When the function controller function is selected, be sure to set this bit to 0.

Bit	Bit Name	Initial Value	R/W	Description
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2	CCPL	0	R/W*[1]	Control Transfer End Enable Enables the status stage end of control transfers when the function controller function is selected. 0: Invalid 1: The control transfer end is enabled. When the software sets this bit to 1 while the corresponding PID bits are set to BUF, this module finishes the control transfer stage. That is, this module sends an ACK handshake in response to OUT transactions from the USB host in the control read transfer, and sends a Zero-Length packet in response to IN transactions from the USB host in control write and no-data control transfers. However, a SET_ADDRESS request is detected, this module automatically sends responses from the SETUP stage until the end of the status stage irrespective of the setting of this bit. When this module receives the next setup packet, this module clears this bit to 0. When VALID = 1, the software cannot write 1 to this bit. When the host controller function is selected, be sure to set this bit to 0.

Bit	Bit Name	Initial Value	R/W	Description
1, 0	PID[1:0]	00	R/W	Response PID Control responses of this module in control transfers. 00: NAK response 01: BUF response (depending on buffer state) 10: STALL response 11: STALL response (1) When the host controller function is selected Change these bits from NAK to BUF. When transmit direction is set Write all transmit data to the FIFO buffer when UACT = 1 and PID = NAK, and then set the PID bits to BUF. After BUF is set, this module executes OUT transactions (or PING transactions). When receive direction is set Check that the FIFO buffer is empty (or make it empty) when UACT = 1 and PID = NAK, and then set the PID bits to BUF. After BUF is set, this module executes IN transactions. This module modifies these bits in the following cases. When this module receives data with a size exceeding the MaxPacketSize value while these bits are set to BUF by the software, this module indicates PID = STALL (11). When this module detects a CRC error or another receive error three times in a row, this module indicates PID = NAK. When this module receives a STALL handshake, this module indicates PID = STALL (11). After this module sends S-SPLIT of split transactions for the selected pipe (indicating CSSTS = 1), this module executes the transaction until C-SPLIT is completed even if the software changed these bits to NAK. When C-SPLIT is completed, this module indicates PID = NAK.

Bit	Bit Name	Initial Value	R/W	Description
1, 0	PID[1:0]	00	R/W	(2) When the function controller function is selected This module modifies these bits in the following cases. This module changes these bits to NAK upon receiving a SETUP packet. At this time, this module indicates VALID = 1. The software cannot modify these bits until the software sets VALID = 0. When this module receives data with a size exceeding the MaxPacketSize value while these bits are set to BUF by the software, this module indicates PID = STALL (11). When this module detects a control transfer sequence error, this module indicates PID = STALL (1x). When this module detects a USB bus reset, this module indicates PID = NAK. This module does not read the value of these bits during the SET_ADDRESS request processing (auto processing).

Notes: 1. These bits are always read as 0. Only writing 1 is enabled.
2. Only writing 1 is enabled.

33.3.30 Pipe Window Select Register (PIPESEL)

Make settings for pipes 1 to F (1 to 9 when the function controller function is selected) using PIPESEL, PIPECFG, PIPEBUF, PIPEMAXP, PIPEPERI, PIPEnCTR, PIPEnTRE, and PIPEnTRN.

Specify a pipe to be used with PIPESEL, and then make function settings for each pipe in PIPECFG, PIPEBUF, PIPEMAXP, and PIPEPERI. The PIPEnCTR, PIPnTRE, and PIPnTRN registers can be set independently from pipe selection using PIPESEL.

Not only the selected pipe but also the corresponding bits in registers for all pipes are initialized by a power-on reset or USB bus reset.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	PIPESEL[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
3 to 0	PIPESEL [3:0]	0000	R/W	Pipe Window Select Specify a pipe number corresponding to PIPECFG, PIPEBUF, PIPEMAXP, and PIPEPERI to be read or written. 0000: No pipe is selected. 0001: Pipe 1 0010: Pipe 2 0011: Pipe 3 0100: Pipe 4 0101: Pipe 5 0110: Pipe 6 0111: Pipe 7 1000: Pipe 8 1001: Pipe 9 1010: Pipe A* 1010: Pipe B* 1010: Pipe C* 1010: Pipe D* 1010: Pipe E* 1010: Pipe F* PIPECFG, PIPEBUF, PIPEMAXP, and PIPEPERI corresponding to the pipe number specified by these bits can be read and written. When these bits are set to 0000, all bits in PIPECFG, PIPEBUF, PIPEMAXP, and PIPEPERI are read as 0 and cannot be modified.

Note * Pipe A to Pipe F are effective only when the function controller function is selected.

33.3.31 Pipe Configuration Register (PIPECFG)

PIPECFG specifies the transfer type, buffer memory access direction, and endpoint number for pipes 1 to F(Pipe A to Pipe F are effective only when the function controller function is selected), selects continuous transfer mode or discontinuous transfer mode, and single buffer or double buffer, and also specifies whether to disable the operation of each pipe when data transfer finishes.

This register is initialized by a power-on reset. The TYPE1 and TYPE0 bits are also initialized by a USB bus reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TYPE[1:0]		—	—	—	BFRE	DBLB	CNT MD	SHT NAK	—	—	DIR	EPNUM[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15, 14	TYPE[1:0]	00	R/W	Transfer Type Select the transfer type of the pipe specified by the PIPESEL bits (selected pipe). Pipes 1 and 2 00: No pipe is used. 01: Bulk transfer 10: Setting prohibited 11: Isochronous transfer Pipes 3 to 5, and 9 to F when the function controller function is selected 00: No pipe is used. 01: Bulk transfer 10: Setting prohibited 11: Setting prohibited Pipes 6 to 8, and 9 when the host controller function is selected 00: No pipe is used. 01: Setting prohibited 10: Interrupt transfer 11: Setting prohibited Before setting the selected pipe for PID = BUF (before starting USB communication using the selected pipe), be sure to set these bits to a value other than 00. Modify these bits when the PID bits of the selected pipe are set to NAK. When changing the setting of these bits after changing the PID bits for the selected pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.
13 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
10	BFRE	0	R/W	BRDY Interrupt Operation Specifies the BRDY interrupt output timing from this module to the CPU for the selected pipe. 0: At a BRDY interrupt timing during data transmission or reception 1: At a BRDY interrupt timing after reading data When this bit is set to 1 by the software and the selected pipe is used in the receive direction, this module detects the transfer end and outputs a BRDY interrupt when the packet is completely read. When a BRDY interrupt occurs with this setting, the software must set BCLR = 1. Unless BCLR = 1 is set, the FIFO buffer allocated to the selected pipe does not enter the receive ready state. When this bit is set to 1 by the software and the selected pipe is used in the transmit direction, this module generates no BRDY interrupt. For details, see section 33.4.2 (1), BRDY Interrupt. Modify this bit when CSSTS = 0, PID = NAK, and no pipe number is specified by the CURPIPE bits. Furthermore, when changing the setting of this bit after USB communication using the selected pipe, set the ACLRM bit to 1 and clear it to 0 continuously by the software to clear the FIFO buffer allocated to the selected pipe, in addition to the three register states above. When changing the setting of this bit after changing the PID bits for the selected pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.

Bit	Bit Name	Initial Value	R/W	Description
9	DBLB	0	R/W	Double Buffer Mode Specifies a single buffer or double buffer for the FIFO buffer used in the selected pipe. 0: Single buffer 1: Double buffer This bit is valid when pipes 1 to 5, 9 to F are selected. When this bit is set to 1 by the software, this module allocates the FIFO buffer size specified by the BUFSIZE bits in PIPEBUF to the selected pipe for two sides. Thus the size of the FIFO buffer that this module allocates to the selected pipe is as follows: (BUFSIZE + 1) * 64 * (DBLB + 1) [bytes] When this bit is set to 1 by the software and the selected pipe is used in the transmit direction, this module generates no BRDY interrupt. For details, see section 33.4.2 (1), BRDY Interrupt. Modify this bit when CSSTS = 0, PID = NAK, and no pipe number is specified by the CURPIPE bits. Furthermore, when changing the setting of this bit after USB communication using the selected pipe, set the ACLRM bit to 1 and clear it to 0 continuously by the software to clear the FIFO buffer allocated to the selected pipe, in addition to the three register states above. When changing the setting of this bit after changing the PID bits for the selected pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.

Bit	Bit Name	Initial Value	R/W	Description
8	CNTMD	0	R/W	Continuous Transfer Mode Selects continuous transfer mode or discontinuous transfer mode to be used in communication for the selected pipe. 0: Discontinuous transfer mode 1: Continuous transfer mode This bit is valid when pipes 1 to 5 (and 9 to F when the function controller function is selected) are selected by the PIPESEL bits and bulk transfer is selected (TYPE = 01). Modify this bit when CSSTS = 0, PID = NAK, and no pipe number is specified by the CURPIPE bits. Furthermore, when changing the setting of this bit after USB communication using the selected pipe, set the ACLRM bit to 1 and clear it to 0 continuously by the software to clear the FIFO buffer allocated to the selected pipe, in addition to the three register states above. When changing the setting of this bit after changing the PID bits for the selected pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.

Bit	Bit Name	Initial Value	R/W	Description
7	SHTNAK	0	R/W	Pipe Disable at the Time of Transfer End Specifies whether to change the setting of the PID bits to NAK at the end of transfer when the selected pipe is in the receive direction. 0: The pipe is continued at the end of transfer. 1: The pipe is disabled at the end of transfer. This bit is valid when the selected pipe is either of pipes 1 to 5 (and 9 to F when the function controller function is selected) and is in the receive direction. When the software sets this bit to 1 for a receive direction pipe, this module changes the setting of the PID bits corresponding to the selected pipe to NAK for the selected pipe when this module determines the transfer end. When the following conditions are satisfied, this module determines the transfer end. When short packet data (including a Zero-Length packet) is correctly received. When the transaction counter is used and packets with a size of the transaction counter are correctly received. Modify this bit when CSSTS = 0 and PID = NAK. When changing the setting of this bit after changing the PID bits for the selected pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK. For transmit direction pipes, set this bit to 0.
6, 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
4	DIR	0	R/W	Transfer Direction Selects the transfer direction of the selected pipe. 0: Receive direction 1: Transmit direction When this bit is set to 0 by the software, this module uses the selected pipe in the receive direction. When this bit is set to 1, this module uses the selected pipe in the transmit direction. Modify this bit when CSSTS = 0, PID = NAK, and no pipe number is specified by the CURPIPE bits. Furthermore, when changing the setting of this bit after USB communication using the selected pipe, set the ACLRM bit to 1 and clear it to 0 continuously by the software to clear the FIFO buffer allocated to the selected pipe, in addition to the three register states above. When changing the setting of this bit after changing the PID bits for the selected pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.
3 to 0	EPNUM[3:0]	0000	R/W	Endpoint Number Specify the endpoint number of the selected pipe. The setting of 0000 means an unused pipe. Modify these bits when CSSTS = 0 and PID = NAK. When changing the setting of these bits after changing the PID bits for the selected pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK. Set these bits so that the combination of the DIR setting and the EPNUM setting does not overlap the setting of other pipes (EPNUM = 0000 is allowed in this case.)

33.3.32 Pipe Buffer Register (PIPEBUF)

PIPEBUF specifies the buffer size and buffer number for pipes 1 to F(Pipe A to Pipe F are effective only when the function controller function is selected).

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	BUFSIZE[4:0]					—	—	BUFNMB[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
14 to 10	BUFSIZE [4:0]	H'00	R/W	Buffer Size Specify the buffer size of the pipe specified by the PIPESEL bits (selected pipe) in units of blocks. One block is 64 bytes. 00000 (H'00): 64 bytes 00001 (H'01): 128 bytes : : 11111 (H'1F): 2 Kbytes When DBLB = 1 is set by the software, this module allocates the FIFO buffer size specified by these bits to the selected pipe for two sides. Thus the size of the FIFO buffer that this module allocates to the selected pipe is as follows: (BUFSIZE + 1) * 64 * (DBLB + 1) [bytes] A value that can be set in these bits varies depending on pipes selected. For pipes 1 to 5 (and 9 to F when the function controller function is selected): Set BUFSIZE to H'00 to H'1F. For pipes 6 to 8 (and 9 when the host controller function is selected): Set BUFSIZE to H'00. When using the buffer with CNTMD = 1, set a value in multiples of MaxPacketSize in these bits. Modify these bits when CSSTS = 0, PID = NAK, and no pipe number is specified by the CURPIPE bits. When changing the setting of this bit after changing the PID bits for the selected pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.
9, 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	BUFNMB [7:0]	H'00	R/W	Buffer Number Specify the FIFO buffer number of the selected pipe with a value from H'04 to H'87. When the selected pipe is either of pipes 1 to 5, 9 to F, these bits can be set to a value according to user systems. Set BUFNMB to H'06 to H'4F. BUFNMB = 0 to 3 are for DCP only. BUFNMB = 4 is for pipe 6 only. However, when pipe 6 is not used, this is available for other pipes. When pipe 6 is selected, these bits cannot be modified and this module automatically allocates BUFNMB = 4. BUFNMB = 5 is for pipe 7 only. However, when pipe 7 is not used, this is available for other pipes. When pipe 7 is selected, these bits cannot be modified and this module automatically allocates BUFNMB = 5. BUFNMB = 6 is for pipe 8 only. However, when pipe 8 is not used, this is available for other pipes. When pipe 8 is selected, these bits cannot be modified and this module automatically allocates BUFNMB = 6. Modify these bits when CSSTS = 0, PID = NAK, and no pipe number is set in the CURPIPE bits. When changing the setting of these bits after changing the PID bits for the selected pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.

33.3.33 Pipe Maximum Packet Size Register (PIPEMAXP)

PIPEMAXP specifies the maximum packet size for pipes 1 to F (Pipe A to Pipe F are effective only when the function controller function is selected).

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DEVSEL[3:0]				—	MXPS[10:0]										
Initial value:	0	0	0	0	0	*	*	*	*	*	*	*	*	*	*	*
R/W:	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	DEVSEL[3:0]	00	R/W	Device Select Specify the USB device address of the peripheral device that is a remote party for communication when the host controller function is selected. 0000: Address 0000 0001: Address 0001 0010: Address 0010 : : 1010: Address 1010 Other than above: Setting prohibited Set these bits after setting DEVADDn (n = 0 to A) corresponding to the value of these bits. When setting DEVSEL = 0010, for example, set the address in DEVADD2. To change these bits after changing the PID bits in DCP from BUF to NAK, check CSSTS = 0 and PBUSY = 0 and then change these bits. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK. When the function controller function is selected, set these bits to B'0000.
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
10 to 0	MXPS[10:0]	*	R/W	Maximum Packet Size Specify the payload of data (maximum packet size) of the selected pipe. The settable value range for each pipe is as follows: Pipes 1 and 2: 1 byte (H'001) to 1024 bytes (H'400) Pipes 3 to 5, and 9 to F when the function controller function is selected: 8 (H'008), 16 (H'010), 32 (H'020), 64 (H'040), or 512 bytes (H'200) (MXPS2 to MXPS0 bits are not provided.) Pipes 6 to 8, and 9 when the host controller function is selected: 1 byte (H'001) to 64 bytes (H'040) Set a value in the MXPS bits based on the USB Specification for each transfer type. To transmit an isochronous pipe in split transactions, set a value of 188 bytes or less in the MXPS bits. When changing the setting of this bit after changing the PID bits for the selected pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK. Do not write the FIFO buffer when the MXPS = 0 or set the PID bits to BUF.

Note: * The initial value is H'000 (when no pipe is selected by the PIPESEL bits in PIPESEL) or H'040 (when a pipe is selected).

33.3.34 Pipe Cycle Control Register (PIPEPERI)

PIPEPERI specifies whether to activate the buffer flush function or not at the time of an interval error during the isochronous IN transfer, and also specifies the interval error detection interval for pipes 1 to F (Pipe A to Pipe F are effective only when the function controller function is selected).

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	IFIS	—	—	—	—	—	—	—	—	—	IITV[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	IFIS	0	R/W	Isochronous IN Buffer Flush Specifies whether to flush the FIFO buffer when the pipe specified by the PIPESEL bits (selected pipe) is isochronous IN transfer type. 0: The FIFO buffer is not flushed. 1: The FIFO buffer is flushed. Buffer flush is a function that this module automatically clears the FIFO buffer when this module does not receive IN-Token from the USB host in a (μ) frame for each interval specified in the IITV bits when the function controller function is selected and the selected pipe is isochronous IN transfer type. When double buffer is selected (DBLB = 1), this module clears data of only the older side. The FIFO buffer is cleared when an SOF packet is received immediately after the (μ) frame where IN-Token is to be received. Even if the SOF packet is corrupted, the FIFO buffer is cleared at the time when the SOF packet is to be received using the internal interpolation. When the host controller function is selected, set this bit to 0. When the selected pipe is not isochronous transfer type, set this bit to 0.

Bit	Bit Name	Initial Value	R/W	Description
11 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2 to 0	IITV[2:0]	000	R/W	Interval Error Detection Interval Specify the interval error detection interval of the selected pipe with a value of 2's n-th power of the frame timing. This function differs in detail between host controller function and function controller function as described later. Set these bits when CSSTS = 0, PID = NAK, and no pipe number is specified by the CURPIPE bits. When changing the setting of these bits after changing the PID bits for the selected pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK. To change the setting of these bits after USB communication, set PID = NAK and then set ACLRM = 1 to initialize the interval timer. These bits are not provided for pipes 3 to 5, and 9 to F when the function controller function is selected. Set 000 in the position of these bits corresponding to pipes 3 to 5, and 9 to F when the function controller function is selected.

33.3.35 Pipe n Control Register (PIPEnCTR) (n = 1 to F (Pipe A to Pipe F are effective only when the function controller function is selected.))

PIPEnCTR monitors the buffer memory status, changes/checks the data PID sequence bits, selects whether to use auto-response mode and buffer auto-clear mode, and specifies a response PID for pipes 1 to F(Pipe A to Pipe F are effective only when the function controller function is selected). This register can be set independently of the pipe selection using PIPESEL.

This register is initialized by a power-on reset. The PID1 and PID0 bits are also initialized by a USB bus reset.

(1) PIPEnCTR (n = 1 to 5, and 9 to F when the function controller function is selected)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BSTS	INBUFM	CSCLR	CSSTS	—	ATREPM	ACLRM	SQCLR	SQSET	SQMON	PBUSY	—	—	—	PID[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W*2	R	R	R/W	R/W	R/W*1	R/W*1	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	BSTS	0	R	Buffer Status Indicates the FIFO buffer status of the pipe. 0: The buffer is not accessible from the CPU. 1: The buffer is accessible from the CPU. The meaning of this bit differs depending on the settings of the DIR, BFRE, and DCLRM bits as shown in Table 33.9.

Bit	Bit Name	Initial Value	R/W	Description
14	INBUFM	0	R	Transmit Buffer Monitor Indicates the FIFO buffer status of the selected pipe in the transmit direction. 0: The buffer memory contains no transmittable data. 1: The buffer memory contains transmittable data. When transmit direction (DIR = 1) is set for the pipe, this module sets this bit to 1 when the software (or DMAC) finishes writing data to the FIFO buffer for at least one register set. When this module finishes sending all data on the register set (writing is completed) of the FIFO buffer, this bit indicates 0. In the case of a double buffer (DBLB = 1), when this module finishes sending all data on both register sets and the software (or DMAC) has not completed writing of data for one register set, this bit indicates 0. When receive direction (DIR = 0) is set for the selected pipe, this bit indicates the same value as the BSTS bit.

Bit	Bit Name	Initial Value	R/W	Description
13	CSCLR	0	R/W*[2]	CSPLIT Status Clear When the software sets this bit to 1 with the host controller function selected, this module clears the CSSTS bit to 0. 0: Invalid 1: Clears the CSSTS bit to 0. To forcibly restart the next transfer with S-SPLIT in data transfer using split transactions, set this bit to 1 by the software. Since this module automatically clears the CSSTS bit to 0 at the end of C-SPLIT in normal split transactions, the software needs not clear the CSSTS bit. Clear the CSSTS bit with this bit while communication is halted by clearing the UACT bit or when it is clarified that no data transfer is performed by detection of Detach mode. Even if this bit is set to 1 when CSSTS is 0, CSSTS remains 0. When the function controller function is selected, be sure to set this bit to 0.
12	CSSTS	0	R	CSSTS Status When the host controller function is selected, this bit indicates the C-SPLIT status of split transactions. 0: START-SPLIT (S-SPLIT) transaction is being processed or no split transaction is used. 1: C-SPLIT transaction is being processed. This module sets this bit to 1 when starting C-SPLIT, and clears this bit to 0 when C-SPLIT end is detected. The value of this bit is valid only when the host controller function is selected.
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
10	ATREPM	0	R/W	Auto-Response Mode Enables or disables auto-response for the selected pipe. 0: Auto-response is disabled. 1: Auto-response is enabled. When the function controller function is selected and the transfer type of the selected pipe is set to bulk transfer, this bit can be set to 1. When this bit is 1, this module sends responses to tokens from the USB host as follows: (1) When the selected pipe is set for Bulk-IN transfer (TYPE = 01 and DIR = 1) When ATREPM = 1 and PID = BUF, this module sends a Zero-Length packet in response to the IN-Token. Each time this module receives ACK from the USB host (flow of one transaction: receiving IN-Token -> sending Zero Length packet -> receiving ACK), this module updates the sequence toggle bit (DATA-PID) by toggling it. No BRDY interrupt or BEMP interrupt is generated. (2) When the selected pipe is set for Bulk-OUT transfer (TYPE = 01 and DIR = 0) When ATREPM = 1 and PID = BUF, this module sends NAK in response to the OUT-Token (or PING-Token) and generates an NRDY interrupt. Modify this bit when CSSTS = 0 and PID = NAK. When setting this bit to 1 after changing the PID bits for the pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK. Be sure to set this bit to 1 for USB communication when the FIFO buffer is empty. Do not write data to the FIFO buffer during USB communication with this bit set to 1. When the selected pipe is set for isochronous transfer, be sure to set this bit to 0. When the host controller function is selected, be sure to set this bit to 0.

Bit	Bit Name	Initial Value	R/W	Description
9	ACLRM	0	R/W	Buffer Auto-Clear Mode Enables or disables buffer auto-clear mode for the selected pipe. 0: Buffer auto-clear mode is disabled. 1: Buffer auto-clear mode is enabled. (All buffers are initialized.) To completely delete the data in the FIFO buffer allocated to the pipe, write 1 and then 0 continuously to the ACLRM bit. Table 33.10 shows data cleared by this module when this bit is set to 1 and then 0 and cases where such data is cleared. Modify this bit when CSSTS = 0 and PID = NAK. When setting this bit to 1 after changing the PID bits for the pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.
8	SQCLR	0	R/W*[1]	Toggle Bit Clear Set this bit to 1 to clear the expected value (in DATA0) of the sequence toggle bit for the next transaction of the selected pipe. 0: Invalid 1: The expected value is cleared in DATA0. When the software sets this bit to 1, this module sets the expected value of the sequence toggle bit of the pipe in DATA0. This module always indicates SQCLR = 0. When this bit is set to 1 for a Bulk-Out transfer pipe with the host controller function selected, this module starts the next transfer with the PING-token for the pipe. Set the SQCLR bit to 1 when CSCTS = 0 and PID = NAK. When setting this bit to 1 after changing the PID bits for the selected pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.

Bit	Bit Name	Initial Value	R/W	Description
7	SQSET	0	R/W*[1]	Toggle Bit Set Set this bit to 1 to set the expected value of the sequence toggle bit for the next transaction of the selected pipe. 0: Invalid 1: The expected value is set in DATA1. When the software sets this bit to 1, this module sets the expected value of the sequence toggle bit of the pipe in DATA1. This module always indicates SQSET = 0. Set the SQSET bit to 1 when CSCTS = 0 and PID = NAK. When setting this bit to 1 after changing the PID bits for the pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.
6	SQMON	0	R	Toggle Bit Check Indicates the expected value of the sequence toggle bit for the next transaction of the selected pipe. 0: DATA0 1: DATA1 If the pipe is not the isochronous transfer type, when a transaction is successfully processed, this module toggles this bit. However, when a DATA-PID mismatch occurs in the receive direction transfer, this bit is not toggled.
5	PBUSY	0	R	Pipe Busy Indicates whether the pipe is currently used in the USB bus or not. 0: The selected pipe is not used in the USB bus. 1: The selected pipe is being used in the USB bus. When this module starts the USB transaction for the selected pipe, this module sets this bit to 1. This module clears this bit to 0 upon completion of each transaction. After the software sets PID = NAK, read this bit to see if changing the pipe setting is enabled or not.
4 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
1, 0	PID[1:0]	00	R/W	Response PID Specify a response used in the next transaction for the selected pipe. 00: NAK response 01: BUF response (depending on buffer state) 10: STALL response 11: STALL response These bits are set to NAK by default. To perform USB transfer with the selected pipe, change the setting of these bits to BUF. Tables 33.11 and 33.12 show the basic operation (with no error in packets) of this module in each setting of the PID bits. When changing these bits from BUF to NAK by the software while the pipe is in USB communication, write 00 (NAK) to these bits and then check PBUSY = 1 to confirm that the USB transfer of the pipe entered the NAK state. However, when this module changed these bits to NAK, the software does not have to check the PBUSY bit. This module modifies these bits in the following cases. • When the pipe is in the receive direction and the software sets the SHTNAK bit of the selected pipe to 1, this module indicates PID = NAK when this module recognizes the transfer end. • When this module receives data with a payload exceeding the MaxPacketSize value for the pipe, this module indicates PID = STALL (11). • When this module detects a USB bus reset with the function control function selected, this module indicates PID = NAK. • When this module detects a CRC error or another receive error three times in a row with the host control function selected, this module indicates PID = NAK. • When this module receives a STALL handshake with the host control function selected, this module indicates PID = STALL (11). Set these bits as follows: • To change the state from NAK (00) to STALL, write 10. • To change the state from BUF (01) to STALL, write 11. • To change the state from STALL (11) to NAK, write 10 then 00. • To change the state from STALL to BUF, set these bits to NAK and then to BUF.

Notes: 1. Only reading 0 and writing 1 are enabled.
2. Only writing 1 is enabled.

Table 33.9 Operations of BSTS Bit

DIR Bit	BFRE Bit	DCLRM Bit	Meaning of BSTS Bit
0	0	0	Indicates 1 when the FIFO buffer becomes ready to read receive data from the buffer, and indicates 0 upon completion of the data read.
		1	Setting prohibited
	1	0	Indicates 1 when the FIFO buffer becomes ready to read receive data from the buffer, and indicates 0 when the software sets BCLR = 1 after the buffer data read.
		1	Indicates 1 when the FIFO buffer becomes ready to read receive data from the buffer, and indicates 0 upon completion of the data read.
1	0	0	Indicates 1 when the FIFO buffer becomes ready to write transmit data to the buffer, and indicates 0 upon completion of the data write.
		1	Setting prohibited
	1	0	Setting prohibited
		1	Setting prohibited

Table 33.10 Data Cleared by This Module when ACLRM = 1

No.	Data Cleared by the ACLRM Bit	Clearing Timing
1	All data in the FIFO buffer (both sides for double FIFO buffer) allocated to the pipe	
2	Interval count value when the pipe is isochronous transfer type	When resetting the interval count value
3	Internal flags related to the BFRE bit	When changing the BFRE setting
4	FIFO buffer toggle control	When changing the DBLB setting
5	Internal flags related to the transaction count	When forcibly terminating the transaction count function

Table 33.11 Operations of This Module in Each Setting of PID Bits (when the Host Controller Function is Selected)

PID Bits	Transfer Type	Transfer Direction (DIR Bit)	Operation of This Module
00 (NAK)	Independent of the setting	Independent of the setting	Issues no token.
01 (BUF)	Bulk or interrupt	Independent of the setting	Issues tokens when UACT = 1 is set and the FIFO buffer for the pipe is ready to receive/transmit. Issues no token when UACT = 0 is set or the FIFO buffer is not ready to receive/transmit.
	Isochronous	Independent of the setting	Issues tokens irrespective of the state of the FIFO buffer for the pipe.
10 (STALL) or 11 (STALL)	Independent of the setting	Independent of the setting	Issues no token.

Table 33.12 Operations of This Module in Each Setting of PID Bits (when the Function Controller Function is Selected)

PID Bits	Transfer Type	Transfer Direction (DIR Bit)	Operation of This Module
00 (NAK)	Bulk or interrupt	Independent of the setting	Sends a NAK response to a token from the USB host. However, for the operation of this module when ATREPM = 1, see the description on the ATREPM bit.
	Isochronous	Independent of the setting	Sends no response to a token from the USB host.
01 (BUF)	Bulk	Receive direction (DIR = 0)	Receives data and sends an ACK response to the OUT token from the USB host when the FIFO buffer for the pipe is ready to receive. Otherwise, sends a NAK response. Sends an ACK response to the PING token from the USB host when the FIFO buffer for the selected pipe is ready to receive. Otherwise, sends a NYET response.
	Interrupt	Receive direction (DIR = 0)	Receives data and sends an ACK response to the OUT token from the USB host when the FIFO buffer for the pipe is ready to receive. Otherwise, sends a NAK response.
	Bulk or interrupt	Transmit direction (DIR = 1)	Sends data in response to a token from the USB host when the FIFO buffer for the pipe is ready to transmit. Otherwise, sends a NAK response.
	Isochronous	Receive direction (DIR = 0)	Receives data in response to the OUT token from the USB host when the FIFO buffer for the pipe is ready to receive. Otherwise, ignores the data.
		Transmit direction (DIR = 1)	Sends data in response to a token from the USB host when the FIFO buffer for the pipe is ready to transmit. Otherwise, sends a Zero-Length packet.
10 (STALL) or	Bulk or interrupt	Independent of the setting	Sends a STALL response to a token from the USB host.
11 (STALL)	Isochronous	Independent of the setting	Sends no response to a token from the USB host.

(2) PIPEnCTR (n = 6 to 8 , 9 when the host controller function is selected)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BSTS	—	CSCLR	CSSTS	—	—	ACLRM	SQCLR	SQSET	SQMON	PBUSY	—	—	—	PID[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W*1	R/W	R	R	R/W	R/W*1	R/W*1	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	BSTS	0	R	Buffer Status Indicates the state of the FIFO buffer of the selected pipe. 0: The buffer is not accessible. 1: The buffer is accessible. The meaning of this bit differs as shown in Table 33.9 depending on the settings of the DIR, BFRE, and DCLRM bits.
14	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
13	CSCLR	0	R/W*1	CSPLIT Status Clear Setting this bit to 1 clears the CSSTS bit of the selected pipe. 0: Invalid 1: Clears the CSSTS bit. To forcibly restart the next transfer with S-SPLIT in data transfer using split transactions, set this bit to 1 by the software. Since this module automatically clears the CSSTS bit to 0 at the end of C-SPLIT in normal split transactions, the software does not have to clear the CSSTS bit. Control the CSSTS bit with this bit while communication is halted by clearing the UACT bit or when it is clarified that no data transfer is performed by detection of Detach mode. Even if this bit is set to 1 when CSSTS is 0, CSSTS remains 0. When the function controller function is selected, be sure to set this bit to 0.

Bit	Bit Name	Initial Value	R/W	Description
12	CSSTS	0	R/W	When the host controller function is selected, this bit indicates the C-SPLIT status of split transactions. 0: START-SPLIT (S-SPLIT) transaction is being processed or the transaction is transferred without split transaction. 1: C-SPLIT transaction is being processed. This module sets this bit to 1 when starting C-SPLIT, and clears this bit to 0 when C-SPLIT end is detected. When the function controller function is selected, the read value of this bit is invalid. This bit is valid only when the host controller function is selected.
11, 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	ACLRM	0	R/W	Buffer Auto-Clear Mode*3*4 Enables or disables buffer auto-clear mode for the selected pipe. 0: Buffer auto-clear mode is disabled. 1: Buffer auto-clear mode is enabled. (All buffers are initialized.) To completely delete the data in the FIFO buffer allocated to the pipe, write 1 and then 0 continuously to the ACLRM bit. Table 33.13 shows data cleared by this module when this bit is set to 1 and then 0 and cases where such data is cleared. Modify this bit when CSSTS = 0, PID = NAK, and the pipe is not set in the CURPIPE bits. When setting this bit to 1 after changing the PID bits for the pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.

Bit	Bit Name	Initial Value	R/W	Description
8	SQCLR	0	R/W*[1]	Toggle Bit Clear*[3]*[4] Set this bit to 1 to clear the expected value (in DATA0) of the sequence toggle bit for the next transaction of the selected pipe. 0: Invalid 1: The expected value is cleared in DATA0. When the software sets this bit to 1, this module sets the expected value of the sequence toggle bit of the pipe in DATA0. This module always indicates SQCLR = 0. When this bit is set to 1 for a Bulk-Out transfer pipe with the host controller function selected, this module starts the next transfer with the PING-token for the pipe. Set the SQCLR bit to 1 when CSCTS = 0 and PID = NAK. When setting this bit to 1 after changing the PID bits for the pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.
7	SQSET	0	R/W*[1]	Toggle Bit Set*[3]*[4] Set this bit to 1 to set the expected value of the sequence toggle bit for the next transaction of the selected pipe. 0: Invalid 1: The expected value is set in DATA1. When the software sets this bit to 1, this module sets the expected value of the sequence toggle bit of the selected pipe in DATA1. This module always indicates SQSET = 0. Set the SQSET bit to 1 when CSCTS = 0 and PID = NAK. When setting this bit to 1 after changing the PID bits for the selected pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.

Bit	Bit Name	Initial Value	R/W	Description
6	SQMON	0	R	Toggle Bit Check Indicates the expected value of the sequence toggle bit for the next transaction of the pipe. 0: DATA0 1: DATA1 If the selected pipe that is not the isochronous transfer type, when a transaction is successfully processed, this module toggles this bit. However, when a DATA-PID mismatch occurs in the receive direction transfer, this bit is not toggled.
5	PBUSY	0	R	Pipe Busy Indicates whether the selected pipe is currently used in the USB bus or not. 0: The selected pipe is not used in the USB bus. 1: The selected pipe is being used in the USB bus. When this module starts the USB transaction for the selected pipe, this module sets this bit to 1. This module clears this bit to 0 upon completion of each transaction. After the software sets PID = NAK, read this bit to see if changing the pipe setting is enabled or not.
4 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
1, 0	PID[1:0]	00	R/W	Response PID Specify a response used in the next transaction for the selected pipe. 00: NAK response 01: BUF response (depending on buffer state) 10: STALL response 11: STALL response These bits are set to NAK by default. To perform USB transfer with the selected pipe, change the setting of these bits to BUF. Tables 33.13 and 33.14 show the basic operation (with no error in packets) of this module in each setting of the PID bits. When changing these bits from BUF to NAK by the software while the pipe is in USB communication, write 00 (NAK) to these bits and then check PBUSY = 1 to confirm that the USB transfer of the selected pipe entered the NAK state. However, when this module changed these bits to NAK, the software needs not check the PBUSY bit. This module modifies these bits in the following cases. • When the selected pipe is in the receive direction and the software sets the SHTNAK bit of the selected pipe to 1, this module indicates PID = NAK when this module recognizes the transfer end. • When this module receives data with a payload exceeding the MaxPacketSize value for the pipe, this module indicates PID = STALL (11). • When this module detects a USB bus reset with the function control function selected, this module indicates PID = NAK. • When this module detects a CRC error or another receive error three times in a row with the host control function selected, this module indicates PID = NAK. • When this module receives a STALL handshake with the host control function selected, this module indicates PID = STALL (11). Set these bits as follows: • To change the state from NAK (00) to STALL, write 10. • To change the state from BUF (01) to STALL, write 11. • To change the state from STALL (11) to NAK, write 10 then 00. • To change the state from STALL to BUF, set these bits to NAK and then to BUF.

Notes: 1. Only reading 0 and writing 1 are enabled.
2. Only writing 1 is enabled.
3. Set the ACLRM, SQCLR, or SQSET bit when CSSTS = 0, PID = NAK, and the selected pipe is not set in the CURPIPE bits.
4. When setting the ACLRM, SQCLR, or SQSET bit after changing the PID bits from BUF to NAK, check that CSSTS = 0 and PBUSY = 0 for the pipe. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.

Table 33.13 Data Cleared by This Module when ACLRM = 1

No.	Data Cleared by the ACLRM Bit	Clearing Timing
1	All data in the FIFO buffer allocated to the selected pipe	
2	Interval count value when the host controller function is selected and the selected pipe is interrupt transfer type	When resetting the interval count value
3	Internal flags related to the BFRE bit	When changing the BFRE setting
4	Internal flags related to the transaction count	When forcibly terminating the transaction count function

33.3.36 Pipe n Transaction Counter Enable Register (PIPnTRE) (n = 1 to 5, and 9 to F when the function controller function is selected)

PIPnTRE enables or disables the transaction counter function and clears the counter for pipes 1 to 5, and 9 to F when the function controller function is selected.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	TRENB	TRCLR	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
9	TRENB	0	R/W	Transaction Counter Enable Enables or disables the transaction counter function. 0: The transaction counter function is disabled. 1: The transaction counter function is enabled. When the software sets the number of total packets in the TRNCNT bits in PIPEnTRN for the receive pipe and then sets this bit to 1, this module controls the following when it received the same number of packets as the setting of the TRNCNT bits. When continuous communication mode is used (CNTMD = 1), this module toggles the received data to the CPU even if the FIFO buffer is not full at the end of reception. When SHTNAK = 1, this module changes the PID bits for the corresponding pipe to NAK when this module received the same number of packets as the setting of the TRNCNT bits. When BFRE = 1, this module asserts the BRDY interrupt when this module received the same number of packets as the setting of the TRNCNT bits and read the receeive data completely. For transmit pipes, set this bit to 0. When the transaction counter function is not used, set this bit to 0. When using the transaction counter function, set the TRNCNT bits and then set this bit to 1. Furthermore, set this bit to 1 before receiving the first packet that is included in the transaction count range.
8	TRCLR	0	R/W	Transaction Counter Clear Clears the current count value of the transaction counter for the pipe and indicates TRCLR = 0. 0: Invalid 1: The current count value is cleared.
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Note: Change the bits in this register when CSSTS = 0 and PID = NAK.
When changing the bits in this register after changing the PID bits for the pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.

33.3.37 Pipe n Transaction Counter Register (PIPEnTRN) (n = 1 to 5, and 9 to F when the function controller function is selected)

PIPnTRE is a transaction counter for pipes 1 to 5, and 9 to F when the function controller function is selected.

This register is initialized by a power-on reset, but the setting of this register is retained through a USB bus reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TRNCNT[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description

Bit	Bit Name	Initial Value	R/W	Description
15 to 0	TRNCNT [15:0]	All 0	R/W	Transaction Counter Writing: Specify the number of transactions of DMA transfer. Reading: When TRENB = 0, the set number of transactions is indicated. When TRENB = 1, the number of current transactions is indicated. This module increments (+1) the value of these bits when the following conditions are all satisfied. TRENB = 1 TRCNT value ≠ current count value +1 when a packet is received. The payload of the received packet equals the value of the MXPS bits. This module clears these bits to 0 when any of the following is satisfied. When the following conditions are all satisfied - TRENB = 1 - TRCNT value = current count value +1 when a packet is received. - The payload of the received packet equals the value of the MXPS bits. When the following conditions are all satisfied - TRENB = 1 - A short packet is received. When the following conditions are all satisfied - TRENB = 1 - The software sets the TRCLR bit to 1.

Bit	Bit Name	Initial Value	R/W	Description
15 to 0	TRNCNT [15:0]	All 0	R/W	For transmit pipes, set these bits to all 0. When the transaction counter function is not used, set these bits to all 0. Change these bits when CSSTS = 0, PID = NAK, and TRENB = 0. When setting these bits to 1 after changing the PID bits for the pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK. When changing these bits, set TRCNT = 1 and then set TRENB = 1.

33.3.38 Device Address n Configuration Register (DEVADDn) (n = 0 to A)

DEVADDn specifies the address and port number of the HUB connected to a peripheral device as a communication target, as well as the transfer rate of the peripheral device, for pipes 0 to 9, and A to F when the function controller function is selected.

When the host controller function is selected, be sure to set the bits in this register before starting communication for each pipe.

Change the bits in this register when there is no valid pipe that uses the setting of these bits. A valid pipe is defined as a pipe that meets the following two conditions.

1. The setting of the DEVSEL bits specifies this register.
2. The PID bits for the selected pipe are set to BUF or the selected pipe is the DCP with SUREQ = 1

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	UPPHUB[3:0]				HUBPORT[2:0]			USBSPD[1:0]		—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14 to 11	UPPHUB [3:0]	0000	R/W	HUB Register Specify the USB address of the HUB connected to the peripheral device as a communication target. 0000: The peripheral device is connected directly to the port of this LSI. 0001 to 1010: USB address of the HUB 1011 to 1111: Setting prohibited When the host controller function is selected, this module reads these bits to generate packets when executing split transactions. When the function controller function is selected, set these bits to 0000.

Bit	Bit Name	Initial Value	R/W	Description
10 to 8	HUBPORT [2:0]	000	R/W	HUB Port for Communication Target Device Specify the port number of the HUB connected to the peripheral device as a communication target. 000: The peripheral device is connected directly to the port of this LSI. 001 to 111: Port number of the HUB When the host controller function is selected, this module reads these bits to generate packets when executing split transactions. When the function controller function is selected, set these bits to 000.
7, 6	USBSPD [1:0]	00	R/W	Communication Target Device Transfer Rate Specify the USB transfer rate of the peripheral device as a communication target. 00: DEVADDn is not used. 01: Low speed 10: Full speed 11: High speed When the host controller function is selected, this module reads these bits to generate packets. When the function controller function is selected, set these bits to 00.
5 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

33.4 Operation

33.4.1 System Control and Oscillation Control

This section describes register operations required for the initial settings of this module and the registers required for the power consumption control.

(1) Reset

Table 33.14 lists the reset types of this module. For initialization states of registers after each reset, see section 33.3, Register Descriptions.

Table 33.14 Reset Types

Reset Name	Operation
Power-on reset	RESETP pin
AP system reset	RESETA pin
Power area reset	Register in the SYSC
Software reset	Register in the CPGA

(2) Setting Selection of Controller Functions

This module can select the host controller function or the function controller function. Select either of these functions by the DCFM bit in SYSCFG. Set the DCFM bit during the initial setting immediately after a power-on reset or in the D+ pull-up disabled state (DPRPU = 0) and D+/D- pull-down disabled state (DRPD = 0).

(3) Enabling High-Speed Operation

This module can set the USB transmission rate (communication bit rate) by the software.

When the host controller function is selected, high-speed operation or full-speed/low-speed operation is selectable. When the function controller function is selected, high-speed operation or full-speed operation is selectable. To enable high-speed operation with this module, set the HSE bit in SYSCFG to 1. When high-speed operation is enabled, this module executes the reset handshake protocol and automatically sets the USB transmission rate. The reset handshake result can be checked by the RHST bits in DVSTCTR.

When high-speed operation is disabled, this module operates in full speed or low speed when the host controller function is selected, and operates only in full speed when the function controller function is selected.

When the host controller function is selected, change the HSE bit during a period from ATTACH detection until a bus reset. When the host controller function is selected, change the HSE bit in the D+ pull-up disabled state (DPRPU = 0).

(4) USB Data Bus Resistor Control

Figure 33.1 shows the connection between this module and the USB connector.

This module incorporates a pull-up resistor of the D+ signal and pull-down resistors of the D+ and D- signals. Specify pull-up and pull-down for each signal using the DPRPU and DRPD bits in SYSCFG.

Furthermore, this module controls the terminating resistors of the D+ and D- signals in high-speed operation, and the output resistors in full-speed operation. This module automatically switches the on-chip resistors after connection to the host controller or the peripheral device upon detecting a reset handshake, suspended state, or resume.

When the function controller function is selected and the DPRPU bit in SYSCFG is set to 0 during communication with the host controller, this module disables the pull-up resistors (or terminating resistors) of the USB data line. Therefore, the USB host can be notified of a disconnection from the device.

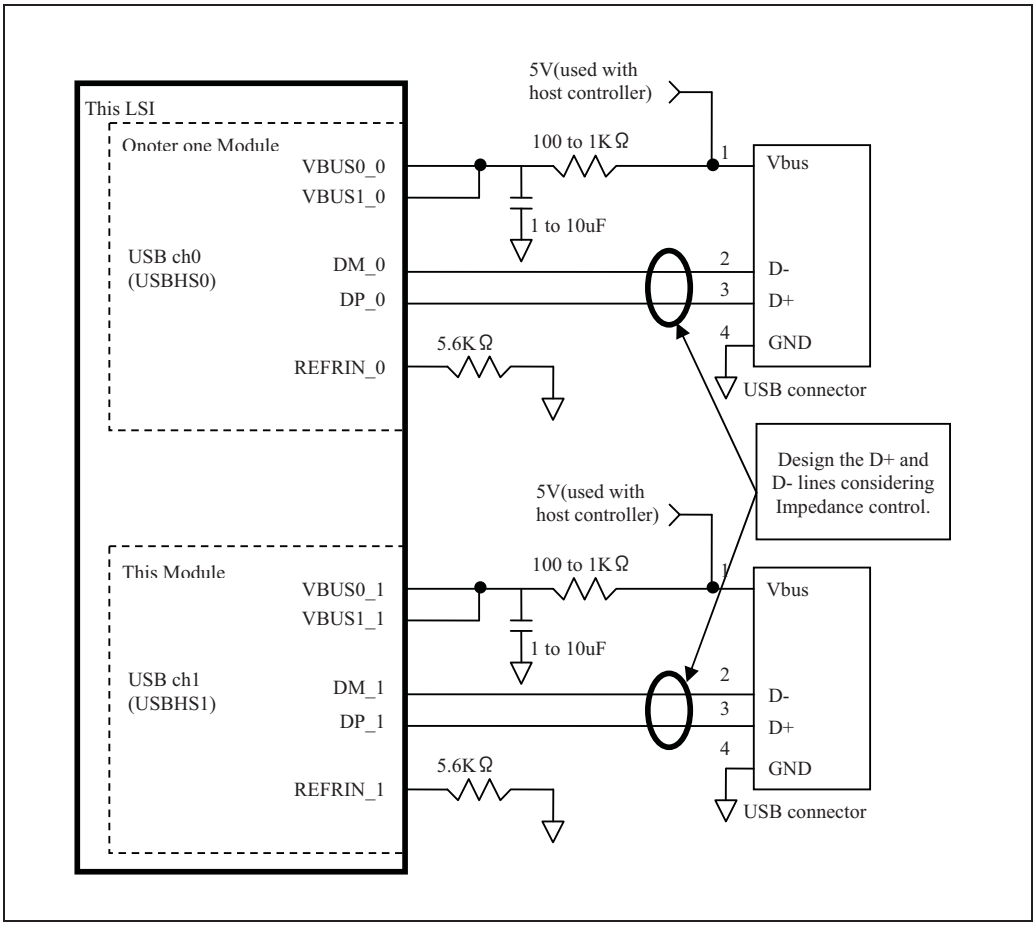


Figure 33.1 Connection to the USB Connector

(5) Software reset when the USB disconnection is detected

Issue a software reset of the USBHS module when the USB disconnection is detected. If the DMA interface is being used, issue a software reset of the USBHS-DMAC module as well. A software reset can be issued via a register in the CPGA.

Whether or not the USB disconnection is detected can be determined by the VBSTS in the INTSTS0 register when the function controller function is selected or the DTCH bit in the INTSTS1 register when the host controller function is selected.

33.4.2 Interrupt Function

Table 33.15 lists the interrupt generating conditions of this module.

When any of the following interrupt generating conditions are satisfied and the interrupt output is enabled by the corresponding interrupt enable register, this module outputs a USB interrupt request to the interrupt controller (INTC).

Table 33.15 Interrupt Generating Conditions

Bit	Interrupt Name	Interrupt Generating Conditions	Function	Related Status
VBINT	VBUS interrupt	When VBUS0_1 and VBUS1_1 input pin state change is detected (both L to H and H to L)	Host and function controller functions	VBSTS
RESM	Resume interrupt	When a USB bus state change is detected in the suspended state (J-State to K-State or J-State to SE0)	Function	—
SOFR	Frame number update interrupt	[When the host controller function is selected] When an SOF packet with a different frame number is sent [When the function controller function is selected] SOFRM = 0: When an SOF packet with a different frame number is received SOFRM = 1: When an SOF packet with a μ frame number of 0 cannot be received due to damage, etc.	Host and function controller functions	—
DVST	Device state transition interrupt	When a device state transition is detected USB bus reset detected Suspended state detected SET_ADDRESS request received SET_CONFIGURATION request received	Function	DVSQ

Bit	Interrupt Name	Interrupt Generating Conditions	Function	Related Status
CTRT	Control transfer stage transition interrupt	When a control transfer stage transition is detected	Function	CTSQ
		Setup stage completed		
		Control write transfer status stage shifted		
		Control read transfer status stage shifted		
		Control transfer completed		
		Control transfer sequence error occurred		
BEMP	Buffer empty interrupt	When the buffer becomes empty after sending all buffer memory data	Host and function controller functions	BEMPSTS.PIPEBEMP
		When a packet with a size exceeding the maximum packet size is received		
NRDY	Buffer not ready interrupt	[When the host controller function is selected]	Host and function controller functions	NRDYSTS.PIPENRDY
		When STALL from the peripheral device in response to the issued token is received		
		When a response from the peripheral device in response to the issued token cannot be received successfully (no response three times in a row or a packet receive error three times in a row)		
		When an overrun or underrun error occurred during isochronous transfer		
		[When the function controller function is selected]		
		When NAK is sent in response to IN token, OUTtoken, or PING token		
		When a CRC error or bit stuffing error occurred during data reception in isochronous transfer		
		When an overrun or underrun error occurred during data reception in isochronous transfer		

Bit	Interrupt Name	Interrupt Generating Conditions	Function	Related Status
BRDY	Buffer ready interrupt	When the buffer becomes ready for reading or writing	Host and function controller functions	BRDYSTS. PIPEBRDY
OVRCR	OVRCR interrupt	When an OVCN_1/OVCN2_1 input pin state change is detected	Host and function controller functions	OVCMON
BCHG	Bus change interrupt	When a USB bus state change is detected	Host and function controller functions	—
DTCH	Disconnection in full-speed operation	When a disconnection from the peripheral device is detected during full-speed operation	Host controller function	—
ATTCH	Device connection	When J-STATE or K-STATE where USB bus state continues for 2.5 μs is detected This interrupt is available for detection of connection to a peripheral device.	Host controller function	—
EOFERR	EOF error	When an EOF error of the peripheral device is detected	Host controller function	—
SACK	SETUP	When an ACK response to the setup transaction is received	Host controller function	—
SIGN	SETUP error	When an error (no response or ACK packet damage) is detected three times in a row in the setup transaction	Host controller function	—

Note: These bits in this table are those of INTSTS0 if any register's name is not indicated.

Figure 33.2 shows a block diagram of the interrupt circuit of this module.

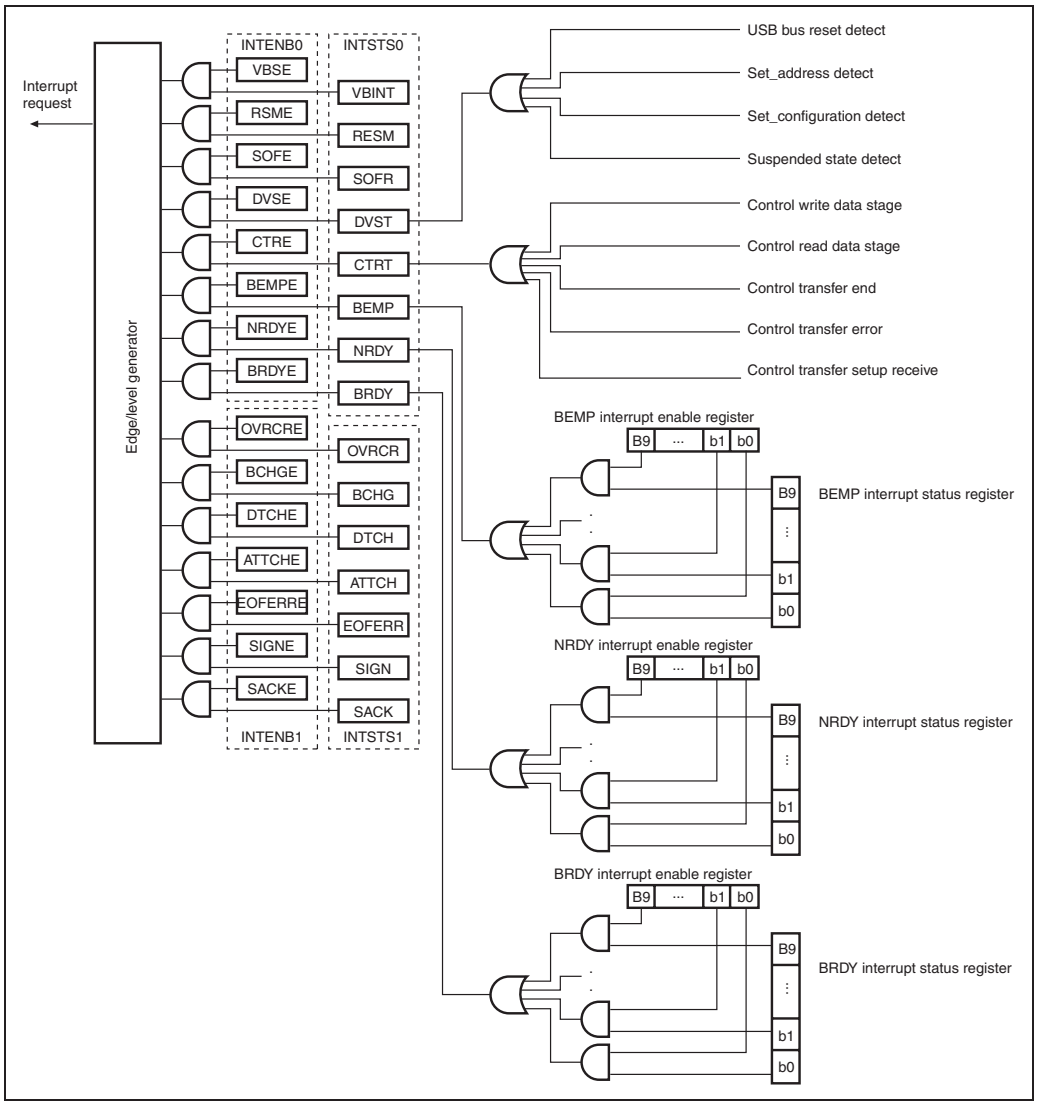


Figure 33.2 Block Diagram of Interrupt Circuit

(1) BRDY Interrupt

A BRDY interrupt can be generated when either of the host controller function and function controller functions is selected. When the following conditions in each pipe are satisfied, this module sets the corresponding bit in BRDYSTS to 1. At this time, when the PIPEBRDYE bit for the pipe in BRDYENB is set to 1 and the BRDYE bit in INTENB0 is set to 1 by the software, this module generates a BRDY interrupt.

BRDY interrupt generating conditions and clearing method depend on the settings of the BRDYM bit and the BFRE bit for each pipe.

(a) When BRDY interrupt disable (BRDYM = 0) and BRDY interrupt output enable (BFRE = 0) at data reception/transmission are specified

With this setting, a BRDY interrupt indicates that the FIFO port is accessible.

This module generates an internal BRDY interrupt request trigger when the following conditions are satisfied, and sets the PIPEBRDY bit corresponding to the request trigger pipe to 1.

1. Pipes set for the transmit direction

- When the software changes the DIR bit from 0 to 1
- When this module finishes sending a packet of the pipe while data write from the CPU to the FIFO buffer allocated to the pipe is disabled (BSTS = 0)

  When continuous communication mode is selected, this module generates a BRDY interrupt request trigger upon completion of sending data for one side of the FIFO buffer.
- When a double FIFO buffer is specified and one side of the FIFO buffer is empty when data write to the other side of the FIFO buffer is completed

  Even if one side of the FIFO buffer becomes empty while the other side is in data write processing, no BRDY interrupt is generated until the ongoing data write finishes.
- When this module generates a buffer flush for a pipe of isochronous transfer type
- When the FIFO buffer becomes write enable state by writing 1 to the ACLRM bit

No BRDY interrupt request trigger is generated for the DCP (in data transmission of control transfer).

2. Pipes set for the receive direction

- When this module receives a packet successfully and the FIFO buffer becomes ready for reading while data read access from the CPU to the FIFO buffer allocated to the pipe is disabled (BSTS = 0)

  No BRDY interrupt request trigger is generated in transactions with incorrect data PID.

  When continuous communication mode is selected, no BRDY interrupt request trigger is generated for packets with a MaxPacketSize data size and when the FIFO buffer still has available space.

  When this module receives a short packet, this module generates a BRDY interrupt request trigger even if the buffer has available space.

  When a transaction counter is used, this module generates a BRDY interrupt request trigger when this module receives a packet with a size of the set value even if the FIFO buffer still has available space.

  When a double FIFO buffer is specified and one side of the FIFO buffer is ready for reading when data read from the other side of the FIFO buffer is completed

  Even if data read for one side of the FIFO buffer is completed while the other side is undergoing data read, no BRDY interrupt request trigger is generated until the ongoing data read finishes.

This interrupt is not generated in communication in the control transfer status stage when the function controller function is selected.

The software can clear the PIPEBRDY interrupt status of the pipe by writing 0 to the PIPEBRDY bit for the pipe in BRDYSTS. At this time, write 1 to the bits corresponding to other pipes.

Be sure to clear the BRDY interrupt status before accessing the FIFO buffer.

(b) When BRDY interrupt disable (BRDYM = 0) and BRDY interrupt output enable (BFRE = 1) at the end of data read are specified

With this setting, this module determines that a **BRDY** interrupt is generated upon completion of reading all data of one transfer in a receive pipe, and sets the bit for the pipe in this register to 1.

This module determines that the last data of a transfer was received in either of the following cases.

- A Zero-Length packet or another short packet is received.
- A transaction counter (TRNCNT bits) is used and a packet with a size of the value of the TRNCNT bits is received.

When either of these conditions is satisfied and the data read is completed, this module determines that reading all data for one transfer is completed.

When this module receives a Zero-Length packet with the FIFO buffer empty, this module determines that reading all data for one transfer is completed when the Zero-Length packet data is toggled to the CPU. In this case, write 1 to the BCLR bit in the corresponding FIFOCTR register by the software to start the next transfer.

With this setting, this module generates no BRDY interrupt for transmit pipes.

The software can clear the PIPEBRDY interrupt status of the pipe to 0 by writing 0 to the PIPEBRDY bit for the pipe. At this time, write 1 to the bits corresponding to other pipes.

When using this mode, do not change the BFRE setting until the processing for one transfer is completed.

To change the BFRE bit during processing, clear all FIFO buffers for the pipe by the ACLRM bit.

(c) When BRDY interrupt enable (BRDYM = 1) and BRDY interrupt output enable (BFRE = 0) at data reception/transmission are specified

With this setting, the value of the PIPEBRDY bit varies with the value of the **BSTS** bit for each pipe. That is, this module indicates 1 or 0 of the BRDY interrupt status according to the FIFO buffer status.

1. Pipes set for the transmit direction
   When the FIFO port is ready to write data, the PIPEBRDY bit indicates 1. When the FIFO port is not ready to write data, the PIPEBRDY bit indicates 0.
   However, even if the transmit pipe of the DCP is ready to write data, no BRDY interrupt is asserted.
2. Pipes set for the receive direction
   When the FIFO port is ready to read data, the PIPEBRDY bit indicates 1. When all data is read from the FIFO port (reading disabled), the PIPEBRDY bit indicates 0.
   When this module receives a Zero-Length packet with the FIFO buffer empty, this module indicates 1 with the corresponding bit until 1 is written to BCLR by the software, and continues to assert the BRDY interrupt.

   With this setting, the software cannot clear the PIPEBRDY bit to 0.
   When BRDYM = 1, set the BFRE bit to 0 for all pipes.

Figure 33.3 shows the BRDY interrupt generation timing.

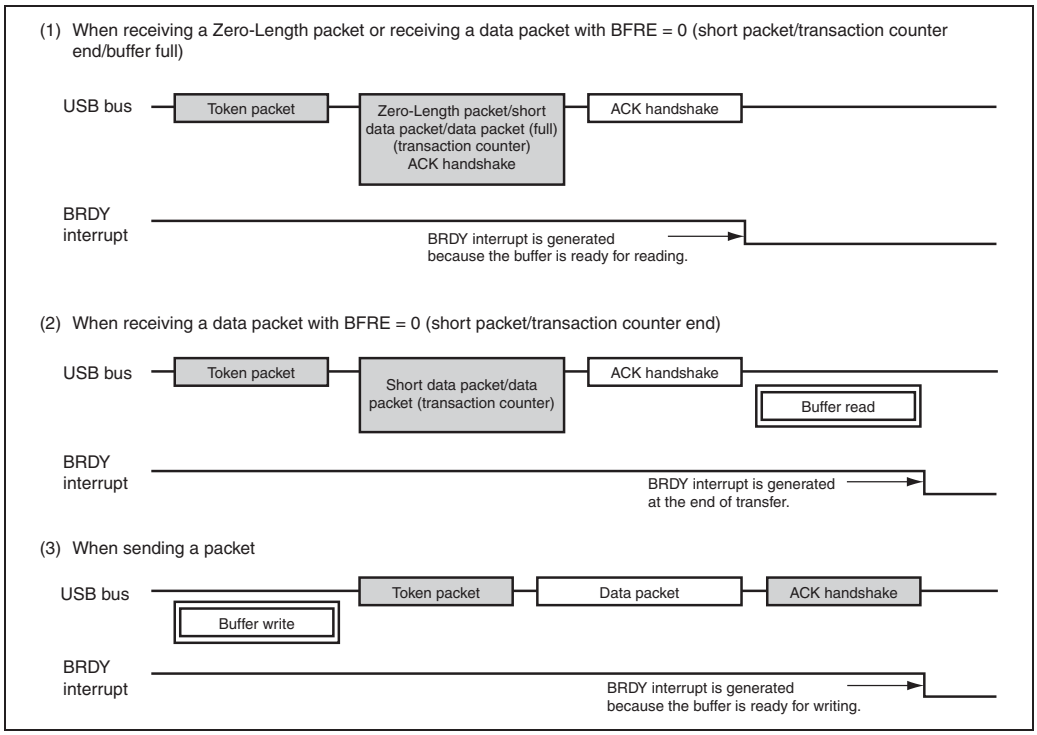


Figure 33.3 BRDY Interrupt Generation Timing

(2) NRDY Interrupt

When this module generates an internal NRDY interrupt request for the pipe in which PID = BUF is set by the software, this module indicates PIPENRDY = 1 for the pipe in NRDYSTS. At this time, when 1 is set in the corresponding bit in NRDYENB by the software, this module indicates NRDY = 1 in INTSTS0 and generates a USB interrupt.

The following shows the conditions for this module to generate an internal NRDY interrupt request for a pipe.

However, the execution of the SETUP transaction when the host controller function is selected is excluded from the following interrupt generation conditions. In the SETUP transaction when the host controller function is selected, this module detects an SACK interrupt or SIGN interrupt.

Furthermore, when executing the control transfer status stage with the function controller function selected, this module generates no interrupt request.

(a) When the host controller function is selected and no split transaction occurs

1. Pipes in the transmit direction

   This module detects an NRDY interrupt when either of the following conditions is satisfied.

   — When the OUT token transmit timing comes with no transmit data in the FIFO buffer in an isochronous transfer-type pipe

   At this time, this module sends a Zero-Length packet following the OUT token, and then indicates PIPENRDY = 1 for the pipe and OVRN = 1.

   — In communication other than SETUP transaction for a pipe of other than isochronous transfer type, when no response from the peripheral device (timeout is detected without detecting a handshake packet from the peripheral device) or an error in a packet from the peripheral device occurred three times in a row in an arbitrary combination

   At this time, this module indicates PIPENRDY = 1 for the pipe and changes the PID bits for the pipe to NAK.

   — When this module receives a STALL handshake from the peripheral device in communication other than the SETUP transaction (including STALL to PING as well as STALL to OUT)

   At this time, this module indicates PIPENRDY = 1 for the pipe and changes the PID bits for the pipe to STALL (11).

2. Pipes in the receive direction
   — When the IN token transmit timing comes with the FIFO buffer occupied in an isochronous transfer-type pipe

     At this time, this module ignores the receive data in response to the IN Token and indicates PIPENRDY = 1 for the pipe and OVRN = 1.

     Furthermore, when a packet error is detected in the receive data in response to the IN Token, this module also indicates CRCE = 1.

     In communication for a pipe of other than isochronous transfer type, when no response from the peripheral device to the IN token sent from this module (timeout is detected without detecting a data packet from the peripheral device) or an error in a packet from the peripheral device occurred three times in a row in an arbitrary combination

     At this time, this module indicates PIPENRDY = 1 for the pipe and changes the PID bits for the pipe to NAK.

     In communication for an isochronous transfer-type pipe, when this module receives no response from the peripheral device to the IN token sent from this module (timeout is detected without detecting a data packet from the peripheral device) or an error in a packet from the peripheral device is detected

     At this time, this module indicates PIPENRDY = 1 for the pipe but does not change the PID bits for the pipe.
   — In communication for an isochronous transfer-type pipe, when a CRC error or a bit stuffing error is detected in the received data packet

     At this time, this module indicates PIPENRDY = 1 for the pipe and CRCE = 1.
   — When this module receives a STALL handshake

     At this time, this module indicates PIPENRDY = 1 for the pipe and changes the PID bits for the pipe to STALL.

(b) When the host controller function is selected and split transactions occur

1. Pipes in the transmit direction
   — When the OUT token transmit timing comes with no transmit data in the FIFO buffer in an isochronous transfer-type pipe

     At this time, this module indicates PIPENRDY = 1 for the pipe and OVRN = 1 when it sends the Start-Split transaction (S-SPLIT). This module also sends a Zero-Length packet following the OUT token.
   — In the S-SPLIT or Complete-Sprit transaction (C-SPLIT) for a pipe of other than isochronous transfer type, when no response from the HUB (timeout is detected without detecting a handshake packet from the HUB) or an error in a packet from the HUB occurred three times in a row in an arbitrary combination

At this time, this module indicates PIPENRDY = 1 for the pipe and changes the PID bits for the pipe to NAK.

When this module detects an NRDY interrupt when sending C-SPLIT, this module clears the CSSTS bit to 0.

— When this module receives a STALL handshake in response to C-SPLIT

At this time, this module indicates PIPENRDY = 1 for the pipe and changes the PID bits for the pipe to STALL (11). This module also clears the CSSTS bit to 0.

However, this interrupt is not detected in the SETUP transaction.

— When this module receives NYET in response to C-SPLIT with microFrame = 4 in an interrupt transfer-type pipe

— At this time, this module indicates PIPENRDY = 1 for the pipe and clears the CSSTS bit to 0 but does not change the PID bits for the pipe.

2. Pipes in the receive direction

— When the IN token transmit timing comes with the FIFO buffer occupied in an isochronous transfer-type pipe

At this time, this module indicates PIPENRDY = 1 for the pipe and OVRN = 1 when it sends S-SPLIT. This module also ignores the receive data in response to the IN token.

— In a transfer for a bulk transfer-type pipe or in a transfer other than the SETUP transaction of the DCP, when no response from the HUB in response to the IN token from this module when sending S-SPLIT or C-SPLIT (timeout is detected without detecting a handshake packet from the HUB) or an error in a packet from the HUB occurred three times in a row in an arbitrary combination

At this time, this module indicates PIPENRDY = 1 for the pipe and changes the PID bits for the pipe to NAK. When this condition is generated in the C-SPLIT transaction, this module clears the CSSTS bit to 0.

— In the C-SPLIT transaction for a pipe of isochronous or interrupt type, when no response from the HUB in response to the IN token from this module (timeout is detected without detecting a data packet from the HUB) or an error in a packet from the HUB occurred three times in a row in an arbitrary combination

When this condition is generated in an interrupt transfer-type pipe, this module indicates PIPENRDY = 1 for the pipe, changes the PID bits for the pipe to NAK, and clears the CSSTS bit to 0.

When this condition is generated in an isochronous transfer-type pipe, this module indicates PIPENRDY = 1 for the pipe and CRCE = 1 and clears the CSSTS to 0, bit to 0 but does not change the PID bits for the pipe.

— When this module receives a STALL handshake response during the C-SPLIT transaction in a pipe of other than isochronous transfer type

At this time, this module indicates PIPENRDY = 1 for the pipe, changes the PID bits for the pipe to STALL (11), and clears the CSSTS bit to 0.

— When this module receives a NYET in response to C-SPLIT with microFrame = 4 in a pipe of isochronous or interrupt transfer type

At this time, this module indicates PIPENRDY = 1 for the pipe and CRCE = 1 and clears the CSSTS bit to 0, but does not change the PID bits for the pipe.

(c) When the function controller function is selected

1. Pipes in the transmit direction

— When this module receives an IN token with no transmit data in the FIFO buffer

This module generates an NRDY interrupt request and indicates PIPENRDY = 1.

When the pipe in which the interrupt is generated is isochronous transfer type, this module sends a Zero-Length packet and indicates OVRN = 1.

2. Pipes in the receive direction pipe

— When this module receives an OUT token with the FIFO buffer occupied

When the pipe in which the interrupt is generated is isochronous transfer type, this module generates an NRDY interrupt request when this module receives an OUT token, and indicates PIPENRDY = 1 and OVRN = 1.

When the pipe in which the interrupt is generated is not isochroous transfer type, this module generates an NRDY interrupt request when this module sends an NAK handshake response after receiving data following the OUT token, and indicates PIPENRDY = 1.

However, this module generates no NRDY interrupt when resending data (in the case of DATA-PID mismatch) or when an error occurs in a data packet.

— When this module receives a PING token with the FIFO buffer occupied

This module generates an NRDY interrupt request when this module receives a PING token and indicates PIPENRDY = 1.

— When a packet is not received correctly within the interval frame in an isochroous transfer-type pipe

This module generates an NRDY interrupt request when this module receives SOF and indicates PIPENRDY = 1.

Figure 33.4 shows the NRDY interrupt generation timing when the function controller function is selected.

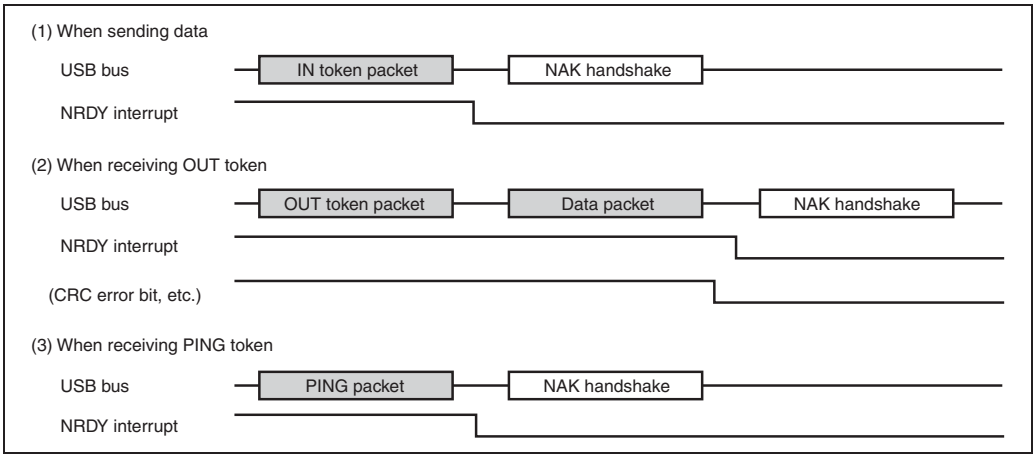


Figure 33.4 NRDY Interrupt Generation Timing when the Function Controller Function is Selected

(3) BEMP Interrupt

When this module detects a BEMP interrupt for the pipe in which PID = BUF is set by the software, this module indicates PIPEBEMP = 1 for the pipe in BEMPSTS. At this time, when 1 is set in the corresponding bit in BEMPENB by the software, this module indicates BEMP = 1 in INTSTS0 and generates a USB interrupt.

This module generates an internal BEMP interrupt request in the following cases.

1. Transmit direction pipes

   When the FIFO buffer for the pipe is empty at the end of transmission (including transmission of a Zero-Length packet)

   When single buffer is set for the FIFO buffer, this module generates an internal BEMP interrupt request concurrently with a BRDY interrupt for pipes other than DCP.
   However, this module generates no internal BEMP interrupt request in the following cases.

   — In the case of double buffer, when the software (DMAC) already started writing data to the FIFO buffer of the CPU at the end of transmission for one-side data
   — When the buffer is cleared (empty) by writing 1 to the ACLRM or BCLR bit.
   — When sending a Zero-Length packet (IN transfer) of the control transfer status stage when the function controller function is selected

2. Receive direction pipes

   When this module receives a packet with a data size exceeding the MaxPacketSize value

   In this case, this module generates a BEMP interrupt request and indicates the PIPEBEMP = 1 for the pipe, ignores the received data, and changes the PID bits for the pipe to STALL (11).

   At this time, this module sends no response when the host controller function is selected, and sends a STALL response when the function controller function is selected.

   However, this module generates no BEMP interrupt request in the following cases.

   — When this module detects a CRC error or bit stuffing error in the receive data

   — When executing the SETUP transaction

   Writing 0 to the PIPEBEMP bits clears the status.

   Writing 0 to the PIPEBEMP bits has no effect on the operation of this module.

Figure 33.5 shows the BEMP interrupt generation timing when the function controller function is selected.

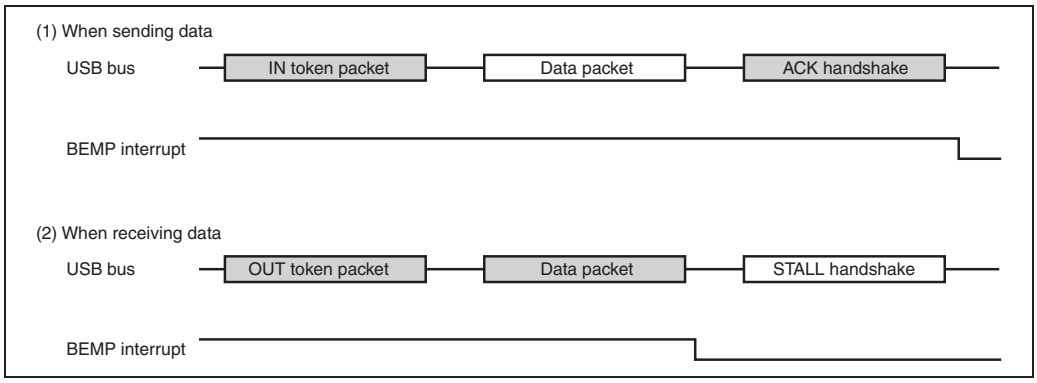


Figure 33.5 BEMP Interrupt Generation Timing when the Function Controller Function is Selected

(4) Device State Transition Interrupt

Figure 33.6 shows the device state transitions of this module. This module controls device states and generates device state transition interrupts. However, when returning from the suspended state (detecting the resume signal), this module detects the transition with a resume interrupt. The device state transition interrupt is enabled or disabled by setting INTENB0. The current device state can be monitored using the DVSQ bits in INTSTS0.

When this module shifts to the default state, a device state transition interrupt occurs after executing the reset handshake protocol.

This module controls the device states only when the function controller function is selected. In addition, device state transition interrupts are generated only when the function controller function is selected.

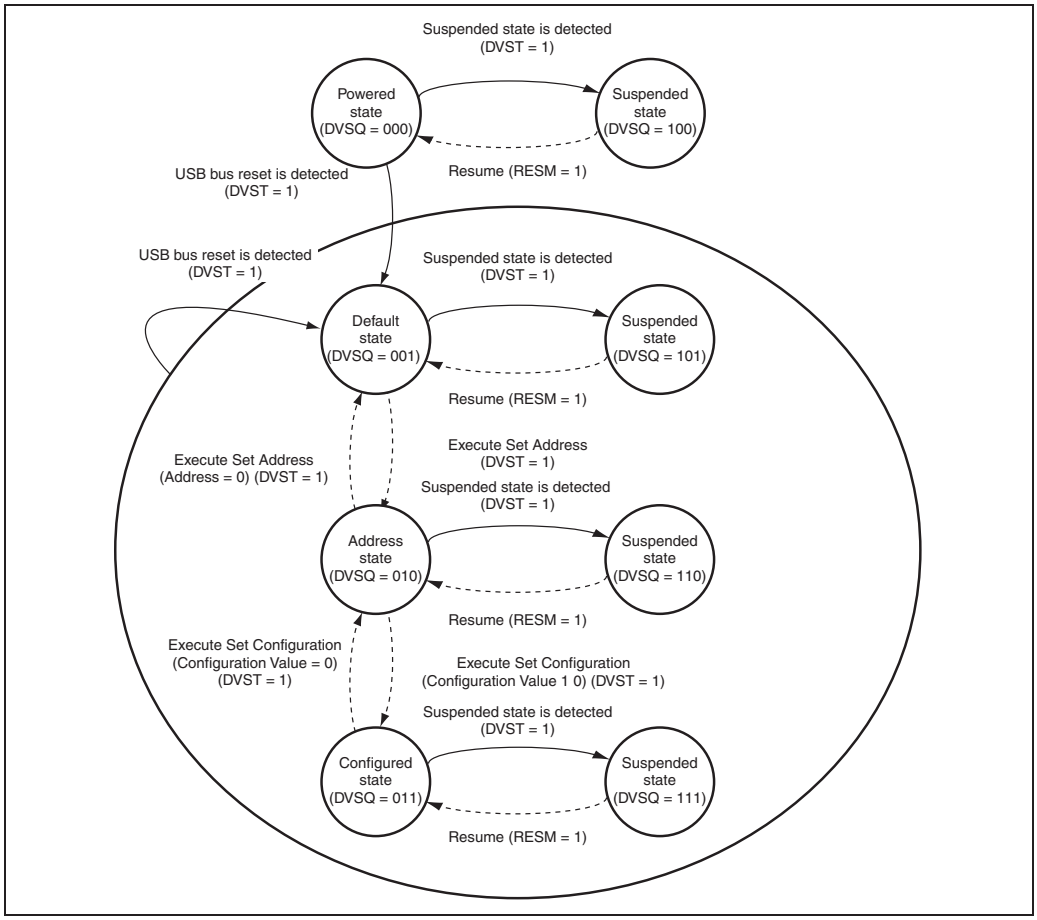


Figure 33.6 Device State Transitions

(5) Control Transfer Stage Transition Interrupt

Figure 33.7 shows control transfer stage transitions of this module. This module manages the sequence of control transfers and generates control transfer stage transition interrupts. Enabling or disabling each control transfer stage transition interrupt can be set by INTENB0. The current transfer stage after transition can be checked by the CTSQ bits in INTSTS0.

Control transfer stage transition interrupts are generated only when the function controller function is selected.

The following describes control transfer sequence errors. When an error occurs, the PID bits in DCPCTR indicate B'1x (STALL response).

1. Control read transfer
   - This module receives an OUT or PING token in response to the IN token in the data stage before starting data transfer.
   - This module receives an IN token in the status stage.
   - This module receives a packet with a data packet of DATAPID = DATA0 in the status stage.
2. Control write transfer
   - This module receives an IN token in response to the OUT token in the data stage before sending an ACK response.
   - This module receives a packet with the first data packet of DATAPID = DATA0.
   - This module receives an OUT or PING token in the status stage.
3. Control write no-data control transfer
   - This module receives an OUT or PING token in the status stage.

If the size of the receive data exceeds the wLength value of the USB request in the control write transfer data stage, this is not treated as a control transfer sequence error. This module sends ACK for normal end in response to a packet other than Zero-Length packet in the control read transfer status stage.

When a CTRT interrupt is generated (SERR = 1) due to a sequence error, CTSQ = 110 is retained until the interrupt status is cleared (CTRT = 0) by the system. For this reason, while CTSQ = 110, even if a new USB request is received, a CTRT interrupt at the end of the setup stage is not generated. (This module retains the setup stage end status and generates a setup stage end interrupt after the interrupt status is cleared by the software.)

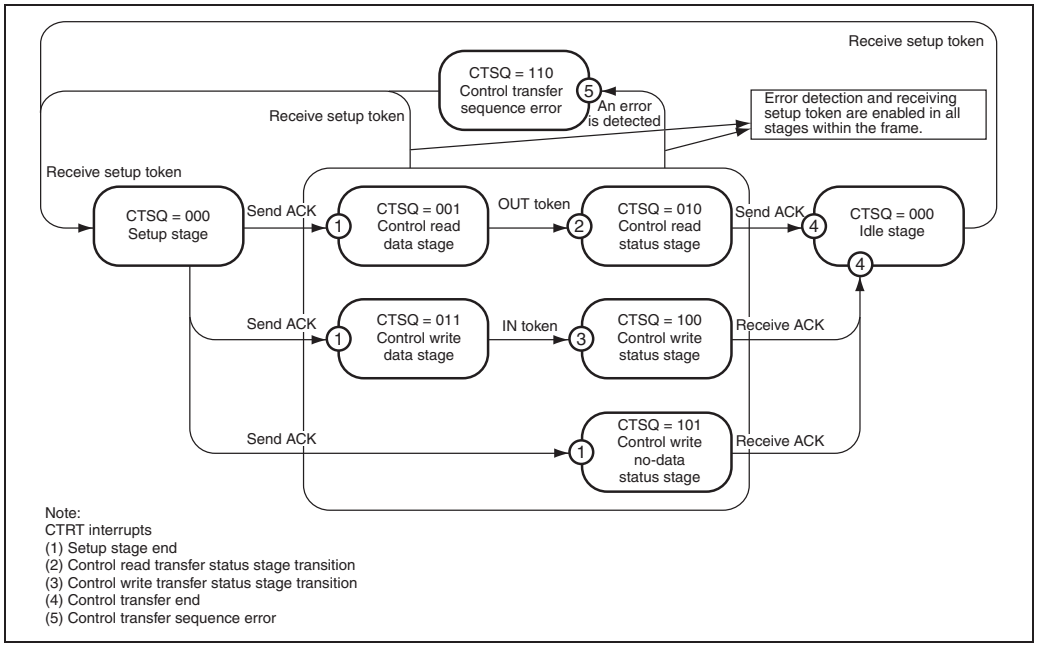


Figure 33.7 Control Transfer Stage Transitions

(6) Frame Update Interrupt

Figure 33.8 shows an example of the SOFR interrupt output timing of this module.

When the host controller function is selected, an SOFR interrupt is generated at the frame number update timing. When the function controller function is selected, an SOFR interrupt is generated immediately after the frame number is updated.

When this module detects a new SOF packet during the full-speed operation with the function controller function selected, this module updates the frame number and generates an SOFR interrupt. In the high-speed operation, however, the frame number is not updated or no SOFR interrupt is generated unless the module enters the μ SOF lock state. Furthermore, the SOF interpolation function is not activated. The μ SOF lock state occurs when this module receives a μ SOF packet twice in a row with different frame numbers without an error.

The μ SOF lock monitoring start and stop conditions are as follows:

1. µ SOF lock monitoring start conditions
   USBE = 1
2. µ SOF lock monitoring stop conditions
   USBE = 0, receiving USB bus reset, or detection of suspended state

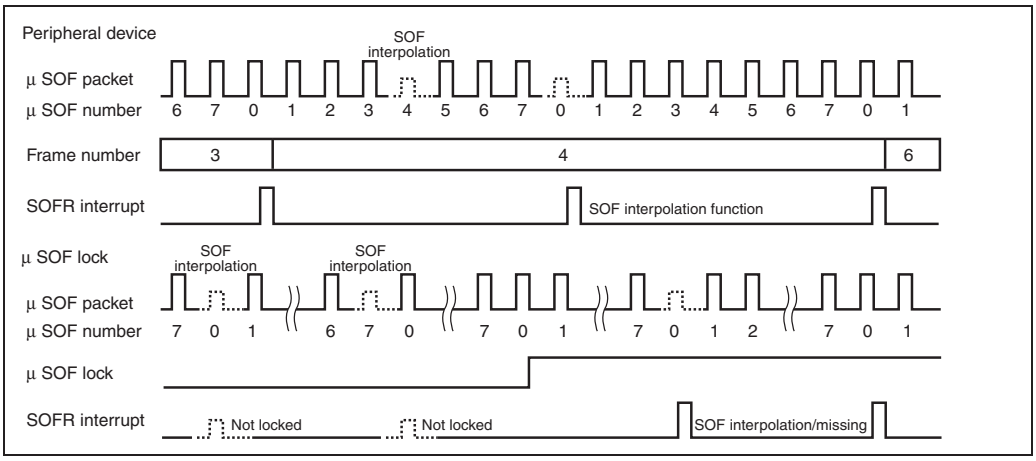


Figure 33.8 Example of SOFR Interrupt Output Timing

(7) VBUS Interrupt

When the VBUS pin state changes, a VBUS interrupt is generated. The VBUS pin level can be checked by the VBSTS bit in INTSTS0. The VBUS interrupt is used to check connection or disconnection to/from the host controller. However, when the system starts up with the host controller connected, the VBUS pin state remains unchanged, and therefore the first VBUS interrupt is not generated.

(8) Resume Interrupt

When the function controller function is selected and the USB bus state changes (J-State to K-State or J-State to SE0) with the device state suspended, a resume interrupt is generated. The resume interrupt is used to detect the return from the suspended state.

When the host controller function is selected, no resume interrupt is generated. Use the BCHG interrupt to detect a change in the USB bus state.

(9) BCHG Interrupt

When the USB bus state changes, a BCHG interrupt is generated. This interrupt is used to detect connection to a peripheral device and to detect remote wakeup when the host controller function is selected. This interrupt occurs when either of the host controller function or function controller function is selected.

(10) DTCH Interrupt

When a disconnection of the USB bus is detected with the host controller function selected, a DTCH interrupt is generated. This module detects a bus disconnection conforming to the USB Specification 2.0.

After detecting a DTCH interrupt, this module performs the following hardware control irrespective of the setting of the corresponding interrupt enable bit. The software must terminate the communication of all pipes with the port and drive this module into the state of waiting for connection to the port (ATTCH interrupt is generated).

- Change the UACT bit of the port that detected the DTCH interrupt to 0 and indicate UACT.
- Drive the port where the DTCH interrupt occurred into the idle state.

(11) SACK Interrupt

When this module receives ACK from the peripheral device in response to the transmitted setup packet with the host controller function selected, a SACK interrupt is generated. This interrupt indicates that a setup transaction is successfully completed.

(12) SIGN Interrupt

When this module cannot receive ACK successfully from the peripheral device in response to the transmitted setup packet three times in a row with the host controller function selected, a SIGN interrupt is generated. This interrupt is used to detect no ACK response from the peripheral device or ACK packet damage.

(13) ATTCH Interrupt

When J-State or K-State of the full-speed/low-speed signal level is detected for 2.5 μs in the USB port with the host controller function selected, an ATTCH interrupt is generated. This interrupt is detected in either of the following cases.

- When the signal level changed from K-State, SE0 or SE1 to J-State, and remains in J-State for 2.5 μs
- When the signal level changed from J-State, SE0 or SE1 to K-State, and remains in K-State for 2.5 μs

(14) EOFERR Interrupt

When this module detects that communication is not completed at the EOF2 timing specified in the USB Specification 2.0, an EOFERR interrupt is generated.

After detecting an EOFERR interrupt, this module performs the following hardware control irrespective of the setting of the corresponding interrupt enable bit. The software must terminate the communication of all pipes with the port and perform reenumeration for the port.

- Change the UACT bit of the port that detected the EOFERR interrupt to 0 and indicate UACT.
- Drive the port where the EOFERR interrupt occurred into the idle state.

33.4.3 Pipe Control

Table 33.16 lists the pipe settings of this module. In the USB data transfer, data must be transmitted or received using virtual pipes called “endpoint.” This module is provided with ten pipes for data transfer. Set each pipe according to system specifications.

Table 33.16 Pipe Settings

For when the host controller function is selected

Register Name	Bit Name	Setting	Remarks
DCPCFG	TYPE	Transfer type	Pipes 1 to 9: Setting allowed
PIPECFG	BFRE	BRDY interrupt mode	Pipes 1 to 5: Setting allowed
	DBLB	Double buffer	Pipes 1 to 5: Setting allowed
	CNTMD	Continuous transfer or discontinuous transfer	Pipes 1, 2: Setting allowed only when bulk transfer is selected Pipes 3 to 5: Setting allowed
	DIR	Transfer direction	IN or OUT selectable
	EPNUM	Endpoint number	Pipes 1 to 9: Setting allowed Set a value other than 0000 when using pipes
	SHTNAK	Disabling pipes at the end of transfer	Pipes 1, 2: Setting allowed only when bulk transfer is selected Pipes 3 to 5: Setting allowed
PIPEBUF	BUFSIZE	Buffer memory size	DCP: Setting disallowed (256 bytes fixed) Pipes 1 to 5: Setting allowed (up to 2 Kbytes) Pipes 6 to 9: Setting disallowed (64 bytes fixed)
	BUFNMB	Buffer memory number	DCP: Setting disallowed (H'0 to H'3 fixed) Pipes 1 to 5: Setting allowed (H'8 to H'7F) Pipes 6 to 9: Setting disallowed (H'4 to H'7 fixed)
DCPMAXP PIPEMAXP	DEVSEL	Device select	Checked only when the host controller functions selected.
	MXPS	Maximum packet size	Setting conforming to the USB Specification

Register Name	Bit Name	Setting	Remarks
PIPEPERI	IFIS	Buffer flush	Pipes 1, 2: Setting allowed only when isochronous transfer is selected Pipes 3 to 5: Setting disallowed Pipes 6 to 9 Setting allowed only when the host control function is selected
	IITV	Interval counter	Pipes 1, 2: Setting allowed only when isochronous transfer is selected Pipes 3 to 5: Setting disallowed Pipes 6 to 9 Setting allowed only when the host control function is selected
DCPCTR PIPEnCTR	BSTS	Buffer status	For DCP, receive buffer status and transmit buffer status are switched by the ISEL bit.
	INBUFM	IN buffer monitor	Provided only for pipes 3 to 5.
	SUREQ	SETUP request	Setting allowed for DCP only Controlled only when the host controller function is selected.
	SUREQCLR	SUREQ clear	Setting allowed for DCP only Controlled only when the host controller function is selected.
	CSCLR	CSSTS clear	Controlled only when the host controller function is selected.
	CSSTS	SPLIT status	Monitored only when the host controller function is selected.
	ATREPM	Auto-response mode	Pipes 1 to 5 setting allowed only when the function controller function is selected.
	ACLRM	Buffer auto-clear	Pipes 1 to 9 Setting allowed
	SQCLR	Sequence clear	Data toggle bit clear
	SQSET	Sequence setting	Data toggle bit setting
	SQMON	Sequence check	Data toggle bit check
	PBUSY	Pipe busy check	
	PID	Response PID	See section 33.4.3 (6), Response PID.

Register Name	Bit Name	Setting	Remarks
PIPEnTRE	TRENB	Transaction count enable	Pipes 1 to 5: Setting allowed
	TRCLR	Current transaction counter clear	Pipes 1 to 5: Setting allowed
PIPEnTRN	TRNCNT	Transaction counter	Pipes 1 to 5: Setting allowed

For when the function controller function is selected

Register Name	Bit Name	Setting	Remarks
DCPCFG	TYPE	Transfer type	Pipes 1 to F: Setting allowed
PIPECFG	BFRE	BRDY interrupt mode	Pipes 1 to 5, 9 to F: Setting allowed
	DBLB	Double buffer	Pipes 1 to 5, 9 to F: Setting allowed
	CNTMD	Continuous transfer or discontinuous transfer	Pipes 1, 2: Setting allowed only when bulk transfer is selected Pipes 3 to 5, 9 to F: Setting allowed
	DIR	Transfer direction	IN or OUT selectable
	EPNUM	Endpoint number	Pipes 1 to F: Setting allowed Set a value other than 0000 when using pipes
	SHTNAK	Disabling pipes at the end of transfer	Pipes 1, 2: Setting allowed only when bulk transfer is selected Pipes 3 to 5, 9 to F: Setting allowed
PIPEBUF	BUFSIZE	Buffer memory size	DCP: Setting disallowed (256 bytes fixed) Pipes 1 to 5, 9 to F: Setting allowed (up to 2 Kbytes) Pipes 6 to 8: Setting disallowed (64 bytes fixed)
	BUFNMB	Buffer memory number	DCP: Setting disallowed (H'0 to H'3 fixed) Pipes 1 to 5, 9 to F: Setting allowed (H'8 to H'7F) Pipes 6 to 8: Setting disallowed (H'4 to H'7 fixed)
DCPMAXP PIPEMAXP	DEVSEL	Device select	Checked only when the host controller functions selected.
	MXPS	Maximum packet size	Setting conforming to the USB Specification

Register Name	Bit Name	Setting	Remarks
PIPEPERI	IFIS	Buffer flush	Pipes 1, 2: Setting allowed only when isochronous transfer is selected Pipes 3 to 5, 9 to F: Setting disallowed Pipes 6 to 8 Setting allowed only when the host control function is selected
	IITV	Interval counter	Pipes 1, 2: Setting allowed only when isochronous transfer is selected Pipes 3 to 5, 9 to F: Setting disallowed Pipes 6 to 8 Setting allowed only when the host control function is selected
DCPCTR PIPEnCTR	BSTS	Buffer status	For DCP, receive buffer status and transmit buffer status are switched by the ISEL bit.
	INBUFM	IN buffer monitor	Provided only for pipes 3 to 5, 9 to F.
	SUREQ	SETUP request	Setting allowed for DCP only Controlled only when the host controller function is selected.
	SUREQCLR	SUREQ clear	Setting allowed for DCP only Controlled only when the host controller function is selected.
	CSCLR	CSSTS clear	Controlled only when the host controller function is selected.
	CSSTS	SPLIT status	Monitored only when the host controller function is selected.
	ATREPM	Auto-response mode	Pipes 1 to 5, 9 to F etting allowed only when the function controller function is selected.
	ACLRM	Buffer auto-clear	Pipes 1 to F Setting allowed
	SQCLR	Sequence clear	Data toggle bit clear
	SQSET	Sequence setting	Data toggle bit setting
	SQMON	Sequence check	Data toggle bit check
	PBUSY	Pipe busy check	
	PID	Response PID	See section 33.4.3 (6), Response PID.

Register Name	Bit Name	Setting	Remarks
PIPEnTRE	TRENB	Transaction count enable	Pipes 1 to 5, 9 to F: Setting allowed
	TRCLR	Current transaction counter clear	Pipes 1 to 5, 9 to F: Setting allowed
PIPEnTRN	TRNCNT	Transaction counter	Pipes 1 to 5, 9 to F: Setting allowed

(1) Pipe Control Registers Switching Procedure

The following bits in the pipe control registers can be modified only when USB communication is set to disabled (PID = NAK).

Bits/registers that cannot be modified when USB communication is set to enabled (PID = BUF)

- Each bit in DCPCFG and DCPMAXP
- SQCLR and SQSET bits in DCPCTR
- Each bit in PIPECFG, PIPEBUF, PIPEMAXP, and PIPEPERI
- ATREPM, ACLRM, SQCLR, and SQSET bits in PIPExCTR
- Each bit in PIPExTRE and PIPExTRN

When changing these bits from the state where USB communication is enabled (PID = BUF), follow the steps below.

1. Generate a pipe control register bit change request.
2. Change the PID bits for the pipe to NAK.
3. Wait until the CSSTS bit for the pipe is cleared to 0 (only when the host controller function is selected).
4. Wait until the PBUSY bit for the pipe is cleared to 0.
5. Change the bits in the pipe control registers.

The following bits in the pipe control registers can be modified only for pipe information that is not set in any of the CURPIPE bits in CFIFOSEL, D0FIFOSEL, and D1FIFOSEL.

Bits/registers that cannot be modified while the CURPIPE bits in FIFO-PORT are being set

- Each bit in DCPCFG and DCPMAXP
- Each bit in PIPECFG, PIPEBUF, PIPEMAXP, and PIPEPERI

Before changing the pipe information, set the CURPIPE bits to a pipe other than that to be changed. For the DCP, clear the buffer by the BCLR bit after modifying the pipe information.

(2) Transfer Type

Specify the transfer type of each pipe by the TYPE bits in PIPEPCFG as follows:

- DCP: Setting is not required (fixed to control transfer).
- Pipes 1, 2: Set bulk transfer or isochronous transfer.

When host controller function is selected:

- Pipes 3 to 5: Set bulk transfer.
- Pipes 6 to 9 Set interrupt transfer.

When function controller function is selected:

- Pipes 3 to 5, 9 to F: Set bulk transfer.
- Pipes 6 to 8 Set interrupt transfer.

(3) Endpoint Number

Specify the endpoint number of each pipe by the EPNUM bits in PIPEPCFG. The endpoint number of the DCP is always 0. For other pipes, endpoint 1 to endpoint 15 are selectable.

- DCP: Setting is not required (fixed to endpoint 0).
- Pipes 1 to 9 Set an endpoint number by selecting a number 1 to 9 when host controller function is selected.
- Pipes 1 to F Set an endpoint number by selecting a number 1 to 15 when function controller function is selected.

  However, set an endpoint number so that combinations of the DIR bit and the EPNUM bits do not overlap.

(4) Maximum Packet Size

Specify the maximum packet size of each pipe by the MXPS bits in DCPMAXP and PIPEMAXP. For the DCP and pipes 1 to 5, and 9 to F when function controller function is selected, any of the maximum packet sizes defined in the USB Specification can be set. For pipes 6 to 8, and 9 when host controller function is selected, a maximum packet size up to 64 bytes can be set. Specify a maximum packet size as follows before starting transfer (PID = BUF):

- DCP: Set 64 for high-speed operation.
- DCP: Set 8, 16, 32, or 64 for full-speed operation.

- Pipes 1 to 5, and 9 to F when function controller function is selected: Set 512 for high-speed bulk transfer.
- Pipes 1 to 5, and 9 to F when function controller function is selected: Set 8, 16, 32, or 64 for full-speed bulk transfer.
- Pipes 1, 2: Set a value from 1 to 1024 for high-speed isochronous transfer.
- Pipes 1, 2: Set a value from 1 to 1023 for full-speed isochronous transfer.
- Pipes 6 to 8, 9 and when function controller function is selected, set a value from 1 to 64.

High Bandwidth in interrupt and isochronous transfers is not supported.

(5) Transaction Counter (Pipes 1 to 5, and 9 to F when function controller function is selected : Read Direction)

When the specified number of transactions with data packet in the receive direction are completed, this module recognizes this as a transfer end. The transaction counter works when the pipe selected for the D0FIFO and D1FIFO ports is set for the data read (from the buffer memory) direction. The transaction counter is provided with the TRNCNT register to specify the number of transactions and the current counter to count transactions internally. When the current counter reaches the specified value, the buffer memory becomes ready for reading. The current counter of the transaction counter function can be initialized by the TRCLR bit to count transactions again from the beginning. The TRNCNT read data varies depending on the TRENB setting.

- TRENB = 0: The set transaction counter value is read.
- TRENB = 1: The internally counted current counter value is read.
- Change the CURPIPE bits according to the following.
- Do not change the CURPIPE bits until the transaction for the specified pipe finishes.
- Change the CURPIPE bits when the current counter is cleared.
- Control the TRCLR bit according to the following.
- Do not clear the current counter during transaction count and PID = BUF.
- Do not clear the current counter while data is remaining in the buffer.

(6) Response PID

Specify the response PID for each pipe by the PID bits in DCPCTR and PIPEnCTR.

This module operates as follows according to the response PID setting.

1. Setting the response PID when the host controller function is selected
   The response PID specifies the execution of transactions.
   — NAK setting: Pipes are disabled and no transaction is executed.
   — BUF setting: Transactions are executed according to the buffer memory status.
   When the buffer memory contains transmit data in the OUT direction, this module sends an OUT token.
   When the buffer memory has available space and is ready to receive data in the IN direction, this module sends an IN token.
   — STALL setting: Pipes are disabled and no transaction is executed.

Note: The DCP setup transaction is set by the SUREQ bit.

2. Setting the response PID when the function controller function is selected
   The response PID specifies a response to transactions from the host.
   — NAK setting: NAK is always sent in response to a transaction.
   — BUF setting: A response is sent to a transaction according to the buffer memory status.
   — STALL setting: STALL is always sent in response to a transaction.

Note: This module always sends ACK in response to a setup transaction irrespective of the PID setting, and stores a USB request in the register.

This module modifies the PID bits in the following cases depending on transaction results.

3. When the response PID is set by the hardware with the host controller function selected
   — NAK setting: This module sets PID = NAK and automatically stops sending tokens.
- When an NRDY interrupt is generated in a transfer other than isochronous transfer
- (For details, see 33.4.2(2) NRDY Interrupt.)
- When this module receives a short packet with the SHTNAK bit in PIPECFG set to 1 in the bulk transfer
- When the SHTNAK bit is set to 1 in the bulk transfer and the transaction counter stops counting
  — BUF setting: This module does not set the PID bits to BUF.
  — STALL setting: This module sets PID = STALL in the following cases and automatically stops sending tokens.
- When this module receives STALL in response to the transmitted token
- When the size of the received data packet is larger than the maximum packet size

4. When the response PID is set by the hardware with the function controller function selected
   — NAK setting: This module sets PID to NAK in the following cases and always sends NAK in response to a transaction.
- When a SETUP token is successfully received (DCP only)
- When the SHTNAK bit in PIPECFG is set to 1 in a bulk transfer and the transaction counter stops counting or this module receives a short packet
  — BUF setting: This module does not set the PID bits to BUF.
  — STALL setting: This module sets PID to STALL in the following cases and always sends STALL in response to a transaction.
- When a maximum packet size exceeded error is detected in a receive data packet
- When a control transfer sequence error is detected (DCP only)

(7) Data PID Sequence Bit

When data is successfully transferred in the control transfer data stage, bulk transfer, or interrupt transfer, this module automatically toggles the data PID sequence bit. The sequence bit of the data PID transmitted next can be monitored by the SQMON bit in DCPCTR and PIPEnCTR. In a data transmission period, the sequence bit switches at the ACK handshake receive timing. In a data reception period, the sequence bit switches at the ACK handshake transmit timing. The data PID sequence bit can also be changed by the SQCLR and SQSET bits in DCPCTR and PIPEnCTR.

In control transfers when the function controller function is selected, this module automatically sets the sequence bit during a stage transition. DATA0 is indicated at the end of the setup stage, and DATA1 is used for responses in the status stage. This does not require the setting of the sequence bit by the software. In control transfers when the host controller function is selected, the software must set the sequence bit during a stage transition.

Note that, when the host controller function or function controller function is selected, the software must also set the data PID sequence bit when sending or receiving a ClearFeature request.

The sequence bit cannot be modified by the SQSET bit for isochronous transfer pipes.

(8) Response PID = NAK Function

This module has a function to disable the pipe operation (Response PID = NAK) at the last data packet receive timing in a transfer (this module automatically identifies the last data packet receive timing at the short packet receive timing or using the transaction counter) by setting the SHTNAK bit in PIPECFG to 1.

This function allows reception of data packets in transfer units when the buffer memory is used as a double buffer. Furthermore, when the pipe operation is disabled, the software must set the response PID to BUF to enable the pipe operation.

This function is available only for bulk transfers.

(9) Auto-Response Mode

When the ATREPM bit in PIPEnCTR is set to 1 in a bulk transfer pipe (pipes 1 to 5 , and 9 to F when the function controller function is selected), this module enters auto-response mode: OUT-NAK mode in OUT transfers (DIR = 0) or null auto-response mode in IN transfers (DIR = 1).

1. OUT-NAK mode

   When the ATREPM bit is set to 1 in a bulk OUT transfer pipe, this module sends NAK in response to an OUT token or PING token and outputs an NRDY interrupt. To change response mode from normal mode to OUT-NAK mode, specify OUT-NAK mode with the pipe operation disabled (Response PID = NAK), and then enable the pipe operation (Response PID = BUF). After that, OUT-NAK mode is enabled. However, if an OUT token is received immediately before the pipe operation is disabled, this module receives the data of the token correctly and sends ACK to the host.

   To change response mode from OUT-NAK mode to normal mode, reset OUT-NAK mode with the pipe operation disabled (Response PID = NAK), and then enable the pipe operation (Response PID = BUF). In normal mode, this module can receive OUT data and sends ACK in response to a PING token when the buffer is ready for receiving.

2. Null auto-response mode

   When the ATREPM bit is set to 1 in a bulk IN transfer pipe, this module continues to send Zero-Length packets. To change response mode from normal mode to null auto-response mode, specify null auto-response mode with the pipe operation disabled (Response PID = NAK), and then enable the pipe operation (Response PID = BUF). After that, null auto-response mode is enabled. However, specify null auto-response mode while the buffer is empty. Verify this by checking INBUFM = 0. Since INBUFM = 1 indicates that the buffer contains data, clear the buffer by setting the ACLRM bit. Do not write data to the buffer from the FIFO port during setting to null auto-response mode.

To change response mode from null auto-response mode to normal mode, delay the pipe operation disabled state (Response PID = NAK) for a time period for sending a Zero-Length packet (full-speed: 10 μs, high-speed: 3 μs), and then reset null auto-response mode. Normal mode allows writing from the FIFO port, and also allows sending packets to the host by enabling the pipe operation (Response PID = BUF).

33.4.4 FIFO Buffer Memory

(1) Allocating FIFO Buffer Memory

Figure 33.9 shows an example of the FIFO buffer memory map of this module. The FIFO buffer memory is an area shared by the CPU and this module. There are two FIFO buffer memory states where the access right is given to the system (CPU) or to this module (SIE).

The FIFO buffer memory provides independent areas for each pipe. A memory area is set with the block start number and the number of blocks (BUFNMB and BUFSIZE bits in PIPEBUF) in 64-byte units as one block.

When continuous transfer mode is selected by the CNTMD bit in PIPEnCFG, be sure to set the BUFSIZE bits to a value in integral multiples of the maximum packet size. When double buffer is selected by the DBLB bit in PIPEnCFG, two sides of the memory area specified by the BUFSIZE bits in PIPEBUF are provided for the same pipe.

Furthermore, three FIFO ports are used for accesses (data read/write) to the buffer memory. The number of a pipe to be allocated to the FIFO ports is specified by the CURPIPE bits in CFIFOSEL and DnFIFOSEL.

The buffer status of each pipe can be monitored by the BSTS and INBUFM bits in DCPCTR and PIPEnCTR. The access right to the FIFO ports can be checked by the FRDY bit in CFIFOCTR and DnFIFOCTR.

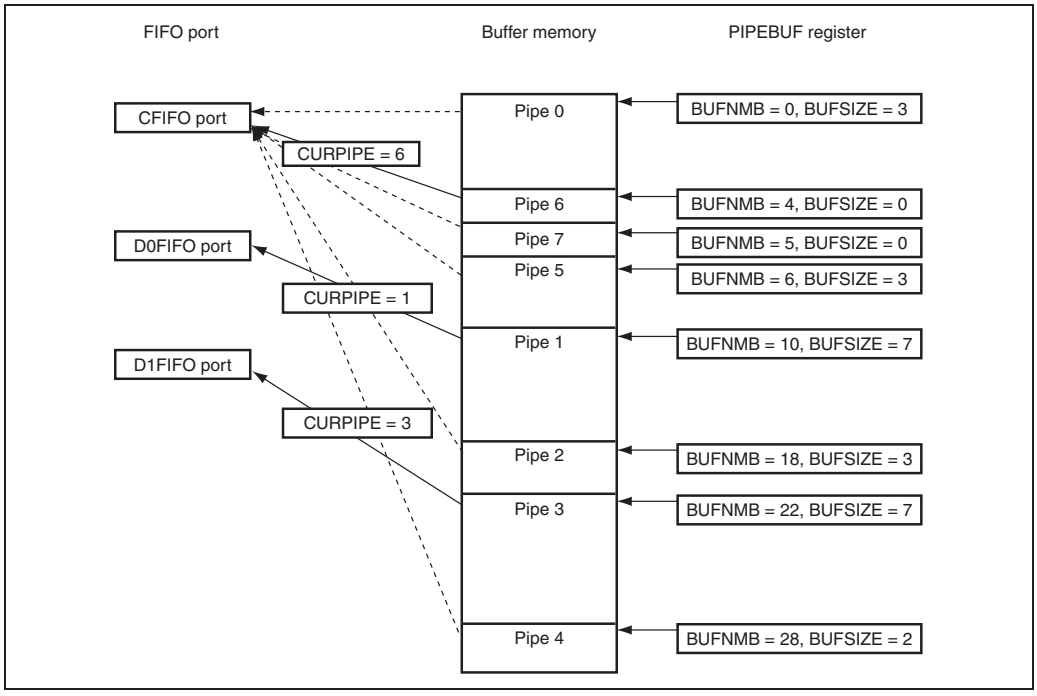


Figure 33.9 Example of Buffer Memory Map

- Buffer status

  Tables 33.17 and 33.18 show the buffer memory status of this module. The buffer memory status can be monitored by the BSTS bit in DCPCTR and the INBUFM bit in PIPEnCTR. The buffer memory access direction is specified by the DIR bit in PIPEnCFG or the ISEL bit in CFIFOSEL (when DCP is selected).

  The INBUFM bit is valid only for pipes 1 to 5, and 9 to F when function controller function is selected in the transmit direction.

  When a transfer pipe in the transmit direction is set to double buffer, the BSTS bit is used to monitor the buffer status on the CPU side, and the INBUFM bit is used to monitor the buffer status on the SIE side. When data write to the FIFO port by the CPU (DMAC) takes time and buffer empty cannot be checked by the BEMP interrupt, the INBUFM bit is available to check completion of transmission.

Table 33.17 Buffer Memory Status That Varies Depending on the BSTS Bit

ISEL or DIR	BSTS	Buffer Memory Status
0 (receive direction)	0	No receive data in the buffer memory or data is being received. Data cannot be read from the FIFO port.
0 (receive direction)	1	Receive data in the buffer memory or a Zero-Length packet is received. Data can be read from the FIFO port. However, the buffer must be cleared because the FIFO port cannot be read when this module receives a Zero-Length packet.
1 (transmit direction)	0	Transmission of data is not completed. Data cannot be written to the FIFO port.
1 (transmit direction)	1	Transmission of data is completed. The CPU can write data to the buffer memory.

Table 33.18 Buffer Memory Status That Varies Depending on the INBUFM Bit

DIR	INBUFM	Buffer Memory Status
0 (receive direction)	Invalid	Invalid
1 (transmit direction)	0	Transmittable data is completely sent. No transmittable data is in the buffer memory.
1 (transmit direction)	1	Transmittable data is written from the FIFO port. The buffer memory contains transmittable data.

- FIFO buffer clear

  Table 33.19 shows clearing of the FIFO buffer memory of this module. The buffer memory can be cleared by the BCLR, DCLRM, and ACLRM bits.

Table 33.19 Buffer Clear

Bit Name	BCLR	DCLRM	ACLRM
Register	CFIFOCTR DnFIFOCTR	DnFIFOSEL	PIPEnCTR
Function	Clears the buffer memory of the CPU.	Automatically clears the buffer memory after reading data of the specified pipe.	Automatically clears the buffer memory by ignoring all received packets.
Clearing method	Writing 1 to this bit clears the buffer memory.	1: This mode is enabled. 0: This mode is disabled.	1: This mode is enabled. 0: This mode is disabled.

- Buffer area

  Table 33.20 shows a buffer memory map of this module. The buffer memory includes a dedicated areas reserved beforehand for pipes and user areas provided for user settings.

  The buffer for DCP is a dedicated area commonly used in control read transfers and control write transfers.

  Areas for pipes 6 to 8, and 9 when host controller function is selected, are allocated respectively in advance. However, when none of pipes 6 to 8, and 9 when host controller function is selected, is used, the areas are available for pipes 1 to 5, 9 to F when function controller function is selected, as user areas.

  Allocate different areas of the buffer memory to each pipe. Note that, when double buffer is specified, the size of an area is twice of the set value.

  Do not set the buffer size to a value smaller than the maximum packet size.

Table 33.20 Buffer Memory Map

Buffer Memory Number	Buffer Size	Pipe Setting	Remarks
H'0	64 bytes	Fixed only for DCP	Single buffer
H'1 to H'3	—	Unavailable	—
H'4	64 bytes	Fixed only for pipe 6	Single buffer
H'5	64 bytes	Fixed only for pipe 7	Single buffer
H'6	64 bytes	Fixed only for pipe 8	Single buffer

Buffer Memory Number	Buffer Size	Pipe Setting	Remarks
H'7	64 bytes	Fixed only for pipe 9	Single buffer when host controller function is selected
H'8to H'7F,and H'7 when function controller function is selected.	Max. 7616 bytes	User area for pipes 1 to 5, and 9 to F when function controller function is selected	Double buffer and continuous transfer can be set

- Buffer auto-clear mode function

  When the ACLRM bit PIPEnCTR is set to 1, this module discards all data packets received. However, when this module receives a data packet successfully, it sends ACK to the host controller. This function is available only for the buffer memory read direction.

  Writing 1 and then 0 continuously to the ACLRM bit clears the buffer memory of the selected pipe irrespective of the access direction.

  Take at least 100 ns between writing 1 and writing 0 for the sequence execution time of the hardware.

- Buffer memory specifications (single buffer/double buffer setting)

  Single buffer or double buffer is selectable for pipes 1 to 5, and 9 to F when function controller function is selected, with the DBLB bit in PIPEnCFG. Double buffer is a function to provide two sides of the memory area specified by the BUFSIZE bits in PIPEBUF for the same pipe. Figure 33.10 shows an example of setting for the buffer memory of this module.

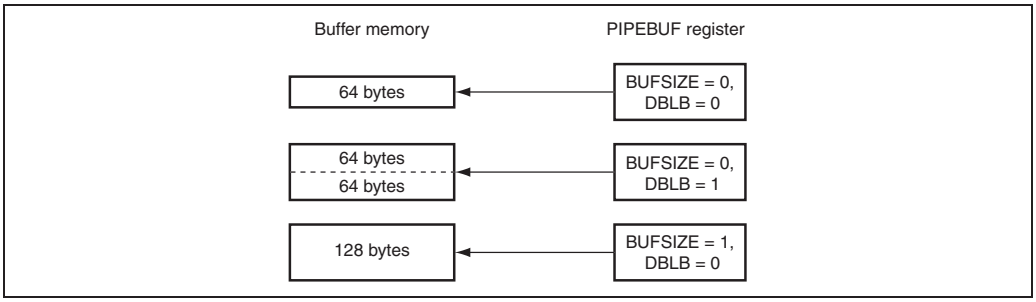


Figure 33.10 Example of Buffer Memory Setting

- Buffer memory operation (continuous transfer setting)

  Continuous transfer mode or discontinuous transfer mode is selectable with the CNTMD bit in PIPEnCFG. This selection is enabled for pipes 1 to 5, 9 to F when function controller function is selected.

The continuous transfer mode function allows continuous transmission/reception of multiple transactions. When continuous transfer mode is selected, data up to the buffer size allocated to each pipe can be transferred without outputting an interrupt to the CPU.

In continuous transmission mode, data in the buffer is divided by the maximum packet size and is then transmitted. To send data less than the buffer size (a short packet or a packet with a size of integral multiples of the maximum packet size and less than the buffer size), set BVAL = 1 after writing transmit data to the buffer.

In continuous reception mode, no interrupt is generated until this module receives packets to the buffer size, the transaction count ends, or this module receives a short packet.

Table 33.21 shows the relationship between the CNTMD setting and determination of transmission/reception end of the FIFO buffer.

Table 33.21 Relationship between CNTMD Setting and Determination of Transmission/Reception End of FIFO Buffer

Transfer Mode	Determination of Buffer Readable State and Data Transmittable State
Discontinuous transfer (CNTMD = 0)	Conditions for FIFO buffer readable state when data receive direction is selected (DIR = 0):
	When this module receives one packet
	Conditions for FIFO buffer data transmittable state when data transmit direction is selected (DIR = 1):
	Any of the following cases:
	The software (or DMAC) writes data of the maximum packet size to the FIFO buffer.
	The software (or DMAC) writes data of a short packet (including 0 bytes) to the FIFO buffer, and then sets BVAL = 1.
Continuous transfer (CNTMD = 1)	Conditions for FIFO buffer readable state when data receive direction is selected (DIR = 0):
	When the bytes of data received in the FIFO buffer for the selected pipe equals the allocated bytes ((BUFSIZE + 1) * 64)
	When this module receives a short packet other than a Zero-Length packet
	When this module receives a Zero-Length packet when data is already stored in the FIFO buffer for the selected pipe
	When this module receives packets as large as the transaction counter value specified for the selected pipe by the software
	Conditions for FIFO buffer data transmittable state when data transmit direction is selected (DIR = 1):
	Any of the following cases:
	The volume of data written by the software (or DMAC) equals the size of one side of the FIFO buffer for the selected pipe.
	The software (or DMAC) writes data less than the size of one side of the FIFO buffer for the selected pipe to the FIFO buffer, and then sets BVAL = 1.

Figure 33.11 shows an example of buffer memory operation of this module.

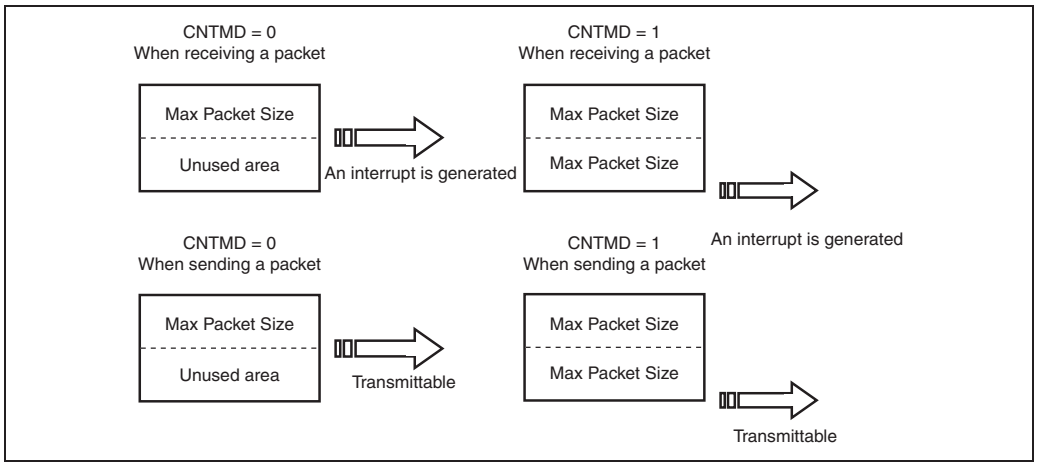


Figure 33.11 Example of Buffer Memory Operation

(2) FIFO Port Function

Table 33.22 lists the settings for the FIFO port functions of this module. During a data write access, when data up to buffer full (or up to the maximum packet size in discontinuous transfer) is written, the FIFO port automatically enters the data transmittable state. To make data less than buffer full (or the maximum packet size in discontinuous transfer) transmittable, set the BVAL bit in CFIFOCTR and DnFIFOCTR to 1 to set write end. For transmission of a Zero-Length packet, clear the buffer using the BCLR bit in these registers and then set the BVAL bit to 1.

During a data read access, when all data is read, the FIFO port automatically enters the new packet receivable state. However, when receiving a Zero-Length packet (DTLN = 0), no data can be read. Therefore, clear the buffer using the BCLR bit in these registers. The receive data length can be checked by the DTLN bits in CFIFOCTR and DnFIFOCTR.

Table 33.22 FIFO Port Function Settings

Register Name	Bit Name	Function	Remarks
CFIFOSEL	RCNT	Selects DTLN read mode.	
DnFIFOSEL	REW	Rewinds the buffer memory (reread/rewrite).	
	DCLRM	Reads and clears receive data of the specified pipe.	DnFIFO only
	DREQE	Enables DMA transfer.	DnFIFO only
	MBW	Specify FIFO port access bit width.	
	BIGEND	Selects FIFO port endian.	
	ISEL	Selects FIFO port access direction.	DCP only
	CURPIPE	Select the current pipe.	
CFIFOCTR	BVAL	Specifies buffer memory write end.	
DnFIFOCTR	BCLR	Clears the buffer memory of the CPU.	
	DTLN	Check receive data length.	

(a) FIFO Port Selection

Table 33.23 shows pipes that can be selected in each FIFO port. Select a pipe to be accessed by the CURPIPE bits in CFIFOSEL and DnFIFOSEL. After selecting a pipe, confirm that the set CURPIPE value is read correctly, check FRDY = 1, and then make an access to the FIFO port. (If the previous pipe number is read, this controller is changing a pipe.)

Also select the bus width to be accessed by the MBW bits. The buffer memory access direction is specified by the DIR bit in PIPEnCFG. However, only the access direction of DCP is determined by the ISEL bit.

Table 33.23 FIFO Port Access

Pipe	Access	Available port
DCP	CPU access	CFIFO port register
Pipes 1 to 9, and A to F when the function controller function is selected	CPU access	CFIFO port register
	DMA access	D0FIFO port, D1FIFO port

(b) REW Bit

The current access to a pipe can be suspended temporarily, and it is also possible to make an access to another pipe to continue the ongoing pipe processing. This processing is allowed by using the REW bit in CFIFOSEL and DnFIFOSEL.

When the REW bit is set to 1 together with the CURPIPE bits in CFIFOSEL and DnFIFOSEL and a pipe is selected, the reading or writing pointer of the buffer memory is reset, which allows reading or writing data from the first byte. Furthermore, when a pipe is selected with the REW bit set to 0, data can be read or written following the data at the previous selection without resetting the reading or writing pointer of the buffer memory.

To make accesses to the FIFO port, select a pipe and check FRDY = 1.

(3) DMA Transfer (Dedicated DMA Interface)

(a) Overview of DMA Transfer

The FIFO port can be accessed by the DMAC for pipes 1 to 9, and A to F when function controller function is selected, When the buffer of a pipe specified for DMA transfer becomes accessible, this module outputs a DMA transfer request.

Specify the data transfer unit to the FIFO port by the MBW bits in DnFIFOSEL, and select a pipe used for DMA transfer by the CURPIPE bits in DnFIFOSEL. Do not change the selected pipe during a DMA transfer.

(b) DMA Transfer End Auto-Recognition

This module can terminate writing of data by DMA transfer to the FIFO buffer by controlling the DMA transfer end signal input. After sampling the transfer end signal, this module drives the buffer memory into the transmittable state (same state as BVAL = 1).

(c) DnFIFO Auto-Clear Mode (D0FIFO/D1FIFO Port Read Direction)

By setting the DCLRM bit in DnFIFOSEL to 1, this module automatically clears the buffer memory for the selected pipe upon completion of data read from the buffer memory.

Table 33.24 shows the relationship between packet reception and buffer memory clear by the software. As shown in the table, buffer clearing conditions vary with the BFRE setting. However, in any state that needs clearing, using the DCLRM bit makes buffer clearing by the software unnecessary. Thus DMA transfer is enabled without requiring any software control.

- This function is available only for the buffer memory read direction.

Table 33.24 Relationship between Packet Reception and Buffer Memory Clear by the Software

Register Setting / Buffer Status When Receiving a Packet	DCLRM = 0		DCLRM = 1	
	BFRE = 0	BFRE = 1	BFRE = 0	BFRE = 1
Buffer full	Clearing not required	Clearing not required	Clearing not required	Clearing not required
Zero-Length packet reception	Clearing required	Clearing required	Clearing not required	Clearing not required
Normal short packet reception	Clearing not required	Clearing required	Clearing not required	Clearing not required
Transaction count end	Clearing not required	Clearing required	Clearing not required	Clearing not required

33.4.5 Control Transfer (DCP)

The default control pipe (DCP) is used for data transfer in the control transfer data stage. The buffer memory for the DCP is a 256-byte single buffer of a fixed area used for both control read and control write. The buffer memory can be accessed only by the CFIFO ports.

(1) Control Transfer when the Host Controller Function is Selected

(a) Setup Stage

USBREQ, USBVAL, USBINDX, and USBLENG are registers used to send USB requests in setup transactions. The specified data is sent as a setup transaction by writing the setup packet data in the register and writing 1 to the SUREQ bit in DCPCTR. The SUREQ bit is cleared to 0 when a transaction ends. Do not access the USB request registers while SUREQ = 1. The device address for a setup transaction is specified by the DEVSEL bits in DCPMAXP.

An interrupt is generated upon receiving a response from the peripheral device in response to the transmitted transaction (SIGN and SACK bits in INTSTS1). The setup transaction result can be checked at the timing of this interrupt request.

For data packets in setup transactions, a DATA0 data packet (USB request) is always sent irrespective of the SQMON setting in DCPCTR.

(b) Data Stage

This module transfers data using the DCP buffer memory in the data stage.

Specify the direction of accesses to the DCP buffer memory by the ISEL bit in CFIFOSEL. Also specify the transfer direction by the DIR bit in DCPCFG.

Transmit the first data packet in the data stage with data PID as DATA1. Set data PID = DATA1 by the SQSET bit in DCPCFG, and set PID = BUF to execute transactions. The completion of data transfer is detected by a BRDY interrupt and a BEMP interrupt.

In a control write transfer, when the transmit data is integral multiples of the maximum packet size, send a Zero-Length packet at the last by the software.

(c) Status Stage

In the status stage, data transfer of Zero-Length packets is performed in the reverse direction of the data stage. The same DCP buffer memory as in the data stage is used for data transfer. Transactions are executed using the same procedure as the data stage.

Send data packets in the data stage with data PID as DATA1. Set data PID = DATA1 by the SQSET bit in DCPCFG.

Furthermore, check the receive data length of a Zero-Length packet by the DTLN bits in CFIFOCTR after a BRDY interrupt is generated, and then clear the buffer memory by the BCLR bit.

(2) Control Transfer when the Function Controller Function is Selected

(a) Setup Stage

1. This module always sends ACK in response to a normal setup packet to this module. The following describes the operation of this module in the setup stage.
   When this module receives a new setup packet, this module sets the following bits.
   — The VALID bit in INTSTS0 to 1
   — The PID bits in DCPCTR to NAK
   — The CCPL bit in DCPCTR to 0
2. When this module receives a data packet following a setup packet, this module stores the USB request parameters in USBREQ, USBVAL, USBINDX, and USBLENG.

Be sure to process responses to control transfers while VALID = 0. The PID bits cannot be set to BUF when VALID = 1, and therefore the data stage cannot be completed.

With the VALID bit function, this module can suspend the ongoing request processing if this module receives a new USB request during a control transfer, and send a response to the latest request.

This module also determines the direction bit (bit 8 of bmRequestType) of the received USB request and the request data length (wLength), identifies a control read transfer, control write transfer, and control write no-data transfer, and controls stage transitions. For an incorrect sequence, a sequence error of the control transfer stage transition interrupt occurs, and the error is reported to the software. For the stage control of this module, see Figure 33.7.

(b) Data Stage

Transfer data in response to the received USB request using the DCP. Before making an access to the DCP buffer memory, specify the access direction by the ISEL bit in CFIFOSEL.

When the transfer data size is larger than the DCP buffer memory size, use a BRDY interrupt for control write transfers and a BEMP interrupt for control read transfers.

In the high-speed control write transfer, this module sends responses using the NYET handshake according to the buffer memory status.

(c) Status Stage

Setting the CCPL bit to 1 with the PID bits in DCPCTR set to BUF finishes a control transfer.

After these settings, this module executes the status stage as follows according to the data transfer direction determined in the setup stage:

- Control read transfer
  This module sends a Zero-Length packet and receives an ACK response from the USB host.
- Control write transfer, no-data control transfer
  This module receives a Zero-Length packet from the USB host and sends an ACK response.

(d) Control Transfer Auto-Response Function

This module automatically responds to a correct SET_ADDRESS request. If any of the following errors occurs in the SET_ADDRESS request, the software must respond to the error.

- Other than control read transfer: bmRequestType ≠ H'00
- Request errors: wIndex ≠ H'00
- Other than no-data control transfer: wLength ≠ H'00
- Request errors: wValue > H'7F

- Control transfer of device state errors: DVSQ = 011 (Configured)

All requests other than SET_ADDRESS require a response made by the software.

33.4.6 Bulk Transfer (Pipes 1 to 5, and 9 to F when the function controller function is selected)

The buffer memory usage (single buffer/double buffer setting or continuous/discontinuous transfer mode setting) can be selected for bulk transfers. The buffer memory size can be set to up to 2 Kbytes. This module manages the buffer memory status and automatically responds to a PING packet and an NYET handshake.

(1) PING Packet Control when the Host Controller Function is Selected

This module automatically sends a PING packet in the OUT direction.

As described below, this module sends an OUT packet upon receiving an ACK handshake with the initial state where a PING packet was transmitted. When this module receives NAK or NYET, it returns to the PING transmission state. This control is also effective for the control transfer data stage and status stage.

1. Set OUT data transmission.
2. Send a PING packet.
3. Receive an ACK handshake.
4. Send an OUT data packet.
5. Receive an ACK handshake.
   (Repeat steps 4 and 5.)
6. Send an OUT data packet.
7. Receive a NAK/NYET handshake.
8. Send a PING packet.

This module returns to the PING packet transmission state at the time of a power-on reset, receiving NYET/NAK handshake, setting the sequence toggle bit, setting clear (SQSET, SQCLR), and setting buffer clear (ACLRM).

(2) NYET Handshake Control when the Function Controller Function is Selected

Table 33.25 lists NYET handshake responses of this module. This module sends a NYET response under the following conditions. However, when this module receives a short packet, this module sends ACK instead of NYET. The same is true of the control write transfer data stage.

Table 33.25 NYET Handshake Responses

Setting of PID Bits in DCPCTR	Buffer Memory Status	Token	Response	Remarks
NAK/STALL	—	SETUP	ACK	—
	—	IN/OUT/PING	NAK/STALL	—
BUF	—	SETUP	ACK	—
	RCV-BRDY1	OUT/PING	ACK	Receives a data packet when receiving an OUT token.
	RCV-BRDY2	OUT	NYET	Receives a data packet. Sends a “reception disable” response.
	RCV-BRDY2	OUT (Short)	ACK	Receives a data packet. Sends a “reception enable” response.
	RCV-BRDY2	PING	ACK	Sends a “reception enable” response.
	RCV-NRDY	OUT/PING	NAK	Sends a “reception disable” response.
	TRN-BRDY	IN	DATA0/1	Sends a data packet.
	TRN-NRDY	IN	NAK	TRN-NRDY

[Legend]

RCV-BRDY1: The buffer memory has available space for two packets or more when receiving an OUT or PING token.

RCV-BRDY2: The buffer memory has available space for only one packet when receiving an OUT token.

RCV-NRDY: The buffer memory is occupied when receiving an PING token.

TRN-BRDY: The buffer memory contains transmit data when receiving an IN token.

TRN-NRDY: The buffer memory contains no transmit data when receiving an IN token.

33.4.7 Interrupt Transfer (Pipes 6 to 8, and 9 when function controller function is selected)

When the function controller function is selected, this module performs interrupt transfer following the cycles controlled by the host controller. In interrupt transfers, this module ignores PING packets (no response), sends no NYET handshake, and sends ACK, NAK, and STALL responses.

When the host controller function is selected, the token output timing can be set using the interval counter. This module sends no PING token, but sends OUT tokens even in the OUT direction transfer.

This module does not support the High-Bandwidth interrupt transfer.

(1) Interval Counter in Interrupt Transfer when the Host Controller Function is Selected

To perform an interrupt transfer, set a transaction interval by the IITV bits in PIPEPERI. This controller sends tokens in the interrupt transfer at the specified intervals.

(a) Counter initialization

This controller initializes the interval counter under the following conditions.

- Power-on reset:
  The IITV bits are initialized.
- Buffer memory initialization by ACLRM
  The IITV bits are not initialized but the counter is initialized. The IITV value is counted from the beginning by clearing the ACLRM bit to 0.

Note that the interval counter is not initialized in the following cases.

- USB bus reset or USB suspended
  The IITV bits are not initialized. Setting the UACT bit to 1 causes the interval counter to start counting from the value before the USB bus reset or USB suspended state.

(b) Operation when this module cannot send/receive tokens at the token generation timing

This module generates no token in the following cases even at the token generation timing. In these cases, this module tries to execute the transaction in the next interval.

- When PID = NAK or STALL is set

- When the buffer memory is occupied at the token transmit timing in the IN direction (reception) transfer
- When the buffer memory contains no transmit data at the token transmit timing in the OUT direction (transmission) transfer

33.4.8 Isochronous Transfer (Pipes 1, 2)

This module is provided with the following functions for isochronous transfers.

- Reporting isochronous transfer error information
- Interval counter (IITV bits)
- Isochronous IN transfer data setup control (IDLY function)
- Isochronous IN transfer buffer flush function (IFIS bit)

This module does not support the isochronous High-Bandwidth transfer.

(1) Isochronous Transfer Error Detection

This module is provided with a function to detect the following error information so that the software can manage isochronous transfer errors. Tables 33.26 and 33.27 show the error detection priority of this module and interrupts generated as a result of error detection.

1. PID error
   — When the PID in a receive packet is invalid
2. CRC error, bit stuffing error
   — When a CRC error is found in a receive packet or bit stuffing is invalid
3. Maximum packet size exceeded error
   — When the data size of a receive packet is over the maximum packet size setting
4. Overrun/underrun error
   — When the host controller function is selected
     When the buffer memory is occupied at the token transmit timing in the IN direction (reception) transfer
     When the buffer memory contains no transmit data at the token transmit timing in the OUT direction (transmission) transfer
   — When the function controller function is selected
     When the buffer memory contains no data when this module receives an IN token in the IN direction (transmission) transfer
     When the buffer memory is occupied when this module receives an OUT token in the OUT direction (reception) transfer

5. Interval error

   When the function controller function is selected, this module generates an interval error in the following cases.

   — When no IN token can be received in interval frames in the isochronous IN transfer

   — When this module receives an OUT token other than interval frames in the isochronous OUT transfer

Table 33.26 Error Detection when Receiving Tokens

Priority for Error Detection	Error	Interrupt and Status
1	PID error	This module generates no interrupt (ignores as a damaged packet) when either of the host controller function or function controller function is selected.
2	CRC error, bit stuffing error	This module generates no interrupt (ignores as a damaged packet) when either of the host controller function or function controller function is selected.
3	Overrun error, underrun error	This module generates an NRDY interrupt and sets the OVRN bit when either of the host controller function or function controller function is selected. When the host controller function is selected, this module sends no token. When the function controller function is selected, this module sends a Zero-Length packet in response to the IN token. This module receives no data packet in response to the OUT token.
4	Interval error	When the function controller function is selected, this module generates an NRDY interrupt. When the host controller function is selected, this module generates no interrupt.

Table 33.27 Error Detection when Receiving Data Packets

Priority for Error Detection	Error	Interrupt and Status
1	PID error	This module generates no interrupt (ignores as a damaged packet).
2	CRC error, bit stuffing error	This module generates an NRDY interrupt and sets the CRCE bit when either of the host controller function or function controller function is selected.
3	Maximum packet size exceeded error	This module generates a BEMP interrupt and sets the PID bits to STALL when either of the host controller function or function controller function is selected.

(2) DATA-PID

This module does not support the High-Bandwidth transfer. The following lists responses to received PIDs when the function controller function is selected.

1. IN direction
   - DATA0: Sent correctly as the PID of data packet.
   - DATA1: Not sent
   - DATA2: Not sent
   - mDATA: Not sent
2. OUT direction (full-speed operation)
   - DATA0: Received correctly as the PID of a data packet.
   - DATA1: Received correctly as the PID of a data packet.
   - DATA2: The packet is ignored.
   - mDATA: The packet is ignored.
3. OUT direction (high-speed operation)
   - DATA0: Received correctly as the PID of a data packet.
   - DATA1: Received correctly as the PID of a data packet.
   - DATA2: Received correctly as the PID of a data packet.
   - mDATA: Received correctly as the PID of a data packet.

(3) Interval Counter

Intervals for isochronous transfers can be set by the IITV bits in PIPEPERI. When the function controller function is selected, the functions shown in Table 33.28 are made available with the interval counter. When the host controller function is selected, the interval counter generates the token transmit timing. When the host controller function is selected, the interval counter works in the same way as in the interrupt transfer.

Table 33.28 Interval Counter Functions when the Function Controller Function is Selected

Transfer Direction	Function	Detection Conditions
IN	Transmit buffer flush	No IN token can be successfully received in the interval frame during the isochronous IN transfer.
OUT	Reporting reception of no token	No OUT token can be successfully received in the interval frame during the isochronous OUT transfer.

Since the interval counter is counted upon receiving an SOF or using the interpolated SOF, the isochronism can be maintained even if the SOF is damaged. The specifiable frame interval is 2^{IITV} frames or 2^{IITV} μ frames.

(a) Counter initialization when the function controller function is selected

This module initializes the interval counter as follows:

- Power-on reset
  The IITV bits are initialized.
- Initializing buffer memory by ACLRM
  The IITV bits are not initialized but the interval counter is initialized. Clearing the ACLRM bit to 0 causes the counter to start counting from the set IITV value.

After the interval counter is initialized, the interval counter starts counting in either of the following cases after a packet is correctly transferred.

1. When this module receives an SOF after sending data in response to the IN token with PID = BUF
2. When this module receives an SOF after receiving the OUT token data with PID = BUF

The interval counter is not initialized under the following conditions.

1. When PID = NAK or STALL
   The interval timer does not stop. Try to execute the transaction in the next interval.
2. USB bus reset and USB suspended
   The IITV bits are not initialized. When this module receives an SOF, the interval counter starts counting from the value before receiving the SOF.

(b) Interval count and transfer control when the host controller function is selected

This module controls the token transmission intervals using the set IITV value. This module sends a token for the selected pipe once every 2^IITV times of (μ) frames.

This module counts the interval at every 1-ms frame for the pipe used for communication with the full-speed/low-speed peripheral device connected to the high-speed HUB.

This module starts counting the token transmission interval from the next (μ) frame where PID = BUF is specified by the software.

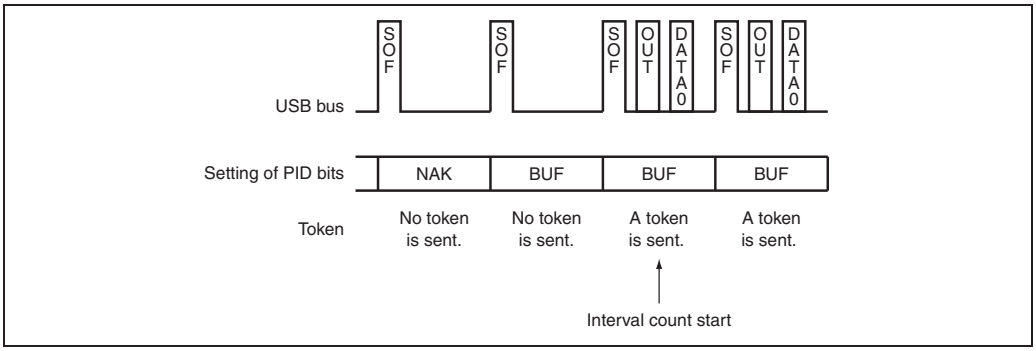


Figure 33.12 Transmission of Tokens when IITV = 0

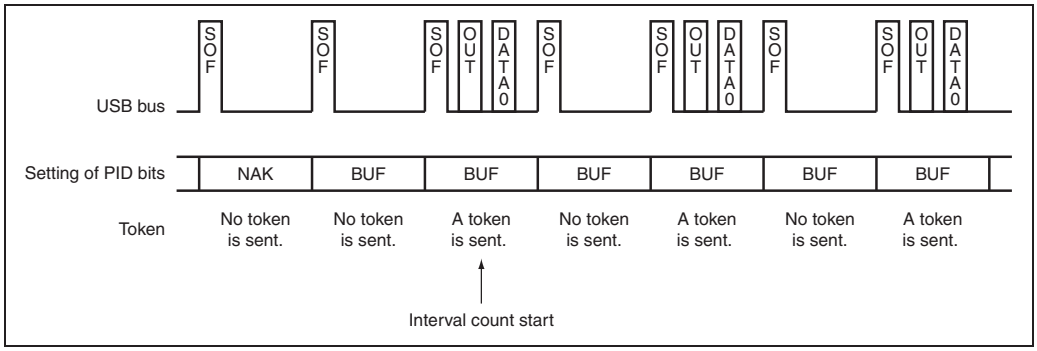


Figure 33.13 Transmission of Tokens when IITV = 1

When the selected pipe is isochronous transfer type, this module performs the following operations in connection with the token transmission interval control. Even if the NRDY interrupt generation conditions are satisfied, this module sends tokens.

1. When the selected pipe is Isochronous-IN transfer pipe

   This module sends an In-Token. When this module does not successfully receive a packet from the peripheral device (including no response and a packet error), this module generates an NRDY interrupt.

   When the IN-Token transmit timing comes before receiving data caused by the FIFO buffer full (due to a delay of reading data from the FIFO buffer by the software or DMAC), this module indicates OVRN = 1 and generates an NRDY interrupt.
2. When the selected pipe is Isochronous-OUT transfer pipe

   When the OUT-Token transmit timing comes with no transmittable data in the FIFO buffer (due to a delay of writing data to the FIFO buffer by the software or DMAC), this module indicates OVRN = 1, generates an NRDY interrupt, and sends a Zero-Length packet.

   The token transmission interval is reset in the following cases.

   — When this module is reset by the hardware (The set IITV value is also cleared to 0.)

   — When ACLRM is set to 1 by the software

(c) Interval count and transfer control when the function controller function is selected

1. When the selected pipe is Isochronous-OUT transfer pipe

   When this module receives no data packet in (μ) frames at the intervals specified by the IITV bits, this controller generates an NRDY interrupt.

   When this module cannot receive data due to a CRC error in the data packet, FIFO buffer full, or other reasons, this module also generates an NRDY interrupt.

   An NRDY interrupt is generated at the SOF packet receive timing. Even if the SOF packet is damaged, this module generates an NRDY interrupt at the SOF packet receive timing using the internal interpolation function.

   When IITV ≠ 0, however, this module generates an NRDY interrupt at the SOF packet receive timing in each interval after the interval count starts.

   When PID = NAK is set by the software after the interval timer is activated, this module generates no NRDY interrupt even when this module receives an SOF packet.

   The interval count start conditions vary with the set IITV value.

   — When IITV = 0: The interval count starts from the next (μ) frame where the PID bits for the selected pipe is changed to BUF.

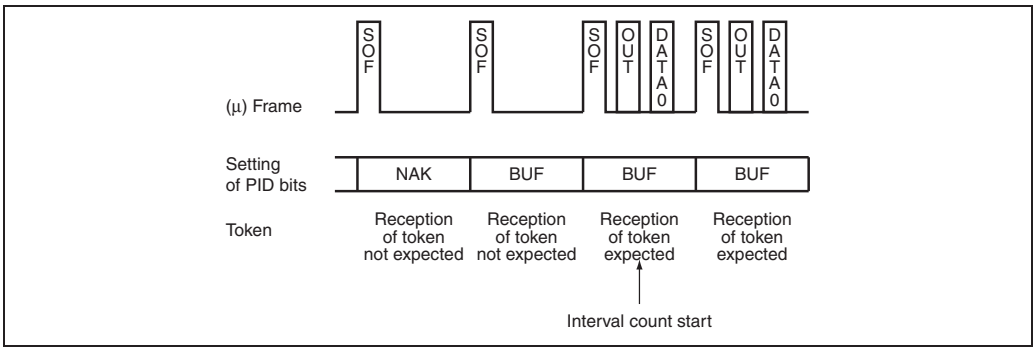


Figure 33.14 (μ) Frames and Expectation of Receiving a Token when IITV = 0

- When IITV ≠ 0: The interval count starts from the time when this module successfully receives the first data packet after the PID bits for the selected pipe is changed to BUF.

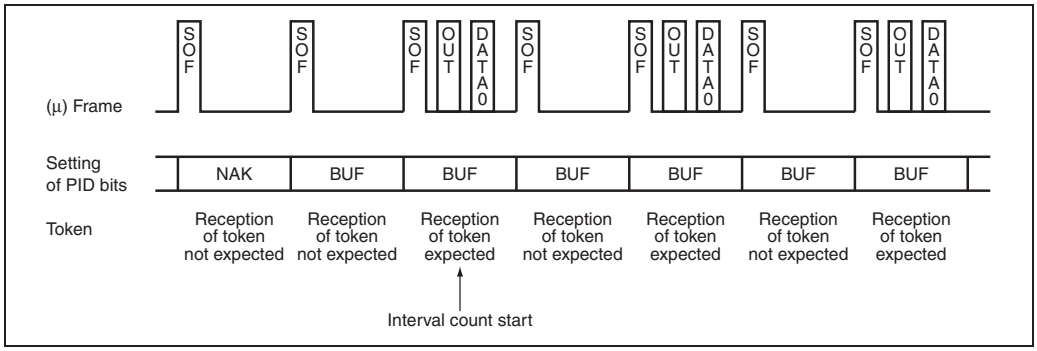


Figure 33.15 (μ) Frames and Expectation of Receiving a Token when IITV ≠ 0

2. When the selected pipe is Isochronous-IN transfer pipe

   Use the selected pipe by combining with the setting of IFIS = 1. When IFIS = 0, this module sends data packets in response to received tokens irrespective of the IITV value.

   When this module receives no IN-Token in (μ) frames at the intervals specified by the IITV bits with transmittable data stored in the FIFO buffer with IFIS = 1, this module clears the FIFO buffer.

   When this module cannot receive data due to a CRC error or another bus error in the IN-Token, this module also clears the FIFO buffer.

   The FIFO buffer is cleared at the SOF packet receive timing. Even if the SOF packet is damaged, this module clears the FIFO buffer at the SOF packet receive timing using the internal interpolation function.

   The interval count start conditions vary with the set IITV value (same as Isochronous-OUT transfer).

   When the function controller function is selected, the interval count start conditions are as follows:

   — When this module is reset by the hardware (The set IITV value is also cleared to 0.)
   — When ACLRM is set to 1 by the software
   — When this module detects a USB reset

(4) Transmit Data Setup in Isochronous Transfer when the Function Controller Function is Selected

In isochronous data transmission when the function controller function is selected, this module can send a data packet in the next frame after this module detects an SOF packet after writing data to the buffer. This function is referred to as the isochronous transfer transmit data setup function. With this function, the frame that started data transmission can be identified.

When the buffer memory is used as a double buffer, even if writing data to both buffers is completed, only one side that finished writing earlier becomes transferable. For this reason, even if multiple IN tokens are received in the same frame, only one packet of the buffer memory is sent.

When the buffer memory is ready for transmission in the IN token reception cycle, this module sends data and an ACK response. However, when the buffer memory is not ready for transmission, this module sends a Zero-Length packet and generates an underrun error.

Figure 33.16 shows an example of transmission using the isochronous transfer transmit data setup function of this module when IITV = 0 (each frame). Transmission of a Zero-Length packet is indicated as hatched “Null” in the figure.

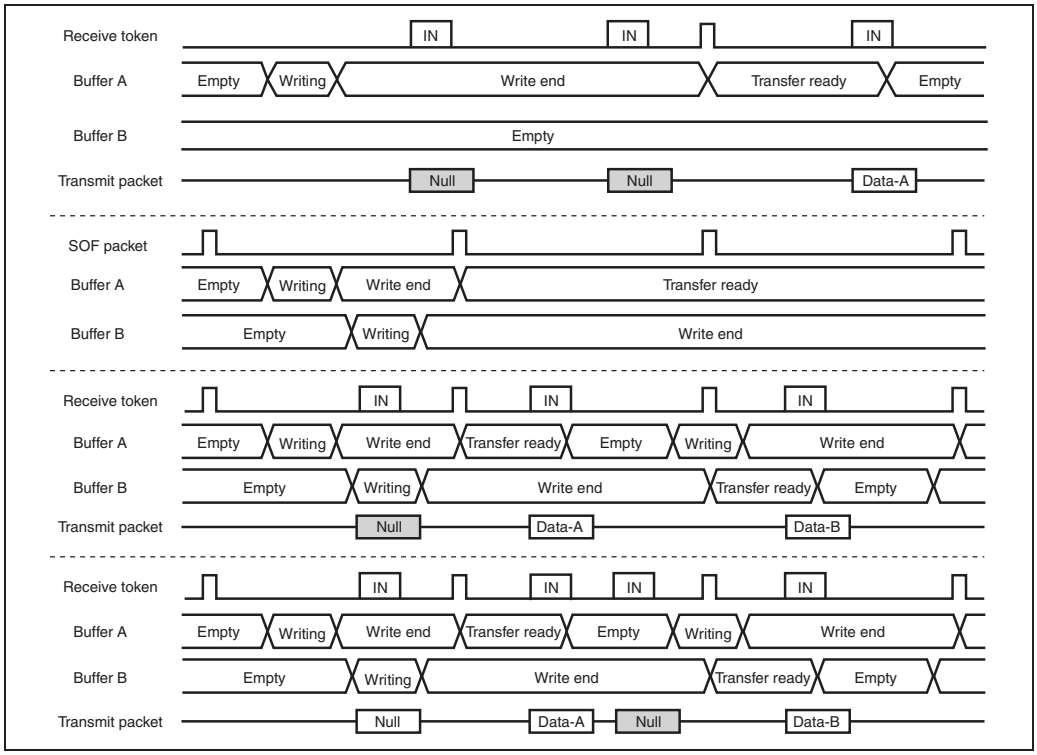


Figure 33.16 Example of Transmit Data Setup Function

(5) Transmit Buffer Flush in Isochronous Transfer when the Function Controller Function is Selected

In isochronous data transmission when the function controller function is selected, this module receives no IN token in the interval frame. When this module receives the SOF or μ SOF packet of the next frame, this module regards the IN token as damaged and clears the buffer that is ready for transmission to make it writable.

At this time, when the buffer memory is used as a double buffer and writing data to both buffers is completed, this module regards the discarded buffer memory data as transmitted in the same interval frame, and drives the buffer memory that is not discarded due to the reception of an SOF or μ SOF packet into the transmission ready state.

The buffer flush function activation timing varies depending on the IITV value.

- When IITV = 0
  This module activates the buffer flush function from the next frame after the pipe is enabled.
- When IITV ≠ 0
  This module activates the buffer flush function from the first normal transaction.

Figure 33.17 shows an example of the buffer flush function of this module. For tokens before the interval frame (outside the specified interval), however, this module sends the data stored in the buffer according to the data setup state or sends a Zero-Length packet as an underrun error.

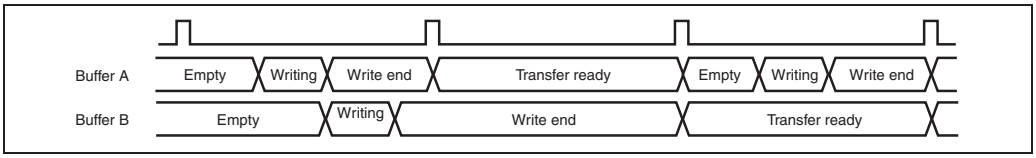


Figure 33.17 Example of Buffer Flush Function

Figure 33.18 shows an example of an interval error of this module. Interval errors are the following five. An interval error occurs at timing [1] in the figure, and the buffer flush function is activated.

When an interval error occurs, the buffer flush function is activated in the IN transfer and an NRDY interrupt occurs in the OUT transfer.

Discriminate an NRDY interrupt (including a receive packet error) from an overrun error with the OVRN bit.

This module sends a response to the hatched tokens in the figure according to the buffer memory status.

1. IN direction
   — When the buffer is ready to transmit data, this module sends the data and an ACK response.
   — When the buffer is not ready to transmit data, this module sends a Zero-Length packet and generates an underrun error.
2. OUT direction
   — When the buffer is ready to receive data, this module receives data and sends an ACK response.
   — When the buffer is not ready to receive data, this module discards the data and generates an overrun error.

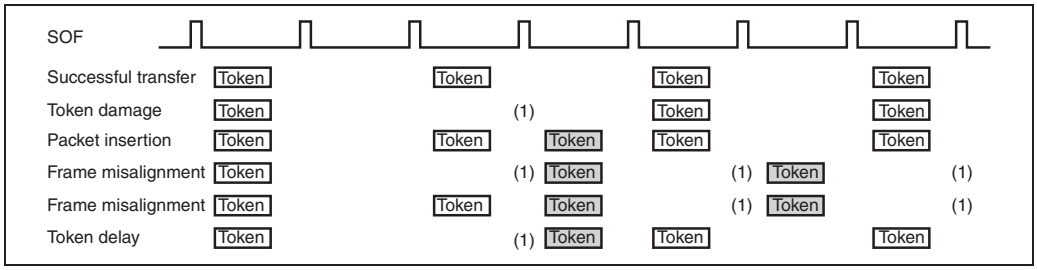


Figure 33.18 Example of Interval Error when IITV = 1

33.4.9 SOF Interpolation Function

When the function controller function is selected, in case this module cannot receive SOF packets at intervals of 1 ms (full-speed operation) or 125 μs (high-speed operation) due to damage or missing of SOF packets, this module interpolates the SOF. The SOF interpolation starts functioning when SYSCFG.USBE = 1, SYSCFG.SCKE = 1, and at the SOF packet receive timing. Furthermore, the interpolation function is initialized in the following cases.

- Power-on reset
- USB bus reset
- When the suspended state is detected

The SOF interpolation functions with the following specifications.

- The frame intervals (125 μs or 1 ms) conform to the result of the reset handshake protocol.
- The SOF interpolation does not function until this module receives an SOF packet.
- After receiving the first SOF packet, 125 μs or 1 ms is counted by the internal 48-MHz clock to interpolate the SOF.
- After receiving the second SOF packet or a following packet, the SOF is interpolated using the previous receive intervals.
- The SOF interpolation does not function in the suspended state and during a USB bus reset. (When this module enters the suspended state in high-speed operation, the SOF interpolation continues for 3 ms from the final packet.)

This module activates the following functions based on the reception of SOF packets. When one or more SOF packets are lost, normal operation can be continued to perform the SOF interpolation.

- Updating frame numbers and μ frame numbers
- SOFR interrupt timing and μ SOF lock

- Isochronous transfer interval count

When one or more SOF packets are lost in full-speed operation, the FRNM bits in FRMNUM are not updated. When one or more μ SOF packets are lost in high-speed operation, the FRNM bits are updated. However, when a μ SOF packet with UFRNM = 000 is lost, the FRNM bits are not updated even if following μ SOF packets with UFRNM ≠ 000 are successfully received.

33.4.10 Pipe Schedule

(1) Transaction Issuing Conditions

When the host controller function is selected, this module issues transactions after setting UACT = 1 according to the conditions in Table 33.29.

Table 33.29 Transaction Issuing Conditions

	Issuing Conditions				
Transaction	**DIR**	**PID**	**IITV0**	**Buffer Status**	**SUREQ**
Setup	—*1	—*1	—*1	—*1	Set to 1
Control transfer data stage, status stage, bulk transfer	IN	BUF	Disabled	Data receive area remaining	—*1
	OUT	BUF	Disabled	Transmit data stored	—*1
Interrupt transfer	IN	BUF	Enabled	Data receive area remaining	—*1
	OUT	BUF	Enabled	Transmit data stored	—*1
Isochronous transfer	IN	BUF	Enabled	*2	—*1
	OUT	BUF	Enabled	*3	—*1

Notes: 1. "—" means that the condition is not related to issuing tokens. "Enabled" shows that transactions are issued only in transfer frames by the interval counter in interrupt transfers and isochronous transfers. "Disabled" shows that transactions are issued irrespective of the interval counter.

2. Transactions are issued irrespective of whether the buffer has a data receive area or not. However, when the buffer has no data receive area, the receive data is discarded.

3. Transactions are issued irrespective of whether the buffer contains transmit data or not. However, when the buffer contains no transmit data, this module sends a Zero-Length packet.

(2) Transfer Schedule

The following describes the within-the-frame transfer scheduling of this module. This module transfers packets in the following procedure after sending the SOF.

1. Execute periodic transfer
   This module searches pipes in the order of pipe 1 -> pipe 2 -> pipe 6 -> pipe 7 -> pipe 8 -> pipe 9. When transactions can be issued in any of these pipes in isochronous transfers or interrupt transfers, this module issues transactions.
2. Control transfer setup transaction
   When the DCP indicates that the setup transaction is enabled, this module sends it.
3. Execute bulk transfer/control transfer data stage and status stage
   This module searches pipes in the order of pipe 1 -> pipe 2 -> pipe 3 -> pipe 4 -> pipe 5. When transactions can be issued in any of these pipes in the bulk transfer/control transfer data stage and control transfer status stage, this module executes transactions.
   When this module issued a transaction and received ACK or NAK from the peripheral device, this module shifts to the transactions for the next pipe. When there is time for transfer within the frame, this module repeats the operation in step 3.

(3) Enabling USB Communication

Setting the UACT bit in DVSTCTR to 1 starts transmission of an SOF or µ SOF, and issuing of transactions is enabled.

Setting the UACT bit to 0 stops transmission of an SOF or µ SOF, and issuing of transactions is suspended. When the UACT bit is changed from 1 to 0, the USB communication is halted after the next SOF or µ SOF is transmitted.

33.5 Guidelines for Designing USB2.0 Hi-Speed Boards

33.5.1 USB Transmission Line

The USB transmission line indicates the pattern that connects the USB connector and the USB transceiver with built-in this LSI.

The USB2.0 has three communication modes: Hi-Speed, Full-Speed and Low-Speed modes. The transmission speed in the Hi-Speed mode is 480 Mbps. Therefore, the USB transmission line must be designed as a high-frequency circuit. Impedance control is required for the USB transmission line.

- The characteristic impedance required for the USB Hi-Speed transmission line is differential impedance 90Ω (±15%).
- The pattern width and pattern pitch for impedance control vary depending on the board thickness, material and layer configuration. For details, consult the board manufacturer.
- A maximum delay of 1 ns is allowed from the USB connector to this LSI. Therefore it is recommended that the pattern length from the USB device to the USB connector is less than 50 mm and the difference between the pattern lengths for D+ and D– is less than 2.5 mm for a generic PCB.
- The lower layer of the USB transmission line must be a solid ground plane. The ground must be wider than the USB transmission line by 2 mm or more. The power supply for a solid ground plane is DG33.
- Do not allocate other signal lines near to the USB transmission line. In particular, lines carrying widely fluctuating signals, such as clock and data bus lines, must be assigned far from the USB transmission line. Furthermore, layout of the USB transmission lines must be such that they do not cross with other signal lines.
- Locate the USB transmission line on the same layer without passing it through a through-hole. Do not create stubs.
- Place the USB transmission lines so that they are equally spaced from each other.
- Locate the USB transmission line as far as possible from the oscillator, power supply circuit, and other I/O connectors.
- Try to avoid bending the USB transmission line as far as possible. If it is absolutely necessary to bend it, do not bend it at acute or right angles. Bend it moderately, at not more than 45 degrees, or bend it into an arc.
- It is recommended to guard ring the clock, reset, read, write and chip select signals with grounds.

When a resistance is connected to the USB transmission line, locate it near to the USB transmission line. The connecting wire must be as short as possible.

33.5.2 Power Supply and Ground Pattern

Analog power supply: AV12 (1.2V), AV33 (3.3V)

Digital power supply: UV12 (1.2V), DV12 (1.2V), DV33 (3.3V)

Analog ground: AG12, AG33

Digital ground: UG12, DG12, DG33

- It is recommended to separate power supplies and ground patterns into digital and analog.
- Connect the power supplies and grounds firmly on wide areas.
- Tantalum solid electrolytic capacitors or ceramic capacitors having excellent high-frequency characteristics are recommended as capacitors for power supplies.
- Aluminum electrolytic capacitors affect the jitter value during measurement of EYE diagram. Use the capacitors after adequately designing and testing them.
- It is recommended to place decoupling capacitors with values of 0.1uF, 0.01uF, and 0.001uF as close as possible to the USB power supply.

33.5.3 Oscillation

- Provide an oscillation circuit near the clock input pin for USB (EXTAL2). It is recommended to guard ring EXTAL2 with a ground.
- When using a crystal resonator, consult its manufacturer to determine the circuit constant.

33.5.4 VBUS

- When this LSI is used as a host controller, it must supply the VBUS power. To do this it is recommended to use a power switch IC with an overcurrent limiter for the USB power bus (hereafter called USB power swtich IC). Current limits should be deteremined on the basis of the current values of the system power supply and the USB peripheral devices to be communicated with. For details on circuits, see the datasheet of your USB power switch IC. Input VBUS (5V) to the VBUS1_1 pin of this LSI. Provide the VBUS1_1 pin with a capacitance of 1uF and a resistance of 100Ω to 1000Ω (never exceeding 1000Ω) as a filter circuit. The potential of the VBUS is normally 5.0V, but when a cable is connected, overshoot may occur as a result of a reflection due to impedance mismatch between the VBUS power IC

and the VBUS in the cable. This overshoot can damage elements. For this reason, the element shown in Figure 33.1, Connection to the USB Connector, should be connected between the VBUS1_1 pin and the connector as a filter circuit.

33.5.5 REFRIN_1 Pin

- Provide a resistor (hereafter called reference resistor) of 5.6 kΩ ±1%, between the REFRIN_1 pin and AG33.
- Locate the reference resistor as close as possible to this LSI.
- The REFRIN_1 pin, the reference resistor and AG33 should be wired on wide areas and the shortest length.
- Use a wiring pattern for and only for the reference resistor and AG33. The pattern should be connected to the analog ground. The pattern should be designed avoiding the possibility for common impedance between REFRIN_1 and other signals.
- To prevent cross talk, very-frequently switched signals such as DP_1, DM_1, clocks, and control signals for addresses and data, should not be placed near to the reference resistor, and their patterns should neither get across nor go parallel to the wiring pattern between the reference resistor and the REFRIN_1 pin.

It is recommended to guard ring the reference resistor and its wiring pattern with ground.

Section 34 Capture Engine Unit (CEU)

The CEU is a capture module that fetches image data externally input and transfers it to the memory. The CEU is connected to the system bus via bus bridge modules.

34.1 Features

Lists the fetures of CEU as follows.

(1) Image data fetch

- Captures an image output from an external module and writes YCbCr data to the memory with it separated into Y data and CbCr data.
- Fetches image data other than YCbCr data, e.g. JPEG data, from an externally connected module, such as a camera, and sequentially writes the image data to the memory.
- Fetches an interlace source image in both-field units or one-field units and writes it to the memory. In both-field capture, an image can be stored in the memory as a frame image.

(2) Filter processing

- Performs scale-down and removal of high-frequency components (only in the horizontal direction) for an image using internal filters. Note that the scaled-down image must not exceed VGA. The filter processing can be applied to only YCbCr input data.

(3) Display information acquisition

- Acquires the complexity level of the captured display and writes it to the memory. This information output at MPEG-4 encoding is useful for determining the scene change.

(4) Format conversion

- Converts image data input in the YCbCr 4:2:2 format into the YCbCr 4:2:0 format and writes it to the memory.Note that the conversion algorithm is simple skipping in which the chrominance component (CbCr) of the even-numbered lines is skipped.

The functional overview of the CEU is shown in table 34.1.

List the two homologous series for the interface connecting to camera as follows.

- 16-bit input for parallel-I/F camera.
- 32-bit input from CSI2C.

This LSI does not support strobe function. Do not attempt to write to the register that controls strobe function.

Table 34.1 Functional Overview of CEU

Classification	Item	Function	Description	Note
Connectable camera	Size	Maximum	8188 pixels × 8188 lines	Horizontal: 4-pixel units
		64M pixels		Vertical: 4-line units
		Minimum	48 pixels × 48 lines	

Classification	Item	Function	Description	Note
Connectable camera	Input format	YCbCr 4:2:2 8 bits	Cb_0, Y_0, Cr_0, $Y_{1...}$	Supports clock ratio of 1:1.
			Cr_0, Y_0, Cb_0, $Y_{1...}$	
			Y_0, Cb_0, Y_1, $Cr_{0...}$	
			Y_0, Cr_0, Y_1, $Cb_{0...}$	
		YCbCr 4:2:2 16 bits	{Y0, Cb0}, {Y1, Cr0}, …	
			{Y0, Cr0}, {Y1, Cb0}, …	
		Binary data	Binary data such as JPEG	Written sequentially
	Horizontal and vertical sync signal polarities	Arbitrary	High-active and low-active	
	Capture start location	Arbitrary	Can be specified in camera input clock units.	Horizontal: 1-cycle units Vertical: 1-HD (horizontal sync signal) units
	Number of captured pixels	Arbitrary	Can be specified in 4-pixel units horizontally and in 4-line units vertically.	
	Interlace	Both-field capture	Stored as a field image	Capture: 2-VD (vertical sync signal period) units
			Stored as a frame image	
		One-field capture	Top field or bottom field can be specified	Capture: 1-VD units
Memory write	Output format	YCbCr 4:2:2 YCbCr 4:2:0	YCbCr 4:2:0 is realized by simple skipping.	

Classification	Item	Function	Description	Note
Strobe function (not supported in this LSI)	Strobe control	Automatic mode	Emission time is controlled by to the emission start counter, strobe exposed signal, or vertical sync signal.	Emission start = Register setting Emission stop = Strobe exposed signal Emission start = Register setting Emission stop = Register setting Emission start = Vertical sync signal Emission stop = Vertical sync signal
		Manual mode	Emission pin is controlled by modifying the register.	Emission start = Modifying the register Emission stop = Clearing the register
Filter function	No scaling or scale-down	Scale-down of captured display	Desired scaling factor from 1/16 to 1 (scaled-down display-width must be 2048 pixels or less horizontally)	
	Low-pass filter		Removal of high-frequency components	Only in the horizontal direction
Display information acquisition	Complexity level	Acquisition of complexity level of captured display	Variation of pixel values is indicated	Used for MPEG-4 16-line units, 8-line units, or 1-display units can be selected

Figure 34.1 shows a block diagram of the CEU.

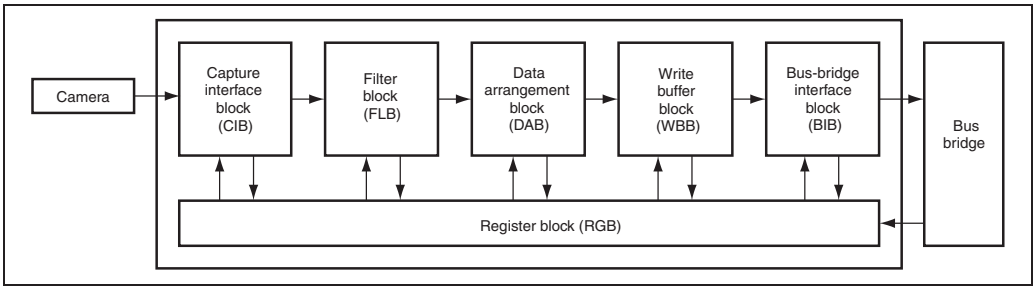


Figure 34.1 Block Diagram of CEU

34.2 Pin Configuration of CEU

The pin configuration of the CEU is shown in table 34.2. And, connected image is shown in Figure 34.2.

Table 34.2 Pin Configuration of CEU

Pin Name	Function	I/O	Description
VIO_D15 to VIO_D0	Main camera data bus	Input	Camera image data input from the main camera
VIO_CLK	Main camera clock	Input	Camera clock input from the main camera
VIO_VD	Main camera vertical sync	Input	Camera vertical sync signal input from the main camera
VIO_HD	Main camera horizontal sync	Input	Camera horizontal sync signal input from the main camera
VIO_FLD	Field signal	Input	Field identification signal
VIO_CKO	Camera clock output	Output	Clock output to the camera

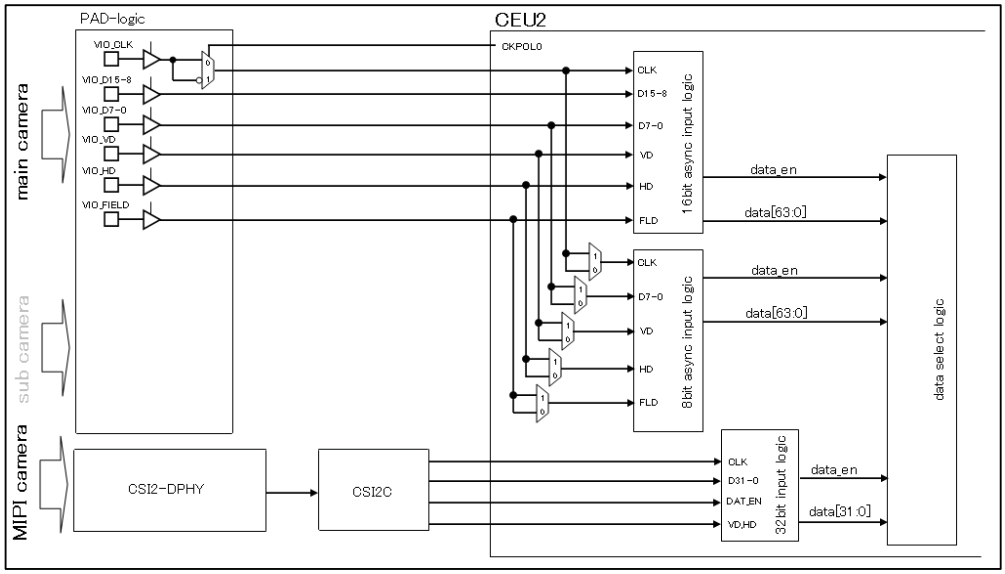


Figure 34.2 shows a connection image

34.3 Description of CEU Registers

The register configuration of the CEU is shown in table 34.3. The register states in each processing mode are shown in table 34.3.

Most CEU registers have a 2-plane configuration (plane A and plane B). The CEU switches the planes when using these 2-plane registers. A mirror address, which is an address that can always access the register on the unused plane, is provided for each 2-plane register. Figure 34.3 shows the timing to switch the register planes. The CEU switches the register planes at the same time a VD interrupt is asserted.

In the following register descriptions, "during operation" indicates the period that begins when the CEU is activated by the CE bit in the capture start register (CAPSR) and ends when a capture end interrupt (CPE) of the capture event flag clear register (CETCR) occurs. In the read-only bits in each register, the write value should always be 0. If a value other than 0 is written to any of these bits, correct operation cannot be guaranteed.

Table 34.3 Register Configuration of CEU

			Addresses			
Register Name	Abbr.	R/W	Address (Plane A)	Address (Plane B)	Mirror Address	Access Size
Capture start register	CAPSR	R/W	H'FE91 0000	—	—	32
Capture control register	CAPCR	R/W	H'FE91 0004	—	—	32
Capture interface control register*	CAMCR	R/W	H'FE91 0008	—	—	32
Capture interface cycle register*	CMCYR	R/W	H'FE91 000C	—	—	32
Capture interface offset register	CAMOR	R/W	H'FE91 0010	H'FE91 1010	H'FE91 2010	32
Capture interface width register	CAPWR	R/W	H'FE91 0014	H'FE91 1014	H'FE91 2014	32
Capture interface input format register	CAIFR	R/W	H'FE91 0018	—	—	32
Camera strobe control register	CSTCR	R/W	H'FE91 0020	—	—	32
Camera strobe emission count register	CSECR	R/W	H'FE91 0024	—	—	32
CEU register control register	CRCNTR	R/W	H'FE91 0028	—	—	32
CEU register forcible control register	CRCMPR	R/W	H'FE91 002C	—	—	32
Capture filter control register	CFLCR	R/W	H'FE91 0030	H'FE91 1030	H'FE91 2030	32
Capture filter size clip register	CFSZR	R/W	H'FE91 0034	H'FE91 1034	H'FE91 2034	32
Capture destination width register	CDWDR	R/W	H'FE91 0038	H'FE91 1038	H'FE91 2038	32

Register Name	Abbr.	R/W	Addresses			Access Size
			Address (Plane A)	Address (Plane B)	Mirror Address	
Capture data address Y register	CDAYR	R/W	H'FE91 003C	H'FE91 103C	H'FE91 203C	32
Capture data address C register	CDACR	R/W	H'FE91 0040	H'FE91 1040	H'FE91 2040	32
Capture data bottom-field address Y register	CDBYR	R/W	H'FE91 0044	H'FE91 1044	H'FE91 2044	32
Capture data bottom-field address C register	CDBCR	R/W	H'FE91 0048	H'FE91 1048	H'FE91 2048	32
Capture bundle destination size register	CBDSR	R/W	H'FE91 004C	H'FE91 104C	H'FE91 204C	32
Firewall operating control register	CFWCR	R/W	H'FE91 005C	—	—	32
Capture low-pass filter control register	CLFCR	R/W	H'FE91 0060	H'FE91 1060	H'FE91 2060	32
Capture data output control register	CDOCR	R/W	H'FE91 0064	H'FE91 1064	H'FE91 2064	32
Capture data complexity level register	CDDCR	R/W	H'FE91 0068	H'FE91 1068	H'FE91 2068	32
Capture data complexity level address register	CDDAR	R/W	H'FE91 006C	H'FE91 106C	H'FE91 206C	32
Capture event interrupt enable register	CEIER	R/W	H'FE91 0070	—	—	32
Capture event flag clear register	CETCR	R/W	H'FE91 0074	—	—	32
Capture status register	CSTSR	R	H'FE91 007C	—	—	32
Capture software reset register	CSRTR	R/W	H'FE91 0080	—	—	32
Capture data capacity register	CDSSR	R/W	H'FE91 0084	—	—	32
Capture data address Y register 2	CDAYR2	R/W	H'FE91 0090	H'FE91 1090	H'FE91 2090	32
Capture data address C register 2	CDACR2	R/W	H'FE91 0094	H'FE91 1094	H'FE91 2094	32
Capture data bottom-field address Y register 2	CDBYR2	R/W	H'FE91 0098	H'FE91 1098	H'FE91 2098	32
Capture data bottom-field address C register 2	CDBCR2	R/W	H'FE91 009C	H'FE91 109C	H'FE91 209C	32

Note: * After changing the setting of a register (CAMCR or CMCYR) that is determined by the external module characteristics, do not start capture until at least 10 external input clock cycles have elapsed.

Table 34.4 CEU Register States in Each Processing Mode

Register Abbreviation	Reset *	Module Standby
CAPSR	Initialized	Retained
CAPCR	Initialized	Retained
CAMCR	Initialized	Retained
CMCYR	Initialized	Retained
CAMOR	Initialized	Retained
CAPWR	Initialized	Retained
CAIFR	Initialized	Retained
CSTCR	Initialized	Retained
CSECR	Initialized	Retained
CRCNTR	Initialized	Retained
CRCMPR	Initialized	Retained
CFLCR	Initialized	Retained
CFSZR	Initialized	Retained
CDWDR	Initialized	Retained
CDAYR	Initialized	Retained
CDACR	Initialized	Retained
CDBYR	Initialized	Retained
CDBCR	Initialized	Retained
CBDSR	Initialized	Retained
CLFCR	Initialized	Retained
CDOCR	Initialized	Retained
CDDCR	Initialized	Retained
CDDAR	Initialized	Retained
CEIER	Initialized	Retained
CETCR	Initialized	Retained
CSTSR	Initialized	Retained
CSRTR	Initialized	Retained
CDAYR2	Initialized	Retained
CDACR2	Initialized	Retained
CDBYR2	Initialized	Retained
CDBCR2	Initialized	Retained

* For details, refer to section 1-D Overview of reset.

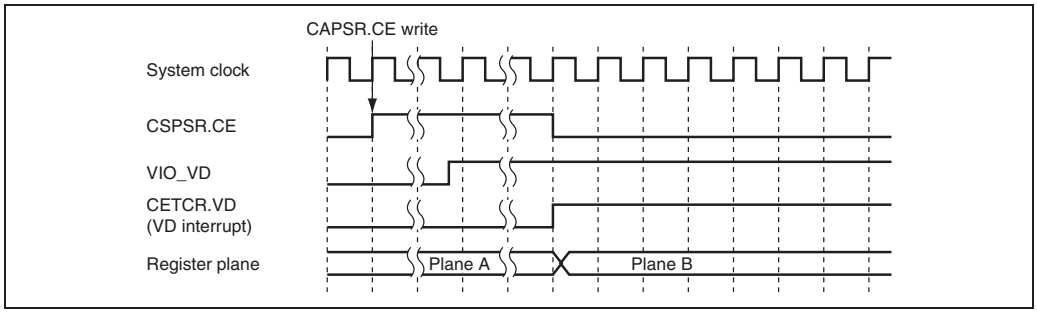


Figure 34.3 Register Plane Switching Timing (VD Polarity is High-Active)

34.3.1 Capture Start Register (CAPSR)

CAPSR captures data input to the CEU from an external module.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CPKIL
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	CPKIL	0	R/W	Write 1 to this bit to perform a software reset of capturing. At a software reset, capturing ends immediately without completing capture operation until the end of a frame. Clear the CE bit to 0 when writing 1 to this bit. Processing of the capture software reset is indicated by this bit being set to 1. When this bit is 1, do not start capturing since reset processing is in progress. When restarting capture operations, after referring to the CPTON bit in CSTSR to ensure that the CEU is halted (in the idle state), wait until this bit is cleared to 0. The timing of restarting capture operations is shown in figure 34.7. When a software reset is generated by this bit, a capture end interrupt (CPE bit in CETCR) may be output immediately after the software reset. However, such kind of interrupt should be ignored. Also, even if the capture end interrupt is not output, the interrupt source (CPE bit) must be cleared before capturing of the next frame. 0: Normal state 1: Software reset of capturing
15 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
0	CE	0	R/W	• Single-capture This bit reserves capturing of the next frame. When 1 is written to this bit, the capture of one frame starts from the next VD input, and stops when the one-frame capture end interrupt (CPE bit in CETCR) is asserted (figure 34.8). To perform capture again, write 1 to this bit. After the VD or HD polarity is changed, do not write 1 to this bit until the next VD interrupt is asserted. As this bit indicates the capture reserve state, this bit is read as 1 after it is set to 1 and until VD is input. When VD is input, this bit returns to 0 and so is read as 0. The capture end is determined by the one-frame capture end interrupt (CPE bit). This is similar in data fetch mode. Registers should be set before the VD interrupt of the frame where capture starts next. The new register settings take effect at the next VD input. When registers are modified during capturing, the register settings take effect from the capture operations of the next VD input. If a setting register to which writing during capturing is prohibited is modified during capturing, an interrupt source (IGRW bit in CETCR) is generated. For details on the interrupt source, see the description on CETCR. • Continuous capture When this bit is set to 1 while the CTNCP bit in CAPCR is set to 1, continuous capture starts from the next frame (figure 34.9). Note that this bit is not cleared to 0 but remains as 1. To stop capturing, clear this bit to 0; capturing stops after the current frame is completed. Continuous capture operations are possible in only image capture mode. The start address of the memory to which the captured data is written to must be set for each frame. 0: Stops capturing. 1: Starts capturing.

When both the VD (vertical sync signal) and HD (horizontal sync signal) polarities are high-active, one frame is defined as a period from a VD rising edge to the next VD rising edge, and one line as a period from an HD rising edge to the next HD rising edge. Figure 34.4 shows the timing of one frame (when both the VD and HD polarities are high-active).

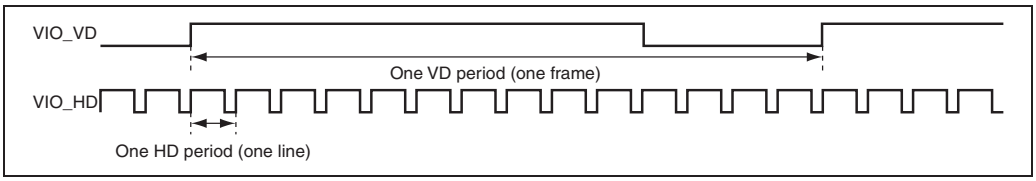


Figure 34.4 Frame Timing

When both the VD and HD polarities are high-active, similar to one frame, one field is defined as follows:

- Period from a VD rising edge to the next VD rising edge
- One line is a period from an HD rising edge to the next HD rising edge.

The field identification signal FLD should be fixed for at least 1-HD period from a VD input. Figure 34.5shows the timing of one field (when both the VD and HD polarities are high-active).

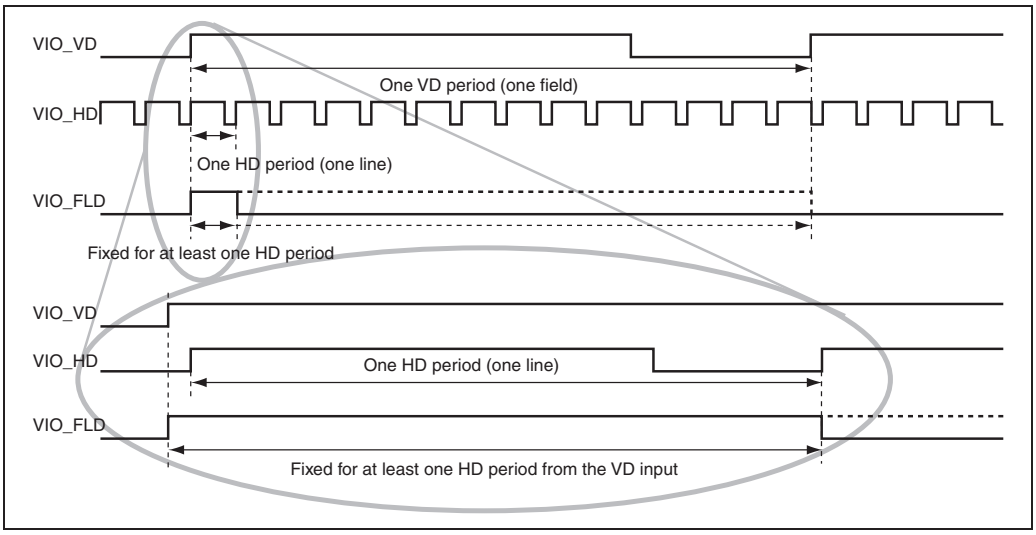


Figure 34.5 One Field Timing

In data enable fetch, one frame is defined as a period from a VD rising edge to the VD falling edge. With the HD as an enable signal (positive polarity), data of a cycle in which the HD is asserted is fetched while the VD is high. Figure 34.6 shows the timing of one frame for data enable fetch.

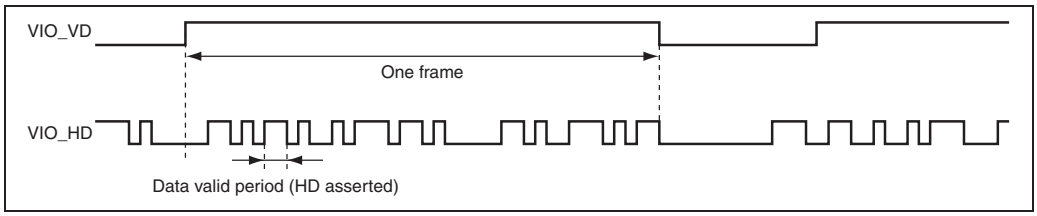


Figure 34.6 Frame Timing (Data Enable Fetch)

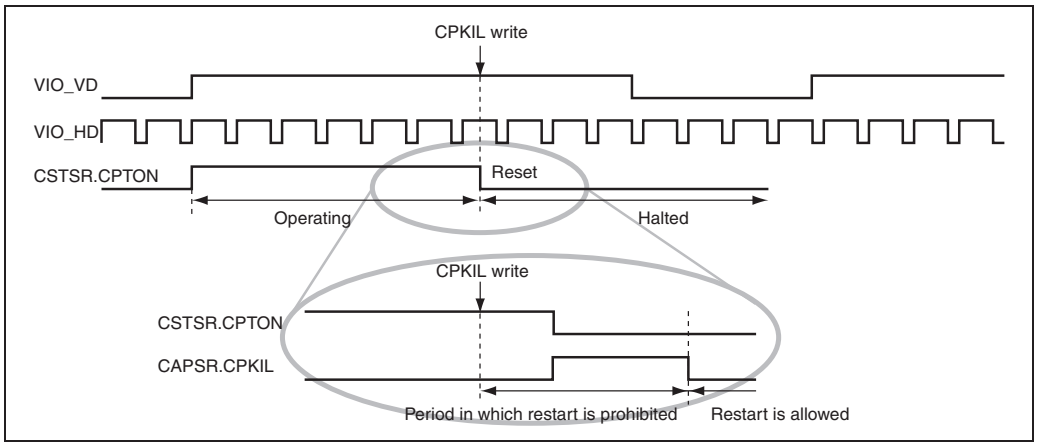


Figure 34.7 Timing of Software Reset and Restart of Capturing

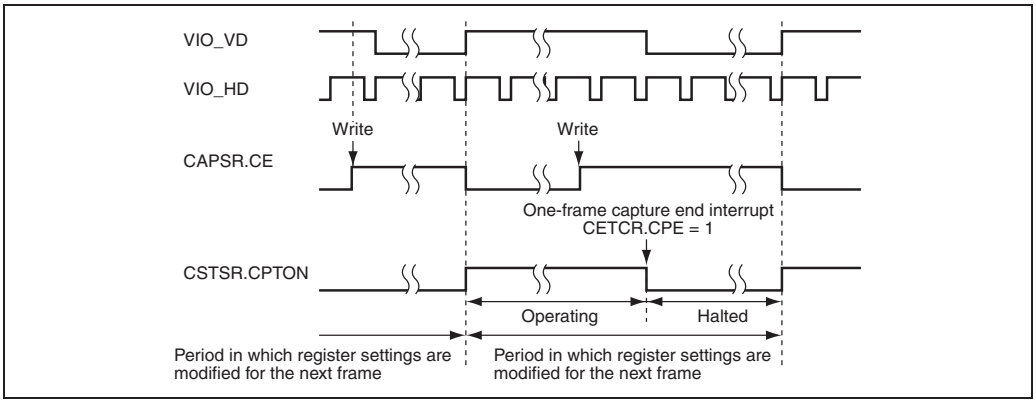


Figure 34.8 Timing of Modifying CE Bit and Register Setting in One Frame Capture

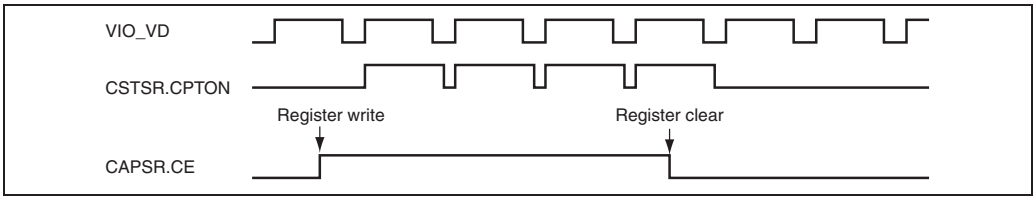


Figure 34.9 Continuous-Frame Capture

34.3.2 Capture Control Register (CAPCR)

CAPCR sets continuous-frame capture and the frame drop intervals.

Do not modify this register during operation. If this register is modified during operation, correct operation cannot be guaranteed. In addition, the IGRW bit (interrupt source) in CETCR is set to B'1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	FDRP[7:0]								—	—	MTCM[1:0]		—	—	—	CTNCP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	FDRP[7:0]	H'00	R/W	These bits set the frame drop interval in continuous-frame capture. When these bits are cleared to 0, frame drop is not performed, and all frames are captured. Figure 34.10 shows the value set in these bits and the timing of captured frames. The frame drop interval unit differs according to the capture setting. Table 34.5shows the relationship between the capture setting and frame drop interval unit. The image of the frame drop timing for each capture setting when these bits are set to 2 is shown in figure 34.11. In both-field capture, capturing is performed continuously for 2-VD periods, regardless of whether the second field is the top field or bottom field. In addition, in both-field capture, the frame drop counter is incremented when the first field has been identified as the top field or bottom field, regardless of whether the second field is the top field or bottom field.

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	FDRP[7:0]	H'00	R/W	When 0 is written to the CE bit in CAPSR, capturing terminates after the current frame has been captured for a capture frame. However, for a drop frame, capturing is forcibly terminated in the CEU so no capture end interrupt (CPE bit in CETCR) is output. Note: Do not change the setting of these bits during continuous capture operations. To change the setting of these bits, stop continuous capture (CE bit = 0), clear the CTNCP bit (continuous capture) in CAPCR to 0, and then restart continuous capture. Continuous capture is performed during the period of CAPSR.CE = 1 shown in figure 34.10.
23, 22	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
21, 20	MTCM[1:0]	00	R/W	These bits specify the unit for transferring data to a bus bridge module. The access efficiency of SDRAM where the image data is to be stored can be improved by continuously accessing the addresses. To improve the write efficiency, set these bits to 11. The setting of these bits appears to be unchanged from the outside. 00: Transferred to the bus in 4-burst 1-transfer (4QW × 1) units 01: Transferred to the bus in 4-burst 2-transfer (4QW × 2) units 10: Transferred to the bus in 4-burst 4-transfer (4QW × 4) units 11: Transferred to the bus in 4-burst 8-transfer (4QW × 8) units (1) Image capture 00: Y data and C data are transferred in 4QW units. 01: Y data and C data are transferred in 4QW × 2 units. 10: Y data and C data are transferred in 4QW × 4 units. 11: Y data and C data are transferred in 4QW × 8 units. (2) Data fetch 00: Data is transferred in 4QW units. 01: Data is transferred in 4QW × 2 units. 10: Data is transferred in 4QW × 4 units. 11: Data is transferred in 4QW × 8 units.

Bit	Bit Name	Initial Value	R/W	Description
19 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	CTNCP	0	R/W	When capturing is started with this bit set to 1, capturing continues until the CE bit in CAPSR is cleared to 0 or a software reset is initiated by the CPKIL bit in CAPSR (see figure 34.10). Continuous capture must be set before capturing is started. This bit is modified only after 0 is written to the CE bit to stop capturing. If this bit is modified during capturing, correct operation cannot be guaranteed. In data fetch mode, clear this bit to 0. 0: One-frame capture when the CE bit is 1 1: Continuous capture until the CE bit is cleared to 0
15 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

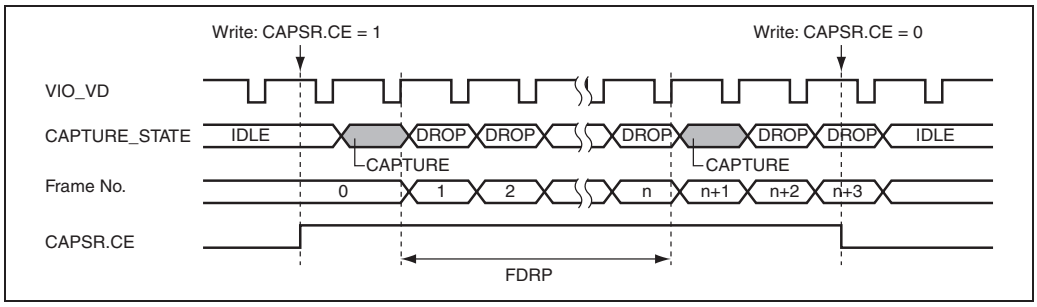


Figure 34.10 Setting of FDRP Bits and Frame Drop Timing

Table 34.5 Relationship between Capture Setting and Frame Drop Interval Unit

Input Mode	Captured Image	First Captured Image	Frame Drop Interval Unit	Capture Setting
Progressive	Frame	Frame immediately after capture start	Frame	A
Interlace	Both-field (2-VD capture)	Field immediately after capture start	2 fields (first capture field count)	B
				C
		Top field	2 fields (top-field count)	D
		Bottom field	2 fields (bottom-field count)	E
	One-field (1-VD capture)	Field immediately after capture start	First capture field	F
				G
		Top field	Top field	H
		Bottom field	Bottom field	I

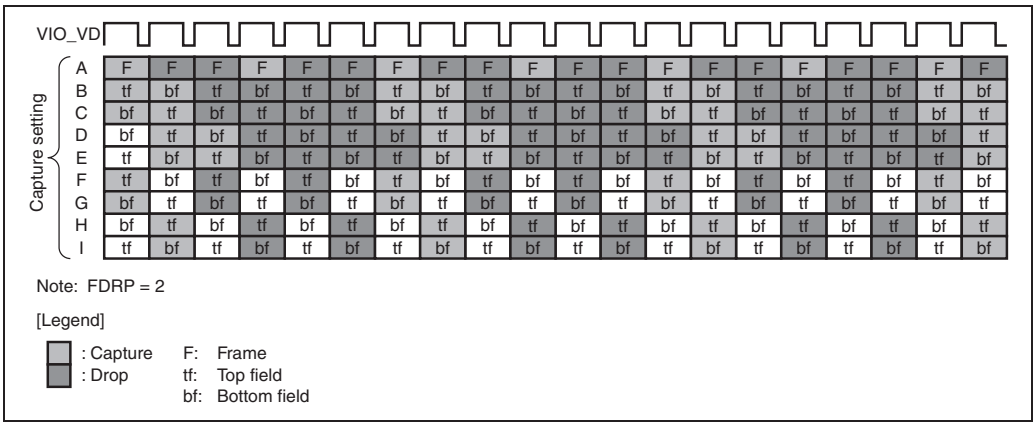


Figure 34.11 Image of Frame Drop Timing for Capture Settings (FDRP Bits = 2)

34.3.3 Capture Interface Control Register (CAMCR)

CAMCR sets the capture interface.

The following items are set by CAMCR.

- Selection between image capture operation or data fetch operation
- Polarities of the vertical and horizontal sync signals
- Input order of image data components (Y, Cb, and Cr) (only for image capture mode)
- Selection of digital image input pins (8 bits or 16 bits)
- Polarity of the field identification signal

CAMCR must be set according to the module connected. In data fetch mode, set the DTARY bits to B'0. Do not modify this register during operation. If this register is modified during operation, correct operation cannot be guaranteed. In addition, the IGRW bit (interrupt source) in CETCR is set to B'1.

Note: After changing the setting of this register, do not start capture until at least 10 external input clock cycles have elapsed.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FLDPOL
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	DTIF[1:0]		—	—	DTARY[1:0]		—	—	JPG[1:0]		—	—	VDPOL	HDPOL
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
16	FLDPOL	0	R/W	Sets the polarity of the field identification signal (FLD) from an external module. 0: When the FLD signal is high-active, the field is detected as the top field and when low-active, the field is detected as the bottom field. 1: When the FLD signal is low-active, the field is detected as the top field and when high-active, the field is detected as the bottom field.
15 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13, 12	DTIF[1:0]	00	R/W	00: Sub camera 8-bit input 01: Main camera 16-bit input 10: Main camera 8-bit input 11: CSI2 32-bit input
11, 10	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
9, 8	DTARY[1:0]	00	R/W	These bits set the input order of the luminance component and chrominance component. The order in which the luminance component (Y) and chrominance component (Cb and Cr) are input from an external module differs among modules. The CEU supports the input orders shown in figure 34.12. Set the corresponding value in these bits. In data fetch mode, set these bits to 00. (1) 8-bit interface 00: Image input data is fetched in the order of Cb_0, Y_0, Cr_0, and Y_1. 01: Image input data is fetched in the order of Cr_0, Y_0, Cb_0, and Y_1. 10: Image input data is fetched in the order of Y_0, Cb_0, Y_1, and Cr_0. 11: Image input data is fetched in the order of Y_0, Cr_0, Y_1, and Cb_0. (2) 16-bit interface 00: Image input data is fetched in the order of {Cb0, Y0}, {Cr0, Y1}. 01: Image input data is fetched in the order of {Cr0, Y0}, {Cb0, Y1}. 10: Image input data is fetched in the order of {Y0, Cb0}, {Y1, Cr0}. 11: Image input data is fetched in the order of {Y0, Cr0}, {Y1, Cb0}.

Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	00	R	Reserved These bits are always read as 0. The write value should always be 0.
5, 4	JPG[1:0]	00	R/W	Selects the fetched data type. 00 Image capture mode (input data is separated into Y data and CbCr data when stored in the memory) 01 Data fetch mode (input data is written to the specified memory addresses in the input order) 10: Data enable fetch mode (Fetch the input data by enabling HD and output to the designated address in the input order) 11: Setting prohibited
3, 2	—	00	R	Reserved These bits are always read as 0. The write value should always be 0.
1	VDPOL	0	R/W	Sets the polarity for detection of the vertical sync signal input from an external module. Figure 34.15 shows the relationship between the VD and VD interrupt when high-active is selected. Since a VD interrupt may occur when this bit value is modified, the VD bit in CETCR must always be cleared to 0 when this bit value is changed. This bit cannot be used in data enable fetch mode. 0: Vertical sync signal (VD) from an external module is detected as high-active. 1: Vertical sync signal (VD) from an external module is detected as low-active.

Bit	Bit Name	Initial Value	R/W	Description
0	HDPOL	0	R/W	Sets the polarity for detection of the horizontal sync signal input from an external module. Figure 34.16 shows the relationship between the HD and HD interrupt when high-active is selected. Since an HD interrupt may occur when this bit value is modified, the HD bit in CETCR must always be cleared to 0 when this bit value is changed. Set to 0 in data enable fetch mode. 0: Horizontal sync signal (HD) from an external module is detected as high-active. 1: Horizontal sync signal (HD) from an external module is detected as low-active.

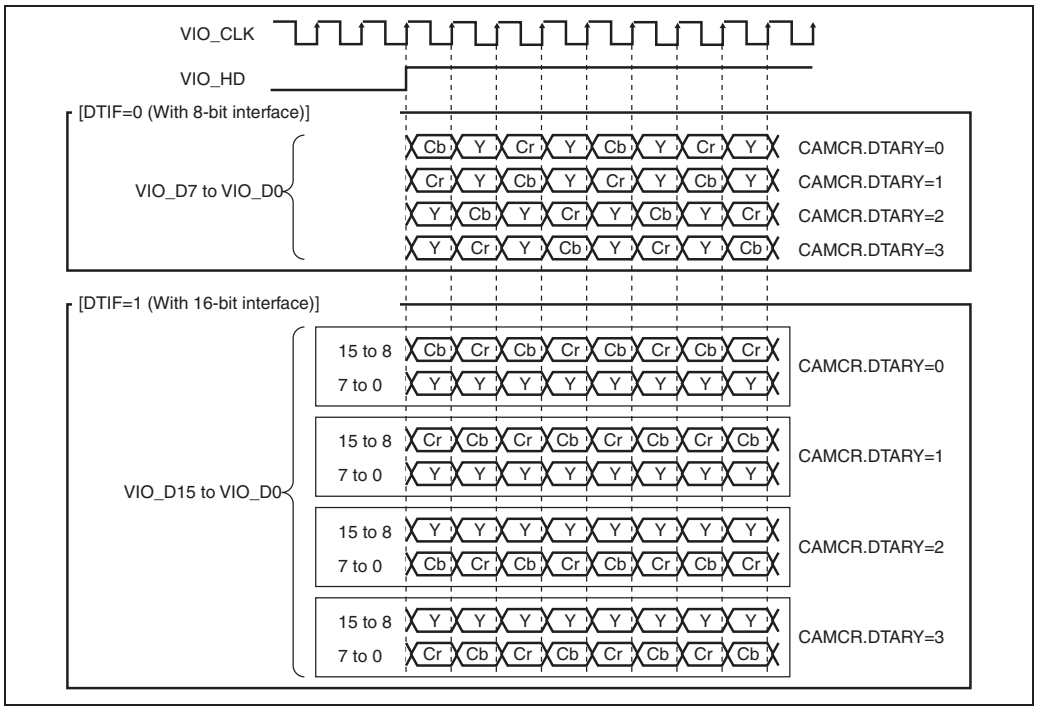


Figure 34.12 Input Order of Image Data

The JPG bit in CAMCR selects whether digital image data is fetched or data such as JPEG is fetched. In addition, when data such as JPEG is fetched, select whether the specified amount of data is continuously fetched in synchronization with the sync signal or data is fetched while the horizontal sync signal is enabled.

In data enable fetch mode, one frame is defined as a period from the rising edge to the falling edge of the vertical sync signal (VD) for data fetching. The horizontal sync signal (HD) is enabled only when the VD is high and treated as an enable signal. Data input in the cycle in which the HD is asserted (high) is fetched and output to the memory continuously.

Figures 34.13 and 34.14 show the interface timing in data enable fetch mode.

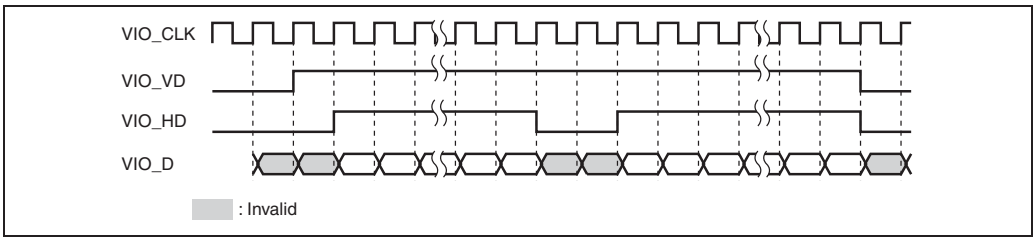


Figure 34.13 Data Enable Fetch Timing (HD Asserted (High) While VD is High)

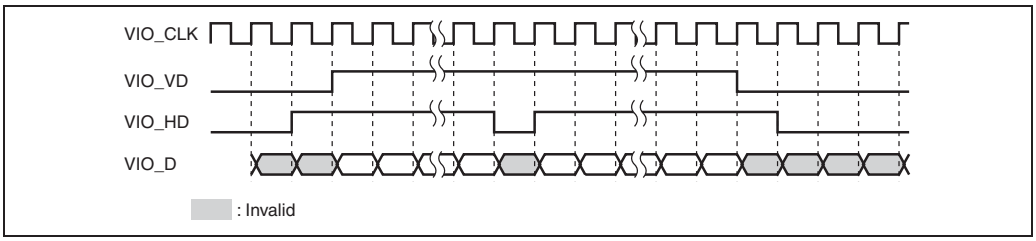


Figure 34.14 Data Enable Fetch Timing (HD Asserted (High) When VD is Not High)

This module starts fetching data at the rising edge of the VD and stops fetching data at the falling edge of the VD in data enable fetch mode. Thus, if the VD remains high and does not go low, end processing does not start. In addition, if the VD remains high and the HD also remains asserted, data continues to be fetched.

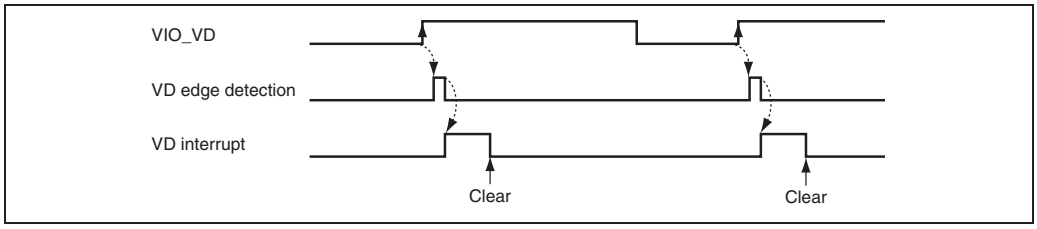


Figure 34.15 Relationship between VIO_VD and VD Interrupt when VD is High-Active

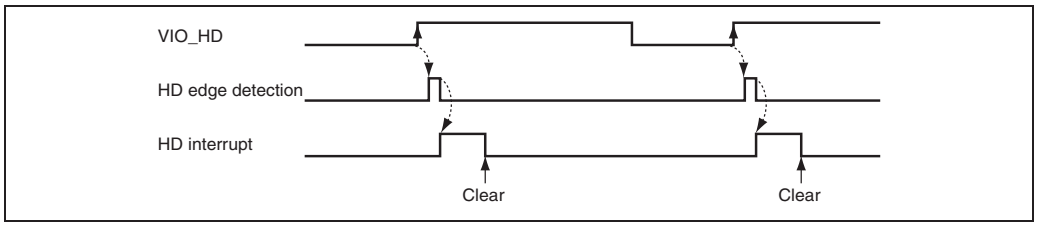


Figure 34.16 Relationship between VIO_HD and HD Interrupt when HD is High-Active

34.3.4 Capture Interface Cycle Register (CMCYR)

CMCYR is used to detect an illegal VD and an illegal HD. For HD, the number of cycles from a rising edge of HD to the next rising edge is set (falling edges when low-active is selected for HD). For VD, the number of HD inputs from a rising edge of VD to the next rising edge is set (falling edges when low-active is selected for VD).

Do not modify this register during operation. If this register is modified during operation, correct operation cannot be guaranteed. In addition, the IGRW bit (interrupt source) in CETCR is set to B'1.

In data enable fetch mode, set 0 to all the bits in CMCYR register.

Note: After changing the setting of this register, do not start capture until at least 10 external input clock cycles have elapsed.

BIT:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	VCYL[13:0]													
initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BIT:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	HCYL[14:0]														
initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29 to 16	VCYL[13:0]	H'0000	R/W	Vertical HD Count of External Module These bits set the number of VD cycles of an external module with the number of HD inputs. The interrupt source bit IGVS in CETCR is set to 1 when the actual number of VD cycles input from the external module differs from this setting. Set these bits for detecting an illegal VD. When these bits are all cleared to 0, the interrupt source bit IGVS in CETCR is not set to 1. Though the interrupt source bit IGVS in CETCR may be set to 1 after the VDPOL bit (VD polarity) in CAMCR is changed, this interrupt should be ignored.
15	—	00	R	Reserved These bits are always read as 0. The write value should always be 0.
14 to 0	HCYL[14:0]	H'0000	R/W	Horizontal Cycle Count of External Module These bits set the number of HD cycles of an external module. The interrupt source bit IGHS in CETCR is set to 1 when the actual number of HD cycles input from the external module differs from this setting. Set these bits for detecting an illegal HD. When these bits are all cleared to 0, the interrupt source bit IGHS in CETCR is not set to 1. Though the interrupt source bit IGHS in CETCR may be set to 1 after the HDPOL bit (HD polarity) in CAMCR is changed, this interrupt should be ignored.

34.3.5 Capture Interface Offset Register (CAMOR)

CAMOR sets the location to start capturing when capturing images.

Since the number of HD (horizontal sync signal) inputs from a VD (vertical sync signal) input to the start of a valid image period, and the number of clock cycles from an HD input to the start of a valid image period differ among external modules, these must be set in CAMOR. By setting a value greater than the valid image area, part of the image can be clipped for capture. When fetching data, the setting of this register becomes the number of cycles (HD count) up to the start of a valid data period.

* Caution: using of CSI2 connection mode is need special setting. Please refer to detail “34.4.4 CSI2 connetion special setting “.

This register cannot be used in data enable fetch mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	VOFST[11:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	HOFST[12:0]												
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
27 to 16	VOFST[11:0]	H'000	R/W	These bits specify the capture start location in terms of the HD count from a vertical sync signal (1-HD units). The blanking period from a vertical sync signal differs among external modules. Therefore, the vertical capture start location must be specified by these bits in terms of the HD count from a vertical sync signal so that an image can be captured from the valid image area (see figure 34.17). Some external modules output a vertical sync signal as a data enable signal. In this case, there is no blanking period so these bits must be cleared to 0 (see figure 34.17).

Bit	Bit Name	Initial Value	R/W	Description
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 0	HOFST[12:0]	H'0000	R/W	These bits specify the capture start location in terms of the number of clock cycles from a horizontal sync signal (1-cycle units). The blanking period from a horizontal sync signal differs among external modules. Therefore, the horizontal capture start location must be specified by these bits in terms of external input clock cycles from a horizontal sync signal so that an image can be captured from the valid image area. This is similar in data fetch mode (see figure 34.19). Some external modules output a horizontal sync signal as a data enable signal. In this case, there is no blanking period so these bits must be cleared to 0 (see figure 34.19). Note: The first HD (horizontal sync signal) being input simultaneously or after the first VD (vertical sync signal) is the operating condition of the CEU. These inputs are affected by the polarities (set by the VDPOL and HDPOL bits in CAMCR).

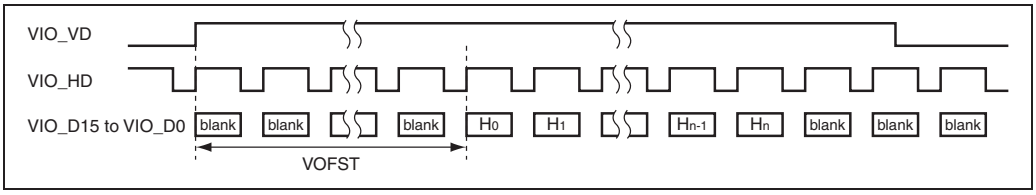


Figure 34.17 Vertical Offset

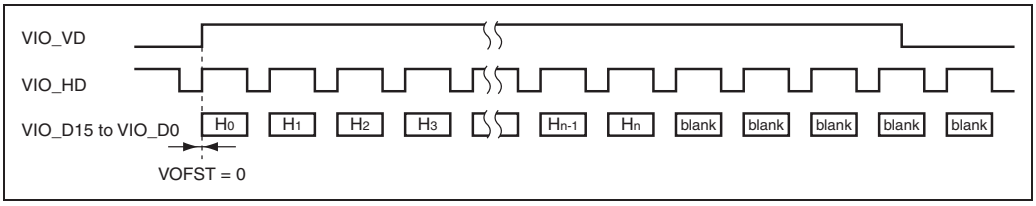


Figure 34.18 Timing when VD is Data Enable Signal

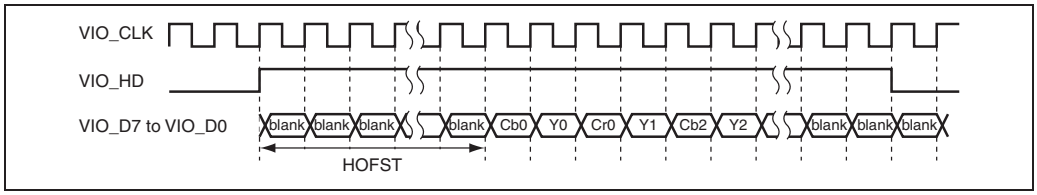


Figure 34.19 Horizontal Offset (8-Bit Interface)

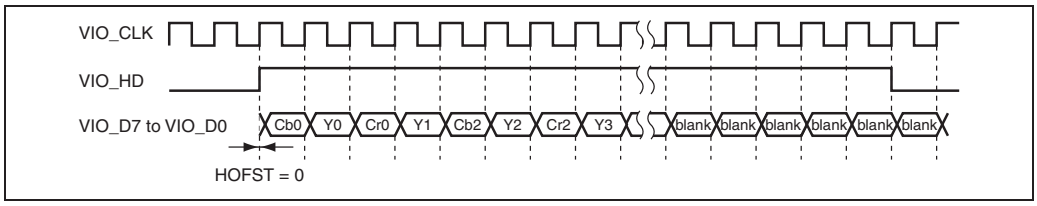


Figure 34.20 Timing when HD is Data Enable Signal (8-Bit Interface)

34.3.6 Capture Interface Width Register (CAPWR)

CAPWR sets the fetch (capture) cycle width when capturing images.

The cycle width unit differs according to the interface and whether image capturing or data fetching is performed. For each setting unit, see table 34.6.

* Caution: using of CSI2 connection mode is need special setting. Please refer to detail “34.4.4 CSI2 connetion special setting “.

This register cannot be used in data enable fetch mode.

BIT:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	VWDTH[12:0]												
initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R

BIT:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	HWDTH[13:0]													
initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 18	VWDTH[12:2]	H'000	R/W	These bits specify the vertical capture period (4-HD units). These bits specify the number of lines (HD count) to be captured from the location specified by the VOFST bits in CAMOR. Figure 34.21 shows the timing when the vertical blanking period is 0. The CEU captures for only the number of lines (HD count) specified by these bits in the vertical direction. Make a similar setting for data fetch. The maximum value to be set is 8188 HD.
17, 16	VWDTH[1:0]		R	
15,14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
13 to 1	HWDTH[13:1]	H'0000	R/W	These bits specify the horizontal capture period.
0	HWDTH[0]		R	These bits specify the number of cycles to be captured from the location specified by the HOFST bits in CAMOR. Figure 34.22 shows the timing when the horizontal blanking period is 0. The CEU captures for only the number of cycles specified by these bits in the horizontal direction. Make a similar setting for data fetch. The maximum value to be set is as follows: • 8-bit interface Image capture (8-cycle units): 8184 cycles (4092 pixels) Data fetch (4-cycle units): 4092 cycles (4092 bytes) • 16-bit interface Image capture (4-cycle units): 4092 cycles (4092 pixels) Data fetch (2-cycle units): 2046 cycles (4092 bytes) Note: In data fetch mode, set CFSZR and CDWDR according to the values set in this register. For details, see the descriptions on CFSZR and CDWDR.

Table 34.6 Unit for Setting Fetch (Capture) Cycle Width

	Vertical Direction		Horizontal Direction	
Interface	Image Capture	Data Fetch	Image Capture	Data Fetch
8-bit interface	4 HD	4 HD	8 cycles	4 cycles
16-bit interface	4 HD	4 HD	4 cycles	2 cycles

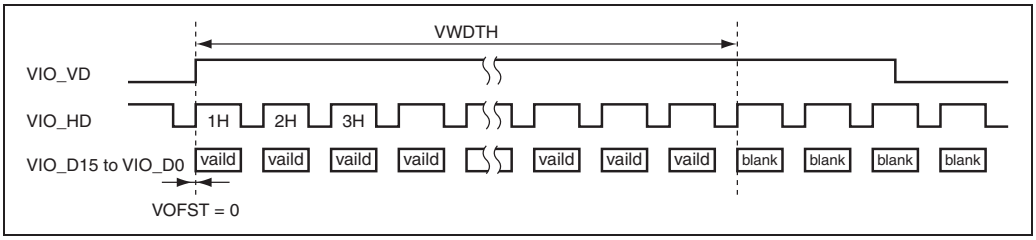


Figure 34.21 Vertical Capture Timing

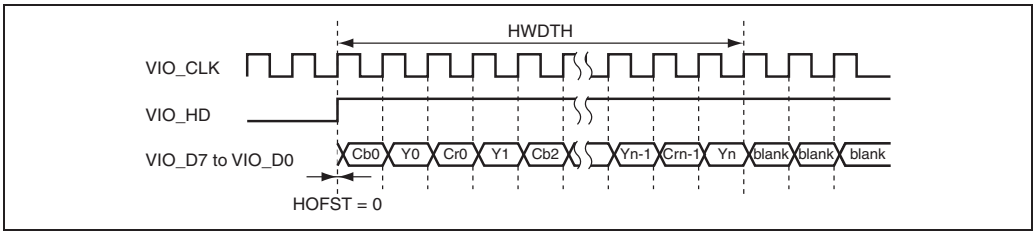


Figure 34.22 Horizontal Capture Timing (Image Capture with 8-Bit Interface)

34.3.7 Capture Interface Input Format Register (CAIFR)

CAIFR sets the input mode (progressive or interlace) for capturing images, the images to be captured (frame, both-field, or one-field), and the image from which capturing starts (top field, bottom field, etc.). CAIFR is not used in data fetch mode (CAMCR bit 4 = 1).

Do not modify this register during operation. If this register is modified during operation, correct operation cannot be guaranteed. In addition, the IGRW bit (interrupt source) in CETCR is set to B'1.

The items set by CAIFR are listed in table 34.7.

:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	IFS	–	–	–	CIM	–	CKPOL0	FC[1:0]	
:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
:	R	R	R	R	R	R	R	R/W	R	R	R	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	IFS	0	R/W	Sets the input mode for capturing images. 0: Progressive 1: Interlace
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	CIM	0	R/W	Sets the images to be captured. Clear this bit to 0 when the input mode for image capture is progressive (frame image) or when the input mode for image capture is interlace for continuous capture of both the top and bottom fields. Set this bit to 1 when the input mode for image capture is interlace for capture of only a one-field image. 0: Capture of frame image (1 VD) or both-field image (2 VD) 1: Capture of one-field image (1 VD)

Bit	Bit Name	Initial Value	R/W	Description
3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	CKPOL0	0	R/W	Main Camera Clock Edge Select 0: Input signals (VIO_D0 to D15, VIO_VD, VIO_HD, VIO_FLD) are captured using the rising edge of the sub camera clock (VIO_CLK). 1: Input signals (VIO_D0 to D15, VIO_VD, VIO_HD, VIO_FLD) are captured using the falling edge of the sub camera clock (VIO_CLK).
1, 0	FCI[1:0]	00	R/W	These bits set the timing to start capturing. The timing to start capturing is set by specifying the image to be captured first. Set these bits to 00 when the input mode is progressive. 00: Capture starts from the VD input immediately after the CEU activation regardless of it being a top or bottom field. 01: After the CEU activation, input of a top-field image is waited, and then capture starts from the top field. 10: After the CEU activation, input of a bottom-field image is waited, and then capture starts from the bottom field. 11: Setting prohibited

Table 34.7 CAIFR Setting Items

Input Mode	IFS Bit	Captured Image	CIM Bit	Image to Start Capture	FCI Bits
Progressive	B'0	Frame	B'0	Frame immediately after activation	B'00
Interlace	B'1	Both-field (2-VD capture)	B'0	Field immediately after activation	B'00
				Top field	B'01
				Bottom field	B'10
				Setting prohibited	B'11
		One-field (1-VD capture)	B'1	Field immediately after activation	B'00
				Top field	B'01
				Bottom field	B'10
				Setting prohibited	B'11

In frame image capture and one-field image capture, a one-frame capture end interrupt occurs when capture for 1 VD finishes. In both-field image capture, a one-field capture end interrupt occurs when capture for 1 VD finishes and a one-frame capture end interrupt occurs when capture for 2 VD finishes. At this time, a one-field capture end interrupt occurs simultaneously with a one-frame capture end interrupt. Figure 34.23 shows the timing of a one-frame capture end interrupt and one-field capture end interrupt in both-field image capture.

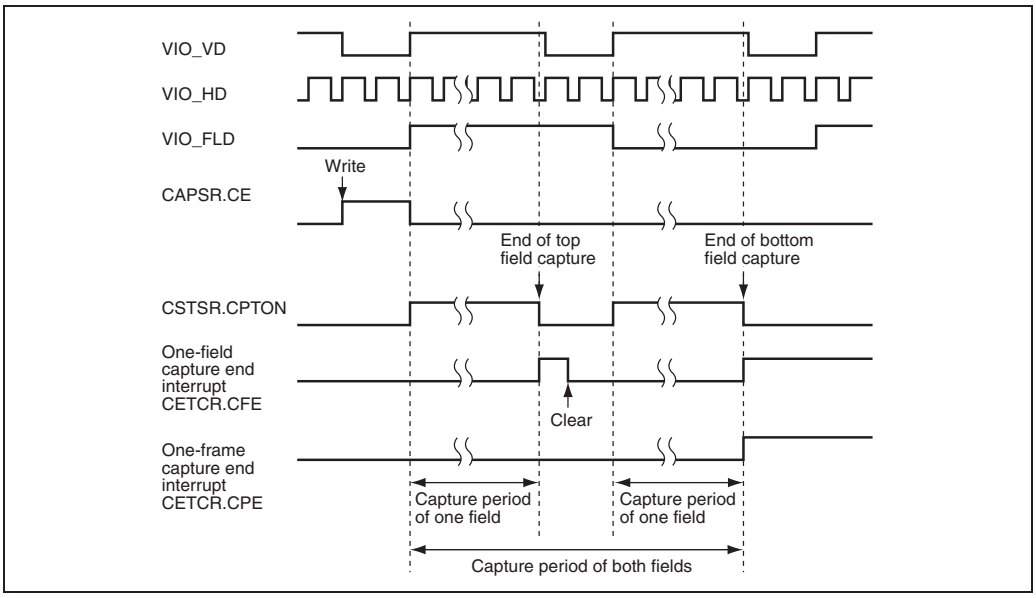


Figure 34.23 One-Frame Capture End Interrupt and One-Field Capture End Interrupt in Both-Field Image Capture

A captured frame image or captured one-field image is stored in the memory from the addresses set in CDAYR and CDACR (figure 34.24). Captured both-field images are stored in different memory areas depending on whether it is a top-field or bottom-field image. A top-field image is stored in the memory from the addresses set in CDAYR and CDACR whereas a bottom-field image is stored in the memory from the addresses set in CDBYR and CDBCR (figure 34.25).

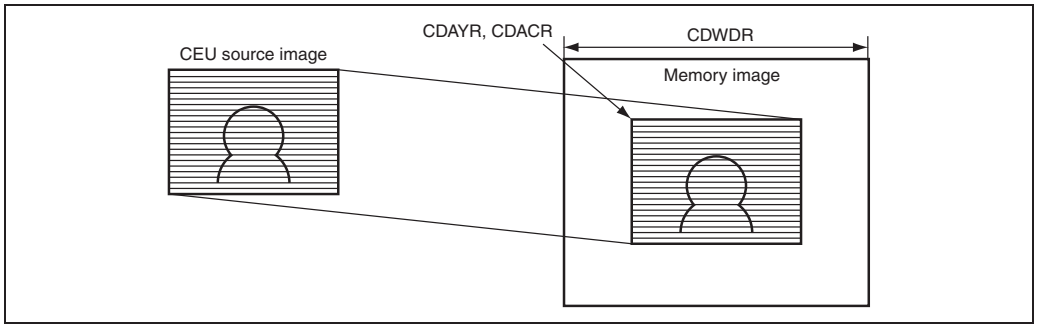


Figure 34.24 Image of Storing Captured Frame Image or Captured One-Field Image in Memory

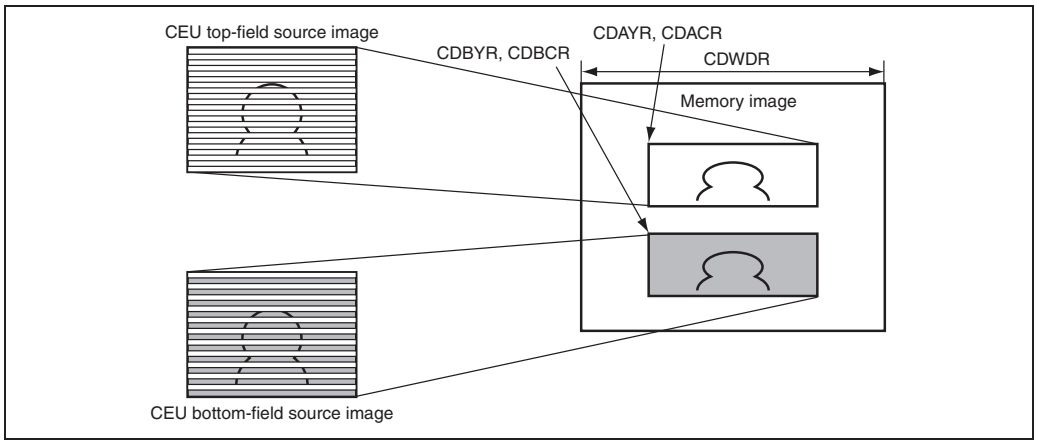


Figure 34.25 Image of Storing Captured Both-Field Images in Memory

If the FCI bits are set to B'00 for continuous capture in interlace input mode, images are continuously captured for 2 VD with the first captured field as the reference in both-field image capture (figure 34.26). In one-field image capture, only the first captured field is continuously captured for 1 VD (figure 34.27).

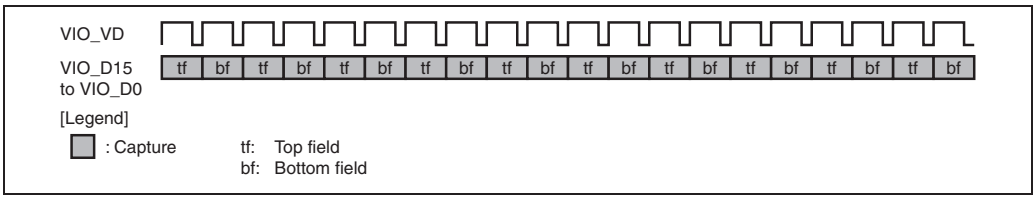


Figure 34.26 Continuous Both-Field Capture in Interlace Mode (Image Immediately after Activation is Top Field (FCI Bits = B'00))

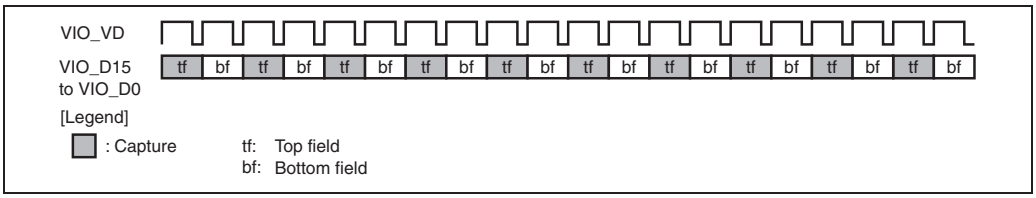


Figure 34.27 Continuous One-Field Capture in Interlace Mode (Image Immediately after Activation is Top Field (FCI Bits = B'00))

(1) Storage of Interlace Input as Frame Image

The CEU can store an interlace source image in the memory as a frame image. To store an interlace source image as a frame image, make the following register settings:

Input mode: Interlace (IFS bit = B'1)

Capture image: Both-field (CIM bit = B'0)

Image to start capture: Any setting other than the prohibited setting (FCI bits = as desired)

Figure 34.28 shows a memory image of capturing both fields of an interlace input and storing it as a frame image in the memory. Set the start addresses of the memory destination for the captured top-field image in CDAYR and CDACR, and the start addresses of the memory destination for the captured bottom-field image in CDBYR and CDBCR. When storing an interlace image as a frame image in the memory, set the horizontal image size of the memory area in CDWDR with the top-field image and bottom-field image placed next to each other as shown in figure 34.28. In addition, set the number of captured lines of the field image in the VWDTH bits in CAPWR.

A memory image of folding the horizontal image size of the memory area in figure 34.28 at CDWDR/2 is shown in figure 34.29. Setting the registers to form the image in figure 34.28 enables an interlace image to be stored as a frame image in the memory as shown in figure 34.29.

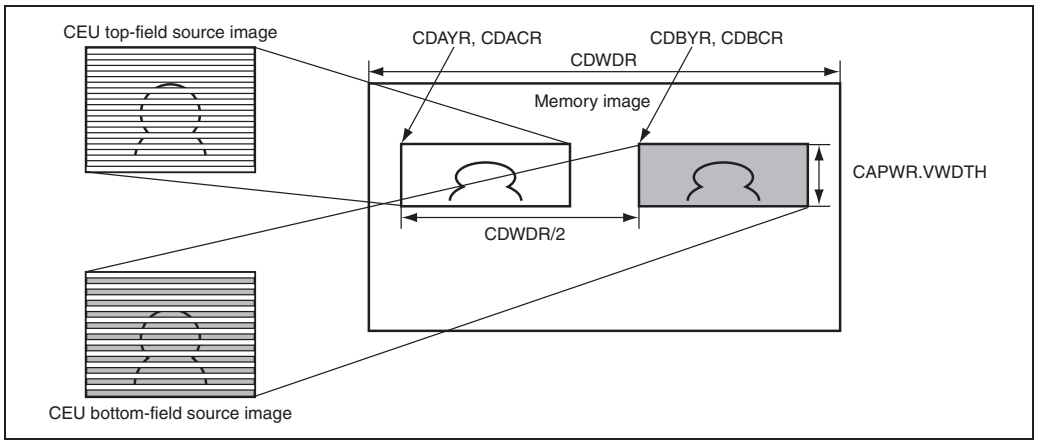


Figure 34.28 Image of Storing Captured Both-Fields of Interlace Input in Memory

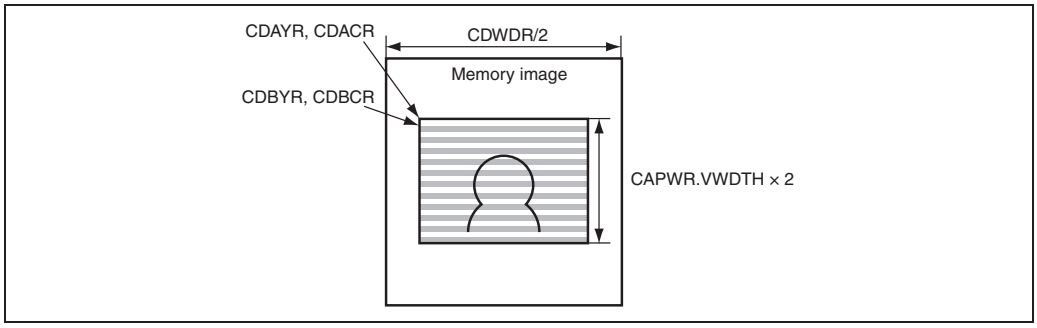


Figure 34.29 Image of Storing Interlace Input as Frame Image in Memory

34.3.8 Camera Strobe Control Register (CSTCR)

Note: CSTCR is not supported in this LSI. Do not attempt to modify this regiser.

CSTCR controls the strobe emission signal. CSTCR is not used in data fetch mode.

Except for the bit used in manual mode, CSTCR should not be modified during strobe emission or in the emission reserved state (STE bit = B'1). If CSTCR is modified during strobe emission or in the emission reserved state, correct operation cannot be guaranteed. Only the SEWR bit is used in manual mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	SVPOL	SHPOL	—	—	—	SEPOL	—	—	—	SEWR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R	RW	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	SMOD[1:0]		—	—	SXPD	SERD	—	—	—	STE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25	SVPOL	0	R/W	Sets the polarity of the strobe sync signal in automatic mode. The polarity of the strobe sync signal can be set independently of the capture interface settings (VDPOL and HDPOL bits in CAMCR). The strobe control unit has an internal counter used to assert an emission signal at the emission timing set in CSECR. This bit sets the edge polarity of VD at which the internal counter is started. 0: Count starts at the rising edge of the vertical sync signal. 1: Count starts at the falling edge of the vertical sync signal.

Bit	Bit Name	Initial Value	R/W	Description
24	SHPOL	0	R/W	Sets the polarity of the strobe sync signal in automatic mode 1 or 2. The polarity of the strobe sync signal can be set independently of the capture interface settings (VDPOL and HDPOL bits in CAMCR). The strobe control unit has an internal counter used to assert or negate an emission signal at the emission timing set in CSECR. This bit sets the edge polarity of HD at which the internal counter is incremented. 0: Count is incremented at the rising edge of the horizontal sync signal. 1: Count is incremented at the falling edge of the horizontal sync signal.
23 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	SEPOL	0	R/W	Sets the polarity of the strobe sync signal in automatic mode 3. The setting of this bit is valid only in automatic mode 3 (SMOD bits = 11). The polarity of the strobe sync signal can be set independently of the capture interface settings (VDPOL and HDPOL bits in CAMCR) and SVPOL bit setting. The strobe control unit has an internal counter used to negate an emission signal at the emission timing set in CSECR. This bit sets the edge polarity of VD at which the internal counter is incremented. 0: Count is incremented at the rising edge of the vertical sync signal. 1: Count is incremented at the falling edge of the vertical sync signal.
19 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
16	SEWR	0	R/W	Sets the emission pin status in manual mode. The setting of this bit is valid only in manual mode (SMOD bits = 10). The emission pin immediately reflects this bit setting regardless of other bit settings. 0: Forcibly drives the strobe emission signal low. 1: Forcibly drives the strobe emission signal high.
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9, 8	SMOD[1:0]	00	R/W	These bits set the strobe operating mode. Automatic mode or manual mode can be selected for the strobe function. These bits must not be modified during strobe operation. If modified, correct operation cannot be guaranteed. 00: Strobe operates in automatic mode 1. 01: Strobe operates in automatic mode 2. 10: Strobe operates in manual mode. 11: Strobe operates in automatic mode 3.
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	SXRD	0	R	Indicates the pin state of the strobe exposed signal which is sampled at the system clock. 0: No strobe exposed signal is input. 1: Strobe exposed signal is input. Note: The strobe exposed signal is high-active.

Bit	Bit Name	Initial Value	R/W	Description
4	SERD	0	R	Indicates the pin state of the strobe emission signal which is sampled at the system clock. 0: No strobe emission signal is output. 1: Strobe emission state Note: The strobe emission signal is high-active.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	STE	0	R/W	Enables or disables strobe emission at the next vertical sync signal in automatic mode. If this bit is set to 1 when the vertical sync signal is input, the emission signal is asserted when the internal counter reaches the value set in the STCT bits in CSECR. This bit is automatically cleared to 0 by a vertical sync signal input. To emit the strobe at the next vertical sync signal input, set this bit to 1 again before the next vertical sync signal input. The polarity of the vertical sync signal is determined by the SVPOL bit setting. 0: Does not emit the strobe. 1: Emits the strobe. Note: When manual mode is selected, this bit must be cleared to 0. Do not write 1 to this bit when the emission signal is being asserted in automatic mode 2.

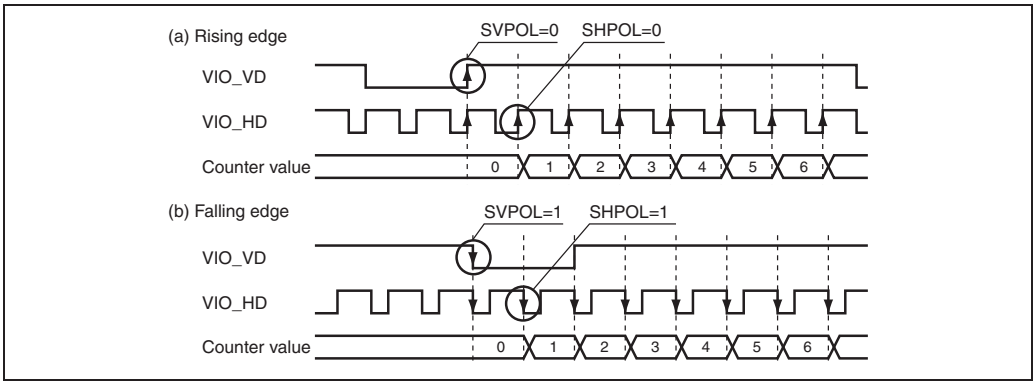


Figure 34.30 Internal Counter Timing Determined by SVPOL and SHPOL Bits

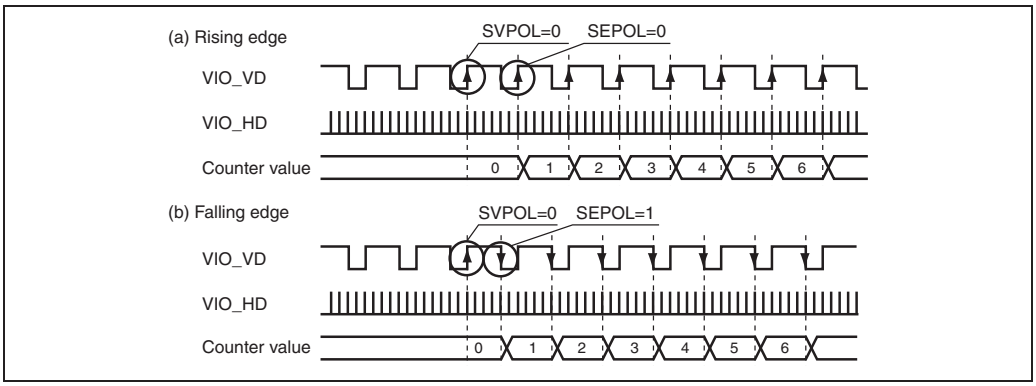


Figure 34.31 Internal Counter Timing Determined by SVPOL and SEPOL Bits

The strobe function has automatic and manual modes. Each mode has the following operations.

(1) Automatic Mode 1 (SMOD Bits = B'00)

- Emission can be enabled or disabled by setting the STE bit.
- The emission signal is asserted at the HD count set by the STCT bits in CSECR.
- The emission signal can be negated only by the exposed signal (writing to the SEWR bit is ignored).

In automatic mode 1, the HD input is counted from the VD edge, and the emission signal is asserted when counting reaches the value set in the STCT bits. The emission signal remains high until the exposed signal is input and is not negated even when the next VD is input. Use manual mode to forcibly negate the emission signal.

Note: For the exposed signal input, drive it high for two or more camera clock cycles.

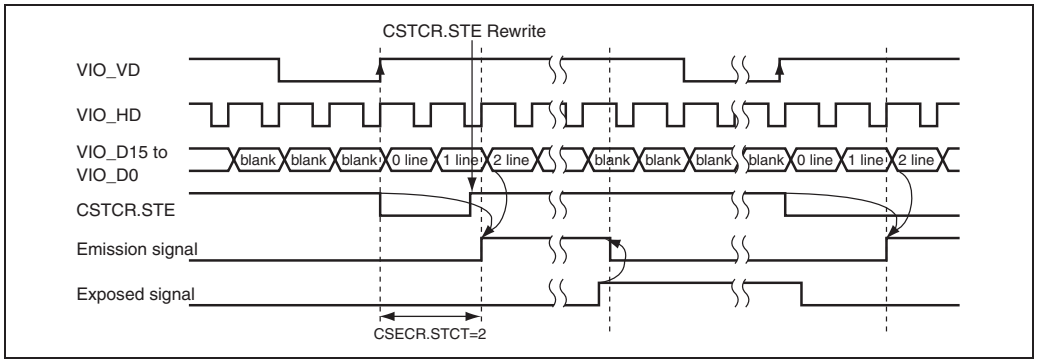


Figure 34.32 Operation Timing of Automatic Mode 1

(2) Automatic Mode 2 (SMOD Bits = B'01)

- Emission can be enabled or disabled by setting the STE bit.
- The emission signal is asserted at the HD count set by the STCT bits in CSECR.
- The emission signal is negated when HD is counted up to the value set by the SEL bits in CSECR.
- The emission signal is not negated even if the exposed signal is asserted.

Operation in automatic mode 2 is similar to that in automatic mode 1 up to the point where the emission signal is asserted. The condition for negating the emission signal is different. The emission signal is negated by input of the exposed signal in automatic mode 1, whereas in automatic mode 2, the emission signal is negated when HD is input for the number of times set in CSECR after the emission signal has been asserted. If the HD count set by the SEL bits is longer than the period until the next VD input, the emission signal is not negated at the next VD input. Strobe control using the exposed signal is not done in automatic mode 2.

In automatic mode 2, the condition for negating the emission signal differs from that in automatic mode 1. The HD inputs are counted, and when the HD count reaches the value set by the SEL bits, the emission signal is negated.

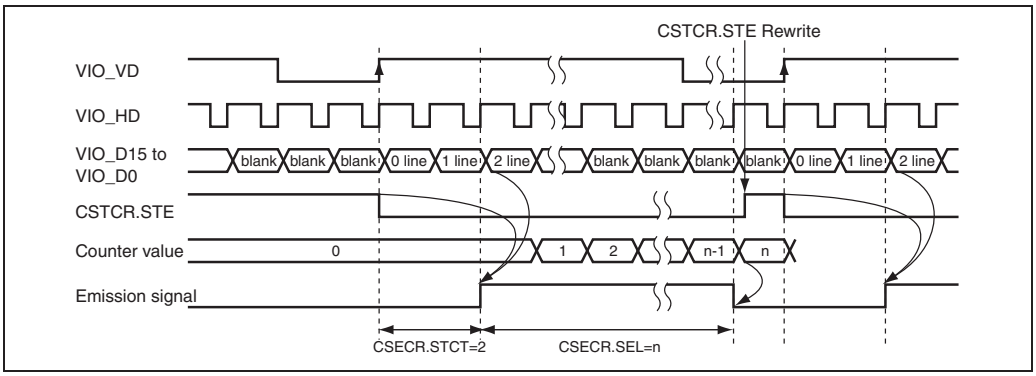


Figure 34.33 Operation Timing of Automatic Mode 2

(3) Manual Mode (SMOD Bits = B'10)

- The emission pin can only be controlled by writing to the SEWR bit.
- The emission timing control counter does not operate. (The STE bit, and the STCT bits in CSECR are ignored.)
- The emission signal is not negated even when the exposed signal is asserted.

In manual mode, the state of the emission pin can be controlled directly by writing to the SEWR bit. In manual mode, the state of the exposed signal can be controlled only by the SEWR bit, and the VD and exposed signals are not referred to.

After the SEWR bit has been written to, it takes several to several tens of system clock cycles for the state of the emission pin to actually change. This delay time depends on the ratio of the camera clock frequency to the system clock frequency. The delay becomes greater as the camera clock becomes slower than the system clock.

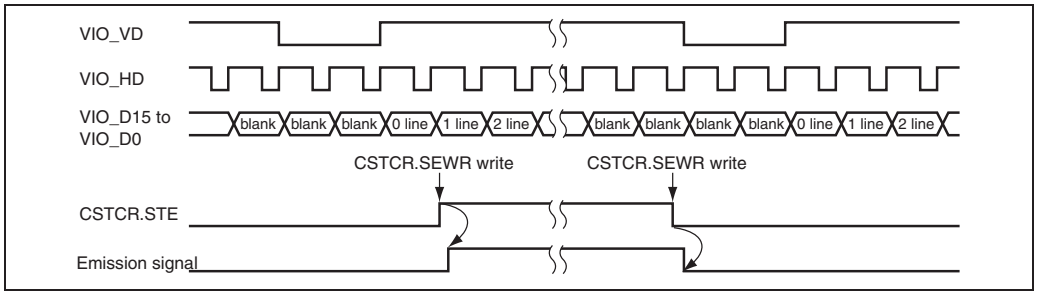


Figure 34.34 Operation Timing of Manual Mode

(4) Automatic Mode 3 (SMOD Bits = B'11)

- Emission can be enabled or disabled by setting the STE bit.
- The emission signal is asserted at the VD input.
- The emission signal is negated when VD is counted up to the value set by the SEL bits in CSECR.
- The emission signal is not negated even if the exposed signal is asserted.

In automatic mode 3, the emission signal is asserted at the VD edge. The emission signal is negated when VD is input for the number of times set in the SEL bits in CSECR after the emission signal has been asserted.

Strobe control using the exposed signal is not done in automatic mode 3.

In automatic mode 3, unlike automatic mode 1 and automatic mode 2 which are synchronized with HD, the emission signal is controlled in synchronization with VD.

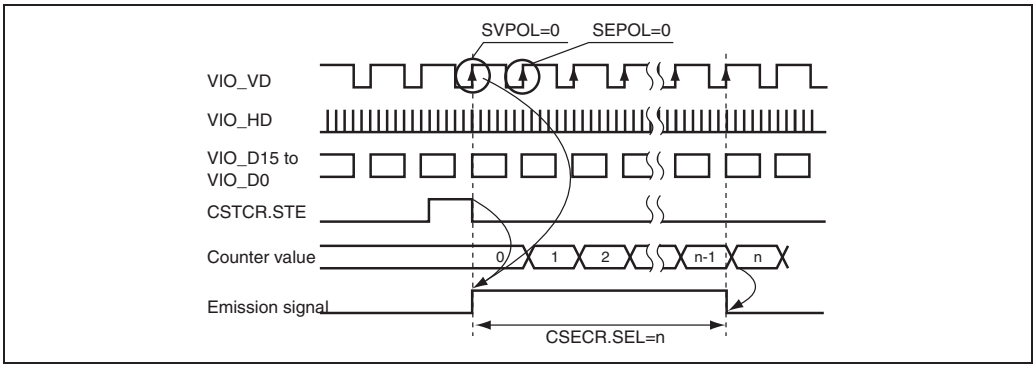


Figure 34.35 Operation Timing of Automatic Mode 3

34.3.9 Camera Strobe Emission Count Register (CSECR)

Note: CSECR is not supported in this LSI. Do not attempt to modify this regiser.

CSECR sets the wait time until the strobe emission signal is asserted, and how long the emission signal is asserted.

The setting of CSECR is not referred to in manual mode. CSECR is also not used in data fetch mode. Do not modify this register during the period that starts when emission is reserved (STE bit in CSTCR is B'1) and ends when the emission signal is negated.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	STCT[13:0]													
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	SEL[13:0]													
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	00	R	Reserved These bits are always read as 0. The write value should always be 0.
29 to 16	STCT[13:0]	H'0000	R/W	These bits set the timing until the emission signal is output (counts the number of rising or falling edges of HD). Counting the number of HD inputs starts when capturing begins, and the emission signal is driven high when HD has been input for the number set by these bits.
15, 14	—	00	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
13 to 0	SEL[13:0]	H'0000	R/W	Assert Period of Strobe Emission Signal • Automatic mode 2 (HD units) When automatic mode 2 is selected, set the assert period of the strobe emission signal with the number of HD inputs. Do not clear these bits to 0 when automatic mode 2 is selected. • Automatic mode 3 (VD units) When automatic mode 3 is selected, set the assert period of the strobe emission signal with the number of VD inputs. Do not clear these bits to 0 when automatic mode 3 is selected.

34.3.10 CEU Register Control Register (CRCNTR)

CRCNTR controls switching of the planes of registers with a 2-plane configuration.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	RVS	—	—	RS	RC
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	RVS	0	R/W	Sets the timing to switch the register plane in both-field capture. The setting of this bit is valid only when the RC bit is 1 in both-field capture. 0: Switches the register plane every two VDs. 1: Switches the register plane every VD.

Bit	Bit Name	Initial Value	R/W	Description
3, 2	—	00	R	Reserved These bits are always read as 0. The write value should always be 0.
1	RS	0	R/W	Specifies which register plane is used by the CEU in synchronization with VD. The setting of this bit is valid only when the RC bit is 0. 0: Uses plane A of the register. 1: Uses plane B of the register.
0	RC	0	R/W	Specifies switching of the register plane used by the CEU in synchronization with VD. If the register plane is not switched, the register plane specified by the RS bit is used. 0: Uses the specified register plane in synchronization with VD. 1: Switches the register plane in synchronization with VD.

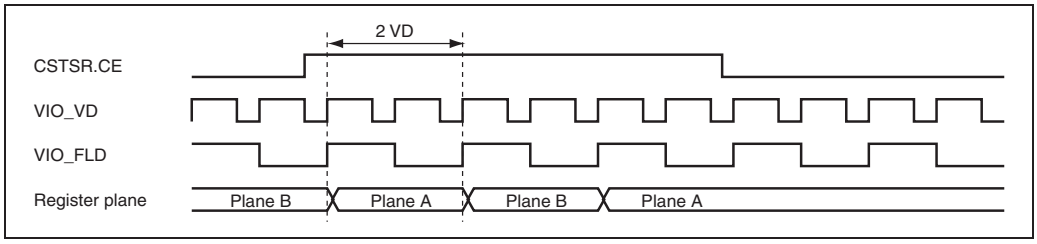


Figure 34.36 Timing for Register Plane Switching when RVS Bit is B'0

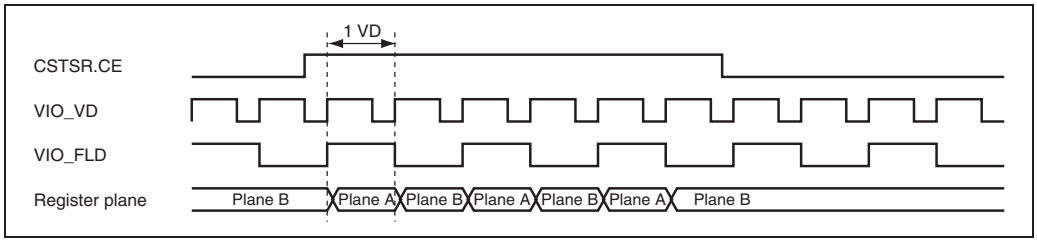


Figure 34.37 Timing for Register Plane Switching when RVS Bit is B'1

34.3.11 CEU Register Forcible Control Register (CRCMPR)

CRCMPR forcibly controls switching of the planes of registers with a 2-plane configuration. Setting this register enables direct control of register plane switching.

Do not modify this register during operation. If this register is modified during operation, correct operation cannot be guaranteed. In addition, the IGRW bit (interrupt source) in CETCR is set to B'1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RA
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	RA	0	R/W	Indicates the register plane currently specified. This register value automatically changes in synchronization with VD for starting capture. To start capture with plane A of the register when a setting to switch the register plane in synchronization with VD has been made (RC bit in CRCNTR is 1), specify plane B of the register using this bit. 0: Specifies plane A of the register. 1: Specifies plane B of the register.

34.3.12 Capture Filter Control Register (CFLCR)

CFLCR sets the scale-down factor for the filter to scale images down.

The CEU has an image scale-down filter which can be used to scale down the captured images before storing them in the memory. Set CFLCR to 0 when not performing scale-down (same size output). If a value other than 0 is set in CFLCR, scale-down is performed. In data fetch mode, set CFLCR to 0.

When handling an interlace source image as a frame image, set CFLCR to 0 to not use the filter.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VMANT[3:0]				VFRAC[11:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HMANT[3:0]				HFRAC[11:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	VMANT[3:0]	H'0	R/W	Mantissa Part of Vertical Scale-Down Factor The specifiable range is H'0 to H'F. When H'0 is set for the VMANT bits and H'000 is set for the VFRAC bits, the scale-down filter is not used.
27 to 16	VFRAC[1:0]	H'000	R/W	Fraction Part of Vertical Scale-Down Factor The specifiable range is H'000 to H'FFF. The fraction of the scale-down factor that cannot be set with only the VMANT bits must be set with these bits.
15 to 12	HMANT[3:0]	H'0	R/W	Mantissa Part of Horizontal Scale-Down Factor The specifiable range is H'0 to H'F. When H'0 is set for the HMANT bits and H'000 is set for the HFRAC bits, the scale-down filter is not used.
11 to 0	HFRAC[11:0]	H'000	R/W	Fraction Part of Horizontal Scale-Down Factor The specifiable range is H'000 to H'FFF. The fraction of the scale-down factor that cannot be set with only the HMANT bits must be specified with these bits.

An image scale-down filter is installed in the CEU, and the captured images can be scaled down and stored in the memory.

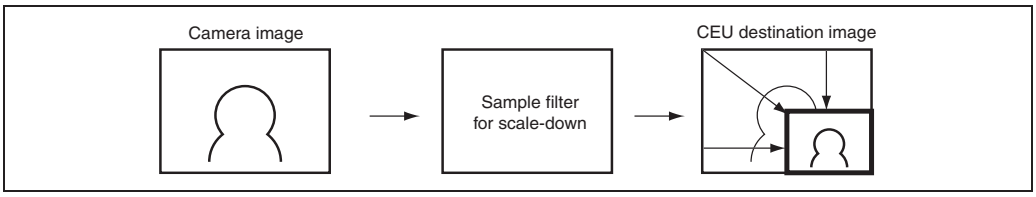


Figure 34.38 Scale-Down of Captured Image

The formulas for obtaining the MANT (VMANT or HMANT) and FRAC (VFRAC or HFRAC) values from the input pixel count and output pixel count of the filter are shown below. Set the MANT and FRAC bits in order to obtain the desired output pixel count from the number of pixels input to the CEU.

First, calculate preliminary MANT and FRAC values. The parameters needed for calculation are defined as follows:

$$\alpha = MANT \times 4096 + FRAC \quad \text{. . . Formula 1}$$

$$SCL \text{ (scaling factor)} = \frac{4096}{\alpha} \quad \text{. . . Formula 2}$$

Assuming an operator $\lfloor x \rfloor$ which discards fractions of an integer x, output size ($SIZE_D$) of the scaled-down filter can be calculated with formula3.

$$SIZE_D = \left\lfloor \frac{SIZE_P}{1 + (SIZE_P \times MANT_{pre} - 1)} \right\rfloor \quad \cdots \text{ Formula 3}$$

$MANT_{pre} = 1 \leftarrow (0 \leqq MANT < 2)$
$MANT_{pre} = 2 \leftarrow (2 \leqq MANT < 4)$
$MANT_{pre} = 4 \leftarrow (4 \leqq MANT < 8)$
$MANT_{pre} = 8 \leftarrow (8 \leqq MANT)$

$SIZE_P$ is calculated by formula 4, 5, and 6. The formula used is different by Horizontal direction, Vertical direction and SCL value. S_{in} is a size of the input image.

case1 : SCL > 1/2

$$SIZE_P = S_{in} \quad \cdots \text{ Formula 4}$$

case2: SCL ≦ 1/2, Horizontal direction

$$SIZE_P = 2 \times \left\lfloor \frac{Sin}{MANT_{pre}} \times \frac{1}{2} \right\rfloor \quad \cdots \text{ Formula 5}$$

case3: SCL ≦ 1/2, Vertical direction

$$SIZE_P = \left\lfloor \frac{Sin}{MANT_{pre}} \right\rfloor \quad \cdots \text{ Formula 6}$$

The number of output pixels can be obtained by substituting the temporarily calculated MANT, FRAC, and input image size into these formulas. If the calculated number of output pixels is smaller than the number of output pixels used to obtain the preliminary MANT and FRAC values, recalculate with a smaller FRAC (α) value, and set the MANT and FRAC values in this register so that a pixel value greater than the desired number of output pixels can be obtained.

Table 34.8 Setting Examples for Each Scale-Down Filter Factor

Scale-Down Factor	FRAC		MANT	Input Pixel Count	Output Pixel Count	Clipping Size (CFSZR)
	Decimal	Hexadecimal				
7/8	576	H'240	1	640	560	560
3/4	1352	H'548	1	640	480	480
5/8	2448	H'990	1	640	400	400
1/2	0	H'0	2	640	320	320
3/8	2728	H'AA8	2	640	240	240
1/3	0.0	H'0	3	640	213	212
1/4	0.0	H'0	4	640	160	160
1/5	0.0	H'0	5	640	128	128
1/6	0.0	H'0	6	640	107	104
1/7	0.0	H'0	7	640	91	88
1/8	0.0	H'0	8	640	80	80
1/16	4088	H'FF8	15	640	40	40

Note: When an image is scaled down, set the scaled-down image size to at least 48 pixels by 48 lines, and to no more than 2048 pixels wide. When an image is not scaled down (same size output), this restriction does not apply.

Attention: The Scale-Down filter of CEU is two step composition. In pre-filter in the former steps, a right and bottom edge of the image might be lacked. The lacking pixel count can be calculated by the following expression.

$$\text{Lack-pixels} = Sin - SIZE_P \times MANT_{pre}$$

34.3.13 Capture Filter Size Clip Register (CFSZR)

CFSZR sets the clipping size for fine adjustment of the image size output from the filter, and must be set in combination with CFLCR. When clipping the output size of the filter, set the clipping size as a number of pixels, and the setting unit should be four pixels. CFSZR must be set even when scale-down is not performed (same size output).

In data fetch mode, set CFSZR according to the setting of CAPWR.

This register cannot be used in data enable fetch mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	VFCLP[11:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	HFCLP[11:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
27 to 18	VFCLP[11:2]	H'000	R/W	These bits set the vertical clipping value of the filter output size (4-pixel units).
17, 16	VFCLP[1:0]		R	
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 1	HFCLP[11:1]	H'000	R/W	These bits specify the horizontal clipping value of the filter output size (4-pixel units).
0	HFCLP[0]		R	

The scale-down filter in the CEU may output an odd number of pixels or lines depending on the settings. To adjust the output size of the filter, the CEU clips the destination image by using the number of pixels specified in CFSZR, as shown in figure 34.39. The clipping size must be specified vertically and horizontally in 4-pixel units.

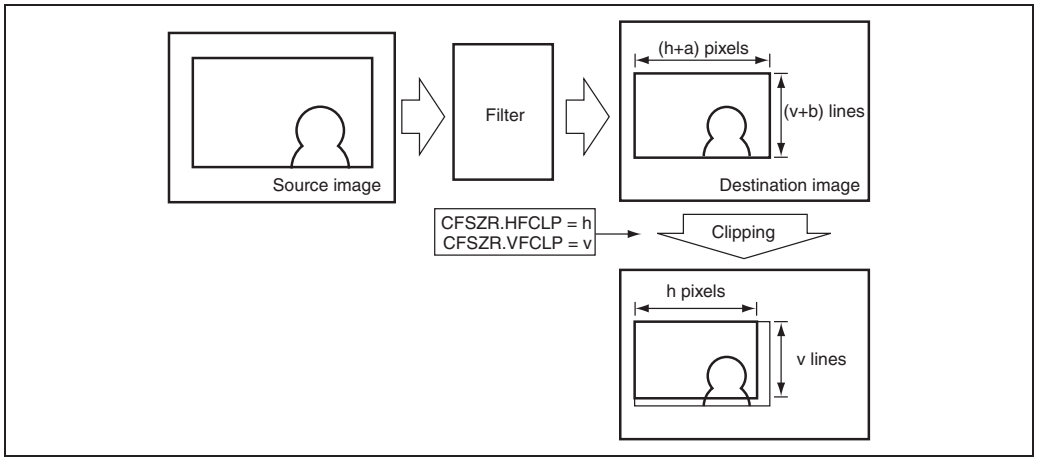


Figure 34.39 Clipping of Image Output from Filter

The pixels to be clipped are counted from the top-left corner of a display. The pixels located to the right of the specified number of pixels or below the specified number of lines are discarded by the clipping function. If the number of pixels specified in CFSZR is larger than that output from the filter, correct operation cannot be guaranteed. To avoid this, the clipping size specified in CFSZR must be equal to or smaller than the number of pixels output from the filter.

Note: In data fetch mode, the following settings are required. Data cannot be fetched correctly unless the following settings are made.
VFCLP = CAPWR.VWDTH
8-bit interface: HFCLP = CAPWR.HWDTH/2
16-bit interface: HFCLP = CAPWR.HWDTH

34.3.14 Capture Destination Width Register (CDWDR)

CDWDR sets the horizontal image size in the memory area where the captured image is to be output in 4-byte units (4-pixel units).

In data fetch mode, set CDWDR according to the setting of CAPWR.

This register cannot be used in data enable fetch mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CHDW[12:0]												
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 2	CHDW[12:2]	H'0000	R/W	These bits specify the horizontal image size in the memory area where the captured image is to be stored (4-byte units). The image data captured by the CEU is stored in the memory. If the right end of the captured image does not match the horizontal image size in the memory area as shown in figure 34.40, some addresses must be skipped at the right end of the image when storing the captured image. Therefore, the horizontal image size in the memory area where the captured image is to be stored must be set in these bits. The maximum value to be set is 8188 bytes (8188 pixels). In data fetch mode, set as follows: 8-bit interface: CHDW = CAPWR.HWDTH 16-bit interface: CHDW = CAPWR.HWDTH × 2
1, 0	CHDW[1:0]		R	

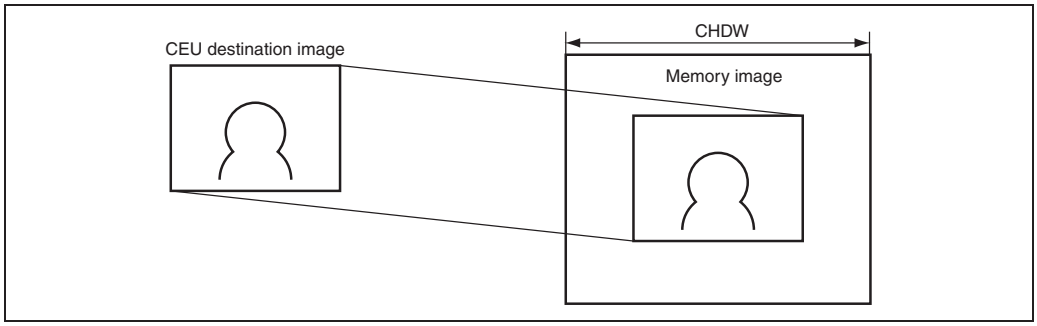


Figure 34.40 Captured Image and Memory Area Image

34.3.15 Capture Data Address Y Register (CDAYR)

CDAYR specifies the address where the luminance (Y) component of the captured data is to be stored in frame image capture or one-field image capture, the address where the luminance (Y) component of the captured top field is to be stored in both-field image capture, and the address where the fetched data is to be stored in data fetch. The CEU separates the captured image data into the luminance component data (Y) and the chrominance component data (C), and stores them in the memory via the bus. In frame image capture or one-field image capture, set the start address of the memory area where the Y (luminance) component of the captured data is to be stored by CDAYR. In both-field image capture, set the start address of the memory area where the Y (luminance) component of the captured top-field image is to be stored by CDAYR. In data fetch, set the start address of the memory area where data is to be stored by CDAYR.

Because the address must be specified in 32 bits, the address set by CDAYR must be in longword units. As the setting is in 4-pixel units for image capture and 4-byte units for data fetch, the lower two bits are always fixed to 0.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CAYR[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CAYR[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 2 1, 0	CAYR[31:2] CAYR[1:0]	H'0000 0000	R/W R	• Frame image capture: These bits set the address for storing the Y (luminance) component data of the captured data (4-pixel units). • One-field image capture: These bits set the address for storing the Y (luminance) component data of the captured data (4-pixel units). • Both-field image capture: These bits set the address for storing the Y (luminance) component data of the captured top-field data (4-pixel units). • Data fetch: These bits set the address for storing data (4-byte units). • Data enable fetch in a bundle write: Set the address of the starting point of the starting point of the memory area where the captured data is to be stored in 32-byte units.

Set the address of the starting point of the memory area where the fetched data is to be stored in this register, as shown in figure 34.41.

- Frame image capture: Set the address of the starting point of the memory area where the Y component of the captured image is to be stored.
- One-field image capture: Set the address of the starting point of the memory area where the Y component of the captured image is to be stored.
- Both-field image capture: Set the address of the starting point of the memory area where the Y component of the captured top-field image is to be stored.
- Data fetch: Set the address of the starting point of the memory area where the fetched data is to be stored. In data fetch mode, the data is simply stuffed in order from the start address so the end address becomes as follows:

  End address = CDAYR + number of fetched bytes - 1
- Data enable fetch in a bundle write: Set the address of the starting point of the starting point of the memory area where the captured data is to be stored in 32-byte units.

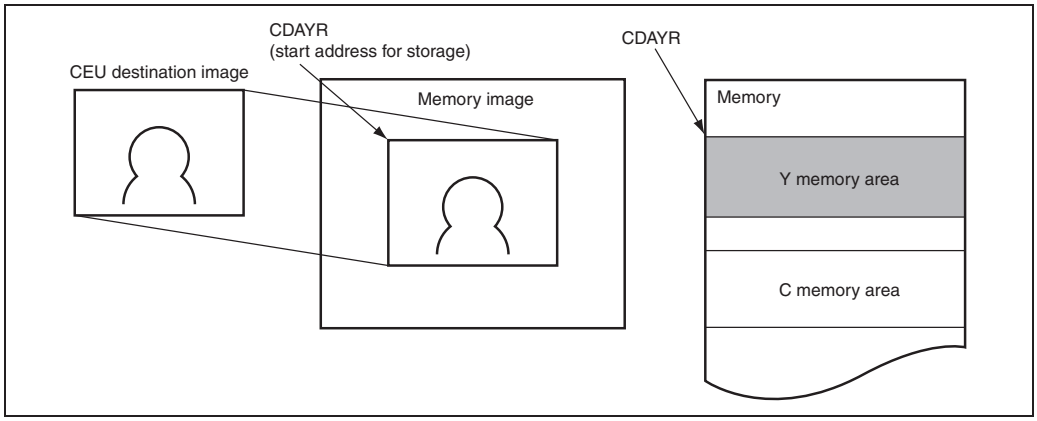


Figure 34.41 Relationship between Captured Image and Y Component Memory Area

34.3.16 Capture Data Address C Register (CDACR)

CDACR specifies the address where the chrominance (C) component of the captured data is to be stored in frame image capture or one-field image capture, and the address where the chrominance (C) component of the captured top field is to be stored in both-field image capture. The CEU separates the captured image data into the luminance component data (Y) and the chrominance component data (C), and stores them in the memory via the bus. In frame image capture or one-field image capture, set the start address of the memory area where the C (chrominance) component of the captured data is to be stored by CDACR. In both-field image capture, set the start address of the memory area where the C (chrominance) component of the captured top-field image is to be stored by CDACR. CDACR is not used in data fetch.

Because the address must be specified in 32 bits, the address set by CDACR must be in longword units. As the setting is in 4-pixel units, the lower two bits are always fixed to 0.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CACR[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CACR[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 2 1, 0	CACR[31:2] CACR[1:0]	H'0000 0000	R/W R	• Frame image capture: These bits set the address for storing the C (chrominance) component data of the captured data (4-pixel units). • One-field image capture: These bits set the address for storing the C (chrominance) component data of the captured data (4-pixel units). • Both-field image capture: These bits set the address for storing the C (chrominance) component data of the captured top-field data (4-pixel units).

Set the address of the starting point of the memory area where the C component of the captured image is to be stored in this register, as shown in figure 34.42. The C component has an output data format like that in figure 34.43, and is saved in the memory in this format.

- Frame image capture: Set the address of the starting point of the memory area where the C component of the captured image is to be stored.
- One-field image capture: Set the address of the starting point of the memory area where the C component of the captured image is to be stored.
- Both-field image capture: Set the address of the starting point of the memory area where the C component of the captured top-field image is to be stored.

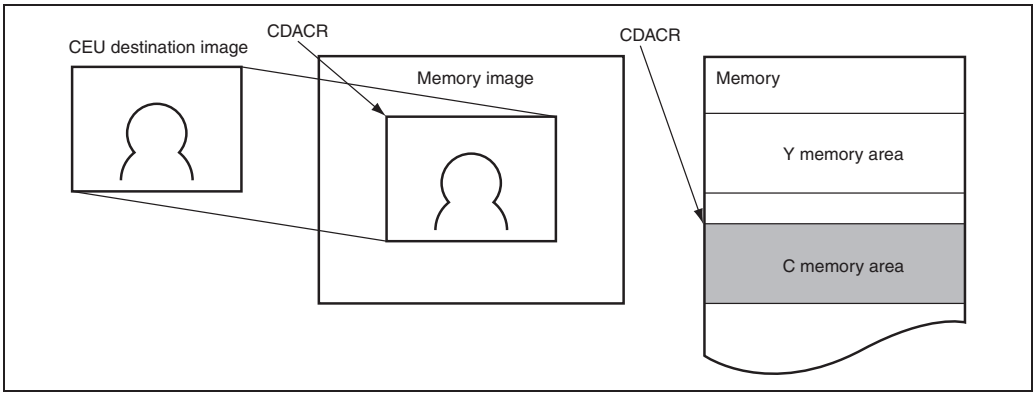


Figure 34.42 Relationship between Captured Image and C Component Memory Area

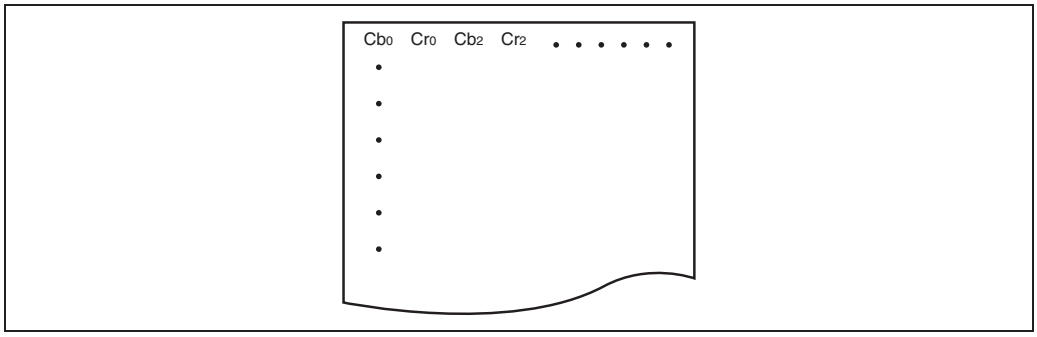


Figure 34.43 Image of Storing C Components in Memory

34.3.17 Capture Data Bottom-Field Address Y Register (CDBYR)

CDBYR specifies the address where the luminance (Y) component of the captured bottom-field data is to be stored in both-field image capture. The CEU separates the captured image data into the luminance component data (Y) and the chrominance component data (C), and stores them in the memory via the bus. Set the start address of the memory area where the Y (luminance) component of the captured bottom-field image is to be stored by CDBYR. CDBYR is not used in frame image capture, one-field image capture, or data fetch.

Because the address must be specified in 32 bits, the address set by CDBYR must be in longword units. As the setting is in 4-pixel units, the lower two bits are always fixed to 0.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CBYR[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CBYR[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	CBYR[31:2]	H'0000 0000	R/W	These bits set the address for storing the Y (luminance) component data of the captured bottom-field data (4-pixel units).
1, 0	CBYR[1:0]		R	

Set the address of the starting point of the memory area where the Y component of the captured bottom-field image is to be stored in this register, as shown in figure 34.44.

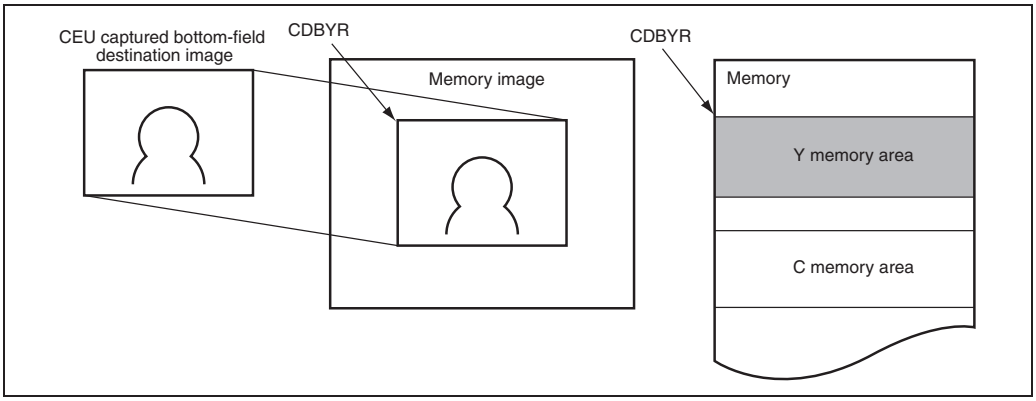


Figure 34.44 Relationship between Captured Bottom-Field Image and Y Component Memory Area

34.3.18 Capture Data Bottom-Field Address C Register (CDBCR)

CDBCR specifies the address where the chrominance (C) component of the captured bottom-field data is to be stored in both-field image capture. The CEU separates the captured image data into the luminance component data (Y) and the chrominance component data (C), and stores them in the memory via the bus. Set the start address of the memory area where the C (chrominance) component of the captured bottom-field image is to be stored by CDBCR. CDBCR is not used in frame image capture, one-field image capture, or data fetch.

Because the address must be specified in 32 bits, the address set by CDBCR must be in longword units. As the setting is in 4-pixel units, the lower two bits are always fixed to 0.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CBCR[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CBCR[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	CBCR[31:2]	H'0000 0000	R/W	These bits set the address for storing the C (chrominance) component data of the captured bottom-field data (4-pixel units).
1, 0	CBCR[1:0]		R	

Set the address of the starting point of the memory area where the C component of the captured bottom-field image is to be stored in this register, as shown in figure 34.45. The C component has an output data format like that in figure 34.46, and is saved in the memory in this format.

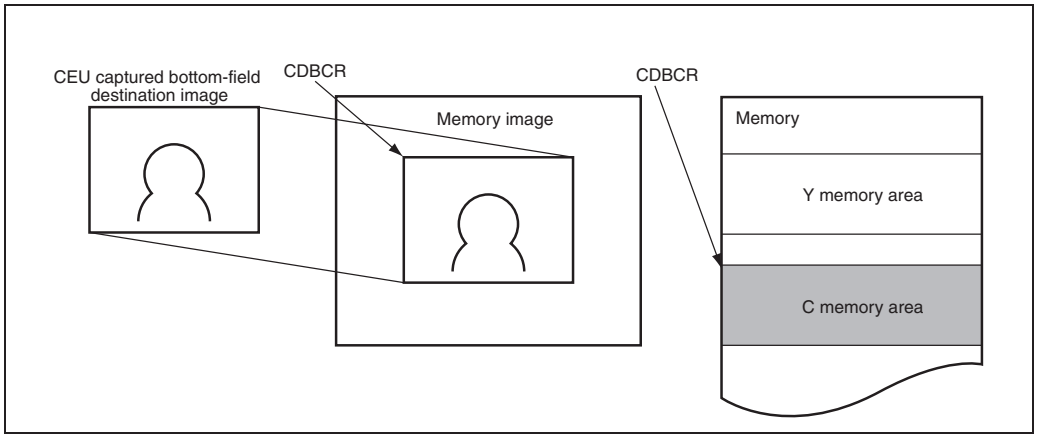


Figure 34.45 Relationship between Captured Bottom-Field Image and C Component Memory Area

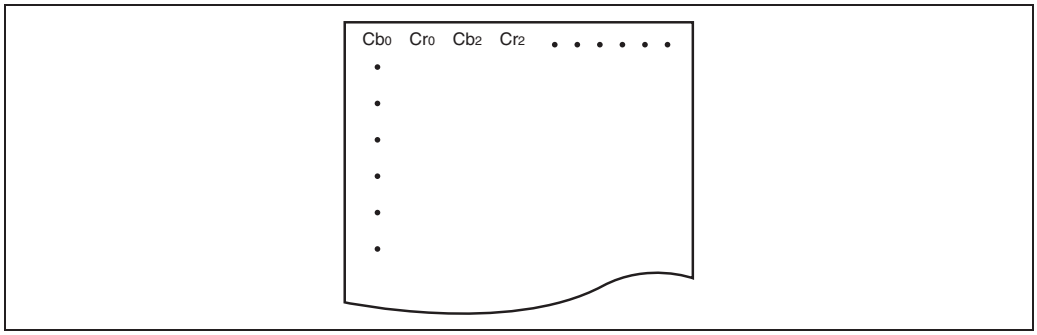


Figure 34.46 Image of Storing C Components in Memory

34.3.19 Capture Bundle Destination Size Register (CBDSR)

CBDSR sets the number of lines output to the memory in a bundle write. CBDSR is not used in data fetch mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	CBVS[11:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 3	CBVS[11:3]	H'000	R/W	These bits set the number of lines output to the memory in a bundle write. Set the number of lines of captured data to be written to the memory by a bundle write as a multiple of eight. This register is valid only when the CBE bit in CDOCR is 1. When the CBE bit is 1 and this register cleared to 0, the CEU operates with the number of lines of captured data to be written to the memory as eight.
2 to 0	CBVS[2:0]		R	

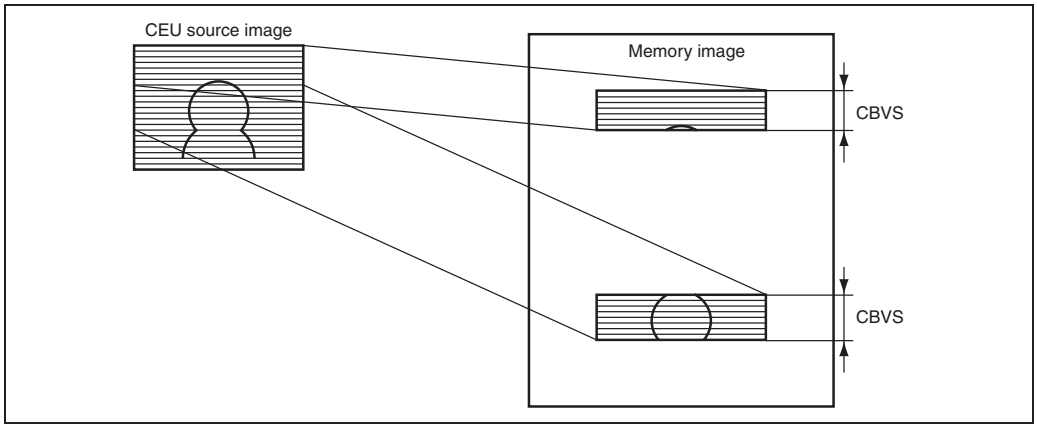


Figure 34.47 Image of Storing Captured Image in Memory by Bundle Write

34.3.20 Capture Low-Pass Filter Control Register (CLFCR)

CLFCR specifies whether or not to operate the low-pass filter. In data fetch mode, clear the LPF bit to B'0.

The characteristic of the low-pass filter installed in the CEU causes the phase location of the image processed by the low-pass filter to be shifted right by one pixel compared to the raw image.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	LPF
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
0	LPF	0	R/W	Enables or disables operation of the low-pass filter. The low-pass filter removes high-frequency components from the destination image in the horizontal direction. Clear this bit to 0 in data fetch mode. 0: Low-pass filter not used 1: Low-pass filter used (only in the horizontal direction)

34.3.21 Firewall Operation Control Register (CFWCR)

CFWCR specifies the upper limit of the write addresses in data enable fetch. When the VD input from an external module dose not go low and end notification is not given, this register can prevent writing to memory from being out of control.

This register is enabled only in data enable fetch.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	FWV[26:11]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FWV[10:0]											—	—	—	—	FWE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	FWV[26:0]	H'0000 000	R/W	These bits specify the upper limit of a write address. For example, when 0x0c008000 is set to the upper limit address, it becomes FWV[26:0]=0x0600400.
4 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
0	FWE		R/W	With the setting of FWE = 1, when an address exceeds the value set with FWV, the address is retained and an interrupt source FWF is set. After this, the address is not incremented and data is overwritten on the upper limit address. 0: Firewall is not activated. 1: Firewall is activated.

34.3.22 Capture Data Output Control Register (CDOCR)

CDOCR sets the format for outputting captured data to the memory. In data fetch mode, set the CDS bit to B'1 and the CBE bit to B'0.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CBE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	CFXAD	—	—	—	CDS	—	COLS	COWS	COBS
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
16	CBE	0	R/W	Controls the number of lines of captured data to be written to the memory. • Image capture This bit controls the number of lines of captured data to be written to the memory. When bundle write is set by this register, captured data is written in line units specified by CBDSR to the addresses specified by CDAYR and CDACR, and CDAYR2 and CDACR2 (CDBYR and CDBCR, and CDBYR2 and CDBCR2 for the bottom field in both-field capture) alternately (figure 34.48). When captured data has been written for the number of lines set by CBDSR, a write end interrupt corresponding to each address setting register occurs. However, after write for one-frame (one-field) capture ends, a bundle write end interrupt does not occur even when bundle write has finished. • Data synchronous fetch This bit controls the number of lines of captured data to be written to the memory. When bundle write is set by this register, captured data is written in line units specified by CBDSR to the addresses specified by CDAYR and CDAYR2 alternately. When captured data has been written for the number of lines set by CBDSR, a write end interrupt corresponding to each address setting register occurs. However, after write for one-frame capture ends, a bundle write end interrupt does not occur even when bundle write has finished.

Bit	Bit Name	Initial Value	R/W	Description
16	CBE	0	R/W	• Data enable fetch This bit controls the number of bytes of captured data to be written to the memory. When bundle write is set by this register, captured data is written in byte units specified by CBDSR to the addresses specified by CDAYR and CDAYR2 alternately. When captured data has been written for the number of bytes set by CBDSR, a write end interrupt corresponding to each address setting register occurs. Also, only in data enable fetch, a bundle write end interrupt occurs when bundle write has finished after write for one-frame capture ends. Table 34.9 shows the correspondence between address setting registers and write end interrupt sources. Figure 34.49 shows the timing of write end interrupts. 0: Normal write 1: Bundle write
15 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	CFXAD	0	R/W	Sets the fixed address mode for outputting images or data processed by the CEU to the memory. If fixed address mode is selected, the addresses to which the CEU outputs images are not incremented and are always the same. In fixed address mode, addresses whose lower five bits are 0 must be set to the output address registers, CDAYR, CDACR, CDBYR, and CDBCR. 0: Output addresses for the output section are incremented (normal operation). 1: Output addresses for the output section are fixed (fixed address mode).
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
4	CDS	0	R/W	Sets the image format when outputting the image data captured in the YCbCr 4:2:2 format to the memory. When 0 is written to this bit, only the luminance component (Y) is output and no chrominance components (Cb and Cr) are output for the odd-numbered lines. With an interlace source image, similarly only the luminance component (Y) is output and no chrominance components (Cb and Cr) are output for the odd-numbered lines of the field. In data fetch mode, set this bit to 1. 0: Converts the YCbCr 4:2:2 format to the YCbCr 4:2:0 format before outputting data to the memory. 1: Outputs data in the YCbCr 4:2:2 format to the memory without conversion.
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2	COLS	0	R/W	Controls swapping in longword units for data output from the CEU. 0: Data is not swapped in longword units. 1: Data is swapped in longword units.
1	COWS	0	R/W	Controls swapping in word units for data output from the CEU. 0: Data is not swapped in word units. 1: Data is swapped in word units.
0	COBS	0	R/W	Controls swapping in byte units for data output from the CEU. 0: Data is not swapped in byte units. 1: Data is swapped in byte units.

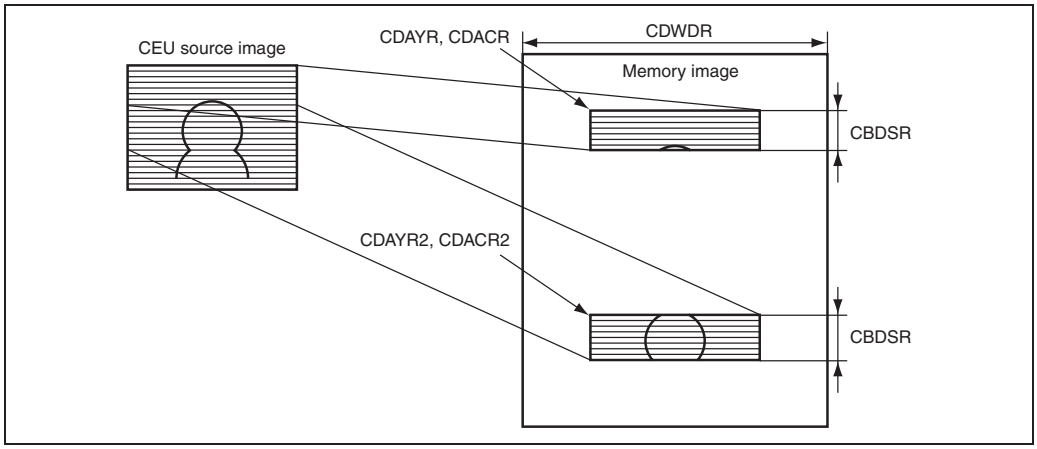


Figure 34.48 Image of Bundle Write to Memory

Table 34.9 Correspondence between Address Setting Registers and Write End Interrupt Sources

Address Setting Registers	Bundle Write End Interrupt Source
CDAYR, CDACR	CPBE1 bit in CETCR
CDAYR2, CDACR2	CPBE2 bit in CETCR
CDBYR, CDBCR	CPBE3 bit in CETCR
CDBYR2, CDBCR2	CPBE4 bit in CETCR

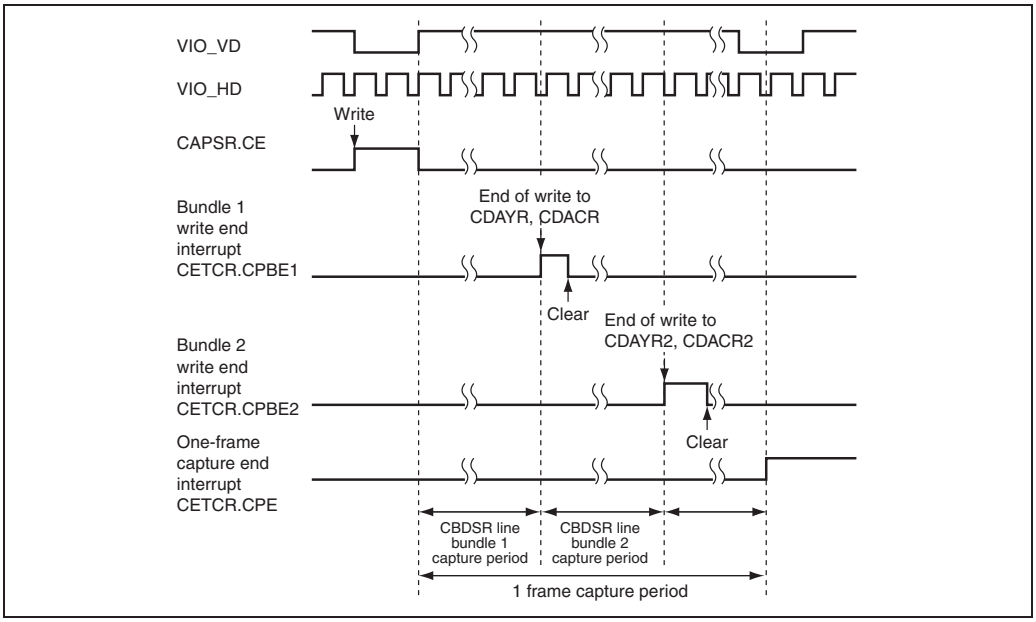


Figure 34.49 Timing of Write End Interrupts

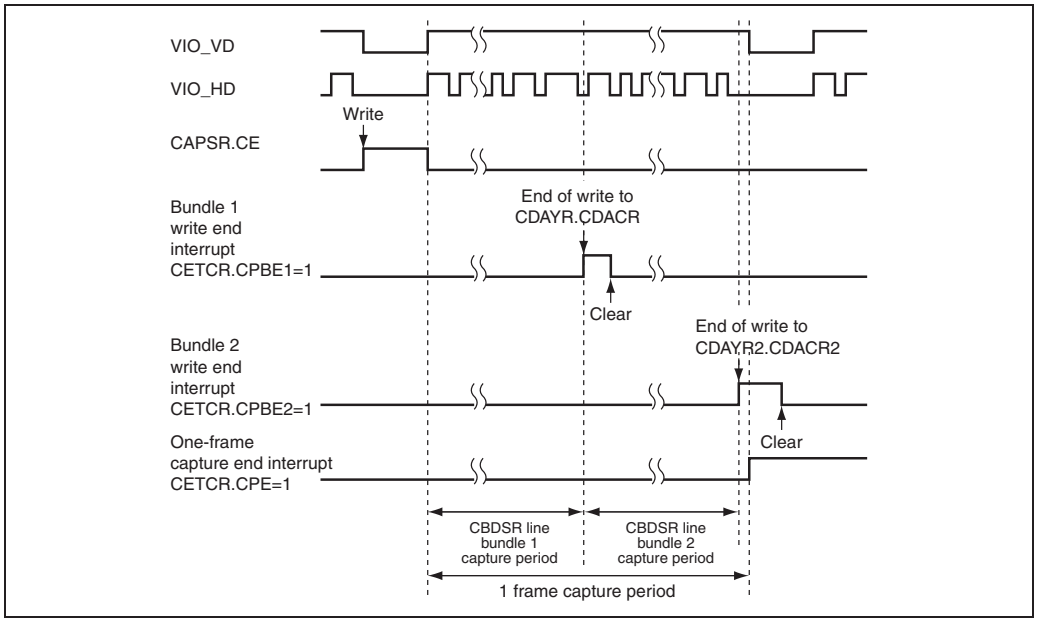


Figure 34.50 Timing of Write End Interrupts (Data Enable Fetch)

For data output from the CEU, the COLS, COWS, and COBS bits control swapping in longword, word, and byte units, respectively. Set these bits when data is misaligned because of a difference in endian. The data swapping bits are shown below. These bits can be set similarly in data fetch mode.

Data can be swapped in byte, word, longword, and byte-word-longword units, as shown in figure 34.51. To enable data swapping, set the corresponding control bit to B'1.

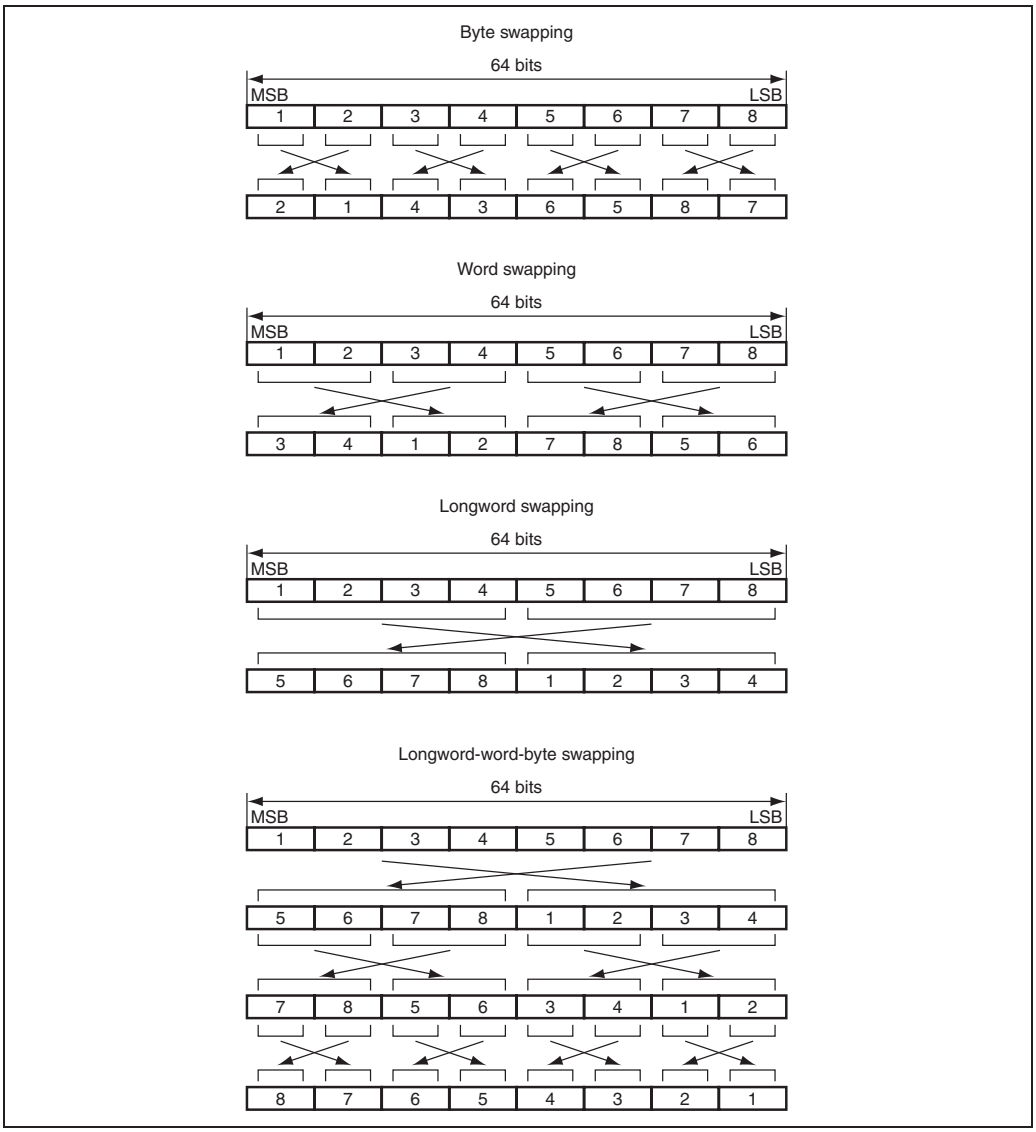


Figure 34.51 Data Swapping by Data Aligner

34.3.23 Capture Data Complexity Level Register (CDDCR)

CDDCR sets how to acquire the complexity level of the captured image. The CEU calculates the complexity level of the image from the luminance component value of the captured image. The result of comparing the complexity levels of continuous images can be useful information in detecting a scene change. CDDCR is not used in data fetch mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	DCOE	—	—	DCSL[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	DCOE	0	R/W	Enables or disables output of the complexity level of the captured image to the memory. When writing 1 to this bit, always set a memory address to write the complexity level. If capturing is started with no address set, data in the memory may be overwritten. In data fetch mode, clear this bit to 0. 0: Complexity level of the captured image is not output to the memory. 1: Complexity level of the captured image is output to the memory.
3, 2	—	00	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
1, 0	DCSL[1:0]	00	R/W	These bits select the operation pixel range when calculating the complexity level of an image. 00: Calculates the complexity level of the luminance component for 16 lines of the captured image. 01: Calculates the complexity level of the luminance component for eight lines of the captured image. 10: Calculates the complexity level of the luminance component for one display of the captured image. 11: Setting prohibited

34.3.24 Capture Data Complexity Level Address Register (CDDAR)

CDDAR specifies the address where the complexity level of the captured image is to be stored. The CEU writes the complexity level of the captured image to the memory when the DCOE bit in CDDCR is B'1. Set the start address of the memory area where the complexity level of the captured image is to be stored by CDDAR. CDDAR is not used in data fetch mode.

Note that the destination address should be set for each frame (field) also in continuous capture.

Whether or not to acquire the complexity level of the captured image is set by the DCOE bit in CDDCR, and the acquisition range (16 lines, eight lines, or one display) is set by the DCSL bit in CDDCR.

Because the address must be specified in 32 bits, the address set by CDDAR must be in longword units. As the setting is in longword units, the lower two bits are always fixed to 0.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DCAR[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DCAR[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	DCAR[31:2]	H'0000 0000	R/W	These bits set the address for storing the complexity level of the captured image (4-byte units).
1, 0	DCAR[1:0]		R	

Set the address of the starting point of the memory area where the complexity level of the captured image is to be stored in this register, as shown in figure 34.52. The complexity level has an output data format in longword units like that in figure 34.53, and is saved in the memory in this format.

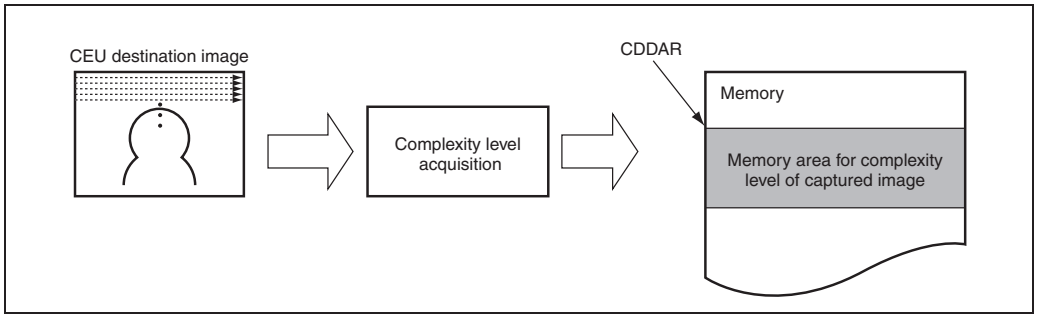


Figure 34.52 Memory Area for Complexity Level of Captured Image

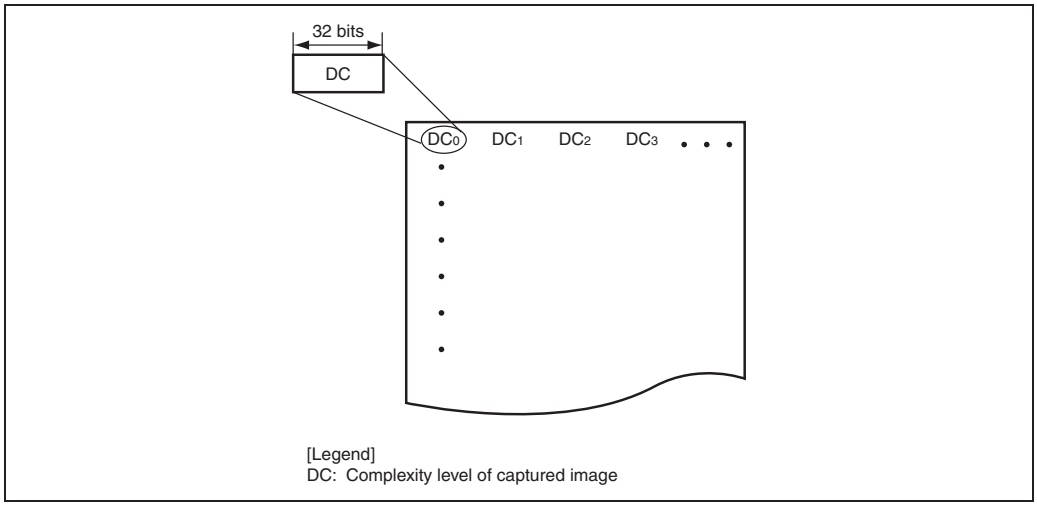


Figure 34.53 Image of Storing Complexity Level of Captured Image in Memory

34.3.25 Capture Event Interrupt Enable Register (CEIER)

CEIER enables or disables interrupts of the event flag register that generates CEU interrupts.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	NVDIE	NHDIE	FWFIE	DCOFIE	—	VBPIE	—	IGVSIE	IGHSIE	CDTOFIE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R	R/W	R	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CPBE4IE	CPBE3IE	CPBE2IE	CPBE1IE	—	—	VDIE	HDIE	—	—	—	IGRWIE	—	—	CFEIE	CPEIE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R	R	R	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25	NVDIE	0	R/W	Non-VD Interrupt Enable 0: Disables a non-VD interrupt. 1: Enables a non-VD interrupt.
24	NHDIE	0	R/W	Non-HD Interrupt Enable 0: Disables a non-HD interrupt. 1: Enables a non-HD interrupt.
23	FWFIE	0	R/W	FWF Interrupt Enable 0: Disbales a FWF interrupt. 1: Enables a FWF interrupt.
22	DCOFIE	0	R/W	DCOF Interrupt Enable 0: Disables a DCOF interrupt. 1: Enables a DCOF interrupt.
21	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
20	VBPIE	0	R/W	VBP Interrupt Enable 0: Disables a VBP interrupt. 1: Enables a VBP interrupt.

Bit	Bit Name	Initial Value	R/W	Description
19	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
18	IGVSIE	0	R/W	IGVS Interrupt Enable 0: Disables an IGVS interrupt. 1: Enables an IGVS interrupt. * When CSI2 is used(CAMCR.DTIF[1:0] = b'11), 0 is set to this bit.
17	IGHSIE	0	R/W	IGHS Interrupt Enable 0: Disables an IGHS interrupt. 1: Enables an IGHS interrupt. * When CSI2 is used(CAMCR.DTIF[1:0] = b'11), 0 is set to this bit.
16	CDTOFIE	0	R/W	CDTOF Interrupt Enable 0: Disables a CDTOF interrupt. 1: Enables a CDTOF interrupt.
15	CPBE4IE	0	R/W	CPBE4 Interrupt Enable 0: Disables a CPBE4 interrupt. 1: Enables a CPBE4 interrupt.
14	CPBE3IE	0	R/W	CPBE3 Interrupt Enable 0: Disables a CPBE3 interrupt. 1: Enables a CPBE3 interrupt.
13	CPBE2IE	0	R/W	CPBE2 Interrupt Enable 0: Disables a CPBE2 interrupt. 1: Enables a CPBE2 interrupt.
12	CPBE1IE	0	R/W	CPBE1 Interrupt Enable 0: Disables a CPBE1 interrupt. 1: Enables a CPBE1 interrupt.
11, 10	—	00	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
9	VDIE	0	R/W	VD Interrupt Enable 0: Disables a VD interrupt. 1: Enables a VD interrupt.
8	HDIE	0	R/W	HD Interrupt Enable 0: Disables an HD interrupt. 1: Enables an HD interrupt.
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	IGRWIE	0	R/W	Register-Access-During-Capture Interrupt Enable 0: Disables a register-access-during-capture interrupt. 1: Enables a register-access-during-capture interrupt.
3, 2	—	00	R	Reserved These bits are always read as 0. The write value should always be 0.
1	CFEIE	0	R/W	CFE Interrupt Enable 0: Disables a CFE interrupt. 1: Enables a CFE interrupt.
0	CPEIE	0	R/W	One-Frame Capture End Interrupt Enable 0: Disables a one-frame capture end interrupt. 1: Enables a one-frame capture end interrupt.

34.3.26 Capture Event Flag Clear Register (CETCR)

CETCR notifies the CPU of the source of an interrupt that is generated in the CEU. The flags of CETCR can be used as interrupt signals. When the corresponding interrupt is enabled, an interrupt is generated. To clear the interrupt, clear the bit corresponding to the interrupt source to 0. After several cycles have passed after modifying the bit, the interrupt is cleared.

To clear the bit corresponding to the interrupt source to be cleared to 0 and retain that state, write 1 to that bit. For example, to clear only the CPE bit to 0, write H'FFFF FFFE to CETCR.

In CETCR, only bits to which 0 is written are cleared. Bits to which 1 is written retain their current values. To clear an interrupt source, write 0 only to the bit corresponding to the interrupt source to be cleared, and 1 to the other bits.

Note: Since the CETCR value becomes undefined in the following cases, clear all bits in CETCR to 0.
- VD and HD bits immediately after reset
- All bits after the clock is stopped
- VD and HD bits after the polarities of the capture interface sync signals are changed

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	NVD	NHD	FWF	DCOF	—	VBP	—	IGVS	IGHS	CDTOF
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R	R/W	R	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CPBE4	CPBE3	CPBE2	CPBE1	—	—	VD	HD	—	—	—	IGRW	—	—	CFE	CPE
Initial value:	0	0	0	0	0	0	—	—	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R	R	R	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25	NVD	0	R/W	This bit is used for an interrupt indicating that no VD was input. A non-VD interrupt occurs when the 14-bit internal counter becomes full. Accordingly, this bit is set to 1 when no VD has been input for at least 16,384 lines since the last VD was input.

Bit	Bit Name	Initial Value	R/W	Description
24	NHD	0	R/W	This bit is used for an interrupt indicating that no HD was input. The timing for a non-HD interrupt to occur differs depending on the bit width of the digital image input pins. 8-bit digital image input pins: Occurs when the 11-bit internal counter that is incremented every eight cycles becomes full. Accordingly, this bit is set to 1 when no HD has been input for at least 16,376 cycles since the last HD was input. 16-bit digital image input pins: Occurs when the 12-bit internal counter that is incremented every four cycles becomes full. Accordingly, this bit is set to 1 when no HD has been input for at least 16,380 cycles since the last HD was input. When connecting a camera whose HD is fixed low when VD is low, this bit may be set to 1.
23	FWF	0	R/W	The interrupt is generated when data is written to the address that exceeds the value specified with CFWCR.FMV. This bit is set to 1 when data is written to the address that exceeds the value specified with CFWCR.FMV while CFWCR.FWE = 1.
22	DCOF	0	R/W	This bit is used for an interrupt indicating that the data requested to be transferred during acquisition of the complexity level of an image has been overwritten with subsequent data. Since there is no buffer to store data while acquiring the complexity level of an image, if data transfer to the bus is not completed until the next complexity level is calculated, data waiting to be transferred to the bus will be overwritten by the next data. This bit is set to 1 when the complexity level of the next image overwrites the complexity level of the image waiting to be transferred to the bus.
21	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
20	VBP	0	R/W	This bit is used for an interrupt indicating that VD has been input while the CEU holds data (insufficient V.B.P.). The conditions for a VBP interrupt to occur are as follows: • Condition 1 VD is input when there is captured data within the CEU. • Condition 2 The last transfer data cannot be internally detected due to a write buffer overflow or an illegal HD so that the end timing is unclear until the next VD (By generating a VBP interrupt at the VD input timing, capture fail can be announced.) When a VBP interrupt occurs, a capture end interrupt (CPE bit in CETCR) does not occur and the image of that frame is not captured correctly. Though a capture end interrupt (CPE bit) will occur on rare occasions, it should be ignored in this case. Capturing cannot be performed until the next VD (even if the CE bit (capture reservation signal) in CAPSR is 1, capturing does not start). In the case of condition 2, instead of waiting for a VBP interrupt to occur, execute a software reset (CPKIL bit in CAPSR) to stop capturing and then restart capturing. In this case, since capture operation is terminated without waiting for the next VD, a VBP interrupt does not occur and capturing can be performed from the next VD.
19	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
18	IGVS	0	R/W	This bit is used for an interrupt generated when the number of VD cycles set in CMCYR differ from the number of VD cycles input from an external module. This bit is set to 1 when there is an illegal VD input from an external module. This bit is set to 1 when the number of HD cycles for the VD input to the CEU differs from the value set in the VCYL bits in CMCYR. Note however that when the VCYL bits are cleared to 0, this interrupt does not occur.

Bit	Bit Name	Initial Value	R/W	Description
17	IGHS	0	R/W	This bit is used for an interrupt generated when the number of HD cycles set in CMCYR differ from the number of HD cycles input from an external module. This bit is set to 1 when there is an illegal HD input from an external module. This bit is set to 1 when the number of clock cycles for the HD input to the CEU differs from the value set in the HCYL bits in CMCYR. Note however that when the HCYL bits are cleared to 0, this interrupt does not occur.
16	CDTOF	0	R/W	This bit is used for an interrupt indicating that data overflowed in the CRAM of the write buffer. Since data is input at realtime from an external module in capture operations, the frame image is overwritten unless the captured data is transferred from the CEU internal buffer to the memory at a certain or higher transfer rate. This bit is set to 1 when writing the data in the CRAM of the CEU internal write buffer to the bus is not performed within time and data has overflowed.
15	CPBE4	0	R/W	This bit is used for an interrupt indicating that writing to CDBYR2 and CDBCR2 in a bundle write has finished. This interrupt is output when the last captured data has been transferred and the end notification received, regardless of the next HD input. This bit is set to 1 when data for the number of lines set in CBDSR has been captured and the last data transfer to the bus has completed. However, this interrupt does not occur when the last captured data in a bundle write is the last captured data of a frame (field).
14	CPBE3	0	R/W	This bit is used for an interrupt indicating that writing to CDBYR and CDBCR in a bundle write has finished. This interrupt is output when the last captured data has been transferred and the end notification received, regardless of the next HD input. This bit is set to 1 when data for the number of lines set in CBDSR has been captured and the last data transfer to the bus has completed. However, this interrupt does not occur when the last captured data in a bundle write is the last captured data of a frame (field).

Bit	Bit Name	Initial Value	R/W	Description
13	CPBE2	0	R/W	This bit is used for an interrupt indicating that writing to CDAYR2 and CDACR2 in a bundle write has finished. This interrupt is output when the last captured data has been transferred and the end notification received, regardless of the next HD input. This bit is set to 1 when data for the number of lines set in CBDSR has been captured and the last data transfer to the bus has completed. However, this interrupt does not occur when the last captured data in a bundle write is the last captured data of a frame (field).
12	CPBE1	0	R/W	This bit is used for an interrupt indicating that writing to CDAYR and CDACR in a bundle write has finished. This interrupt is output when the last captured data has been transferred and the end notification received, regardless of the next HD input. This bit is set to 1 when data for the number of lines set in CBDSR has been captured and the last data transfer to the bus has completed. However, this interrupt does not occur when the last captured data in a bundle write is the last captured data of a frame (field).
11, 10	—	00	R	Reserved These bits are always read as 0. The write value should always be 0.
9	VD	Undefined	R/W	This bit is used for an interrupt indicating that VD (vertical sync signal) was input from an external module. This bit is set to 1 when a VD input from an external module is detected. Immediately after the VDPOL bit in CAMCR is modified, a pseudo VD is input and this bit is set to 1. The VD interrupt after the VDPOL bit is modified should be ignored.

Bit	Bit Name	Initial Value	R/W	Description
8	HD	Undefined	R/W	This bit is used for an interrupt indicating that HD (horizontal sync signal) was input from an external module. This bit is set to 1 when an HD input from an external module is detected. Immediately after the HDPOL bit in CAMCR is modified, a pseudo HD is input and this bit is set to 1. The HD interrupt after the HDPOL bit is modified should be ignored.
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	IGRW	0	R/W	This bit is used for an interrupt indicating that during capturing, access was attempted to a register to which writing during operation is prohibited. Among the CEU registers, writing during capturing is prohibited for some registers. Table 34.10 shows which registers can/cannot be written to during capturing. This bit is set to 1 when a register to which writing during capturing is prohibited has been written to.
3, 2	—	00	R	Reserved These bits are always read as 0. The write value should always be 0.
1	CFE	0	R/W	This bit is used for an interrupt indicating that capturing of one field from an external module has finished. This interrupt is output when the last captured data has been transferred and the end notification received, regardless of the next VD input (see figure 34.54). This interrupt occurs only in both-field capture mode.
0	CPE	0	R/W	This bit is used for an interrupt indicating that capturing of one frame from an external module has finished. This interrupt is output when the last captured data has been transferred and the end notification received, regardless of the next VD input. This interrupt indicates that capturing of one frame has finished. This bit is set to 1 when the image of the size set in CAPWR is captured and the last data transfer to the bus finished (see figure 34.55).

Table 34.10 Registers that Can/Cannot Be Modified during Capturing

Register Name	Modification during Capturing	Register Name	Modification during Capturing
CAPSR	Possible	CDBYR	Possible
CAPCR	Prohibited	CDBCR	Possible
CAMCR	Prohibited	CBDSR	Possible
CMCYR	Prohibited	CLFCR	Possible
CAMOR	Possible	CDOCR	Possible
CAPWR	Possible	CDDCR	Possible
CAIFR	Prohibited	CDDAR	Possible
CSTCR	Possible	CEIER	Possible
CSECR	Possible	CETCR	Possible
CRCNTR	Possible	CSTSR	Prohibited
CRCMPR	Prohibited	CSRTR	Possible
CFLCR	Possible	CDAYR2	Possible
CFSZR	Possible	CDACR2	Possible
CDWDR	Possible	CDBYR2	Possible
CDAYR	Possible	CDBCR2	Possible
CDACR	Possible		

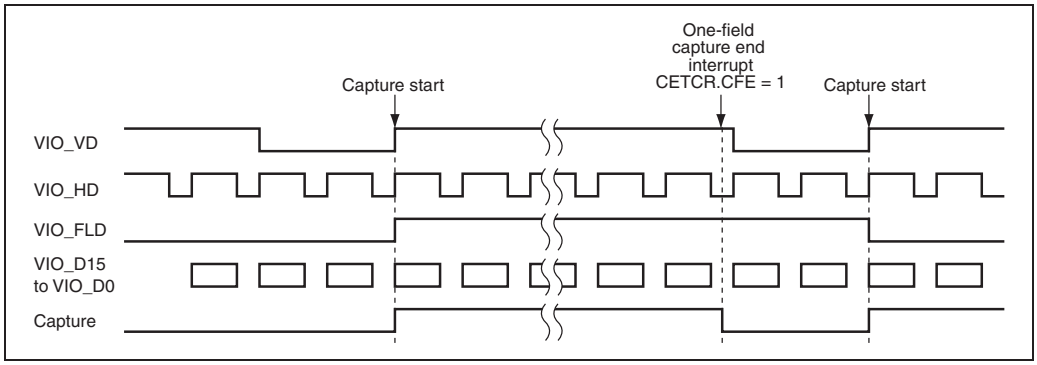


Figure 34.54 CFE Generation Timing

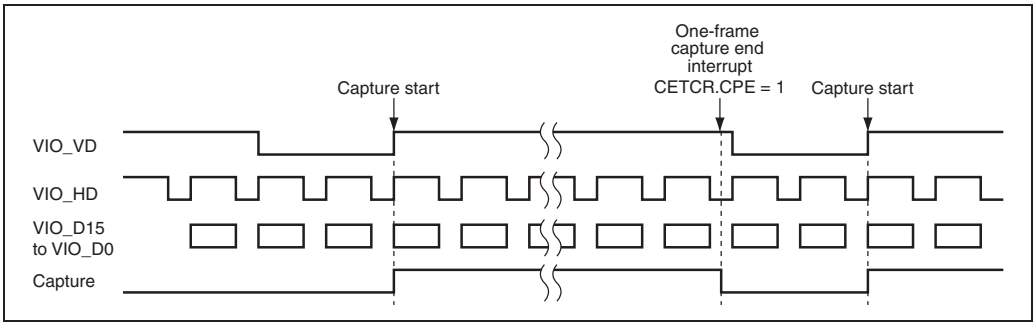


Figure 34.55 CPE Generation Timing

34.3.27 Capture Status Register (CSTSR)

CSTSR indicates the internal status of the CEU. CSTSR differs from CETCR in that no interrupt is generated for the events indicated in CSTSR.

The CEU operating/halt state can be confirmed using CSTSR. To confirm the halt state of the CEU, make sure that all status bits (bits 9, 8, and 0) indicating that the CEU is operating are cleared to 0 for sure.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	CRST	—	—	—	—	—	—	—	CP FLD
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	CP REQ	CP ACK	—	—	—	—	—	—	—	CP TON
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	CRST	0	R	Indicates which register plane is currently used. 0: Plane A of the register is being used. 1: Plane B of the register is being used.

Bit	Bit Name	Initial Value	R/W	Description
23 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	CPFLD	0	R	Indicates which field is being captured. 0: Bottom field is being captured. 1: Top field is being captured.
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	CPREQ	0	R	Indicates the request output port level of the bridge interface.
8	CPACK	0	R	Indicates the acknowledge input port level of the bridge interface.
7 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	CPTON	0	R	Indicates that the CEU is operating. This bit retains 1 during the period that starts from the internal VD at capture start and ends when a one-frame capture end interrupt occurs. Figure 34.56 shows the CEU operating period.

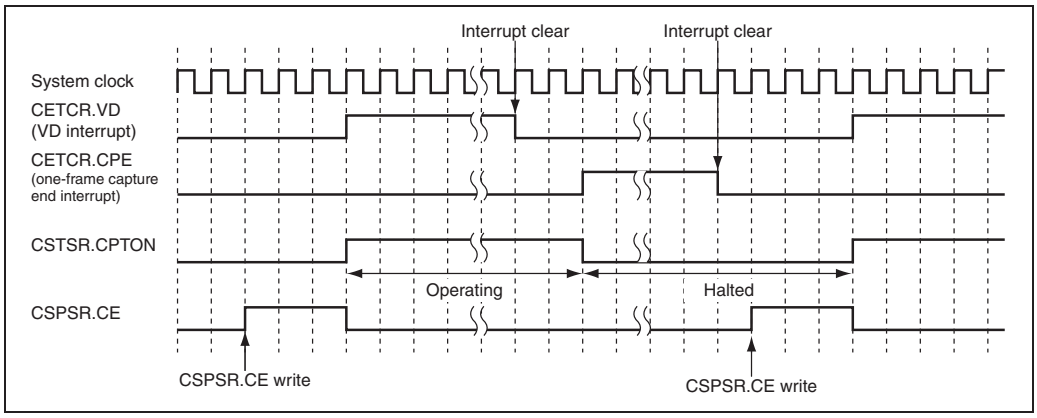


Figure 34.56 Operating Status during Capturing

34.3.28 Capture Software Reset Register (CSRTR)

CSRTR executes a module reset of the CEU internal circuit. This reset processing that does not take the bus state in account should not be used in the normal state.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	$\overline{\text{ALLRST}}$
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	ALLRST	0	R/W	Resets the entire CEU and request signals to the bus. 0: Normal state 1: Performs a module reset of the entire sync circuit of the CEU.

Do not modify the ALLRST bit except for in special cases, such as when the entire system hangs. If the ALLRST bit is written to while the CEU is operating, a fatal error may occur; the system may get out of control, or memory areas other than the specified area may be overwritten.

34.3.29 Capture Data Size Register (CDSSR)

CDSSR indicates the size of data written to the memory in data enable fetch. As this register indicates a correct value at the end of capture, confirm this register when capture is completed.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CDSS[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CDSS[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	CDSS[31:0]	H'0000 0000	R	Indicate the size of data written to the memory in data enable fetch. In a bundle write, size of data written to the selected address at the end of one-frame capture is indicated. In a bundle write, as soon as the number of bytes specified by CBDSR is transferred to the bus, address to which data is written is switched. Therefore, if one-frame capture is completed at the same time as a bundle write is completed, this register indicates H'0000 0000. Figures 34.57 and 34.58 show the overall timing of the CDSSR operation in a bundle write.

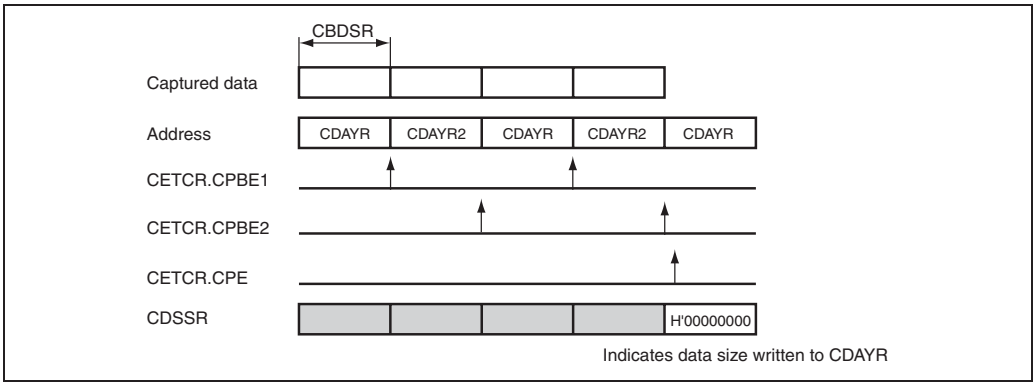


Figure 34.57 Overall Timing of CDSSR Operation in Bundle Write (When Bundle Write End and Capture End Coincide)

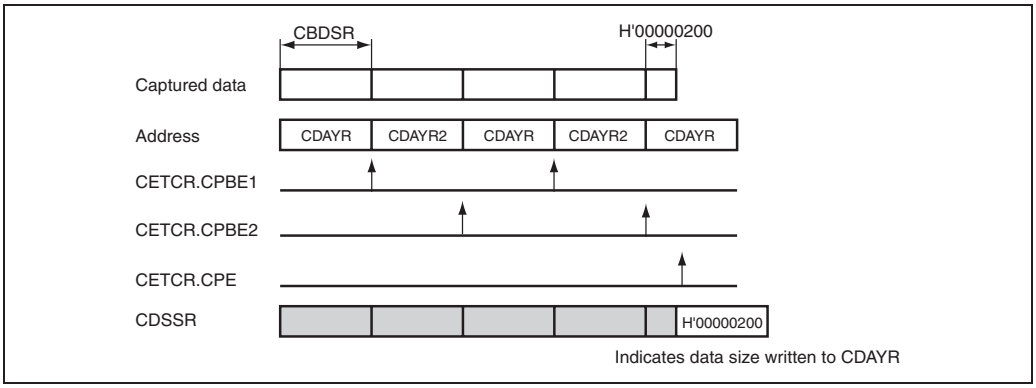


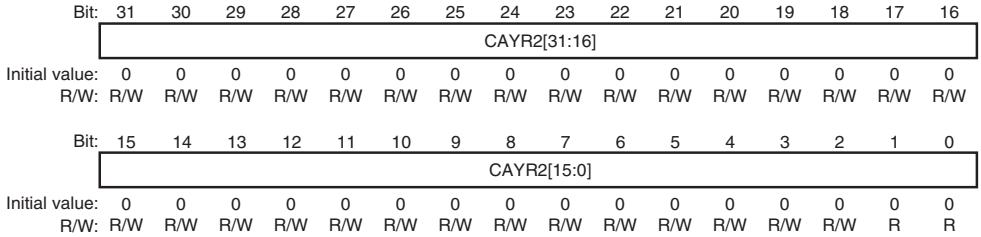
Figure 34.58 Overall Timing of CDSSR Operation in Bundle Write (When Bundle Write End and Capture End Does Not Coincide)

34.3.30 Capture Data Address Y Register 2 (CDAYR2)

CDAYR2 specifies the address for the luminance (Y) component used in a bundle write. CDAYR2 is used only in a bundle write.

CDAYR2 specifies the address where the Y component of the captured data is to be stored in frame image capture or one-field image capture, and the address where the Y component of the captured top field is to be stored in both-field image capture. The CEU separates the captured image data into the luminance component data (Y) and the chrominance component data (C), and stores them in the memory via the bus. In frame image capture or one-field image capture, set the start address of the memory area where the Y component of the captured data is to be stored by CDAYR2. In both-field image capture, set the start address of the memory area where the Y component of the captured top-field image is to be stored by CDAYR2. CDAYR2 is not used in data fetch.

Because the address must be specified in 32 bits, the address set by CDAYR2 must be in longword units. As the setting is in 4-pixel units, the lower two bits are always fixed to 0.



Bit	Bit Name	Initial Value	R/W	Description
31 to 2	CAYR2[31:2]	H'0000 0000	R/W	• Frame image capture: These bits set the address for storing the Y component data of the captured data (4-pixel units).
1, 0	CAYR2[1:0]		R	• One-field image capture: These bits set the address for storing the Y component data of the captured data (4-pixel units).
				• Both-field image capture: These bits set the address for storing the Y component data of the captured top-field data (4-pixel units).

Set the address of the starting point of the memory area where the Y component of the captured image is to be stored in this register, as shown in figure 34.59.

- Frame image capture: Set the address of the starting point of the memory area where the Y component of the captured image is to be stored.
- One-field image capture: Set the address of the starting point of the memory area where the Y component of the captured image is to be stored.
- Both-field image capture: Set the address of the starting point of the memory area where the Y component of the captured top-field image is to be stored.
- Data enable fetch: Set the address of the starting point of the memory area where the fetched data is to be stored in 32-byte units.

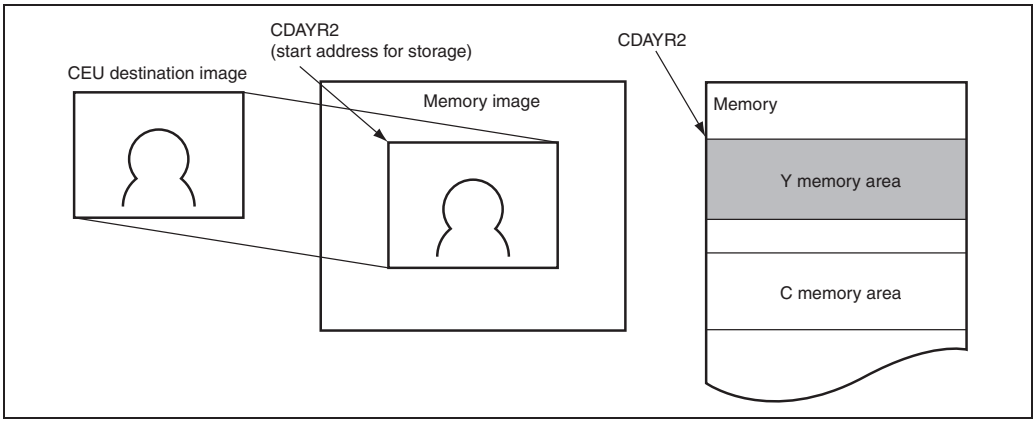


Figure 34.59 Relationship between Captured Image and Y Component Memory Area

34.3.31 Capture Data Address C Register 2 (CDACR2)

CDACR2 specifies the address for the chrominance (C) component used in a bundle write. CDACR2 is used only in a bundle write.

CDACR2 specifies the address where the C component of the captured data is to be stored in frame image capture or one-field image capture, and the address where the C component of the captured top field is to be stored in both-field image capture. The CEU separates the captured image data into the luminance component data (Y) and the chrominance component data (C), and stores them in the memory via the bus. In frame image capture or one-field image capture, set the start address of the memory area where the C component of the captured data is to be stored by CDACR2. In both-field image capture, set the start address of the memory area where the C component of the captured top-field image is to be stored by CDACR2. CDACR2 is not used in data fetch.

Because the address must be specified in 32 bits, the address set by CDACR2 must be in longword units. As the setting is in 4-pixel units, the lower two bits are always fixed to 0.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CACR2[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CACR2[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	CACR2[31:2]	H'0000 0000	R/W	• Frame image capture: These bits set the address for storing the C component data of the captured data (4-pixel units). • One-field image capture: These bits set the address for storing the C component data of the captured data (4-pixel units). • Both-field image capture: These bits set the address for storing the C component data of the captured top-field data (4-pixel units). • Data enable fetch: These bits set the address for storing data (32-byte units).
1, 0	CACR2[1:0]		R	

Set the address of the starting point of the memory area where the C component of the captured image is to be stored in this register, as shown in figure 34.60. The C component has an output data format like that in figure 34.61, and is saved in the memory in this format.

- Frame image capture: Set the address of the starting point of the memory area where the C component of the captured image is to be stored.
- One-field image capture: Set the address of the starting point of the memory area where the C component of the captured image is to be stored.
- Both-field image capture: Set the address of the starting point of the memory area where the C component of the captured top-field image is to be stored.

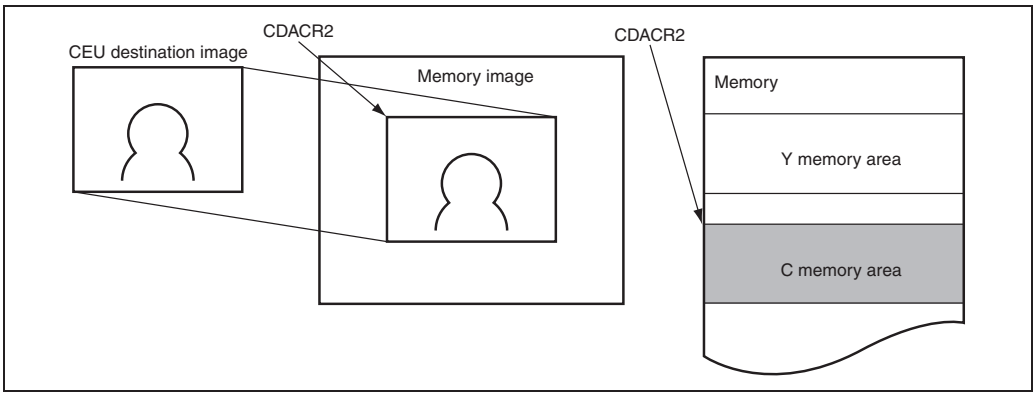


Figure 34.60 Relationship between Captured Image and C Component Memory Area

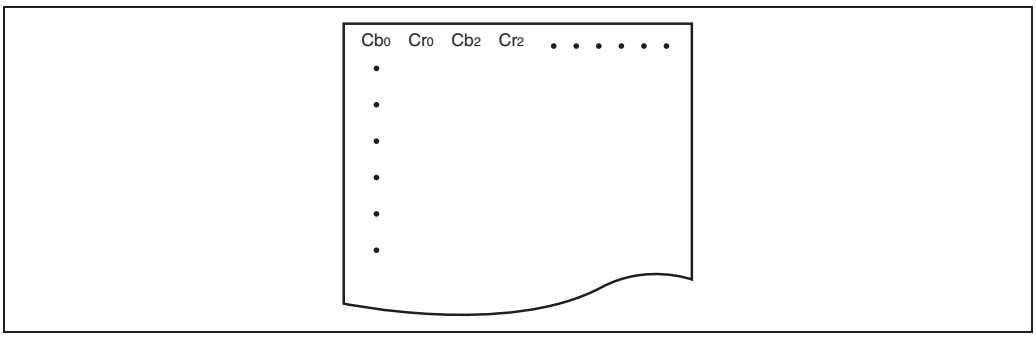


Figure 34.61 Image of Storing C Components in Memory

34.3.32 Capture Data Bottom-Field Address Y Register 2 (CDBYR2)

CDBYR2 specifies the address for the luminance (Y) component of the bottom field used in a bundle write. CDBYR2 is used only in a bundle write.

CDBYR2 specifies the address where the Y component of the captured bottom-field data is to be stored in both-field image capture. The CEU separates the captured image data into the luminance component data (Y) and the chrominance component data (C), and stores them in the memory via the bus. Set the start address of the memory area where the Y component of the bottom-field image captured in both-field image capture is to be stored by CDBYR2. CDBYR2 is not used in frame image capture, one-field image capture, or data fetch.

Because the address must be specified in 32 bits, the address set by CDBYR2 must be in longword units. As the setting is in 4-pixel units, the lower two bits are always fixed to 0.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CBYR2[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CBYR2[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	CBYR2[31:2]	H'0000 0000	R/W	These bits set the address for storing the Y component data of the captured bottom-field data (4-pixel units).
1, 0	CBYR2[1:0]		R	

Set the address of the starting point of the memory area where the Y component of the captured bottom-field image is to be stored in this register, as shown in figure 34.62.

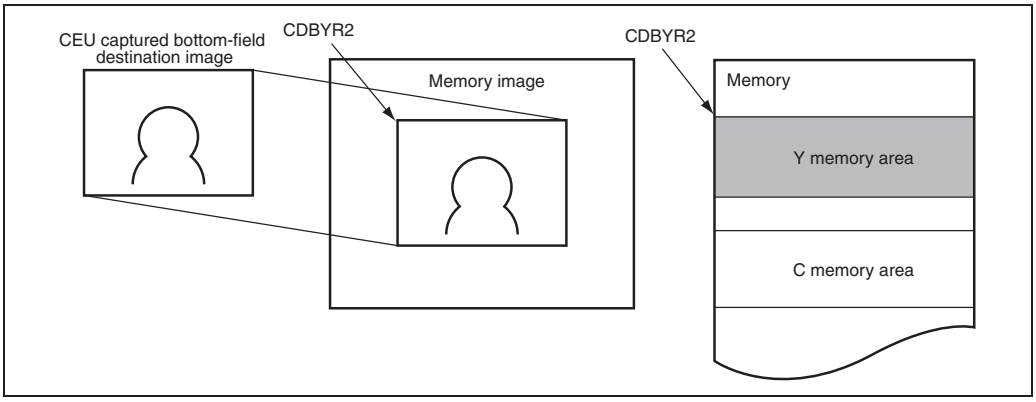


Figure 34.62 Relationship between Captured Bottom-Field Image and Y Component Memory Area

34.3.33 Capture Data Bottom-Field Address C Register 2 (CDBCR2)

CDBCR2 specifies the address for the chrominance (C) component of the bottom field used in a bundle write. CDBCR2 is used only in a bundle write.

CDBCR2 specifies the address where the C component of the captured bottom-field data is to be stored in both-field image capture. The CEU separates the captured image data into the luminance component data (Y) and the chrominance component data (C), and stores them in the memory via the bus. Set the start address of the memory area where the C component of the bottom-field image captured in both-field image capture is to be stored by CDBCR2. CDBCR2 is not used in frame image capture, one-field image capture, or data fetch.

Because the address must be specified in 32 bits, the address set by CDBCR2 must be in longword units. As the setting is in 4-pixel units, the lower two bits are always fixed to 0.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CBCR2[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CBCR2[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	CBCR2[31:2]	H'0000 0000	R/W	These bits set the address for storing the C component data of the captured bottom-field data (4-pixel units).
1, 0	CBCR2[1:0]		R	

Set the address of the starting point of the memory area where the C component of the captured bottom-field image is to be stored in this register, as shown in figure 34.63. The C component has an output data format like that in figure 34.64, and is saved in the memory in this format.

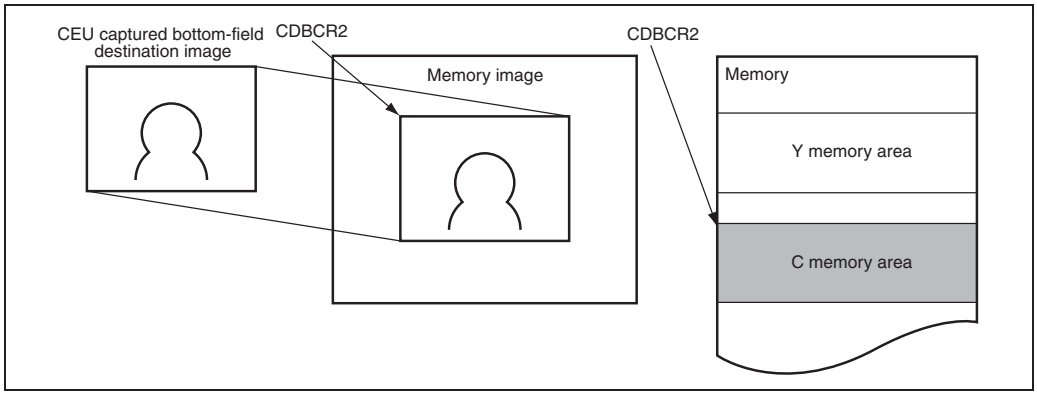


Figure 34.63 Relationship between Captured Bottom-Field Image and C Component Memory Area

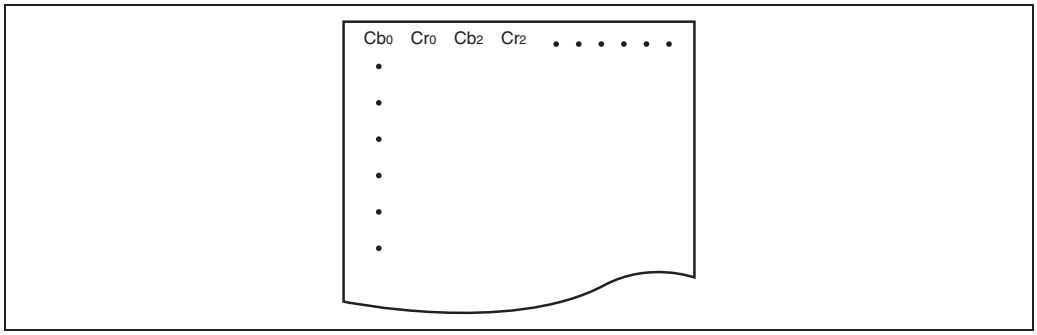


Figure 34.64 Image of Storing C Components in Memory

34.4 Usage Notes for CEU

34.4.1 Conditions for Connection to an External Module

(1) Clock Frequency

The external input clock should have a frequency at least the same as the CEU operating clock frequency, with jitter on both sides included.

CEU operating clock frequency ≥ External input clock frequency

(2) Blanking Period

The blanking (back-porch) period of the horizontal sync signal HD must be at least 20 cycles.

(3) Fixed Period of Field Identification Signal

The field identification signal FLD should be fixed for at least 1-HD period since a VD input

34.4.2 End Interrupt Output at Time of Scale-Down Processing

Depending on the scale-down factor in relation to the number of input pixels, the number of pixels output by the scale-down filter might be less than the required number of pixels. As a result, the interrupt for the end of the capture might not be output. This is indicated by an "—" in the Interrupt column of table 34.11. Do not set the size of values indicated by an "—" in table 34.12.

Table 34.11 Conditions for Generating an End Interrupt for Scale-Down Processing

Horizontal MANT Register Settings CFLCR[15:12]	Number of Input Horizontal Pixels CAPWR[12:0]	Number of PRE Filter Output Pixels	Image	Interrupt
0 or more, less than 2	Normal operation			
2 or more, less than 4	16n	Even	Clipped capture	Clipped capture
	16n + 4	Even	Clipped capture	Clipped capture
	16n + 8	Even	Clipped capture	Clipped capture
	16n + 12	Even	Clipped capture	Clipped capture
4 or more, less than 8	16n	Even	Clipped capture	Clipped capture
	16n + 4	Odd	*	Clipped capture
	16n + 8	Even	Clipped capture	Clipped capture
	16n + 12	Odd	*	Clipped capture
8 or more	16n	Even	Clipped capture	Clipped capture
	16n + 4	Even	Clipped capture	Clipped capture
	16n + 8	Odd	—	—
	16n + 12	Odd	*	Clipped capture

[Legend]

*: 4 pixels other than the specified range for capture affect the output pixel of horizontal end filter. There is no trouble with picture quality for the extraction capture.

—: Trouble with operations might be generated. Set the size of the value other than this.

34.4.3 Restrictions on Input/Output Functions

Table 34.12 lists the restrictions regarding the CEU input/output functions.

Table 34.12 Restrictions on CEU Input/Output Functions

Item	Restrictions
External module interface	The operating clock of the external module should always have a frequency at most the same as that of the CEU operating clock, with jitter on both sides included.
	Selecting the interface, or modifying the frequency of the external module operating clock or HD/VD polarity must be done when capture operations are halted for sure.
	The capture horizontal size in image capture must be specified as follows: 8-bit interface: 8-cycle units 16-bit interface: 4-cycle units
	The capture horizontal size in data fetch must be specified as follows: 8-bit interface: 4-cycle units 16-bit interface: 2-cycle units
	The capture vertical size must be specified in 4-line units.
	The maximum number of cycles in the horizontal sync signal period should be 16,383 external input clock cycles.
	The maximum number of lines (HD count) in the vertical sync signal should be 16,383 lines.
	The minimum number of captured pixels should be 48 × 48.
	The maximum number of captured pixels should be 64M (8188 × 8188) pixels. Note that it always depends on the camera clock frequency.
	Captured size in data enable fetch Maximum: 6 Mbytes (2048 × 1536 × 2) Minimum: 16 bytes (must be specified in 4-byte units)

Item	Restrictions
Memory output	The output address must be specified in longword units.
	The horizontal size of the destination image (memory) must be specified in 4-pixel units.
	The number of horizontal output pixels (= horizontal clipping size) must be specified in 4-pixel units.
	The number of vertical output lines (HD) (= vertical clipping size) must be specified in 4-line (HD) units.
	In fixed address mode, the lower five bits in an output address must be 0, and the output size must be specified in 8-pixel (8-byte) units.
	In data enable fetch bundle write, the output address must be specified in 32-byte units.
Internal processing	The filter clipping size must be specified as a value equal to or lower than the actual output size of the filter.

34.4.4 CSI2 connection special setting

When CSI2 is connected and used (CAMCR.DTIF[1:0] = b'11), A special following setting is necessary.

- CAMOR.HOFST[12:0]

  Horizontal offset is every two pixels. And, a set value is twice the pixel count.

  For example, When 60 pixels are done in offset, CAMOR.HOFST[12:0] is 0x0078

- CAPWR.HWDTH[13:0]

  The pixel count that does capture is defined as "N". A set value is ((N – 2) * 2) or more.

Section 35 Video Engine Unit (VEU)

The VEU is a module used connected to the buses via bus bridge modules. The VEU reads an image from a specified memory area, and writes it back to a specified address.

35.1 Features

- Four modules are installed (VEU0, VEU1, VEU2, and VEU3)
- Format conversion using the RGB ⇔ YCbCr conversion function
- Scaling of an image using the filter function
- Tone reduction (quantization) to pack RGB data in 32-bit units
- Dithering for tone reduction of RGB data
- Removal of high-frequency components using the low-pass filter function
- Low-pass filter is applied to only the boundary of the blocks using the deblocking filter function
- Median filter function
- Edge enhancement of an image (enhancer function)
- Edge emphasis processing with FIR filter (VEU2 and 3)
- Plain α can be scaled (with RGB resize: VEU2 and 3)

35.2 Functional Overview of VEU

The functional overview of the VEU is shown in table 35.1. Some functions of the VEU cannot be used at the same time unless the VEU is re-activated. Table 35.2 shows which functions can/cannot be used simultaneously during one VEU activation.

Note that when the instructions at other places in this manual differ from instructions in the following table, the instructions in section 35.4, Usage Notes for VEU, are given priority.

Table 35.1 Functional Overview of VEU

Item	Function	Description	Note
Input format	YCbCr (4:4:4/4:2:2/4:2:0)		
	RGB pack		
Output format	YCbCr (4:4:4/4:2:2/4:2:0)		
	RGB pack		
Read mode	Normal read	8 to 960 lines can be set as the number of lines in bundle read	
	Bundle read		
Low-pass filter	Removal of high-frequency components		
FIR filter	Removal of high-frequency components / Edge enhancement		Only VEU2 and VEU3
Deblocking filter	Removal of high-frequency components only at the boundary of blocks		
Enhancer	Enhancement of image		
Median filter	Removal of shot noise		
Rotation/ inversion of image	Vertical or horizontal inversion	Can be specified independently	A combination of both functions can realize rotation by 180 degrees
	Rotation by 90 or 270 degrees	Rotated clockwise	
Scale-up, scale-down, or no scaling	Scale-up or scale-down of memory display	Any scaling factor from × 1/16 to × 16	
Format conversion	YCbCr ⇔ RGB conversion	Bidirectional conversion between YCbCr format and RGB format	

Item	Function	Description	Note
Dithering (tone reduction)	24 bpp	Full colors (16,700,000 colors)	Dithering not possible
	18 bpp	260,000 colors	Dithering not possible
	16 bpp	High colors (65,536 colors)	
	12 bpp	4,096 colors	
	8 bpp	256 colors	
Maximum image size	16M pixels	4092 pixels × 4092 lines*1,*2	
Minimum image size	4 x 4 pixels	4 pixels x 4 lines*3	

Note: The scaling factor of the filter can be set between 1/16 and 16. For details, see section 35.3.11, VEU Resize Filter Control Register (VRFCR), and section 35.3.12, VEU Resize Filter Size Clip Register (VRFSR).

*1 When the tap count is set to 11, the maximum number of horizontal pixel is to be 2048.

*2 The maximum input size in the resize processing becomes in 8188x8188 and the maximum output size becomes 4092x8188. (VEU2,VEU3)

*3 When the tap count is set to 11, the minimum image size becames 8x8.

Table 35.2 Simultaneous Usage of Functions in One VEU Activation

	Bundle Mode	Color Conversion	Low-Pass Filter (Deblocking Filter)	FIR Filter	Median Filter	Enhancer	Vertical/ Horizontal Inversion	90°/270° Rotation	Scale-Up/ Scale-Down
Bundle Mode	—	O	×	×	×	O	O	×	O
Color Conversion	O	—	O	O	O	O	O	O	O
Low-Pass Filter (Deblocking Filter)	×	O	—	×	O*1,*2	×	O	O*3	×
FIR Filter	×	O	×	—	×	×	O	×	×
Median Filter	×	O	O*1,*2	×	—	×	O	O*3	×
Enhancer	O	O	×	×	×	—	O	×	O
Vertical/ Horizontal Inversion	O	O	O	O	O	O	—	O	O
90°/270° Rotation	×	O	O*3	×	O*3	×	O	—	×
Scale-Up/ Scale-Down	O	O	×	×	×	O	O	×	—

[Legend]

O: Possible

×: Not possible

Notes: The register values corresponding to the items in this table are shown below.

Bundle mode: VESTR.VBE

Color conversion: VTRCR.TE

Low-pass filter: VFMCR.LPHV

Deblocking filter: VFMCR.LPHV && VFMCR.DBLK

Median filter: VFMCR.MED

Enhancer: VENHR.ENHH || VENHR.ENHV

Vertical/horizontal inversion: VFMCR.VMRR/VFMCR.HMRR

90°/270° rotation: VFMCR.POTR/VFMCR.POTL

Scale-up/scale-down: VRFCR != 0

1 order of deblocking filter → median filter is allowed. However, a reversed order is not allowed. (When a high-speed filter is processed, reverse order is possible.)

2 When the tap count is set to 11, the concurrent usage is not possible.

3 It is not possible to operate simultaneously when a high-speed filter is processed.

Figure 35.1 shows a block diagram of the VEU.

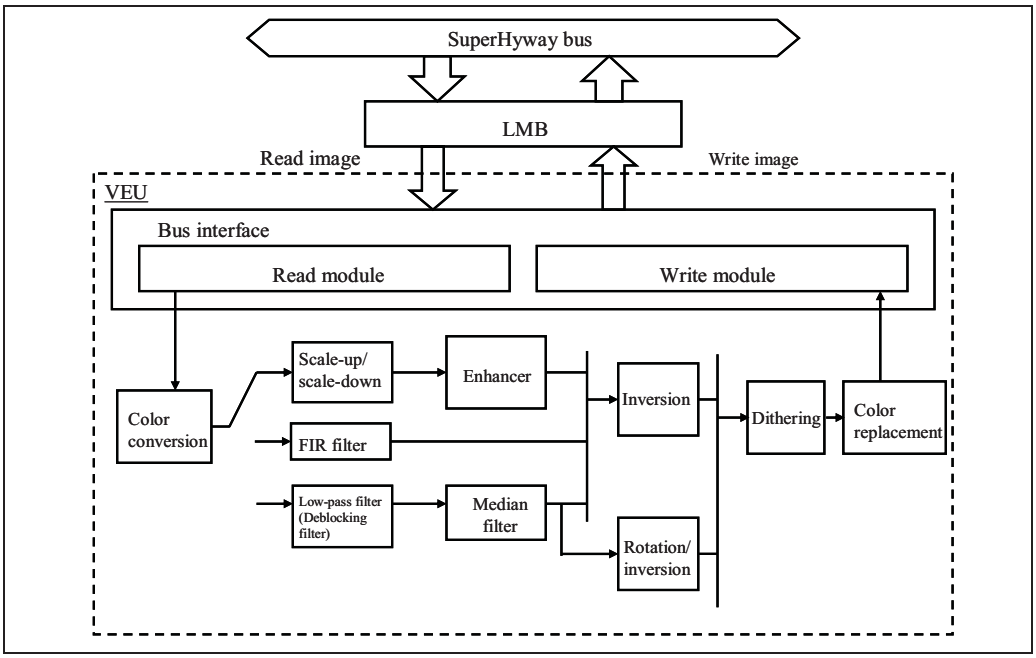


Figure 35.1 Block Diagram of VEU

Note: In figure 35.1, inversion indicates horizontal or vertical inversion, and rotation indicates 90° or 270° rotation.
In the inversion circuit after scale-up/scale-down, horizontal inversion, vertical inversion, or 180° rotation, which is a combination of the two types of inversion, can be performed.
In the rotation/inversion circuit after the median filter, in addition to the possible operations in the inversion circuit after scale-up/scale-down, 90° rotation, 270° rotation, a combination of 90° rotation and horizontal inversion, or a combination of 90° rotation and vertical inversion can be performed. When a high-speed filter is processed, the rotation operation cannot be used. (VMFCR.FLTPI=1)

- Operation

  Figure 35.2 shows the sequence of the VEU operation processing. Though the VEU has various functions, some functions cannot be used simultaneously during one VEU activation, as shown in table 35.2. Either flow 1a/1b or flow 2 shown in figure 35.2 is possible. Accordingly, processing in different flows cannot be performed together.

  1. Flow 1 is selected when the following condition is satisfied.
     VESTR.VBE || (VENHR.ENHH || VENHR.ENHV) || (VRFCR != 0) or VFMCE.FLTPI = 1
  2. Flow 2 is selected in cases other than above.

  Flow 1 separates into Flow 1a/1b further according to the condition.

  1a. It becomes scale-up/scale-down/edge emphasis processing of Flow 1a for VFMCR.FLTPI=0.

  1b. It becomes line filter processing of Flow 1b for VFMCR.FLTPI=1.

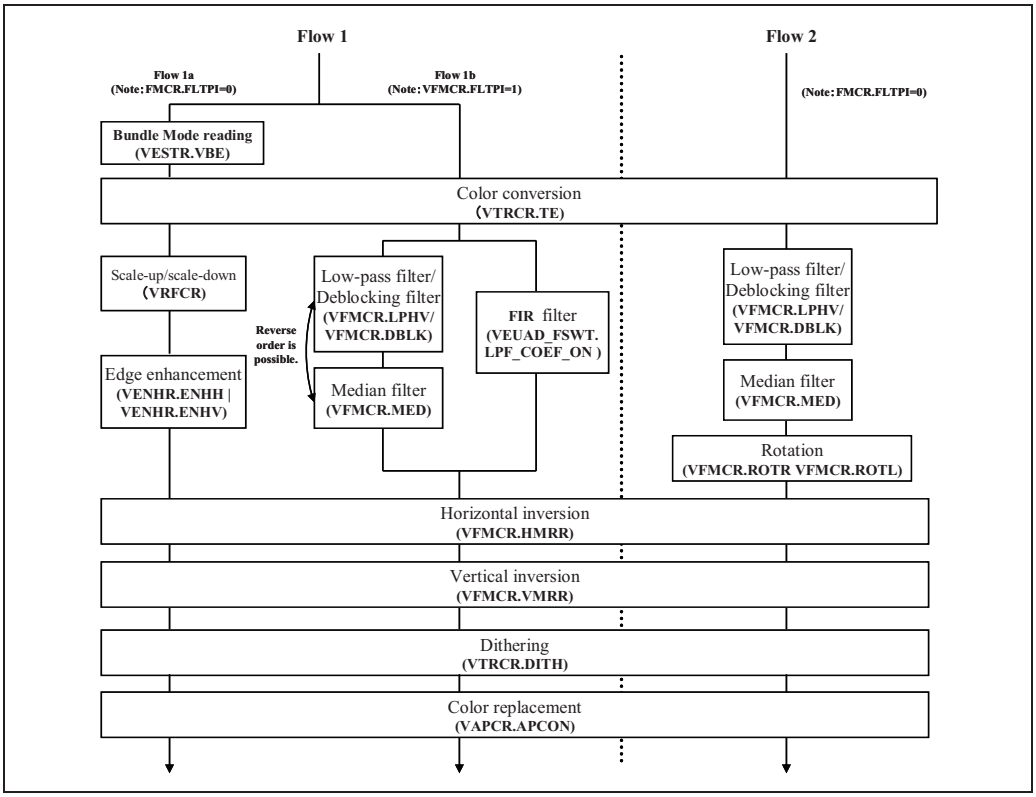


Figure 35.2 Register Settings, Processing Flows, and Simultaneously Executable Functions of VEU

35.3 Register Descriptions of VEU

(1) R/W Restrictions on VEU Registers

The read/write restrictions on the VEU registers are listed below. If the following register handling is not guaranteed, a malfunction may occur.

1. For the read-only bits in all VEU registers and the reserved areas, writing 1 is prohibited. Do not specify an unspecified value.
2. Though a value other than 0 may be read from a read-only bit, do not modify this bit.
3. For registers (bits) to which writing during operation is prohibited, do not modify them during operation (reading is possible). The VEU operating state can be confirmed by reading the VE bit in the VEU start register (VESTR). Modify the above registers when this bit is 0.
4. Allocate all VEU registers in a non-cacheable area.

(2) Terms and Abbreviations Used in This Section

The terms used in this section are described below.

1. "software reset" indicates that the VEU processing was halted and the current processing is stopped. The image processing result of the frame in which a software reset occurs is not guaranteed.
2. "module reset" indicates the VEU internal circuit was forcibly reset. In a module reset, reset processing is performed with no consideration to the hardware state. Therefore, if a module reset is generated when the VEU is operating normally, the VEU peripheral hardware may become unable to operate.
3. "during operation" in this section indicates a state in which the VE bit in the VEU start register (VESTR) is set to 1.
4. When a bit name in a register is referred to in this section, it is indicated in the format of (register name).(bit name).

   Example: VESTR.VE

(3) List of Registers

The register configuration of the VEU is shown in table 35.3. The register states in each processing mode are shown in table 35.4.

Table 35.3 Register Configuration of VEU

Register Name	Abbr.	R/W	Address	Access Size
VEU0 start register	VE0STR	R/W	H'FE92 0000	32
VEU0 source memory width register	VE0SWR	R/W	H'FE92 0010	32
VEU0 source size register	VE0SSR	R/W	H'FE92 0014	32
VEU0 source address Y register	V0SAYR	R/W	H'FE92 0018	32
VEU0 source address C register	V0SACR	R/W	H'FE92 001C	32
VEU0 bundle source size register	V0BSSR	R/W	H'FE92 0020	32
VEU0 destination memory width register	VE0DWR	R/W	H'FE92 0030	32
VEU0 destination address Y register	V0DAYR	R/W	H'FE92 0034	32
VEU0 destination address C register	V0DACR	R/W	H'FE92 0038	32
VEU0 transform control register	V0TRCR	R/W	H'FE92 0050	32
VEU0 resize filter control register	V0RFCR	R/W	H'FE92 0054	32
VEU0 resize filter size clip register	V0RFSR	R/W	H'FE92 0058	32
VEU0 enhance register	VE0NHR	R/W	H'FE92 005C	32
VEU0 resize filter sub control register	V0RSCR	R/W	H'FE92 0064	32
VEU0 resize filter size clip offset register	V0RSOR	R/W	H'FE92 0068	32
VEU0 filter mode control register	V0FMCR	R/W	H'FE92 0070	32
VEU0 vertical tap coefficient register	V0VTCR	R/W	H'FE92 0074	32
VEU0 horizontal tap coefficient register	V0HTCR	R/W	H'FE92 0078	32
VEU0 designated color register	V0APCR	R/W	H'FE92 0080	32
VEU0 conversion color register	VE0CCR	R/W	H'FE92 0084	32
VEU0 fill color specification register	V0FLCR	RW	H'FE92 0088	32
VEU0 address fixed register	V0AFXR	R/W	H'FE92 0090	32
VEU0 swapping register	V0SWPR	R/W	H'FE92 0094	32
VEU0 event interrupt enable register	VE0IER	R/W	H'FE92 00A0	32
VEU0 event register	VE0VTR	R/W	H'FE92 00A4	32
VEU0 status register	V0STAR	R	H'FE92 00B0	32
VEU0 module reset register	V0BSRR	R/W	H'FE92 00B4	32
VEU0 resize passband register	V0RPBR	R/W	H'FE92 00C8	32

Register Name	Abbr.	R/W	Address	Access Size
VEU1 start register	VE1STR	R/W	H'FE92 4000	32
VEU1 source memory width register	VE1SWR	R/W	H'FE92 4010	32
VEU1 source size register	VE1SSR	R/W	H'FE92 4014	32
VEU1 source address Y register	V1SAYR	R/W	H'FE92 4018	32
VEU1 source address C register	V1SACR	R/W	H'FE92 401C	32
VEU1 bundle source size register	V1BSSR	R/W	H'FE92 4020	32
VEU1 destination memory width register	VE1DWR	R/W	H'FE92 4030	32
VEU1 destination address Y register	V1DAYR	R/W	H'FE92 4034	32
VEU1 destination address C register	V1DACR	R/W	H'FE92 4038	32
VEU1 transform control register	V1TRCR	R/W	H'FE92 4050	32
VEU1 resize filter control register	V1RFCR	R/W	H'FE92 4054	32
VEU1 resize filter size clip register	V1RFSR	R/W	H'FE92 4058	32
VEU1 enhance register	VE1NHR	R/W	H'FE92 405C	32
VEU1 resize filter sub control register	V1RSCR	R/W	H'FE92 4064	32
VEU1 resize filter size clip offset register	V1RSOR	R/W	H'FE92 4068	32
VEU1 filter mode control register	V1FMCR	R/W	H'FE92 4070	32
VEU1 vertical tap coefficient register	V1VTCR	R/W	H'FE92 4074	32
VEU1 horizontal tap coefficient register	V1HTCR	R/W	H'FE92 4078	32
VEU1 designated color register	V1APCR	R/W	H'FE92 4080	32
VEU1 conversion color register	VE1CCR	R/W	H'FE92 4084	32
VEU1 fill color specification register	V1FLCR	RW	H'FE92 4088	32
VEU1 address fixed register	V1AFXR	R/W	H'FE92 4090	32
VEU1 swapping register	V1SWPR	R/W	H'FE92 4094	32
VEU1 event interrupt enable register	VE1IER	R/W	H'FE92 40A0	32
VEU1 event register	VE1VTR	R/W	H'FE92 40A4	32
VEU1 status register	V1STAR	R	H'FE92 40B0	32
VEU1 module reset register	V1BSRR	R/W	H'FE92 40B4	32
VEU1 resize passband register	V1RPBR	R/W	H'FE92 40C8	32

Register Name	Abbr.	R/W	Address	Access Size
VEU2 start register	VE2STR	R/W	H'FE92 8000	32
VEU2 source memory width register	VE2SWR	R/W	H'FE92 8010	32
VEU2 source size register	VE2SSR	R/W	H'FE92 8014	32
VEU2 source address Y register	V2SAYR	R/W	H'FE92 8018	32
VEU2 source address C register	V2SACR	R/W	H'FE92 801C	32
VEU2 bundle source size register	V2BSSR	R/W	H'FE92 8020	32
VEU2 destination memory width register	VE2DWR	R/W	H'FE92 8030	32
VEU2 destination address Y register	V2DAYR	R/W	H'FE92 8034	32
VEU2 destination address C register	V2DACR	R/W	H'FE92 8038	32
VEU2 transform control register	V2TRCR	R/W	H'FE92 8050	32
VEU2 resize filter control register	V2RFCR	R/W	H'FE92 8054	32
VEU2 resize filter size clip register	V2RFSR	R/W	H'FE92 8058	32
VEU2 enhance register	VE2NHR	R/W	H'FE92 805C	32
VEU2 resize filter sub control register	V2RSCR	R/W	H'FE92 8064	32
VEU2 resize filter size clip offset register	V2RSOR	R/W	H'FE92 8068	32
VEU2 filter mode control register	V2FMCR	R/W	H'FE92 8070	32
VEU2 vertical tap coefficient register	V2VTCR	R/W	H'FE92 8074	32
VEU2 horizontal tap coefficient register	V2HTCR	R/W	H'FE92 8078	32
VEU2 designated color register	V2APCR	R/W	H'FE92 8080	32
VEU2 conversion color register	VE2CCR	R/W	H'FE92 8084	32
VEU2 fill color specification register	V2FLCR	RW	H'FE92 8088	32
VEU2 address fixed register	V2AFXR	R/W	H'FE92 8090	32
VEU2 swapping register	V2SWPR	R/W	H'FE92 8094	32
VEU2 event interrupt enable register	VE2IER	R/W	H'FE92 80A0	32
VEU2 event register	VE2VTR	R/W	H'FE92 80A4	32
VEU2 status register	V2STAR	R	H'FE92 80B0	32
VEU2 module reset register	V2BSRR	R/W	H'FE92 80B4	32
VEU2 resize passband register	V2RPBR	R/W	H'FE92 80C8	32
VEU2 resize interpolation setting register	VEUAD2_RSZ_ITP	R/W	H'FE92 8180	32
VEU2 horizontal FIR filter coefficient Y/G pixel setting 0	VEUAD2_FCOE_HY0	R/W	H'FE92 8200	32

Register Name	Abbr.	R/W	Address	Access Size
VEU2 horizontal FIR filter coefficient Y/G pixel setting 1	VEUAD2_FCOE_HY1	R/W	H'FE92 8204	32
VEU2 horizontal FIR filter coefficient Y/G pixel setting 2	VEUAD2_FCOE_HY2	R/W	H'FE92 8208	32
VEU2 horizontal FIR filter coefficient Cb/B pixel setting 0	VEUAD2_FCOE_HCB0	R/W	H'FE92 8210	32
VEU2 horizontal FIR filter coefficient Cb/B pixel setting 1	VEUAD2_FCOE_HCB1	R/W	H'FE92 8214	32
VEU2 horizontal FIR filter coefficient Cb/B pixel setting 2	VEUAD2_FCOE_HCB2	R/W	H'FE92 8218	32
VEU2 horizontal FIR filter coefficient Cr/R pixel setting 0	VEUAD2_FCOE_HCR0	R/W	H'FE92 8220	32
VEU2 horizontal FIR filter coefficient Cr/R pixel setting 1	VEUAD2_FCOE_HCR1	R/W	H'FE92 8224	32
VEU2 horizontal FIR filter coefficient Cr/R pixel setting 2	VEUAD2_FCOE_HCR2	R/W	H'FE92 8228	32
VEU2 vertical FIR filter coefficient Y/G pixel setting 0	VEUAD2_FCOE_VY0	R/W	H'FE92 8230	32
VEU2 vertical FIR filter coefficient Y/G pixel setting 1	VEUAD2_FCOE_VY1	R/W	H'FE92 8234	32
VEU2 vertical FIR filter coefficient Y/G pixel setting 2	VEUAD2_FCOE_VY2	R/W	H'FE92 8238	32
VEU2 vertical FIR filter coefficient Cb/B pixel setting 0	VEUAD2_FCOE_VCB0	R/W	H'FE92 8240	32
VEU2 vertical FIR filter coefficient Cb/B pixel setting 1	VEUAD2_FCOE_VCB1	R/W	H'FE92 8244	32
VEU2 vertical FIR filter coefficient Cb/B pixel setting 2	VEUAD2_FCOE_VCB2	R/W	H'FE92 8248	32
VEU2 vertical FIR filter coefficient Cr/R pixel setting 0	VEUAD2_FCOE_VCR0	R/W	H'FE92 8250	32
VEU2 vertical FIR filter coefficient Cr/R pixel setting 1	VEUAD2_FCOE_VCR1	R/W	H'FE92 8254	32
VEU2 vertical FIR filter coefficient Cr/R pixel setting 2	VEUAD2_FCOE_VCR2	R/W	H'FE92 8258	32
VEU2 FIR filter calculation optional setting register	VEUAD2_FCOE_FSWT	R/W	H'FE92 8260	32
VEU2 alpha resize clip threshold setting register	VEUAD2_ALPTH	R/W	H'FE92 8300	32

Register Name	Abbr.	R/W	Address	Access Size
VEU2 resize clip value setting register	VEUAD2_ALPVAL	R/W	H'FE92 8304	32

Register Name	Abbr.	R/W	Address	Access Size
VEU3 start register	VE3STR	R/W	H'FE92 C000	32
VEU3 source memory width register	VE3SWR	R/W	H'FE92 C010	32
VEU3 source size register	VE3SSR	R/W	H'FE92 C014	32
VEU3 source address Y register	V3SAYR	R/W	H'FE92 C018	32
VEU3 source address C register	V3SACR	R/W	H'FE92 C01C	32
VEU3 bundle source size register	V3BSSR	R/W	H'FE92 C020	32
VEU3 destination memory width register	VE3DWR	R/W	H'FE92 C030	32
VEU3 destination address Y register	V3DAYR	R/W	H'FE92 C034	32
VEU3 destination address C register	V3DACR	R/W	H'FE92 C038	32
VEU3 transform control register	V3TRCR	R/W	H'FE92 C050	32
VEU3 resize filter control register	V3RFCR	R/W	H'FE92 C054	32
VEU3 resize filter size clip register	V3RFSR	R/W	H'FE92 C058	32
VEU3 enhance register	VE3NHR	R/W	H'FE92 C05C	32
VEU3 resize filter sub control register	V3RSCR	R/W	H'FE92 C064	32
VEU3 resize filter size clip offset register	V3RSOR	R/W	H'FE92 C068	32
VEU3 filter mode control register	V3FMCR	R/W	H'FE92 C070	32
VEU3 vertical tap coefficient register	V3VTCR	R/W	H'FE92 C074	32
VEU3 horizontal tap coefficient register	V3HTCR	R/W	H'FE92 C078	32
VEU3 designated color register	V3APCR	R/W	H'FE92 C080	32
VEU3 conversion color register	VE3CCR	R/W	H'FE92 C084	32
VEU3 fill color specification register	V3FLCR	RW	H'FE92 C088	32
VEU3 address fixed register	V3AFXR	R/W	H'FE92 C090	32
VEU3 swapping register	V3SWPR	R/W	H'FE92 C094	32
VEU3 event interrupt enable register	VE3IER	R/W	H'FE92 C0A0	32
VEU3 event register	VE3VTR	R/W	H'FE92 C0A4	32
VEU3 status register	V3STAR	R	H'FE92 C0B0	32
VEU3 module reset register	V3BSRR	R/W	H'FE92 C0B4	32
VEU3 resize passband register	V3RPBR	R/W	H'FE92 C0C8	32
VEU3 resize interpolation setting register	VEUAD3_RSZ_ITP	R/W	H'FE92 C180	32
VEU3 horizontal FIR filter coefficient Y/G pixel setting 0	VEUAD3_FCOE_HY0	R/W	H'FE92 C200	32

Register Name	Abbr.	R/W	Address	Access Size
VEU3 horizontal FIR filter coefficient Y/G pixel setting 1	VEUAD3_FCOE_HY1	R/W	H'FE92 C204	32
VEU3 horizontal FIR filter coefficient Y/G pixel setting 2	VEUAD3_FCOE_HY2	R/W	H'FE92 C208	32
VEU3 horizontal FIR filter coefficient Cb/B pixel setting 0	VEUAD3_FCOE_HCB0	R/W	H'FE92 C210	32
VEU3 horizontal FIR filter coefficient Cb/B pixel setting 1	VEUAD3_FCOE_HCB1	R/W	H'FE92 C214	32
VEU3 horizontal FIR filter coefficient Cb/B pixel setting 2	VEUAD3_FCOE_HCB2	R/W	H'FE92 C218	32
VEU3 horizontal FIR filter coefficient Cr/R pixel setting 0	VEUAD3_FCOE_HCR0	R/W	H'FE92 C220	32
VEU3 horizontal FIR filter coefficient Cr/R pixel setting 1	VEUAD3_FCOE_HCR1	R/W	H'FE92 C224	32
VEU3 horizontal FIR filter coefficient Cr/R pixel setting 2	VEUAD3_FCOE_HCR2	R/W	H'FE92 C228	32
VEU3 vertical FIR filter coefficient Y/G pixel setting 0	VEUAD3_FCOE_VY0	R/W	H'FE92 C230	32
VEU3 vertical FIR filter coefficient Y/G pixel setting 1	VEUAD3_FCOE_VY1	R/W	H'FE92 C234	32
VEU3 vertical FIR filter coefficient Y/G pixel setting 2	VEUAD3_FCOE_VY2	R/W	H'FE92 C238	32
VEU3 vertical FIR filter coefficient Cb/B pixel setting 0	VEUAD3_FCOE_VCB0	R/W	H'FE92 C240	32
VEU3 vertical FIR filter coefficient Cb/B pixel setting 1	VEUAD3_FCOE_VCB1	R/W	H'FE92 C244	32
VEU3 vertical FIR filter coefficient Cb/B pixel setting 2	VEUAD3_FCOE_VCB2	R/W	H'FE92 C248	32
VEU3 vertical FIR filter coefficient Cr/R pixel setting 0	VEUAD3_FCOE_VCR0	R/W	H'FE92 C250	32
VEU3 vertical FIR filter coefficient Cr/R pixel setting 1	VEUAD3_FCOE_VCR1	R/W	H'FE92 C254	32
VEU3 vertical FIR filter coefficient Cr/R pixel setting 2	VEUAD3_FCOE_VCR2	R/W	H'FE92 C258	32
VEU3 FIR filter calculation optional setting register	VEUAD3_FCOE_FSWT	R/W	H'FE92 C260	32
VEU3 alpha resize clip threshold setting register	VEUAD3_ALPTH	R/W	H'FE92 C300	32

Register Name	Abbr.	R/W	Address	Access Size
VEU3 resize clip value setting register	VEUAD3_ALPVAL	R/W	H'FE92 C304	32

Table 35.4 VEU Register States in Each Processing Mode

Register Abbreviation	Reset *	Module Standby
VEnSTR	Initialized	Retained
VEnSWR	Initialized	Retained
VEnSSR	Initialized	Retained
VnSAYR	Initialized	Retained
VnSACR	Initialized	Retained
VnBSSR	Initialized	Retained
VEnDWR	Initialized	Retained
VnDAYR	Initialized	Retained
VnDACR	Initialized	Retained
VnTRCR	Initialized	Retained
VnRFCR	Initialized	Retained
VnRFSR	Initialized	Retained
VEnNHR	Initialized	Retained
VnFMCR	Initialized	Retained
VnVTCR	Initialized	Retained
VnHTCR	Initialized	Retained
VnAPCR	Initialized	Retained
VEnCCR	Initialized	Retained
VnFLCR	Initialized	Retained
VnAFXR	Initialized	Retained
VnSWPR	Initialized	Retained
VEnIER	Initialized	Retained
VEnVTR	Initialized	Retained
VnSTAR	Initialized	Retained
VnBSRR	Initialized	Retained
VnRPBR	Initialized	Retained
VEUADm_RSZ_ITP	Initialized	Retained
VEUADm_FCOE_HY0	Initialized	Retained
VEUADm_FCOE_HY1	Initialized	Retained

Register Abbreviation	Reset *	Module Standby
VEUADm_FCOE_HY2	Initialized	Retained
VEUADm_FCOE_HCB0	Initialized	Retained
VEUADm_FCOE_HCB1	Initialized	Retained
VEUADm_FCOE_HCB2	Initialized	Retained
VEUADm_FCOE_HCR0	Initialized	Retained
VEUADm_FCOE_HCR1	Initialized	Retained
VEUADm_FCOE_HCR2	Initialized	Retained
VEUADm_FCOE_VY0	Initialized	Retained
VEUADm_FCOE_VY1	Initialized	Retained
VEUADm_FCOE_VY2	Initialized	Retained
VEUADm_FCOE_VCB0	Initialized	Retained
VEUADm_FCOE_VCB1	Initialized	Retained
VEUADm_FCOE_VCB2	Initialized	Retained
VEUADm_FCOE_VCR0	Initialized	Retained
VEUADm_FCOE_VCR1	Initialized	Retained
VEUADm_FCOE_VCR2	Initialized	Retained
VEUADm_FCOE_FSWT	Initialized	Retained
VEUADm_ALPTH	Initialized	Retained
VEUADm_ALPVAL	Initialized	Retained

Note: n = 3 to 0

Note: m = 3 to 2

* For details, refer to section 1-D Overview of reset

35.3.1 VEU Start Register (VESTR)

VESTR controls activation of the VEU and software reset of VEU processing. Before starting VEU processing by VESTR, all registers related to the VEU must be set.

Writing 1 to read-only bits is prohibited. If 1 is written to any of these bits, a malfunction may occur.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	VBE	—	—	—	—	—	—	—	VE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	VBE	0	R/W	Sets the bundle read mode (N-line read mode). In bundle read mode (N-line read mode), the VEU divides a one-frame image at the number of lines set by VBSSR and reads data for that number of lines. When the VEU is activated in bundle read mode (N-line read mode), rotation processing, deblocking filter processing, low-pass filter processing, and median filter processing cannot be executed (horizontal inversion, vertical inversion, and horizontal-vertical inversion are possible). 0: Normal operation 1: Bundle read (N-line read) mode
7 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
0	VE	0	R/W	Controls the VEU processing start and software reset of processing (processing halt). If this bit is set to 1 when the VEU is halted, the VEU starts processing images in the memory according to the register settings, and this bit is read as 1. In addition, if 0 is written to this bit when it is 1, the current VEU processing is immediately terminated. The end of software reset processing can be confirmed when this bit becomes 0 after a software reset has been issued to the VEU. Confirm that this bit is 0 before restarting the VEU after a software reset. 0: NOP (software reset processing when 0 is written to this bit when it is 1) 1: VEU processing starts

If B'1 is written to the VE bit when the VBE bit is B'1 at VEU activation, bundle read mode (N-line read mode) is selected. In bundle read mode, data is read from two memory areas alternately for the number of lines set by the VBSS bits in VBSSR. If reading for the entire frame is not finished when the VEU has completed reading for the number of lines set by VBSSR, a bundle end interrupt (VEVTR.VBEND) occurs and the VEU waits for reading to be restarted. To restart reading, first clear the bundle end interrupt source, and then write B'1 to the VE bit again (write with the VBE bit still set to B'1). After repeating this until reading for the entire frame finishes, a one-frame end interrupt (VEVTR.VEEND) occurs. The image of processing in bundle read mode is shown in figure 35.5. The status of normal image processing, read processing in bundle read mode, and waiting of read to be restarted in bundle read mode can be confirmed by reading VSTAR.

Notes on software reset:

1. Though the VEU end interrupt flag (VEVTR.VEEND) may become B'1 depending on the timing to issue a VEU software reset, the processed image of the frame in which a software reset was issued is not guaranteed.
2. Even when the VEEND flag does not become B'1 after a VEU software reset, the VEEND flag must always be cleared to B'0.
3. When issuing a software reset in bundle read mode, issue it before reading is restarted subsequent to a bundle end interrupt.

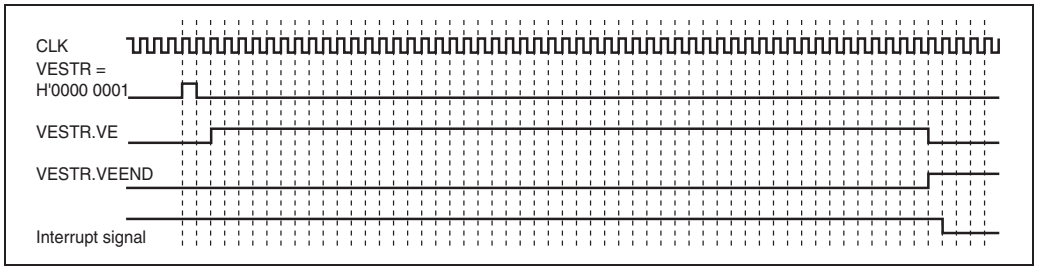


Figure 35.3 Operation Timing of VE Bit and Each Status

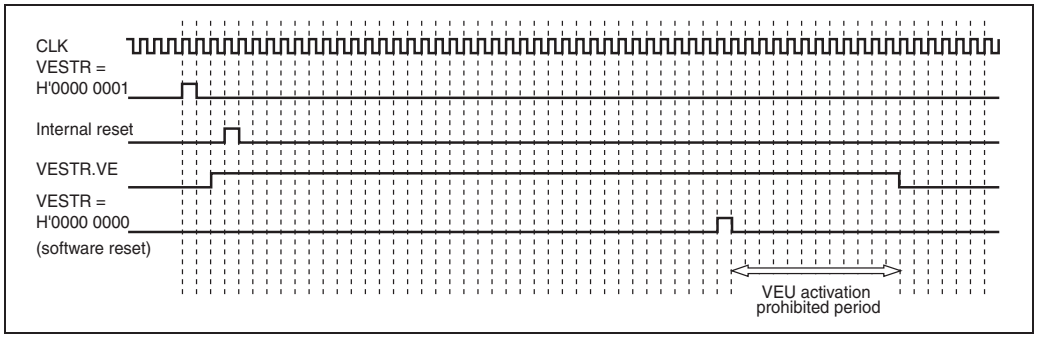


Figure 35.4 Operation Timing of Software Reset and Each Status

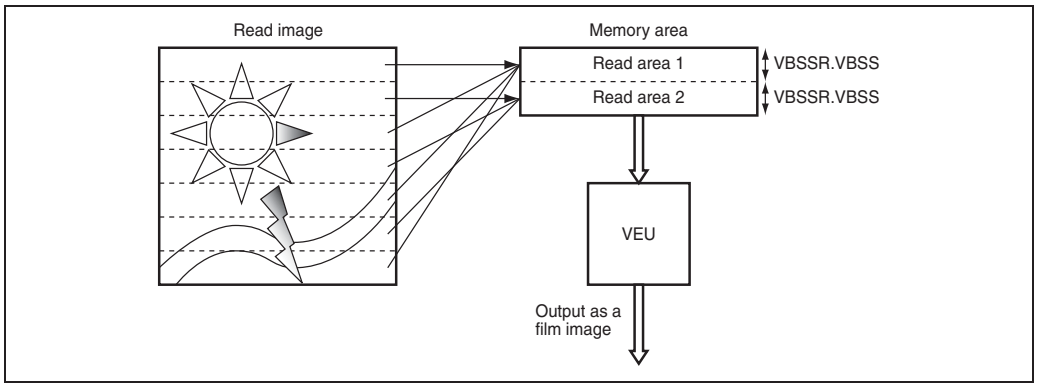


Figure 35.5 Image of Bundle Read Mode Processing

35.3.2 VEU Source Memory Width Register (VESWR)

VESWR sets the memory width of the source memory area of the VEU.

Modifying this register during operation is prohibited.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VSW[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 2 1, 0	VSW[15:2] VSW[1:0]	H'0000	R/W R	These bits set the width of the source memory area of the VEU (4-pixel units). This setting should be made in 2-pixel units when the RPKF bits in VTRCR are set to 0,1,3,7, or 13.

In the VSW bits, set the horizontal width of the source memory area where the source image is located in the VEU processing as a number of bytes. This setting must be made in byte units that correspond to four pixels of the source image. If the read image is in the YCbCr format, make a setting matching the Y component. For reading data in the YCbCr 4:2:0, YCbCr 4:2:2, and YCbCr 4:4:4 formats, the VSW setting, VSW setting, and (VSW setting × 2) are applied respectively to the horizontal width of the source memory area for the C component. When the RPKF bits in VTRCR are set to 0,1,3,7, or 13 (RGB 2 bytes/pixel or RGB 4 bytes/pixel), a setting in byte units that corresponds to two pixels of the source image is possible. As shown in (A) in figure 35.6, when an image is clipped from the memory area, the right-end address of a line's image is discontinuous from the left-end address of the next line's image. Compared to this, (B) in figure 35.6 shows an example where the horizontal size of an image input to the VEU matches the horizontal length of the memory. In this case, the right-end address of a line's image and the left-end address of the next line's image have continuous values.

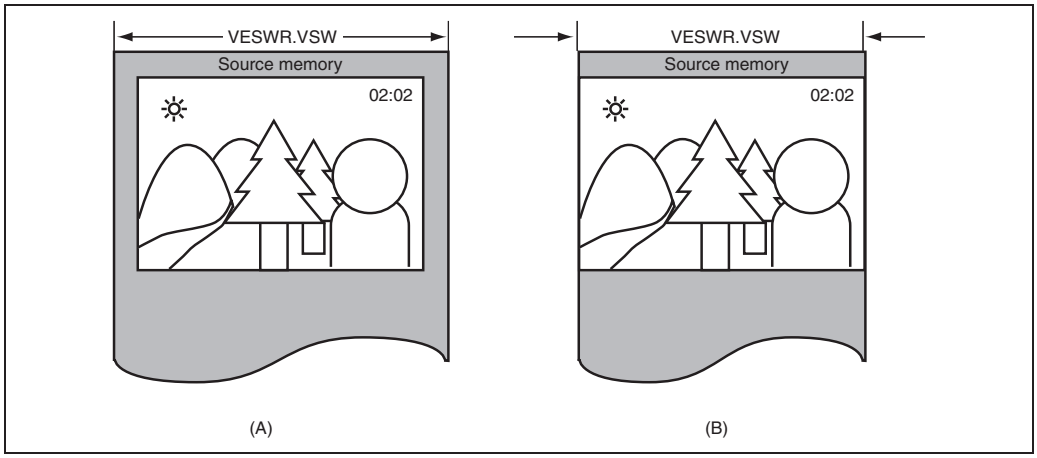


Figure 35.6 Relationship between Image Clipping Size and VESWR

35.3.3 VEU Source Size Register (VESSR)

VESSR sets the vertical and horizontal sizes (number of pixels) of the image read by the VEU.

Modifying this register during operation is prohibited.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	VVSS[11:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	VHSS[11:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
27 to 16 (28 to 16)	VVSS[11:0]	H'000	R/W	These bits set the number of vertical pixels read by the VEU. Set the number of vertical read pixels of the source image read by the VEU in these bits (see figure 35.7). • Scale-up/down, enhancer, or bundle read is not performed (see figure 35.7): A setting in 2-pixel units is possible for the following cases: Reading and writing are both in RGB format. RPKF bit in VTRCR is either 3 (RGB 2 bytes/pixel), 0, 1, 7, 13 (RGB 4 bytes/pixel) and WPKF bit in VTRCR is either 1, 2, 6 (RGB 2 bytes/pixel), 14, 19, 20, 22, 23 (RGB 4 bytes/pixel). Other than those settings, specify a setting in 4-pixel units. • Scale-up/down, enhancer, or bundle read is performed, a setting in 1-pixel unit is possible (see figure 35.7). However, the data should be allocated in the memory to specify 2-pixel units when the input format is YCbCr4:2:0. The maximum value to be set is 4092 pixels.

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 0 (12~0)	VHSS[11:0]	H'000	R/W	These bits set the number of horizontal pixels read by the VEU. Set the number of horizontal read pixels of the source image read by the VEU in these bits (see figure 35.7). • Scale-up/down, enhancer, or bundle read is not performed (see figure 35.7): A setting in 2-pixel units is possible for the following cases: Reading and writing are both in RGB format. RPKF bit in VTRCR is either 3 (RGB 2 bytes/pixel), 0, 1, 7, 13 (RGB 4 bytes/pixel) and WPKF bit in VTRCR is either 1, 2, 6 (RGB 2 bytes/pixel), 14, 19, 20, 22, 23 (RGB 4 bytes/pixel). Other than those settings, specify a setting in 4-pixel units. • Scale-up/down, enhancer, or bundle read is performed, a setting in 1-pixel unit is possible (see figure 35.7). However, set in the VESWR.VSW[15:0] a value (a value that VHSS[11:0] specify in 4-pixel units) × 4 / (P_density_y in use format) or more. Further, the data should be allocated in the memory to specify in 2-pixel units when the input format is YCbCr4:2:0 and YCbCr4:2:2. The maximum value to be set is 4092 pixels.

Note: When resizing it, it can be assumed the horizontal 8188 or less and it is vertical 8188 or less (Only VEU2 and VEU3). However, it is necessary to do the ratio and the output setting for the output size not to exceed the horizontal 4092 and vertical 8188 in that case. (example, VESSR.VHSS=8188→VRFCR.VHMNT=2, VRFCR.VHFRC=4, VRSOR.VHCLOFS=0, and VRFSR.VHCLP=4092)

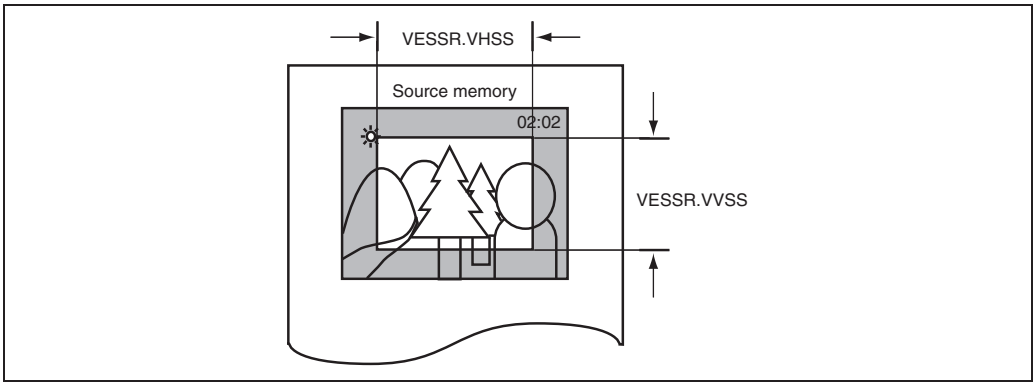


Figure 35.7 Relationship between Read Size and VESSR

35.3.4 VEU Source Address Y Register (VSAYR)

VSAYR sets the start address for the Y/RGB plane of the image read by the VEU.

Modifying this register during operation is prohibited. However, this register can be modified in the restart wait state (when VSTAR = H'0000 1001) in N-line read mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VSAY[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VSAY[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	VSAY[31:2]	H'0000 0000	R/W	These bits set the start address for reading the Y/RGB plane by the VEU (longword units).
1, 0	VSAY[1:0]		R	

Set the start address for the Y/RGB plane of the source image of the VEU in the VSAY bits, as shown in figure 35.8. When reading a YCbCr image, specify the start address of the Y plane. When reading an RGB image, specify the start address (top-left address in the read image area) of the RGB plane. Figure 35.8 shows the input format for the Y plane of the YCbCr format. For the input format of the RGB format, refer to table 35.8.

Note: In bundle read mode, set two addresses alternately for each VEVTR.VBEND interrupt.

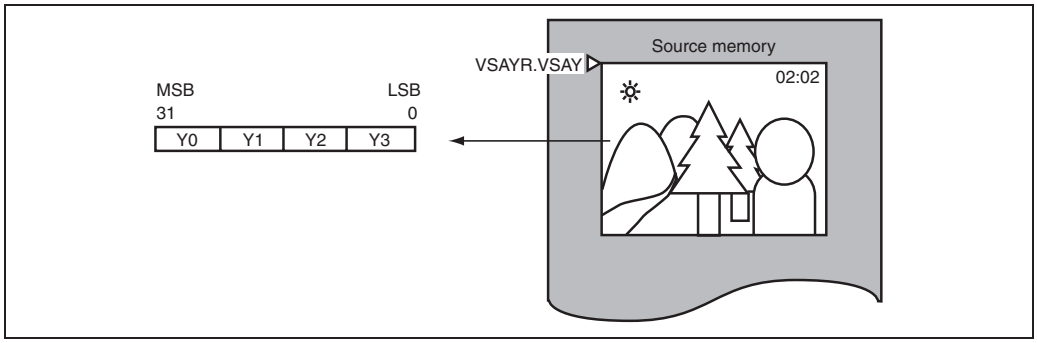


Figure 35.8 Address Set in VSAYR and Y-Plane Format

35.3.5 VEU Source Address C Register (VSACR)

VSACR sets the start address for the C plane of the image read by the VEU.

Modifying this register during operation is prohibited. However, this register can be modified in the restart wait state (when VSTAR = H'0000 1001) in N-line read mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VSAC[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VSAC[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 2 1, 0	VSAC[31:2] VSAC[1:0]	H'0000 0000	R/W R	These bits set the start address for reading the C plane by the VEU. (1-longword units. 2-longword units for the YCbCr 4:4:4 format.)

Set the start address for the C plane of the source image of the VEU in the VSAC bits, as shown in figure 35.9. When reading a YCbCr image, specify the start address (top-left address in the read image area) of the C plane. Figure 35.9 shows the input format for the C plane. When reading an RGB image, VSACR is not used. VSACR should be set in 1-longword units for the YCbCr 4:2:0 or YCbCr 4:2:2 format, and in 2-longword units for the YCbCr 4:4:4 format.

Note: In bundle read mode, set two addresses alternately for each VEVTR.VBEND interrupt.

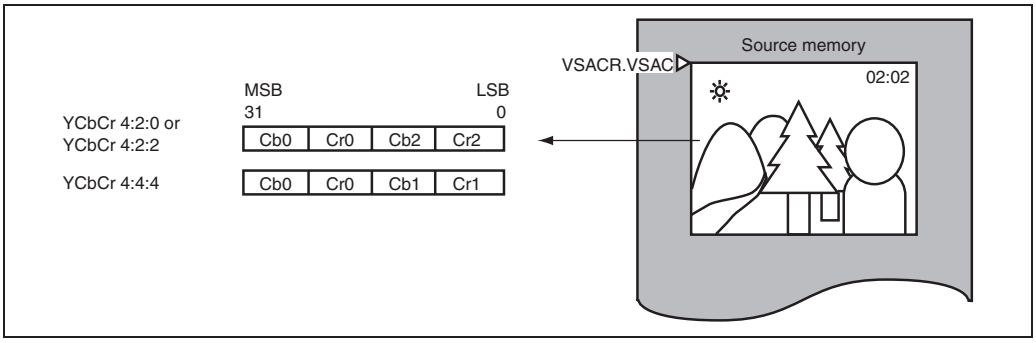


Figure 35.9 Address Set in VSACR and C-Plane Format

35.3.6 VEU Bundle Source Size Register (VBSSR)

VBSSR sets the number of lines (number of pixels) to be read when the VEU is activated once in bundle read mode (N-line read mode). VBSSR needs to be set only in bundle read mode.

Modifying this register during operation is prohibited.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	VBSS[11:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 3 2, 0	VBSS[11:3] VBSS[2:0]	H'000	R/W R	These bits set the number of lines to be read when the VEU is activated once in bundle read mode (N-line read mode) (8-line units).

Set the number of lines of the source image to be read by the VEU in one processing in bundle read mode in the VBSS bits. The VBSS bits should be set in 8-line units, and the maximum value to be set is 960 lines.

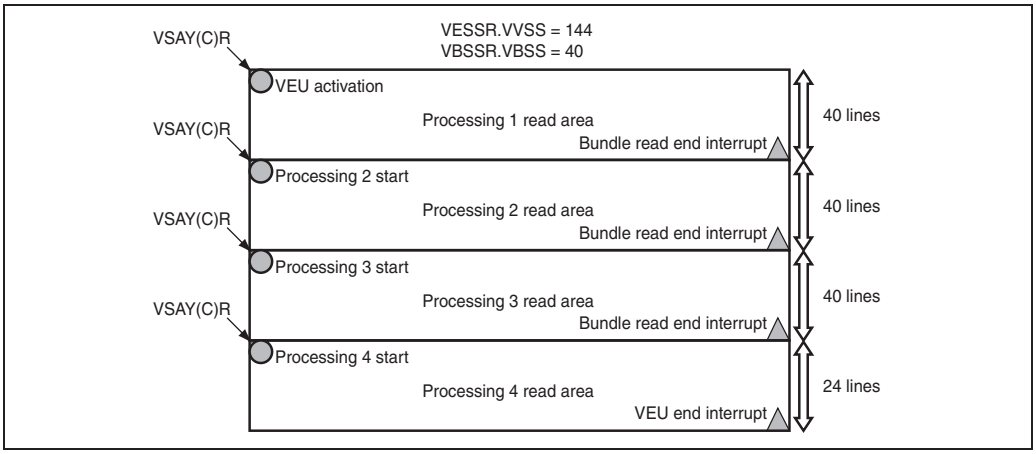


Figure 35.10 Relationship between Read Image in Bundle Read Mode and Read Image in Each Processing

35.3.7 VEU Destination Memory Width Register (VEDWR)

VEDWR sets the memory width of the destination memory area of the VEU.

Modifying this register during operation is prohibited.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VDW[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 2	VDW[15:2]	H'0000	R/W	These bits set the width of the destination memory area of the VEU (longword units).
1, 0	VDW[1:0]		R	

Set the horizontal width of the destination memory area where the destination image is located as a number of bytes in the VDW bits. This setting must be made in byte units that correspond to four pixels of the destination image. If the drawing image is in the YCbCr format, make a setting matching the Y component. For writing data in the YCbCr 4:2:0, YCbCr 4:2:2, and YCbCr 4:4:4 formats, the VDW setting, VDW setting, and (VDW setting × 2) are applied respectively to the horizontal width of the destination memory area for the C component. When the WPKF bits in VTRCR are set to 1, 2, 6 (RGB 2 bytes/pixel), 8 to 14, 19, 20, 22, 23 (RGB 4 bytes/pixel), a setting in byte units that corresponds to two pixels of the destination image is possible. As shown in (A) in figure 35.11, when an image is pasted to the back display or the like in the memory area, the right-end address of a line's image is discontinuous from the left-end address of the next line's image. Compared to this, (B) in figure 35.11 shows an example where the horizontal size of an image output from the VEU matches the horizontal length of the memory. In this case, the right-end address of a line's image and the left-end address of the next line's image have continuous values.

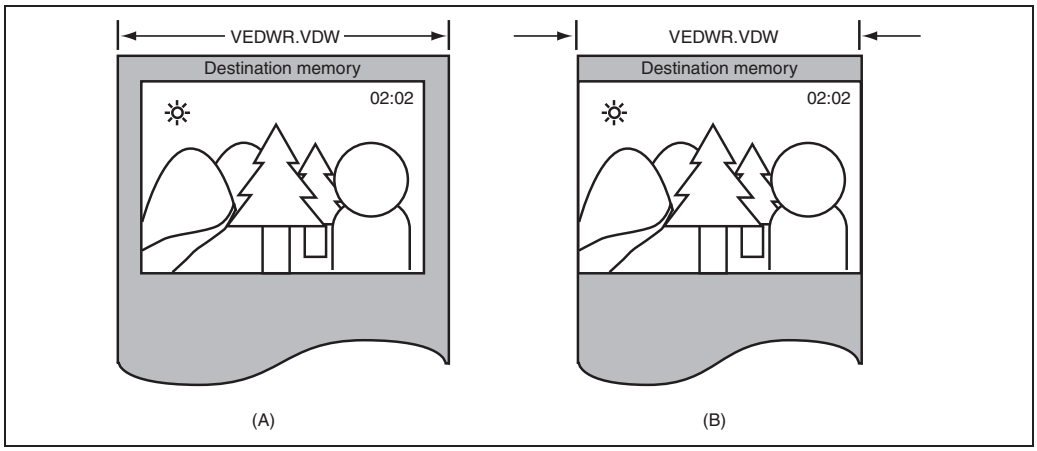


Figure 35.11 Relationship between Image Pasting Size and VEDWR

35.3.8 VEU Destination Address Y Register (VDAYR)

VDAYR sets the start address for the Y/RGB plane of the image drawn by the VEU.

Modifying this register during operation is prohibited.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VDAY[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VDAY[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	VDAY[31:2]	H'0000 0000	R/W	These bits set the start address for drawing the Y/RGB plane by the VEU (longword units).
1, 0	VDAY[1:0]		R	

Set the start address of the destination image (top-left address in the destination image area) of the VEU in the VDAY bits, as shown in figure 35.12. When drawing a YCbCr image, specify the start address of the Y plane. When drawing an RGB image, specify the start address of the RGB plane.

When VTRCR.WPKF = 6 (RGB 16-bpp), a setting in word units is possible.

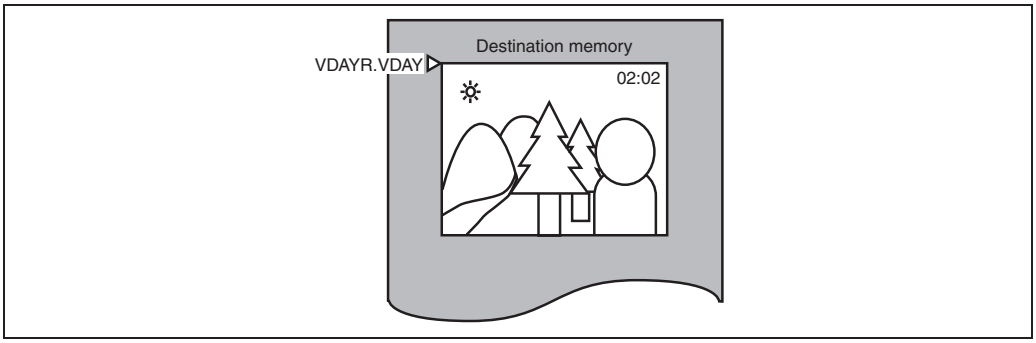


Figure 35.12 Address Set in VDAYR

The point specified as the address to be set in VDAYR changes when the image is rotated or inverted. This specification point of the address for each processing is shown in table 35.5. Figure 35.13 illustrates the address specification point in block processing, and figure 35.14 illustrates that in line processing. The gray quadrangle is assumed as the destination image and the ☆ marks as the address specification points.

The address specification point if neither scale-up/down, enhancer, bundle read, nor VFMCR.FLTPI = 0 is performed is the top-left address for the block located in one of the four corners with the destination image divided into blocks of 16 × 16 pixels. In a case that scale-up/down, enhance, and bundle read are not used and even FLTPI = 0, or either scale-up/down, enhance, or bundle read is used, each address specification point becomes one of the four corners in the destination image.

Table 35.5 Address Specification Point for Setting VDAYR

	No Rotation/ Inversion	90° Rotation	270° Rotation	90° Rotation + Horizontal Inversion	90° Rotation + Vertical Inversion	Horizontal Inversion	Vertical Inversion	Horizontal Inversion + Vertical Inversion
Block processing: No scale-up/down, enhancer, or bundle read and even FLTPI = 0.	—	D	E	F	G	A	B	C
Line processing: Scale-up/down, enhancer, or bundle read performed and even VFMCR.FLTPI = 1.	—	×	×	×	×	H	J	K

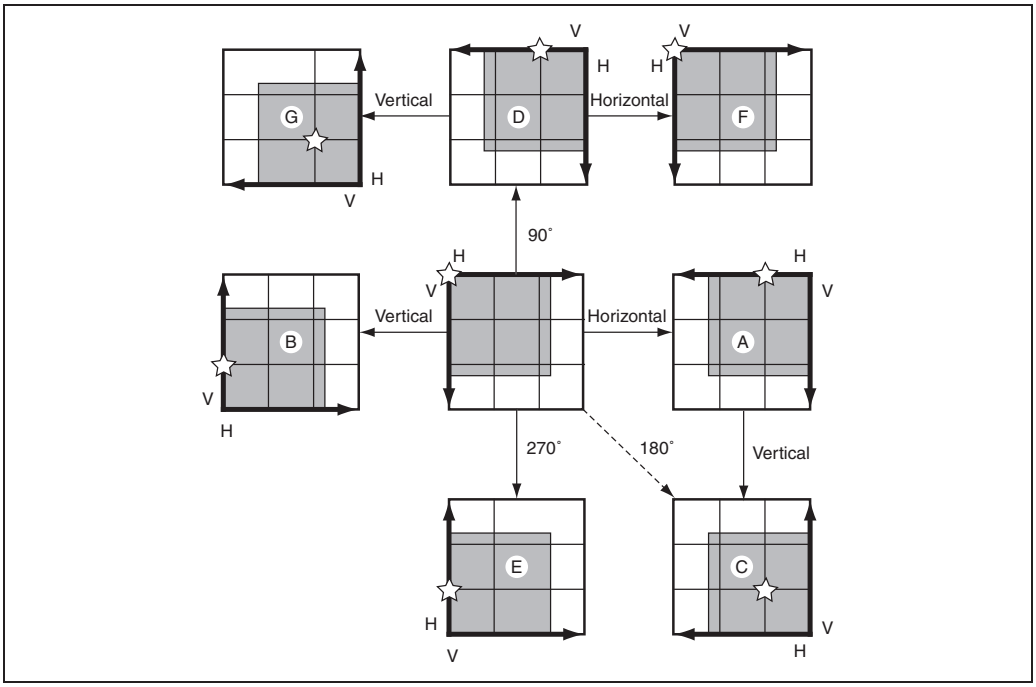


Figure 35.13 Location of Address Specification Point for VDAYR (Block Processing)

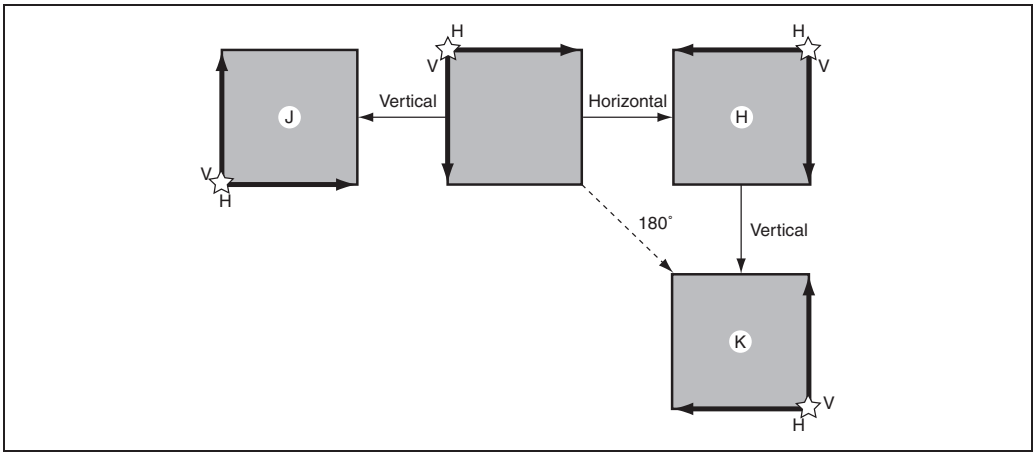


Figure 35.14 Location of Address Specification Point for VDAYR (Line Processing)

When drawing a YCbCr image, specify an address of the Y plane. When drawing an RGB image, specify an address of the RGB plane.

The formulas for setting the addresses are shown below.

Offset_ad	Becomes the address location of the top-left corner in the destination image	
yuv420out	Drawing format is YCbCr 4:2:0	1: VTRCR. CHDS = 0 0: VTRCR. CHDS = 1 or 2
clip_hsize	Horizontal size of line processing output	VRFSR.VHCLP
clip_vsize	Vertical size of line processing output	VRFSR.VVCLP
clip_vsize_c	Vertical size (C) of line processing output	(clip_vsize + 1)/2: VTRCR. CHDS = 0 (round-down) clip_vsize: VTRCR. CHDS = 1 or 2
dest_width	Destination memory width	VEDWR.VEW
dest_width_c	Destination memory width (C)	dest_width: VTRCR.CHDS = 2 dest_width × 2: VTRCR.CHDS = 2
src_hblk	Horizontal block count	VESSR.VHSS/16 (round-up)
src_vblk	Vertical block count	VESSR.VVSS/16 (round-up)
src_sideh	Horizontal size of right-end block	(VESSR.VHSS + 15)%16 + 1
src_sidev	Vertical size of bottom-end block	(VESSR.VHSS + 15)%16 + 1
< >	Operator changing a negative value to 0	0 when the value in < > is 0 or lower, otherwise the value in < >

For P_density_y of an RGB output, see table 27.6. For P_density_y and P_density_c of a YCbCr output, see table 35.7.

[Address for Y component output]

0 VDAYR = offset_ad

F VDAYR = offset_ad

D VDAYR = offset_ad + <((src_vblk – 2) × 16 + src_sidev)> × (4/P_density_y)

A VDAYR = offset_ad + <((src_hblk – 2) × 16 + src_sideh)> × (4/P_density_y)

E VDAYR = offset_ad + <((src_hblk – 2) × 16 + src_sideh)> × dest_width

B VDAYR = offset_ad + <((src_vblk – 2) × 16 + src_sidev)> × dest_width

G VDAYR = offset_ad + <((src_hblk – 2) × 16 + src_sideh)> × dest_width + <((src_vblk – 2) × 16 + src_sidev)> × (4/P_density_y)

C VDAYR = offset_ad + <((src_vblk – 2) × 16 + src_sidev)> × dest_width + <((src_hblk – 2) × 16 + src_sideh)> × (4/P_density_y)

H VDAYR = offset_ad + clip_hsize × (4/P_density_y)

J VDAYR = offset_ad + (clip_vsize – 1) × dest_width

K VDAYR = offset_ad + (clip_vsize – 1) × dest_width + clip_hsize × (4/P_density_y)

[Address for C component output]

0 VDACR = offset_ad

F VDACR = offset_ad

D VDACR = offset_ad + <((src_vblk – 2) × 16 + src_sidev)> × (4/P_density_c)

A VDACR = offset_ad + <((src_hblk – 2) × 16 + src_sideh)> × (4/P_density_c)

E VDACR = offset_ad + <((src_hblk – 2) × 16 + src_sideh)>/(1 + yuv420out) × dest_width_c

B VDACR = offset_ad + <((src_vblk – 2) × 16 + src_sidev)>/(1 + yuv420out) × dest_width_c

G VDACR = offset_ad + <((src_hblk – 2) × 16 + src_sideh)>/(1 + yuv420out) × dest_width_c + <((src_vblk – 2) × 16 + src_sidev)> × (4/P_density_c)

C VDACR = offset_ad + <((src_vblk – 2) × 16 + src_sidev)>/(1 + yuv420out) × dest_width_c + <((src_hblk – 2) × 16 + src_sideh)> × (4/P_density_c)

H VDACR = offset_ad + clip_hsize × (4/P_density_c)

J VDACR = offset_ad + (clip_vsize_c – 1) × dest_width_c

K VDACR = offset_ad + (clip_vsize_c – 1) × dest_width_c + clip_hsize × (4/P_density_c)

35.3.9 VEU Destination Address C Register (VDACR)

VDACR specifies the start address for the C plane of the image drawn by the VEU.

Modifying this register during operation is prohibited.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VDAC[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VDAC[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	VDAC[31:2]	H'0000 0000	R/W	These bits set the start address for drawing the C plane by the VEU. (1-longword units. 2-longword units for the YCbCr 4:4:4 format.)
1, 0	VDAC[1:0]		R	

Set the start address of the destination image (top-left address in the destination image area) of the VEU in the VDAC bits, as shown in figure 35.15. When drawing a YCbCr image, specify the start address of the C plane. When reading an RGB image, VDACR is not used.

The point specified as the address to be set in VDACR changes when the image is rotated or inverted. As this specification point is similar to that for VDAYR, see figure 35.13 and table 35.5 for details. However, when an image is drawn in the YCbCr 4:2:0 format, the number of lines output in the vertical direction for the C component is half of the number of lines for the Y component or an RGB output. When calculating the address in the vertical direction (memory width × number of vertical lines), take notice that the number of lines will become half. (See the description in section 35.3.8, VEU Destination Address Y Register (VDAYR).)

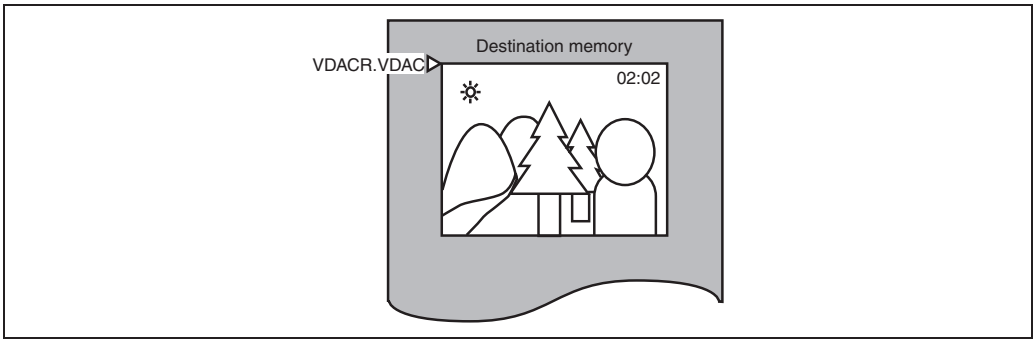


Figure 35.15 Address Set in VDACR

35.3.10 VEU Transform Control Register (VTRCR)

VTRCR mainly sets the processing contents related to color conversion by the VEU and the input/output data format.

Writing 1 to read-only bits is prohibited. If 1 is written to any of these bits, a malfunction may occur. Modifying this register during operation is prohibited.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PAD[7:0]								CHDS[1:0]		WPKFR	WPKF[4:0]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CHRR[1:0]				RPKF[3:0]							DITH	TM2	TM1	TE	RY
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	PAD[7:0]	H'00	R/W	These bits set the PAD value to be stuffed into the output data when the VEU output data is in the RGB format. Some forms of RGB output data packs (see table 35.6) include a PAD field as shown in figure 35.16. In the PAD field, any 8-bit data can be added. Specify the value to be added to the PAD field to these bits.*
23, 22	CHDS[1:0]	00	R/W	These bits select the output format when the VEU output data is in the YCbCr format. For the YCbCr format, data is output in one of the pack patterns shown in table 35.7. Conversion from YCbCr 4:4:4 to YCbCr 4:2:2 or YCbCr 4:2:0 is performed by taking the average of two pixels for the horizontal direction, and simply skipping pixels for the vertical direction. The planes for outputting the Y and C data to memory are separate. Therefore, the ratio of the Y:C memory areas is 2:1 for YCbCr 4:2:0, 2:2 for YCbCr 4:2:2, and 2:4 for YCbCr 4:4:4. 00: YCbCr 4:2:0 output for YCbCr-format output 01: YCbCr 4:2:2 output for YCbCr-format output 10: YCbCr 4:4:4 output for YCbCr-format output 11: Setting prohibited
21	WPKF	0	R/W	These bits set the output data pack form when the VEU output data is in the BGR format. When the BGR888(3byte/pix) format output is used, it changes to the setting of VTRCR.WPKFR=1 and the VTRCR.WPKF=H '15.

20 to 16	WPKF[4:0]	00000	R/W	These bits set the output data pack form when the VEU output data is in the RGB format. The VEU packs output data into a 32-bit pack. When data is output in the RGB format and YCbCr format, the data is packed into one of the patterns shown in tables 35.6 and 35.7, respectively. For RGB-format output, set a value in the WPKF column in table 35.18 in these bits. When the RGB stuffing output pack is used (WPKF = H'10, H'11, H'12, or H'15), the start line must have the pack form of phase 0 shown in table 35.6.

Note: * When the alpha resize is used, the alpha value is output to the change of the PAD value. (Only VEU2 and 3: ALP_ON=1).

Bit	Bit Name	Initial Value	R/W	Description
15, 14	CHRR[1:0]	00	R/W	These bits set the source image form for the VEU. When a YCbCr image is input, output is done in one of the pack patterns shown in table 35.7. 00: Source image is read in the YCbCr 4:2:0 format 01: Source image is read in the YCbCr 4:2:2 format 10: Source image is read in the YCbCr 4:4:4 format 11: Setting prohibited
13, 12	—	00	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 8	RPKF[3:0]	000	R/W	These bits set the RGB input data pack form when the VEU input data is in the RGB format. Table 35.8 shows the relationship between the RGB format selected by these bits and the input form. When the VEU input data is in the RGB format, set a value in the RPKF column in table 35.8 in these bits.
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	DITH	0	R/W	Selects whether dithering is applied or not when performing tone reduction of an RGB image. The VEU has a tone reduction function for RGB images. The number of tones after this processing is determined by the WPKF bit setting. Tone reduction processing for RGB images uses quantization which causes the resultant image to contain false contours. This problem becomes more serious as the number of tones is reduced, and it generally degrades the image quality. The VEU can perform dithering to lessen this degradation caused by tone reduction. 0: Does not apply dithering at tone reduction for the VEU destination image in the RGB format 1: Applies dithering at tone reduction for the VEU destination image in the RGB format

Bit	Bit Name	Initial Value	R/W	Description
3 2	TM2 TM1	0 0	R/W R/W	Selects the color converting equation of color conversion circuit. 00: Use color conversion of full-range RGB[0,255] ⇔ Y[16,235], CbCr[16,240] conforms to ITU-R BT.601. 01: Use color conversion of full range RGB[0,255] ⇔ YCbCr[0,255] conforms to ITU-R BT.601. 10: Use color conversion of full-range RGB[0,255] ⇔ Y[16,235], CbCr[16,240] conforms to ITU-R BT.709. 11: Use color conversion of full-range RGB[16,235] ⇔ Y[16,235], CbCr[16,240] conforms to ITU-R BT.709.
1 0	TE RY	0 0	R/W R/W	The TE bit turns on or off the circuit for RGB ⇔ YCbCr conversion. The RY bit specifies whether the image input is in the YCbCr format or RGB format. Table 35.9 shows the relationship between the TE and RY bit settings and the input/output data format. 00: Reads a YCbCr source image and does not perform YCbCr → RGB conversion 01: Reads an RGB source image and does not perform RGB → YCbCr conversion 10: Reads a YCbCr source image and performs YCbCr → RGB conversion 11: Reads an RGB source image and performs RGB → YCbCr conversion

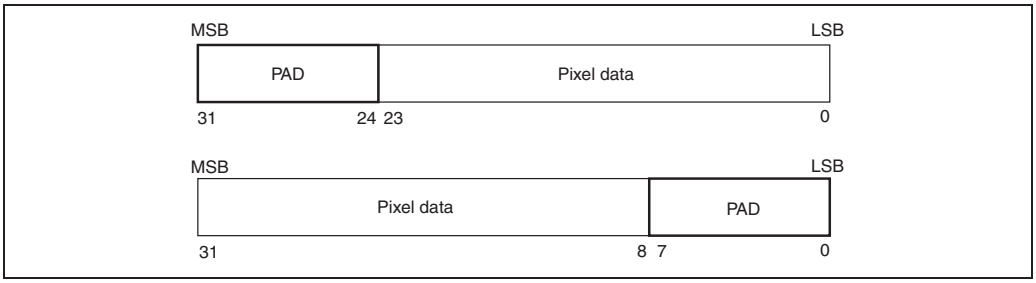


Figure 35.16 Data Pack Forms Including PAD

Table 35.6 RGB Data Output Pack Forms

| No. | WPKF | Bit Rate [bpp] | P Density_y [pix/LW] | Phase | Bit | | |

Table 35.8 RGB Data Input Pack Forms

No	RPKF	Bit Rate [bpp]	P_density_y [pix/LW]	Phase	Bit 31~24								23~16								15~8								7~0							
0	B'0000	24	1	–	x	x	x	x	x	x	x	x	R0	R0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	B0	B0
1	B'0001			–	R0	R0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	B0	B0	x	x	x	x	x	x	x	x
2	B'0010		4/3	0	R0	R0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	B0	B0	R1	R1	R1	R1	R1	R1	R1	R1
				1	G1	G1	G1	G1	G1	G1	G1	G1	B1	B1	B1	B1	B1	B1	B1	B1	R2	R2	R2	R2	R2	R2	R2	R2	G2	G2	G2	G2	G2	G2	G2	G2
				2	B2	B2	B2	B2	B2	B2	B2	B2	R3	R3	R3	R3	R3	R3	R3	R3	G3	G3	G3	G3	G3	G3	G3	G3	B3	B3	B3	B3	B3	B3	B3	B3
3	B'0011	16	2	–	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	R1	R1	R1	R1	R1	G1	G1	G1	G1	G1	G1	B1	B1	B1	B1	B1
7	B'0111	18	1	–	x	x	x	x	x	x	x	x	x	x	x	x	x	x	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	B0
11	B'1011	24	4/3	0	B0	B0	B0	B0	B0	B0	B0	B0	G0	G0	G0	G0	G0	G0	G0	G0	R0	R0	R0	R0	R0	R0	R0	R0	B1	B1	B1	B1	B1	B1	B1	B1
				1	G1	G1	G1	G1	G1	G1	G1	G1	R1	R1	R1	R1	R1	R1	R1	R1	B2	B2	B2	B2	B2	B2	B2	B2	G2	G2	G2	G2	G2	G2	G2	G2
				2	R2	R2	R2	R2	R2	R2	R2	R2	B3	B3	B3	B3	B3	B3	B3	B3	G3	G3	G3	G3	G3	G3	G3	G3	R3	R3	R3	R3	R3	R3	R3	R3
12	B'1100		1	–	x	x	x	x	x	x	x	x	B0	B0	B0	B0	B0	B0	B0	B0	G0	G0	G0	G0	G0	G0	G0	G0	R0	R0	R0	R0	R0	R0	R0	R0
13	B'1101	16		–	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0

Note: When the alpha resize is used, 31~24bit of RPKF=0 and 7~0bit of RPKF=1 replace the alpha value.

Table 35.9 Relationship between TE and RY Bits in VTRCR and Input/Output Data Format

TE Bit	RY Bit	Input	Output
0	0	YCbCr format	YCbCr format
0	1	RGB format	RGB format
1	0	YCbCr format	RGB format
1	1	RGB format	YCbCr format

35.3.11 VEU Resize Filter Control Register (VRFCR)

VRFCR sets the scale-up/down factor for the image scaling filter. When performing scale-up/down processing, some other processings cannot be performed simultaneously (see table 35.14).

Modifying this register during operation is prohibited.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VVMNT[3:0]				VVFRC[11:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VHMNT[3:0]				VHFRC[11:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	VVMNT[3:0]	H'0	R/W	Mantissa Part of Vertical Scaling Factor These bits set the vertical scaling factor. A value from H'0 to H'F can be set. When the VVMNT bits are set to H'0 and the VVFRC bits to H'000, the output is the same size.
27 to 16	VVFRC[11:0]	H'000	R/W	Fraction Part of Vertical Scaling Factor These bits set the vertical scaling factor. A value from H'000 to H'FFF can be set.
15 to 12	VHMNT[3:0]	H'0	R/W	Mantissa Part of Horizontal Scaling Factor These bits set the horizontal scaling factor. A value from H'0 to H'F can be set. When the VHMNT bits are set to H'0 and the VHFRC bits to H'000, the output is the same size.
11 to 0	VHFRC[11:0]	H'000	R/W	Fraction Part of Horizontal Scaling Factor These bits set the horizontal scaling factor. A value from H'000 to H'FFF can be set.

The VEU has an image scaling filter that can scale the image up and down, as shown in figure 35.17. The scaling filter cannot be operated simultaneously with the median filter, deblocking filter, or low-pass filter, and rotation is also prohibited. Accordingly, set B'0 to the bits in VFMCR, except the HMRR (horizontal inversion) and VMRR (vertical inversion) bits, when setting VRFCR.

The scaling factor for scale-up/down can be set between 1/16 to 16.

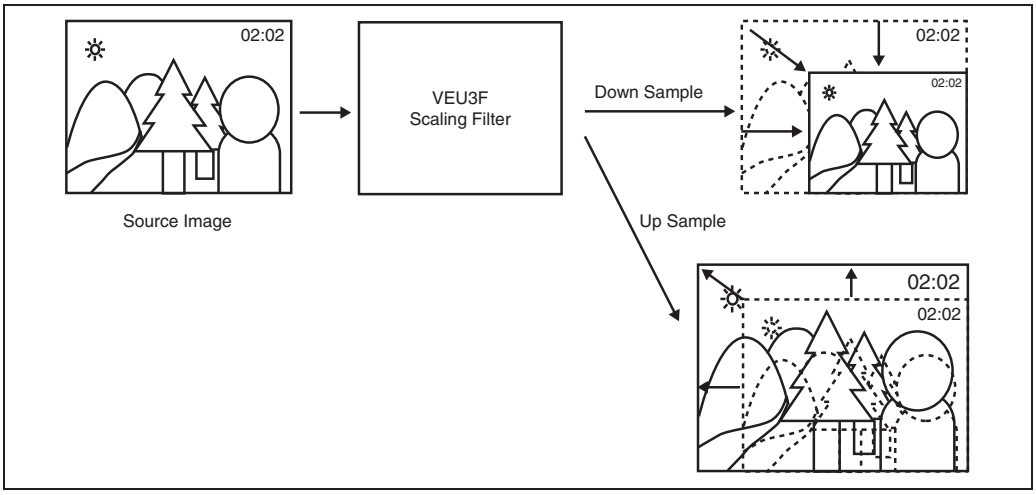


Figure 35.17 Scaling of Image by VEU

The formulas for obtaining the output pixel count of the scale-up/-down from the scaling ratio and the input pixel count are defined as follows:

$$\alpha = MANT \times 4096 + FRAC \quad \text{. . . Formula 1}$$

$$SCL \text{ (scaling factor)} = \frac{4096}{\alpha} \quad \text{. . . Formula 2}$$

In a formula listed below, decimal place of a calculation result of <A> is rounded off. Here, a input image size is indicated as Sin, and a output image size as SIZE.

Note: Horizontal: Sin = VESSR.VHSS
Vertical: Sin = VESSR.VVSS

[Scale-down]

$$SIZE =< 1 + (< 1 + (Sin - 1) / MANTpre > - 1) \times MANTpre \times SCL > \quad [1/16 < SCL \leq 1\ ]$$

…Formula 3

$$MANTpre = 1 \quad [1 \leq MANT > 4]$$
$$= 2 \quad [4 \leq MANT > 8]$$
$$= 4 \quad [8 \leq MANT > 16] \quad \text{…Formula 4}$$

[Scale-up]

SIZE = < 1 + (Sin – 1) × SCL > [1 < SCL ≤ 16, VRSCR.AMD = 0] …Formula 5
SIZE - < Sin × SCL > [1 < SCL ≤ 16, VRSCR.AMD = 1] …Formula 6

Note: See section 35.3.14, VEU Resize Filter Control Register (VRSCR) details on the AMD bit

Example : Scale up 88 pixels to 352 pixels (VRSCR.AME = 0)

SCL = 352/88 = 4, suppose SCL = 4, and the preliminary settings of MANT = 0 and FRAC = 1024 are made based on formulas 1 and 2. Substituting these in formula 5 results in an output pixel count of 349. Since this calculated value is smaller than the desired output pixel count of 352, set FRAC to a value that is smaller than this value but at the same time the maximum value (MANT = 0, FRAC = H'3FF). At this point, the output pixel count is 349, which is not the desired output pixel count so that the calculation to be repeated. Setting to a value FRAC = H'3F7, the output pixel count becomes 352 which is the desired output pixel count. So set MANT = 0, FRAC = H'3F7 for the scaling up 88 pixels to 352.

Table 35.10 Settings for Each Horizontal Scaling Factor of Scaling Filter

		FRAC		
Scaling Factor	**AMD**	**Decimal**	**Hexadecimal**	**MANT**
8	0	508	H'1FC	0
4	0	1017	H'3F9	0
2	0	2039	H'7F7	0
1.5	0	2723	H'AA3	0
8	1	512	H'200	0
4	1	1024	H'400	0
2	1	2048	H'800	0
1.5	1	2730	H'AAA	0
7/8	0	585	H'249	1
3/4	0	1365	H'555	1
5/8	0	2457	H'999	1
1/2	0	0	H'0	2
1/4	0	0	H'0	4
1/8	0	0	H'0	8

35.3.12 VEU Resize Filter Size Clip Register (VRFSR)

VRFSR sets the clipping (discarded) size of fractions in pixels output from the filter, and must be set in combination with VRFCR.

Modifying this register during operation is prohibited.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	VVCLP[11:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	VHCLP[11:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
27 to 16 (28 to 16)	VVCLP[11:0]	H'000	R/W	These bits set the vertical clipping size after scale-up/down in pixel units (1-pixel units). This setting should be made in 2-pixel units when the YCbCr format is 4:2:0.*
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 0	VHCLP[11:0]	H'000	R/W	These bits set the horizontal clipping size after scale-up/down in pixel units (4-pixel units). This setting should be made in 2-pixel units when the WPKF bits (write pack) in VTRCR are set to 1, 2, 6, 8 to 14, 19, 20, 22, or 23.

Note: When resizing it, it can be assumed it is vertical 8188 or less (Only VEU2 and VEU3).

The VVCLP and VHCLP bits in the VRFSR register set the output size when line processing (scale-up/down, enhancer, or bundle read) is performed. The size can be specified in 4-pixel units horizontally and in 1-pixel (2-pixel for YCbCr4:2:0 format) units vertically in VRFSR. However, a setting in 2-pixel units horizontally is possible for RGB 2 bytes/pixel (VTRCR.WPKF=1, 2, 6) and RGB 4 bytes/pixel (VTRCR.WPKF=8 to 14, 19, 20, 22, 23).

The maximum value to be set in the VVCLP and VHCLP bits in the VRFSR register is 4092 pixels. The minimum value for them is 4 pixels*[1]. Note that the values should be such that VRFSR.VHCLP + VRSOR.VHCLOFS ≤ 4092*[2].

Note: 1 When the FIR11tap filter is used, The minimum value for them is 8 pixels

2 When the FIR11tap filter is used, it becomes 2048 or less (VEU2,3).

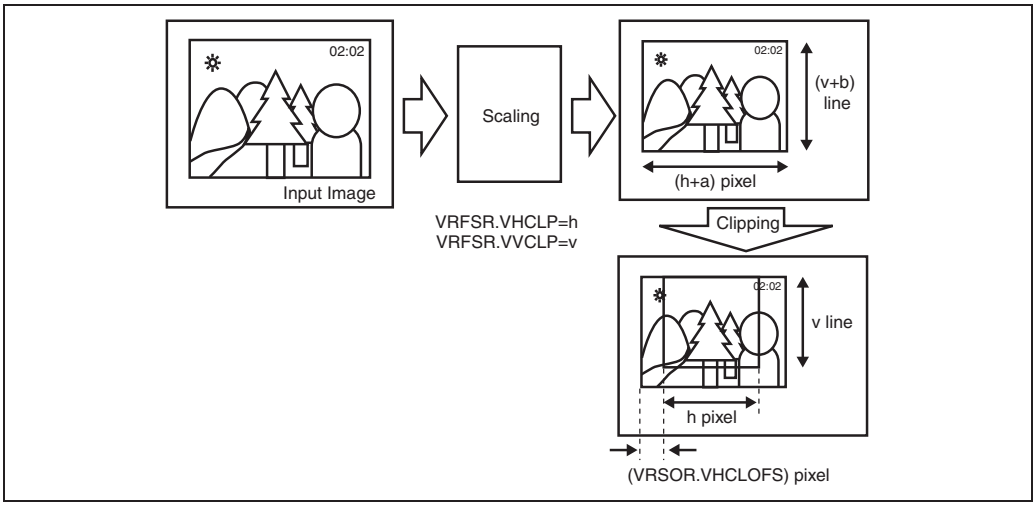


Figure 35.18 Clipping of Image Output from VEU Scaling Filter

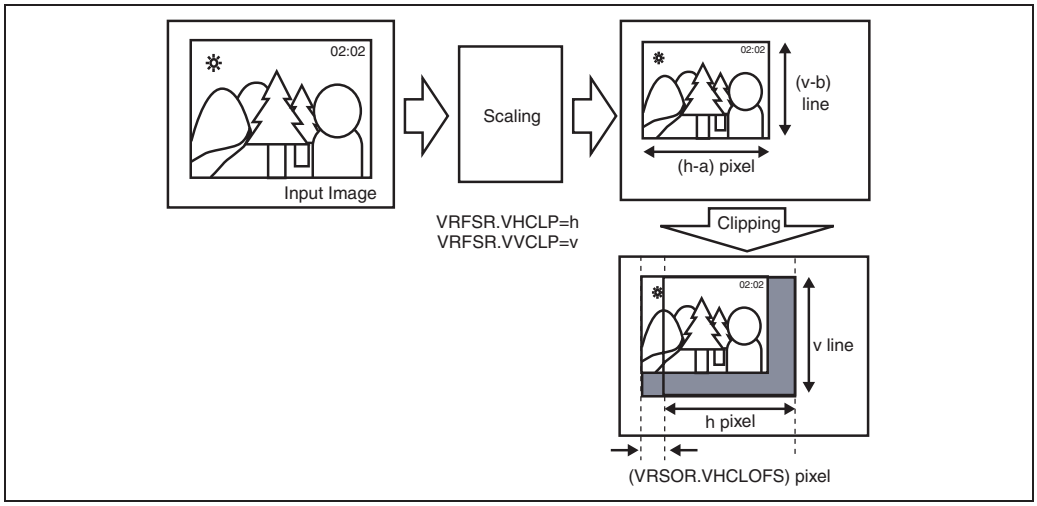


Figure 35.19 Shifting of Image Output from VEU Scaling Filter

If the values are smaller than the filter output pixel count, output images are clipped as shown in figure 35.18. The number of output pixels is counted from the position shifted to the right by the offset specified in the VHCLOFS bit in the VRSOR register. The pixels that are located at the right of the specified pixel count or below the specified line count are discarded by the clipping function.

If the values are larger than the filter output pixel count, images are output by complementing pixels up to the specified pixel count according to the FMD bit in the VRSCR register, where the pixels are counted from the position shifted to the right by the offset specified in the VHCLOFS bit in the VRSOR register (see figure 35.19).

However, if the horizontal number of pixels specified in VRFSR is larger than the number of the scaling filter output pixels rounded up to the nearest multiple of 4, the complementary function does not work. In this case, the VEU may be hung up, so the VRFSR value should be a value that is obtained by calculating by the formulas 1 to 6 and rounding up to a multiple of 4.

If the filter output pixel count obtained by the formulas 1 to 6 is equal to 4M +N (M is an integer. N = 1 to 4), VRFSR.VV(H)CLP ≤ 4M+4.

When scale-up/down is not performed, set VRFSR.VHCLP = VESSR.VHSS, VRFSR.VVCLP = VESSR.VVSS.

35.3.13 VEU Enhance Register (VENHR)

VENHR sets up the filter (enhancer) for enhancing the edges of images. Some other processings cannot be performed simultaneously with the edge enhancement processing (see table 35.2). Modifying this register during operation is prohibited.

The enhancer cannot be operated simultaneously with the median filter, deblocking filter, or low-pass filter, and rotation is also prohibited. Accordingly, set B'0 to the bits in VFMCR, except the HMRR (horizontal inversion) and VMRR (vertical inversion) bits, when setting VENHR.

Moreover, when the alpha resize is used, enhancement processing cannot be used(VEU2,3).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	ENSCL[2:0]			—	—	—	—	—	—	ENHV	ENHH
Initial value:	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 8	ENSCL[2:0]	010	R/W	These bits set the factor for edge enhancement. 001: Enhancement level 1 (max) 010: Enhancement level 2 011: Enhancement level 3 100: Enhancement level 4 (min) Other than above: Setting prohibited
7 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
1	ENHV	0	R/W	Enables or disables edge enhancement in the vertical direction. 0: Vertical edge enhancement is not performed 1: Vertical edge enhancement is performed
0	ENHH	0	R/W	Enables or disables edge enhancement in the horizontal direction. 0: Horizontal edge enhancement is not performed 1: Horizontal edge enhancement is performed

35.3.14 VEU Resize Filter Control Register (VRSCR)

VRSCR performs scaling filter adjustments for line processing (with scaling, enhance, and bundle read). For block processing, set all of the initial values of VRSCR to 0 (without scaling, enhance, or bundle read).

Writing 1 to the read-only bits is prohibited. If 1 is written to any of these bits a malfunction may occur. Modifying this register during operation is prohibited.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	AMD	FMD	LC[1:0]		—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	AMD	0	R/W	This bit specifies the pixel count generated when the scaling filter performs a scale-up. When AMD = 1 is specified, int (n * scale-up factor) pixels are created by complementing horizontal and vertical pixels in the destination image for AMD = 0. 0: The pixel count obtained at a scale-up is 1+int ((n1)*scale-up factor). 1: The pixel count obtained at a scale-up is int (n*scale-up factor).
30	FMD	0	R/W	This bit specifies the pixel complementing method for the scaling filter. When the scaling filter outputs an image that does not fill the clip size, the pixels are complemented up to the clip size. 0: Copy right (lower) pixels and provide complementary pixels. 1: Provide complementary right(lower) pixels of a color specified by VFLCR.
29, 28	LC[1:0]	00	R/W	These bits specify the number of pixels for source image horizontal-left clipping. From 0 to 3 can be specified. Because the source address registers VSAYR and VSCAR are both in longword units, if the input format is YCbCr, the starting position for horizontal clipping from the background image is in four-pixel units. Therefore, if you perform background image clipping from pixel position at the left end 4M+LC (M; integer, LC: 0-3), 4M is adjusted by the VSAYR read start address, and the lower two bits are adjusted by this bit (LC). When the value of this bit has been set, input to the scaling filter is specified by the VHSS bits in VESSR and the LC bits in VRSCR for the horizontal direction and by the VVSS bits in VESSR for the vertical direction.
27 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

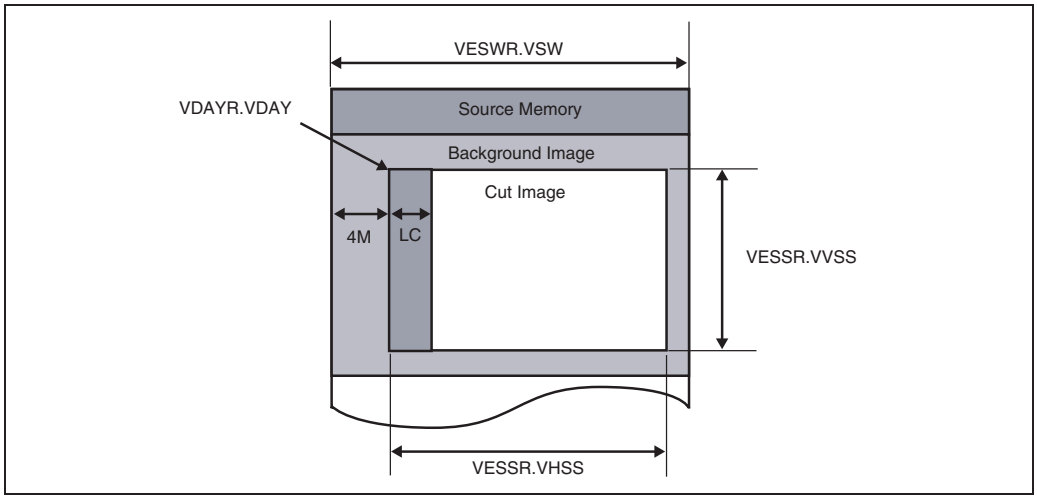


Figure 35.20 Relations between the Background Image and Clipping Pixel Location

35.3.15 VEU Resize Filter Size Clip Offset Register (VRSOR)

VRSOR sets the left clip offset when images are clipped bases on the filter output pixel count. For details on the offset positions, see figures 35.18 and 35.19. When following Flow 2 in figure 35.2, set an offset that is smaller than the horizontal number of pixels of the output image after scaling down.

Also, make sure such that VRFSR.VHCLP + VRSOR.VHCLOF ≤ 4092*.

Note: When the FIR11tap filter is used, it becomes 2048 or less (VEU2,3).

When this register is set, the VRFCR and VRFSR registers should also be set. Since the register setting is used as the output size when Flow 2 describe in section 35.2, Functional Overview of VEU (Scale-up/down, enhancer, or bundle read is performed), this register should be set even if scale-up/down is not performed.

Writing to this register during operation is prohibited.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
									VVCLOFS[7:0]							
Initial valude:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
									VHCLOFS[7:0]							
Initial valude:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 16	VVCLOFS [7:0]	H'00	R/W	Specifies the vertical clip offset by the number of pixel (one-pixel unit) after scale-up/down(Only VEU2 and 3).
15 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	VHCLOFS [7:0]	H'00	R/W	Specifies the lateral clip offset by the number of pixel (one-pixel unit) after scale-up/down.

35.3.16 VEU Filter Mode Control Register (VFMCR)

VFMCR sets the operating mode for filter processing.

Writing 1 to read-only bits is prohibited. If 1 is written to any of these bits, a malfunction may occur. Modifying this register during operation is prohibited.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
							MEDFST	FLTPI								MED
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				TPN			DBLK	LPHV			VMRR	HMRR			ROTL	ROTR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25	MEDFST	0	R/W	Changes the order of applying the median filter and deblocking filter when the FLTPI bit is set to 1. 0: Applies the LPF/deblocking filer and median filter in this order. 1: Applies the median filer and LPF/deblocking filter in this order. Note: Only when a high-speed filter is processed(FLTPI=1), it is possible to use it.
24	FLTPI	0	R/W	Controls fast processing of LPF, deblocking filer, and median filter. 0: Disables fast processing of LPF, deblocking filer, and median filter. 1: Enables fast processing of LPF, deblocking filer, and median filter. Note: When the FIR filter is used, it is necessary to

Bit	Bit Name	Initial Value	R/W	Description
				set it to 1(VEU2,3). When the FLTPI is set to 1, the possible settings are restricted to the followings: (1) VFMCR.ROTR = 0 (2) VFMCR.ROTL = 0 (3) VESTR.VBE = 0 (4) VRSOR.VHCLOFS = 0 (VEU0,1) (5) VRFSR.VVCLP = VSSR.VVSS (VEU0,1) (6) VRFSR.VHCLP = VSSR.VHSS (VEU0,1) (5)' VRSOR.VVCLOFS＋VRFSR.VVCLP=VSSR.VVSS(VEU2,3) (6)' VRSOR.VHCLOFS＋VRFSR.VHCLP<=VSSR.VHSS(VEU2,3)
23 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	MED	0	R/W	Enables or disables usage of the median filter. When the median filter is applied to an image, scale-up/down processing and edge enhance processing cannot be performed at the same time. In bundle read mode, the median filter cannot be used. Therefore, when this bit is set to 1, set VRFCR, VENHR, and the VBE bit in VESTR to 0. (Interoperating with the scale-up/down processing, edge enhance processing, and bundle read mode is prohibited.) The relationship between this bit and the filter operation is shown in table 35.11. 0: Median filter is not used 1: Median filter is applied to the source image

Bit	Bit Name	Initial Value	R/W	Description
15, 13	—	00	R	Reserved These bits are always read as 0. The write value should always be 0.
12 (13 to 12)	TPN[1:0]	00	R/W	Sets the FIR filter (high-speed process: FLTPI = 1) and the number of taps of the low-pass filter (LPF). 00: Count for FIR filter or LPF tap is set to 3 taps (initial value) 01: Count for FIR filter or LPF tap is set to 5 taps 10: FIR filter count is set to 11 taps*
11, 10	—	00	R	Reserved These bits are always read as 0. The write value should always be 0.
9	DBLK	0	R/W	Enables or disables usage of the deblocking filter. When the deblocking filter is applied to an image in bundle read mode, scale-up/down processing and edge enhance processing cannot be performed at the same time. When this bit is set to 1, set VRFCR, VENHR, and the VBE bit in VESTR to 0. Specifies the lateral clip offset by the number of pixel (one-pixel unit) after scale-up/down. The relationship between this bit and the filter operation is shown in table 35.11. 0: LPF is applied to the entire source image (normal mode) 1: LPF is applied to only the boundary of the 8 × 8 pixel blocks of the source image (deblocking mode)
8	LPHV	0	R/W	Enables or disables usage of the low-pass filter. In bundle read mode, the low-pass filter cannot be used. When the low-pass filter is applied to an image, scale-up/down processing and edge enhance processing cannot be performed at the same time. When this bit is set to 1, set VRFCR, VENHR, and the VBE bit in VESTR to 0. (Interoperating with the scale-up/down processing, edge enhance processing, and bundle read mode is prohibited.) The relationship between this bit and the filter operation is shown in table 35.11. 0: NOP 1: LPF is applied to the source image

Bit	Bit Name	Initial Value	R/W	Description
				Note: When the FIR filter is used, it is necessary to set it to 1(VEU2,3).
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	VMRR	0	R/W	Enables or disables usage of the vertical inversion (symmetric with regard to horizontal axis) filter. The relationship between this bit and the rotate/invert operation is shown in table 35.12. 0: NOP 1: Vertical inversion (symmetric with regard to horizontal axis) filter is applied to the source image
4	HMRR	0	R/W	Enables or disables usage of the horizontal inversion (symmetric with regard to vertical axis) filter. The relationship between this bit and the rotate/invert operation is shown in table 35.12. 0: NOP 1: Horizontal inversion (symmetric with regard to vertical axis) filter is applied to the source image
3, 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	ROTL	0	R/W	Enables or disables usage of the 270-degree rotation (clockwise) filter. In bundle read mode, rotation cannot be performed. When rotation processing is performed for an image, scale-up/down processing and edge enhance processing cannot be performed at the same time. When this bit is set to 1, set VRFCR, VENHR, and the VBE bit in VESTR to 0. (Interoperating with the scale-up/down processing, edge enhance processing, and bundle read mode is prohibited.) The relationship between this bit and the rotate/invert operation is shown in table 35.12. 0: NOP 1: 270-degree rotation (clockwise) filter is applied to the source image

Bit	Bit Name	Initial Value	R/W	Description
0	ROTR	0	R/W	Enables or disables usage of the 90-degree rotation (clockwise) filter. In bundle read mode, rotation cannot be performed. When rotation processing is performed for an image, scale-up/down processing and edge enhance processing cannot be performed at the same time. When this bit is set to 1, set VRFCR, VENHR, and the VBE bit in VESTR to 0. (Interoperating with the scale-up/down processing, edge enhance processing, and bundle read mode is prohibited.) The relationship between this bit and the rotate/invert operation is shown in table 35.12. 0: NOP 1: 90-degree rotation (clockwise) filter is applied to the source image

Note: * When the tap count is set to 11, the maximum number of horizontal pixel is to be 2048. The setting enables only for the VEU2 and VEU3.
The setting disables other than when FLTPI = 1. Further more, in scale-up/-down or enhancing, set to 0 or 1.

Table 35.11 Relationship between MED, DBLK, and LPHV Bits and Filter Operation

MED Bit	DBLK Bit	LPHV Bit	Filter Operation
0	0	0	Passed through
0	0	1	Low-pass filter/FIR filter
0	1	1	Deblocking filter
1	1	1	Deblocking filter + median filter*
1	0	0	Median filter
1	0	1	Low-pass filter + Median filter**
Other than above			Setting prohibited

Note: * The order of deblocking filter → median filter cannot be changed.
** It is effective only to process a high-speed filter (FLTPI=1).

Table 35.12 Relationship between VMRR, HMRR, ROTL, and ROTR Bits and Rotate/Invert Operation

VMRR Bit	HMRR Bit	ROTL Bit	ROTR Bit	Rotate/Invert Operation
0	0	0	0	No rotation/inversion
0	0	0	1	Rotated by 90 degrees clockwise
0	0	1	0	Rotated by 270 degrees clockwise
0	1	0	1	Rotated by 90 degrees clockwise and then inverted in the horizontal direction
1	0	0	1	Rotated by 90 degrees clockwise and then inverted in the vertical direction
0	1	0	0	Inverted in the horizontal direction
1	0	0	0	Inverted in the vertical direction
1	1	0	0	Rotated by 180 degrees
Other than above				Setting prohibited

To rotate the image 270 degrees and then invert it in the horizontal direction, rotate the image 90 degrees and then invert it in the vertical direction. Likewise, to rotate the image 270 degrees and then invert it in the vertical direction, rotate the image 90 degrees and then invert it in the horizontal direction.

Figures 35.21 and 35.22 show the relationship between the rotated/inverted images and raw image.

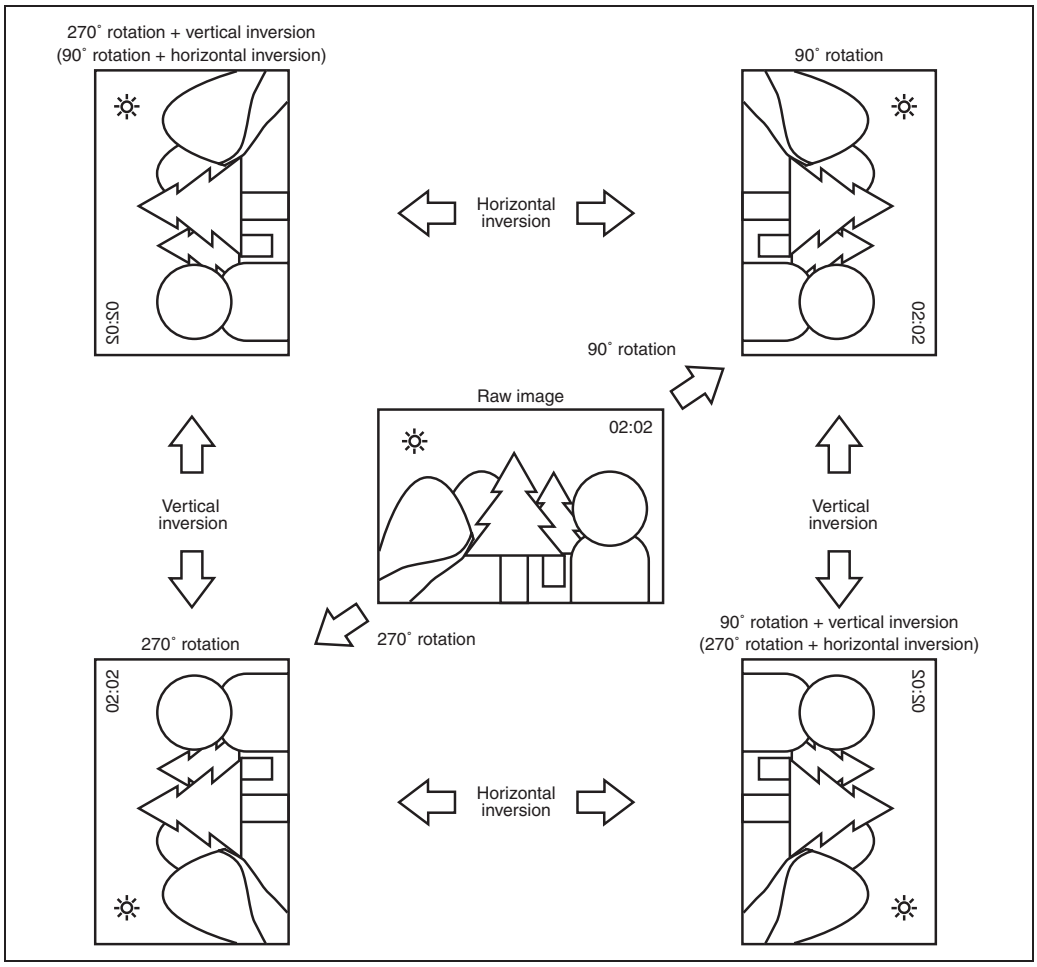


Figure 35.21 Relationship between Rotated/Inverted Images and Raw Image

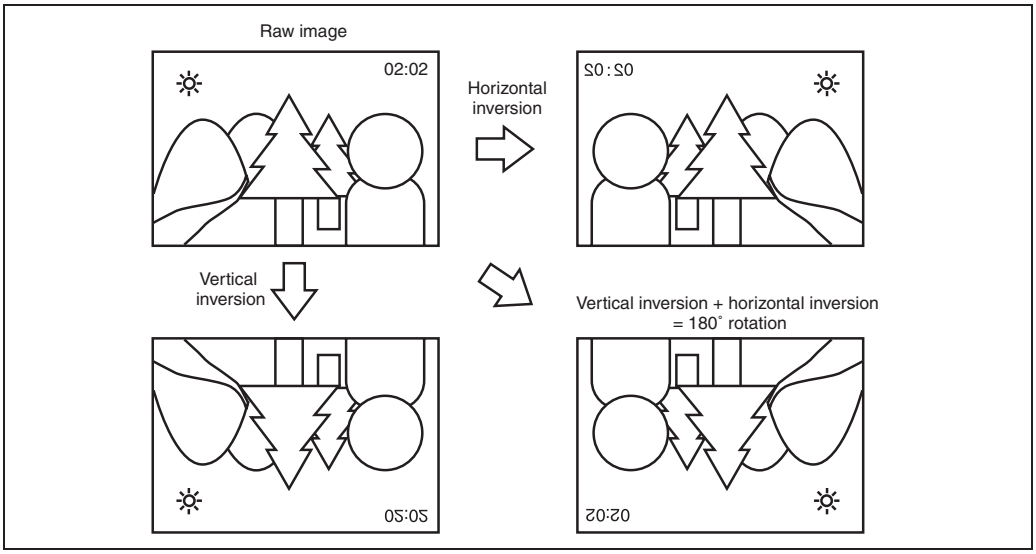


Figure 35.22 Relations between Inverted Images and Raw Image

35.3.17 VEU Vertical Tap Coefficient Register (VVTCR)

VVTCR sets the vertical tap coefficients when applying the low-pass filter.

Writing 1 to read-only bits is prohibited. If 1 is written to any of these bits, a malfunction may occur. Modifying this register during operation is prohibited.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	VSHFT[2:0]			VTPC4[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VTPC3[3:0]				VTPC2[3:0]				VTPC1[3:0]				VTPC0[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 23	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
22 to 20	VSHFT[2:0]	000	R/W	These bits specify the shift capacity after vertical tap calculation. Set how many pixels the location is to be shifted right after adding each vertical tap coefficient. This setting must correspond to the sum of the VTPC0 to VTPC4 bits. See table 35.13 for details on the values corresponding to the total value of VVTCR.VTPC.
19 to 16	VTPC4[3:0]	H'0	R/W	These bits set vertical tap coefficient 4 (clear these bits to 0 for a 3-tap filter). Set the component of the pixel two pixels right of that location to be given when applying a 5-tap low-pass filter. Clear these bits to 0 when applying a 3-tap low-pass filter.
15 to 12	VTPC3[3:0]	H'0	R/W	These bits set vertical tap coefficient 3. Set the component of the pixel on the right of that location to be given when applying a low-pass filter.

Bit	Bit Name	Initial Value	R/W	Description
11 to 8	VTPC2[3:0]	H'0	R/W	These bits set vertical tap coefficient 2. Set the component of that location to be given when applying a low-pass filter.
7 to 4	VTPC1[3:0]	H'0	R/W	These bits set vertical tap coefficient 1. Set the component of the pixel on the left of that location to be given when applying a low-pass filter
3 to 0	VTPC0[3:0]	H'0	R/W	These bits set vertical tap coefficient 0 (clear these bits to 0 for a 3-tap filter). Set the component of the pixel two pixels left of that location to be given when applying a 5-tap low-pass filter. Clear these bits to 0 when applying a 3-tap low-pass filter.

Table 35.13 Shifting Value Corresponds to Sum of VTPC4 to VTPC0

ΣVVTCR.VTPC	VVTCR.VSHFT
4	2
8	3
16	4
32	5
64	6

Examples of setting VVTCR are shown below. When the VTPC4 bits are H'0 and the VTPC0 bits are H'0, set the TPN bit in VFMCR to B'0 because a 3-tap low-pass filter is to be used. In all other cases, set the TPN bit to B'1 because a 5-tap low-pass filter is to be used.

Table 35.14 Values Set in VVTCR

Bit Name	VSHFT	VTPC4	VTPC3	VTPC2	VTPC1	VTPC0
Values to be set	2	0	1	2	1	0
	3	0	1	6	1	0
	3	1	2	2	2	1
	3	1	1	4	1	1
	4	0	1	14	1	0
	4	0	3	10	3	0
	4	0	5	6	5	0
	4	1	1	12	1	1
	4	1	2	10	2	1
	4	1	3	8	3	1
	4	1	4	6	4	1
	4	2	3	6	3	2
	4	3	3	4	3	3
	5	0	9	14	9	0
	5	1	8	14	8	1
	5	1	9	12	9	1
	5	1	10	10	10	1
	5	2	7	14	7	2
	5	2	9	10	9	2
	5	3	6	14	6	3
	5	3	7	12	7	3
	5	3	8	10	8	3
	5	4	5	14	5	4
	5	4	7	10	7	4
	5	5	5	12	5	5
	5	5	6	10	6	5
	5	5	7	8	7	5

Bit Name	VSHFT	VTPC4	VTPC3	VTPC2	VTPC1	VTPC0
Values to be set	5	5	6	10	6	5
	5	5	7	8	7	5
	6	11	14	14	14	11
	6	12	13	14	13	12

Note: Horizontal and vertical taps should be set in the same size.

35.3.18 VEU Horizontal Tap Coefficient Register (VHTCR)

VHTCR sets the horizontal tap coefficients when applying the low-pass filter.

Writing 1 to read-only bits is prohibited. If 1 is written to any of these bits, a malfunction may occur. Modifying this register during operation is prohibited.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	HSHFT[2:0]			HTPC4[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HTPC3[3:0]				HTPC2[3:0]				HTPC1[3:0]				HTPC0[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 23	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
22 to 20	HSHFT[2:0]	000	R/W	These bits specify the shift capacity after horizontal tap calculation. Set how many pixels the location is to be shifted right after adding each horizontal tap coefficient. For details on the setting, see the description of the VSHFT bits in VVTCR. See table 35.13 for details on the values corresponding to the total value of VHTCR.HTPC.
19 to 16	HTPC4[3:0]	H'0	R/W	These bits set horizontal tap coefficient 4. Set the component of the pixel two pixels right of that location to be given when applying a 5-tap low-pass filter. Clear these bits to 0 when applying a 3-tap low-pass filter.
15 to 12	HTPC3[3:0]	H'0	R/W	These bits set horizontal tap coefficient 3. Set the component of the pixel on the right of that location to be given when applying a low-pass filter.
11 to 8	HTPC2[3:0]	H'0	R/W	These bits set horizontal tap coefficient 2. Set the component of that location to be given when applying a low-pass filter.

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	HTPC1[3:0]	H'0	R/W	These bits set horizontal tap coefficient 1. Set the component of the pixel on the left of that location to be given when applying a low-pass filter
3 to 0	HTPC0[3:0]	H'0	R/W	These bits set horizontal tap coefficient 0. Set the component of the pixel two pixels left of that location to be given when applying a 5-tap low-pass filter. Clear these bits to 0 when applying a 3-tap low-pass filter.

Table 35.15 Shifting Value Corresponds to Sum of HTPC4 to HTPC0

ΣVHTCR.HTPC	VHTCR.HSHFT
4	2
8	3
16	4
32	5
64	6

Examples of setting VHTCR are shown below. When both the HTPC4 bits and HTPC0 bits are H'0, set the TPN bit in VFMCR to B'0 because a 3-tap low-pass filter is to be used. In all other cases, set the TPN bit to B'1 because a 5-tap low-pass filter is to be used.

Table 35.16 Values Set in VHTCR

Bit Name	HSHFT	HTPC4	HTPC3	HTPC2	HTPC1	HTPC0
Values to be set	2	0	1	2	1	0
	3	0	1	6	1	0
	3	1	2	2	2	1
	3	1	1	4	1	1
	4	0	1	14	1	0
	4	0	3	10	3	0
	4	0	5	6	5	0
	4	1	1	12	1	1
	4	1	2	10	2	1
	4	1	3	8	3	1
	4	1	4	6	4	1
	4	2	3	6	3	2
	4	3	3	4	3	3
	5	0	9	14	9	0
	5	1	8	14	8	1
	5	1	9	12	9	1
	5	1	10	10	10	1
	5	2	7	14	7	2
	5	2	9	10	9	2
	5	3	6	14	6	3
	5	3	7	12	7	3
	5	3	8	10	8	3
	5	4	5	14	5	4
	5	4	7	10	7	4
	5	5	5	12	5	5
	5	5	6	10	6	5
	5	5	7	8	7	5
	5	5	5	12	5	5

Bit Name	HSHFT	HTPC4	HTPC3	HTPC2	HTPC1	HTPC0
Values to be set	5	5	6	10	6	5
	5	5	7	8	7	5
	6	11	14	14	14	11
	6	12	13	14	13	12

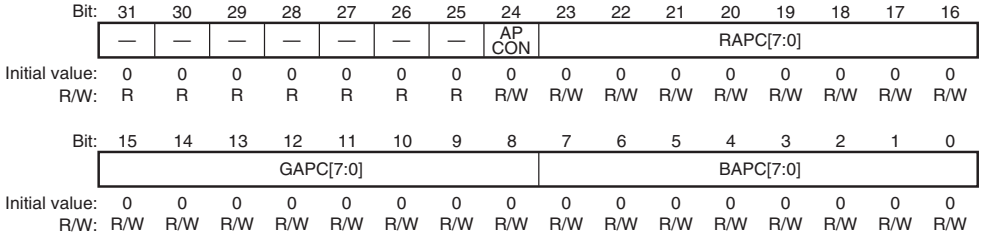
Note: Horizontal and vertical taps should be set in the same size.

35.3.19 VEU Designated Color Register (VAPCR)

VAPCR specifies the designated color.

When any pixel in an image to be processed by the VEU is the same as the designated color set by this register, that pixel is replaced with the conversion color set by VECCR. For an RGB output, clear the lower bits except the valid bits to 0. For a YCbCr output, only the YCbCr 4:4:4 format is supported.

Writing 1 to read-only bits is prohibited. If 1 is written to any of these bits, a malfunction may occur. Modifying this register during operation is prohibited.



Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	APCON	RAPC[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GAPC[7:0]								BAPC[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	APCON	0	R/W	Enables or disables replacement of the designated color. 0: VEU processed image is output as it is 1: VEU processed image is output after pixels corresponding to the designated color have been replaced with the conversion color
23 to 16	RAPC[7:0]	H'00	R/W	These bits specify the R (Cb) component of the designated color.
15 to 8	GAPC[7:0]	H'00	R/W	These bits specify the G (Y) component of the designated color.
7 to 0	BAPC[7:0]	H'00	R/W	These bits specify the B (Cr) component of the designated color.

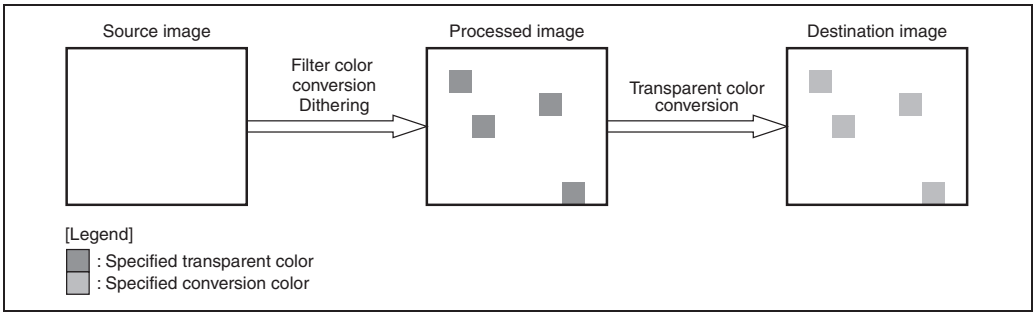


Figure 35.23 Replacement of Designated-Color Pixels in VEU Processed Image with Conversion –Color Pixels

35.3.20 VEU Conversion Color Register (VECCR)

VECCR specifies the conversion color.

When any pixel in an image to be processed by the VEU is the same as the designated color set by VAPCR, that pixel is replaced with the conversion color set by this register. For an RGB output, clear the lower bits except for the valid bits to 0. For a YCbCr output, only the YCbCr 4:4:4 format is supported.

Writing 1 to read-only bits is prohibited. If 1 is written to any of these bits, a malfunction may occur. Modifying this register during operation is prohibited.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	RCHGC[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GCHGC[7:0]								BCHGC[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
23 to 16	RCHGC[7:0]	H'00	R/W	These bits specify the R (Cb) component of the conversion color.
15 to 8	GCHGC[7:0]	H'00	R/W	These bits specify the G (Y) component of the conversion color.
7 to 0	BCHGC[7:0]	H'00	R/W	These bits specify the B (Cr) component of the conversion color.

35.3.21 VEU Fill Color Specification Register (VFLCR)

VFLCR is a fill color specification register.

When the FMD bit in VRSCR is set to 1, VFLCR specifies the fill color used to complement pixels when the pixel area created by the VEU scaling filter is smaller than the clip area specified by the clip size register. For RGB output, specify 0 for the lower bits other than the valid bits. RGB

Writing 1 to read-only bits is prohibited. If 1 is written to any of these bits, a malfunction may occur. Modifying this register during operation is prohibited.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	RFILC[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GFILC[7:0]								BFILC[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 16	RFILC[7:0]	H'00	R/W	These bits specify the R (Cb) component of the fill color.
15 to 8	GFILC[7:0]	H'00	R/W	These bits specify the G (Y) component of the fill color.
7 to 0	BFILC[7:0]	H'00	R/W	These bits specify the B (Cr) component of the fill color.

35.3.22 VEU Address Fixed Register (VAFXR)

VAFXR specifies fixed mode for the addresses of the data output from the VEU.

Writing 1 to read-only bits is prohibited. If 1 is written to any of these bits, a malfunction may occur. Modifying this register during operation is prohibited.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VAFIX
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
0	VAFIX	0	R/W	Sets fixed mode for output addresses. When this bit is 1, the addresses to draw the image output from the VEU is fixed to the values set in VDAYR. When this bit is 0, the output address is incremented according to the data and VEDWR. Fixed address mode is enabled only when the VEU destination image is in the RGB format. For YCbCr destination images, set the following bits or register to 0; the bits MED, LPHV, ROTL, and ROTR in VFMCR (which prohibit median filter, low-pass filter, and rotation), VRFCR (same-size output), and the lower three bits in VDAYR and VRFSR (which disable other than burst transfer). 0: Output addresses are not in fixed address mode 1: Output addresses are in fixed address mode

35.3.23 VEU Swapping Register (VSWPR)

VSWPR sets swapping within the 64-bit data at the data input/output section of the VEU.

When dividing addresses into 64 bits, make the following setting for each case.

- When swapping data in longword units for all inputs/outputs: H'0000 0044
- When swapping data in word units for all inputs/outputs: H'0000 0022
- When swapping data in byte units for all inputs/outputs: H'0000 0011
- When swapping data in byte units from the MSB to the LSB: H'0000 0077

Writing 1 to read-only bits is prohibited. If 1 is written to any of these bits, a malfunction may occur. Modifying this register during operation is prohibited.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	VEOLS	VEOWS	VEOBS	—	VEILS	VEIWS	VEIBS
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6	VEOLS	0	R/W	Sets swapping in longword units for output data. In longword swapping for output data, data is swapped in longword units within the 32 bits on the MSB side and within the 32 bits on the LSB side for 64-bit data in the VEU output section (figure 35.24). 0: Output data is not swapped in longword units 1: Output data is swapped in longword units
5	VEOWS	0	R/W	Sets swapping data in word units for output data. In word swapping for output data, data is swapped in word units within the 32 bits on the MSB side and within the 32 bits on the LSB side for 64-bit data in the VEU output section (figure 35.25). 0: Output data is not swapped in word units 1: Output data is swapped in word units
4	VEOBS	0	R/W	Sets swapping data in byte units for output data. In byte swapping for output data, data is swapped in byte units within each 16 bits for 64-bit data in the VEU output section (figure 35.26). 0: Output data is not swapped in byte units 1: Output data is swapped in byte units
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2	VEILS	0	R/W	Sets swapping data in longword units for input data. In longword swapping for input data, data is swapped in longword units within the 32 bits on the MSB side and within the 32 bits on the LSB side for 64-bit data in the VEU input section (figure 35.24). 0: Input data is not swapped in longword units 1: Input data is swapped in longword units
1	VEIWS	0	R/W	Sets swapping data in word units for input data. In word swapping for input data, data is swapped in word units within the 32 bits on the MSB side and within the 32 bits on the LSB side for 64-bit data in the VEU input section (figure 35.25). 0: Input data is not swapped in word units 1: Input data is swapped in word units

Bit	Bit Name	Initial Value	R/W	Description
0	VEIBS	0	R/W	Sets swapping data in byte units for input data. In byte swapping for input data, data is swapped in byte units within each 16 bits for 64-bit data in the VEU input section (figure 35.26). 0: Input data is not swapped in byte units 1: Input data is swapped in byte units

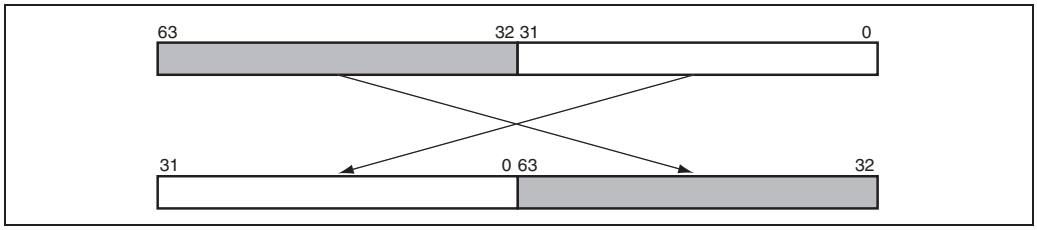


Figure 35.24 Relations before and after Data Swapping in Longword Units

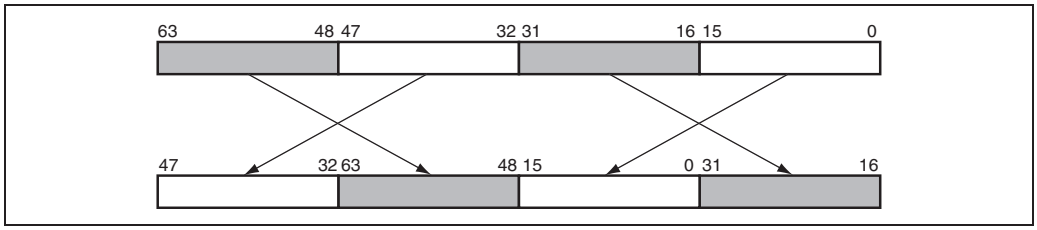


Figure 35.25 Relations before and after Data Swapping in Word Units

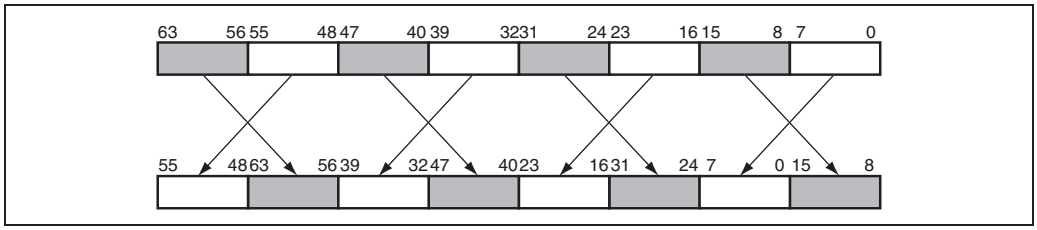


Figure 35.26 Relations before and after Data Swapping in Byte Units

35.3.24 VEU Event Interrupt Enable Register (VEIER)

VEIER enables or disables output of the interrupt signal of a VEVTR flag.

Writing 1 to read-only bits is prohibited. If 1 is written to any of these bits, a malfunction may occur. Modifying this register during operation is prohibited.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	VBENDE	—	—	—	—	—	—	—	VEENDE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	VBENDE	0	R/W	Enables or disables the interrupt signal of VEVTR.VBEND to be output. 0: Disables output of the VEVTR.VBEND interrupt signal 1: Enables output of the VEVTR.VBEND interrupt signal
7 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	VEENDE	0	R/W	Enables or disables the interrupt signal of VEVTR.VEEND to be output. 0: Disables output of the VEVTR.VEEND interrupt signal 1: Enables output of the VEVTR.VEEND interrupt signal

35.3.25 VEU Event Register (VEVTR)

VEVTR indicates the interrupt source when an internal interrupt occurs in the VEU. Whether output of the interrupt signal of each source in VEVTR is enabled or disabled is set by VEIER.

Writing 1 to read-only bits is prohibited. If 1 is written to any of these bits, a malfunction may occur. Modifying this register during operation is prohibited.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	VB END	—	—	—	—	—	—	—	VE END
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	VBEND	0	R/W	This flag is set to 1 when VEU processing has finished for a single read (reading of the number of lines set in VBSSR) in bundle read mode (N-line read mode). The VEU enters the read restart wait state when this flag is set. Therefore, after clearing the interrupt source, switch the address registers, and start reading again (VESTR = H'0000 0011). [Reading] 0: Indicates in progress of reading in bundle read processing, or this flag has already been cleared 1: Indicates that restart is being waited in bundle read processing [Writing] 0: Clears this flag by writing 0 to it 1: Holds the current value

Bit	Bit Name	Initial Value	R/W	Description
7 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	VEEND	0	R/W	This flag is set to 1 when VEU processing has totally finished. This flag is not cleared unless 0 is written to clear the bit after VEU processing ends. Therefore, 0 must be written to this bit to clear it before the VEU is activated again. [Reading] 0: Indicates that VEU processing has not finished, or this flag has already been cleared 1: Indicates that VEU processing has finished [Writing] 0: Clears this flag by writing 0 to it 1: Holds the current value

35.3.26 VEU Status Register (VSTAR)

VSTAR indicates the internal status of the VEU and the internal signal states.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	INTL	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	VB PRC	—	—	—	VB READ	—	—	—	—	—	—	—	VE PRC
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
24	INTL	0	R	Indicates the assert state of the VEU interrupt signal to the CPU. 0: Indicates that no interrupt signal is asserted at the VEU interrupt signal port 1: Indicates that an interrupt signal is asserted at the VEU interrupt signal port
23 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	VBPRC	0	R	Indicates the VEU status in bundle read mode. For details, see table 35.27. 0: Indicates that the VEU is not operating in bundle read (N-line read) mode 1: Indicates that the VEU is operating in bundle read (N-line read) mode
11 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	VBREAD	0	R	For details, see table 35.18. 0: Indicates that the VEU is waiting to be restarted in bundle read (N-line read) mode 1: Indicates that the VEU is reading in bundle read (N-line read) mode
7 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	VEPRC	0	R	Indicates the same value as the VE bit in VESTR. For details, see table 35.18. 0: VEU is ready (halted) 1: VEU is busy (operating state)

The VEU operates in either normal operating mode or bundle read mode. In normal operating mode, the registers are not to be modified between activation and processing end. In bundle read mode, there are two operating states: read processing state and the state waiting for the VEU to be restarted by software. The values when reading VSTAR in each state are shown in table 35.17. Figure 35.27 shows the VSTAR state transitions in normal operating mode, and figure 35.27 shows the VSTAR state transitions in bundle read mode.

Table 35.17 VSTAR Value Read in Each State

Operating Mode		VBPRC Bit	VBREAD Bit	VEPRC Bit
Normal operation	Halted	0	0	0
	Operating	0	0	1
N-line read mode	Halted	0	0	0
	During read processing	1	1	1
	Waiting for restart	1	0	1

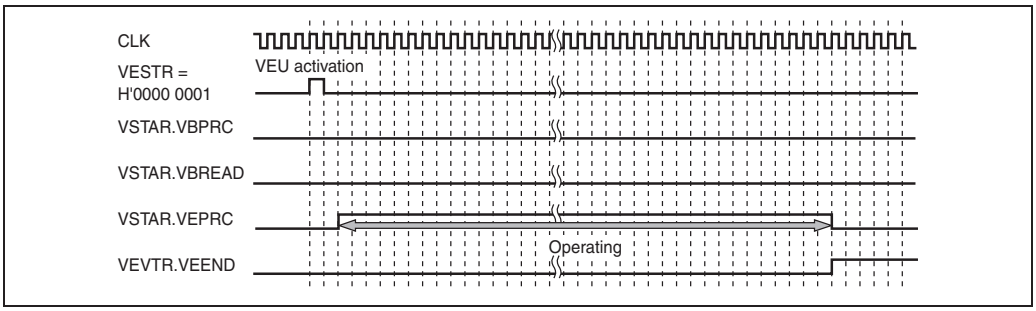


Figure 35.27 VSTAR State Transitions in Normal Operating Mode

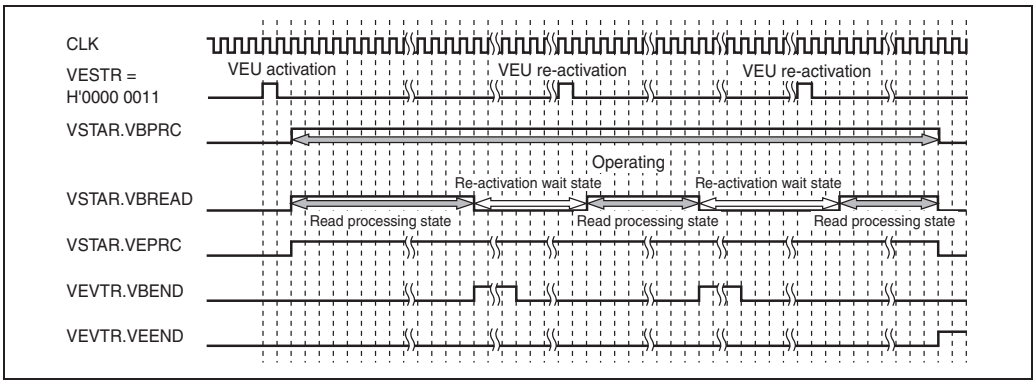


Figure 35.28 VSTAR State Transitions in Bundle Read Mode

35.3.27 VEU Module Reset Register (VBSRR)

VBSRR executes the module reset of the VEU.

Writing 1 to read-only bits is prohibited. If 1 is written to any of these bits, a malfunction may occur. Modifying this register during operation is prohibited.

If a module reset is performed during operation, the logic circuits handshaking with the CPU bus are forcibly reset, and malfunction may also affect modules other than the VEU. To correctly break the handshake with the CPU bus before VEU termination, see section 35.3.1, VEU Start Register (VESTR).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	ALL RST	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	ALLRST	0	W	Module Reset When 1 is written to this bit, all internal control signals of the VEU are reset. 0: Setting prohibited 1: Internal reset of the VEU
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

35.3.28 VEU Resize Passband Register (VRPBR)

VRPBR sets the signal passbands when scale-up/-down is performed. When this register is set, the VRFCR and VRFSR registers should be also set. Writing this register during operation is prohibited.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	VBW[6:0]						
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	HBW[6:0]						
Initial vlaue:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 23	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
22 to 16	VBW[6:0]	H'00	R/W	Sets the vertical signal passband when scaling-up/down.
15 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6 to 0	HBW[6:0]	H'00	R/W	Sets the horizontal signal passband when scaling-up/down.

When scaling up vertically (the VMNT bit in the VRFCR register is 0), set 64 in the VBW bit in the VRPBR register.

When scaling down vertically (the VMNT bit in the VRFCR register is other than 0), set a value obtained by the following formula in the VBW bit in the VRPBR register:

$$VSPBR.VBW = \left(64 \times \frac{4096 \times VMANTpre}{4096 \times VRFCR.VMNT + VRFCR.VFRC} \right)$$

Where VMANTpre is

4(8 ≤ VRFCR.VMNT<16)
2(4 ≤ VRFCR.VMNT<8)
1(1 ≤ VRFCR.VMNT<4)

Note that <A> is an operation that rounds value A down to the nearest integer.

When scaling up horizontally (the HMNT bit in the VRFCR register is 0), set 64 in the HBW bit in the VRPBR register.

When scaling down horizontally (the HMNT bit in the VRFCR register is other than 0), set a value obtained by the following formula in the HBW bit in the VRPBR register:

$$VSPBR.HBW = \left(64 \times \frac{4096 \times HMANTpre}{4096 \times VRFCR.HMNT + VRFCR.HFRC} \right)$$

Where HMANTpre is

4(8 ≤ VRFCR.HMNT<16)
2(4 ≤ VRFCR.HMNT<8)
1(1 ≤ VRFCR.HMNT<4)

Note that <A> is an operation that rounds value A down to the nearest integer.

35.3.29 VEU Resize interpolation setting register(VEUAD_RSZ_ITP)

VEUAD_RSZ_ITP sets the interpolation method when resizing images. However, it is possible to use it only with VEU2 and 3.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
				BLADV				ALP_TH_ON				ALP_ON				BC_ON
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				NE_ON_A				NE_ON_R				NE_ON_G				NE_ON_B
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28	BLADV	0	R/W	The interpolation accuracy in the bilinear / nearest neighbor interpolation is changed. The aliasing characteristic of 1/2~1/4 reduction processing is improved by this function. This set value is not effective following the expansion or 1/8 reductions(VVMNT[VHMNT]<=1 or VVMNT[VHMNT]>=8). 0: The bilinear /nearest neighbor interpolation enhancing is not done (initial value). 1: The bilinear /nearest neighbor interpolation enhancing is done
27 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	ALP_TH_ON	0		Enables or disables usage of threshold clipping for the alpha pixels. 0: The clipping is not done (initial value). 1: The clipping is done.
23 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	ALP_ON	0	R/W	Enables or disables usage of scaling-up/down for the alpha pixels. 0: The scaling is not done (initial value). 1: The scaling is done. Note: it is not possible to use it in a bicubic mode. Please use it as BC_ON=0.
19 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	BC_ON	0	R/W	Sets the bicubic interpolation when the scaling-up/down. 0: bilinear / nearest neighbor interpolation 1: bicubic interpolation(initial value)

15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	NE_ON_A	0	R/W	Sets the method of interpolating for alhpa when non-bicubic interpolation. 0: bilinear(initial value) 1: nearest neighbor*
11 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	NE_ON_R	0	R/W	Sets the method of interpolating for R/Cr when non-bicubic interpolation. 0: bilinear(initial value) 1: nearest neighbor*
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	NE_ON_G	0	R/W	Sets the method of interpolating for G/Y when non-bicubic interpolation. 0: bilinear(initial value) 1: nearest neighbor*
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	NE_ON_B	0	R/W	Sets the method of interpolating for B/Cb when non-bicubic interpolation. 0: bilinear(initial value) 1: nearest neighbor*

Note: * It is possible to use it at the expansion or 1/1~1/4 reductions.

35.3.30 VEU FIR Filter Horizontal Coefficient Register Y0 (VEUAD_FCOE_HY0)

VEUAD_FCOE_HY0 to VEUAD_FCOE_HY2 set the horizontal tap coefficients for the luminance (Y) component and G-pixel component of the FIR filter. The each coefficient is signed 8-bit data and the VHY5 is the center tap. Set the sum of tap coefficients to a 2's power and the shift value to a $\log_2$ (the sum of coefficients).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VHY0[7:0]								VHY1[7:0]							
Initial valude:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VHY2[7:0]								VHY3[7:0]							
Initial valude:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	VHY0[7:0]	H'00	R/W	Horizontal FIR filter tap coefficient 0 for luminance or G-pixel in RGB.
23 to 16	VHY1[7:0]	H'00	R/W	Horizontal FIR filter tap coefficient 1 for luminance or G-pixel in RGB.
15 to 8	VHY2[7:0]	H'00	R/W	Horizontal FIR filter tap coefficient 2 for luminance or G-pixel in RGB.
7 to 0	VHY3[7:0]	H'00	R/W	Horizontal FIR filter tap coefficient 3 for luminance or G-pixel in RGB.

35.3.31 VEU FIR Filter Horizontal Coefficient Register Y1 (VEUAD_FCOE_HY1)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VHY4[7:0]								VHY5[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VHY6[7:0]								VHY7[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	VHY4[7:0]	H'00	R/W	Horizontal FIR filter tap coefficient 4 for luminance or G-pixel in RGB.
23 to 16	VHY5[7:0]	H'01	R/W	Horizontal FIR filter tap coefficient 5 for luminance or G-pixel in RGB.
15 to 8	VHY6[7:0]	H'00	R/W	Horizontal FIR filter tap coefficient 6 for luminance or G-pixel in RGB.
7 to 0	VHY7[7:0]	H'00	R/W	Horizontal FIR filter tap coefficient 7 for luminance or G-pixel in RGB.

35.3.32 VEU FIR Filter Horizontal Coefficient Register Y2 (VEUAD_FCOE_HY2)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VHY8[7:0]								VHY9[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VHY10[7:0]												HYSFT[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	VHY8[7:0]	H'00	R/W	Horizontal FIR filter tap coefficient 8 for luminance or G-pixel in RGB.
23 to 16	VHY9[7:0]	H'01	R/W	Horizontal FIR filter tap coefficient 9 for luminance or G-pixel in RGB.
15 to 8	VHY10[7:0]	H'00	R/W	Horizontal FIR filter tap coefficient 10 for luminance or G-pixel in RGB.
3 to 0	HYSFT[3:0]	H'0	R/W	Horizontal FIR filter bit shift value for luminance or G-pixel in RGB.

35.3.33 VEU FIR Filter Horizontal Coefficient Register CB0 (VEUAD_FCOE_HCB0)

VEUAD_FCOE_HCB0 to VEUAD_FCOE_ HCB2 set the horizontal tap coefficients for the chrominance (Cb) component and B-pixel component of the FIR filter. The each coefficient is signed 8-bit data and the VHU5 is the center tap. Set the sum of tap coefficients to a 2's power and the shift value to a $\log_2$ (the sum of coefficients).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VHU0[7:0]								VHU1[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VHU2[7:0]								VHU3[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	VHU0[7:0]	H'00	R/W	Horizontal FIR filter tap coefficient 0 for chrominance (Cb) component or B-pixel in RGB.
23 to 16	VHU1[7:0]	H'00	R/W	Horizontal FIR filter tap coefficient 1 for chrominance (Cb) component or B-pixel in RGB.
15 to 8	VHU2[7:0]	H'00	R/W	Horizontal FIR filter tap coefficient 2 for chrominance (Cb) component or B-pixel in RGB.
7 to 0	VHU3[7:0]	H'00	R/W	Horizontal FIR filter tap coefficient 3 for chrominance (Cb) component or B-pixel in RGB.

35.3.34 VEU FIR Filter Horizontal Coefficient Register CB1 (VEUAD_FCOE_HCB1)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VHU4[7:0]								VHU5[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VHU6[7:0]								VHU7[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	VHU4[7:0]	H'00	R/W	Horizontal FIR filter tap coefficient 4 for chrominance (Cb) component or B-pixel in RGB.
23 to 16	VHU5[7:0]	H'01	R/W	Horizontal FIR filter tap coefficient 5 for chrominance (Cb) component or B-pixel in RGB.
15 to 8	VHU6[7:0]	H'00	R/W	Horizontal FIR filter tap coefficient 6 for chrominance (Cb) component or B-pixel in RGB.
7 to 0	VHU7[7:0]	H'00	R/W	Horizontal FIR filter tap coefficient 7 for chrominance (Cb) component or B-pixel in RGB.

35.3.35 VEU FIR Filter Horizontal Coefficient Register CB2 (VEUAD_FCOE_HCB2)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VHU8[7:0]								VHU9[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VHU10[7:0]												HUSFT[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	VHU8[7:0]	H'00	R/W	Horizontal FIR filter tap coefficient 8 for chrominance (Cb) component or B-pixel in RGB.
23 to 16	VHU9[7:0]	H'01	R/W	Horizontal FIR filter tap coefficient 9 for chrominance (Cb) component or B-pixel in RGB.
15 to 8	VHU10[7:0]	H'00	R/W	Horizontal FIR filter tap coefficient 10 for chrominance (Cb) component or B-pixel in RGB.
3 to 0	HUSFT[3:0]	H'0	R/W	Horizontal FIR filter bit shift value for chrominance (Cb) component or B-pixel in RGB.

35.3.36 VEU FIR Filter Horizontal Coefficient Register CR0 (VEUAD_FCOE_HCR0)

VEUAD_FCOE_CR0 to VEUAD_FCOE_CR2 set the horizontal tap coefficients for the luminance (Cr) component and R-pixel component of the FIR filter. The each coefficient is signed 8-bit data and the VHV5 is the center tap. Set the sum of tap coefficients to a 2's power and the shift value to a $\log_2$ (the sum of coefficients).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VHV0[7:0]								VHV1[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VHV2[7:0]								VHV3[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	VHV0[7:0]	H'00	R/W	Horizontal FIR filter tap coefficient 0 for chrominance (Cr) component or R-pixel in RGB.
23 to 16	VHV1[7:0]	H'00	R/W	Horizontal FIR filter tap coefficient 1 for chrominance (Cr) component or R-pixel in RGB.
15 to 8	VHV2[7:0]	H'00	R/W	Horizontal FIR filter tap coefficient 2 for chrominance (Cr) component or R-pixel in RGB.
7 to 0	VHV3[7:0]	H'00	R/W	Horizontal FIR filter tap coefficient 3 for chrominance (Cr) component or R-pixel in RGB.

35.3.37 VEU FIR Filter Horizontal Coefficient Register CR1 (VEUAD_FCOE_HCR1)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VHV4[7:0]								VHV5[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VHV6[7:0]								VHV7[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	VHV4[7:0]	H'00	R/W	Horizontal FIR filter tap coefficient 4 for chrominance (Cr) component or R-pixel in RGB.
23 to 16	VHV5[7:0]	H'01	R/W	Horizontal FIR filter tap coefficient 5 for chrominance (Cr) component or R-pixel in RGB.
15 to 8	VHV6[7:0]	H'00	R/W	Horizontal FIR filter tap coefficient 6 for chrominance (Cr) component or R-pixel in RGB.
7 to 0	VHV7[7:0]	H'00	R/W	Horizontal FIR filter tap coefficient 7 for chrominance (Cr) component or R-pixel in RGB.

35.3.38 VEU FIR Filter Horizontal Coefficient Register CR2 (VEUAD_FCOE_HCR2)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VHV8[7:0]								VHV9[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VHV10[7:0]												HVSFT[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	VHV8[7:0]	H'00	R/W	Horizontal FIR filter tap coefficient 8 for chrominance (Cr) component or R-pixel in RGB.
23 to 16	VHV9[7:0]	H'01	R/W	Horizontal FIR filter tap coefficient 9 for chrominance (Cr) component or R-pixel in RGB.
15 to 8	VHV10[7:0]	H'00	R/W	Horizontal FIR filter tap coefficient 10 for chrominance (Cr) component or R-pixel in RGB.
3 to 0	HVSFT[3:0]	H'0	R/W	Horizontal FIR filter bit shift value for chrominance (Cr) component or R-pixel in RGB.

35.3.39 VEU FIR Filter Vertical Coefficient Register Y0 (VEUAD_FCOE_VY0)

VEUAD_FCOE_VY0 to VEUAD_FCOE_VY2 set the horizontal tap coefficients for the luminance (Y) component and G-pixel component of the FIR filter. The each coefficient is signed 8-bit data and the VVY5 is the center tap. Set the sum of tap coefficients to a 2's power and the shift value to a $\log_2$ (the sum of coefficients).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VVY0[7:0]								VVY1[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VVY2[7:0]								VVY3[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	VVY0[7:0]	H'00	R/W	Vertical FIR filter tap coefficient 0 for luminance or G-pixel in RGB.
23 to 16	VVY1[7:0]	H'00	R/W	Vertical FIR filter tap coefficient 1 for luminance or G-pixel in RGB.
15 to 8	VVY2[7:0]	H'00	R/W	Vertical FIR filter tap coefficient 2 for luminance or G-pixel in RGB.
7 to 0	VVY3[7:0]	H'00	R/W	Vertical FIR filter tap coefficient 3 for luminance or G-pixel in RGB.

35.3.40 VEU FIR Filter Vertical Coefficient Register Y1 (VEUAD_FCOE_VY1)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VVY4[7:0]								VVY5[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VVY6[7:0]								VVY7[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	VVY4[7:0]	H'00	R/W	Vertical FIR filter tap coefficient 4 for luminance or G-pixel in RGB.
23 to 16	VVY5[7:0]	H'01	R/W	Vertical FIR filter tap coefficient 5 for luminance or G-pixel in RGB.
15 to 8	VVY6[7:0]	H'00	R/W	Vertical FIR filter tap coefficient 6 for luminance or G-pixel in RGB.
7 to 0	VVY7[7:0]	H'00	R/W	Vertical FIR filter tap coefficient 7 for luminance or G-pixel in RGB.

35.3.41 VEU FIR Filter Vertical Coefficient Register Y2 (VEUAD_FCOE_VY2)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VVY8[7:0]								VVY9[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VVY10[7:0]												VYSFT[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	VVY8[7:0]	H'00	R/W	Vertical FIR filter tap coefficient 8 for luminance or G-pixel in RGB.
23 to 16	VVY9[7:0]	H'01	R/W	Vertical FIR filter tap coefficient 9 for luminance or G-pixel in RGB.
15 to 8	VVY10[7:0]	H'00	R/W	Vertical FIR filter tap coefficient 10 for luminance or G-pixel in RGB.
3 to 0	VYSFT[3:0]	H'0	R/W	Vertical FIR filter bit shift value for luminance or G-pixel in RGB.

35.3.42 VEU FIR Filter Vertical Coefficient Register CB0 (VEUAD_FCOE_VCB0)

VEUAD_FCOE_VCB0 to VEUAD_FCOE_ VCB2 set the horizontal tap coefficients for the chrominance (Cb) component and B-pixel component of the FIR filter. The each coefficient is signed 8-bit data and the VVU5 is the center tap. Set the sum of tap coefficients to a 2's power and the shift value to a $\log_2$ (the sum of coefficients).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VVU0[7:0]								VVU1[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VVU2[7:0]								VVU3[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	VVU0[7:0]	H'00	R/W	Vertical FIR filter tap coefficient 0 for chrominance (Cb) component or B-pixel in RGB.
23 to 16	VVU1[7:0]	H'00	R/W	Vertical FIR filter tap coefficient 1 for chrominance (Cb) component or B-pixel in RGB.
15 to 8	VVU2[7:0]	H'00	R/W	Vertical FIR filter tap coefficient 2 for chrominance (Cb) component or B-pixel in RGB.
7 to 0	VVU3[7:0]	H'00	R/W	Vertical FIR filter tap coefficient 3 for chrominance (Cb) component or B-pixel in RGB.

35.3.43 VEU FIR Filter Vertical Coefficient Register CB1 (VEUAD_FCOE_VCB1)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VVU4[7:0]								VVU5[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VVU6[7:0]								VVU7[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	VVU4[7:0]	H'00	R/W	Vertical FIR filter tap coefficient 4 for chrominance (Cb) component or B-pixel in RGB.
23 to 16	VVU5[7:0]	H'01	R/W	Vertical FIR filter tap coefficient 5 for chrominance (Cb) component or B-pixel in RGB.
15 to 8	VVU6[7:0]	H'00	R/W	Vertical FIR filter tap coefficient 6 for chrominance (Cb) component or B-pixel in RGB.
7 to 0	VVU7[7:0]	H'00	R/W	Vertical FIR filter tap coefficient 7 for chrominance (Cb) component or B-pixel in RGB.

35.3.44 VEU FIR Filter Vertical Coefficient Register CB2 (VEUAD_FCOE_VCB2)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VVU8[7:0]								VVU9[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VVU10[7:0]												VUSFT[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	VVU8[7:0]	H'00	R/W	Vertical FIR filter tap coefficient 8 for chrominance (Cb) component or B-pixel in RGB.
23 to 16	VVU9[7:0]	H'01	R/W	Vertical FIR filter tap coefficient 9 for chrominance (Cb) component or B-pixel in RGB.
15 to 8	VVU10[7:0]	H'00	R/W	Vertical FIR filter tap coefficient 10 for chrominance (Cb) component or B-pixel in RGB.
3 to 0	VUSFT[3:0]	H'0	R/W	Vertical FIR filter bit shift value for chrominance (Cb) component or B-pixel in RGB.

35.3.45 VEU FIR Filter Vertical Coefficient Register CR0 (VEUAD_FCOE_VCR0)

VEUAD_FCOE_CR0 to VEUAD_FCOE_CR2 set the vertical tap coefficients for the luminance (Cr) component and R-pixel component of the FIR filter. The each coefficient is signed 8-bit data and the VVV5 is the center tap. Set the sum of tap coefficients to a 2's power and the shift value to a $\log_2$ (the sum of coefficients).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VVV0[7:0]								VVV1[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VVV2[7:0]								VVV3[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	VVV0[7:0]	H'00	R/W	Vertical FIR filter tap coefficient 0 for chrominance (Cr) component or R-pixel in RGB.
23 to 16	VVV1[7:0]	H'00	R/W	Vertical FIR filter tap coefficient 1 for chrominance (Cr) component or R-pixel in RGB.
15 to 8	VVV2[7:0]	H'00	R/W	Vertical FIR filter tap coefficient 2 for chrominance (Cr) component or R-pixel in RGB.
7 to 0	VVV3[7:0]	H'00	R/W	Vertical FIR filter tap coefficient 3 for chrominance (Cr) component or R-pixel in RGB.

35.3.46 VEU FIR Filter Vertical Coefficient Register CR1 (VEUAD_FCOE_VCR1)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VVV4[7:0]								VVV5[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VVV6[7:0]								VVV7[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	VVV4[7:0]	H'00	R/W	Vertical FIR filter tap coefficient 4 for chrominance (Cr) component or R-pixel in RGB.
23 to 16	VVV5[7:0]	H'01	R/W	Vertical FIR filter tap coefficient 5 for chrominance (Cr) component or R-pixel in RGB.
15 to 8	VVV6[7:0]	H'00	R/W	Vertical FIR filter tap coefficient 6 for chrominance (Cr) component or R-pixel in RGB.
7 to 0	VVV7[7:0]	H'00	R/W	Vertical FIR filter tap coefficient 7 for chrominance (Cr) component or R-pixel in RGB.

35.3.47 VEU FIR Filter Vertical Coefficient Register CR2 (VEUAD_FCOE_VCR2)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VVV8[7:0]								VVV9[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VVV10[7:0]												VVSFT[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	VVV8[7:0]	H'00	R/W	Vertical FIR filter tap coefficient 8 for chrominance (Cr) component or R-pixel in RGB.
23 to 16	VVV9[7:0]	H'01	R/W	Vertical FIR filter tap coefficient 9 for chrominance (Cr) component or R-pixel in RGB.
15 to 8	VVV10[7:0]	H'00	R/W	Vertical FIR filter tap coefficient 120 for chrominance (Cr) component or R-pixel in RGB.
3 to 0	HVSFT[3:0]	H'0	R/W	Vertical FIR filter bit shift value for chrominance (Cr) component or R-pixel in RGB.

35.3.48 VEU FIR Filter Calculation Optional Setting Register (VEUAD_FSWT)

VEUAD_FSWT performs the optional settings for the FIR filter calculation. This register specifies a rounding selection and a sign-extended for the chrominance data in shifting bits.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
												LPF_COEF_ON				CSGNOF
Initial valude:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								RCV				RCU				RCY
Initial valude:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved
20	LPF_COEF_ON	1	R/W	FIR filter input coefficient specification register The coefficient input to the FIR filter is selected. 0: FIR registers（VEUADx_FCOE_HY0~HCR2、VEUADx_FCOE_VY0~VCR2） 1: LPF registers (VVTCR,VHTCR：initial value)
19 to 17	—	All 0	R	Reserved
16	CSGNOF	1	R/W	Chrominance Signed Bit Extension Option 0: Bit is sign-extended 1: Bit is not sign-extended* (initial value)
15 to 9	—	All 0	R	Reserved
8	RCV	0	R/W	Rounding Specifications for Chrominance (Cr) Component or R-pixel in RGB 0: Round down (initial value) 1: Round up
7 to 5	—	All 0	R	Reserved
4	RCU	0	R/W	Rounding Specifications for Chrominance (Cb) Component or B-pixel in RGB 0: Round down (initial value) 1: Round up
3 to 1	—	All 0	R	Reserved
0	RCY	0	R/W	Rounding Specifications for luminance or G-pixel in RGB 0: Round down (initial value) 1: Round up

Note: * Not to be specified when the coefficient specified for the FIR filter is a negative value. This can be used only when all the coefficients are positive.

35.3.49 VEU Alpha Resize Clip Threshold Setting Register (VEUAD_ALPTH)

VEUAD_ALPTH sets the threshold to pixel value after the alpha is resized and replaces pixel value according to the VEUAD_ALPVAL register value. However, it is possible to use it only with VEU2 and 3.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ALP_TH1								ALP_TH0							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 8	ALP_TH1	H'00	R/W	Alpha threshold setting register 1 When pixel value is ALP_TH1 or more, the pixel is replaced with VEUAD_ALPVAL.ALP_VAL2.
7 to 0	ALP_TH0	H'00	R/W	Alpha threshold setting register 0 When pixel value is ALP_TH0 or less, the pixel is replaced with VEUAD_ALPVAL.ALP_VAL0.

35.3.50 VEU Alpha Resize Clip Value Setting Register (VEUAD_ALPVAL)

VEUAD_ALPVAL specifies pixel value replaced when pixel value after α is resized exceeds (falls below) the threshold. It becomes effective only at VEUAD_RSZ_ITP.ALP_TH_ON=1. However, it is possible to use it only with VEU2 and 3.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
									ALP_VAL2							
Initial valude:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R /W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ALP_VAL1								ALP_VAL0							
Initial valude:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R /W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 16	ALP_VAL2	H'00	R/W	Alpha clip value setting register 2 Sets the pixel replaced value, when pixel value is VEUAD_ALPTH.ALP_TH1 or more.
15 to 8	ALP_VAL1	H'00	R/W	Alpha clip value setting register 1
7 to 0	ALP_VAL0	H'00	R/W	Alpha clip value setting register 0 Sets the pixel replaced value, when pixel value is VEUAD_ALPTH.ALP_TH0 or less.

35.4 Usage Notes for VEU

(1) Restrictions during Operation

Do not halt the clock or module during VEU operation.

(2) Restrictions on Input/Output Functions

Note that when restrictions at other places in this manual differ from restrictions in the following table, restrictions in the following table are given priority.

Table 35.18 Restrictions on VEU Input/Output Functions

Item	Pack Type	Restrictions
Input	RGB565, 4 bytes/pixel	• The start address for input must be specified in longword units. • The horizontal size of the raw image (memory) must be specified in byte units that correspond to two pixels of the source image.
	Others	• The start address for input must be specified in longword units. However, when the RGB stuffing pack is input, the address must be specified so that reading starts from the pack of phase 0. • The horizontal size of the raw image (memory) must be specified in byte units that correspond to four pixels of the destination image.
Output	RGB565 4 bytes/pixel	• The output address must be specified in longword units. • The horizontal size of the destination image (memory) must be specified in byte units that correspond to two pixels of the destination image.
	Others	• The output address must be specified in longword units. • The horizontal size of the destination image (memory) must be specified in byte units that correspond to four pixels of the destination image.

(3) Data alignment restriction

In the line processing of VEU, data is accessed by 8 byte alignment. Therefore, the byte in the image terminal might be exceeded and it access it. However, when data is output, extra four bytes are not written because masking is word enable it done. There is a similar 8 byte alignment restriction in the block processing of the rotation operation etc.

Reading of the data of the line processing rounds up in four pixels and is read. Please note that the address in the horizontal terminal is different according to the format.

(4) Input access area in block processing

There is a possibility of accessing it exceeding the horizontal input data area when the block processing is done. This extra bytes differs according to the format, and is shown in the following table. In the block processing, please reserve this extra bytes in addition to the input image area.

Format	Number of excess access bytes from inputting the horizontal edge (maximum)
YUV：Y image	12 bytes
YUV：C image(422/420)	12 bytes
YUV：C image(444)	20 bytes
RGB565	50 bytes
RGB0888(8880)	96 bytes
RGB24/BGR24	73 bytes

Section 36 Blend Engine Unit (BEU)

36.1 Features

The BEU is a module used connected to the buses via bus bridge modules. The BEU blends three displays, supports some function as follow

- Supports video display.
- Supports OSD (On-Screen Display).
- Supports graphic display.
- The three displays can be blended at desired positions.
- Any one of the three inputs can be used as the parent display.
- The location of a child display can overflow from the parent display, but the overflowed area is not output.

36.1.1 Functional Overview

The functional overview of the BEU is shown in the table 36.1

Table 36.1 Functional Overview of BEU

Classification	Item	Function	Description	Note
Input format	YCbCr format	YCbCr 4:4:4/4:2:2/4:2:0 αYCbCr 4:4:4/4:2:2/4:2:0	α, Y, and C are input from separate planes. For YCbCr 4:2:0, the vertical line is read twice.	With input system 1, conversion is possible for RGB/YCbCr
	RGB format	RGB pack alpha RGB pack alpha plane + RGB pack		
Output format	YCbCr format	YCbCr 4:4:4/4:2:2/4:2:0	Y and C are output to separate planes	With output, conversion is possible for RGB/YCbCr
	RGB format	RGB pack alpha RGB pack		
Source/ destination image size	Maximum	4092 × 4092	YCbCr420: 2-pixel units both horizontally and vertically YCbCr422: 2-pixel units horizontally In other formats 1-pixel units can be specified.	
	Minimum	4 × 4 pixels : parent display 1 × 1 pixels : child display		
Dithering (tone reduction)	RGB decrease color	18, 24bpp: dithering not possible		
		8, 12, 16bpp : dithering possible		
Blending	Blend source	three displays from image memory		• Any of the three inputs can be used as the parent display. • The three displays can be blended at desired locations. • Overflow from the parent display area is allowed, but the overflowed area is not output. • The tile pattern can be blended.
	Select the alpha of input	pixel alpha, fixed alpha, alpha plane		
	alpha blend	8, 1bpp(RGB only)		
OSD	Data format	8 bpp	It is possible to select 256 color of full color	Input 3 possible only
	CLUT size	32-bit αRGB 32-bit αYCbCr		
Color key	Color replace	Compare data: RGB, Y Replace date: α RGB, α Y	α and RGB/Y data replacement	The three input are possible
	transparency color	Compare data: α RGB, α Y Replace data: α	Replace α data only	
Color space conversion	compliant color space	ITU-R BT.601 ITU-R BT.709	The conversion is possible as follows RGB<->BT.601 RGB<->BT.709	With input system 1 and output systerm, conversion is possible
Display data output	Destination setting	Output system + write back to memory		

36.1.2 Module Block

Figure 36.1 is block diagram of BEU respectively. BEU is composed of bus interface (Bus I/F) to LMB (Local Media Bridge) and input pixel format converter (RPF) in three input systems, blend processing part (Blend Core), outputpixel format converter (WPF).

Input pixel format converter (RPF) in three systems is read the image data from each plane imager through the bus interface, converts those different formats of three systems into the same format so that it may be possible to process internal.

Blend core inputs three image data that converted into the same format by RPF, and blends those images. The resultion of blend processing is input to output pixel format converter (WPF). It is converted the format to be stored in output plane image. The image data that the format conversion is done is stored in output plane through the bus interface.

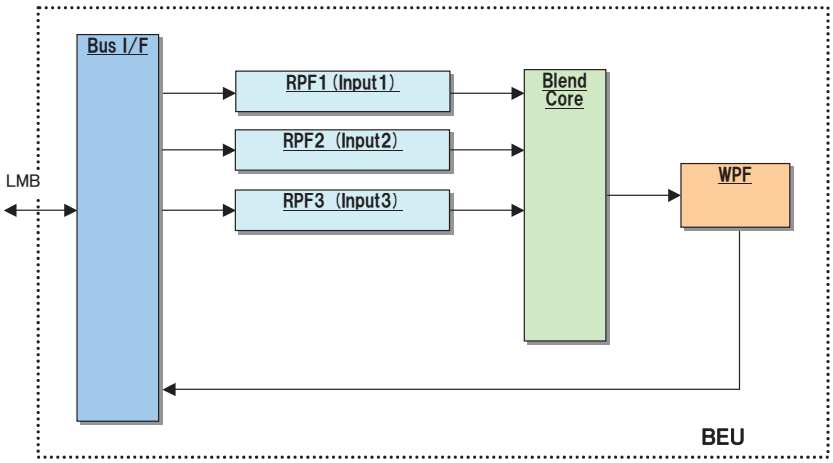


Figure 36.1 Block Diagram of BEU

Function explanation
Bus I/F : bus interface
RPF1~3: input pixel format converter
Blend Core : blend process
WPF : output pixel format converter
LMB : local media bridge

Figure 36.2 is shown the block diagram of input pixel format converter (RPF). RPF is composed of the input format development (de-packing unit), index color development (OSD-CLUT unit) Color key unit, color space converter and dither unit.

The de-packing unit and OSD-CLUT unit progress the image data input from the bus interface to the image format of internal processing.

Color key unit specifies the color substitution and the penetration color for the image data input from the output selecter of De-packing unit and OSD-CLUT.

Color space converter does the color space conversion of RGB-YCbCr to the image data input from Color Key if necessary, and processes the dither to the output image in Dither unit according to the output image format.

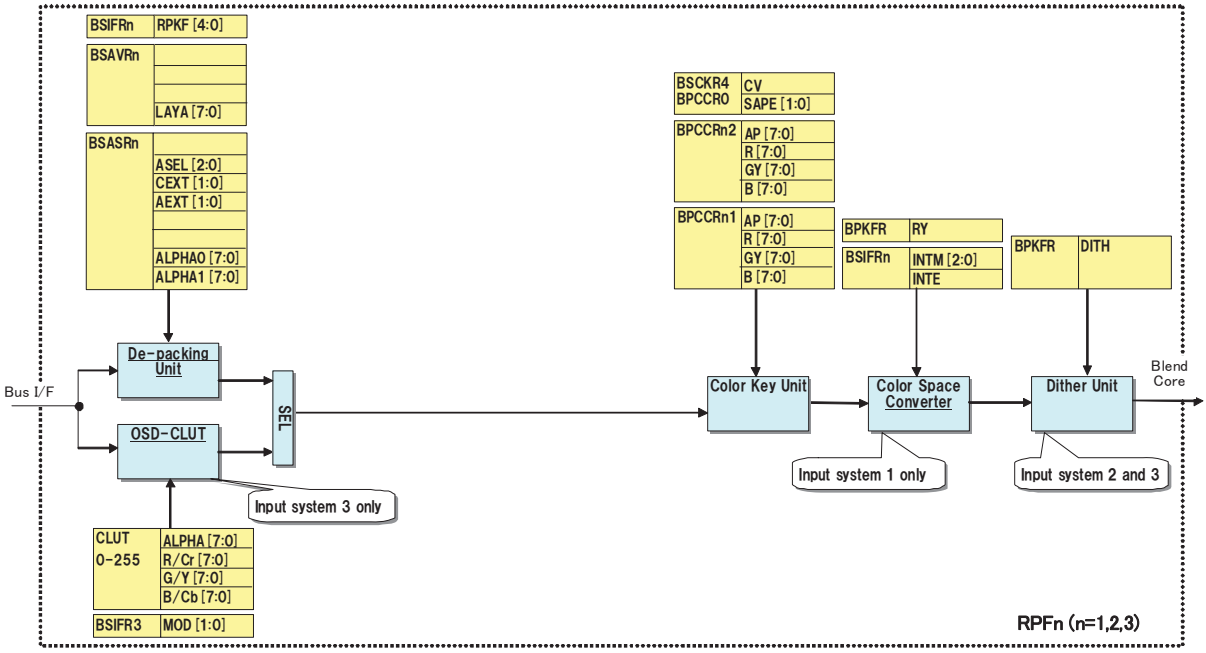


Figure 36.2 BEU-RPF block diagram

Function explanation
De-packing Unit : input format development
OSD-CLUT : index color developent
Color Key Unit : color key processing (color substitution, penetration color)
Color Space Converter : color space converter processing
Dither Unit : dither processing
SEL : the selecter of De-packing Unit and OSD-CLUT
The image data is composed of alpha data and color data (RGB/YCbCr).

Figure 36.3 is shown the block diagram of Blend Core. Blend Core is composed of two blend units (Blend Unit-m, m=A, C) and input switch container (SEL) of those blend unit.

Two blend units operate the image blending that connects each input with SEL and the out of Blend Unit-m.

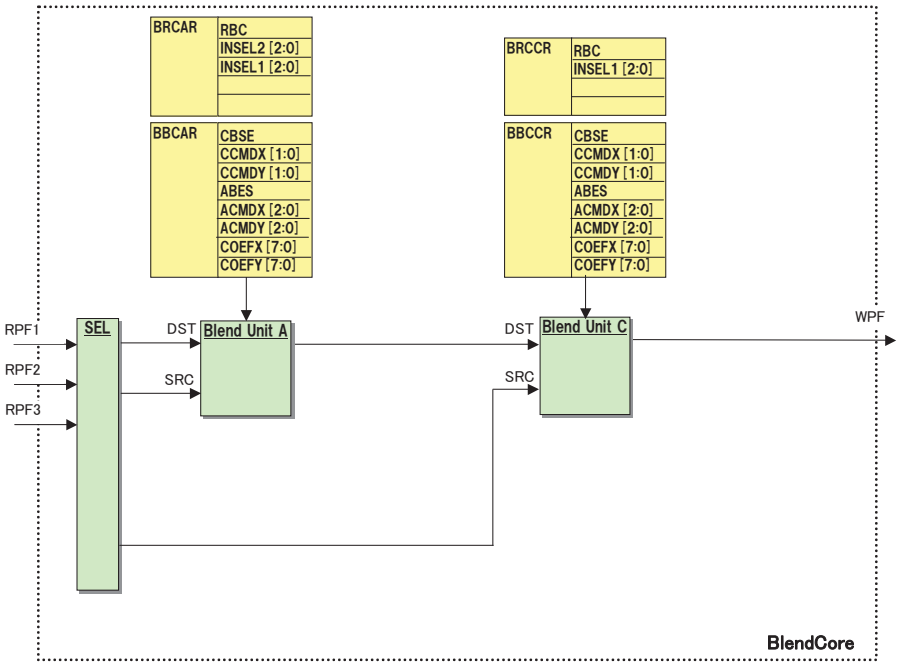


figure 36.3 Block diagram of Blend Core

Function explanation
Blend Unit-m : blend operater
SEL : the selecter of blend operater

Figure 36.4 is shown the block diagram of output pixel format converter (WPF). WPF is composed of color space converter and output format converter (Packing Unit).

Color space converter operates the conversion for RGB-YCbCr. Packing Unit operates the format conversion according to the format that stored in image plane.

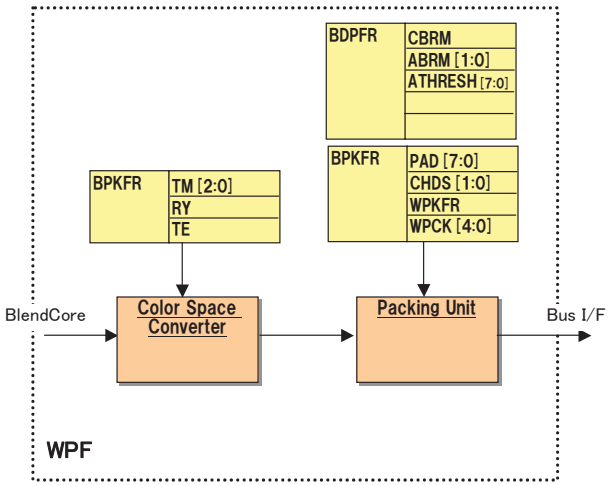


figure 36.4 Block diagram of WPF

Function explanation
Color space converter : color space converter unit
Packing unit : output format converter unit

36.2 Description of BEU Registers

36.2.1 Description of BEU Registers

Table 36.2 is shown the description of BEU registers. Most of BEU registers have a 2-side configuration (side A, side B). The register incorporated in the BEU consists of two sides registers. An incorporated register with tow sides of registers has a mirror address to access the register set not currently being used.

This LSI has three BEU. The address of BEU1, BEU2 and BEU3 register is allocated as follows.

- BEU1 : H'FE93_0000 ~ H'FE93_3FFF
- BEU2 : H'FE93_4000 ~ H'FE93_7FFF
- BEU3 : H'FE93_8000 ~ H'FE93_BFFF

Table 36.2 is shown the BEU1 register.

Table 36.2 BEU Register Configurations

			Addresses			
Register Name	Symbol	R/W	Address (A side)	Address (B side)	Mirror Address	Access size
Start/stop register	BESTR	R/W	H'FE93_0000	—	—	32
Input 1:source image memory width	BSMWR1	R/W	H'FE93_0010	H'FE93_1010	H'FE93_2010	32
Input 1:source image size	BSSZR1	R/W	H'FE93_0014	H'FE93_1014	H'FE93_2014	32
Input 1:source image Y/RGB start address	BSAYR1	R/W	H'FE93_0018	H'FE93_1018	H'FE93_2018	32
Input 1:source image Cb/Cr start address	BSACR1	R/W	H'FE93_001C	H'FE93_101C	H'FE93_201C	32
Input 1:source image α start address	BSAAR1	R/W	H'FE93_0020	H'FE93_1020	H'FE93_2020	32
Input 1:source image format	BSIFR1	R/W	H'FE93_0024	H'FE93_1024	H'FE93_2024	32
Input 2:source image memory width	BSMWR2	R/W	H'FE93_0028	H'FE93_1028	H'FE93_2028	32
Input 2:source image size	BSSZR2	R/W	H'FE93_002C	H'FE93_102C	H'FE93_202C	32
Input 2:source image Y/RGB start address	BSAYR2	R/W	H'FE93_0030	H'FE93_1030	H'FE93_2030	32
Input 2:source image Cb/Cr start address	BSACR2	R/W	H'FE93_0034	H'FE93_1034	H'FE93_2034	32
Input 2:source image α start address	BSAAR2	R/W	H'FE93_0038	H'FE93_1038	H'FE93_2038	32
Input 2:source image format	BSIFR2	R/W	H'FE93_003C	H'FE93_103C	H'FE93_203C	32
Input 3:source image memory width	BSMWR3	R/W	H'FE93_0040	H'FE93_1040	H'FE93_2040	32
Input 3:source image size	BSSZR3	R/W	H'FE93_0044	H'FE93_1044	H'FE93_2044	32

Register Name	Symbol	R/W	Addresses Address (A side)	Address (B side)	Mirror Address	Access size
Input 3 : source image Y/RGB start address	BSAYR3	R/W	H'FE93_0048	H'FE93_1048	H'FE93_2048	32
Input 3 : source image Cb/Cr start address	BSACR3	R/W	H'FE93_004C	H'FE93_104C	H'FE93_204C	32
Input 3 : source image α start address	BSAAR3	R/W	H'FE93_0050	H'FE93_1050	H'FE93_2050	32
Input 3 : source image format	BSIFR3	R/W	H'FE93_0054	H'FE93_1054	H'FE93_2054	32
Tile pattern output size	BTPSR	R/W	H'FE93_0058	H'FE93_1058	H'FE93_2058	32
Blend control	BBLCR1	R/W	H'FE93_0104	—	—	32
Input 1 : blend location	BLOCR1	R/W	H'FE93_0114	H'FE93_1114	H'FE93_2114	32
Input 2 : blend location	BLOCR2	R/W	H'FE93_0118	H'FE93_1118	H'FE93_2118	32
Input 3 : blend location	BLOCR3	R/W	H'FE93_011C	H'FE93_111C	H'FE93_211C	32
BEU output format	BPKFR	R/W	H'FE93_0140	H'FE93_1140	H'FE93_2140	32
Transparency color control	BPCCR0	R/W	H'FE93_0144	H'FE93_1144	H'FE93_2144	32
Input 1 : transparency color control register 1	BPCCR11	R/W	H'FE93_0148	H'FE93_1148	H'FE93_2148	32
Input 1 : transparency color control register 2	BPCCR12	R/W	H'FE93_014C	H'FE93_114C	H'FE93_214C	32
Input 2 : transparency color control register 1	BPCCR21	R/W	H'FE93_0150	H'FE93_1150	H'FE93_2150	32
Input 2 : transparency color control register 2	BPCCR22	R/W	H'FE93_0154	H'FE93_1154	H'FE93_2154	32
Input 3 : transparency color control register 1	BPCCR31	R/W	H'FE93_0158	H'FE93_1158	H'FE93_2158	32
Input 3 : transparency color control register 2	BPCCR32	R/W	H'FE93_015C	H'FE93_115C	H'FE93_215C	32
Destination memory width	BDMWR	R/W	H'FE93_0160	H'FE93_1160	H'FE93_2160	32
Destination image Y/RGB start address	BDAYR	R/W	H'FE93_0164	H'FE93_1164	H'FE93_2164	32
Destination image Cb/Cr start address	BDACR	R/W	H'FE93_0168	H'FE93_1168	H'FE93_2168	32
Destination image format	BDPFR	R/W	H'FE93_016C	H'FE93_116C	H'FE93_216C	32
Address fixed	BAFXR	R/W	H'FE93_0180	H'FE93_1180	H'FE93_2180	32
Data swapping control	BSWPR	R/W	H'FE93_0184	H'FE93_1184	H'FE93_2184	32
Event interrupt control	BEIER	R/W	H'FE93_0188	—	—	32
Event flag and clear	BEVTR	R/W	H'FE93_018C	—	—	32
Register side control	BRCNTR	R/W	H'FE93_0194	—	—	32
Status register	BSTAR	R/W	H'FE93_0198	—	—	32

Register Name	Symbol	R/W	Addresses Address (A side)	Address (B side)	Mirror Address	Access size
Module reset register	BBRSTR	R/W	H'FE93_019C	—	—	32
Register side forcible setting	BRCHR	R/W	H'FE93_01A0	—	—	32
Input 1 : source image α control	BSASR1	R/W	H'FE93_0224	H'FE93_1224	H'FE93_2224	32
Input 1 : source image α value set	BSAVR1	R/W	H'FE93_0228	H'FE93_1228	H'FE93_2228	32
Input 2 : source image α control	BSASR2	R/W	H'FE93_0264	H'FE93_1264	H'FE93_2264	32
input2 : source image α value set	BSAVR2	R/W	H'FE93_0268	H'FE93_1268	H'FE93_2268	32
Input 3 : source image α control	BSASR3	R/W	H'FE93_02A4	H'FE93_12A4	H'FE93_22A4	32
Input 3 : source image α value set	BSAVR3	R/W	H'FE93_02A8	H'FE93_12A8	H'FE93_22A8	32
Blend Unit-A : ROP control	BRCAR	R/W	H'FE93_0350	H'FE93_1350	H'FE93_2350	32
Blend Unit-A : Blend control	BBCAR	R/W	H'FE93_0354	H'FE93_1354	H'FE93_2354	32
Blend Unit-C : ROP control	BRCCR	R/W	H'FE93_0370	H'FE93_1370	H'FE93_2370	32
Blend Unit-C : Blend control	BBCCR	R/W	H'FE93_0374	H'FE93_1374	H'FE93_2374	32
The CLUT area is used on OSD	CLUT	R/W	H'FE93_3000 ↓ H'FE93_33FF	—	—	32

36.2.2 Register explanation

In the following, it explains the register of BEU.

- For the read-only bits in all BEU registers and the reserved areas, writing 1 is prohibited. Do not specify an unallowable value.
- Most BEU registers have a 2-side configuration (side A, side B). For registers (bit) to which writing during operation is prohibited, do not modify them during operation (reading is possible). The BEU operating state can be confirmed by reading the BEPRC bit in the BEU status register (BSTAR). Modify the above registers when this bit is B'0. When a mirror address is written to for a 2-side register, the register on the unused side is always accessed. To directly write to side A or side B, prohibit writing to the plane currently used.

There is a possibility of the operation failure when the above-mentioned register operation is not guaranteed.

The terms used in this section are described below.

- "forcible termination" or "software reset" indicates that the BEU2 processing was forcibly terminated. In this case, the current processing is stopped but hardware terminates normally. The image processing result of the frame in which a software reset occurs is not guaranteed.
- "module reset" indicates the BEU internal circuit was forcibly reset. In a module reset, reset processing is performed with no consideration to the hardware state. Therefore, if a module reset is generated when the BEU is operating normally, the BEU peripheral hardware may become unable to operate.
- "during operation" in this section indicates a state in which the BEPRC bit in the BEU status register (BSTAR) is set to B'1.
- When a bit name in a register is referred to in this section, it is indicated in the format of (register name).(bit name). Example: BESTR.BEIVK

36.2.3 BEU Start Register (BESTR)

BESTR activates and halts the BEU, and enables or disables input displays. Before activating the BEU, all registers that specify the operating parameters, except for this register, must be set.

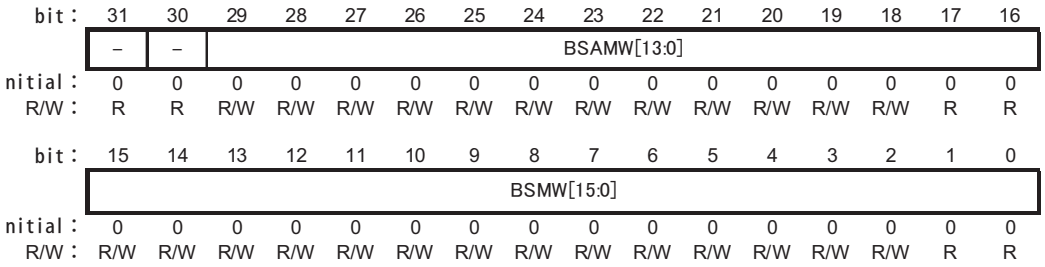
bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	CHON3	CHON2	CHON1	–	–	–	–	–	–	–	BEIVK
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10	CHON3	0	R/W	Each bit specifies whether the corresponding input system is used or not. 1 must be written to the bit corresponding to the input system selected as the parent display by the PWD bits in BBLCR1. If the parent display is set not to be used, the BEVIO bit in BEVTR is set to 1 immediately after the BEU is activated, and processing is halted. CHONn (n = 1 to 3) 0: Input system n is not used. 1: Input system n is used.
9	CHON2	0	R/W	
8	CHON1	0	R/W	
7 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	BEIVK	0	R/W	Controls the start and stop of BEU processing. If 1 is written to this bit when the BEU is halted, the BEPRC bit in BSTAR is set to 1 and blending starts. In addition, if 0 is written to this bit when the BEU is in the operating state (BEPRC bit = 1), BEU processing is halted after the software reset processing is carried out. Note that if 0 is written to this bit when the BEU is halted (BEPRC bit = 0), no operation takes place. 0: NOP (software reset processing if 0 is written to this bit when BEPRC bit = 1). 1: BEU processing starts.

36.2.4 BEU Source Memory Width Registers 1 to 3 (BSMWR1 to BSMWR3)

BSMWR are registers that set the memory width of the source memory areas of BEU input systems 1 to 3.



Bit	Bit Name	Initial Value	R/W	Description
31 to 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29 to 18	BSAMW[13:2]	H'0000	R/W	These bits set the α plane source memory area width of input systems 1 to 3 (set by the number of bytes. Long word or word units).
17, 16	BSAMW[1:0]		R	
15 to 2	BSMW[15:2]	H'0000	R/W	These bits set the source memory area width of input systems 1 to 3 (set by the number of bytes. Long word or word units). These bits set the horizontal width of the source memory area where the source image is located. These bits are set in 2-longword units for input data in the YCbCr or RGB24bpp (stuffing) format, and in longword units for input data in other formats. For a YCbCr 4:4:4 image, the setting is doubled in the BEU because the data size of the C plane is twice as large as that of the Y plane.
1,0	BSMW[1:0]		R	

36.2.5 BEU Source Size Registers 1 to 3 (BSSZR1 to BSSZR3)

BSSZR are registers that set the vertical and horizontal sizes of the images read by BEU input systems 1 to 3.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	BVSS[11:0]											
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	BHSS[11:0]											
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
27 to 16	BVSS[11:0]	H'000	R/W	These bits set the number of vertical pixels read by input systems 1 to 3. These bits set the number of vertical read pixels of the source image read by input systems 1 to 3. When input system n is YCbCr 4:2:0, these bits can be set in 2-pixel units. For other formats, these bits can be set in 1-pixel units. The setting should be in 4-pixel units in VOU or LCDC output mode The settings are in 8-pixel units in VOU output mode when VSKIP is enabled. When input system n is the parent display, the size set in these bits becomes the destination image size. Therefore, when the BEU operates together with the VOU or LCDC, make this setting match the destination image size of the interacting block. Specify 4-pixel units for BVSS when input system 3 is in OSD mode.
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 0	BHSS[11:0]	H'000	R/W	These bits set the number of horizontal pixels read by input systems 1 to 3. These bits set the number of horizontal read pixels of the source image read by input systems 1 to 3. When input system n is YCbCr4:2:2 or YCbCr4:2:0, these bits can be set in 2-pixel units, for other formats these bits can be set in 1-pixel units. The setting should be in 4-pixel units in VOU output mode, and in 8-pixel units in LCDC mode (only for the parent display size). When input system n is the parent display, the size set in these bits becomes the destination image size. Therefore, when the BEU operates together with the VOU or LCDC, make this setting match the destination image size of the interacting block. Specify 4-pixel units for BHSS when input system 3 is in OSD mode.

36.2.6 BEU Source Address Y Registers 1 to 3 (BSAYR1 to BSAYR3)

BSAYR are registers that set the start address for the Y/RGB plane of the images read by BEU input systems 1 to 3.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	BSAY[31:16]															
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BSAY[15:0]															
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	BSAY[31:2]	H'0000 0000	R/W	These bits set the start address for reading the Y/RGB plane of input systems 1 to 3 (2-longword or longword units). When reading a YCbCr image, set the start address of the Y plane. When reading an RGB image, set the start address of the RGB plane. These bits are set in 2-longword units for input data in the YCbCr or RGB24bpp (stuffing) format, and in longword units for input data in other formats.
1, 0	BSAY[1:0]		R	

36.2.7 BEU Source Address C Registers 1 to 3 (BSACR1 to BSACR3)

BSACR are registers that set the start address for the C plane of the images read by BEU input systems 1 to 3.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	BSAC[31:16]															
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BSAC[15:0]															
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	BSAC[31:2]	H'0000 0000	R/W	These bits set the start address for reading C plane of input systems 1 to 3 (longword units). When reading YCbCr image, set the start address of C plane. Note that when reading RGB image, this register is not used.
1, 0	BSAC[1:0]		R	

36.2.8 BEU Source Address α Registers 1 to 3 (BSAAR1 to BSAAR3)

BSAAR are registers that set the start address for the α plane of the images read by BEU input systems 1 to 3.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	BSAA[31:16]															
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BSAA[15:0]															
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	BSAA[31:2]	H'0000 0000	R/W	These bits set the start address for reading the α plane of input systems 1 to 3 (longword units).
1, 0	BSAA[1:0]		R	

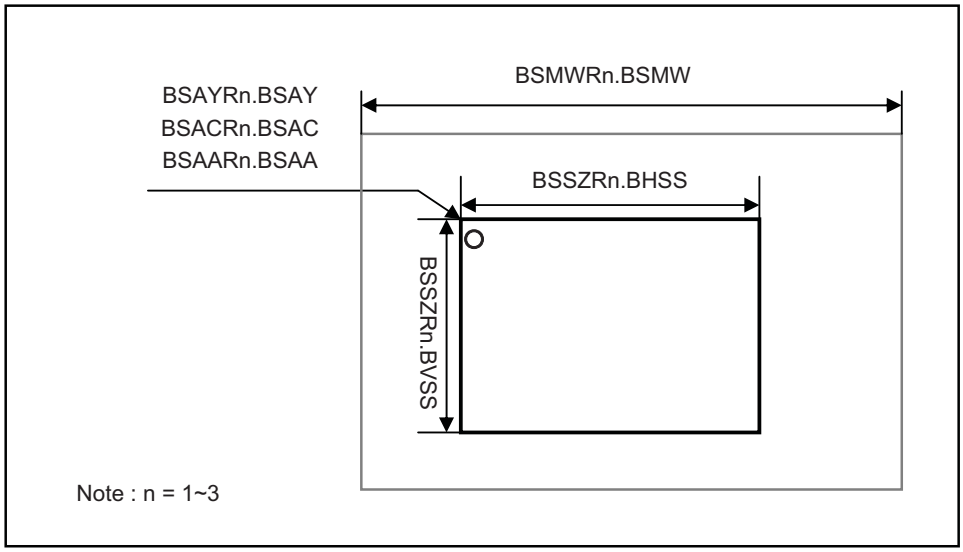


Figure 36.5 Number of Read Pixels of Input System n and Start Addresses

36.2.9 BEU Source Image Format Registers 1 to 2 (BSIFR1 to BSIFR2)

BSIFR are registers that specify the format of the images read by BEU input systems 1 to 2.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INTM[2:0]			INTE	–	CHRR[2:0]						RPKF[4:0]				
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 13	INTM[2:0]	3'b000	R/W	These bits set the color space converter in the input pixel format converter n-unit (RPFn). These bits are only used input system 1. 000: ITU-R BT.601 standard for YCbCr with 8-bit full scale RGB color conversion are used. (initial) BT.601[16,235/240] <-> RGB[0,255] 001: ITU-R BT.601 standard for YCbCr with 8-bit full scale RGB color conversion are used. BT.601[0,255] <-> RGB[0,255] 010: ITU-R BT.709 standard for YCbCr with 8-bit full scale RGB color conversion are used. BT.709[16,235/240] <-> RGB[0,255] 011: ITU-R BT.709 standard for YCbCr with ARIB STD-B24 standard for RGB color conversion are used. BT.709[16,235/240] <-> RGB[16,235] 100-111: Setting prohibited
12	INTE	0	R/W	Turns on or off the RGB ⇔ YCbCr conversion circuit. The direction of conversion is selected with BPKFR.RY 0: No RGB ⇔ YCbCr conversion 1: RGB ⇔ YCbCr conversion performed Note: When performing RGB ⇔ YCbCr conversion, read the source image so that the conversion result has the same format as the other input systems. For details, see table 36.3.

Bit	Bit Name	Initial Value	R/W	Description
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10 to 8	CHRR[2:0]	000	R/W	The format of the image input to input system n is determined by the settings of the RY bit in BPKFR and the INTE bit. When YCbCr image is input to input system n, the data pack form can be selected by the setting of these bits. The data pack forms are shown in table 36.4. 000: Image read in the YCbCr 4:4:4 format 001: Image read in the YCbCr 4:2:2 format 010: Image read in the YCbCr 4:2:0 format 011-111: Setting prohibited
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4 to 0	RPKF[4:0]	00000	R/W	These bits set the RGB input data pack form when the image input to input system n is in the RGB format. The format of the image input to input system n is determined by the settings of the RY bit in BPKFR and the INTE bit. When an RGB image is input to input system 1, the data pack form can be selected from the data pack forms in table 32.5 by the setting of these bits.

Table 36.3 The relation between BSIFRn.INTE, BPKFR.RY and input data pack

INTE	RY	RPF input	Blend Core input
0	0	YCbCr pack	YCbCr pack
0	1	RGB pack	RGB pack
1	0	RGB pack	YCbCr pack
1	1	YCbCr pack	RGB pack

Table 36.4 YCbCr data pack

YCbCr 4:4:4 data pack

Component	31 ～ 24								23 ～ 16								15 ～ 8								7 ～ 0							
Y Data	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3
C Data	Cb0	Cb0	Cb0	Cb0	Cb0	Cb0	Cb0	Cb0	Cr0	Cr0	Cr0	Cr0	Cr0	Cr0	Cr0	Cr0	Cb1	Cb1	Cb1	Cb1	Cb1	Cb1	Cb1	Cb1	Cr1	Cr1	Cr1	Cr1	Cr1	Cr1	Cr1	Cr1

YCbCr 4:2:2 / 4:2:0 data pack

Component	31 ～ 24								23 ～ 16								15 ～ 8								7 ～ 0							
Y Data	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3
C Data	Cb0	Cb0	Cb0	Cb0	Cb0	Cb0	Cb0	Cb0	Cr0	Cr0	Cr0	Cr0	Cr0	Cr0	Cr0	Cr0	Cb2	Cb2	Cb2	Cb2	Cb2	Cb2	Cb2	Cb2	Cr2	Cr2	Cr2	Cr2	Cr2	Cr2	Cr2	Cr2

α YCbCr 4:4:4 data pack

Component	31 ～ 24								23 ～ 16								15 ～ 8								7 ～ 0							
α Data	α0	α0	α0	α0	α0	α0	α0	α0	α1	α1	α1	α1	α1	α1	α1	α1	α2	α2	α2	α2	α2	α2	α2	α2	α3	α3	α3	α3	α3	α3	α3	α3
Y Data	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3
C Data	Cb0	Cb0	Cb0	Cb0	Cb0	Cb0	Cb0	Cb0	Cr0	Cr0	Cr0	Cr0	Cr0	Cr0	Cr0	Cr0	Cb1	Cb1	Cb1	Cb1	Cb1	Cb1	Cb1	Cb1	Cr1	Cr1	Cr1	Cr1	Cr1	Cr1	Cr1	Cr1

α YCbCr 4:2:2 / 4:2:0 data pack

Component	31 ～ 24								23 ～ 16								15 ～ 8								7 ～ 0							
α Data	α0	α0	α0	α0	α0	α0	α0	α0	α1	α1	α1	α1	α1	α1	α1	α1	α2	α2	α2	α2	α2	α2	α2	α2	α3	α3	α3	α3	α3	α3	α3	α3
Y Data	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3
C Data	Cb0	Cb0	Cb0	Cb0	Cb0	Cb0	Cb0	Cb0	Cr0	Cr0	Cr0	Cr0	Cr0	Cr0	Cr0	Cr0	Cb2	Cb2	Cb2	Cb2	Cb2	Cb2	Cb2	Cb2	Cr2	Cr2	Cr2	Cr2	Cr2	Cr2	Cr2	Cr2

Table 36.5 RGB input data pack

No	RPKF [4:0]	Bit Rate [bpp]	Phase	Bit 31 ~ 24								23 ~ 16								15 ~ 8								7 ~ 0							
0	5b'00000	24	–	A0	A0	A0	A0	A0	A0	A0	A0	R0	R0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	B0	B0
1	5b'00001		–	R0	R0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	B0	B0	A0	A0	A0	A0	A0	A0	A0	A0
2	5b'00010		0	R0	R0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	B0	B0	R1	R1	R1	R1	R1	R1	R1	R1
			1	G1	G1	G1	G1	G1	G1	G1	G1	B1	B1	B1	B1	B1	B1	B1	B1	R2	R2	R2	R2	R2	R2	R2	R2	G2	G2	G2	G2	G2	G2	G2	G2
			2	B2	B2	B2	B2	B2	B2	B2	B2	R3	R3	R3	R3	R3	R3	R3	R3	G3	G3	G3	G3	G3	G3	G3	G3	B3	B3	B3	B3	B3	B3	B3	B3
3	5b'00011	16	–	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	R1	R1	R1	R1	R1	G1	G1	G1	G1	G1	G1	B1	B1	B1	B1	B1
7	5b'00111	18	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0
11	5b'01011	24	0	B0	B0	B0	B0	B0	B0	B0	B0	G0	G0	G0	G0	G0	G0	G0	G0	R0	R0	R0	R0	R0	R0	R0	R0	B1	B1	B1	B1	B1	B1	B1	B1
			1	G1	G1	G1	G1	G1	G1	G1	G1	R1	R1	R1	R1	R1	R1	R1	R1	B2	B2	B2	B2	B2	B2	B2	B2	G2	G2	G2	G2	G2	G2	G2	G2
			2	R2	R2	R2	R2	R2	R2	R2	R2	B3	B3	B3	B3	B3	B3	B3	B3	G3	G3	G3	G3	G3	G3	G3	G3	R3	R3	R3	R3	R3	R3	R3	R3
12	5b'01100	24	–	A0	A0	A0	A0	A0	A0	A0	A0	B0	B0	B0	B0	B0	B0	B0	B0	G0	G0	G0	G0	G0	G0	G0	G0	R0	R0	R0	R0	R0	R0	R0	R0
13	5b'01101	16	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0
14	5b'01110	12	–	A0	A0	A0	A0	R0	R0	R0	R0	G0	G0	G0	G0	B0	B0	B0	B0	A1	A1	A1	A1	R1	R1	R1	R1	G1	G1	G1	G1	B1	B1	B1	B1
15	5b'01111		–	R0	R0	R0	R0	G0	G0	G0	G0	B0	B0	B0	B0	A0	A0	A0	A0	R1	R1	R1	R1	G1	G1	G1	G1	B1	B1	B1	B1	A1	A1	A1	A1
16	5b'10000	15	–	A0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	A1	R1	R1	R1	R1	R1	G1	G1	G1	G1	G1	B1	B1	B1	B1	B1
17	5b'10001		–	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	A0	R1	R1	R1	R1	R1	G1	G1	G1	G1	G1	B1	B1	B1	B1	B1	A1
18	5b'10010	12	–	A0	A0	A0	A0	B0	B0	B0	B0	G0	G0	G0	G0	R0	R0	R0	R0	A1	A1	A1	A1	B1	B1	B1	B1	G1	G1	G1	G1	R1	R1	R1	R1
19	5b'10011		–	B0	B0	B0	B0	G0	G0	G0	G0	R0	R0	R0	R0	A0	A0	A0	A0	B1	B1	B1	B1	G1	G1	G1	G1	R1	R1	R1	R1	A1	A1	A1	A1
20	5b'10100	15	–	A0	B0	B0	B0	B0	B0	G0	G0	G0	G0	G0	R0	R0	R0	R0	R0	A1	B1	B1	B1	B1	B1	G1	G1	G1	G1	G1	R1	R1	R1	R1	R1
21	5b'10101		–	B0	B0	B0	B0	B0	G0	G0	G0	G0	G0	R0	R0	R0	R0	R0	A0	B1	B1	B1	B1	B1	G1	G1	G1	G1	G1	R1	R1	R1	R1	R1	A1

Note : when the No2 (RGB 24-bit) is selected, the reading initial address must specify the address that becomes the first of the pixel.

A0, A1 in the table show α value.

36.2.10 BEU Source Image Format Register 3 (BSIFR3)

BSIFR3 is register that specify the format of the images read by BEU input systems 3.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	MOD 1	MOD 0	–	CHRR[2:0]						RPKF[4:0]				
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13	MOD1	0	R/W	Sets the method for fetching source image data when input system 3 is in OSD mode. This bit should be set to 1 (CLUT) only when input system 3 is in OSD mode. Access to read from or write to the CLUT during operation is prohibited. When input system 3 is an OSD and this bit is 1, the color information and alpha values are obtained by referencing the CLUT. The CLUT contents can be modified by longword access from H'FE93 3000 to H'FE93 33FF. The color information and alpha values of the CLUT are stored in the order shown in figure 36.6. Note that the initial values of the CLUT are undefined. 0: Same graphic image or video input as input systems 1 and 2 1: Color information and alpha values are referenced from the CLUT.

Bit	Bit Name	Initial Value	R/W	Description
12	MOD0	0	R/W	Sets whether input system 3 is operated in normal mode or OSD mode. When this bit is 0, input system 3 handles graphic images and video inputs, and the operation is the same as that of input system 1 or 2. In this case, the number of read pixels of the source image is set by BSSZR3. When this bit is 1, input system 3 handles OSD images, and supports repeated pattern output. Repeated pattern output indicates output of tiles with the same picture in rows. The size of one tile is determined by the BHSS and BVSS bits in BSSZR3, and the size in which to paste it to the destination display is determined by the TPHS and TPVS bits in BTPSR. The output appears different according to the magnitude relation of the BSSZR3 and BTPSR settings, as shown in figure 36.7. 0: Input system 3 is used as the same Graphic or Video as input systems 1 and 2 1: Input system 3 is used as OSD.
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10 to 8	CHRR[2:0]	000	R/W	When the RY bit in BPKFR is 0, the image input to input system 3 is in the YCbCr format, and the data pack form can be selected by the setting of these bits. The data pack forms for a YCbCr image input in input system 3 are shown in table 36.4. 000: Image read in the YCbCr 4:4:4 format 001: Image read in the YCbCr 4:2:2 format 010: Image read in the YCbCr 4:2:0 format 011~111: Setting prohibited
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4 to 0	RPKF[4:0]	00000	R/W	These bits set the RGB input data pack form when the image input to input system 3 is in the RGB format. When the RY bit in BPKFR is 1, the image input to input system 3 is in the RGB format, and the data pack form can be selected from the data pack forms in table 36.5 by the setting of these bits.

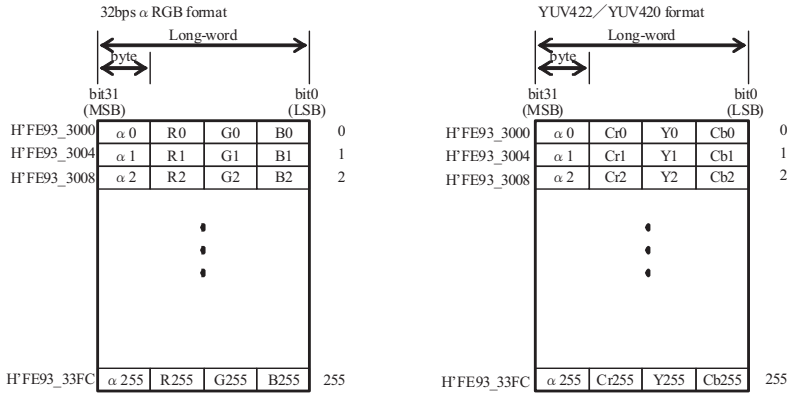


Figure 36.6 Order of Storing CLUT color information

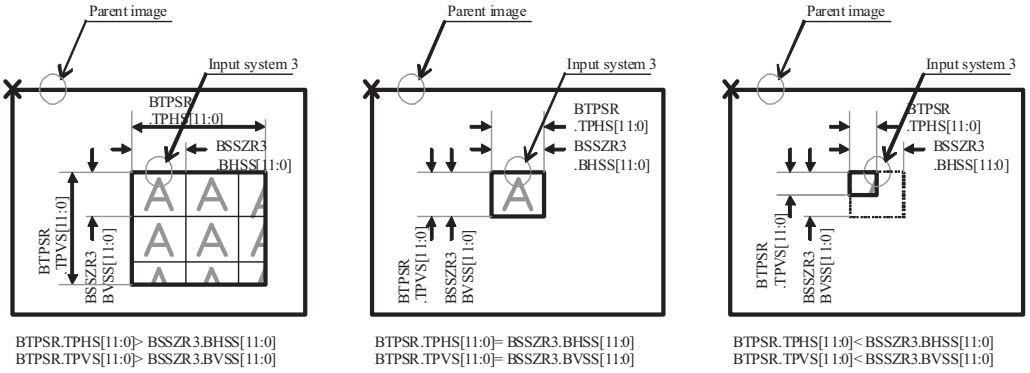


Figure 36.7 Repeated Pattern Output

36.2.11 BEU Tile Pattern Size Register (BTPSR)

BTPSR specifies the size for pasting image to the destination display when input system 3 is in OSD mode.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	TPVS[11:0]											
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	TPHS[11:0]											
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
27 to 16	TPVS[11:0]	H'000	R/W	These bits set the vertical output size of a tile pattern. Set the vertical size for pasting to the destination display when OSD mode is selected for input system 3 in these bits. For YCbCr 4:2:0, these bits can be set in 2-pixel units. For other formats, these bits can be set in 1-pixel units and the maximum value is 4092. This setting is ignored when input system 3 is not in OSD mode.
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 0	TPHS[11:0]	H'000	R/W	These bits set the horizontal output size of a tile pattern. Set the horizontal size for pasting to the destination display when OSD mode is selected for input system 3 in these bits. When input system 3 is not OSD mode, this setting is disregarded. Moreover, input system 3 becomes and this set size becomes an output image size for the parents screen in the OSD mode. For YCbCr 4:2:2 and YCbCr 4:2:0, these bits can be set in 2-pixel units. For other formats, these bits can be set in 1-pixel units. For YCbCr 4:2:0 or YCbCr 4:2:2, the minimum setting value is two pixels, the other formats are one pixel, and the maximum setting value is 4092 pixels. The bits BLOCR3 [1:0] of the blend offset position are added to the BTPSR.TPHS setting value when input system 3 is child screen, and reading data is generated even in the pixel within the range of the value rounded up four-pixel units (There is no problem because pixel data within the range rounded up is not used if it is possible to read). The price rounded up must not rise 4092 though the maximum setting value is 4092. If the input system 3 is set as the parent display (in the

	case, please set BLOCR3 [1:0] to 0), these bits can be set in four-pixel units, and set the ouput image size to the value rounded up.

36.2.12 BEU Blend Control Register 1 (BBLCR1)

BBLCR1 sets blending of the BEU input systems.

Modifying this register during operation is prohibited.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	PWD[2:0]								MT[2:0]		
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W :	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–			–								PXA
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 27	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
26 to 24	PWD[2:0]	00	R/W	These bits specify the parent display at BEU processing. The source image read size (BSSZR1 to BSSZR3) of the input system selected by these bits as the parent display is used as the destination display size. 000: Input system 1 is set as the parent display. 001: Input system 2 is set as the parent display. 010: Input system 3 is set as the parent display. 011~111: Setting prohibited
23 to 19	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
18 to 16	MT[2:0]	001	R/W	These bits specify the output mode for BEU processing*. 001: Memory output mode Other than above: Setting prohibited
15 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	PXA	0	R/W	Selects the pixel-unit alpha value of the input system or the alpha value specified in BPKFR.PAD[7:0] as the value to be added to the PAD field when the RGB output pack includes the PAD field. The α data finally output is decided depending on BBCmR and BRCmR register (n=A, C) set. 0: Alpha value set in the PAD bits in BPKFR is used for the PAD field in the destination image. 1: Pixel-unit alpha value of the input system is used for the PAD field in the destination image.

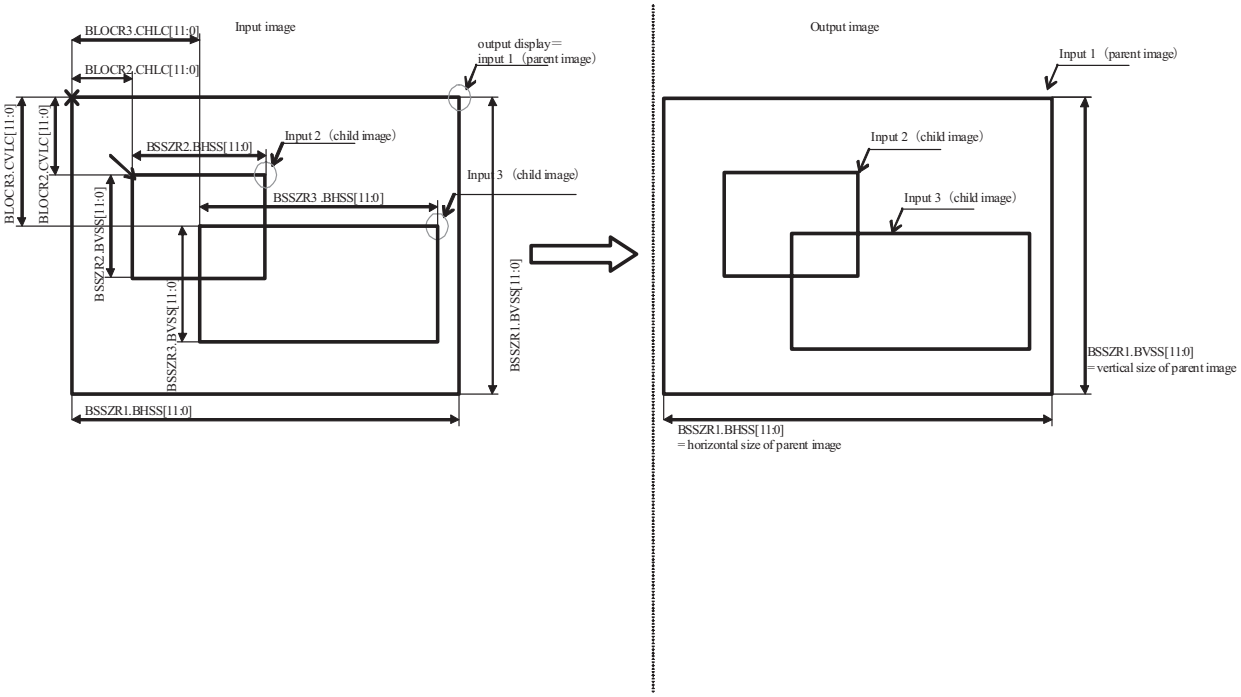


Figure 36.8 The Output Image

36.2.13 Blend Location Registers 1 to 3 (BLOCR1 to BLOCR3)

BLOCR are registers that specify the locations for input systems 1 to 3 at BEU blending.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	CVLC[11:0]											
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	CHLC[11:0]											
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
27 to 16	CVLC[11:0]	H'000	R/W R	These bits specify the number of pixels for the vertical offset from the base point as the blending start location of input systems 1 to 3. it is possible to be set by 1 pixel unit. Set 0 to BLOCRn.CVLC[11:0] when the input n is parent image.
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 0	CHLC[11:0]	H'000	R/W R	These bits specify the number of pixels for the horizontal offset from the base point as the blending start location of input systems 1 to 3. It is possible to be set by 1 pixel unit. Set 0 to BLOCRn.CHLC[11:0] when the input n is parent image.

Figures 36.10 to 36.11 show destination displays of the BEU. The destination display size matches that of the parent display size. The parent display can be selected as input system 1, 2, or 3 by the PWD bits in BBLCR1. The order in which to overlay these input systems can be specified as desired, independent of the parent display setting. Blending operation is not performed for areas where the source displays do not overlap. Areas in a child display which overflow from the parent display are not written to the destination display (see figure 36.9).

The top-left corner of the parent display (= destination display) becomes the base point. The locations of the child displays are expressed by offsets from the base point. For example, if input display 1 is set as the parent display, the top-left corner of input display 1 becomes the base point, the location of input display 2 is determined by the CHLC and CVLC bits in BLOCR2, and the location of input display 3 is determined by the CHLC and CVLC bits in BLOCR3.

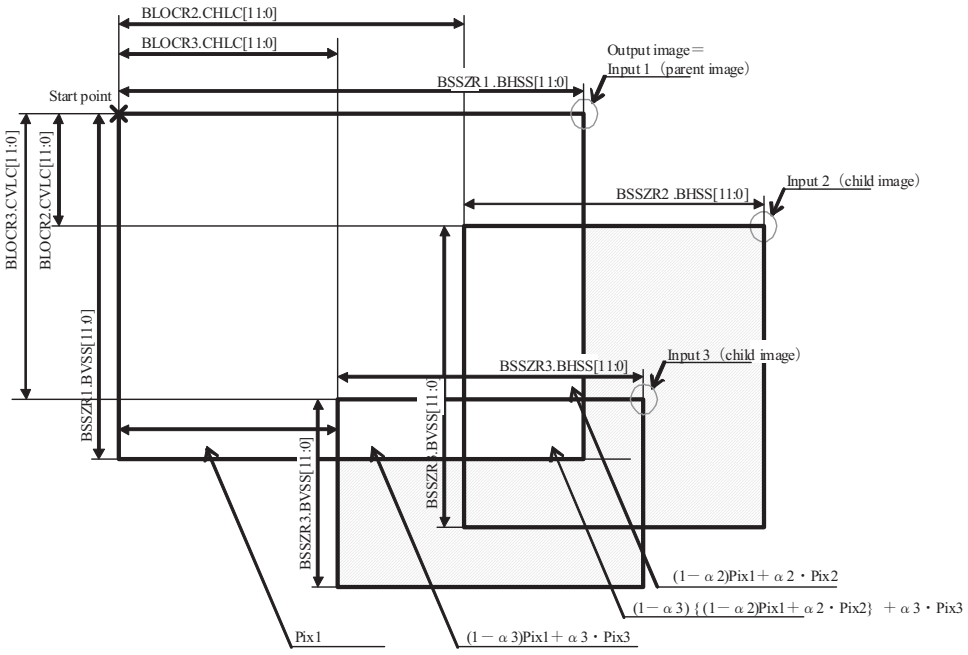


Figure 36.9 BEU Destination Display

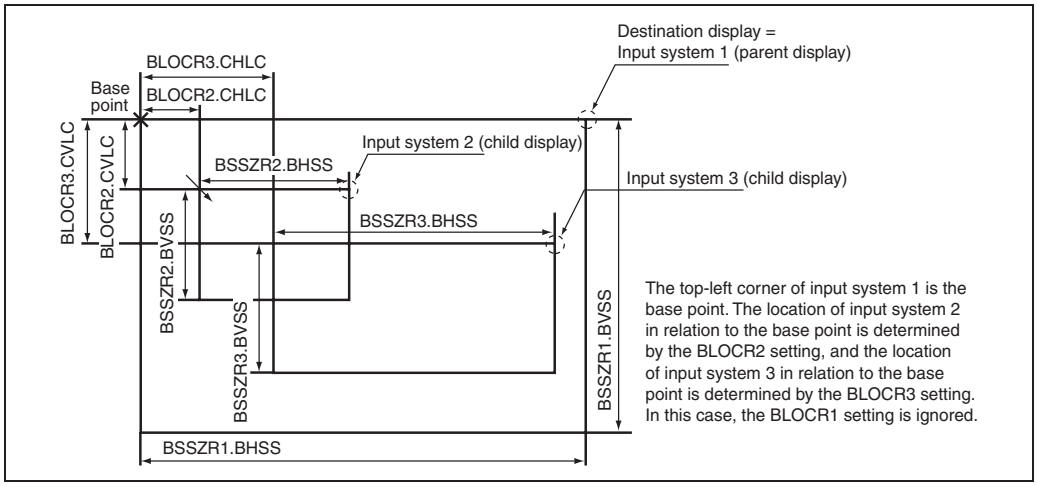


Figure 36.10 Destination Display when Input System 1 is Parent Display

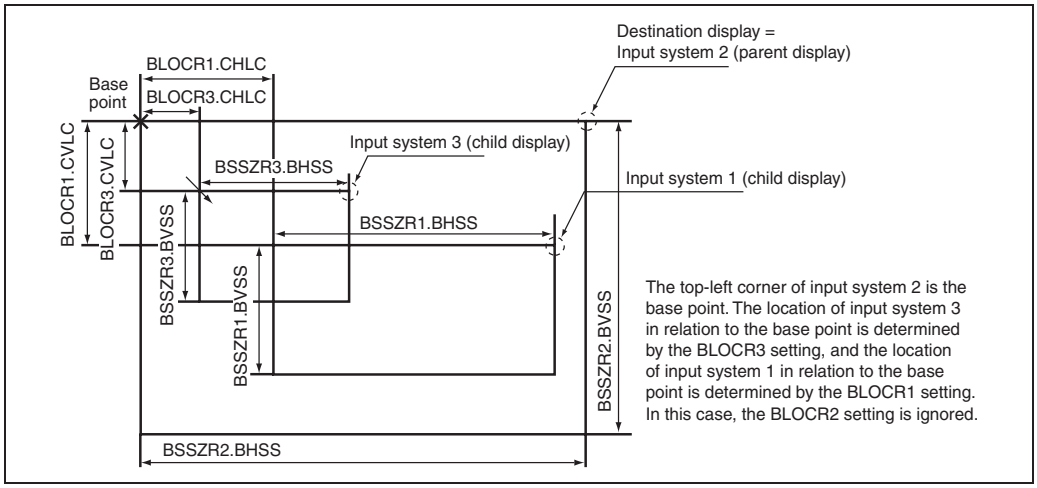


Figure 36.11 Destination Display when Input System 2 is Parent Display

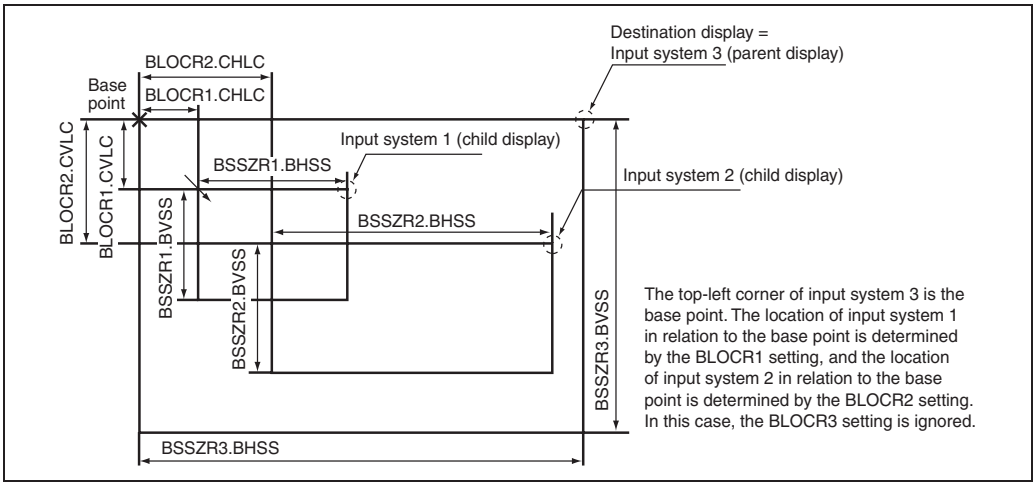


Figure 36.12 Destination Display when Input System 3 is Parent Display

36.2.14 Blend Pack Form Register (BPKFR)

BPKFR specifies the pack form for the blended BEU output.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PAD[7:0]									TM[2:0]					NRM	DITH2
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	DITH1	RY	TE	CHDS[1:0]				WPKFR	WPCK[4:0]				
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	PAD[7:0]	H'00	R/W	These bits specify the PAD value in the output data pack. When data is output in a pack shown in table 36.8, set the value to be stored in the PAD field in these bits. When the BBLCR1.PXA bit is 0, the setting becomes effective.
23	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
22 to 20	TM[2:0]	0	R/W	These bits specify the color conversion in the output pixel format converter (WPF). 000: Use ITU-R BT.601 YCbCr and 8-bit full scale RGB color conversion. BT.601[16,235/240] <-> RGB[0,255] 001: 8-bit full scale BT.601 YCbCr and 8-bit full scale RGB color vonversion BT.601[0,255] <-> RGB[0,255] 010: Use ITU-R BT.709 YCbCr and 8-bit full scale RGB color conversion. BT.709[16,235/240] <-> RGB[0,255] 011: Use ITU-R BT.709 YCbCr and ARIB STD-B24 RGB color conversion BT.709[16,235/240] <-> RGB[16,235] 100~111: Setting prohibited
19 to 18	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
17	NRM	0	R/W	This bit is set whether to divide the output color value from Blend Core to WPF in the α value. It is possible to use it when converting it from the format of color data (Premultiplied Color) multiplied by the α value into the format of color data (Non Premultiplied Color) not multiplied by the α value. 0: The output color value is not divided in the α value. 1: The output color value is divided in the α value.

Bit	Bit Name	Initial Value	R/W	Description
16	DITH2	0	R/W	Selects quantization or dithering for tone reduction in input system 2. 0: Performs quantization at tone reduction in input system 2. 1: Performs dithering at tone reduction in input system 2. Note: Dithering is performed only when the format for reading images is set to the RGB format (BPKFR.RY = 1).
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	DITH1	0	R/W	Selects quantization or dithering for tone reduction in input system 1. 0: Performs quantization at tone reduction in input system 1. 1: Performs dithering at tone reduction in input system 1. Note: Dithering is performed only when the format for reading images is set to the RGB format (BPKFR.RY = 1).
11	RY	0	R/W	The RY bit selects the direction of RGB ⇔ YCbCr conversion. Table 36.6 shows the relationship between the TE and RY bit settings and the input/output data format. 0: Blend Core is operated by the YCbCr format 1: Blend Core is operated by the RGB format
10	TE	0	R/W	
10	TE	0	R/W	The TE bit sets enable or disable of the RGB ⇔ YCbCr color space conversion circuit in output pixel format conversion unit (WPF). 0: disable RGB ⇔ YCbCr conversion in WPF 1: enable RGB ⇔ YCbCr conversion in WPF
9, 8	CHDS[1:0]	00	R/W	These bits set the YCbCr output format of the BEU. The YCbCr data output pack forms are shown in table 36.7. 00: Output as YCbCr 4:4:4 when the image output from input system 2 is in the YCbCr format 01: Output as YCbCr 4:2:2 when the image output from input system 2 is in the YCbCr format 10: Output as YCbCr 4:2:0 when the image output from input system 2 is in the YCbCr format 11: Setting prohibited
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	WPKFR	0	R/W	Sets the output data pack form when BEU output data is in RGB format. The RGB data pack forms are shown in table 36.8.
4 to 0	WPCK[4:0]	00000	R/W	These bits specify the BEU output pack form. The BEU packs output data into a 32-bit pack. When data is output in the RGB format, the data is packed into one of the patterns shown in table 36.8. Set a value in the WPCK column in table 36.8 in these bits.

Table 36.6 Relationship between TE and RY Bits in BPKFR and Input/Output Data Format

TE Bit	RY Bit	Blend Core Input	WPF Output
0	0	YCbCr format	YCbCr format
0	1	RGB format	RGB format
1	0	YCbCr format	RGB format
1	1	RGB format	YCbCr format

Table 36.7 YCbCr Data Output Pack Forms

YCbCr 4:4:4 data form

Component	31 ～ 24								23 ～ 16								15 ～ 8								7 ～ 0							
Y Data	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3
C Data	Cb0	Cb0	Cb0	Cb0	Cb0	Cb0	Cb0	Cb0	Cr0	Cr0	Cr0	Cr0	Cr0	Cr0	Cr0	Cr0	Cb1	Cb1	Cb1	Cb1	Cb1	Cb1	Cb1	Cb1	Cr1	Cr1	Cr1	Cr1	Cr1	Cr1	Cr1	Cr1

YCbCr 4:2:2/4:2:0 data form

Component	31 ～ 24								23 ～ 16								15 ～ 8								7 ～ 0							
Y Data	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3
C Data	Cb0	Cb0	Cb0	Cb0	Cb0	Cb0	Cb0	Cb0	Cr0	Cr0	Cr0	Cr0	Cr0	Cr0	Cr0	Cr0	Cb2	Cb2	Cb2	Cb2	Cb2	Cb2	Cb2	Cb2	Cr2	Cr2	Cr2	Cr2	Cr2	Cr2	Cr2	Cr2

Table 36.8 RGB Data Output Pack Forms

No	WP	WPCK	Bit	Ph	bit 31 ~ 24								23 ~ 16								15 ~ 8								7 ~ 0							
0	b'0	5b'00000	8	–	R0	R0	R0	G0	G0	G0	B0	B0	R1	R1	R1	G1	G1	G1	B1	B1	R2	R2	R2	G2	G2	G2	B2	B2	R3	R3	R3	G3	G3	G3	B3	B3
1	b'0	5b'00001	12	–	0	0	0	0	R0	R0	R0	R0	G0	G0	G0	G0	B0	B0	B0	B0	0	0	0	0	R1	R1	R1	R1	G1	G1	G1	G1	B1	B1	B1	B1
2	b'0	5b'00010			R0	R0	R0	R0	G0	G0	G0	G0	B0	B0	B0	B0	0	0	0	0	R1	R1	R1	R1	G1	G1	G1	G1	B1	B1	B1	B1	0	0	0	0
6	b'0	5b'00110	16	–	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	R1	R1	R1	R1	R1	G1	G1	G1	G1	G1	G1	B1	B1	B1	B1	B1
8	b'0	5b'01000			R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	0	0	0	0	0	0	PAD							
10	b'0	5b'01010		–	PAD								R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	0	0	0	0	0	0	0
13	b'0	5b'01101			PAD								R0	R0	R0	R0	R0	R0	0	0	G0	G0	G0	G0	G0	G0	0	0	B0	B0	B0	B0	B0	B0	0	0
14	b'0	5b'01110	18		R0	R0	R0	R0	R0	R0	0	0	G0	G0	G0	G0	G0	G0	0	0	B0	B0	B0	B0	B0	B0	0	0	PAD							
16	b'0	5b'10000		0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	B0	0	0	0	0	0	0	R1	R1	R1	R1	R1	R1	G1	G1
				1	G1	G1	G1	G1	B1	B1	B1	B1	B1	B1	0	0	0	0	0	0	R2	R2	R2	R2	R2	R2	G2	G2	G2	G2	G2	B2	B2	B2	B2	
				2	B2	B2	0	0	0	0	0	0	R3	R3	R3	R3	R3	R3	G3	G3	G3	G3	G3	B3	B3	B3	B3	B3	B3	B3	0	0	0	0	0	0
17	b'0	5b'10001		0	0	0	R0	R0	R0	R0	R0	R0	0	0	G0	G0	G0	G0	G0	G0	0	0	B0	B0	B0	B0	B0	B0	0	0	R1	R1	R1	R1	R1	R1
				1	0	0	G1	G1	G1	G1	G1	G1	0	0	B1	B1	B1	B1	B1	B1	0	0	R2	R2	R2	R2	R2	R2	0	0	G2	G2	G2	G2	G2	G2
				2	0	0	B2	B2	B2	B2	B2	B2	0	0	R3	R3	R3	R3	R3	R3	0	0	G3	G3	G3	G3	G3	G3	0	0	B3	B3	B3	B3	B3	B3
18	b'0	5b'10010		0	R0	R0	R0	R0	R0	R0	0	0	G0	G0	G0	G0	G0	G0	0	0	B0	B0	B0	B0	B0	B0	0	0	R1	R1	R1	R1	R1	R1	0	0
				1	G1	G1	G1	G1	G1	G1	0	0	B1	B1	B1	B1	B1	B1	0	0	R2	R2	R2	R2	R2	R2	0	0	G2	G2	G2	G2	G2	G2	0	0
				2	B2	B2	B2	B2	B2	B2	0	0	R3	R3	R3	R3	R3	R3	0	0	G3	G3	G3	G3	G3	G3	0	0	B3	B3	B3	B3	B3	B3	0	0
19	b'0	5b'10011		–	PAD								R0	R0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	B0	B0
20	b'0	5b'10100			R0	R0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	B0	B0	PAD							
21	b'0	5b'10101	24	0	R0	R0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	B0	B0	R1	R1	R1	R1	R1	R1	R1	R1
				1	G1	G1	G1	G1	G1	G1	G1	G1	B1	B1	B1	B1	B1	B1	B1	B1	R2	R2	R2	R2	R2	R2	R2	R2	G2	G2	G2	G2	G2	G2	G2	G2
				2	B2	B2	B2	B2	B2	B2	B2	B2	R3	R3	R3	R3	R3	R3	R3	R3	G3	G3	G3	G3	G3	G3	G3	G3	B3	B3	B3	B3	B3	B3	B3	B3
22	b'0	5b'10110	18	–	0	0	0	0	0	0	0	R0	R0	R0	R0	R0	R0	G0	G0	G0	0	0	0	0	0	0	0	G0	G0	G0	B0	B0	B0	B0	B0	B0
23	b'0	5b'10111			0	0	0	0	0	0	0	0	0	0	0	0	0	0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0
53	b'1	5b'10101	24	0	B0	B0	B0	B0	B0	B0	B0	B0	G0	G0	G0	G0	G0	G0	G0	G0	R0	R0	R0	R0	R0	R0	R0	R0	B1	B1	B1	B1	B1	B1	B1	B1
				1	G1	G1	G1	G1	G1	G1	G1	G1	R1	R1	R1	R1	R1	R1	R1	R1	B2	B2	B2	B2	B2	B2	B2	B2	G2	G2	G2	G2	G2	G2	G2	G2
				2	R2	R2	R2	R2	R2	R2	R2	R2	B3	B3	B3	B3	B3	B3	B3	B3	G3	G3	G3	G3	G3	G3	G3	G3	R3	R3	R3	R3	R3	R3	R3	R3
25	b'0	5b'11001	12	–	PAD				R0	R0	R0	R0	G0	G0	G0	G0	B0	B0	B0	B0	PAD				R1	R1	R1	R1	G1	G1	G1	G1	B1	B1	B1	B1
26	b'0	5b'11010		–	R0	R0	R0	R0	G0	G0	G0	G0	B0	B0	B0	B0	PAD				R1	R1	R1	R1	G1	G1	G1	G1	B1	B1	B1	B1	PAD			
27	b'0	5b'11011	15	–	P	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	P	R1	R1	R1	R1	R1	G1	G1	G1	G1	G1	B1	B1	B1	B1	B1
28	b'0	5b'11100		–	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	P	R1	R1	R1	R1	R1	G1	G1	G1	G1	G1	B1	B1	B1	B1	B1	B1	P
29	b'0	5b'11101	12	–	PAD				B0	B0	B0	B0	G0	G0	G0	G0	R0	R0	R0	R0	PAD				B1	B1	B1	B1	G1	G1	G1	G1	R1	R1	R1	R1
30	b'0	5b'11110		–	B0	B0	B0	B0	G0	G0	G0	G0	R0	R0	R0	R0	PAD				B1	B1	B1	B1	G1	G1	G1	G1	R1	R1	R1	R1	PAD			
31	b'0	5b'11111	15	–	P	B0	B0	B0	B0	B0	G0	G0	G0	G0	G0	R0	R0	R0	R0	R0	P	B1	B1	B1	B1	B1	G1	G1	G1	G1	G1	R1	R1	R1	R1	R1
32	b'1	5b'00000		–	B0	B0	B0	B0	B0	G0	G0	G0	G0	G0	R0	R0	R0	R0	R0	P	B1	B1	B1	B1	B1	G1	G1	G1	G1	G1	R1	R1	R1	R1	R1	R1	P

The P in table is shown PAD. The value output to the PAD is set by BBLCR1.PXA and BPKFRPAD.PAC

36.2.15 BEU Transparent Color Control Register 0 (BPCCR0)

BPCCR0 enables or disables transparent color comparison or color replacement.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	CV2	CV1	CV0	–	–	–	–	–	–	SAPE 32	SAPE 31	SAPE 22	SAPE 21	SAPE 12	SAPE 11
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R/W	R/W	R/W	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 15	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
14 to 12	CV2 CV1 CV0	000	R/W	CV2: Input system 3 display color replacement function CV1: Input system 2 display color replacement function CV0: Input system 1 display color replacement function When input pixel values of input system 1 to input system 3 match BPCCRx1.R, BPCCRx1.GY, and BPCCRx1.B, those pixel values and α are replaced with BPCCRx2. (They correspond to each input system at x: 1, 2, and 3.) Color replacement function is enabled when the input format for that input system is RGB 565, 666, 888, or YCbCr. Color replacement function can be set independently for each input system. When CV2 = 1, set BPCCR0.SAPE32-31 = 0. When CV1 = 1, set BPCCR0.SAPE22-21 = 0. When CV0 = 1, set BPCCR0.SAPE12-11 = 0. Note 1: Color replacement function cannot be specified when performing center enlargement (BBLCR1.SELRDD = 1) on input data. Note 2: System 1 transparent color function cannot be used when using system 1 color replacement. 0: Input system x display color replacement function off 1: Input system x display color replacement function on
11 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

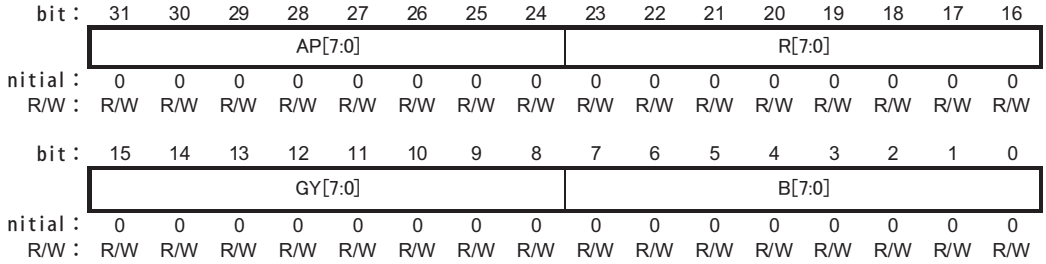
Bit	Bit Name	Initial Value	R/W	Description
5	SAPE32	0	R/W	Two types of color comparison are possible for each input system as transparent color comparison. When the SAPE32 bit is set to 1, input data of input system 3 is compared with the data set in BPCCR32. When the SAPE31 bit is set to 1, input data of input system 3 is compared with the data set in BPCCR31. When both the SAPE32 and SAPE31 bits are cleared to 0, data comparison is disabled. 00: Disables data comparison 1 and 2 for input system 3. 01: Enables data comparison 1 for input system 3. 10: Enables data comparison 2 for input system 3. 11: Enables data comparison 1 and 2 for input system 3.
4	SAPE31	0	R/W	
3	SAPE22	0	R/W	Two types of color comparison are possible for each input system as transparent color comparison. When the SAPE22 bit is set to 1, input data of input system 2 is compared with the data set in BPCCR22. When the SAPE21 bit is set to 1, input data of input system 2 is compared with the data set in BPCCR21. When both the SAPE22 and SAPE21 bits are cleared to 0, data comparison is disabled. 00: Disables data comparison 1 and 2 for input system 2. 01: Enables data comparison 1 for input system 2. 10: Enables data comparison 2 for input system 2. 11: Enables data comparison 1 and 2 for input system 2.
2	SAPE21	0	R/W	
1	SAPE12	0	R/W	Two types of color comparison are possible for each input system as transparent color comparison. When the SAPE12 bit is set to 1, input data of input system 1 is compared with the data set in BPCCR12. When the SAPE11 bit is set to 1, input data of input system 1 is compared with the data set in BPCCR11. When both the SAPE12 and SAPE11 bits are cleared to 0, data comparison is disabled. 00: Disables data comparison 1 and 2 for input system 1. 01: Enables data comparison 1 for input system 1. 10: Enables data comparison 2 for input system 1. 11: Enables data comparison 1 and 2 for input system 1.
0	SAPE11	0	R/W	

36.2.16 BEU Transparent Color Control Registers 1(BPCCRn1 (n=1 to 3))

BPCCRn1 are registers that set the compare data used in transparent color comparison and the alpha value.

If the pack form of BEU input systems 1 to 3 is RGB565, RGB666, RGB888, or YCbCr, the input data is compared with the R, GY, and B data set in these bits. The bit size to be compared differs for each input pack form, and bits become valid from the upper side. Clear bits other than the valid bits to 0.

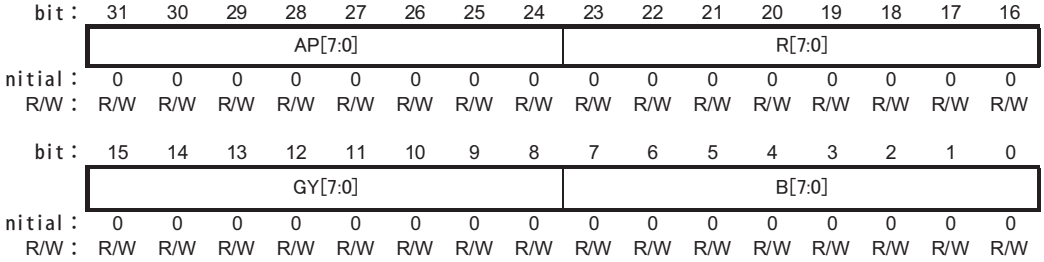
Note that only the Y component is to be compared in case of the YCbCr format. In case of the RGB565 pack form, for example, the R data is compared with the value in the R[7:3] bits, the G data with the value in the GY[7:2] bits, and the B data with the value in the B[7:3] bits.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	AP[7:0]	H'00	R/W	Color replace function: set 0 Transparent color function: α data for substitution of set # 1 These bits set the alpha value used at a data comparison match. Performs data comparison with the BPCCRxx value corresponding to each bit when the input pack form of BEU input system 1 is RGB565, RGB666, RGB888, or YCbCr with the SAPExx bit in BPCCR0 set to 1. When data comparison results in a match, the pixel-unit alpha value is replaced with the alpha value set in these bits (xx = 11, 12, 21, 22, 31, or 32).
23 to 16	R[7:0]	H'00	R/W	Color replace function: compare data R (RGB) Transparent color function: compare data R of set #1 Set 0 to the LSB side of R element to be compared, except when the comparison data of RGB format is not 24bpp. Set BPCCRn1.GY and the BPCCRn.B bit similarly.
15 to 8	GY[7:0]	H'00	R/W	Color replace function: compare data G (RGB) or Y (YCbCr) Transparent color function: compare data G (RGB) or Y (YCbCr of set #1
7 to 0	B[7:0]	H'00	R/W	Color replace function: compare data B (RGB) Transparent color function: compare data B of set #1

36.2.17 BEU Transparent Color Control Registers 2(BPCCRn2 (n=1 to 3))

BPCCRn2 are registers that set the compare data used in transparent color comparison and the alpha value.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	AP[7:0]	H'00	R/W	Color replace function: set 0 Transparent color function: α data for substitution of set # 1 These bits set the alpha value used at a data comparison match. Performs data comparison with the BPCCRxx value corresponding to each bit when the input pack form of BEU input system 1 is RGB565, RGB666, RGB888, or YCbCr with the SAPExx bit in BPCCR0 set to 1. When data comparison results in a match, the pixel-unit alpha value is replaced with the alpha value set in these bits (xx = 11, 12, 21, 22, 31, or 32).
23 to 16	R[7:0]	H'00	R/W	Color replace function: compare data R (RGB) Transparent color function: compare data R of set #1 Set 0 to the LSB side of R element to be compared, except when the comparison data of RGB format is not 24bpp. Set BPCCRn1.GY and the BPCCRn.B bit similarly.
15 to 8	GY[7:0]	H'00	R/W	Color replace function: compare data G (RGB) or Y (YCbCr) Transparent color function: compare data G (RGB) or Y (YCbCr of set #1
7 to 0	B[7:0]	H'00	R/W	Color replace function: compare data B (RGB) Transparent color function: compare data B of set #1

36.2.18 BEU Destination Memory Width Register (BDMWR)

BDMWR sets the memory width of the destination memory area of the BEU.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BDW[15:0]															
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 2	BDW[15:2]	H'00000	R/W	These bits set the width of the destination memory area of the BEU (longword units). These bits specify the horizontal width of the destination memory area where the destination image is to be located by BEU processing.
1, 0	BDW[1:0]		R	

36.2.19 BEU Destination Address Y Register (BDAYR)

BDAYR sets the start address for the Y/RGB plane of the image drawn by the BEU.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	BDAYR[31:16]															
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BDAYR[15:0]															
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	BDAY[31:2]	H'0000 0000	R/W	These bits set the start address for drawing the Y/RGB plane by the BEU (longword units). When drawing a YCbCr image, set the start address of the Y plane. When drawing an RGB image, set the start address of the RGB plane.
1, 0	BDAY[1:0]		R	

36.2.20 BEU Destination Address C Register (BDACR)

BDACR sets the start address for the C plane of the image drawn by the BEU.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	BDACR[31:16]															
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BDAYR[15:0]															
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	BDAC[31:2]	H'0000 0000	R/W	These bits set the start address for drawing the C plane by the BEU (longword units). When drawing a YCbCr image, set the start address of the C plane. Note: When drawing an RGB image, this register is not used.
1, 0	BDAC[1:0]		R	

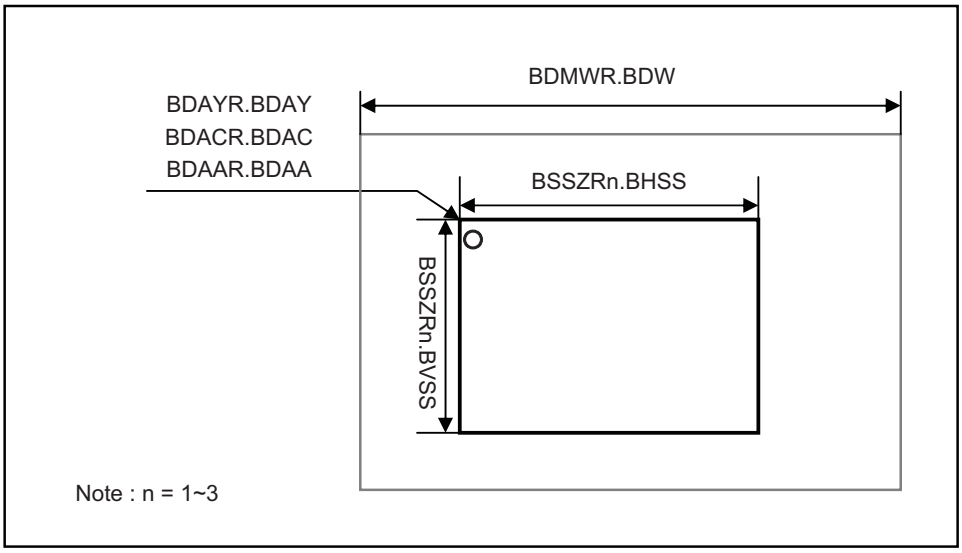


Figure 36.13 Destination Display Size and Start Address

36.2.21 BEU Destination Pixel Format Register (BDPFR)

BDPFR sets the destination pixel format that output to memory.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	ABRM[1:0]		ATRESH[7:0]							
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25, 24	ABRM[1:0]	00	R/W	ABRM select the operation method at decreasing bit of the α data. When the case of 1bit and the BDPFR.ABRM=b '10 are set, the output α decides according to the threshold set by the BDPFR.ATHRESH bit. 00: the number of α bit conversion : LSB is cut 01: the number of α bit conversion : round operation 10: the number of α bit conversion : threshold judgment (when it is 1bpp) 11: Setting prohibited
23 to 16	ATRESH [7:0]	H'00	R/W	The threshold when converting it into 1bit -α data BDPFR.ATHRES set the threshold to convert 8bit-α data into 1bit-α data when BDPFR.ABRM is set b'10. 1bit-α data is set 0 that the value of 8bit-α data is less than ATHRES. Except the 1bit-α data is set 1.
15 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

36.2.22 BEU Address Fixed Register (BAFXR)

BAFXR sets fixed address mode for the data output from the BEU.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	BAFIX
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	BAFIX	0	R/W	When this bit is 1, the addresses to write the image output from the BEU is fixed to the values set in BDAYR and BDACR. When this bit is 0, the address is incremented according to BDMWR. 0: Output addresses of the BEU are not in fixed address mode. 1: Output addresses of the BEU are in fixed address mode. Note: Fixed address mode can be used only for RGB images. Correct operation cannot be guaranteed for YCbCr images.

36.2.23 BEU Swapping Register (BSWPR)

BSWPR sets swapping within 64-bit data at the data input/output section of the BEU.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MODSEL	–	–	–	–	–	–	–	–	–	–	–	AIS3	BEILS3	BEIWS3	BEIBS3
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	AIS2	BEILS2	BEIWS2	BEIBS2	–	BEOLS	BEOWS	BEOBS	AIS1	BEILS1	BEIWS1	BEIBS1
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	MODSEL	0	R/W	When MODSEL = 1 in BSWPR, swap setting is possible for each input system. When MODSEL = 0 in BSWPR, the swap settings made by BEILS, BEIWS, and BEIBS bits in BSWPR are available for all input systems. 0: Disables swap setting mode for each input system. 1: Enables swap setting mode for each input system.
30 to 20	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
19	AIS3	0	R/W	0: byte ordr of α plane of input system 3 is swapped according to swap control {BEILS3, BEIW3, BEIBS3} of the data system. 1: The control of the swap of byte order of α plane of input system 3 is done as follows. BSILS3 | BEIWS3 | BEIBS3 = 0 : not swapped BSILS3 | BEIWS3 | BEIBS3 = 0 : swapped in long word, word, byte word units.
18	BEILS3	0	R/W	0: Input system 3 (multidisplay) input data is not swapped in longword units. 1: Input system 3 (multidisplay) input data is swapped in longword units.
17	BEIWS3	0	R/W	0: Input system 3 (multidisplay) input data is not swapped in word units. 1: Input system 3 (multidisplay) input data is swapped in word units.
16	BEIBS3	0	R/W	0: Input system 3 (multidisplay) input data is not swapped in byte units. 1: Input system 3 (multidisplay) input data is swapped in byte units.

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11	AIS2	0	R/W	0: byte ordr of α plane of input system 2 is swapped according to swap control {BEILS2, BEIWS2, BEIBS2} of the data system. 1: The control of the swap of byte order of α plane of input system 2 is done as follows. BSILS2 | BEIWS2 | BEIBS2 = 0 : not swapped BSILS2 | BEIWS2 | BEIBS2 = 0 : swapped in long word, word, byte word units.
10	BEILS2	0	R/W	0: Input system 2 (multidisplay) input data is not swapped in longword units. 1: Input system 2 (multidisplay) input data is swapped in longword units.
9	BEIWS2	0	R/W	0: Input system 2 (multidisplay) input data is not swapped in word units. 1: Input system 2 (multidisplay) input data is swapped in word units.
8	BEIBS2	0	R/W	0: Input system 2 (multidisplay) input data is not swapped in byte units. 1: Input system 2 (multidisplay) input data is swapped in byte units.
7	—	All 0	R	Reserved This bit is always read as 0. The write value should always be 0.
6	BEOLS	0	R/W	Sets swapping in longword units for output data. In longword swapping for output data, data is swapped in longword units within the 32 bits on the MSB side and within the 32 bits on the LSB side for 64-bit data in the BEU output section. 0: BEU output data is not swapped in longword units. 1: BEU output data is swapped in longword units.
5	BEOWS	0	R/W	Sets swapping data in word units for output data. In word swapping for output data, 16 bits are swapped in word units from the MSB side or LSB side for 64-bit data in the BEU output section. 0: BEU output data is not swapped in word units. 1: BEU output data is swapped in word units.

Bit	Bit Name	Initial Value	R/W	Description
4	BEOBS	0	R/W	Sets swapping data in byte units for output data. In byte swapping for output data, 16 bits are swapped in byte units from the MSB side or LSB side for 64-bit data in the BEU output section. 0: BEU output data is not swapped in byte units. 1: BEU output data is swapped in byte units.
3	AIS1	0	R/W	0: byte ordr of α plane of input system 1 or all input systems is swapped according to swap control {BEILS1, BEIWS1, BEIBS1} of the data system. 1: The control of the swap of byte order of α plane of input system 1 or all input systems is done as follows. BSILS1 | BEIWS1 | BEIBS1 = 0 : not swapped BSILS1 | BEIWS1 | BEIBS1 = 0 : swapped in long word, word, byte word units. (1) BSWPR.MODSEL=0 Same byte swap of alpha plane is set to all the input system reading parts in the BEU by setting the BSWPR.AIS1 bit. (2) BSWPR.MODSEL=1 The byte swap of input plain α is set to system n(n=1 to3) each input respectively by setting the BSWPR.AISn bit.
2	BEILS1	0	R/W	Sets swapping data in longword units for input data. In longword swapping for input data, data is swapped in longword units within the 32 bits on the MSB side and within the 32 bits on the LSB side for 64-bit data in the BEU input section (for all input systems). (1) BSWPR.MODSEL=0 BEILS1 = 1 in BSWPR, data is swapped in longword units within the 32 bits on the MSB side and within the 32 bits on the LSB side for 64-bit data in the BEU input read section (for all input systems). BEILS1 = 0 in BSWPR, data is not swapped in longword units. (2) BSWPR.MODSEL=1 BEILSn = 1 in BSWPR, data is swapped in longword units within the 32 bits on the MSB side and within the 32 bits on the LSB side for 64-bit data in the BEU input system 1 to 3 read section. BEILSn = 0 in BSWPR, data is not swapped in longword units. 0: the alpha plane of the input system 1 or all input systems is not swapped in longword units. 1: the alpha plane of the input system 1 or all input systems is swapped in longword units.

Bit	Bit Name	Initial Value	R/W	Description
1	BEIWS1	0	R/W	Sets swapping data in word units for input data. In word swapping for input data, 16 bits are swapped in word units from the MSB side or LSB side for 64-bit data in the BEU input section (for all input systems). (1) BSWPR.MODSEL = 0 BEIWS1 = 1 in BSWPR, data is swapped in word units within the 16 bits on the MSB or LSB side for 64-bit data in the BEU2 input read section (for all input systems). BEIWS1 = 0 in BSWPR, data is not swapped in word units. (2) BSWPR.MODSEL = 1 BEIWSn = 1 in BSWPR, data is swapped in word units within the 16 bits on the MSB or LSB side for 64-bit data in the BEU2 input system 1 read section. BEIWSn = 0 in BSWPR, data is not swapped in word units. 0: the input data of system 1 or all systems is not swapped in word units. 1: the input data of system 1 or all systems is swapped in word units.
0	BEIBS1	0	R/W	Sets swapping data in byte units for input data. In byte swapping for input data, 16 bits are swapped in byte units from the MSB side or LSB side for 64-bit data in the BEU input section (for all input systems). (1) BSWPR.MODSEL = 0 BEIBS1 = 1 in BSWPR, data is swapped in byte units within the 16 bits on the MSB or LSB side for 64-bit data in the BEU2 input read section (for all input systems). BEIBS1 = 0 in BSWPR, data is not swapped. (2) BSWPR.MODSEL = 1 BEIBS = 1 in BSWPR, data is swapped in byte units within the 16 bits on the MSB or LSB side for 64-bit data in the BEU2 input system 1 read section. BEIBS = 0 in BSWPR, data is not swapped. 0: the input system 1 or all input systems is not swapped in byte units. 1: the input system 1 or all input systems is swapped in byte units.

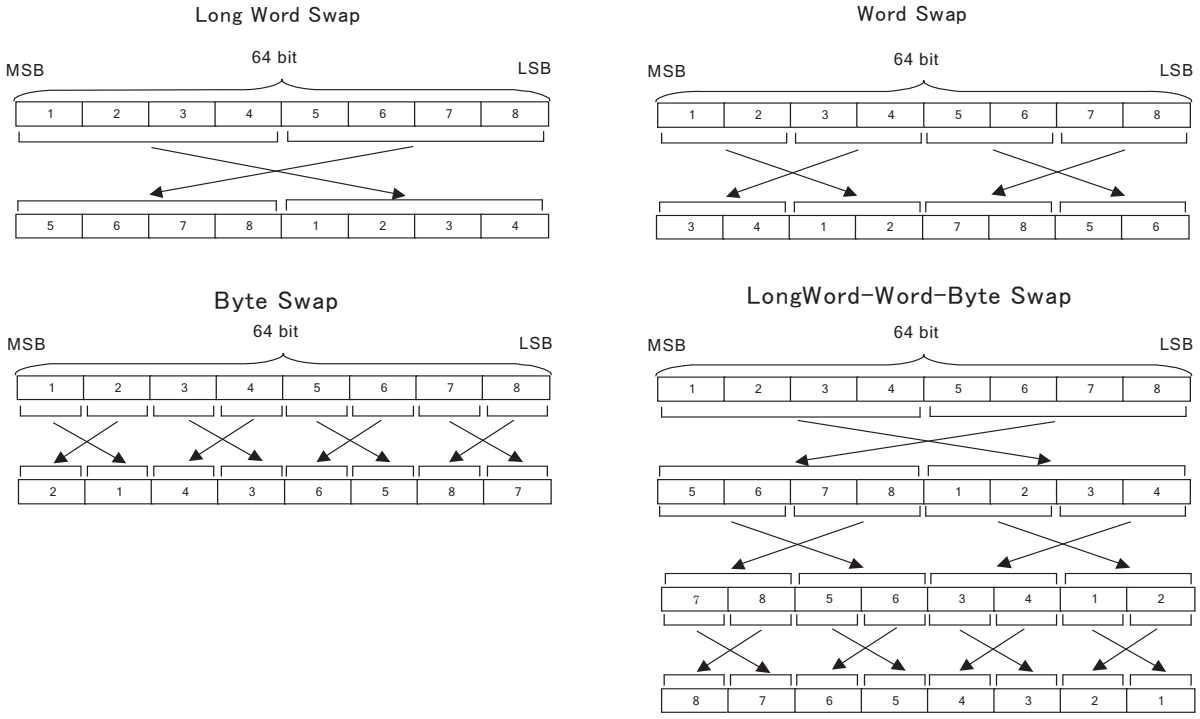


Figure 36.14 Data Swapping by Data Aligner

36.2.24 BEU Event Interrupt Enable Register (BEIER)

BEIER enables or disables output of the interrupt signal of a BEVTR flag.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	FINTE	–	–	–	–	–	–	BEVIOE	BEEND E
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	FINTE	0	R/W	BEIER.FINTE sets whether to generate the BEEND interrupt of each field or frame in the mode that output to the memory and BEU-VOU2 operation.
1	BEVIOE	0	R/W	Enables or disables the interrupt signal of the BEVIO bit in BEVTR to be output. 0: Disables output of the interrupt signal of the BEVIO bit in BEVTR. 1: Enables output of the interrupt signal of the BEVIO bit in BEVTR.
0	BEENDE	0	R/W	Enables or disables the interrupt signal of the BEEND bit in BEVTR to be output. 0: Disables output of the interrupt signal of the BEEND bit in BEVTR. 1: Enables output of the interrupt signal of the BEEND bit in BEVTR.

36.2.25 BEU Event Register (BEVTR)

BEVTR indicates the interrupt source when an internal interrupt occurs in the BEU. Whether output of the interrupt signal of each source in BEVTR is enabled or disabled is set by BEIER.

Modifying this register during operation is prohibited.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	INTREQ
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	BEVIOE	BEENDE
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	INTREQ	0	R	This bit is set to 1 when an interrupt source occurs in the BEU while output of the corresponding interrupt signal is enabled in BEIER. This bit remains cleared to 0 in the case where even though an interrupt source occurs in the BEU, output of the corresponding interrupt signal is disabled in BEIER, or in the case where even though output of the corresponding interrupt signal is enabled in BEIER, no interrupt source occurs in the BEU. 0: Indicates no interrupt is output externally. 1: Indicates an interrupt source has occurred in the BEU, and an interrupt is being output externally.
15 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	BEVIO	0	R/W	BEVIO Flag (violation status) [Reading] 0: Indicates that no violation setting has been detected, or the BEVIO flag has already been cleared. 1: Indicates that a violation setting has been detected. [Writing] 0: Clears the BEVIO flag by writing 0 to it. 1: NOP

Bit	Bit Name	Initial Value	R/W	Description
0	BEEND	0	R/W	BEEND Flag (end status) [Reading] 0: Indicates that BEU processing has not finished, or the BEEND flag has already been cleared. 1: Indicates that BEU processing has finished. [Writing] 0: Clears the BEEND flag by writing 0 to it. 1: NOP

The BEEND flag (end status) is set when BEU operation has finished. At this time, if the BEENDE bit (enables or disables an end interrupt) in BEIER is 1, be2o_intreq_n (interrupt signal) becomes active. The BEEND flag can be reset by writing 0 to the BEEND bit. The BEEND flag is not cleared unless 0 is written to the BEEND bit after BEU processing ends. Therefore, 0 must always be written to the BEEND bit to clear it before the BEU is activated again.

When operation ends normally, the BEIVK bit (operation start) in BESTR is reset when both be2o_beuw_endreq_w (bus acquisition signal request) and be2i_beuw_ack_w (write acknowledge) of the Media bus bridge are active. The BEEND flag is reset when be2i_beuw_end (bus acquisition signal) of the Media bus bridge becomes active.

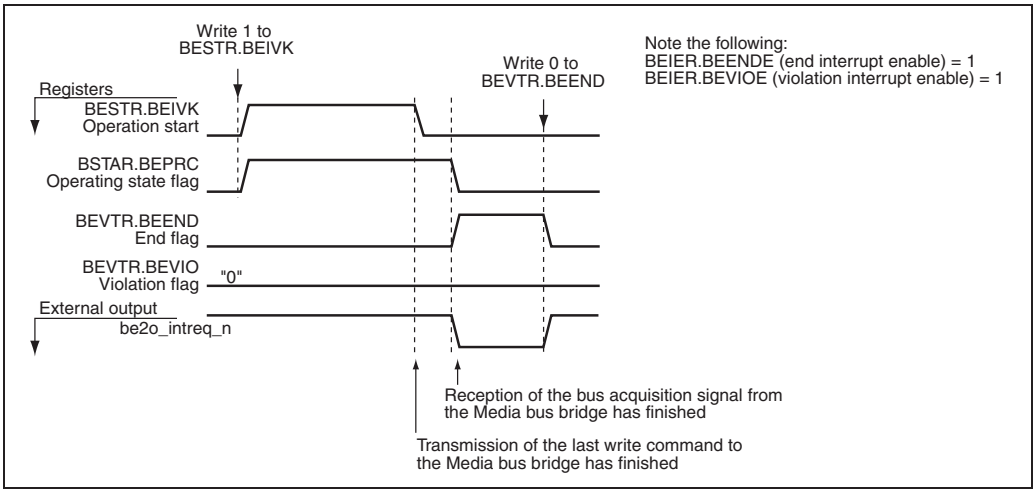


Figure 36.15 Operation Sequence without Violation Setting and Forcible Setting of End Flag

When a violation setting is made as shown in figure 36.16, and the BEIVK bit (operation start) in BESTR is set to 1, the BEU does not start operation and the BEVIO flag (violation status) is set. At this time, if the BEVIOE bit (enables or disables a violation interrupt) in BEIER is 1, be2o_intreq_n (interrupt signal) becomes active. The BEVIO flag can be reset by writing 0 to the BEVIO bit. When the BEVIO flag is set, the BEEND bit (end status) in BEVTR is not set, and the scheduling section, data transfer section, and data processing section are not activated.

The BEVIO flag is not cleared unless 0 is written to the BEVIO bit after BEU processing ends. Therefore, 0 must always be written to the BEVIO bit to clear it before the BEU is activated again.

The BEIVK bit is reset simultaneously to the BEVIO flag being set.

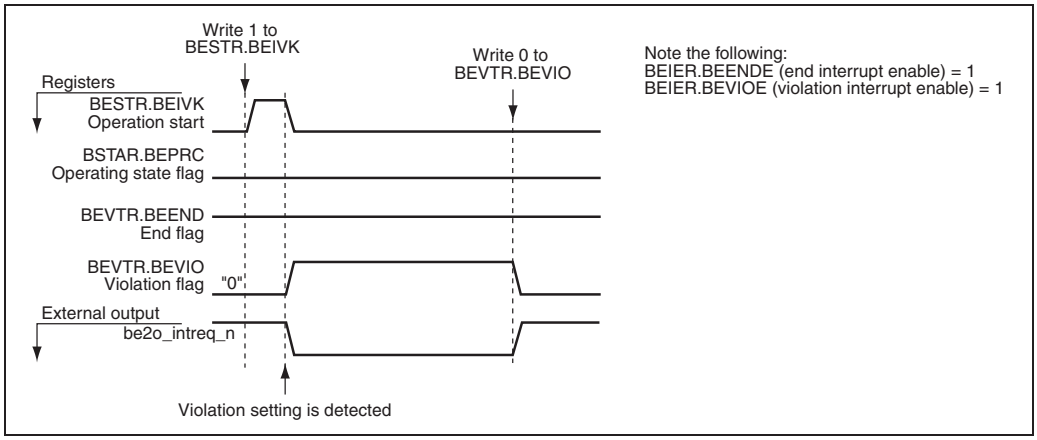


Figure 36.16 Operation Sequence with Violation Setting and Forcible Setting of Violation Flag

36.2.26 BEU Register Control Register (BRCNTR)

BRCNTR controls switching of the planes of BEU registers with a 2-plane configuration. Modifying these registers during operation is prohibited.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	RS	RC
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	RS	0	R/W	Specifies the register plane. Specifies which register plane is used by the BEU in synchronization with VSYNC. The setting of this bit is valid only when the RC bit is 0. 0: BEU uses plane A of the register. 1: BEU uses plane B of the register.
0	RC	0	R/W	Enables register plane switching. Specifies whether or not to switch the register plane used by the BEU in synchronization with VSYNC. If the register plane is not switched, the register plane specified by the RS bit is used. If the BEU is operating alone at register plane switching, the register plane is switched when the BEU is activated. If the BEU is operating together with the VOU or LCDC, the register plane is switched by the switching signal from the VOU or LCDC. 0: Uses the specified register plane. 1: Switches the register plane.

36.2.27 BEU Status Register (BSTAR)

BSTAR indicates the internal status of the BEU and the internal signal states.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	REGST	–	–	–	–	–	–	–	BEPRC
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	REGST	0	R	Indicates which register plane is currently used. 0: BEU is using plane A of the register. 1: BEU is using plane B of the register.
7 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	BEPRC	0	R	This bit is set to 1 when the BEU is activated by the BEIVK bit in BESTR. This bit being set to 1 indicates that the BEU is operating. During this period, do not modify registers that are prohibited to be modified during operation. This bit is automatically cleared to 0 simultaneously with clearing of the BEEND flag in BEVTR. 0: BEU is halted. 1: BEU is operating.

36.2.28 BEU Module Reset Register (BBRSTR)

BBRSTR executes the module reset of the BEU.

Modifying this register during operation is prohibited. If B'1 is written to the ALLRST bit during operation, the logic circuits handshaking with the CPU bus are forcibly reset, and malfunction may also affect modules other than the BEU.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ALL RST
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	ALLRST	0	W	When 1 is written to this bit, all internal control signals of the BEU are reset. If 1 is written to this bit during operation, the logic circuits handshaking with the CPU bus are forcibly reset, and malfunction may also affect modules other than the BEU. 0: NOP 1: Module reset of the BEU

36.2.29 BEU Register-Plane Forcible Setting Register (BRCHR)

BRCHR forcibly specifies the register plane.

Modifying this register during operation is prohibited.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	RCH
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	RCH	0	R/W	Specifies the register plane forcibly. This bit forcibly switches the register plane currently used. Switching of the register plane can be done by this register only when the RC bit in BRCNTR is 1. To forcibly switch the register plane, set the RC bit to 1 in advance. 0: Specifies plane A of the register. 1: Specifies plane B of the register.

36.2.30 BEU Source Alpha Select Register n (n = 1 to 3) (BSASRn)

BSASRn (n = 1 to 3) control the alpha data of input system n and color data.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	ASEL[2:0]			–	–	–	–	–	–	–	–	AEXT[1:0]		CEXT[1:0]	
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ALPHA1[7:0]								ALPHA0[7:0]							
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
30 to 28	ASEL[2:0]	000	R/W	Select the alpha value. When set b'010 or b'011, BSASRn.Alpha0[7:0] and BSASRn.Alpha1[7:0] is used to generate 8bit-alpha value from the input 1bit alpha value. When set b'100, the value that set by BSAVRN.LAYA[7:0] is used. In each input format, table 36.9 is shown the α value selected by ASEL. When the input format is RGB and doesn't have α value that set with BSIFRn.RPKF, h'FF fixed value is selected. The input format is RGB: 000: 1/4/8bit-α (αRGB pack) 001: 8bit-α plane (α plane data is sepecified by BSAARn resigeter) 010: 1bit-α (αRGB pack) input and be generated 8bit-α by BSASRn.Alpha0 register. 011: 1bit-α plane input and be generated 8bit-α by BSASRn.Alpha0 and BSASRn.Alpha1 register 100: fixed α value (use the setting value of BSAVRn.LAYA) The input format is YCbCr 000: fixed α value (h'FF fixed value) 001: 8bit-α plane (a plane data is specified by BSAARn register) 010: fixed α value (h'FF fixed value) 011: Setting prohibited 100: fixedα value (use the setting value of BSAVRn.LAYA)
Bit	**Bit Name**	**Initial**	**R/W**	**Description**

		Value		
27 to 20	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
19 to 18	AEXT[1:0]	00	R/W	BSASRn.AEXT[1:0] bits select the conversion method for the input α data is enhanced to 8bit. 00: the LSB bit of α data is enhanced by 0 01: the LSB bit of α data is enhanced by MSB bit 10: the LSB bit of α data is enhanced by 0 and the maximum value is 0xFF 11: setting prohibited
17 to 16	CEXT[1:0]	00	R/W	BSASRn.CEXT[1:0] bits select the conversion method for the input color data is enhanced to 8bit. 00: the LSB bit of color data is enhanced by 0 01: the LSB bit of color data is enhanced by MSB bit 10: the LSB bit of color data is enhanced by 0 and the maximum value is 0xFF 11: setting prohibited
15 to 8	ALPHA1 [7:0]	H'00	R/W	Set 8bit α data when the input 1bit-α data is 1. When BSASRn.ASEL is set b'010 or b'011, this setting is enabled.
7 to 0	ALPHA0 [7:0]	H'00	R/W	Set 8bit α data when the input 1bit-α data is 0. When BSASRn.ASEL is set b'010 or b'011, this setting is enabled.

BSASRn.ASEL	RGB	YCbCr
b'000	1/4/8bit-α	h'FF
b'001	8bit-α plane	8bit-α plane
b'010	BSASRn.ALPHA0/1	h'FF
b'011	BSASRn.ALPHA0/1	Setting prohibited
b'100	BSAVRn.LAYA	BSAVRn.LAYA

Table 36.9 Alpha Value with ASEL in input format

36.2.31 BEU Source Alpha Value Set Register n (n = 1 to 3) (BSAVRn)

BSAVRn (n=1 to 3) specify the fixed alpha value of input system n.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	LAYA[7:0]								–	–	–	–	–	–	–	–
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	LAYA [7:0]	H'00	R/W	Set the alpha value that BSASRn.ASEL is set b'100.
23 to 0	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.

36.2.32 BEU ROP Control m Register (m=A, C) (BRCmR)

BRCmR is register that control the Blend Unit-m (m=A,C).

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RBC	–	–	–	–	–	–	–	–	INSEL2[2:0]			–	INSEL1[2:0]		
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	RBC	0	R/W	Select the blend operation. The blend operation is disable when RBC is set 0, and the input data of DST side in the Blend unit-m output. 0: blend operation is disable 1: blend operation is enable
30 to 23	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
22 to 20	INSEL2 [2:0]	000	R/W	Set the input of DST side in the Blend unit-m. These bits of BRCAR are used, and these bits of BRCCR are not used. 000: input system 1 (ouput of RPF1) input to DST 001: input system 2 (output of RPF2) input to DST 010: input system 3 (output of PRF3) input to DST 011~111: setting prohibited
19	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
18 to 16	INSEL1	000	R/W	Set the input of SRC side in the Blend unit-m. 000: input system 1 (output of RPF1) input to SRC 001: input system 2 (output of RPF2) input to SRC 010: input system 3 (output of RPF3) input ot SRC 011~111: setting prohibited
15 to 0	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.

36.2.33 BEU Blend Control m Register (m=A, C) (BBCmR)

BBCmR is register that control the Blend Unit-m.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CBES	CCMDX[2:0]			–	–	CCMDY[1:0]		ABES	ACMDX[2:0]			–	ACMDY[2:0]		
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	COEFX[7:0]								COEFY[7:0]							
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	CBES	0	R/W	Set the blend operational expression of color data in Blend Unit-m. The blend coefficient x is set by BBCmR.CCMDX, and the blend coefficient y is set by BBCmR.CCMDY. 0: (blend coefficient x) *(input color data of DST) + (blend coefficient y)*(input color data of SRC) 1: (blend coefficient x)*(input color data of DST) - (blend coefficient y)*(input color data of SRC)
30 to 28	CCMDX	00	R/W	Set the blend coefficient x in the blend operational expression set by BBCmR.CBES. 000: the input alpha data of DST 001: 255 – (the input alpha data of DST) 010: the input alpha data of SRC 011: 255 – (the input alpha data of SRC) 100: the fixed alpha value 1 (COEFX) 101~111: setting prohibited
27	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
26 to 24	CCMDY	00	R/W	Set the blend coefficient y in the blend operational expression set by BBCmR.CBES. 000: the input alpha data of DST 001: 255 – (the input alpha data of DST) 010: the input alpha data of SRC 011: 255 – (the input alpha data of SRC) 100: the fixed alpha value 2 (COEFY) 101~111: setting prohibited

Bit	Bit Name	Initial Value	R/W	Description
23	ABES	0	R/W	Set the blend operational expression of alpha in Blend Unit-m. The blend coefficient x is set by BBCmR.ACMDX, and the blend coefficient y is set by BBCmR.ACMDY. 0: (blend coefficient x) *(input alpha data of DST) + (blend coefficient y)*(input alpha data of SRC) 1: (blend coefficient x)*(input alpha data of DST) - (blend coefficient y)*(input alpha data of SRC)
22 to 20	ACMDX [2:0]	000	R/W	Set the blend coefficient x in the blend operational expression set by BBCmR.ABES. 000: the input alpha data of DST 001: 255 – (the input alpha data of DST) 010: the input alpha dat of SRC 011: 255 – (input alpha data of SRC) 100: the fixed alpha value 1 (COEFX)
18 to 16	ACMDY [2:0]	000	R/W	Set the blend coefficient y in the blend operation expression set by BBCmR.ABES. 000: the input alpha data of DST 001: 255 – (the input alpha data of DST) 010: the input alpha data of SRC 011: 255 – (the input alpha data of SRC) 100: the fixed alpha value 2 (COEFY)
15 to 8	COEFX	H'00	R/W	Set the fixed alpha value 1 when BBCmR.CCMDX is set b'100 or BBCmR.ACMDX is set b'100
7 to 0	COEFY	H'00	R/W	Set the fixed alpha value 2 when BBCmR.CCMDY is set b'100 or BBCmR.ACMDY is set b'100

Section 37 Video Processing Unit (VPU5HG)

The VPU5HG is a multi-codec module which provides encoding and decoding capabilities on the basis of multiple video coding schemes, e.g., H.264/AVC, MPEG-4, MPEG-2 and VC-1. Equipped with SHwy interface and combined with a CPU core, e.g., SH2A, the VPU5HG permits implementation of a video processing system on a chip (SOC) for mobile designs such as cellular phones, DSCs and DVCs as well as set-top designs such as DVD recorders.

37.1 Features

The VPU5HG has the following excellent features:

- Flexible architecture (microcode)
  H.264/MPEG-4 AVC High Profile (HP) encoding and decoding
  H.262/MPEG-2 AVC Main Profile (MP) encoding and decoding
  MPEG-4 ASP Advanced Simple Profile (ASP) encoding and decoding
  VC-1 SP/MP/AP (Simple, Main, Advanced Profile) decoding
  H.263 Baseline encoding and decoding
- Support for full HDTV resolutions
  1920 pixels × 1080 lines × 30 frames/second
  High throughput achieved by parallel operation on two codec elements (2 CEs) (capability to process 1280 clock cycles/2 MB)
  Bus master operation via 64-bit SHwy interface
- Data handled on a picture-by-picture basis
  Encodes and decodes data one picture (frame or field) at a time.
- High picture quality
  Supports the H.264 high-efficiency coding tools (CABAC, interlace, 8 × 8 frequency conversion, and quantization matrix).
  High-efficiency motion vector detection by a combination of discrete search and trace search
  Highly efficient real-time intra-prediction by Prediction from Original Image (POI)
  Optimal-mode selection by Rate-Distortion (RD) cost evaluation
  Picture quality control based on activity analysis results which match visual models
- Block-noise elimination filter incorporated
  This filter reduces block noise to support the standards (MPEG-4, MPEG-2, H.263 and DivX) to which in-loop filters are not applied. Post-filtering is incorporated to reduce block noise for signals in formats (MPEG-4, MPEG-2, H.263, and DivX) where a filter is not applied within the loop.

- Low power dissipation
  Dynamically disables the clocks for the entire VPU5HG.
  Dynamically disables the clocks for individual submodules.

See table 27.1 for details of the specification of the VPU5HG.

Table 27.1 Main Functions of the VPU5HG

Item	Description
Encoding standard supported	H.264 High Profile@Level 4.1
	Main Profile@Level 4.1
	Baseline Profile@Level 3
	MPEG-2 Main Profile@High Level
	MPEG-4 advanced Simple Profile@Level 5, Simple Profile@Level 6
	H.263 Baseline@Level 40
Decoding standard supported	H.264 High Profile@Level 4.1
	Main Profile@Level 4.1
	Baseline Profile[1]@Level 3
	MPEG-2 Main Profile@High Level
	MPEG-4 Advanced Simple Profile[2]@Level 5, Simple Profile@Level 6
	VC-1 Simple Profile@Medium Level, Main Profile@High LevelVC-1 Advanced Profile@Level 3
	H.263 Baseline@Level 40
Image post-processing	Block noise elimination filter (for decoding MPEG-2, MPEG-4 and H.263 images only)
Maximum throughput	1920 pixels × 1080 lines × 30 frames/second (at operation frequencies: 162 MHz or more)
Maximum bit rate	40 Mbps (at operation frequencies: 162 MHz or more)
	Except for MPEG-4 Data Partition (30 Mbps) and VC-1 AP (38 Mbps)
Picture size supported	Minimum size: Horizontally 80 pixels × Vertically 80 lines
	Maximum size: Horizontally 1920 pixels × Vertically 1080 lines
	Horizontally: 8-pixel units
	Vertically: 8-line units
	320 × 180 and 854 × 480 (WVGA+) are supported
Color format	YCbCr 4:2:0 format

Item	Description
Bit stream format	Video elementary stream
	(See table 27.2, detail on the processing range in encoding and decoding)
	Function to add/remove the emulation prevention byte in the H.264 VCL-NAL unit[3].
	Function to remove the emulation prevention byte in the VC-1 AP bit stream data unit.
Picture structure	Frame structure
	Field structure
Motion detection	Motion search accuracy: 1/4 pixels (1/2 pixels for MPEG-2, MPEG-4, and H.263) Motion search range: Horizontal (H) ±64 pixels, Vertical (V) ±32 lines, and search range enhanced feature.

Notes: 1. It is non-corresponed toASO/FMO/RS
2. It is non-corresponed toGMC(Global Motion Compensation), Qpel MC
3. VCL(Video Coding Layer), NAL(Network Abstraction Layer)

Table 27.2 Data Handled by the VPU5HG

Standard	Encoding	Decoding
MPEG-4	VOP header and subsequent	Video packet header or Motion shape texture and subsequent data
H.264	Slice header and subsequent data	Slice data and subsequent data
H.263	Picture header and subsequent data	Picture header and subsequent data
MPEG-2	Picture header and subsequent data	Picture header and subsequent data
MPEG-1	Not supported	Picture header and subsequent data
VC-1	Not supported	Slice data and subsequent data

Table 27.3 lists some of the parameters included in the headers which are added by software for encoding. Set these listed parameters to the fixed values shown in table 27.3.

Table 27.3 Setup of the Intra-header Parameters for Encoding

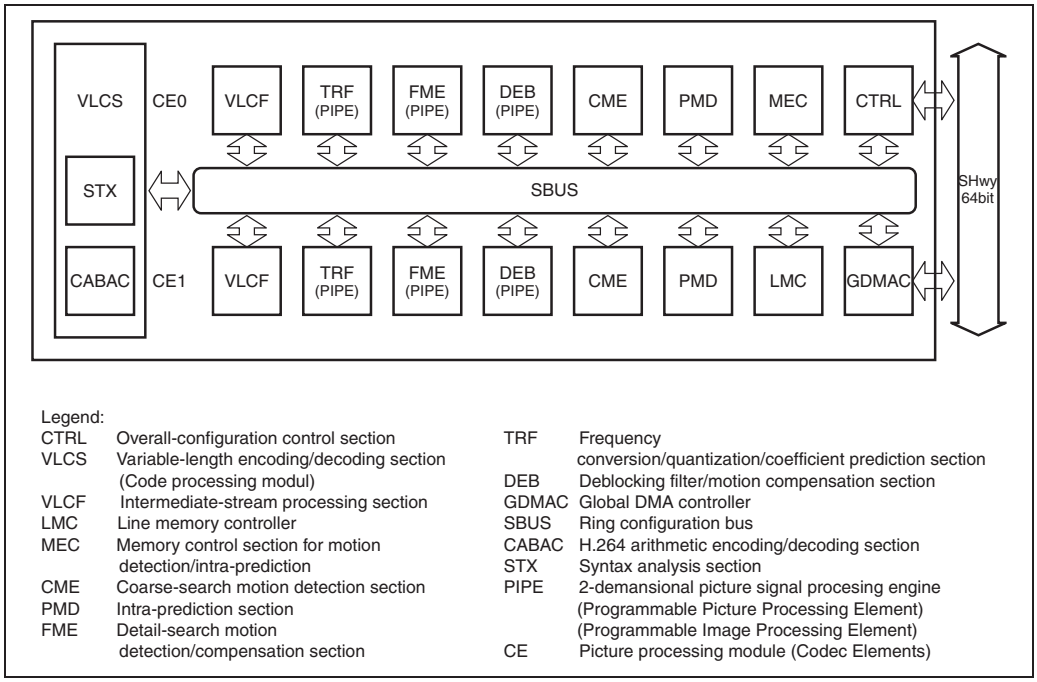
Standard	Intra-header Parameter	Setting	Remarks
MPEG-4	quarter_sample	0	Does not support QpelMC.
H.264	mb_adaptive_frame_field_flag	0	Does not support MB-AFF.
	direct_8x8_inference_flag	1	Supports block sizes greater than or equal to 8 × 8 only.
	weighted_pred_flag	0	Does not support weighted prediction video encoding.
	weighted_bipred_idc	0	
	constrained_intra_pred_flag	0	Not supported.
	direct_spatial_mv_pred_flag	1	Supports spatial direct mode only.
MPEG-2	concealment_motion_vectors	0	Not supported.

Figure 27.1 shows a block diagram of the VPU5HG.

Table 27.1 explains its submodules. |
The VPU5HG offers interface for each of the two systems for the target and initiator connected to the 64-bit SHwy bus.

The VPU5HG consist of: a code processing module (VLCS) which performs variable-length encoding and decoding; picture processing modules (CEs) which process 2-dimensional picture signals; an MEC and LMC which control the internal memory shared by the submodules; a GDMAC which provides master transfer to external RAM as the SHwy initiator and a CTRL which achieves overall control. The submodules are connected together via a ring configuration bus (SBUS). The CEs are two systems which interact with each other to perform parallel processing of two macroblocks per period of 1280 clock cycles. The VPU5HG is only available for MPEG-4/H.263 encoding if one of its CEs is used. In this case, the CE used is CE0.

The STX in the VLCS uses microcode to flexibly encode and decode pictures. The TRF, FME and DEB in each CE also use microcode to do the same.



Legend:

CTRL	Overall-configuration control section	TRF	Frequency conversion/quantization/coefficient prediction section
VLCS	Variable-length encoding/decoding section (Code processing modul)	DEB	Deblocking filter/motion compensation section
VLCF	Intermediate-stream processing section	GDMAC	Global DMA controller
LMC	Line memory controller	SBUS	Ring configuration bus
MEC	Memory control section for motion detection/intra-prediction	CABAC	H.264 arithmetic encoding/decoding section
CME	Coarse-search motion detection section	STX	Syntax analysis section
PMD	Intra-prediction section	PIPE	2-demansional picture signal procesing engine (Programmable Picture Processing Element) (Programmable Image Processing Element)
FME	Detail-search motion detection/compensation section	CE	Picture processing module (Codec Elements)

Figure 27.1 VPU5HG Block Diagram

(1) Microcode Configurations

Table 27.4 and 27.5 show the microcode configurations for VPU5HG. Settings are required for the encoding standard, the VLCS (encode processing module), and the CE (picture processing module) which performs 2DG picture signal processing.

Table 27.4 VPU5HG Encoding Microcode Configurations

	VLCS Microcode		CE Microcode	
Standard	**Name**	**Size**	**Name**	**Size**
H.264	s264e.bin	16 Kbytes	p264e_h.bin	41 Kbytes
MPEG-4/H.263	smp4e.bin	44 Kbytes	pmp4e_h.bin	48 Kbytes
			pmp4e_s.bin (*)	44 Kbytes
MPEG-2	smp2e.bin	35 Kbytes	pmp2e_h.bin	44 Kbytes

Note: Firmware for encoding which involves one CE.

Tabler27.5 VPU5HG Decoding Microcode Configurations

	VLCS Microcode		CE Microcode	
Standard	**Name**	**Size**	**Name**	**Size**
H.264	s264d.bin	40 Kbytes	p264d_h.bin	48 Kbytes
MPEG-4/H.263	smp4d.bin	42 Kbytes	pmp4d_h.bin	40 Kbytes
MPEG-1/-2	smp2d.bin	32 Kbytes	pmp2d_h.bin	36 Kbytes
VC-1 SP/MP	svc1d.bin	24 Kbytes	pvc1d_h.bin	52 Kbytes
VC-1 AP	svc1apd.bin	36 Kbytes		

37.2 Register Description

The VPU5HG contains the registers (table 27.6) which can directly be read/write-accessed by the host CPU. It also contains the internal registers (table 27.8 and 27.9) which can be configured by the initialization routine.

The host can access any long word (32 bits) in the registers.

The internal registers can be configured using the initialization routine the VPU5HG GDMAC, which serves as a master, transfers operation control parameter settings from the external RAM to an internal register or memory. Before the VPU5HG is activated, the operation control parameters are stored in a predetermined format in the external memory. Data in the internal registers can be accessed in units of 64 bits.

The registers with names which are prefixed with "VP5_CE_" should be configured when the picture processing module (CE) is activated. The registers with names which are prefixed with "VP5_VLC_" should be configured when the code processing module (VLCS) is activated. The registers with names which are prefixed with "VP5_" should be configured when the CE or VLCS is activated. Suffixes 0 and 1 for registers indicate that these registers are for CE0 and CE1.

The grayed portions represent reserved areas for debugging or future functional expansion. Do not access the reserved areas. Never access the registers when the VPU5HG is in the module standby mode (with the operation clock placed in hold status).

Table 27.6 VPU5HG Register Configuration

Register Name	Abbreviation	R/W	Address	Access Size
VPU5HG version control register H	VP5_VCRH	R	H'FE90 0000	32
VPU5HG version control register L	VP5_VCRL	R	H'FE90 0004	32
VPU5HG command register	VP5_CMD	R/W	H'FE90 0008	32
VPU5HG overall control register	VP5_CTRL	R/W	H'FE90 000C	32
VPU5HG interrupt control register	VP5_IRQ_ENB	R/W	H'FE90 0010	32
VPU5HG interrupt status register	VP5_IRQ_STA	R/W	H'FE90 0014	32
VPU5HG clock supply control register	VP5_CLK_STOP	R/W	H'FE90 001C	32
VPU5HG status register	VP5_STATUS	R	H'FE90 0020	32
Motion vector count register	VP5_CE_MV_NUM	R	H'FE90 0050	32
Forward reference horizontal motion vector sum register	VP5_CE_MVH_REF0	R	H'FE90 0054	32
Forward reference vertical motion vector sum register	VP5_CE_MVV_REF0	R	H'FE90 0058	32
Backward reference horizontal motion vector sum register	VP5_CE_MVH_REF1	R	H'FE90 005C	32
Backward reference vertical motion vector sum register	VP5_CE_MVV_REF1	R	H'FE90 0060	32
CE microcode base address register	VP5_CE_MBA	R/W	H'FE90 0080	32
CE parameter base address register 0	VP5_CE_PBA0	R/W	H'FE90 0084	32
CE parameter base address register 1	VP5_CE_PBA1	R/W	H'FE90 0088	32
CE error code register	VP5_CE_ERR	R	H'FE90 00C0	32
Intermediate stream bit count register 0	VP5_CE_INT_TB0	R	H'FE90 00C8	32
Intermediate stream bit count register 1	VP5_CE_INT_TB1	R	H'FE90 00CC	32
Macroblock attribute register	VP5_CE_MB_ATTR	R	H'FE90 00D0	32
Macroblock intra-SAD register	VP5_CE_MB_SADA	R	H'FE90 00D4	32
Macroblcok inter-SAD register	VP5_CE_MB_SADR	R	H'FE90 00D8	32
Macroblcok used-SAD register	VP5_CE_MB_USAD	R	H'FE90 00DC	32
Activity total value register	VP5_CE_ASUM	R	H'FE90 00E0	32
Activity register	VP5_CE_ACT	R	H'FE90 00E4	32
Quantization coefficient total value register	VP5_CE_QSUM	R	H'FE90 00E8	32
Virtual buffer register	VP5_CE_DJS	R	H'FE90 00EC	32

Register Name	Abbreviation	R/W	Address	Access Size
MB average luminance total value register	VP5_CE_YSUM	R	H'FE90 00F0	32
VLCS microcode base address register	VP5_VLC_MBA	R/W	H'FE90 0100	32
VLCS parameter base address register 0	VP5_VLC_PBA0	R/W	H'FE90 0104	32
VLCS parameter base address register 1	VP5_VLC_PBA1	R/W	H'FE90 0108	32
Picture byte count register	VP5_VLC_TB	R	H'FE90 0144	32
VLCS status register H	VP5_VLC_ERRH	R	H'FE90 0148	32
VLCS status register L	VP5_VLC_ERRL	R	H'FE90 014C	32
Intermediate stream bit count register 0	VP5_VLC_INT_TB0	R	H'FE90 0150	32
Intermediate stream bit count register 1	VP5_VLC_INT_TB1	R	H'FE90 0154	32

Table 27.7 Register States in Each Operating Mode

Abbreviation	Power-on Reset	Module Standby
VP5_VCRH	Initialized	Retained
VP5_VCRL	Initialized	Retained
VP5_CMD	Initialized	Retained
VP5_CTRL	Initialized	Retained
VP5_IRQ_ENB	Initialized	Retained
VP5_IRQ_STA	Initialized	Retained
VP5_CLK_STOP	Initialized	Retained
VP5_STATUS	Initialized	Retained
VP5_CE_MV_NUM	Initialized	Retained
VP5_CE_MVH_REF0	Initialized	Retained
VP5_CE_MVV_REF0	Initialized	Retained
VP5_CE_MVH_REF1	Initialized	Retained
VP5_CE_MVV_REF1	Initialized	Retained
VP5_CE_MBA	Initialized	Retained
VP5_CE_PBA0	Initialized	Retained
VP5_CE_PBA1	Initialized	Retained
VP5_CE_ERR	Initialized	Retained
VP5_CE_INT_TB0	Initialized	Retained

Abbreviation	Power-on Reset	Module Standby
VP5_CE_INT_TB1	Initialized	Retained
VP5_CE_MB_ATTR	Initialized	Retained
VP5_CE_MB_SADA	Initialized	Retained
VP5_CE_MB_SADR	Initialized	Retained
VP5_CE_MB_USAD	Initialized	Retained
VP5_CE_ASUM	Initialized	Retained
VP5_CE_ACT	Initialized	Retained
VP5_CE_QSUM	Initialized	Retained
VP5_CE_DJS	Initialized	Retained
VP5_CE_YSUM	Initialized	Retained
VP5_VLC_MBA	Initialized	Retained
VP5_VLC_PBA0	Initialized	Retained
VP5_VLC_PBA1	Initialized	Retained
VP5_VLC_TB	Initialized	Retained
VP5_VLC_ERRH	Initialized	Retained
VP5_VLC_ERRL	Initialized	Retained
VP5_VLC_INT_TB0	Initialized	Retained
VP5_VLC_INT_TB1	Initialized	Retained

Table 27.8 VPU5HG Internal Registers (Set with Initial Routine DMAC Channel 0)

Register Name	Abbreviation	VPU Address	Remarks
Base address array register 0	VP5_BAAR0	H'0014 4000	Refer to table 27.20 for details.
Decode luminance picture DMA channel register 0	VP5_CE_DCHR_DECY0	H'0014 0040	
Decode chrominance picture DMA channel register 0	VP5_CE_DCHR_DECC0	H'0014 0048	
Filter luminance picture DMA channel register 0	VP5_CE_DCHR_DISPY0	H'0014 0050	
Filter chrominance picture DMA channel register 0	VP5_CE_DCHR_DISPC0	H'0014 0058	
Reference picture DMA channel register	VP5_CE_DCHR_REF	H'0014 0060	
Encode picture DMA channel register 0	VP5_CE_DCHR_TMP0	H'0014 0068	Set only for encoding which involves one CE
MV information output DMA channel register 0	VP5_CE_DCHR_MVINFO0	H'0014 0090	
Odd MB line MV information output DMA channel register 0	VP5_CE_DCHR_MVINFOB0	H'0014 0098	
Anchor picture MV information DMA channel register 0	VP5_CE_DCHR_MVR0	H'0014 00A0	
Anchor picture odd MB line MV information DMA channel register 0	VP5_CE_DCHR_MVRB0	H'0014 00A8	
CE intermediate stream DMA channel register 0	VP5_CE_DCHR_CEIS0	H'0014 00B0	
CE intermediate control stream DMA channel register 0	VP5_CE_DCHR_CEIC0	H'0014 00B8	
Stream A DMA channel register	VP5_VLC_DCHR_STRA	H'0014 00C0	
Stream B DMA channel register	VP5_VLC_DCHR_STRB	H'0014 00C8	
Command stream DMA channel register	VP5_VLC_DCHR_CMDS	H'0014 00D0	
VLCS data partition DMA channel register	VP5_VLC_DCHR_BPDP	H'0014 00D8	

Register Name	Abbreviation	VPU Address	Remarks
VLCS intermediate stream DMA channel register 0	VP5_VLC_DCHR_VLIS0	H'0014 00E0	
VLCS intermediate control stream DMA channel register 0	VP5_VLC_DCHR_VLIC0	H'0014 00E8	
VLCS co-location not coded DMA channel register	VP5_VLC_DCHR_CLNC	H'0014 00F0	
VLCS data partition write DMA channel register	VP5_VLC_DCHR_DPW	H'0014 00F8	
GDMAC operation control register	VP5_GDMAC_ARDPRI	H'0014 1008	
GDMAC SHwy arbitration control register	VP5_GDMAC_SHWARBT	H'0014 1038	
CE sequence level control register	VP5_CE_SPAR	H'0000 0000	
CE picture level control register	VP5_CE_PPAR	H'0000 0010	
Reserved register	VP5_CE_ENC_WPRED	H'0000 0050	
Encode control register	VP5_CE_ENC_CTRL	H'0000 0058	
Activity control register	VP5_CE_ACQ_CTRL	H'0000 0060	
Intermode judgement control register	VP5_CE_ME_COST	H'0000 0068	
VLCF control register	VP5_CE_VLCF	H'0000 00A0	
Slice size register	VP5_CE_SLC_SIZE	H'0000 00A8	
Target bit rate control register	VP5_CE_TBIT	H'0000 00B0	
Virtual buffer control register	VP5_CE_RCDJ	H'0000 00B8	
Intra refresh control register	VP5_CE_MBRF	H'0000 00C8	
Reverse quantization matrix	VP5_CE_IQMAT	H'003D 0600	EMASK = H'10
Quantization matrix	VP5_CE_QMAT	H'003D 0840	EMASK = H'10
CE intermediate stream 0 buffer size register	VP5_CE_IS_BS0	H'0012 0440	
FME0QNC0 control register	VP5_CE_FME0_QNC0	H'000B 00F0	Set only for encoing which involves one CE

Register Name	Abbreviation	VPU Address	Remarks
FME0QNC1 control register	VP5_CE_FME0_QNC1	H'000B 80F0	Set only for encoing which involves one CE
TRF0QNC0 control register	VP5_CE_TRF0_QNC0	H'000F 00F0	Set only for encoing which involves one CE
TRF0QNC1 control register	VP5_CE_TRF0_QNC1	H'000F 80F0	Set only for encoing which involves one CE
VLCS sequence level control register	VP5_VLC_SPAR	H'0002 0000	
VLCS slice header register	VP5_VLC_SH	H'0002 8000	
VLCS mode register	VP5_VLC_MODE	H'0002 0F50	
Stream A buffer size register	VP5_VLC_STRA_BS	H'0002 0F80	
Stream B buffer size register	VP5_VLC_STRB_BS	H'0002 0F88	
VLCS intermediate stream 0 buffer size register	VP5_VLC_IS_BS0	H'0002 0FA0	
VLCS intermediate stream 1 buffer size register	VP5_VLC_IS_BS1	H'0002 0FB0	

Table 27.9 VPU5HG Internal Registers (Set with Initialization Routine DMAC Channel 1)

Register Name	Abbreviation	VPU Address	Remarks
Base address array register	VP5_BAAR1	H'0034 4000	Refer to table 27.25 for details.
Decode luminance picture DMA channel register 1	VP5_CE_DCHR_DECY1	H'0034 0040	
Decode chrominance picture DMA channel register 1	VP5_CE_DCHR_DECC1	H'0034 0048	
Filter luminance picture DMA channel register 1	VP5_CE_DCHR_DISPY1	H’0034 0050	
Filter chrominance picture DMA channel register 1	VP5_CE_DCHR_DISPC1	H’0034 0058	
Encode picture DMA channel register	VP5_CE_DCHR_TMP1	H'0034 0068	
MV information output DMA channel register 1	VP5_CE_DCHR_MVINFO1	H'0034 0090	
Odd MB line MV information output DMA channel register 1	VP5_CE_DCHR_MVINFOB1	H'0034 0098	
Anchor picture MV information DMA channel register 1	VP5_CE_DCHR_MVR1	H'0034 00A0	
Anchor picture odd MB line MV information DMA channel register 1	VP5_CE_DCHR_MVRB1	H'0034 00A8	
CE intermediate stream DMA channel register 1	VP5_CE_DCHR_CEIS1	H'0034 00B0	
CE intermediate control stream DMA channel register 1	VP5_CE_DCHR_CEIC1	H'0034 00B8	
CE intermediate stream 1 buffer size register	VP5_CE_IS_BS1	H'0032 0440	
DEB1LMDMA synchronous register	VP5_CE_DEB_LMDMASR1	H'0030 0050	
VLCS intermediate stream DMA channel register 1	VP5_VLC_DCHR_VLIS1	H'0034 00E0	
VLC intermediate control stream DMA channel register 1	VP5_VLC_DCHR_VLIC1	H'0034 00E8	

37.2.1 VPU5HG Version Control Register H (VP5_VCRH)

VP5_VCRH is a version control register (VCR) for SHwy. It reads a fixed value.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TOPMB								BOTMB							
Initial value:	1	1	1	0	1	0	0	0	1	1	1	0	1	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VCID															
Initial value:	0	1	0	1	0	1	0	1	1	1	1	1	0	1	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	TOPMB	H'E8	R	High-order eight bits for the upper address allocated to the VPU5HG.
23 to 16	BOTMB	H'E8	R	High-order eight bits for the lower address allocated to the VPU5HG.
15 to 0	VCID	H'55F4	R	VPU5HG identification number (VPU) Bit [15]: Reserved Bits [14:10]: 10101: Indicate "V." Bits [9:5]: 01111: Indicate "P." Bits [4:0]: 10100: Indicate "U."

37.2.2 VPU5HG Version Control Register L (VP5_VCRL)

VP5_VCRL is a version control register (VCR) for the SHwy. It reads a fixed value.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VPU				ARC		VER					REV				
Initial value	0	1	0	1	0	1	0	0	0	1	0	0	0	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MERR								PERR							
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	VPU	0101	R	VPU Series Information 101: Indicates the VPU5
27, 26	ARC	01	R	VPU Configuration Information 01: Indicates the VPU5H configuration.
25 to 21	VER	010	R	Version Information 00: Indicates the VPU5HC 01: Indicates the VPU5HM 10: Indicates the VPU5HG/VPU5HG2 Others: Reserved
20 to 16	REV	00001	R	Revision Information H'01: Indicates a revision H'02 to H'1F: Reserved
15 to 8	MERR	All 0	R	merr_flags Indicates a VPU5HG-specific error defined in SHwy VCR.Fixedly set to 0 for the VPU5HG implementation.
7 to 0	PERR[7:6]	All 0	R	perr_flags
	PERR[5]		R/W	Indicates an error generated in an interface between VPU5 and a packet rooter.
	PERR[4]		R	
	PERR[3:0]		R/W	Set the bit listed in table 27.10 for the VPU5 implementation.

Table 27.10 PERR

37.2.3 VPU5HG Command Register (VP5_CMD)

The VP5_CMD register controls the VPU5HG operation.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	MRST	RST	—	—	—	—	—	—	—	—	VE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10	MRST	0	R/W	Software Module Reset Regardless of the VPU5HG operation state, software module reset causes the internal registers to return to their initial states. To operate the VPU5HG after software module reset, reconfigure all the registers. Do not set both this bit and the VE bit to 1 (for performing software module reset and activation at the same time). Do not set both this bit and the RST bit to 1 (for performing software module reset and software reset at the same time). After this bit is set to 1, it is switched back to 0 automatically. 0: — 1: Forcibly terminates the VPU5HG operation. (Module reset)

Bit	Bit Name	Initial Value	R/W	Description
9	RST	0	R/W	Software Reset After bus master operation by the VPU5HG, software reset stops the VPU5HG and causes its internal registers to return to their initial states. To operate the VPU5HG after software module reset, reconfigure all the registers. Do not set both this bit and the VE bit to 1 (for performing software reset and activation at the same time). Do not set both this bit and the MRST bit to 1 (for performing software reset and software module reset at the same time). After this bit is set to 1, it is switched back to 0 automatically. 0: — 1: Terminates the VPU5HG operation after bus master operation.
8 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	VE	0	R/W	Operation Enable This bit specifies the start of the VPU5HG processing. After this bit is set to 1, it is switched back to 0 automatically. 0: — 1: Starts the VPU5HG operation. The VPU5HG evaluates the VP5_CTRL settings to perform processing. Table 27.11 and 27.12 show the combinations of the operation control parameters specified in VP5_CTRL. When VP5_STATUS.VC = 1 (at setting up the VLCS), do not start the VLCS. When VP5_STATUS.CC = 1 (at setting up the CE), do not start the CE.

37.2.4 VPU5HG Overall Control Register (VP5_CTRL)

The VP5_CTRL register specifies the overall operation of the VPU5HG.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	VL_PED[2:0]			—	VL_MED[2:0]			CEMD	CE_PED[2:0]			—	CE_MED[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VL_SO[3:0]				—	VME	VCN	VE	CE_SO[3:0]				—	CME	CCN	CE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
30 to 28	VL_PED[2:0]	000	R/W	VLCS Parameter Endian Settings These bits make endian settings for the operation control parameters for the code processing module (VLCS). The operation control parameters are set in the internal registers by the initialization routine. Bit 30 specifies interchanging data in byte units, bit 29 interchaning data in word (16-bit) units, and bit 28 interchanging data in long-word (32-bit) units. B W LW Byte order 0 0 0 : 12345678 (Big endian) 0 0 1 : 56781234 0 1 0 : 34127856 0 1 1 : 78563412 1 0 0 : 21436587 1 0 1 : 65872143 1 1 0 : 43218765 1 1 1 : 87654321 (little endian)
27	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
26 to 24	VL_MED[2:0]	000	R/W	VLCS Microcode Endian Settings These bits make endian settings for the microcode e for the code processing module (VLCS). Bit 26 specifies interchanging data in byte units, bit 25 interchanging data in word (16-bit) units, and bit 24 interchanging data in long-word (32-bit) units. B W LW Byte order 0 0 0 : 12345678 (Big endian) 0 0 1 : 56781234 0 1 0 : 34127856 0 1 1 : 78563412 1 0 0 : 21436587 1 0 1 : 65872143 1 1 0 : 43218765 1 1 1 : 87654321 (little endian)
23	CEMD	0	R/W	CE Operation Mode 0: Starts encoding the picture processing module (CE) 1: Starts decoding the picture processing module (CE)
22 to 20	CE_PED[2:0]	000	R/W	CE Parameter Endian Settings These bits make endian settings for the operation control parameters for the picture processing module (CE). The operation control parameters are set in the internal registers by the initialization routine. Bit 22 specifies interchanging data in byte units, bit 21 interchanging data in word (16-bit) units, and bit 20 interchanging data in long-word (32-bit) units. B W LW Byte order 0 0 0 : 12345678 (Big endian) 0 0 1 : 56781234 0 1 0 : 34127856 0 1 1 : 78563412 1 0 0 : 21436587 1 0 1 : 65872143 1 1 0 : 43218765 1 1 1 : 87654321 (little endian)

Bit	Bit Name	Initial Value	R/W	Description
19	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
18 to 16	CE_MED[2:0]	000	R/W	CE Microcode Endian Settings These bits make endian settings for the microcode for the picture processing module (CE). Bit 18 specifies interchanging data in byte units, bit 17 interchanging data in word (16-bit) units, and bit 16 interchanging data in long-word (32-bit) units. B W LW Byte order 0 0 0 : 12345678 (Big endian) 0 0 1 : 56781234 0 1 0 : 34127856 0 0 1 : 78563412 1 0 0 : 21436587 1 0 1 : 65872143 1 1 0 : 43218765 1 1 1 : 87654321 (little endian)
15 to 12	VL_SO[3:0]	H'0	R/W	Source Offset Specification for the Code Processing Module (VLCS) Microcode /Operation Parameters H'0: — H'C (12): Specifies 12 for the VPU5HG.
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10	VME	0	R/W	Code Processing Module (VLCS) Microcode Downloading 0: Does not download the code processing module microcode 1: Downloads the code processing module microcode.

Bit	Bit Name	Initial Value	R/W	Description
9	VCN	0	R/W	Code Processing Module (VLCS) Restart The VLCS suspends its operation after it has processed data ending at the last position in the stream or intermediate-stream buffer. At this time, this bit is set to 1 and a 1 is written to the VE bit in the VP5_CMD register, thereby causing the VPU5 to continue the operation. To terminate rather than continue the VPU5 operation after it is suspended, disable the buffer end interrupt with the VP5_IRQ_ENB register. To continue the operation, set this bit to 1 and write a 1 to the VE bit in the VP5_CMD register. At this time, the other settings should be the same as those used for the immediately preceding activation. 0: Normally starts the code processing module. 1: Restarts the code processing module.
8	VE	0	R/W	Code Processing Module (VLCS) Enable 0: Does not start the code processing module. 1: Starts the code processing module.
7 to 4	CE_SO[3:0]	H'0	R/W	Source Offset Specification for the Picture Processing Module (CE) Microcode /Operation Control Parameters 0: — 1: Specifies 11 for the VPU5HG.
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2	CME	0	R/W	CE Microcode Downloading 0: Does not download the picture processing module microcode. 1: Downloads the picture processing module microcode.

Bit	Bit Name	Initial Value	R/W	Description
1	CCN	0	R/W	Operation Restart The CE suspends its operation after it has processed data ending at the last position in the intermediate-stream buffer. At this time, this bit is set to 1 and a 1 is written to the VE bit in the VP5_CMD register, thereby causing the VPU5 to continue the operation. To terminate rather than continue the VPU5 operation after it is suspended, disable the buffer end interrupt with the VP5_IRQ_ENB register. To continue the operation, set this bit to 1 and write a 1 to the VE bit in the VP5_CMD register. At this time, the other settings should be the same as those used for the immediately preceding activation. 0: Normally starts the picture processing module. 1: Restarts the picture processing module.
0	CE	0	R/W	Picture Processing Module (CE) Enable 0: Does not start the picture processing module. 1: Starts the picture processing module.

The VLCS and CE can be operated independently of each other. Table 27.11 and 12.10 show the combinations of the operation control parameter settings for the VLCS and CE. The downloading of the microcode is required when switching between the operation modes (encode and decode). It is not required when changing the type of picture.

Table 27.11 VLCS Operation Control Parameter Settings

VME	VE	Operation
0	1	Starts VLCS normal operation.
1	0	Downloads only the VLCS microcode.
1	1	After download the VLCS microcode, starts VLCS normal operation.

Table 27.12 CE Operation control Parameter Settings

CME	CE	Operation
0	1	Starts CE normal operation.
1	0	Downloads only the CE microcode.
1	1	After download the CE microcode, starts CE normal operation.

37.2.5 VPU5HG Interrupt Control Register (VP5_IRQ_ENB)

VP5_IRQ_ENB is an interrupt control register for the VPU5HG.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	VISE1	—	VISE0	—	—	VBBE	VBAE	—	CISE1	—	CISE0	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R	R/W	R	R	R/W	R/W	R	R/W	R	R/W	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	VLE	—	—	—	—	—	—	—	CEE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
30	VISE1	0	R/W	VLCS Intermediate-Stream 1 Buffer End Interrupt Enable 0: Disables the VLCS intermediate-stream 1 buffer end interrupt. Be sure to use this value for the VPU5HG 1: Enables the VLCS intermediate-stream 1 buffer end interrupt. Do not use this value for the VPU5HG.
29	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
28	VISE0	0	R/W	VLCS Intermediate-Stream 0 Buffer End Interrupt Enable 0: Disables the VLCS intermediate-stream 0 buffer end interrupt. Be sure to use this value for the VPU5HG. 1: Enables the VLCS intermediate-stream 0 buffer end interrupt. Do not use this value for the VPU5HG.
27, 26	—	00	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
25	VBBE	0	R/W	VLCS Stream B Buffer End Interrupt Enable 0: Disables the VLCS stream B buffer end interrupt. Be sure to use this value for the VPU5HG. 1: Enables the VLCS stream B buffer end interrupt. Do not use this value for the VPU5HG.
24	VBAE	0	R/W	VLCS Stream A Buffer End Interrupt Enable 0: Disables the VLCS stream A buffer end interrupt. Be sure to use this value for the VPU5HG. 1: Enables the VLCS stream A buffer end interrupt. Do not use this value for the VPU5HG.
23	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
22	CISE1	0	R/W	CE Intermediate Stream 1 Buffer End Interrupt Enable 0: Disables the CE intermediate stream 1 buffer end interrupt. 1: Enables the CE intermediate stream 1 buffer end interrupt.
21	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
20	CISE0	0	R/W	CE Intermediate Stream 0 Buffer End Interrupt Enable 0: Disables the CE intermediate stream 0 buffer end interrupt. 1: Enables the CE intermediate stream 0 buffer end interrupt.
19 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	VLE	0	R/W	VLCS Termination Interrupt Enable 0: Disables the VLCS termination interrupt. 1: Enables the VLCS termination interrupt.
7 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	CEE	0	R/W	Enables the VLCS termination interrupt. 0: Disables the CE termination interrupt. 1: Enables the CE termination interrupt

37.2.6 VPU5HG Interrupt Status Register (VP5_IRQ_STA)

VP5_IRQ_STA is a register which indicates the cause of a VPU5HG interrupt. The flag which indicates the occurrence of an interrupt can only be cleared to 0. To clear a bit, write a 0 to the bit and write 1s to the other bits.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	VIS1	—	VIS0	—	—	VBB	VBA	—	CIS1	—	CIS0	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R	R/W	R	R	R/W	R/W	R	R/W	R	R/W	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	VLE	—	—	—	—	—	—	—	CE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
30	VIS1	0	R/W	VLCS Intermediate Stream 1 Buffer End Interrupt Status 0: — 1: Indicates the VLCS has processed data up to the end of the intermediate stream 1 buffer.
29	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
28	VIS0	0	R/W	VLCS Intermediate Stream 0 Buffer End Interrupt Status 0: — 1: Indicates the VLCS has processed data up to the end of the intermediate stream 0 buffer.
27, 26	—	00	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
25	VBB	0	R/W	VLCS Stream B Buffer End Interrupt Status 0: — 1: Indicates the VLCS has processed data up to the end of the stream B buffer.
24	VBA	0	R/W	VLCS Stream A Buffer End Interrupt Status 0: — 1: Indicates the VLCS has processed data up to the end of the stream A buffer.
23	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
22	CIS1	0	R/W	CE Intermediate Stream 1 Buffer End Interrupt Status 0: — 1: Indicates the CE has processed data up to the end of the intermediate stream 1 buffer.
21	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
20	CIS0	0	R/W	CE Intermediate Stream 0 Buffer End Interrupt Status 0: — 1: Indicates the CE has processed data up to the end of the intermediate stream 0 buffer.
19 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	VLE	0	R/W	VLCS Termination Interrupt Status 0: — 1: Indicates the VLCS has terminated its operation.
7 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	CE	0	R/W	Termination Interrupt Status 0: — 1: Indicates the CE has terminated its operation.

37.2.7 VPU5HG Clock Supply Control Register (VP5_CLK_STOP)

The VP5_CLK_STOP register controls the clock for each VPU5HG module.

Do not access this register during operation (i.e., while CS =1 or VS = 1 in the VP5_STATUS register).

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CSMD	CSTP
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	CSMD	0	R/W	Inactive-block Selection This bit selects whether to disable clock supply to each internal module or to the whole system when clock supply to the VPU5HG stops dynamically. Do not access this bit during operation (i.e., while CS = 1 or VS = 1 in VP5_STATUS). 0: Disables the operation clock supply to each module. Clock supply starts when each module becomes active and stops when it becomes inactive. 1: Disables the operation clock supply to the whole system. Clock supply starts when the system becomes active and stops when it becomes inactive.

Bit	Bit Name	Initial Value	R/W	Description
0	CSTP	0	R/W	Module Clock Supply Settings This bit stops the operation clock supply to individual modules in the VPU5HG dynamically. Do not access this bit during operation (i.e., while CS =1 or VS = 1 in VP5_STATUS). 0: Dynamically stops the operation clock supply. 1: Always supplies the operation clocks.

37.2.8 VP5_STATUS: VPU5HG Status Register (VP5_STATUS)

The VP5_STATUS register indicates the VPU5HG status.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	VC	CC	—	—	—	—	—	—	VS	CS
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	VC	0	R	Code Processing Module (VLCS) Setup Status Bit 0: Indicates the VLCS is not active. 1: Indicates the VLCS is active. VLCS should not be started during VLCS setup.
8	CC	0	R	Picture Processing Module (CE) Status Bit 0: Indicates the CE is not active. 1: Indicates the CE is active. CE should not be started during CE setup.
7 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	VS	0	R	Code Processing Module (VLCS) Status Bit 0: Indicates the VLCS is not active. 1: Indicates the VLCS is active.
0	CS	0	R	Picture Processing Module (CE) Status Bit 0: Indicates the CE is not active. 1: Indicates the CE is active.

37.2.9 Motion Vector Count Register (VP5_CE_MV_NUM)

The VP5_CE_MV_NUM register indicates the number of motion vectors (MVs) for encoding. This register becomes valid after the completion of CE encoding.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MV0															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MV1															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	MV0[15:0]	All 0	R	Number of MVs referenced by ref0 (0 to 32640)
15 to 0	MV1[15:0]	All 0	R	Number of MVs referenced by ref1 (0 to 32640)

37.2.10 Forward Reference Horizontal Motion Vector Sum Register (VP5_CE_MVH_REF0)

The VP5_CE_MVH_REF0 register indicates the sum of forward reference horizontal MVs for encoding. This register becomes valid after the completion of CE encoding.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MVH															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MVH															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	MVH0[31:0]	All 0	R	Sum of horizontal motion vectors (-2, 147, 483, 648 to 2, 147, 483, 647)

37.2.11 Forward Reference Vertical Motion Vector Sum Register (VP5_CE_MVV_REF0)

The VP5_CE_MVV_REF0 register indicates the sum of forward reference vertical MVs for encoding. This register becomes valid after the completion of CE encoding.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MVV															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MVV															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	MVV0[31:0]	All 0	R	Sum of vertical motion vectors (-1, 040, 400 to 1, 040, 399)

37.2.12 Backward Reference Horizontal Motion Vector Sum Register (VP5_CE_MVH_REF1)

The VP5_CE_MVH_REF1 register indicates the sum of backward reference horizontal MVs for encoding. This register becomes valid after the completion of CE encoding.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MVH															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MVH															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	MVH1[31:0]	All 0	R	Sum of horizontal motion vectors (-2, 147, 483, 648 to 2, 147, 483, 647)

37.2.13 Backward Reference Vertical Motion Vector Sum Register (VP5_CE_MVV_REF1)

VP5_CE_MVV_REF1 register indicates the sum of backward reference vertical MVs for encoding. This register becomes valid after the completion of CE encoding.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MVV															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MVV															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	MVV1[31:0]	All 0	R	Sum of vertical motion vectors (-1, 040, 400 to 1, 040, 399)

37.2.14 CE Microcode Base Address Register (VP5_CE_MBA)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CMBA[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMBA[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	CMBA[31:0]	All 0	R/W	CE Microcode Base Address Specification These bits specify in units of 32 bytes the start address for storing the CE microcode. Before starting the CE for the VPU5HG, place the microcode in the address specified in this register.

37.2.15 CE Parameter Base Address Register 0 (VP5_CE_PBA0)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CPBA[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CPBA[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	CPBA0[31:0]	All 0	R/W	CE Parameter Base Address Specification These bits specify in units of 32 bytes the start address for storing the CE0 operation control parameter. Before starting the CE for the VPU5HG, place the operation configuration parameter (initialization routine format) in the address specified in this register.

37.2.16 CE Parameter Base Address Register 1 (VP5_CE_PBA1)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CPBA[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CPBA[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	CPBA1[31:0]	All 0	R/W	CE1 Parameter Base Address Specification These bits specify in units of 32 bytes the start address for storing the CE1 operation control parameter. Before starting the CE for the VPU5HG, place the operation configuration parameter (initialization routine format) in the address specified in this register.

37.2.17 CE Error Code Register (VP5_CE_ERR)

VP5_CE_ERR indicates the warning status which is present after CE operation. This register's values are determined at the end of operation. Warning takes place when the specified upper or lower limit is reached. Typically, it does not take place concerning a stream encoded with the VPU5HG.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ERC[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EPY[7:0]								EPX[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	ERC[15:0]	All 0	R	Warning Code 0: Indicates normal termination. 1: Indicate warning status. Lists the warnings at decoding time in table 27.13 and at encoding time in table 27.14.
15 to 8	EPY[7:0]	All 0	R	Indicates the internal status This bit is for debagging. Not for the end user.
7 to 0	EPX[7:0]	All 0	R	Indicates the internal status This bit is for debugging. Not for the end user.

Table 27.13 Decode Warnings

Bit position	Symbol	Error description
20	CRO	Indicates the internal status This bit is for debugging. Not for the end user.
19	INTRA_MODE_CLIP	INTRA_MODE is used although it should not be used.
18	MV_RANGE_OVER	The MV range exceeds the specified maximum.

Table 27.14 Encode warnings

Bit position	Symbol	Error description
20	CRO	Indicates the internal status This bit is for debugging. Not for the end user.

37.2.18 Intermediate-Stream Bit Count Register 0 (VP5_CE_INT_TB0)

VP5_CE_INT_TB0 indicates the number of bits in a CE0 intermediate stream. This register becomes valid after the completion of encoding.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	VB[26:0]										
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:						R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VB[26:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 27	—	All 0	—	Reserved These bits are always read as 0. The write value should always be 0.
26 to 0	VB0[26:0]	All 0	R	Intermediate-Stream 0 Bit Count Indicate the number of bits in intermediate stream 0. (H'000 0000 to H'7FF FFFF)

37.2.19 Intermediate-Stream Bit Count Register 1 (VP5_CE_INT_TB1)

VP5_CE_INT_TB1 indicates the number of bits in a CE1 intermediate stream. This register becomes valid after the completion of encoding.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	VB[26:0]										
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VB[26:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 27	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
26 to 0	VB1[26:0]	All 0	R	Intermediate-Stream 1 Bit Count Indicate the number of bits in intermediate stream 1. (H'000 0000 to H'7FF FFFF)

37.2.20 Macroblock Attribute Register (VP5_CE_MB_ATTR)

The VP5_CE_MB_ATTR register indicates the macroblock attributes at encoding time. This register becomes valid after the completion of CE encoding.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	INTRA[12:0]												
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	INTER[12:0]												
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 16	INTRA[12:0]	All 0	R	Intra Macroblock Count Indicate the number of intra macroblocks in a picture. (0 to 8160)
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 0	INTER[12:0]	All 0	R	Inter Macroblock Count Indicate the number of inter macroblocks in a picture. (0 to 8160)

37.2.21 Macroblock Intra SAD Register (VP5_CE_MB_SADA)

The VP5_CE_MB_SADA register indicates the intra sum of absolute differences (SAD) of macroblocks at H.264 encoding time. This register becomes valid after the completion of CE encoding.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SADA[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SADA[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	SADA[31:0]	All 0	R	Intra Macroblock SAD Indicate total value of the intra SAD of macroblocks in a picture at H.264 encoding time (0 to 534,765,600). Indicates 0 other than H.264.

37.2.22 Macroblock Inter SAD Register (VP5_CE_MB_SADR)

The VP5_CE_MB_SADR register indicates the inter sum of absolute differences (SAD) of macroblocks at encoding time. This register becomes valid after the completion of CE encoding.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SADR[31:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SADR[31:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	SADR[31:0]	All 0	R	Inter Macroblock SAD Indicate total value of the inter SAD of macroblocks in a picture (0 to 534,765,600).

37.2.23 Macroblock Used SAD Register (VP5_CE_MB_USAD)

The VP5_CE_MB_USAD register indicates the sum of absolute differences (SAD) of encoded macroblocks at encoding time in H.264 encoding. This register becomes valid after the completion of CE encoding.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	USAD[31:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	USAD[31:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	USAD[31:0]	All 0	R	Used SAD Indicate total value of the SAD of macroblocks in a picture for the mode determined by intra/inter mode decision at H.264 encoding time (0 to 534,765,600). Indicates 0 other than H.264.

37.2.24 Activity Sum Register (VP5_CE_ASUM)

The VP5_CE_ASUM register indicates the sum of total activities of macroblocks. This register becomes valid after the completion of CE encoding

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	ASUM[23:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ASUM[23:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	ASUM[23:0]	All 0	R	Activity Sum Indicate the sum of total activities of macroblocks in a picture. To obtain this sum, follow these steps: [Step1] Determine the activity evaluation value act_8 × 8 for the 8 × 8 pixel block as follows. $act_8x8 = \sum_{i=0}^{63} \mid p_i - average_p \mid / 8$ where p_i is a pixel value (0 - 255) and average_p is an average of pixel values in the 8 × 8 block. [Step2] Select the minimum from the activity evaluation values of the four 8 × 8 pixel blocks in the macroblock. [Step3] Determine the sum of the total activities for the macroblocks in one picture.

37.2.25 Activity Register (VP5_CE_ACT)

The VP5_CE_ACT register indicates the maximum and minimum values for activities of macroblocks for encoding. This register becomes valid after the completion of encoding.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	AMAX[10:0]										
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	AMIN[10:0]										
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 27	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
26 to 16	AMAX[10:0]	All 0	R	Activity Maximum Value Indicate the maximum value for activities of macroblocks in a picture. (0 to 2,040) For information about the activity evaluation formula for macroblocks, refer to the VP5_CE_ASUM register description.
15 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 0	AMIN[10:0]	All 0	R	Activity Minimum Value Indicate the minimum value for activities of macroblocks in a picture. (0 to 2,040) For information about the activity evaluation formula for macroblocks, refer to the VP5_CE_ASUM register description.

37.2.26 Quantization Coefficient Sum Register (VP5_CE_QSUM)

The VP5_CE_QSUM register indicates the sum of quantization coefficients for pictures at encoding time. This register becomes valid after the completion of encoding.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	QSUM[18:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:														R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	QSUM[18:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 19	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
18 to 0	QSUM[18:0]	All 0	R	Quantization Coefficient Sum Sum of picture quantization coefficients (0 to 416, 160)

37.2.27 Virtual Buffer Register (VP5_CE_DJS)

The VP5_CE_DJS register indicates the virtual buffer value which is available after encoding. This register becomes valid after the completion of encoding.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DJ[31:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DJ[31:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DJ[31:0]	All 0	R	Virtual Buffer Indicate the virtual buffer amount (signed) which is reached after encoding. (-2,147,483,658 to 2,147,483,657) These bits are valid when macroblock-level quantization parameter control based on TM5 step 2 is provided (i.e., when dq_disable in the VP5_CE_ENC_CTRL register is 0). The virtual buffer is updated for each macroblock by using the formula below. The virtual buffer's updated value after picture processing is reflected in this register. Virtual buffer (j) = Virtual buffer (j-1) + Intermediate code amount - Target code amount where j indicates a macroblock number.

37.2.28 MB Average Luminance Sum Register (VP5_CE_YSUM)

The VP5_CE_YSUM register indicates the total value of macroblock average for luminance at encoding time. This register becomes valid after the completion of encoding.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	YSUM[24:16]								
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	YSUM[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	—	Reserved These bits are always read as 0. The write value should always be 0.
24 to 0	YSUM[24:0]	All 0	R	Macroblock Luminance Average Sum Sum of the macroblock luminance average (0 to 2,080,800)

37.2.29 VLCS Firmware-Based Address Register (VP5_VLC_MBA)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VMBA[31:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VMBA[31:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	VMBA[31:0]	All 0	R/W	VLCS Microcode-Based Address Specification These bits specify the start address in 32-byte units for storing the VLCS microcode. Before starting the VLCS in the VPU5HG, place the microcode (initialization routine format) in the address specified in this register.

37.2.30 VLCS Parameter-Based Address Register 0 (VP5_VLC_PBA0)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VPBA[31:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VPBA[31:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	VPBA0[31:0]	All 0	R/W	VLCS Parameter-Based Address Specification These bits specify the start address in 32-byte units for storing the VLCS operation control parameter. Before starting the VLCS in the VPU5HG, place the operation control parameter (initialization routine format) in the address specified in this register.

37.2.31 VLCS Parameter-Based Address Register 1 (VP5_VLC_PBA1)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VPBA[31:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VPBA[31:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	VPBA1[31:0]	All 0	R/W	VLCS Parameter-Based Address Specification These bits specify the start address in 32-byte units for storing the VLCS operation control parameter. Before starting the VLCS in the VPU5HG, place the operation control parameter (initialization routine format) in the address specified in this register.

37.2.32 Picture Byte Count Register (VP5_VLC_TB)

The VP5_VLC_TB register indicates the number of bytes which exist after picture processing. This register becomes valid after the completion of VLCS encoding, decoding.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TB[31:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TB[31:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	TB[31:0]	All 0	R	Total Bytes Indicate the number of processing bytes which exist after picture processing (0 to 4294967295). At encoding time, these bits indicate the number of bytes output by processing data (in units of pictures) via the overall VLCS operation. They include bytes output before the stream for alignment. They also include inserted emulation prevention bytes. That number does not include the size of a slice if the processing of the slice was aborted due to a fatal error during the encoding by the VLCS. At decoding time, these bits indicate the number of bytes which the VLCS referenced for processing the last slice. They include padding bytes preceding the slice. They also include deleted emulation prevention bytes. They do not include cabac_zero_word. If processing of the slice was aborted due to a fatal error, these bits indicate the number of bytes for the portion which was subject to getbit processing before the abortion (any fractions are rounded off).

37.2.33 VLCS Status Register H (VP5_VLC_ERRH)

The VP5_VLC_ERRH register indicates the error and warning status after the completion of the VLCS operation. The status bits vary depending on the operation mode. If two or more errors or warnings are detected, this register provides information about the error or warning at the highest level of seriousness (ELVL). If they are at the same level of seriousness, this register provides information about the first error or warning detected. The values in this register are determined after the completion of operation.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	ESRC[1:0]		ELVL[1:0]		SN[10:0]										
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MBH[7:0]								MBV[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R		R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
30, 29	ESRC[1:0]	00	R	VLCS Block Where Error/Warning Was Detected 00: No error/warning detected 01: Error/warning detected in the VLCS CTL 10: Error/warning detected in the STX 11: Error/warning detected in the CABAC
28, 27	ELVL[1:0]	00	R	Error/Warning Level 00: No error/warning detected 01: Warning. (A problem was detected, but it was ignored and processing continued.) 10: Error. (Concealment was applied and processing coninued.) 11: Fatal error. (Execution stopped.)

Bit	Bit Name	Initial Value	R/W	Description
26 to 16	SN[10:0]	All 0	R	Error Processing Termination Slice Number Indicate the number (0 to 2,047) of a slice which caused an error/warning for H.264 processing. 0 corresponds to the first slice. These bits are invalid and are always read as 0 for processing non-H.264 content.
15 to 8	MBH[7:0]	All 0	R	MB H Position Horizontal position of an MB which caused an error/warning. (0 to 119)
7 to 0	MBV[7:0]	All 0	R	MB V Position Vertical position of an MB which caused an error/warning. (0 to 67)

37.2.34 VLCS Status Register (VP5_VLC_ERRL)

The VP5_VLC_ERRL register indicates the error and warning status after the completion of the VLCS operation. The status bits vary depending on the operation mode. If two or more errors or warnings are detected, this register provides information about the error or warning at the highest level of seriousness (ELVL). If the errors or warnings are at the same level of seriousness, this register provides information about the first error or warning detected. The values in this register are determined after the completion of operation.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ERC[5:0]							SBCV[25:0]								
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SBCV[25:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 26	ERC[5:0]	H'00	R	Error Code Indicate error code. The code varies depending on the ESRC bits in the VP5_VLC_ERRH register. If the ESRC bit indicates STX or CABAC, the code is the number of the syntax element which is the major cause of the problem. For details, refer to table 27.15 to 27.19.
25 to 0	SBCV[25:0]	H'000 0000	R	Indicate the error occurrence position by using the number of reference bits starting at the beginning of the picture. At encoding time, these bits indicate the number of bytes which exist before inserting the emulation prevention byte. At decoding time, they indicate the number of bytes which exist after deleting the emulation prevention byte. Thus, they do not indicate the address of stream data in memory when using the function to insert/delete the emulation prevention byte.

Table 27.15 Error Codes (Not Depending on Codec)

ESRC	ELVL	ERC	Error description
00	00	H'00	Normal termination
01	10	H'01	Unconsecutive macroblock start addresses were detected. (Slices were ignored because their overlapping was detected.) This error is not detected if the I bit for the command stream is 1 at decoding time. (This is because the internal macroblock address counter is forcibly set to the specified value in the command stream.) This error is not detected at encoding time.
01	10	H'02	Unconsecutive macroblock start addresses were detected. (Unconsecutive macroblocks were detected, and the required macroblock was output as an error macroblock.) This error is not detected if the I bit for the command stream is 1 at decoding time. (This is because the internal counter is forcibly set to the specified value in the command stream.) This error is not detected at encoding time.
01	10	H'03	When a command stream was used for decoding, the VOP last macroblock (lower right) was not detected in the last slice.
01	10	H'04	At decoding time, an attempt was made to process a macroblock larger than a range of screen sizes, and the slice was ignored.
01	10	H'05	When a command stream was used for decoding, the processing was completed without the command for the last slice.
01	11	H'3D	When operation for a channel could not continue, LDMAC write buffer full status was detected in that channel. (Write buffer overflow)
01	11	H'3E	Abnormal command was detected in a command stream.
01	11	H'3F	Abnormal word count was detected in a command stream. (Up to 1023 command words/slice)

Table 27.16 Error Codes (H.264 Processing)

ESRC	ELVL	ERC	Error description
10	10	H'01	The mb_skip_run value exceeded the number of remaining MBs.
10	10	H'02	The mb_type value exceeded the specifiable range.
10	10	H'03	The sub_mb_type value exceeded the specifiable range.
10	10	H'04	The intra_chroma_pred_mode value exceeded the specifiable range.
10	10	H'05	The ref_idx value exceeded the specifiable range.
10	10	H'06	The mvd value exceeded the specifiable range.
10	10	H'08	The coded_block_pattern value exceeded the specifiable range.
10	10	H'09	The mb_qp_delta value exceeded the specifiable range.
10	10	H'0A	A bit row not found in the table was specified for coeff_token.
10	10	H'0B	A value out of the correct range was specified for total_coeff.
10	10	H'0C	The level value exceeded the specifiable range.
10	10	H'0D	A bit row not found in the table was specified for total_zeros.
10	10	H'0E	A value out of the correct range was specified for total_zeros.
10	10	H'0F	A bit row not found in the table was specified for run_before.
10	10	H'10	A value out of the correct range was specified for run_before.
10	01	H'11	An illegal value was specified for pcm_alignment_zero_bit.
10	01	H'12	An illegal value was specified for rbsp_stop_one_bit or rbsp_alignment_zen_bit.
11	01	H'01	An illegal value was specified for cabac_alignment_one_bit.
11	10	H'02	The ref_idx value exceeded the specifiable range.
11	10	H'03	The mvd value exceeded the specifiable range.
11	10	H'05	The mb_qp_delta value exceeded the specifiable range.
11	10	H'06	The level value exceeded the specifiable range.
10	10	H'07	An illegal value was specified for end_of_slice_flag.
11	01	H'08	An illegal value was specified for pcm_alignment_zero_bit.
11	01	H'09	An illegal value was specified for rbsp_stop_one_bit or rbsp_alignment_zero_bit.
10	11	N/A	The intermediate stream was illegal at encoding time. Not enough buffer space might be available to read necessary data. The ERC value is for debugging. Not for the end user.

ESRC	ELVL	ERC	Error description
10	01	H'02	The code amount per MB exceeded the specified value at encoding time.
11	11	H'01	The intermediate stream was illegal at encoding time (i.e., during CABAC processing). Not enough buffer space might be available to read necessary data.
11	01	H'02	The code amount per MB exceeded the specified value at encoding time (i.e., during CABAC processing).

Table 27.17 Error Codes (MPEG-2/MPEG-1 Processing)

ESRC	ELVL	ERC	Error description
10	10	H'01	An illegal value was specified for slice_start_code.
10	10	H'02	An illegal value was specified for quantiser_scale_code.
10	10	H'03	The macroblock address exceeded the number of macroblock in a picture.
10	10	H'04	A bit row not found in the table was specified for macroblock_address_increment.
10	10	H'05	A bit row not found in the table was specified for macroblock_type.
10	10	H'06	frame_motion_type/field_motion_type value exceeded the specifiable range.
10	10	H'07	A bit row not found in the table was specified for motion_code.
10	10	H'08	A bit row not found in the table was specified for coded_block_pattern.
10	10	H'09	A bit row not found in the table was specified for the DC coefficient of a non-intra MB. .
10	10	H'0A	The AC coefficient value exceeded the specifiable range.
10	10	H'0B	A bit row not found in the table was specified for the AC coefficient.
10	10	H'0C	The LEVEL value of ESCAPE code was specified 0 (setting 0 is prohibited).
10	10	H'0D	slice_vertical_position is incorrect.
10	01	H'10	marker_bit was not a correct value.
10	01	H'11	The size had been GetBit was exceeded the slice size which was specified by the slice parameter.
10	01	H'12	A non-zero value exists in byte alignment.

ESRC	ELVL	ERC	Error description
10	11	N/A	The intermediate stream was illegal at encoding time. Not enough buffer space might be available to read necessary data. The ERC value is for debugging. Not for the end user.

Table 27.18 Error Codes (MPEG-4/H.263 Processing)

ESRC	ELVL	ERC	Error description
10	10	H'01	mcbpc exceeded the specifiable range.
10	10	H'02	mb_type(B) exceeded the specifiable range.
10	10	H'03	cbpy(intraMB) exceeded the specifiable range.
10	10	H'04	cbpy(interMB) exceeded the specifiable range.
10	10	H'05	cbpb exceeded the specifiable range.
10	10	H'06	horizontal_mv_data or vertical_mv_data was not found in the table.
10	10	H'07	dct_dc_size_luminance, dct_dc_size_chrominance were not found in the table.
10	10	H'08	AC coefficient of the intraMB was not found in the table.
10	10	H'09	AC coefficient of the interMB was not found in the table.
10	10	H'0a	escape type1 and type2 indicated the error, which was not found in the table.
10	10	H'0b	Indicated 64 coefficients were in per block.
10	10	H'0c	Indicated the VP header quantization parameter was 0.
10	10	H'0d	macroblock_number in VP didn't match with the location of MB at currently decoding.
10	10	H'0e	modulo_time_base was an illegal value. (0 was read 256 times or more, or contents didn't match with the one in VOP headder.)
10	10	H'0f	The vop_coding_type value in the VP did not match the vop_coding_type value in the VOP.
10	10	H'10	intra_dc_vlc_thr value in VP didn't match with the value of intra_dc_vlc_thr value in VOP.
10	01	H'11	vop_fcode_forward value in VP didn't match with the value of vop_fcode_forward in VOP.
10	01	H'12	vop_fcode_backward value in VP, modulo = time = basesaan didn't match with the value of vop_fcode_backward in VOP.
11	01	H'13	gob_number in gob_layer didn't match with GOB number at currently decoding.

ESRC	ELVL	ERC	Error description
11	10	H'14	The quantization parameter in gob_layer was 0.
11	10	H'15	At Data Partition (DP) decoding time, mcbpc exceeded the specifiable range.
11	10	H'16	At DP decoding time, cbpy(intraMB) exceeded the specifiable range.
11	10	H'17	At DP decoding time, cbpy(interMB) exceeded the specifiable range.
11	10	H'18	At DP decoding time, horizontal_mv_data or verticatl_mv_data were not found in the table.
11	01	H'19	At DP decoding time, dct_dc_size, dct_dc_size_chrominance were not found in the table.
11	01	H'1a	At RVLC decoding time, the second ESCAPE code was an illegal value.
10	11	H'1b	At DP decoding time, the number of MBs of DP3 were more than the number of MBs of video packet.
10	01	H'1c	DC marker was not detected at DP decoding time.
10	10	H'1d	At DP decoding time, MOTION marker was not detected.
10	10	H'1e	At DP decoding time, The number of MBs of DP3 were more than the number of MBs of video packet.
10	01	H'30	Marker bit was 0.
10	01	H'31	The coefficient was out of range in coefficient escape code processing.
10	01	H'32	DC coefficient was out of range in H.263 processing.
10	01	H'33	The size had been GetBit was exceeded the slice size specified by the slice parameter.
10	11	N/A	The intermediate stream was illegal at encoding time. Not enough buffer space might be available to read necessary data. The ERC value is for debugging. Not for the end user.
10	01	H'02	The video packet size exceeded the size specified by VP5_VLC_SH: word 16 at DP encoding time.
10	11	H'03	The DP buffer of VLC_S was overflow at DP encoding time. The stream might be got damages.

Table 27.19 Error Codes (VC-1 Processing)

ESRC	ELVL	ERC	Error description
10	10	H'01	cbpcy (I) was outside of the table range.
10	10	H'02	cbpcy (P, 1-MV) was outside of the table range.
10	10	H'03	cbpcy (P, 4-MV) was outside of the table range.
10	10	H'04	cbpcy (B) was outside of the table range.
10	10	H'05	bmvtype was illegal.
10	10	H'06	TTMB was outside of the table range.
10	10	H'08	TTBLK was outside of the table range.
10	10	H'0a	SUBBLKPAT was outside of the table range.
10	10	H'0a	MVDATA was outside of the table range.
10	10	H'10	There were 64 or more coefficients in a single block.
10	10	H'11	The DC coefficient was outside of the table range.
10	10	H'12	When the AC coefficient was Escape code, an Escape code was furthermore included.
10	10	H'13	The mode of coefficient Escape was outside of the table range.
10	10	H'14	The AC coefficient for Escape was outside of the table range.
10	10	H'15	Run or Level for Escape was outside of the table range.
10	01	H'16	The AC coefficient of the inter MB was outside of the table range.
10	10	H'17	The coefficient value of Escape Type 3 was 0.
10	10	H'18	The MQUANT range exceeded the range between 1 and 31.
10	10	H'19	The ABSMQ value was 0.
10	10	H'30	SLICE_ADDR was illegal (Advanced Profile) or Syncmarker was illegal (Simple/Main Profile).
10	01	H'33	The GetBit size exceeded the slice size specified by the slice parameter.

37.2.35 Intermediate Stream Bit Count Register 0 (VP5_VLC_INT_TB0)

The VP5_VLC_INT_TB0 register indicates the number of bits in an intermediate stream for CE0. This register becomes valid after the completion of decoding or .

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	VB[26:0]										
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VB[26:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 27	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
26 to 0	VB0[26:0]	All 0	R	Number of Bits in Intermediate Stream 0 Indicate the number of bits in intermediate steam 0 (H'000 0000 to H'7FF FFFF).

37.2.36 Intermediate Stream Bit Count Register 1 (VP5_VLC_INT_TB1)

The VP5_VLC_INT_TB1 register indicates the number of bits in an intermediate stream for CE1. This register becomes valid after the completion of decoding or .

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	VB[26:0]										
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VB[26:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 27	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
26 to 0	VB1[26:0]	All 0	R	Intermediate Stream Number of 1-bit Indicates the number of 1-bit in intermediate stream. (H'000 0000 to H'7FF FFFF)

37.3 VPU5HG Internal Register Descriptions

The VPU5HG internal registers are 64-bit access registers configured by the initialization routine. Before starting the VPU5HG, values should be stored in the predetermined format shown in section 6.2.2 in the external memory. For operation involving the two CEs, the initialization routine uses two channels: GDMAC channel 0 and channel 1. For operation involving one of these CEs, the initialization routine uses only GDMAC channel 0. Specify the values in the format for each channel in the order shown in this manual. A failure to follow this order might cause a malfunction. If any registers need not be set, it is not problematic to skip the registers while specifying the values. Note that the VPU5HG internal registers might be updated by the VPU5HG during operation. Even if the settings for these registers are the same as before, be sure to reset these registers.

VP5_BAAR0 and VP5_BAAR1 should be set when starting the picture processing module (CE) or code processing module (VLCS) according to the setting category shown in table 27.20 and 27.28. Registers with names which are prefixed with "VP5_CE" should be set when starting the CE. Registers with names which are prefixed with "VP5_VLC" should be set when starting the VLCS.

37.3.1 Base Address Array Register 0 (VP5_BAAR0)

This register specifies the base address of external memory which the VPU5HG should access. The parameters in this register are required when starting the VLCS or CE. Table 27.20 lists the specifiable base addresses.

Common bit fields are available for the base addresses shown in table 27.20.

Table 27.20 Description of Base Address Array 0

No.	Address Offset	Setting Category	Associated DMA Channel	Description	Remarks
8	H'040	CE	DECY0	Decode picture luminance base address	
9	H'048	CE	DECC0	Decode picture chrominance base address	
10	H'050	CE	DECBY0	Decode picture luminance base address (bottom field)	For frame structure and field picgure arrangement only
11	H'058	CE	DECBC0	Decode picture chrominance base address (bottom field)	For frame structure and field picgure arrangement only
12	H'060	CE	TMPY0	Encode picture luminance base address	For encoding which involves one CE only
13	H'068	CE	TMPC0	Encode picture chrominance base address	For encoding which involves one CE only
18	H'090	CE	MVINFO0	MV information (write) base address	
19	H'098	CE	MVINFOB0	MV information (odd MB line) (write) base address	PIC-AFF /MB-AFF
20	H'0A0	CE	MVR0	Anchor picture MV information (read) base address	
21	H'0A8	CE	MVRB0	Anchor picture MV information (odd MB line) (read) base address	PIC-AFF /MB-AFF
22	H'0B0	CE	CEIS0	CE intermediate stream base address	
23	H'0B8	CE	CEIC0	CE intermediate control stream base address	
24	H'0C0	VLCS	STRA	Stream A base address	

No.	Address Offset	Setting Category	Associated DMA Channel	Description	Remarks
25	H'0C8	VLCS	STRB	Stream B base address	
26	H'0D0	VLCS	CMDS	Command stream base address	
27	H'0D8	VLCS	VLBD	VLCS bit plane/DP base address	
28	H'0E0	VLCS	VLIS0	VLCS intermediate stream base address	
29	H'0E8	VLCS	VLIC0	VLCS intermediate control stream base address	
30	H'0F0	VLCS	CLNC	Co-location not coded base address	
31	H'0F8	VLCS	DPW	Data partition base address	
32	H'100	CE	DISPY0	Filter picture luminance base address	
33	H'108	CE	DISPC0	Filter picture chrominance base address	
34	H'110	CE	DISPBY0	Filter picture luminance base address (bottom field)	For frame structure and fied picture arrangement only
35	H'118	CE	DISPBC0	Filter picture chrominance base address (bottom field)	For frame structure and fied picture arrangement only
64	H'200	CE	REF	Reference picture luminance address 0	
65	H'208	CE	REF	Reference picture chrominance address 0	
66	H'210	CE	REF	Reference picture luminance address 1	
67	H'218	CE	REF	Reference picture chrominance address 1	
68	H'220	CE	REF	Reference picture luminance address 2	

No.	Address Offset	Setting Category	Associated DMA Channel	Description	Remarks
69	H'228	CE	REF	Reference picture chrominance address 2	
70	H'230	CE	REF	Reference picture luminance address 3	
71	H'238	CE	REF	Reference picture chrominance address 3	
72	H'240	CE	REF	Reference picture luminance address 4	
73	H'248	CE	REF	Reference picture chrominance address 4	
74	H'250	CE	REF	Reference picture luminance address 5	
75	H'258	CE	REF	Reference picture chrominance address 5	
76	H'260	CE	REF	Reference picture luminance address 6	
77	H'268	CE	REF	Reference picture chrominance address 6	
78	H'270	CE	REF	Reference picture luminance address 7	
79	H'278	CE	REF	Reference picture chrominance address 7	
80	H'280	CE	REF	Reference picture luminance address 8	
81	H'288	CE	REF	Reference picture chrominance address 8	
82	H'290	CE	REF	Reference picture luminance address 9	
83	H'298	CE	REF	Reference picture chrominance address 9	
84	H'2A0	CE	REF	Reference picture luminance address 10	
85	H'2A8	CE	REF	Reference picture chrominance address 10	
86	H'2B0	CE	REF	Reference picture luminance addr90ess 11	

No.	Address Offset	Setting Category	Associated DMA Channel	Description	Remarks
87	H'2B8	CE	REF	Reference picture chrominance address 11	
88	H'2C0	CE	REF	Reference picture luminance address 12	
59	H'2C8	CE	REF	Reference picture chrominance address 12	
90	H'2D0	CE	REF	Reference picture luminance address 13	
91	H'2D8	CE	REF	Reference picture chrominance address 13	
92	H'2E0	CE	REF	Reference picture luminance address 14	
93	H'2E8	CE	REF	Reference picture chrominance address 14	
94	H'2F0	CE	REF	Reference picture luminance address 15	
95	H'2F8	CE	REF	Reference picture chrominance address 15	
96	H'300	CE	REF	Reference picture luminance address 16	
97	H'308	CE	REF	Reference picture chrominance address 16	
98	H'310	CE	REF	Reference picture luminance address 17	
99	H'318	CE	REF	Reference picture chrominance address 17	
100	H'320	CE	REF	Reference picture luminance address 18	
101	H'328	CE	REF	Reference picture chrominance address 18	
102	H'330	CE	REF	Reference picture luminance address 19	
103	H'338	CE	REF	Reference picture chrominance address 19	
104	H'340	CE	REF	Reference picture luminance address 20	

No.	Address Offset	Setting Category	Associated DMA Channel	Description	Remarks
105	H'348	CE	REF	Reference picture chrominance address 20	
106	H'350	CE	REF	Reference picture luminance address 21	
107	H'358	CE	REF	Reference picture chrominance address 21	
108	H'360	CE	REF	Reference picture luminance address 22	
109	H'368	CE	REF	Reference picture chrominance address 22	
110	H'370	CE	REF	Reference picture luminance address 23	
111	H'378	CE	REF	Reference picture chrominance address 23	
112	H'380	CE	REF	Reference picture luminance address 24	
113	H'388	CE	REF	Reference picture chrominance address 24	
114	H'390	CE	REF	Reference picture luminance address 25	
115	H'398	CE	REF	Reference picture chrominance address 25	
116	H'3A0	CE	REF	Reference picture luminance address 26	
117	H'3A8	CE	REF	Reference picture chrominance address 26	
118	H'3B0	CE	REF	Reference picture luminance address 27	
119	H'3B8	CE	REF	Reference picture chrominance address 27	
120	H'3C0	CE	REF	Reference picture luminance address 28	
121	H'3C8	CE	REF	Reference picture chrominance address 28	
122	H'3D0	CE	REF	Reference picture luminance address 29	

No.	Address Offset	Setting Category	Associated DMA Channel	Description	Remarks
123	H'3D8	CE	REF	Reference picture chrominance address 29	
124	H'3E0	CE	REF	Reference picture luminance address 30	
125	H'3E8	CE	REF	Reference picture chrominance address 30	
126	H'3F0	CE	REF	Reference picture luminance address 31	
127	H'3F8	CE	REF	Reference picture chrominance address 31	

Table 27.21 VP5_BAAR0 Bit Fields

Bit	Name	Setting value	Description
63 to 32	BAA	Base address	32-bit base address. The smallest unit of external memory accessed at once by the VPU5HG is eight bytes. Be sure to set the low-order three bits for the address specified in BAAR to 0. The unit of alignment might be 32 bytes or more depending on the base address. Specify the base address according to the alignment.
31 to 0	reserved	Reserved	Reserved

In encoding and decoding, the intermediate stream and the intermediate stream control base address should be specified according to the case listed as follows.

At the time of 2-CE encoding, CE output address is specified in the base address of the intermediate stream and the intermediate stream control to be set in VLCS as follows.

VP5_BAAR0.CEIS0 → VP5_BAAR1.VLIS1

VP5_VAAR0.CEIC0 → VP5_BAAR1.VLIC1

VP5_BAAR1.CEIS1 → VP5_BAAR0.VLIS0

VP5_BAAR1.CEIC1 → VP5_BAAR0.VLIC0

At the time of 1-CE encoding (in MPEG-4/H.263 format only), CE output address is specified in the base address of the intermediate stream and the intermediate stream control to be set in VLCS as follows.

VP5_BAAR0.CEIS0 → VP5_BAAR0.VLIS0

VP5_BAAR0.CEIC0 → VP5_BAAR0.VLIC0

At decoding time, VLCS output address is specified in the base address of the intermediate stream and the intermediate stream control to be set CE as follows.

VP5_BAAR0.VLIS0 → VP5_BAAR0.CEIS0

VP5_BAAR0.VLIC0 → VP5_BAAR0.CEIC0

VP5_BAAR1.VLIS1 → VP5_BAAR1.CEIS1

VP5_BAAR1.VLIC1 → VP5_BAAR1.CEIC1

In encoding and decoding, the MV information base address should be specified according to the case listed as follows.

At the time of 2-CE encoding time, MV information base address is specified as follows.

Anchor flame: VP5_BAAR0.MVINFO0 → VP5_BAAR1.MVR1

Anchor flame: VP5_BAAR0.MVINFOB0 → VP5_BAAR1.MVRB1

Anchor flame: VP5_BAAR1.MVINFO1 → VP5_BAAR0.MVR0

Anchor flame: VP5_BAAR1.MVINFOB1 → VP5_BAAR0.MVRB0

At the time of 1-CE encoding (in MPEG-4/H.263 format only), MV information base address is specified as follows.

Anchor flame: VP5_BAAR0.MVINFO0 → VP5_BAAR0.MVR0

At decoding time, MV information base address is specified as follows.

Anchor flame: VP5_BAAR0.MVINFO0 → VP5_BAAR0.MVR0

Anchor flame: VP5_BAAR0.MVINFOB0 → VP5_BAAR0.MVRB0

Anchor flame: VP5_BAAR1.MVINFO1 → VP5_BAAR1.MVR1

Anchor flame: VP5_BAAR1.MVINFOB1 → VP5_BAAR1.MVRB1

Figure 27.2 shows how to set reference picture addresses for MPEG-2/MPEG-4/H.263 decoding.

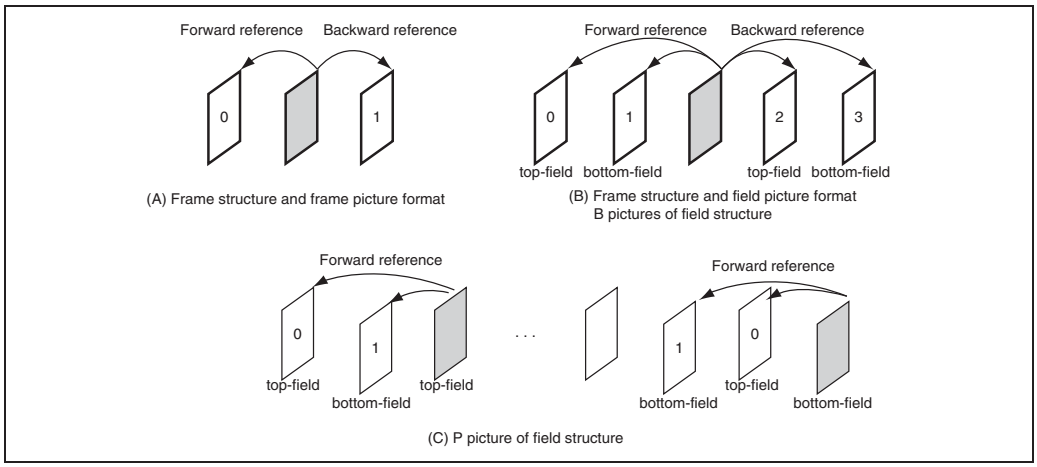


Figure 27.2 Setting Reference Picture Addresses for MPEG2/MPEG4/H.263 Decoding

For MPEG-4/H.263 processing, set the addresses by associating the numbers shown in figure 27.2 with reference picture address n (n = 0, 1) for items 64 through 67 in table 27.20.

In the case of MPEG-2, the method for reference picture address setting varies depending on the structure (frame/field) of streams to be decoded and on the format (frame/field) of pictures in external RAM. For the frame structure and frame picture format, this method is the same as that for MPEG-4 processing. For the frame structure and field picture format or for B pictures of field structure, there are up to four reference pictures as shown in figure 27.2 and thus set the addresses by associating the numbers shown in figure 27.2 with reference picture address n (N = 0, 1, 2, 3) for items 64 through 71 in table 27.20. For P pictures of field structure, be sure to set the last decoded top and bottom fields as shown in figure 27.2.

Figure 27.3 shows how to set reference picture addresses for VC-1 decoding.

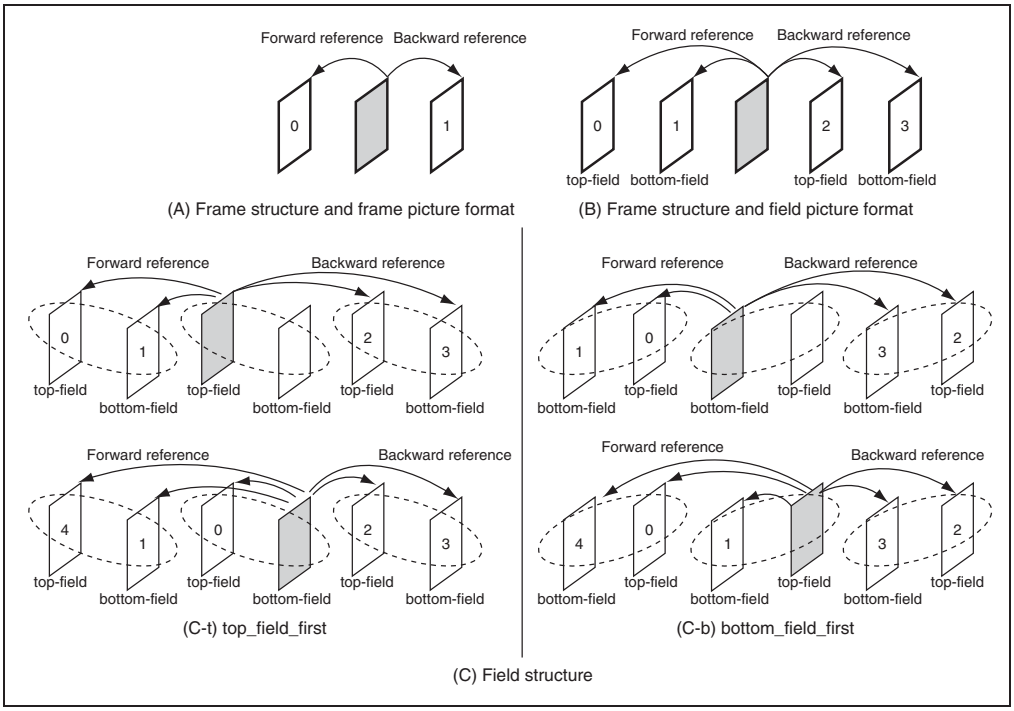


Figure 27.3 Setting Reference Picture Addresses for VC-1 Decoding

In the case of VC-1, the method for reference picture address setting varies depending on the structure (frame/field) of streams to be decoded and on the format (frame/field) of pictures in external RAM. For the frame structure (figure 27.3), this method is the same as that for MPEG-2 processing. For the field structure, there is a need for five reference pictures (three for P pictures) as shown in figure 27.3 and thus set the addresses by associating the numbers shown in figure 27.3 with reference picture address n (n = 0, 1, 2, 3, 4) for items 64 through 73 in table 27.20.

For B picture field encoding, set the references so that the same parity is used for reference.

37.3.2 Decode Luminance Picture DMA Channel Register 0 (VP5_CE_DCHR_DECY0)

This register specifies the operation of the DMA channel (DECY0) to output decode luminance pictures or local decode luminance pictures. The parameters in this register are required when starting the CE.

Bit	Name	Setting value	Description
63 to 48	(reserved)	H'D000	Always set to this value.
47 to 43	(reserved)	0	Always set to this value.
42 to 32	hsize		Horizontal size of the picture area. (The bits are set to a value rounded up to a multiple 16 and divided by 8.) Set the bits to twice the horizontal size of the picture area size when storing frame pictures in external memory for field encoding/decoding.
31 to 16	(reserved)	H'0000	Always set to this value.
15 to 13	endian	0 to 7	Endian. (Refer to table 27.22)
12 to 9	src_offset	4	Set to 4 for the VPU5HG.
8 to 0	(reserved)	8	Always set to this value.

Bits 15:13 make endian settings. Bit 15 specifies interchanging data in byte units, bit 14 interchanging data in word (16-bit) units, and bit 13 interchanging data in long-word (32-bit) units. Similar bit specifications are given for the other DMA channels.

Table 27.22 DMA Channel Register Endian Settings

Bits 15 to 13			
B	**W**	**LW**	**Byte Order**
0	0	0	12345678 (Big endian)
0	0	1	56781234
0	1	0	34127856
0	1	1	78563412
1	0	0	21436587
1	0	1	65872143
1	1	0	43218765
1	1	1	87654321 (Little endian)

37.3.3 Decode Chrominance Picture DMA Channel Register 0 (VP5_CE_DCHR_DECC0)

This register specifies the operation of the DMA channel (DECC0) to output decode chrominance pictures or local decode chrominance pictures. The parameters in this register are required when starting the CE.

Bit	Name	Setting value	Description
63 to 48	(reserved)	H'D000	Always set to this value.
47 to 43	(reserved)	H'0	Always set to this value.
42 to 32	hsize		Horizontal size of the picture area. (The bits are set to a value rounded up to a multiple 16 and divided by 8.) Set the bits to twice the horizontal size of the picture area size when storing frame pictures in external memory for field encoding/decoding.
31 to 16	(reserved)	H'0000	Always set to this value.
15 to 13	endian	0 to 7	Endian. (Refer to table 27.22)
12 to 9	src_offset	4	Set to 4 for the VPU5HG.
8 to 0	(reserved)	9	Always set to this value.

37.3.4 Filter Luminance Picture DMA Channel Register 0 (VP5_CE_DCHR_DISPY0

This register specifies the operation of the DMA channel (DISPY0) to output filter luminance pictures. The parameters in this register are required when starting the CE using at MPEG-1/-2/-4 or H.263. They are also required when starting the CE for VC-1 RangeReduction or RangeMapping stream decoding.

Bit	Name	Setting value	Description
(reserved)	63 to 48	H'D000	Always set to this value.
(reserved)	47 to 43	All 0	Always set to this value.
hsize	42 to 32		Horizontal size of the picture area. (The bits are set to a value rounded up to a multiple 16 and divided by 8.) Set the bits to twice the horizontal size of the picture area size when storing frame pictures in external memory for field encoding/decoding.
(reserved)	31 to 16	All 0	Always set to this value.
endian	15 to 13	0 to 7	Endian. (Refer to table 27.22)
src_offset	12 to 9	5	Set to 5 for the VPU5HG.
(reserved)	8 to 0	32	Always set to this value.

37.3.5 Filter Chrominance Picture DMA Channel Register 0 (VP5_CE_DCHR_DISPC0)

This register specifies the operation of the DMA channel (DISPY0) to output filter chrominance pictures. The parameters in this register are required when starting the CE using at MPEG-1/-2/-4 or H.263. They are also required when starting the CE for VC-1 RangeReduction or RangeMapping stream decoding.

Bit	Name	Setting value	Description
(reserved)	63 to 48	H'D000	Always set to this value.
(reserved)	47 to 43	All 0	Always set to this value.
hsize	42 to 32		Horizontal size of the picture area. (The bits are set to a value rounded up to a multiple 16 and divided by 8.) Set the bits to twice the horizontal size of the picture area size when storing frame pictures in external memory for field encoding/decoding.
(reserved)	31 to 16	All 0	Always set to this value.
endian	15 to 13	0 to 7	Endian. (Refer to table 27.22)
src_offset	12 to 9	5	Set to 5 for the VPU5HG.
(reserved)	8 to 0	33	Always set to this value.

37.3.6 Reference Picture DMA Channel Register (VP5_CE_DCHR_REF)

This register specifies the operation of the DMA channel (REF) to read reference pictures (references). The parameters in this register are required when starting the CE. There is not always a need to set this register for I pictures. Setting it for I pictures is only necessary if decoding involves inter-error concealment (i.e., VP5_CE_VLCF.ec_mode = 1).

Bit	Name	Setting value	Description
63 to 48	(reserved)	H'B000	Always set to this value.
47 to 43	(reserved)	H'0	Always set to this value.
42 to 32	hsize		Horizontal size of the picture area. (The bits are set to a value rounded up to a multiple 16 and divided by 8.) Set the bits to twice the horizontal size of the picture area size when the reference pictures are stored as frame pictures in external memory for field encoding/decoding.
31 to 16	(reserved)	H'0000	Always set to this value.
15 to 13	endian	0 to 7	Endian. (Refer to table 27.22)
12 to 9	src_offset	1	Set to 1 for decoding and 15 for encoding.
8 to 0	(reserved)	0	Always set to this value.

37.3.7 Encode Picture DMA Channel Register 0 (VP5_CE_DCHR_TMP0)

This register specifies the operation of the DMA channel (TMP0) to read encode pictures (templates) when encoding involves one CE. The parameters in this register are required when starting the CE. Setting these parameters is unnecessary for decoding.

For encoding which involves the two CEs, use VP5_CE_DCHR_TMP1 only.

Bit	Name	Setting value	Description
63 to 48	(reserved)	H'B000	Always set to this value.
47 to 43	(reserved)	0	Always set to this value.
42 to 32	hsize	64, 128, 256	Horizontal size of the picture area. (The bits are set to a value rounded up to a multiple 16 and divided by 8.) Set the bits to twice the horizontal size of the picture area size when the encode pictures are stored as frame pictures in external memory for field encoding/decoding.
31 to 16	(reserved)	H'0000	Always set to this value.
15 to 13	endian	0 to 7	Endian (refer to table 27.22.)
12 to 9	src_offset	0	Set to 0.
8 to 0	(reserved)	0	Always set to this value.

37.3.8 MV Information Output DMA Channel Register 0 (VP5_CE_DCHR_MVINFO0)

This register specifies the operation of the DMA channel (MVINFO0) to output MV information. The parameters in this register are required when starting the CE. Do not set this register when outputting no MV information.

Bit	Name	Setting value	Description
63 to 32	(reserved)	H'C000 0000	Always set to this value.
31 to 16	(reserved)	H'0000	Always set to this value.
15 to 13	endian	0 to 7	Endian. (Refer to table 27.22)
12 to 9	src_offset	6	Set to 6 for the VPU5HG.
8 to 0	(reserved)	18	Always set to this value.

37.3.9 MB Odd Line MV Information DMA Channel Register 0 (VP5_CE_DCHR_MVINFOB0)

In H.264 PIC-AFF, this register specifies the operation of the DMA channel (MVINFO0) to output MB odd line MV information. The parameters in this register are required when starting the CE. Setting is not necessary when MV information is not to be output.

Bit	Name	Setting value	Description
63 to 32	(reserved)	H'C000 0000	Always set to this value.
31 to 16	(reserved)	H'0000	Always set to this value.
15 to 13	endian	0 to 7	Endian. (Refer to table 27.22)
12 to 9	src_offset	6	Set to 6 for the VPU5HG.
8 to 0	(reserved)	19	Always set to this value.

37.3.10 Anchor Picture MV Information DMA Channel Register 0 (VP5_CE_DCHR_MVR0)

This register specifies the operation of the DMA channel (MVR0) to read anchor picture MV information. At encoding mode time, the register setting is executed at the same time with accessing to the external memory. So that the setting is prohibited when the anchor picture MV information is not used.

- Setting for decoding

Bit	Name	Setting value	Description
63 to 32	(reserved)	H'0890 7000	Always set to this value.
31 to 16	(reserved)	H'0000	Always set to this value.
15 to 13	endian	0 to 7	Endian. (Refer to table 27.22)
12 to 9	src_offset	7	Set to 7 for the VPU5HG.
8 to 0	(reserved)	20	Always set to this value.

- Setting for encoding

Bit	Name	Setting value	Description
63 to 32	(reserved)	H'8890 7000	Always set to this value.
31 to 16	(reserved)	H'0000	Always set to this value.
15 to 13	endian	0 to 7	Endian. (Refer to table 27.22)
12 to 9	src_offset	7	Set to 7 for the VPU5HG.
8 to 0	(reserved)	20	Always set to this value.

37.3.11 Anchor Picture MB Odd Line MV Information DMA Channel Register 0 (VP5_CE_DCHR_MVRB0)

In H.264 PIC-AFF or MB-AFF, this register specifies the operation of the DMA channel (MVRB0) to read anchor picture MV information of MB odd line. At encoding time, the register setting is executed at the same time with accessing to the external memory. So that the setting is prohibited when the anchor picture MV information is not used.

- Setting for decoding

Bit	Name	Setting value	Description
63 to 32	(reserved)	H'0898 7000	Always set to this value.
31 to 16	(reserved)	H'0000	Always set to this value.
15 to 13	endian	0 to 7	Endian. (Refer to table 27.22)
12 to 9	src_offset	7	Set to 7 for the VPU5HG.
8 to 0	(reserved)	21	Always set to this value.

- Setting for encoding

Bit	Name	Setting value	Description
63 to 32	(reserved)	H'8898 7000	Always set to this value.
31 to 16	(reserved)	H'0000	Always set to this value.
15 to 13	endian	0 to 7	Endian. (Refer to table 27.22)
12 to 9	src_offset	7	Set to 7 for the VPU5HG.
8 to 0	(reserved)	21	Always set to this value.

37.3.12 CE Intermediate Stream DMA Channel Register 0 (VP5_CE_DCHR_CEIS0)

This register specifies the operation of the DMA channel (CEIS0) which allows the CE to input/output intermediate streams. The parameters in this register are required when starting the CE.

- Setting for decoding

Bit	Name	Setting value	Description
63 to 32	(reserved)	H'8880 7000	Always set to this value.
31 to 16	(reserved)	H'0000	Always set to this value.
15 to 13	endian	0 to 7	Endian. (Refer to table 27.22)
12 to 9	src_offset	8	Set to 8 for the VPU5HG.
8 to 0	(reserved)	22	Always set to this value.

- Setting for encoding

Bit	Name	Setting value	Description
63 to 32	(reserved)	H'C000 0000	Always set to this value.
31 to 16	(reserved)	H'0000	Always set to this value.
15 to 13	endian	0 to 7	Endian. (Refer to table 27.22)
12 to 9	src_offset	8	Set to 8 for the VPU5HG.
8 to 0	(reserved)	22	Always set to this value.

37.3.13 CE Intermediate Control Stream DMA Channel Register 0 (VP5_CE_DCHR_CEIC0)

This register specifies the operation of the DMA channel (CEIC0) which allows the CE to input/output intermediate control streams. The parameters in this register are required when starting the CE.

- Setting for decoding

Bit	Name	Setting value	Description
63 to 32	(reserved)	H'8888 7000	Always set to this value.
31 to 16	(reserved)	H'0000	Always set to this value.
15 to 13	endian	0 to 7	Endian. (Refer to table 27.22)
12 to 9	src_offset	8	Set to 8 for the VPU5HG.
8 to 0	(reserved)	23	Always set to this value.

- Setting for encoding

Bit	Name	Setting value	Description
63 to 32	(reserved)	H'C000 0000	Always set to this value.
31 to 16	(reserved)	H'0000	Always set to this value.
15 to 13	endian	0 to 7	Endian. (Refer to table 27.22)
12 to 9	src_offset	8	Set to 8 for the VPU5HG.
8 to 0	(reserved)	23	Always set to this value.

37.3.14 Stream A DMA Channel Register (VP5_VLC_DCHR_STRA)

This register specifies the operation of the DMA channel (STRA) which allows the VLCS to input/output streams. The parameters in this register are required when starting the VLCS.

- Setting for decoding

Bit	Name	Setting value	Description
63 to 32	(reserved)	H'08A0 7000	Always set to this value.
31 to 16	(reserved)	H'0000	Always set to this value.
15 to 13	endian	0 to 7	Endian. (Refer to table 27.22)
12 to 9	src_offset	10	Set to 10 for the VPU5HG.
8 to 0	(reserved)	24	Always set to this value.

- Setting for encoding

Bit	Name	Setting value	Description
63 to 32	(reserved)	H'C000 0000	Always set to this value.
31 to 16	(reserved)	H'0000	Always set to this value.
15 to 13	endian	0 to 7	Endian. (Refer to table 27.22)
12 to 9	src_offset	10	Set to 10 for the VPU5HG.
8 to 0	(reserved)	24	Always set to this value.

37.3.15 Stream B DMA Channel Register (VP5_VLC_DCHR_STRB)

At decoding time, this register specifies the operation of the DMA channel (STRB), which allows VLCS to read the stream. The parameters in this register are required when starting the VLCS.

- Setting for decoding

Bit	Name	Setting value	Description
63 to 32	(reserved)	H'08A8 7000	Always set to this value.
31 to 16	(reserved)	H'0000	Always set to this value.
15 to 13	endian	0 to 7	Endian. (Refer to table 27.22)
12 to 9	src_offset	10	Set to 10 for the VPU5HG.
8 to 0	(reserved)	25	Always set to this value.

37.3.16 Command Stream DMA Channel Register (VP5_VLC_DCHR_CMDS)

For decoding, this register specifies the operation of the DMA channel (CMDS) to read command streams for decoding.The parameters in this register are required when starting the VLCS.

- Setting for decoding

Bit	Name	Setting value	Description
63 to 32	(reserved)	H'88B0 7000	Always set to this value.
31 to 16	(reserved)	H'0000	Always set to this value.
15 to 13	endian	0 to 7	Endian. (Refer to table 27.22)
12 to 9	src_offset	10	Set to 10 for the VPU5HG.
8 to 0	(reserved)	26	Always set to this value.

37.3.17 VLCS Data Partition DMA Channel Register (VP5_VLC_DCHR_BPDP)

This register specifies the operation of the DMA channel (BPDP), which allows the VLCS to read the data partition information, bit plane information and MapColtolist information. The parameters in this register are required when starting the VLCS.

Set this register for MPEG-4 data partition decoding/VC-1 decoding/H.264MapColtoList setting.

- Setting for decoding (H.264)

Bit	Name	Setting value	Description
63 to 32	(reserved)	H'08B8 7000	Always set to this value.
31 to 16	(reserved)	H'0000	Always set to this value.
15 to 13	endian	0 to 7	Endian. (Refer to table 27.22)
12 to 9	src_offset	10	Set to 10 for the VPU5HG.
8 to 0	(reserved)	27	Always set to this value.

- Setting for decoding (MPEG-4)

Bit	Name	Setting value	Description
63 to 32	(reserved)	H'08A8 7000	Always set to this value.
31 to 16	(reserved)	H'0000	Always set to this value.
15 to 13	endian	0 to 7	Endian. (Refer to table 27.22)
12 to 9	src_offset	15	Set to 15 for the VPU5HG.
8 to 0	(reserved)	27	Always set to this value.

- Setting for decoding (VC-1)

Bit	Name	Setting value	Description
63 to 32	(reserved)	H'08A8 7000	Always set to this value.
31 to 16	(reserved)	H'0000	Always set to this value.
15 to 13	endian	0 to 7	Endian. (Refer to table 27.22)
12 to 9	src_offset	10	Set to 10 for the VPU5HG.
8 to 0	(reserved)	27	Always set to this value.

37.3.18 VLCS Intermediate Stream DMA Channel Register 0 (VP5_VLC_DCHR_VLIS0)

This register specifies the operation of the DMA channel (VLIS0) which allows the VLCS to input/output intermediate streams. The parameters in this register are required when starting the VLCS.

- Setting for decoding

Bit	Name	Setting value	Description
63 to 32	(reserved)	H'C000 0000	Always set to this value.
31 to 16	(reserved)	H'0000	Always set to this value.
15 to 13	endian	0 to 7	Endian. (Refer to table 27.22)
12 to 9	src_offset	9	Set to 9 for the VPU5HG.
8 to 0	(reserved)	28	Always set to this value.

- Setting for encoding

Bit	Name	Setting value	Description
63 to 32	(reserved)	H'88A0 7000	Always set to this value.
31 to 16	(reserved)	H'0000	Always set to this value.
15 to 13	endian	0 to 7	Endian. (Refer to table 27.22)
12 to 9	src_offset	9	Set to 9 for the VPU5HG.
8 to 0	(reserved)	28	Always set to this value.

37.3.19 VLCS Intermediate Control Stream DMA Channel Register 0 (VP5_VLC_DCHR_VLIC0)

This register specifies the operation of the DMA channel (VLIC0) which allows the VLCS to input/output intermediate control streams. The parameters in this register are required when starting the VLCS.

- Setting for decoding

Bit	Name	Setting value	Description
63 to 32	(reserved)	H'C000 0000	Always set to this value.
31 to 16	(reserved)	H'0000	Always set to this value.
15 to 13	endian	0 to 7	Endian. (Refer to table 27.22)
12 to 9	src_offset	9	Set to 9 for the VPU5HG.
8 to 0	(reserved)	29	Always set to this value.

- Setting for encoding

Bit	Name	Setting value	Description
63 to 32	(reserved)	H'88A8 7000	Always set to this value.
31 to 16	(reserved)	H'0000	Always set to this value.
15 to 13	endian	0 to 7	Endian. (Refer to table 27.22)
12 to 9	src_offset	9	Set to 9 for the VPU5HG.
8 to 0	(reserved)	29	Always set to this value.

37.3.20 VLCS Co-location Not Coded DMA Channel Register (VP5_VLC_DCHR_CLNC)

This register specifies the operation of the DMA channel (CLNC), which allows the VLCS to input/output the co-location not coded information. The parameters in this register are required when starting the VLCS.

- Setting for B-VOP (MPEG-4)

Bit	Name	Setting value	Description
63 to 32	(reserved)	H'8898 7000	Always set to this value.
31 to 16	(reserved)	H'0000	Always set to this value.
15 to 13	endian	0 to 7	Endian. (Refer to table 27.22)
12 to 9	src_offset	13	Set to 13 for the VPU5HG.
8 to 0	(reserved)	30	Always set to this value.

- Setting for I-VOP, P-VOP(MPEG4)

Bit	Name	Setting value	Description
63 to 32	(reserved)	H'C000 0000	Always set to this value.
31 to 16	(reserved)	H'0000	Always set to this value.
15 to 13	endian	0 to 7	Endian. (Refer to table 27.22)
12 to 9	src_offset	13	Set to 13 for the VPU5HG.
8 to 0	(reserved)	30	Always set to this value.

37.3.21 VLCS Data Partition Write DMA Channel Register (VP5_VLC_DCHR_DPW)

This register specifies the operation of the DMA channel (DPW), which allows the VLCS to write the data partition information. The parameters in this register are required when starting the VLCS.

- Setting for decoding (MPEG-4)

Bit	Name	Setting value	Description
63 to 32	(reserved)	H'C000 0000	Always set to this value.
31 to 16	(reserved)	H'0000	Always set to this value.
15 to 13	endian	0 to 7	Endian. (Refer to table 27.22)
12 to 9	src_offset	14	Set to 14 for the VPU5HG.
8 to 0	(reserved)	31	Always set to this value.

37.3.22 GDMAC Operation Control Register (VP5_GDMAC_ARDPRI)

This register controls the internal operation of the GDMAC. The parameters in this register are required when starting the CE and VLCS. Do not change the settings when the CE or VLCS is active. Set the same value for the CE and VLCS.

The bits which are omitted here are reserved. They are set to 0.

- Bits Set for Decoding

Bit	Name	Setting value	Description
37 to 32	(reserved)	16	Always set to this value.

- Bits Set for Encoding

Bit	Name	Setting value	Description
37 to 32	(reserved)	0	Always set to this value.

37.3.23 GDMAC SHwy Arbitration Control Register (VP5_GDMAC_SHWARBT)

This register contains the arbitration settings when the GDMAC accesses the external memory via the SHwy. The parameters in this register are required when starting the CE and VLCS.The bits which are omitted here are reserved. They are set to 0.

Table 27.22 VP5_GDMAC_SHWARBT Bit Fields

Bit	Name	Setting value	Description
39 to 36	ratio	8	Always set to this value. Select 0 for encoding which involves one CE.

37.3.24 CE Sequence Level Control Register (VP5_CE_SPAR)

This register contains the CE control parameters. They are required when starting the CE. They are specified using the CE initialization routine. The bits in the grayed areas and bits which are omitted here are reserved. All these bits are set to 0.

Table 27.23 VP5_CE_SPAR Bit Fields

		Setting		
Name	**Bit**	DEC	ENC	**Description**
62	interlace	0, 1	0, 1	Specifies whether to perform field prediction. 0: Frame prediction 1: Frame/field prediction Table 27.20 shows the combinations of settings for interlacing. To encode B pictures, specify the same structure as that for anchor pictures.
61	field_pic_if	0, 1	0, 1	Field picture input/output flag. Specifies the format of pictures in external RAM. 0: Frame picture 1: Field picture Select 1 when frame pictures are encoded as field pictures or when field structure streams are decoded to output frame pictures. Table 27.20 shows the combinations of settings for interlacing.
60	mb_aff	0, 1	0, 1	For encoding: Specifies the use of adaptive frame/field prediction or frame/field DCT for each MB in frame pictures. Select 0 for H.264 processing. For decoding: Select 0 for processing non-H.264 content. Specify the picture structure for H.264 processing. 0: FLD/FRM 1: AFRM

Name	Bit	Setting		Description
		DEC	ENC	
59	entropy_coding_mode_flag	0, 1	0, 1	Information source encoding specification 0: CAVLC 1: CABAC
58	force_deblock	0, 1	0, 1	Post filter enable 0: Normal Operation 1: Deblock filtering applied (MPEG-1,-2,-4,H.263) Select 0 for encoding.
57	q_scale_type	0, 1	0, 1	Q scale type (MPEG2)
56	q_type	0, 1	0, 1	Quantization type 0: Quantization matrix is not used 1: Quantization matrix is used
54	frame_mbs_only_flag_inv	0, 1	0, 1	H.264: 0: Progressive sequence 1: Interlace sequence MPEG-2: (set same value with field_pic_if) 0: Frame picture 1: Field picture MGEG4/H.263: set to 0. When using VC-1; 0:Progressive 1:Interlace Frame and Interlace Field
53	monochrome	0, 1	0, 1	0: 420, 1: 400 (monochrome)
52	mb_aff_sequence	0, 1	0, 1	mb_adaptive_frame_field 0: Normal sequence 1: MB-AFF sequence
47	avc_profile	0, 1	0, 1	Specifies a profile 0: Baseline, Main 1: High

Name	Bit	Setting		Description
		DEC	ENC	
46	vc1_profile	0,1	0,1	Specifiles a profile 0:Simple,Main 1:Advance
44 to 40	num_ref_frames	0 to 16	0 to 16	Specifies num_ref_frames (for H.264). Select a non-zero value for B pictures.
44	Range_mapy	0, 1	—	Specify MSB for RANGE_MAPY for VC-1 processing.
39, 38	ce	0, 1	0, 1	Number of CEs 0: 1 1: 2 2/3: Reserved Usually, select 1. Select 0 only for encoding which involves one CE.
36	dec_out_disable	0, 1	0, 1	Local-decode picture output suppression 0: Output allowed 1: Output not allowed Select 0 for decoding.
34 to 32	stream_type			Stream type 0: MPEG-4 1: H.263 2: H.264 6: MPEG-2 7: MPEG-1)
31 to 24	mb_width			Horizontal macroblock count in MB units). (Includes the number of MBs distributed across the screen boundary if the horizontal pixel count is not a multiple of 16. Refer to table 27.24.

Name	Bit	Setting		Description
		DEC	ENC	
19 to 16	hsize_odd	0 to 15	0 to 15	For encoding: Set the horizontal picture size remainder (in pixel units). For decoding: Set to 0 for H.264, MPEG-2, VC-1 SP/MP.Set the horizontal picture size remainder (in pixel units) for MPEG-4, H.263,VC-1 AP.
15 to 8	mb_height			Vertical macroblock count (in MB units; Includes the number of MBs distributed across the screen boundary if the vertical pixel count is not a multiple of 16.) At encoding time: The associable minimum picture size is to be changed according to serch_range setting value of VP5_CE_CTRL. Refer to table 27.24.
3 to 0	vsize_odd	0 to 15	0 to 15	For encoding: Set the vertical picture size remainder (in pixel units). For decoding: Set to 0 for H.264, MPEG-2, VC-1 SP/MP.Set the vertical picture size remainder (in pixel units) for MPEG-4, H.263,VC-1 AP.

Table 27.23 Combinations of Interlace Parameter Settings

Mode	Standard	Encoding Method	Input/Output picture format	interlace	field_pic_if
Decoding	H.264	Progressive*4/ Frame	Frame	0	0
			Field	0	1
		Field	Frame	1	0
			Field	1	1
	MPEG4	Progressive*1	Frame	0	0
			Field	0	1
		Frame (Interlace)	Frame	0 (VP5_CE_SPAR) 1 (VP5_VLC_SPAR)	0
			Field	0 (VP5_CE_SPAR) 1 (VP5_VLC_SPAR)	1
	Others	Progressive*1/ Frame	Frame	0	0
			Field	0	1
		Field	Frame	1	0
			Field	1	1
Encoding	H.264	Progressive*1	Frame	0	0
		Field	Frame	1	1*2
			Field	1	1
	MPEG4	Progressive*1	Frame	0	0
		Frame (Interlace)	Frame	0 (VP5_CE_SPAR) 1 (VP5_VLC_SPAR)	0
	Others	Progressive*1	Frame	0	0
		Field	Frame	1	1*2
			Field	1	1
		Frame	Frame	0	0

Notes: When combined with ICB, progressive encoding stores only frame pictures and field encoding stores only field pictures.

1. Progressive encoding above means frame encoding which does not involve adaptive frame/field prediction for each MB.
2. Set twice hsize in VP5_CE_DCHR_DECY0/1, VP5_CE_DCHR_DECC0/1, VP5_CE_DCHR_REF and VP5_CE_DCHR_TMP1. In VP5_BAAP0/1, specify the picture base address as the start address of the field. That is, specify the position of the bottom field which is displaced one line from the top field.

37.3.25 CE Picture-Level Control Register (VP5_CE_PPAR)

This register contains the CE control parameters. They are required when starting the CE. They are specified using the CE initialization routine. Bits which are omitted here are reserved. The bits are set to 0.

Setting this register is unnecessary for decoding.

- H.264 Bit fields

Bit	Name	Setting value	Description
63 to 61	pic_type		Type of picture encoding 0: I 1: P 2: B
60 to 56	refidx_last0		Number of valid L0 reference planes. For P pictures, set to 0 (single reference) or 1 (multi-reference). For B pictures, set to 0 (single reference).
52 to 48	refidx_last1	0 to 31	Number of valid L1 reference planes. At encoding time, set to 0 (single reference)
47	bottom_field	0 to 1	Bottom field flag 0: Top field 1: Bottom field
46	col_field_pic	0, 1	Anchor picture field flag 0: Frame 1: Field
32	const_intra_pred	0, 1	constrained_intra_pred_flag. Fixedly set to 0 for encoding.
28 to 24	qp_c_offset0	(-12) to (+12)	qp_chroma_index_offset value (Cb for HighProfile)
23 to 19	qp_c_offset1	(-12) to (+12)	qp_chroma_index_offset value (Cr for HighProfile)
17, 16	deblock_filter_idc	0 to 2	disable_deblocking_filter_idc
15 to 12	alpha_offset	(-6) to (+6)	slice_alpha_c0_offset_div2
11 to 8	beta_offset	(-6) to (+6)	slice_beta_offset_div2

Bit	Name	Setting value	Description
7 to 4	motion_mb_h	(-3) – (+3)	Horizontal motion quantity (in MB units) Specifies in MB units the quantity of horizontal motion of the entire screen. If this is done for encoding PAN pictures, then a search is performed mostly along the motion direction, thereby improving the picture quality. If the quantity of motion of the entire screen is unknown, select 0. If the screen size is less than CIF (352 × 288), select 0. The specifiable values and associated fcode settings vary depending on the motion detection search range. Refer to table 27.24.
3 to 0	motion_mb_v	(-1) – (+1)	Vertical motion quantity (in MB units) Specifies in MB units the quantity of vertical motion of the entire screen. If this is done for encoding PAN pictures, then a search is performed mostly along the motion direction, thereby improving the picture quality. If the quantity of motion of the entire screen is unknown, select 0. If the screen size is less than CIF (352 × 288), select 0. The specifiable values and associated fcode settings vary depending on the motion detection search range. Refer to table 27.24.

- MPEG-2 /MPEG-1Bit Fields

Bit	Name	Setting value	Description
63 to 61	pic_type	0 to 2	Picture type 0: I 1: P 2: B
60 to 56	refidx_last0	0, 1	Subtract 1 from the number of valid L0 reference planes (Valid for encoding only). For P pictures, set to 0 (single reference) or 1 (multi-reference).

Bit	Name	Setting value	Description
52 to 48	refidx_last1	0 to 31	Subtract 1 from the number of valid L1 reference planes (Valid for encoding only). Set to 0 (single reference).
47	bottom_field	0, 1	Bottom field flag 0: Top field 1: Bottom field
33	alt_vscan	0, 1	alternate_vertical_scan
25	top_field_first	0, 1	0: Bottom field comes first 1: Top field comes first
24	concealment_motion_vector	0, 1	concealment_motion_vector
23	frame_pred_frame_dct	0, 1	frame_pred_frame_dct
22	intra_vlc_format	0, 1	MPEG-2 intra VLC table switching
21, 20	intra_dc_precision	0 to 2	MPEG-2 internal DC accuracy
7 to 4	motion_mb_h	(-3) – (+3)	Horizontal motion quantity (in MB units) Specifies in MB units the quantity of horizontal motion of the entire screen. If this is done for encoding PAN pictures, then a search is performed mostly along the motion direction, thereby improving the picture quality. If the quantity of motion of the entire screen is unknown, select 0. If the screen size is less than CIF (352 288), select 0. The specifiable values and associated fcode settings vary depending on the motion detection search range. Refer to table 27.24.

Bit	Name	Setting value	Description
3 to 0	motion_mb_v	(-1) – (+1)	Vertical motion quantity (in MB units) Specifies in MB units the quantity of vertical motion of the entire screen. If this is done for encoding PAN pictures, then a search is performed mostly along the motion direction, thereby improving the picture quality. If the quantity of motion of the entire screen is unknown, select 0. If the screen size is less than CIF (352 × 288), select 0. The specifiable values and associated fcode settings vary depending on the motion detection search range. Refer to table 27.24.

- MPEG-4/H.263 Bit Fields

Bit	Name	Setting value	Description
63 to 61	pic_fype	0 to 2	Picture type 0: I 1: P 2: B
60 to 56	refidx_last0	0	Subtract 1 from the number of valid L0 reference planes (Valid for encoding only). Set to 0 (single reference).
52 to 48	refidx_last1	0	Subtract 1 from the number of valid L1 reference planes (Valid for encoding only). Set to 0 (single reference).
45	runding_type	0, 1	vop_rounding_type
42	resync_marker	0, 1	Resync_marker_disable inversion value
41	data_partitioned	0, 1	DP ON/OFF
40	reversible_vlc	0, 1	RVLC ON/OFF
38 to 36	intra_dc_vlc_thr	0 to 7	Intra_dc_vlc_thr (specifies QP threshold value to switch VLCtable)

Bit	Name	Setting value	Description
33	alt_vscan	0, 1	Alternate_vertical_scan 0: zigzag scan 1: alternate scan
25	top_field_first	0, 1	0: bottom field is the initial field 1: top field is the initial field
7 to 4	motion_mb_h	(-3) – (+3)	Horizontal motion quantity (in MB units) Specifies in MB units the quantity of horizontal motion of the entire screen. If this is done for encoding PAN pictures, then a search is performed mostly along the motion direction, thereby improving the picture quality. If the quantity of motion of the entire screen is unknown, select 0. If the screen size is less than CIF (352 x 288), select 0. The specifiable values and associated fcode settings vary depending on the motion detection search range. Refer to table 27.24.
3 to 0	motion_mb_v	(-1) – (+1)	Vertical motion quantity (in MB units) Specifies in MB units the quantity of vertical motion of the entire screen. If this is done for encoding PAN pictures, then a search is performed mostly along the motion direction, thereby improving the picture quality. If the quantity of motion of the entire screen is unknown, select 0. If the screen size is less than CIF (352 x 288), select 0. The specifiable values and associated fcode settings vary depending on the motion detection search range. Refer to table 27.24.

37.3.26 Weighted Prediction Control Register (VP5_CE_ENC_WPRED)

This register is reserved. Set each item to 1.

Bit	Name	Setting value	Description
63 to 56	Reserved	1	Always set to 1.
55 to 48	Reserved	1	Always set to 1.
47 to 40	Reserved	1	Always set to 1.
39 to 32	Reserved	1	Always set to 1.
31 to 24	Reserved	1	Always set to 1.
23 to 16	Reserved	1	Always set to 1.

37.3.27 Encode Control Register (VP5_CE_ENC_CTRL)

This register contains the encode control parameters. These parameters are required when starting the CE for encoding. Bits which are omitted here are reserved. The bits are set to 0.

Bit	Name	Setting value	Description
60	ac_pred_off	0, 1	0: Enables AC prediction. 1: Disables AC prediction. Be sure to select 1 for MPEG-4 encoding which involves one CE.
56	transform_8 × 8	0, 1	8 × 8 conversion enable 0: Only 4 × 4 integer conversion used (for encoding with Baseline, Main profiles). 1: 4 × 4 or 8 × 8 integer conversion used (for encoding with High profiles)
55 to 48	intra_th_act	0 to 255	Intra/inter decision threshold 2 If the activity evaluation value for a macroblock exceeds this setting, it is determined to be an inter macroblock. intra_th_act takes preference over intra_th_high. (Recommended value: 255)
47 to 40	intra_th_high	0 to 65535	Intra/inter decision threshold 1 If the inter coding cost evaluation value (based on the Sum of Absolute Differences (SAD) for a macroblock exceeds this setting, it is determined to be an intra macroblock. (Recommended value: 32)
39 to 32	intra_th_offset	0 to 65535	Intra/inter decision offset Specifies the offset value for intra macroblock encoding cost. The greater this setting, the smaller the intra macroblock rate. (Recommended value: 64) Set to 0 when data is coded into a stream which complies with standards other than H.264.

Bit	Name	Setting value	Description
31 to 24	motion_pel_h	(-128)-(+127)	Horizontal motion quantity (in pixel units) Specifies in pixel units the quantity of horizontal motion of the entire screen. This improves the picture quality for encoding PAN pictures. If the quantity of motion of the entire screen is unknown, select 0. For P picture multi-referencing, it is recommended to specify the quantity of motion relative to the Ref0 reference picture. Select 0 for B pictures. The selected value should be consistent with VP5_CE_SPAR.motion_mb_h settings.
23 to 16	motion_pel_v	(-48)-(+47)	Vertical motion quantity (in pixel units) Specifies in pixel units the quantity of vertical motion of the entire screen. This improves the picture quality for encoding PAN pictures. If the quantity of motion of the entire screen is unknown, select 0. For P picture multi-referencing, it is recommended to specify the quantity of motion relative to the Ref0 reference picture. Select 0 for B pictures. The selected value should be consistent with VP5_CE_SPAR.motion_mb_v settings.
15	(reserved)	1	Always set to 1.

Bit	Name	Setting value	Description
12	dq_disable	0, 1	DQ disable 0: Controls the macroblock-level quantization parameters based on TM5 step 2. 1: Does not control the macroblock-level quantization parameters based on TM5 step 2. (Recommended.) Select 1 if a constant amount of code is required throughout the sequence when the line speed is fixed for wireless or other communication technologies. In this case, virtual buffer feedback control based on TM5 step 2 is provided. Note that the picture quality is not enhanced by activity picture quality control.
10	umv_disable	0, 1	UMV disable 0: Screen outside reference made 1: Screen outside reference not made Select 1 if data is coded into a stream which complies with the MPEG2 and H.263 Baseline standards; otherwise, select 0.
9	force_forward	0, 1	Forcible forward reference 0: Normal 1: Forcible forward reference
8	force_backward	0, 1	Forcible backward reference 0: Normal 1: Forcible backward reference

Bit	Name	Setting value	Description
6 to 4	search_range		Motion detection search range 0: ±16(HV) 1: ±32(HV) 2: ±32(H)±16(V) 3: ±64(H)±16(V) 4: ±64(H)±32(V) The specifiable motion detection search range varies depending on the picture type and the number of reference areas. Refer to tables 27.24 and 27.25. The minimum picture size supported varies depending on the settings. Refer to table 27.26.
1	ref_bottom_l0	0, 1	L0 reference picture bottom field flag 0: Top field 1: Bottom field Select the same parity field for B picture.
0	ref_bottom_l1	0, 1	L1 reference picture bottom field flag 0: Top field 1: Bottom field Select the same parity field for B picture.

Table 37.1 Relationship between the Motion Detection Search Ranges, Picture Types and Number of Reference Areas

	VP5_CE_PPAR	VP5_CE_ENC_CTRL
pic_type Setting	**refidx_last0 Setting**	**search_range Setting**
0 (I pictrure)	Don't care	Don't care
1 (P picture)	0 (single-reference)	0, 1, 2, 3, 4
	1 (multi-reference)	0, 2, 3
2 (B picture)	0 (single-reference)	0, 2, 3

Table 37.2 Settings by Motion Detection Search Range

Search Range	**search_range Settings (Motion Detection Search Range)**	
	P Picture (Single-reference)	**B or P Picture (Multi-reference)**
Narrow	0 (±16(HV))	0 (±16(HV))
Medium	1 (±32(HV))	2 (±32(H) ±16(V))
Wide	4 (±64(H) ±32(V))	3 (±64(H) ±16(V))

Table 27.26 Associated Minimum Picture Size Range in Every Motion Detection Search Range

Search_range Setting Value	**Motion detection Search Range**	**Associated Min. Picture size**
0	± ¥16 (HV)	80 × 80
1	±32 (HV)	80 × 80
2	±32 (H) ±16 (V)	80 × 80
4	±64 (H) ±32 (V)	144 × 80
Others	Reserved	Reserved

37.3.28 Activity Control Register (VP5_CE_ACQ_CTRL)

This register contains the picture quality control parameters which depend on the picture activities. The VPU5HG controls the quantization coefficient between q_min and q_max for activities of macroblock data to be coded. Bits which are omitted here are reserved. The bits are set to 0.

Bit	Name	Setting value	Description
61 to 56	q_max	0 to 51	Specifies the maximum quantization coefficient within a picture. Condition q_max >= q_min should always be satisfied.
53 to 48	q_min	0 to 51	Specifies the minimum quantization coefficient within a picture. Condition q_max >= q_min should always be satisfied.
42 to 32	act_avg	0 to 2040	Average activity value (recommended initial setting: 60) It is recommended to set the average activity value (calculated from VP5_CE_ASUM) for the previous frame.
26 to 16	act_max	0 to 2040	Maximum activity value (recommended initial setting: 40) It is recommended to set the maximum activity value (AMAX bit in the VP5_CE_ACT register) for the previous frame.
10 to 0	act_min	0 to 2040	Minimum activity value (recommended initial setting: 20) It is recommended to set the minimum activity value (AMIN bit in the VP5_CE_ACT register) for the previous frame.

37.3.29 Inter Mode Judgment Control Register (VP5_CE_ME_COST)

This register contains the parameters for determining the inter macroblock block sizes. It also contains clip values for quantization parameter changes between macroblocks. The VPU5HG selects the optimal block size based on the inter SAD and vector cost (evaluation value which is an estimated value of the amount of motion vector code). The inter SAD and vector cost weight are changed according to the quantization parameter. Bits which are omitted here are reserved. The bits are set to 0.

Bit	Name	Setting value	Description
53 to 48	cost_thq1	0 to 51	Threshold 1 for the scale factor for the amount of inter mode judgment motion vector code Upper limit on Q which sets Vector cost:Inter SAD = 4:1 (recommended value: 23) Set to 0 unless data is coded into a stream which complies with the H.264 standard.
45 to 40	cost_thq2	0 to 51	Threshold 2 for the scale factor for the amount of inter mode judgment motion vector code Upper limit on Q which sets Vector cost:Inter SAD = 8:1 (recommended value: 29) Set to 0 unless data is coded into a stream which complies with the H.264 standard.
37 to 32	cost_thq3	0 to 51	Threshold 3 for the scale factor for the amount of inter mode judgment motion vector code Upper limit on Q which sets Vector cost:Inter SAD = 16:1 (recommended value: 35) Set to 0 unless data is coded into a stream which complies with the H.264 standard.

Bit	Name	Setting value	Description
29 to 24	cost_Qthq4	0 to 51	Threshold 4 for the scale factor for the amount of inter mode judgment motion vector code Upper limit on Q which sets Vector cost:Inter SAD = 32:1 (recommended value: 41) Set to 0 unless data is coded into a stream which complies with the H.264 standard.
21 to 16	cost_thq5	0 to 51	Threshold 5 for the scale factor for the amount of inter mode judgment motion vector code Upper limit on Q which sets Vector cost:Inter SAD = 64:1 (recommended value: 46)If the quantization parameter exceeds the maximum of values cost_thq1 through cost_thq5, Vector cost:Inter SAD = 128:1 is used for processing. (Refer to figure 27.3.) Set to 0 unless data is coded into a stream which complies with the H.264 standard.
3 to 0	dq_clip	0 to 51	Clip value for the change in the quantization parameter 0: No limit 1-15: Limits the change in the quantization parameter between macroblocks. Set to 2 when data is coded into a stream which complies with the MPEG-4 or H.263 standard; otherwise, set to 0.

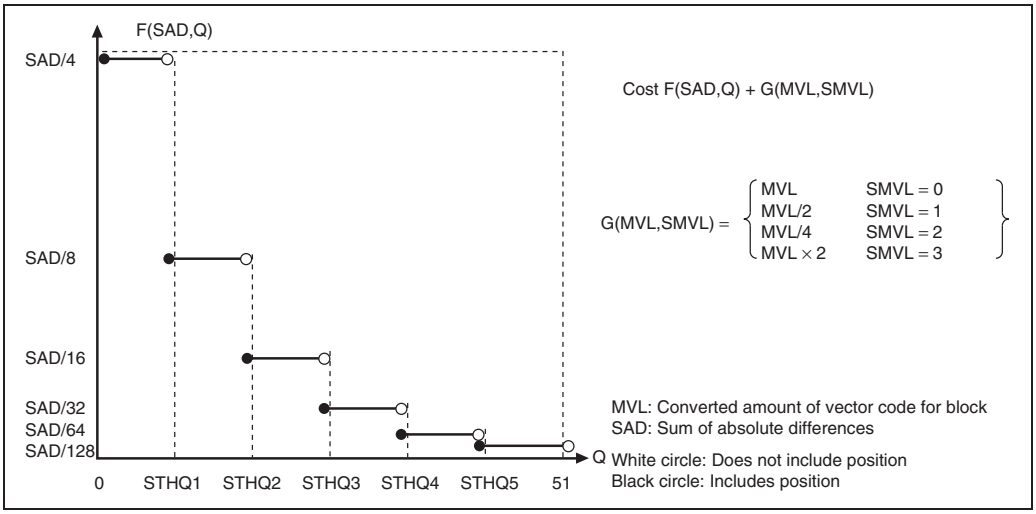


Figure 27.4 MB Partition Cost Calculation

37.3.30 VLCF Control Register (VP5_CE_VLCF)

This register sets the operational mode of VLCF.The parameters in this register are required when starting the CE. Bits which are omitted here are reserved. The bits are set to 0.

- Bit Fields for Encoding (H.264)

Bit	Name	Setting value	Description
29 to 24	slice_qp	0 to 51	pic_init_qp + slice_qp_delta
17 to 16	cabac_init_idc	0 to 2	cabac_init_idc
13 to 8	InitialQpY	0 to 51	InitialQpY(PPS : pic_init_qp)
2	Qnc_disable	0, 1	Always set to 1
1	mv_info	0, 1	MV information output specification 0: Information output 1: Information not output)

- Bit Fields for Encoding (MPEG-2/MPEG-4/H.263)

Bit	Name	Setting value	Description
29 to 24	InitialQpY	0 to 31	InitialQpY
23 to 20	fcode00	Described in the right column.	Specifies fcode[0][0] values MPEG-4 enc: 1 to 4(forward fcode is set) H.263 enc: 1 MPEG-1/-2 enc: 1 to 5 Others: Setting unnecessary
19 to 16	fcode01	Described in the right column.	Specifies fcode[0][1] values (For MPEG-4, forward fcode is set)
15 to 12	fcode10	Described in the right column.	Specifies fcode[1][0] values (For MPEG-4, forward fcode is set)
11 to 8	fcode11	Described in the right column.	Specifies fcode[1][1] values (For MPEG-4, forward fcode is set)

Bit	Name	Setting value	Description
2	qnc_disable	0, 1	Always set to 1.
1	mv_info	0, 1	Specifies the MV information output 0: The information is to be output. 1: The information is not to be output.

- Bit Fields for Decoding

Bit	Name	Setting value	Description
63 to 32	currPicOrderCnt	0 to 2,147,483,647	current PicOrderCnt (POC)
1	mv_info	0, 1	Specifies the MV information output 0: The information is to be output. 1: The information is not to be output.
0	ec_mode	0, 1	Error Conceal Mode Specification 0: Intra conceal (concealing in frame) In a frame, performs the conceal processing to the macroblock after an error generation. At decoding time in H.264, performs the pixel padding with the interpolated value calculated from the edge pixel value. When an error is generated at the upper-left block, performs the pixel padding with the intermediate value. The setting is only for H.264. For setting, use the inter conceal mode by specifying the reference picture address. 1:1 Inter Conceal (concealing between frames) Performs the switch processing the macroblock after an error generation to a skip macroblock, MV = (0, 0). This setting is enable when a reference image is specified even one picture. In B picture, use the direct mode.

Table 27.27 Motion Quantity and fcode Settings by Motion Detection Search Range

Search range	Element	H : motion_mb_h V : motion_mb_v	fcode Setting			
			MPEG-2		MPEG-4(H.263)	
			P Picture	B Picture	P Picture	B Picture
0 (±16 (HV))	H	0	2	←	1(1)	←
	V	0				
1 (±32 (HV))	H	0	3		2	
	V	0				
2 (±32 (H) ±16 (V))	H	-1	4	←	2 if motion_mb_h is 0, 3 otherwise.	←
		0	3	←		
		1	4	←		
	V	0	2	←		
3 (±64 (H) ±16 (V))	H	-3 to -1	5	←	3 if motion_mb_h is 0, 4 otherwise.	←
		0	4	←		
		1 to 3	5	←		
	V	0	2	←		
4 (±64 (H) ±32 (V))	H	-3 to -1	5		3 if both motion_mb_h and motion_mb_v are 0, 4 otherwise.	
		0	4			
		1 to 3	5			
	V	-1	4			
		0	3			
		1	4			
Other than above	Other than above	Other than above	Reserved		Reserved	

Set fcode[*][0] to the horizontal element (H) value. Set fcode[0][0] and fcode[1][0] to the same value.

Set fcode[*][1] to the vertical element (V) value. Set fcode[0][1] and fcode[1][1] to the same value.

37.3.31 Slice Size Register (VP5_CE_SLC_SIZE)

The VP5_CE_SLC_SIZE register controls the size of a slice or video packet. Bits which are omitted here are reserved. The bits are set to 0.

Bit	Name	Setting value	Description
59 to 48	psmb	0 to 68	Slice MB count (initial value: 0) Inserts the next slice or packet header when the number of MB lines exceeds the set value. If the value is 0, control with the number of MB lines is not provided. Set PSMB or PS to 0 for encoding with slices or video packets. In the case of MPEG-2, select 1.
46 to 32	ps	0 to 32, 767	Slice bit count (initial value: 0) Select 0 for encoding which involves the two CEs. For MPEG-4/H.263 encoding which involves one CE, calculate the intermediate-stream size in 16-bit units by using the target video packet size and specify the calculation result. When the intermeidate-stream size exceeds the set value of these bits, termination processing with the video packet size is performed (the actual output intermidate-stream size might exceed the set value in this register). If the value is 0, control with the number of MB lines is not provided. Any value from 1 through 32,767 (for 16 to 524,272 bits) can be specified. Set PSMB or PS to 0 for encoding with video packets.

Note: Intermediate-stream Size Calculation:
It is recommended to calculate the settings by using the formula below.
Target viedo packet size × 2/3 × R + 96
R = 1.00(I-VOP), 1.67(P-VOP), 2,00(B-VOP)

37.3.32 Target Bit Rate Control Register (VP5_CE_TBIT)

This register contains parameters for bit rate control. It does not need to be set when controlling the picture quality by activities. Bits which are omitted here are reserved. The bits are set to 0.

Bit	Name	Setting value	Description
44 to 32	mb_num	0 to 8,160	Macroblock count
15 to 0	mb_target	0 to 65,535	Target amount of coding per macroblock. This parameter specifies the target number of bits per macroblock for encoding. The setting should be the result of dividing the target bit count per picture by the macroblock count. The VPU5HG controls the quantization coefficient so the amount of coding per macroblock can become the bit count setting.

37.3.33 Virtual Buffer Control Register (VP5_CE_RCDJ)

This register contains parameters for bit rate control. It does not need to be set when controlling the picture quality by activities. Bits which are omitted here are reserved. The bits are set to 0.

Bit	Name	Setting value	Description
52 to 32	reac_param	1 to 2,2097,151	Reaction parameter. This parameter specifies 2 × Bit rate ÷ Frame rate.
31 to 0	rcdj	–2,147,483,658 to 2,147,483,657	Virtual buffer. This parameter specifies the singed value which indicates the amount of virtual buffer. The value should be a 2's complement number.

37.3.34 Intra Refresh Control Register (VP5_CE_MBRF)

This register controls the intra refresh of macroblock. Only a macroblock which is specified an intra macroblock start and end location is encoded to an intra macroblock. This register is valid only at encoding. Bits which are omitted here are reserved.

Bit	Name	Setting value	Description
63 to 56	irst_h	0 to 119	Specifies the intra refresh start macroblock horizontal location.
55 to 48	irst_v	0 to 67	Specifies the intra refresh start macroblock vertical location.
47 to 40	ired_h	0 to 119	Specifies the intra refresh end macroblock horizontal location.
39 to 32	ired_v	0 to 67	Specifies the intra refresh end macroblock vertical location.
31	ir_en	0, 1	Intra refresh enable

37.3.35 Inverse Quantization Matrix (VP5_CE_IQMAT)

This register specifies the quantization matrix for inverse quantization. The parameters in this register are required when starting the CE. For VPU5H processing, set the EMASK bit to H'10 by using the initial routine format.

Setting a 4 × 4 matrix is not necessary for processing non-H.264 content.

No.	Offset	Description	Remarks
0	000	Intra 4 × 4 luminance Y	Specifies the values in 8-bit units in ascending order for the matrix for big endian mode.
1	010	Intra 4 × 4 chrominance Cb	
2	020	Intra 4 × 4 chrominance Cr	
3	030	Inter 4 × 4 luminance Y	
4	040	Inter 4 × 4 chrominance Cb	
5	050	Inter 4 × 4 chrominance Cr	
6	060	Intra 8 × 8 luminance Y	
7	0A0	Inter 8 × 8 luminance Y	

37.3.36 Quantization Matrix (VP5_CE_QMAT)

This register specifies the reciprocal of the quantization matrix for inverse quantization. The parameters in this register are required when starting the CE. For VPU5H processing, set the EMASK bit to H'10 by using the initial routine format.

The range of specifiable quantization matrix values is from 6 to 255 for H.264 content and from 1 to 255 for non-H.264 content.

Setting a 4 x 4 matrix is unnecessary for processing non-H.264 content.

Calculate the reciprocal of a quantization matrix as follows.

[H.264]

IQmat (8-bit width, 8-bit accuracy) = Quantization matrix value

Qmat (16-bit width, 13-bit accuracy) = 8192 (= 2 U 13) / IQmat

/: Round down to the nearest integer

[MPEG-2 or MPEG-4]

IQmat (8-bit width, 8-bit accuracy) = Quantization matrix value

Qmat (16-bit width, 14-bit accuracy) = 8192 (= 2 U 13) // IQmat

//: Round off to the nearest integer

In VPUHG2, this register is used to set coefficient cut flags if the quantization type (VP5_CE_SPAR.q_type) is 0 for MPEG-4/H.263 encoding which involves one CE. Specify 0x0000 (invalid) and 0xFFFF (valid) in ascending order for the matrix. The coefficient in the position where 0x0000 is specified is forcibly encoded as 0. A separate coefficient cut flag should be set for each quantization type (intra or inter). For H.263 processing, be sure to set the DC position to 0xFFFF.

No.	Offset	Description	Remarks
0	000	Intra 4 × 4 luminance Y	Specifies the values in 16-bit units in ascending order for the matrix for big endian mode.
1	020	Intra 4 × 4 chrominance Cb	
2	040	Intra 4 × 4 chrominance Cr	
3	060	Inter 4 × 4 luminance Y	
4	080	Inter 4 × 4 chrominance Cb	
5	0A0	Inter 4 × 4 chrominance Cr	
6	0C0	Intra 8 × 8 luminance Y	
7	140	Inter 8 × 8 luminance Y	

37.3.37 CE Intermediate Stream 0 Buffer Size Register (VP5_CE_IS_BS0)

Bit	Name	Setting Value	Description
31 to 25	reserved	0	Reserved
24	CNT0	0, 1	Set to 1 when start-up the continue.
23 to 9	CIS0		CE intermediate stream 0 buffer size specification. This parameter specifies the intermediate stream 0 buffer size in 256-byte units (with the low-order eight bits being 0). For encoding, the CE stops writing after it has written intermediate stream 0 of the specified size. For decoding, the CE stops reading after it has read intermediate stream 0 of the specified size. In either case, it stops writing or reading and generates an interrupt. The interrupt is a CE error termination interrupt if the CIE0 bit in VP5_IRQ_ENB is 0 or a CE intermediate stream 0 buffer end interrupt if that bit is 1. The bits should be set before the start of the VPU5HG CE and after the generation of a CE intermediate stream 0 buffer end interrupt.
8 to 0	reserved	0	Reserved

37.3.38 FME0QNC0 Control Register (VP5_CE_FME0_QNC0)

This register controls the quantization parameter. This parameter is required for starting one CE for encoding. Select 0.

Bit	Name	Setting Value	Description
63 to 0	qnc	0	Always set to 1.

37.3.39 FME0QNC1 Control Register (VP5_CE_FME0_QNC1)

This register controls the quantization parameter. This parameter is required for starting one CE for encoding. Select 0.

Bit	Name	Setting Value	Description
63 to 0	qnc	0	Always set to 1.

37.3.40 TRF0QNC0 Control Register (VP5_CE_TRF0_QNC0)

This register controls the quantization parameter. This parameter is required for starting one CE for encoding. Select 0.

Bit	Name	Setting Value	Description
63 to 0	qnc	0	Always set to 1.

37.3.41 TRF0QNC1 Control Register (VP5_CE_TRF0_QNC1)

This register controls the quantization parameter. This parameter is required for starting one CE for encoding. Select 0.

Bit	Name	Setting Value	Description
63 to 0	qnc	0	Always set to 1.

37.3.42 VLCS Sequence Level Control Register (VP5_VLC_SPAR)

This register contains a parameter necessary for syntax interpretation by the VLCS STX. The parameter is required when starting the VLCS. The parameter should be specified using the VLCS initialization routine. Table 27.27 shows the bit fields. Bits which are omitted here are reserved. The bits are set to 0.

Table 27.27 VP5_VLC_SPAR Bit Fields

Name	Bit	Setting		Description
		DEC	ENC	
63	mode	01	0	Operation mode 0: Encoding 1: Decoding
62	interlace	0, 1	0, 1	Frame /field encoding method 0: Frame structure 1: Field structure For MPEG-4 processing, select one of the following: 0: Progressive encoding 1: Interlaced encoding Table 27.23 shows the combinations of interlace setting.

Name	Bit	Setting		Description
		DEC	ENC	
61	field_pic_if	0, 1	0, 1	Field picture input/output flag. Specifies the format for pictures in the external RAM. 0: Frame picture 1: Field picture Select 1 when the frame pictures are encoded as field pictures or when the field structure streams are decoded to output frame pictures. Table 27.23 shows the combinations of interlace settings.
60	mb_aff	0, 1	0, 1	For encoding: Specifies the use of adaptive frame/field prediction or frame/field DCT for each MB in frame pictures. Select 0 for H.264 processing. For decoding: Select 0 for processing non-H.264 content. Specify the picture structure for processing H.264 content. 0: FLD/FRM 1: AFRM
59	entropy_coding_mode_flag	0, 1	0, 1	Information source coding specification 0: CAVLC 1: CABAC
57	q_scale_type	0, 1	0, 1	Q scale type (MPEG2)
56	q_type	0, 1	0, 1	Quantization type When using H.264; 0: Quantization matrix not used 1: Quantization matrix used
54	frame_mbs_only_flag_inv	0, 1	0, 1	When using H.264; 0: Progressive sequence 1: Interlace sequence When using MPEG-2; (set same value with field_pic_if) 0: Frame picture

Name	Bit	Setting		Description
		DEC	ENC	
				1: Field picture
				When using MPEG-4,H.263; Set 0
				When using VC-1;
				0: Progressive
				1: Interlace Frame and Interlace Field
53	monochrome	0, 1	0, 1	0: 420, 1: 400 (monochrome
				e)
47	avc_profile	0, 1	0, 1	Specifies a profile
				0: Baseline, Main
				1: High
44 to 40	num_ref_frames	0 to 16	0 to 16	Specifies num_ref_frames (for H.264).
				Can only be set to 1 for interaction with VBLx.
39, 38	Ce	1	1	Always set to 1.
34 to 32	stream_type			Stream type
				0: MPEG4
				1: H.263
				2: H.264
				4: VC-1
				6: MPEG-2
				7: MPEG-1

Name	Bit	Setting		Description
		DEC	ENC	
31 to 24	mb_width			Horizontal macroblock count (in MB units). Includes MBs distributed across the screen boundary if the horizontal pixel count is not a multiple of 16.
19 to 16	hsize_odd	0 to 15	0 to 15	For encoding: Set the horizontal picture size remainder (in pixel units). For decoding: Set to 0 for H.264, MPEG-2, VC-1 SP/MP. Set the horizontal picture size remainder (in pixel units) for MPEG-4, VC-1 AP.
15 to 8	mb_height			Vertical macroblock count (in MB units; Includes the number of MBs distributed across the screen boundary if the vertical pixel count is not a multiple of 16.)
3 to 0	vsize_odd	0 to 15	0 to 15	For encoding: Set the vertical picture size remainder (in pixel units) For decoding:Set to 0 for H.264, MPEG-2, VC-1 SP/MP. Set the vertical picture size remainder (in pixel units) for MPEG-4, VC-1 AP.

37.3.43 VLCS Slice Header Register (VP5_VLC_SH)

The VPU5_VLC_SH register contains parameters for creating a slice header for H.264 encoding. The parameters in this register are required when starting the VLCS. They are set using the VLCS initialization routine. Bits which are omitted here are reserved. The bits are set to 0. Since the MPEG-2 header is byte aligned, setting in bit units is not necessary.

(1) VP5_VLC_SH Word 0

This parameter specifies the offset from the alignment position to the stream storage start position.

Bit	Name	Setting value	Description
4 to 0	offset_byte	0 to 31	Byte count for the stream storage start position offset. This parameter specifies the number of bytes from the alignment position to the stream storage start position. Starting first with VP5_VLC_SH word 1 to VP5_VLC_SH word 4 in sequence, store the words in the area from the alignment position to the stream storage start position.

(2) VP5_VLC_SH Word 1

Bit	Name	Setting value	Description
63 to 0	pad_bytes	0 to 31	Value to be stored in the area from the alignment position to the stream storage start position. (fill from MSB)

(3) VP5_VLC_SH Word 2

Bit	Name	Setting value	Description
63 to 0	pad_bytes		Value to be stored in the area from the alignment position to the stream storage start position. (fill from MSB)

(4) VP5_VLC_SH Word 3

Bit	Name	Setting value	Description
63 to 0	pad_bytes		Value to be stored in the area from the alignment position to the stream storage start position. (fill from MSB)

(5) VP5_VLC_SH Word 4

Bit	Name	Setting value	Description
63 to 0	pad_bytes		Value to be stored in the area from the alignment position to the stream storage start position. (fill from MSB)

(6) VP5_VLC_SH Word 5

- Bit Field (H.264)

Bit	Name	Setting value	Description
52 to 48	slice_header_size	0 to 31	High-order five bits for the slice header bit count (high-order five bits [8:4] for the slice_header bit count (byte count for the valid portions in VP5_VLC_SH words 6 through 13).
35 to 32	slice_header_size	0 to 15	Low-order four bits for the slice header size in bits (low-order four bits [3:0] for the slice_header bit count (valid portions in VP5_VLC_SH words 6 through 13)).
23 to 16	nal_unit_header		nal unit header (stream for the forbidden_zero_bit, nal_ref_idc and nal_unit_type portions)
0	start_code_insertion	0, 1	Start code (H'0000 0001) insertion in the position immediately before NAL. 0: Not inserted 1: Inserted)

- Bit Field (MPEG-4/H.263)

Bit	Name	Setting value	Description
52 to 48	slice_header_size	0 to 31	High-order five bits for the VOP header size in bits (high-order five bits [8:4] for the header bit count (byte count for the valid portions in VP5_VLC_SH words 6 through 13)).
35 to 32	slice_header_size	0 to 15	Low-order four bits for the VOP header size in bits (low-order four bits [3:0] for the header bit count (valid portions in VP5_VLC_SH words 6 through 13)).

(7) VP5_VLC_SH: Words 6 through 13

Bit	Name	Setting value	Description
63 to 0	slice_header		Slice header (which should be stored in big endian order). The emulation prevention byte can be inserted automatically. If the automatic insertion function is turned on, there is no need to insert the emulation prevention byte when setting this register. For H.264 processing, specify the area for slice_header() starting at slice_type and ending at a position immediately before cabac_init_idc (this area does not include cabac_init_idc). For MPEG-4 processing, specify the area for Video Object Plane up to a position immediately before motion_shape_texture(). For H.263 processing, specify the area for Video Plane with Short Header up to a position immediately before gob_layer().

(8) VP5_VLC_SH: Word 14

Bit	Name	Setting value	Description
63 to 0	PicSizeInMbs	1 to 8,160	Number of MBs in each picture

(9) VP5_VLC_SH: Word 16

Bit	Name	Setting value	Description
19 to 16	mb_num_bitlen	1 to 14	macroblock number bit length (setting only at MPEG-4 VP encoding)
15 to 0	dp_size_limit	0 to 65,535	Data Partition At encoding time, if VP exceeds the number of these bits, VLCS issues a warning to CTRL (Inevitable due to that 0 bit is synonymous with infinity, a warning is not issued).

37.3.44 VLCS Mode Register (VP5_VLC_MODE)

This register controls the VLCS operation. The parameters in this register are required when starting the VLCS. They are specified using the VLCS initialization routine. Bits which are omitted here are reserved. The bits are set to 0.

Bit	Name	Setting value	Description
36	Reserved	1	Always set to 1.
33, 32	Reserved	2	Always set to 2.
16	ParallelMode	0, 1	Parallel CE operation mode (for the VPU5H only) 0: 1-CE operation 1: 2-CE operation
12	ColInfoDir	0, 1	MPEG-4 collocation not-coded information stream transfer direction. 0: Read (B picture) 1: Write (I/P picture) Set to 0 for encoding or when the stream complies with other standards.
11	DPWEn	0, 1	MPEG-4 collocation not-coded information stream enable. 0: Disable 1: Enable Set to 0 for encoding or when the stream complies with other standards.
10	BPDPREn	0, 1	MPEG-4 data partition output stream enable. 0: Disable 1: Enable Set to 0 for encoding or when the stream complies with other standards.

Bit	Name	Setting value	Description
9	EPervDelEn	0, 1	H.264 MapColToList setting in MB units or units of MB lines/VC-1 bit plane/MPEG-4 data partition input stream enable. 0: Disable 1: Enable Set to 0 for encoding or when the stream complies with other standards.When using the DP, the DPWEn bit must be set to 1.When using the H.264 MapColToList, set the collist_proc_mode value of command stream word 1.
6	EPrevDelEn	0, 1	H.264 /VC-1 APemulation prevention byte deletion function. (0: Disable, 1: Enable) Select 0 for encoding or 1 for decoding.
5	EPrevInsEn	0, 1	H.264 emulation prevention byte insertion function. 0: Disable 1: Enable Select 0 for encoding or 1 for decoding.
4	CmdEn	0, 1	Command stream enable. Always select 1 for decoding. Select 0 for encoding.
3 to 0	Reserved	14	Set to 14.

37.3.45 Stream A Buffer Size Register (VP5_VLC_STRA_BS)

Bit	Name	Setting value	Description
32 to 24	reserved	0	Reserved
23 to 0	BVSA		Stream A buffer size specification. This parameter specifies the stream A buffer size in units of 256 bytes (with the low-order eight bits being 0). For encoding, the system stops writing after it has written a stream of the specified size. For decoding, the system stops reading after it has read a stream of the specified size. In either case, it stops writing or reading and generates an interrupt. The interrupt is a VLCS error termination interrupt if the VBAE bit in VP5_IRQ_ENB is 0 or a stream A buffer end interrupt if that bit is 1. The bits should be set before the start of the VPU5HG VLCS and after the generation of a stream A buffer end interrupt. For decoding, the stream A buffer size should be specified with command type 8 in the command stream (see section 23.6.2 (3), Command Stream, and thus this register's settings are ignored at activation time.

37.3.46 Stream B Buffer Size Register (VP5_VLC_STRB_BS)

Bit	Name	Setting value	Description
31 to 24	reserved	0	Reserved
23 to 0	VBSB		Stream B buffer size specification This parameter specifies the stream B buffer size in units of 256 bytes (with the low-order eight bits being 0). For decoding, the system stops reading after it has read a stream of the specified size. Also, it stops writing or reading and generates an interrupt. The interrupt is a VLCS error termination interrupt if the VBBE bit in VP5_IRQ_ENB is 0 or a stream B buffer end interrupt if that bit is 1. The bits should be set before the start of the VPU5HG VLCS and after the generation of a stream B buffer end interrupt. At activation time, the stream B buffer size should be specified with command type 8 in the command stream (see section 23.6.2 (3), Command Stream) and thus this register's settings at activation time are ignored.

37.3.47 VLCS Intermediate Stream 0 Buffer Size Register (VP5_VLC_IS_BS0)

Bit	Name	Setting value	Description
31 to 24	reserved	0	Reserved
23 to 0	VIS0		VLCS intermediate stream 0 buffer size specification. This parameter specifies the VLCS intermediate stream 0 buffer size in units of 256 bytes (with the low-order eight bits being 0). For encoding, the VLCS stops reading after it has read intermediate stream 0 of the specified size. For decoding, the VLCS stops writing after it has written intermediate stream 0 of the specified size. In either case, it stops writing or reading and generates an interrupt. The interrupt is a VLCS error termination interrupt if the VISE0 bit in VP5_IRQ_ENB is 0 or a VLCS intermediate stream 0 buffer end interrupt if that bit is 1. The bits should be set before the start of the VPU5HG VLCS and after the generation of a VLCS intermediate stream 0 buffer end interrupt.

37.3.48 VLCS Intermediate Stream 1 Buffer Size Register (VP5_VLC_IS_BS1)

Bit	Name	Setting value	Description
31 to 24	reserved	0	Reserved
23 to 0	VIS1		VLCS intermediate stream 1 buffer size specification. This parameter specifies the VLCS intermediate stream 1 buffer size in units of 256 bytes (with the low-order eight bits being 0). For encoding, the VLCS stops reading after it has read intermediate stream 1 of the specified size. For decoding, the VLCS stops writing after it has written intermediate stream 1 of the specified size. In either case, it stops writing or reading and generates an interrupt. The interrupt is a VLCS error termination interrupt if the VISE1 bit in VP5_IRQ_ENB is 0 or a VLCS intermediate stream 1 buffer end interrupt if that bit is 1. The bits should be set before the start of the VPU5HG VLCS and after the generation of a VLCS intermediate stream 0 buffer end interrupt.

37.3.49 GDMAC Base Address Array Register 1 (VP5_BAAR1)

This register specifies the base address so the VPU5HG can access the external memory. The parameters in this register are required when starting the VLCS or CE. Table 27.29 lists the specifiable base addresses. Common bit fields are available for the base addresses shown in the table 27.29.

Table 27.28 Description of Base Address Array 1

No.	Address offset	Setting category	Associated DMA channel	Description	Remarks
8	H'040	CE	DECY1	Decode picture luminance base address	
9	H'048	CE	DECC1	Decode picture chrominance base address	
10	H'050	CE	DECBY1	Decode picture luminance base address (bottom field)	For frame structure and field picture arrangement only
11	H'058	CE	DECBC1	Decode picture chrominance base address (bottom field)	For frame structure and field picture arrangement only
12	H'060	CE	TMP1	Encode picture luminance base address	For encoding only
13	H'068	CE	TMP1	Encode picture chrominance base address	For encoding only
18	H'090	CE	MVINFO1	MV information (write) base address	
19	H'098	CE	MVINFOB1	MV information (odd MB line) (write) base address	PIC-AFF/MB-AFF
20	H'0A0	CE	MVR1	Anchor picture MV information (read) base address	
21	H'0AB	CE	MVRB1	Anchor picture MV information (odd MB line) (read) base address	PIC-AFF/MB-AFF
22	H'0B0	CE	CEIS1	CE1 intermediate stream base address	

No.	Address offset	Setting category	Associated DMA channel	Description	Remarks
23	H'0B8	CE	CEIC1	CE1 intermediate control stream base address	
28	H'0E0	VLCS	VLIS1	VLCS intermediate stream base address	
29	H'0E8	VLCS	VLCI1	VLCS intermediate control stream base address	
32	H'100	CE	DISPY1	Filter picture luminance base address	
33	H'108	CE	DISPC1	Filter picture chrominance base address	
34	H'110	CE	DISPBY1	Filter picture luminance base address (bottom field)	For frame structure and field picture arrangement only
35	H’118	CE	DISPBC1	Filter picture chrominance base address (bottom field)	For frame structure and field picture arrangement only

Table 27.29 VP5_BAAR1 Bit Fields

Bit	Name	Setting value	Description
63 to 32	BAA	Base address	32-bit base address.The smallest unit of external memory accessed at once by the VPU5HG is eight bytes. Be sure to set the low-order three bits for the address specified in BAAR to 0. The unit of alignment might be 32 bytes or more depending on the base address. Specify the base address according to the alignment.
31 to 0	reserved	Reserved	Reserved

In encoding and decoding, the intermediate stream and the intermediate stream control base address should be specified according to the case listed as follows.

At encoding time, CE output address is specified in the base address of the intermediate stream and the intermediate stream control to be set in VLCS as follows.

VP5_BAAR0.CEIS0 → VP5_BAAR1.VLIS1

VP5_VAAR0.CEIC0 → VP5_BAAR1.VLIC1

VP5_BAAR1.CEIS1 → VP5_BAAR0.VLIS0

VP5_BAAR1.CEIC1 → VP5_BAAR0.VLIC0

At decoding time, VLCS output address is specified in the base address of the intermediate stream and the intermediate stream control to be set CE as follows.

VP5_BAAR0.VLIS0 → VP5_BAAR0.CEIS0

VP5_BAAR0.VLIC0 → VP5_BAAR0.CEIC0

VP5_BAAR1.VLIS1 → VP5_BAAR1.CEIS1

VP5_BAAR1.VLIC1 → VP5_BAAR1.CEIC1

In encoding and decoding, the MV information base address should be specified according to the case listed as follows.

At encoding time, MV information base address is specified as follows.

Anchor flame: VP5_BAAR0.MVINFO0 → VP5_BAAR1.MVR1

Anchor flame: VP5_VAAR0. MVINFOB0 → VP5_BAAR1. MVRB1

Anchor flame: VP5_BAAR1. MVINFO1 → VP5_BAAR0. MVR0

Anchor flame: VP5_BAAR1. MVINFOB1 → VP5_BAAR0. MVRB0

At decoding time, MV information base address is specified as follows.

Anchor flame: VP5_BAAR0. MVINFO 0 → VP5_BAAR0. MVR0

Anchor flame: VP5_BAAR0. MVINFOB0 → VP5_BAAR0. MVRB0

Anchor flame: VP5_BAAR1. MVINFO1 → VP5_BAAR1. MVR1

Anchor flame: VP5_BAAR1. MVINFOB1 → VP5_BAAR1. MVRB1

37.3.50 Decode Luminance Picture DMA Channel Register 1 (VP5_CE_DCHR_DECY1)

This register specifies the operation of the DMA channel (DECY1) to output decode luminance pictures or local decode luminance pictures. The parameters in this register are required when starting the CE.This register contains the same bit fields as those in VP5_CE_DCHR_DEY0. Set the bit fields to the values which are the same as those for VP5_CE_DCHR_DEY0.

37.3.51 Decode Chrominance DMA Channel Register 1 (VP5_CE_DCHR_DECC1)

This register specifies the operation of the DMA channel (DECC1) to output decode chrominance pictures or local decode chrominance pictures. The parameters in this register are required when starting the CE.This register contains the same bit fields as those in VP5_CE_DCHR_DECC0. Set the bit fields to the values which are the same as those for VP5_CE_DCHR_DECC0.

37.3.52 Filter Luminance Picture DMA Channel Register 1 (VP5_CE_DCHR_DISPY1)

This register specifies the operation of the DMA channel (DECY1) to output filter luminance pictures.

The parameters in this register are required when starting the CE by using the post filter for MPEG-2/MPEG-1/MPEG-4/H.263 processing. They are also required when starting the CE for VC-1 RangeReduction and RangeMapping stream decoding.

This register contains the same bit fields as VP5_CE_DCHR_DISPY0. Set the same values as those for VP5_CE_DCHR_DISPY0.

37.3.53 Filter chrominance Picture DMA Channel Register 1 (VP5_CE_DCHR_DISPC1)

This register specifies the operation of the DMA channel (DECC1) to output filter chrominance pictures.

The parameters in this register are required when starting the CE by using the post filter for MPEG-2/MPEG-1/MPEG-4/H.263 processing. They are also required when starting the CE for VC-1 RangeReduction and RangeMapping stream decoding.

This register contains the same bit fields as VP5_CE_DCHR_DISPC0. Set the same values as those for VP5_CE_DCHR_DISPC0.

37.3.54 Coded-Picture DMA Channel Register (VP5_CE_DCHR_TMP1)

This register specifies the operation of the DMA channel (TMP1) to read encoded pictures (templates). The parameters in this register are required when starting the CE. This register need not be set for decoding.

Bit	Name	Setting value	Description
63 to 48	(reserved)	H'B000	Always set to this value.
47 to 43	(reserved)	0	Always set to this value.
42 to 32	hsize		Horizontal size of the picture area. (The bits are set to a value rounded up to a multiple 16 and divided by 8.) Set to twice the horizontal size of the picture area when the encode pictures are stored as frame pictures in external memory for field encoding.
31 to 16	(reserved)	H'0000	Always set to this value.
15 to 13	endian	0 to 7	Endian. (Refer to table 27.22)
12 to 9	src_offset	0	Set to 0.
8 to 0	(reserved)	0	Always set to this value.

37.3.55 MV Information Output DMA Channel Register 1 (VP5_CE_DCHR_MBINFO1)

This register specifies the operation of the DMA channel to output MV information. The parameters in this register are required when starting the CE. Set the EMASK bit to H'0 by using the initialization routine format. This register contains the same bit fields as those in VP5_CE_DCHR_MVINFO0. Set the bit fields to the values which are the same as those for VP5_CE_DCHR_MVINFO0.

37.3.56 Odd MB Line MV Information Output DMA Channel Register 1 (VP5_CE_DCHR_MVINFOB1)

This register specifies the operation of the DMA channel (MVINFOB1) to output MV information about odd-numbered MB lines for the H.264 PIC-AFF or MB-AFF. The parameters in this register are required when starting the CE. This register need not be set when no MV information is output. This register contains the same bit fields as those in VP5_CE_DCHR_MVINFOB0. Set the bit fields to the values which are the same as those for VP5_CE_DCHR_MVINFOB0.

37.3.57 Anchor Picture MV Information DMA Channel register 1 (VP5_CE_DCHR_MVR1)

This register specifies the operation of the DMA channel (MVR1) to read anchor picture MV information. The parameters in this register are required when starting the CE. When this register is set, the external memory is accessed at the same time. Thus, it must not be set when no anchor picture MV information is used. This register contains the same bit fields as those in VP5_CE_DCHR_MVR0. Set the bit fields to the values which are the same as those for VP5_CE_DCHR_MVR0.

37.3.58 Anchor Picture Odd MB Line MV Information DMA Channel register 1 (VP5_CE_DCHR_MVRB1)

This register specifies the operation of the DMA channel (MVRB1) to read anchor picture MV information about odd-numbered MB lines for the H.264 PIC-AFF or MB-AFF. The parameters in this register are required when starting the CE. When this register is set, the external memory is accessed at the same time. Thus, it must not be set when no anchor picture MV information is used. This register contains the same bit fields as those in VP5_CE_DCHR_MVRB0. Set the bit fields to the values which are the same as those for VP5_CE_DCHR_MVRB0.

37.3.59 CE Intermediate Stream DMA Channel Register 1 (VP5_CE_DCHR_CEIS1)

This register specifies the operation of the DMA channel (CEIS1) which allows the CE to input/output intermediate streams. The parameters in this register are required when starting the CE.

This register contains the same bit fields as those in VP5_CE_DCHR_CEIS0. Set the bit fields to the values which are the same as those for VP5_CE_DCHR_CEIS0.

- Decoding

Bit	Name	Setting value	Description
63 to 32	(reserved)	H'8980 7000	Always set this value.
31 to 16	(reserved)	H'0000	Always set this value.
15 to 13	endian	0 to 7	Endian (See table 27.22)
12 to 9	Src_offset	8	Set to 8.
8 to 0	(reserved)	22	Always set this value.

37.3.60 CE Intermediate Control Stream DMA Channel Register 1 (VP5_CE_DCHR_CEIC1)

This register specifies the operation of the DMA channel (CEIS1) which allows the CE to input/output intermediate control streams. The parameters in this register are required when starting the CE.

This register contains the same bit fields as those in VP5_CE_DCHR_CEIC0. Set the bit fields to the values which are the same as those for VP5_CE_DCHR_CEIC0.

- Decoding

Bit	Name	Setting value	Description
63 to 32	(reserved)	H'88B0 7000	Always set this value.
31 to 16	(reserved)	H'0000	Always set this value.
15 to 13	endian	0 to 7	Endian (See table 27.22)
12 to 9	Src_offset	8	Set to 8.
8 to 0	(reserved)	23	Always set this value.

37.3.61 CE Intermediate Stream 1 Buffer Size Register (VP5_CE_IS_BS1)

Bit	Name	Setting value	Description
31 to 25	reserved	0	Reserved
24	CNT1	0, 1	When starts the continue, set to 1.
23 to 9	CIS1		CE intermediate stream 1 buffer size specification. This parameter specifies the intermediate stream 1 buffer size in 256-byte units (with the low-order eight bits being 0). For encoding, the CE stops writing after it has written intermediate stream 1 of the specified size. For decoding, the CE stops reading after it has read intermediate stream 1 of the specified size. In either case, it stops writing or reading and generates an interrupt. The interrupt is a CE error termination interrupt if the CIE1 bit in VP5_IRQ_ENB is 0 or a CE intermediate stream 1 buffer end interrupt if that bit is 1. The bits should be set before the start of the VPU5HG CE and after the generation of a CE intermediate stream 1 buffer end interrupt.
8 to 0	reserved	0	Reserved

37.3.62 DEB1 LMDMA Synchronization Register (VP5_CE_DEB_LMDMASR1)

Bit	Name	Setting value	Description
63 to 36	(reserved)	0	Reserved
35 to 32	GRC	4	Set to 4 for VPU5HG.
31 to 0	(reserved)	0	Reserved

37.3.63 VLCS Intermediate Stream DMA Channel Register 1 (VP5_VLC_DCHR_VLIS1)

This register specifies the operation of the DMA channel which allows the VLCS to input/output intermediate streams.

This register contains the same bit fields as those in VP5_CE_DCHR_VLIS0. Set the bit fields to the values which are the same as those for VP5_CE_DCHR_VLIS0.

37.3.64 VLCS Intermediate Control Stream DMA Channel Register 1 (VP5_VLC_DCHR_VLIC1)

This register specifies the operation of the DMA channel which allows the VLCS to input/output intermediate control streams. The parameters in this register are required when starting the VLCS. Set the EMASK bit to H'0 by using the initialization routine format.

This register contains the same bit fields as those in VP5_VLC_DCHR_VLIC0. Set the bit fields to the values which are the same as those for VP5_VLC_DCHR_VLIC0.

37.4 Command Stream Parameter Descriptions

The command stream parameters are slice-level parameters for H.264 decoding. They should be specified using a command stream. They constitute a single word with 64 bits. For decoding based on standards other than the H.264 standard, specify only VP5_VLC_CMD words 0 and 1 at the beginning of the frame.

37.4.1 Slice-Level Command Register (VP5_VLC_CMD)

This register contains parameters required for the STX to interpret the H.264 syntax. The parameters are required when starting the VLCS. They are set using a command stream. They make up the first parameter group in the command stream.

(1) VP5_VLC_CMD: Word 0

- H.264 Bit Field

Bit	Name	Setting value	Description
63 to 61	pic_type	0 to 2	Picture type 0: I 1: P 2: B Select 0 when concealing the entire picture. Set not only the other parameters in the command stream but also the internal registers assuming that I pictures are to be decoded. For information about concealing the entire picture, refer to section 28.6.2 (3), Command Stream.
60 to 56	refidx_last0	0 to 31	Valid number of L0 reference areas
52 to 48	refidx_last1	0 to 31	Valid number of L1 reference areas
47	bottom_field	0, 1	Bottom field flag 0: Top field 1: Bottom field
46	col_field_pic	0, 1	Anchor picture field flag 0: Frame 1: Field
45	rounding_type	0, 1	vop_rounding_type
44	wpred_flag	0, 1	Weighted-prediction flag 0: Weighted-prediction not used 1: Weighted-prediction used
42 to 40	wpred_wd_l	0 to 7	Weighted-prediction luminance scale (luma_log2_weight_denom)
38 to 36	wpred_wd_c	0 to 7	Weighted-prediction chrominance scale (chroma_log2_weight_denom)
33	alt_vscan	0, 1	alternate_vertical_scan
32	const_intra_pred	0, 1	constrained_intra_pred_flag
28 to 24	qp_c_offset0	(-12) to (+12)	qp_chroma_index_offset value (Cb for high profiles)

Bit	Name	Setting value	Description
23 to 19	qp_c_offset1	(-12) to (+12)	qp_chroma_index_offset value (Cr for high profiles)
17, 16	deblock_filter_idc	0 to 2	disable_deblocking_filter_idc
15 to 12	alpha_offset	(-6) to (+6)	slice_alpha_c0_offset_div2
11 to 8	beta_offset	(-6) to (+6)	slice_beta_offset_div2

- MPEG-2/MPEG-1 Bit Field

Bit	Name	Setting value	Description
63 to 61	pic_type	0 to 2	Picture type 0: I 1: P 2: B 4: D Select 0 when concealing the entire picture. Set not only the other parameters in the command stream but also the internal registers assuming that I pictures are to be decoded. For information about concealing the entire picture, refer to section 28.6.2 (3), Command Stream.
47	bottom_field	0, 1	Bottom field flag 0: Top field 1: Bottom field
35	full_pel_backward_vector	0, 1	full_pel_b_vector value (0 for MPEG-1/MPEG-2 processing)
34	full_pel_forward_vector	0, 1	full_pel_f_vector value (0 for MPEG-1/MPEG-2 processing)
33	alt_vscan	0, 1	alternate_vertical_scan
25	top_field_first	0, 1	0: Bottom field first 1: Top field first
24	concealment_motion_vector	0, 1	concealment_motion_vector Select 0 when concealing the entire picture. For information about concealing the entire picture, refer to section 28.6.2 (3), Command Stream.
23	frame_pred_frame_dct	0, 1	frame_pred_frame_dct
22	intra_vlc_format	0, 1	MPEG-2 intra-VLC table changeover
21, 20	intra_dc_precision	0 to 2	MPEG-2 intra-DC precision

- MPEG-4/H.263 Bit Field

Bit	Name	Setting value	Description
63 to 61	pic_type	0 to 2	Picture encode type 0: I 1: P 2: B Select 0 when concealing the entire picture. Set not only the other parameters in the command stream but also the internal registers assuming that I pictures are to be decoded. For information about concealing the entire picture, refer to section 28.6.2 (3), Command Stream.
45	rounding_type	0, 1	vop_rounding_type
42	resync_marker	0, 1	Always set to 1.
41	data_partitioned	0, 1	DP ON/OFF
40	reversible_vlc	0, 1	RVLC ON/OFF
38 to 26	intra_dc_vlc_thr	0, 1	intra_dc_vlc_thr value (VLCtable changeover QP threshold setting)
33	alt_vscan	0, 1	alternate_vertical_scan 0: zigzag scan 1: alternate scan
25	top_field_first	0, 1	0: Bottom field first 1: Top field first

- VC-1 Bit Field

Bit	Name	Setting value	Description
63 to 61	pic_type	0 to 2	Picture type 0: I 1: P 2: B Use 0 for selecting BI. Select 0 when intra-concealing the entire picture. Set not only the other parameters in the command stream but also the internal registers assuming that I pictures are to be decoded. Select 1 when inter-concealing the entire picture. Set not only the other parameters in the command stream but also the internal registers assuming that P pictures are to be decoded. For information about concealing the entire picture, refer to section 28.6.2 (3), Command Stream.
55	ref_interlace0	0, 1	Reference area type for baa_pointer value 0 0: Progressive 1: Int-Frame/Field
54	ref_interlace1	0, 1	Reference area type for baa_pointer value 1 0: Progressive 1: Int-Frame/Field
53	ref_interlace2	0, 1	Reference area type for baa_pointer value 2 0: Progressive 1: Int-Frame/Field
52	ref_interlace3	0, 1	Reference area type for baa_pointer value 3 0: Progressive 1: Int-Frame/Field
51	range_mapy_flag	0, 1	RANGE_MAPY_FLAG
50	range_mapuv_flag	0, 1	RANGE_MAPUV_FLAG
48	second_field	0, 1	2nd field flag 0: 1st field 1: 2nd field

Bit	Name	Setting value	Description
47	bottom_field	0, 1	Bottom field flag 0: Top field 1: Bottom field
46	col_field_pic	0, 1	Anchor picture field flag 0: Frame 1: Field
45	rounding_type	0, 1	vop_rounding_type
43, 42	range_mapy	0 to 3	RANGE_MAPY low-order two bits
41 to 39	range_mapuv	0 to 7	RANGE_MAPUV
38	range_red	0, 1	Range reduction 0: Invalid 1: Valid
37	range_red_cur	0, 1	RANGEREDFRM for the current frame 0: Invalid 1: Valid
36	range_red_ref	0, 1	RANGEREDFRAM for the forward reference frame 0: Invalid 1: Valid
35	intensity comp	0, 1	Intensity compensation 0: Invalid 1: Valid
34	uniform_quantizer	0, 1	0: uniform quantizer 1: non-uniform quantizer
33	alt_vscan	0, 1	alternate_vertical_scan 0: zigzag scan 1: alternate scan
31 to 26	pquant	1 to 31	PQUANT value
25	bi_linear	0, 1	Specifies whether the filter for half pel interpolation is bi-linear or bi-cubic. 0: Bi-Cubic 1: Bi-Linear
24	vc1_loopfilter	0, 1	VC-1 loop filter
23	fastuvmc	0, 1	FASTUVMC enable

Bit	Name	Setting value	Description
22	overlap	0, 1	OVT enable for VC-1
21, 20	condover	0, 2, 3	CondOver 0: None 2: All 3: Some (selected based on the bit plane)
15	intcomp_double	0, 1	First-stage IntComp valid flag for the top field
14	intcomp_double2	0, 1	First-stage IntComp valid flag for the bottom field
13 to 8	lumascale	0 to 63	LUMSCALE for the progressive sequence or forward reference top field The default is 32.
7	intcomp_bwd	0, 1	IntComp valid flag for backward reference
5 to 0	lumashift	0 to 63	LUMSHIFT for the progressive sequence or forward reference top field The default is 0.

(2) VP5_VLC_CMD: Word 1

- H.264 Bit Field

Bit	Name	Setting value	Description
63 to 32	slice_size	—	Slice data size
29 to 24	slice_qp	0 to 51	Specifies the quantization parameter (included in PPS) for the first macroblock in the slice. Specifies pic_init_qp + slice_qp_delta.
23, 22	weighted_bipred_idc	0 to 2	Specifies weighted_bipred_idc.
21	direct_bot_use_flag	0, 1	Selected for the frame picture B_Slice in an MBAFF sequence. (topAbsDiffPOC<botAbsDiffPOC) ?0:1
20	direct_8x8_inference_ flag	1	Specifies direct_8 × 8_interface_flag.
19	direct_spatial_mv_ pred_flag	1	Specifies direct_spatial_mv_pred_flag.
18	transform_8x8_ mode_flag	0, 1	Specifies whether to use 8 × 8 integer conversion. 0: No 1: Yes
17, 16	cabac_init_idc	0 to 2	Specifies cabac_init_idc.
15, 14	collist_proc_mode	0 to 2	Specifies how to process mapcoltolist. 0: Uses a command stream for processing. 1: Processes data in MB line units. 2: Processes data in MB units. If 1 or 2 is selected, setting both a separate channel and VP5_VLC_MODE is necessary. Select 0 when concealing the entire picture. For information about concealing the entire picture, refer to section 28.6.2 (3), Command Stream.
13 to 8	InitialQpY	0 to 51	Specifies pic_init_qp included in PPS.

- MPEG-2/MPEG-4/H.263 Bit Field

Bit	Name	Setting value	Description
63 to 32	frame_size	—	Frame data size Select 0 when concealing the entire picture. For information about concealing the entire picture, refer to section 28.6.2 (3), Command Stream.
29 to 24	InitialQpY	1 to 31	InitialQpY (for MPEG-4 only)
23 to 20	fcode00	1 to 9	Specifies the fcode[0][0] value. MPEG-4 dec: 1 to 7 (forward fcode) H.263 dec: 1 MPEG-2 dec: 1 to 9 Others: Need not be selected.
19 to 16	fcode01	1 to 9	Specifies the fcode[0][1] value (or forward fcode for MPEG-4 processing).
15 to 12	fcode10	1 to 9	Specifies the fcode[1][0] value (or forward fcode for MPEG-4 processing).
11 to 8	fcode11	1 to 9	Specifies the fcode[1][1] value (or forward fcode for MPEG-4 processing).

- VC-1 Bit Field

Bit	Name	Setting value	Description
63 to 32	frame_size	—	Frame data size Select 0 when concealing the entire picture for decoding Advanced Profile. For information about concealing the entire picture, refer to section 28.6.2 (3), Command Stream.
29 to 24	InitialQpY	1 to 31	ALTPQUANT value
21, 20	mvrange	0 to 3	0: (H[-64,63.f] × V[-32,31.f]) 1: (H[-128,127.f] × V[-64,63.f]) 2: (H[-512,511.f] × V[-128,127.f]) 3: (H[-1024,1023.f] × V[-256,255.f])
19, 18	dmvrange	0 to 3	DMVRANGE value
17	REFFIELD	1, 0	REFFIELD value
16	HALFPEL value	1, 0	HALFPEL (0:Halfpel, 1: HalfpelBilinear)
15	numref	1, 0	NUMREF value
14	tff	1, 0	Top Field First value
13, 12	refdist_fwd	0 to 3	REFDIST FWD value (reduced to 3 if it is 4 or more)
11, 10	refdist_bwd	1, 0	REFDIST BWD value (reduced to 3 if it is 4 or more)
9	curfld	1, 0	first field = 0, second field = 1
8	ref0_bottom	1, 0	REF0_BOTTOM
7 to 0	pic_header_len	0 to 255	Picture Header length (0 to 255) Used for multi-slice images.

(3) VP5_VLC_CMD: Word 2

- H.264 Bit Fields

These bits specify whether the L0 and L1 reference pictures are top or bottom fields.

Bit	Name	Setting value	Description
63	ref_bottom_field[63]	0, 1	L0 prediction ref0 0: Top field 1: Bottom field
62	ref_bottom_field[62]	0, 1	L0 prediction ref1 0: Top field 1: Bottom field
61	ref_bottom_field[61]	0, 1	L0 prediction ref2 0: Top field 1: Bottom field
60	ref_bottom_field[60]	0, 1	L0 prediction ref3 0: Top field 1: Bottom field
:	:	0, 1	:
bit	ref_bottom_field[bit]	0, 1	L0 prediction ref[63-bit] 0: Top field 1: Bottom field
:	:	0, 1	:
33	ref_bottom_field[33]	0, 1	L0 prediction ref30 0: Top field 1: Bottom field
32	ref_bottom_field[32]	0, 1	L0 prediction ref31 0: Top field 1: Bottom field
31	ref_bottom_field[31]	0, 1	L0 prediction ref0 0: Top field 1: Bottom field

Bit	Name	Setting value	Description
30	ref_bottom_field[30]	0, 1	L0 prediction ref1 0: Top field 1: Bottom field
:	:	0, 1	:
bit	ref_bottom_field[bit]	0, 1	L0 prediction ref[31-bit] 0: Top field 1: Bottom field
:	:	0, 1	:
3	ref_bottom_field[3]	0, 1	L0 prediction ref28 0: Top field 1: Bottom field
2	ref_bottom_field[2]	0, 1	L0 prediction ref29 0: Top field 1: Bottom field
1	ref_bottom_field[1]	0, 1	L0 prediction ref30 0: Top field 1: Bottom field
0	ref_bottom_field[0]	0, 1	L0 prediction ref31 0: Top field 1: Bottom field

- MPEG-4 Bit Fields

Bit	Name	Setting value	Description
49 to 32	TRD		TRD[i] for B_direct (except δ[i])
17 to 0	TRB		TRB[i] for B_direct (except δ[i])

- VC-1 Bit Field

Bit	Name	Setting value	Description
63 to 58	lumascale5	0 to 63	LUMASCALE for backward reference (refer to figure 27.5)
			The default is 32.
57 to 52	lumashift5	0 to 63	LUMASHIFT for backward reference (refer to figure 27.5)
			The default is 0.
51 to 46	lumascale4	0 to 63	First-stage LUMASCALE for the forward reference bottom field (refer to figure 27.5)
			The default is 32.
45 to 40	lumashift4	0 to 63	First-stage LUMASHIFT for the forward reference bottom field (refer to figure 27.5)
			The default is 0.
39 to 34	lumascale3	0 to 63	First-stage LUMASCALE for the forward reference top field (refer to figure 27.5)
			The default is 32.
33 to 28	lumashift3	0 to 63	First-stage LUMASHIFT for the forward reference top field (refer to figure 27.5)
			The default is 0.
27 to 22	lumascale2	0 to 63	LUMASCALE for the forward reference bottom field (refer to figure 27.5)
			The default is 32.
21 to 16	lumashift2	0 to 63	LUMASHIFT for the forward reference bottom field (refer to figure 27.5)
			The default is 32.
15 to 0	ScaleFactor		Scale factor used for B_direct

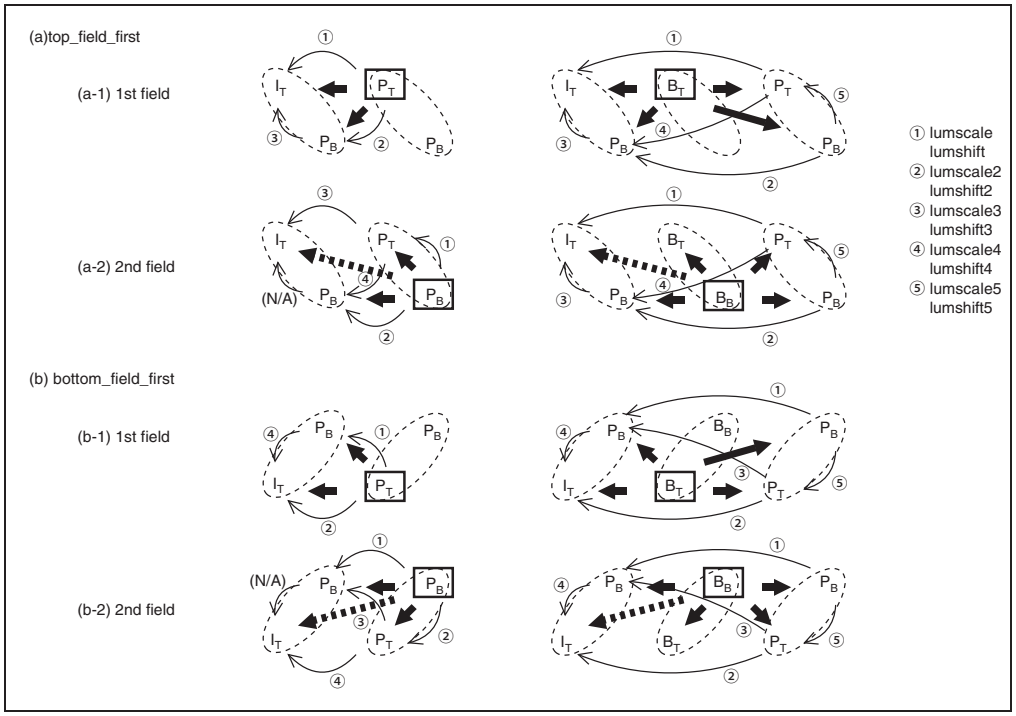


Figure 27.5 VC-1 intenity_compensation Parameter Settings

(4) VP5_VLC_CMD: Word 3

- VC-1 Bit Field

Bit	Name	Setting value	Description
63	TRANSDCTAB	0, 1	TRANSDCTAB
62	TRANSACTAB1	0 to 2	TRANSACTAB coding set
60, 59	TRANSACTAB2	0 to 2	TRANSACTAB2 coding set
58, 57	MVMODE	0 to 3	0: 1-MV Half-pel bilinear 1: 1-MV Half-pel 2: 1-MV 3: Mixed-MV
56, 55	MVTAB	0 to 3	MVTAB (Table 51 in the standard)
54, 53	CBPTAB	0 to 3	CBPTAB (Table 52 in the standard)
52	TTMBF	0, 1	TTMBF 0: MB or frame level 1: MB level
51, 50	TTFRM	0 to 3	Transform Type for TTMBF = 1 0: 8 × 8 1: 8 × 4 2: 4 × 8 3: 4 × 4
49, 48	DQPROFILE	0 to 3	DQPROFILE 0: all for edges 1: double edge 2: single edge 3: all MBs
47	DQUANTFRM	0, 1	DQUANTFRM (set to 1 even if DQUANT == 2)

Bit	Name	Setting value	Description
46, 45	DQEDGE	0 to 3	MB location where Q is changed for the single edge 0: left 1: top 2: right 3: bottom MB location where Q is changed for the double edge 0: left&top 1: top&right 2: right&bottom 3: bottom&left
44, 43	DQUANT	0 to 3	DQUANT value
42	DQBILEVEL	0, 1	DQBILEVEL
41, 40	ACPRED bitplane	0 to 2	0: Raw 1: Diff 2: Others For VC-1 processing, select 1 when inter-concealing the entire picture. For information about concealing the entire picture, refer to section 28.6.2 (3), Command Stream.
39, 38	OVERFLAGS bitplane	0 to 2	0: Raw 1: Diff 2: Others For VC-1 processing, select 1 when inter-concealing the entire picture. For information about concealing the entire picture, refer to section 28.6.2 (3), Command Stream.

Bit	Name	Setting value	Description
37, 36	MVTYPEMB bitplane	0 to 2	0: Raw 1: Diff 2: Others For VC-1 processing, select 1 when inter-concealing the entire picture. For information about concealing the entire picture, refer to section 28.6.2 (3), Command Stream.
35, 34	SKIPMB bitplane	0 to 2	0: Raw 1: Diff 2: Others For VC-1 processing, select 1 when inter-concealing the entire picture. For information about concealing the entire picture, refer to section 28.6.2 (3), Command Stream.
33, 32	DIRECTMB bitplane	0 to 2	0: Raw 1: Diff 2: Others For VC-1 processing, select 1 when inter-concealing the entire picture. For information about concealing the entire picture, refer to section 28.6.2 (3), Command Stream.
31, 30	FIELDTX bitplane	0 to 2	0: Raw 1: Diff 2: Others For VC-1 processing, select 1 when inter-concealing the entire picture. For information about concealing the entire picture, refer to section 28.6.2 (3), Command Stream.

Bit	Name	Setting value	Description
29, 28	FORWARDMB bitplane	0 to 2	0: Raw 1: Diff 2: Others For VC-1 processing, select 1 when inter-concealing the entire picture. For information about inter-concealing the entire picture, refer to section 28.6.2 (3), Command Stream.
27	SYNCMARKER	0, 1	0: SyncMarker not provided 1: SyncMarker provided For VC-1 processing, select 1 when inter-concealing the entire picture. For information about concealing the entire picture, refer to section 28.6.2 (3), Command Stream.
26	PQINDEX	0, 1	0: PQINDEX ≦ 8 1: PQINDEX > 8
25	ACPRED invert	0, 1	ACPRED bitplane Invert bit
24	OVERFLAGS invert	0, 1	OVERFLAGS bitplane Invert bit
23	MVTYPEMB invert	0, 1	MVTYPEMB bitplane Invert bit
22	SKIPMB invert	0, 1	SKIPMB bitplane Invert bit
21	DIRECTMB invert	0, 1	DIRECTMB bitplane Invert bit
20	FIELDTX invert	0, 1	FIELDTX bitplane Invert bit
19	FORWARDMB invert	0, 1	FORWARDMB bitplane Invert bit
18 to 16	MBMODETAB	0 to 7	MBMODETAB (set for AP only)
15	HALFQP	0, 1	Half QP value in units of pictures
14 to 12	IMVTAB	0 to 7	IMVTAB (set for AP only)
11 to 9	ICBPTAB	0 to 7	ICBPTAB (set for AP only)
8 to 7	2MVBPTAB	0 to 3	2MVBPTAB (set for AP only)
5 to 4	4MVBPTAB	0 to 3	4MVBPTAB (set for AP only)

Bit	Name	Setting value	Description
0	SKIPFRAME	0, 1	Specifies how to conceal the entire pictue for VC-1 processing. 0: Intra concealment 1: Inter concealment For information about concealing the entire picture, refer to section 28.6.2 (3), Command Stream. Other options 0: Non-skipped frame 1: Skipped frame

37.4.2 Reference Address Conversion Table (VP5_VLC_REF_TBL)

For H.264 decoding, these bits provide parameters for updating the offset for the association between the list after REF_idx update for each slice and VP5_BAAR at the beginning of a picture and for respecifying the long or short term for each reference. These bits are specified in a command stream. They are added for P and B pictures. The number of words can vary depending on num_ref_frames.

If a reference picture with field_pic_flag = 0 is located in a separate address for each field, these bits specify the BAA pointer for the top field.

- VP5_REF_TBL Structure

Description	
if (pic_type != I_Pic) {	
for(i = 0; i <= ((num_ref_frames*2-1)/8); i++) {	
VP5_REF_TBL [i];	BAA pointer conversion table for L0 prediction with ref_idx = i
}	
}	
if (pic_type == B_Pic) {	
for(i = 0; i <= ((num_ref_frames*2-1)/8); i++) {	
VP5_REF_TBL [num_ref_frames+i];	BAA pointer conversion table for L1 prediction with ref_idx = i
}	
}	

- VP5_REF_TBL Words 0 through 7

Address offset	Name	Description
0000	VP5_REF_TBL[0]	BAA pointer conversion table for L0 prediction with ref_idx = 0 to 7
0008	VP5_REF_TBL[1]	BAA pointer conversion table for L0 prediction with ref_idx = 8 to 15
0010	VP5_REF_TBL[2]	BAA pointer conversion table for L0 prediction with ref_idx = 16 to 23
0018	VP5_REF_TBL[3]	BAA pointer conversion table for L0 prediction with ref_idx = 24 to 31
0020	VP5_REF_TBL[4]	BAA pointer conversion table for L1 prediction with ref_idx = 0 to 7
0028	VP5_REF_TBL[5]	BAA pointer conversion table for L1 prediction with ref_idx = 8 to 15
0030	VP5_REF_TBL[6]	BAA pointer conversion table for L1 prediction with ref_idx = 16 to 23
0038	VP5_REF_TBL[7]	BAA pointer conversion table for L1 prediction with ref_idx = 24 to 31

- VP5_REF_TBL[I:I = 0:3] Bit Fields

Bit	Setting Value	Description
63	0, 1	Flag for L0 prediction reference picture ref_idx[i*8+0] 0: Short term 1: Long term
62 to 56	0 to 31	BAA pointer for L0 prediction reference picture ref_idx[i*8+0]
55	0, 1	Flag for L0 prediction reference picture ref_idx[i*8+1] 0: Short term 1: Long term
54 to 48	0 to 31	BAA pointer for L0 prediction reference picture ref_idx[i*8+1]
47	0, 1	Flag for L0 prediction reference picture ref_idx[i*8+2] 0: Short term 1: Long term
46 to 40	0 to 31	BAA pointer for L0 prediction reference picture ref_idx[i*8+2]
39	0, 1	Flag for L0 prediction reference picture ref_idx[i*8+3] 0: Short term 1: Long term
38 to 32	0 to 31	BAA pointer for L0 prediction reference picture ref_idx[i*8+3]
31	0, 1	Flag for L0 prediction reference picture ref_idx[i*8+4] 0: Short term 1: Long term
30 to 24	0 to 31	BAA pointer for L0 prediction reference picture ref_idx[i*8+4]
23	0, 1	Flag for L0 prediction reference picture ref_idx[i*8+5] 0: Short term 1: Long term
22 to 16	0 to 31	BAA pointer for L0 prediction reference picture ref_idx[i*8+5]
15	0, 1	Flag for L0 prediction reference picture ref_idx[i*8+6] 0: Short term 1: Long term
14 to 8	0 to 31	BAA pointer for L0 prediction reference picture ref_idx[i*8+6]
7	0, 1	Flag for L0 prediction reference picture ref_idx[i*8+7] 0: Short term 1: Long term
6 to 0	0 to 31	BAA pointer for L0 prediction reference picture ref_idx[i*8+7]

- VP5_REF_TBL[i:i=4:7] Bit Fields

Bit	Setting Value	Description
63	0, 1	Flag for L1 prediction reference picture ref_idx[i*8+0] 0: Short term 1: Long term
62 to 56	0 to 31	BAA pointer for L1 prediction reference picture ref_idx[i*8+0]
55	0, 1	Flag for L1 prediction reference picture ref_idx[i*8+1] 0: Short term 1: Long term
54 to 48	0 to 31	BAA pointer for L1 prediction reference picture ref_idx[i*8+1]
47	0, 1	Flag for L1 prediction reference picture ref_idx[i*8+2] 0: Short term 1: Long term
46 to 40	0 to 31	BAA pointer for L1 prediction reference picture ref_idx[i*8+2]
39	0, 1	Flag for L1 prediction reference picture ref_idx[i*8+3] (0: Short term, 1: Long term
38 to 32	0 to 31	BAA pointer for L1 prediction reference picture ref_idx[i*8+3]
31	0, 1	Flag for L1 prediction reference picture ref_idx[i*8+4] 0: Short term 1: Long term
30 to 24	0 to 31	BAA pointer for L1 prediction reference picture ref_idx[i*8+4]
23	0, 1	Flag for L1 prediction reference picture ref_idx[i*8+5] 0: Short term 1: Long term
22 to 16	0 to 31	BAA pointer for L1 prediction reference picture ref_idx[i*8+5]
15	0, 1	Flag for L1 prediction reference picture ref_idx[i*8+6] 0: Short term 1: Long term
14 to 8	0 to 31	BAA pointer for L1 prediction reference picture ref_idx[i*8+6]
7	0, 1	Flag for L1 prediction reference picture ref_idx[i*8+7] 0: Short term 1: Long term
6 to 0	0 to 31	BAA pointer for L1 prediction reference picture ref_idx[i*8+7]

37.4.3 Anchor Picture MV Information Address (VP5_VLC_MVR_ADDR)

At H.264 decoding time, this register specifies the anchor picture MV information address in every slice using a command stream.

The setting is necessary at picture decoding time including B-slice.

1word setting for the 1CE.

Bit	Name	Setting value	Description
63 to 32	mvr_addr	—	Frame or top field anchor picture MV information address
31 to 0	mvr_addr_odd	—	Bottom field anchor picture MV information address

37.4.4 VP5_VLC_MCTL: MapColToList

These bits specify MapColToList for each slice for H.264 decoding. It is a mapping table of ref_idx values for the current picture which uses colPic ref_idx as the index. The number of words can vary depending on num_ref_frames.

Set these bits for temporal direct prediction used for B slices (when direct_spatial_mv_pred_flag = 0).

Address offset	Name	Description
H'0004_8068	VP5_VLC_MCTL[i:i=0]	ref_idx conversion table for the current picture for colPic L0 prediction ref_idx = 0 to 7
H'0004_8070	VP5_VLC_MCTL[i:i=1]	ref_idx conversion table for the current picture for colPic L0 prediction ref_idx = 8 to 15
H'0004_8078	VP5_VLC_MCTL[i:i=2]	ref_idx conversion table for the current picture for colPic L0 prediction ref_idx = 16 to 23
H'0004_8080	VP5_VLC_MCTL[i:i=3]	ref_idx conversion table for the current picture for colPic L0 prediction ref_idx = 24 to 31

- Bit Field Description

Bit	Setting Value	Description
63 to 56	0 to 31	ref_idx for the current picture for colPic ref_idx[i*8+0]
55 to 48	0 to 31	ref_idx for the current picture for colPic ref_idx[i*8+1]
47 to 40	0 to 31	ref_idx for the current picture for colPic ref_idx[i*8+2]
39 to 32	0 to 31	ref_idx for the current picture for colPic ref_idx[i*8+3]
31 to 24	0 to 31	ref_idx for the current picture for colPic ref_idx[i*8+4]
23 to 16	0 to 31	ref_idx for the current picture for colPic ref_idx[i*8+5]
15 to 8	0 to 31	ref_idx for the current picture for colPic ref_idx[i*8+6]
7 to 0	0 to 31	ref_idx for the current picture for colPic ref_idx[i*8+7]

37.4.5 VP5_VLC_POC: POC List

These bits specify the POC list for H.264 decoding. The number of words can vary depending on num_ref_frames.

Set these bits for temporal direct prediction used for B slices (when direct_spatial_mv_pred_flag = 0) or implicit weighted prediction.

- VP5_VLC_POC Structure

Description

```
if (pic_type == B_Pic) {
if (direct_spatial_mv_pred_flag == 0 || weighted_bipred_idc==implicit ) {
            for( i = 0; i <= (num_ref_frames+2); i++ ) {
          VP5_VLC_POC[i];                                          POC list
            }
      }
}
```

- Frame Used as the Current Picture

Address offset	Name	Description
0000	VP5_VLC_POC[0]	Current-picture POC ([63:32]: Top field, [31:0]: Bottom field)
0008	VP5_VLC_POC[1]	RefPicList1 POC ([63:32]: Top field, [31:0]: Bottom field)
0010	VP5_VLC_POC[2]	RefPicList0 ref_idx=0 POC ([63:32]: TOP field, [31:0]: Bottom field)
0018	VP5_VLC_POC[3]	RefPicList0 ref_idx=1 POC ([63:32]: TOP field, [31:0]: Bottom field)
0020	VP5_VLC_POC[4]	RefPicList0 ref_idx=2 POC ([63:32]: TOP field, [31:0]: Bottom field)
0028	VP5_VLC_POC[5]	RefPicList0 ref_idx=3 POC ([63:32]: TOP field, [31:0]: BOT field)
0030	VP5_VLC_POC[6]	RefPicList0 ref_idx=4 POC ([63:32]: TOP field, [31:0]: BOT field)
0038	VP5_VLC_POC[7]	RefPicList0 ref_idx=5 POC ([63:32]: TOP field, [31:0]: BOT field)
0040	VP5_VLC_POC[8]	RefPicList0 ref_idx=6 POC ([63:32]: TOP field, [31:0]: BOT field)
0048	VP5_VLC_POC[9]	RefPicList0 ref_idx=7 POC ([63:32]: TOP field, [31:0]: BOT field)
0050	VP5_VLC_POC[10]	RefPicList0 ref_idx=8 POC ([63:32]: TOP field, [31:0]: BOT field)
0058	VP5_VLC_POC[11]	RefPicList0 ref_idx=9 POC ([63:32]: TOP field, [31:0]: BOT field)
0060	VP5_VLC_POC[12]	RefPicList0 ref_idx=10 POC ([63:32]: TOP field, [31:0]: BOT field)
0068	VP5_VLC_POC[13]	RefPicList0 ref_idx=11 POC ([63:32]: TOP field, [31:0]: BOT field)
0070	VP5_VLC_POC[14]	RefPicList0 ref_idx=12 POC ([63:32]: TOP field, [31:0]: BOT field)
0078	VP5_VLC_POC[15]	RefPicList0 ref_idx=13 POC ([63:32]: TOP field, [31:0]: BOT field)
0080	VP5_VLC_POC[16]	RefPicList0 ref_idx=14 POC ([63:32]: TOP field, [31:0]: BOT m field)
0088	VP5_VLC_POC[17]	RefPicList0 ref_idx=15 POC ([63:32]: TOP field, [31:0]: BOT field)

- Field Used as the Current Picture

Address offset	Name	Description
0000	VP5_VLC_POC[0]	Current-picture POC ([63:32]: Top field, [31:0]: Bottom field)
0008	VP5_VLC_POC[1]	RefPicList1 POC ([63:32]: Top field, [31:0]: Bottom field)
0010	VP5_VLC_POC[2]	RefPicList0 ref_idx=0 POC ([63:32]: Top field, [31:0]: Bottom field)
0018	VP5_VLC_POC[3]	RefPicList0 ref_idx=1 POC ([63:32]: Top field, [31:0]: Bottom field)
0020	VP5_VLC_POC[4]	RefPicList0 ref_idx=2 POC ([63:32]: Top field, [31:0]: Bottom field)
0028	VP5_VLC_POC[5]	RefPicList0 ref_idx=3 POC ([63:32]: Top field, [31:0]: Bottom field)
0030	VP5_VLC_POC[6]	RefPicList0 ref_idx=4 POC ([63:32]: Top field, [31:0]: Bottom field)
0038	VP5_VLC_POC[7]	RefPicList0 ref_idx=5 POC ([63:32]: Top field, [31:0]: Bottom field)
0040	VP5_VLC_POC[8]	RefPicList0 ref_idx=6 POC ([63:32]: Top field, [31:0]: Bottom field)
0048	VP5_VLC_POC[9]	RefPicList0 ref_idx=7 POC ([63:32]: Top field, [31:0]: Bottom field)
0050	VP5_VLC_POC[10]	RefPicList0 ref_idx=8 POC ([63:32]: Top field, [31:0]: Bottom field)
0058	VP5_VLC_POC[11]	RefPicList0 ref_idx=9 POC ([63:32]: Top field, [31:0]: Bottom field)
0060	VP5_VLC_POC[12]	RefPicList0 ref_idx=10 POC ([63:32]: Top field, [31:0]: Bottom field)
0068	VP5_VLC_POC[13]	RefPicList0 ref_idx=11 POC ([63:32]: Top field, [31:0]: Bottom field)
0070	VP5_VLC_POC[14]	RefPicList0 ref_idx=12 POC ([63:32]: Top field, [31:0]: Bottom field)
0078	VP5_VLC_POC[15]	RefPicList0 ref_idx=13 POC ([63:32]: Top field, [31:0]: Bottom field)
0080	VP5_VLC_POC[16]	RefPicList0 ref_idx=14 POC ([63:32]: Top field, [31:0]: Bottom field)
0088	VP5_VLC_POC[17]	RefPicList0 ref_idx=15 POC ([63:32]: Top field, [31:0]: Bottom field)

37.4.6 Weighing Control Conversion Table (VP5_VLC_WP_TBL)

These bits provide parameters for updating the weighted prediction offset for each slice for H.264 decoding. Even when ref_idx is updated, specify the weighted prediction parameter consistent with ref_idx at the beginning of the picture. These bits should be set in a command stream.

The size specified in VP5_WP_TBL depends on num_ref_idx_10 and num_ref_idx_11. That size ranges from 2 words to 64 words (each consisting of 64 bits).

- VP5_WP_TBL Structure

Description	
for(I = 0; i <= num_ref_idx_l0_active_minus1; i++) {	
VP5_WP_TBL[i];	Weighted prediction parameter for L0 prediction with ref_idx = i.
}	
for(i = 0; i <= num_ref_idx_l1_active_minus1; i++) {	
VP5_WP_TBL[num_ref_idx_l0_active_minis1+i];	Weighted prediction parameter for L1 prediction with ref_idx = i.
}	

- Bit Fields in Each Word

Bit	Name	Setting Value	Description
63 to 48	reserved		Reserved
58 to 56	luma_log2_weight_denom	0 to 7	luma_log2_weight_denom (Don't care except for i = 0)
55	reserved		Reserved
54	luma_weight_ln_128	0, 1	luma_weight_ln[i] (n = 0 or 1) 128 flags 0: luma_weight_ln[i] = (-128) to 127 1: luma_weight_ln[i] = 128
53	chroma_weight_ln_128[0]	0, 1	chroma_weight_ln[i][0](Cb) (n = 0 or 1) 128 flags 0: chroma_weight_ln[i][0] = (-128) to 127 1: chroma_weight_ln[i][0] = 128
52	chroma_weight_ln_128[1]	0, 1	chroma_weight_ln[i][1](Cr) (n = 0 or 1) 128 flags 0: chroma_weight_ln[i][1] = (-128) to 127 1: chroma_weight_ln[i][1] = 128
51	reserved		Reserved
50 to 48	chroma_log2_weight_denom	0 to 7	chroma_log2_weight_denom (Don't care except for i = 0)
47 to 40	luma_weight_ln[i]	(-128) -127	luma_weight_ln[i] (n: 0/1)
39 to 32	luma_offset_ln[i]	(-128) -127	luma_offset_ln[i] (n: 0/1)
31 to 24	chroma_weight_ln[i][0]	(-128) -127	chroma_weight_ln[i][0](Cb) (n: 0/1)
23 to 16	chroma_offset_ln[i][0]	(-128) -127	chroma_offset_ln[i][0] (Cb) (n: 0/1)
15 to 8	chroma_weight_ln[i][1]	(-128) -127	chroma_weight_ln[i][1] (Cr) (n: 0/1)
7 to 0	chroma_offset_ln[i][1]	(-128) -127	chroma_offset_ln[i][1] (Cr) (n: 0/1)

37.4.7 Next-slice First-MB Number (VP5_VLC_NEXT_FMS_ADDR)

This register specifies the first MB number in the next slice with a command stream for H.264 decoding. Select 0 for the last slice of a picture.

Bit	Name	Setting value	Description
12 to 0	first_mb_number_in_next_slice	0 to 8159	First MB number in the next slice

37.4.8 MPEG-4 VP Header Decoding Parameter (VP5_VLC_BITLEN0)

Bit	Name	Setting value	Description
63 to 32	ldmac_base_adr		Decoding DP buffer start address (set only at MPEG-4 DP decoding time)
19 to 16	mb_num_bitlen	1 to 14	macroblock number bit length (set only at MPEG-4 decoding time)
4 to 0	vop_time_inc_bitlen	1 to 16	VOP time increment bit length (set only at MPEG-4 decoding time)

37.4.9 MPEG-4 VP Header Decoding Parameter (VP5_VLC_BITLEN1)

Bit	Name	Setting value	Description
39 to 32	modulo_time_base_bitlen	0 to 255	modulo time base bit length (set only at MPEG-4 decoding time)
14 to 0	total_number_of_mbs	1 to 16384	macroblock number in VOP (set only at MPEG-4 decoding time)

37.5 Data Stored in External RAM and Its Format

37.5.1 Encode Picture

An encode picture is an original picture encoded by the VPU5HG. It is required when starting the VPU5HG CE for encoding.

The VPU5HG uses 4:2:0 sampling to process pictures. This sampling involves one Cb (blue chrominance) pixel and one Cr (red chrominance) pixel for four Y (luminance) pixels. That is, there is one pixel of chrominance information for two vertical pixels x two horizontal pixels of luminance information. Human eyes are more sensitive to changes in luminance than they are to those in chrominance. Thus, information can be successfully compressed by using four pixels of luminance information and one pixel of chrominance information. Figure 27.6 shows the format for encoded pictures. The picture origin is in the upper left-hand corner.

The start address of an input/output picture should be aligned on a 32-byte boundary. In the address register for the VPU5HG, specify the physical memory address space which can be accessed from the bus controller connected to the VPU5HG.

If the horizontal size of a picture is insufficient and its rightmost edge does not reach a 16-byte boundary, add an empty area to the rightmost edge of each line to ensure that the line starts on the 16-byte boundary (the size of the empty area should be the same for each line). Even if the vertical size of a picture is not a multiple of 16 lines, a multiple of 16 lines are accessed. Thus, an accessible area including a coded picture consisting of a multiple of 16 lines is required. Chrominance blue (Cb) and chrominance red (Cr) should be stored alternately in units of sampling pixels (for details, refer to the chrominance format shown in figure 27.6).

Specify the horizontal size of an encode picture stored in memory as hsize in VP5_CE_DCHR_TMP. This size should be a value (horizontal size/8) in units of eight pixels. When the VPU5HG is used with the VBLx, the horizontal size can be set to 512, 1024 or 2048. Thus, hsize should be 64, 128 or 256.

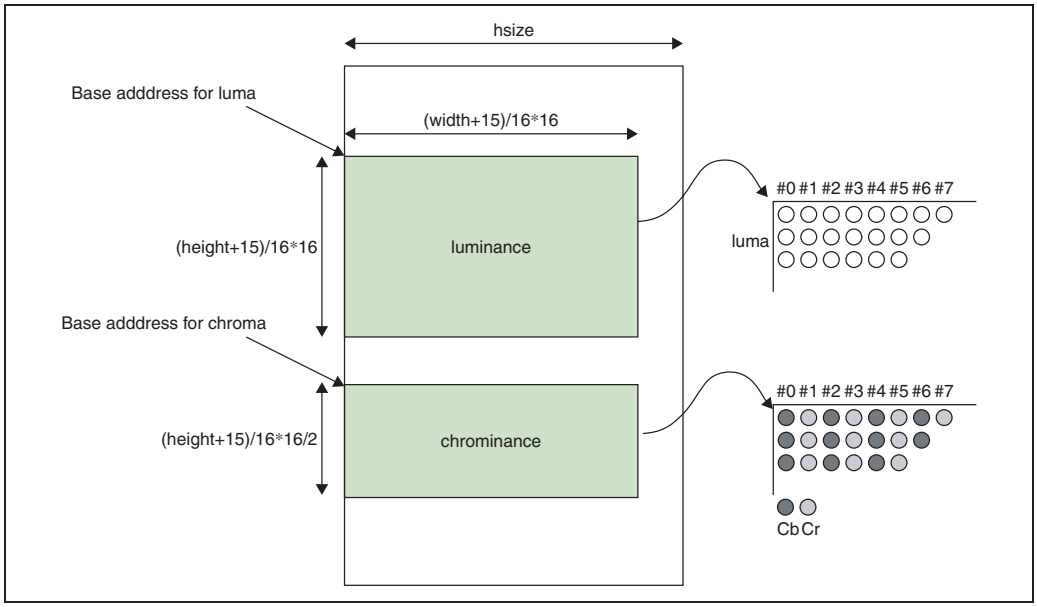


Figure 27.6 Picture Format

37.5.2 Reference Picture

A reference picture is required when starting the CE for encoding or decoding. Its format is shown in figure 27.6.

Specify the horizontal size of a reference picture stored in memory as hsize in VP5_CE_DCHR_REF. This size should be a value (horizontal size/8) in units of eight pixels. When the VPU5HG is used with the VBLx, the horizontal size can be set to 512, 1024 or 2048. Thus, hsize should be 64, 128 or 256.

37.5.3 Decode Picture

A decode picture is required when starting the CE for encoding or decoding. Its format is shown in figure 27.6.

Specify the horizontal size of a decode picture stored in memory as hsize in both VP5_CE_DCHR_DECY and VP5_CE_DCHR_DECC. This size should be a value (horizontal size/8) in units of eight pixels. When the VPU5HG is used with the VBLx, the horizontal size can be set to 512, 1024 or 2048. Thus, hsize should be 64, 128 or 256.

37.5.4 Stream

This is a data area required for starting the VLCS. Data are output for encoding and input for decoding.

The start address of the stream buffer should be aligned on a 32-byte boundary. Secure a stream data area whose size is in units of 256 bytes. Specify also the buffer size.

Streams are variable-length data. The VLCS accesses a position at a distance in 256 byte units from the start address of the buffer. When buffer end interrupts are disabled, the VLCS operation is forcibly terminated if an attempt is made to write or read data at a position after the last buffer address. An error is reported via the VP5_VLC_ERRH and VP5_VLC_ERRL registers. When buffer end interrupts are enabled, the VLCS operation is suspended if an attempt is made to write or read data at a position after the last buffer address. The VLCS waits until it resumes operation. If the end of the stream is 2048 bytes or less away from the last buffer address at the time of reading, a buffer end interrupt might occur and cause the VLCS to wait until it resumes operation.

Regardless of whether buffer end interrupts are enabled or disabled, a DMA prefetch is performed to read 512 additional bytes from the area after the last buffer address. Be careful not to make this area inaccessible.

At the time of decoding, specify the last buffer address for startup by using a command stream. To specify the last buffer address for resuming operation, use the VP5_VLC_STRA_BS register. For H.264 decoding, stream A and stream B are alternated for each slice so the streams can be read. Select the VP5_VLC_STRA_BS or VP5_VLC_STRB_BS register according to the buffer end interrupt source, and specify the last buffer address in the selected register.

At the time of encoding, stream A is used for writing streams. Thus, specify the last buffer address in the VP5_VLC_STRA_BS register.

37.5.5 Command Stream

A command stream is required when starting the VLCS for decoding.

A command stream is input for decoding by the VLCS. Specify a control parameter for each slice.

The start address of the command stream buffer should be aligned on a 32-byte boundary. Command stream data area should be established in 256-byte units. The VLCS access the area in 256-byte units starting at the buffer start address.

Allocate the command stream in consecutive memory areas.

37.5.6 Intermediate Stream

An intrermediate stream is used for buffering data between the VLCS and CE. It is a data area required for starting the VLCS and CE. At the time of encoding, an intermeidate stream is ouput from the CE and serves as an input for the VLCS. At the time of decoding, an intermediate stream is output from the VLCS and serves as an input for the CE.

The start address of the intermediate-stream buffer should be aligned on a 32-byte boundary. Secure an intermediate-stream data area whose size is in units of 512 bytes. Specify also the buffer size.

Intermediate streams are variable-length data. The VLCS accesses a position at a distance in 256 byte units from the start address of the buffer. When buffer end interrupts are disabled, the VLCS operation is forcibly terminated if an attempt is made to write or read data at a position after the last buffer address. An error is reported via the VP5_VLC_ERRH and VP5_VLC_ERRL registers.

When buffer end interrupts are enabled, the VLCS operation is suspended if an attempt is made to write or read data at a position after the last buffer address. The VLCS waits until it resumes operation. If the end of the stream is 2048 bytes or less away from the last buffer address at the time of reading, a buffer end interrupt might occur and cause the VLCS to wait until it resumes operation.

Regardless of whether buffer end interrupts are enabled or disabled, a DMA prefetch is performed to read 512 additional bytes from the area after the last buffer address. Be careful not to make this area inaccessible.

The CE accesses a position at a distance in units of 512 bytes for encoding (writing) or in units of 256 bytes for decoding (reading) from the buffer start address. If an attempt is made to write or read data at a position after the last buffer address, the CE suspends its operation and waits until it resumes operation. If the end of an intermediate stream is 2048 bytes or less away from the last buffer address at the time of reading, a buffer end interrupt might occur and cause the CE to wait until it resumes operation. At the time of reading, a DMA prefetch is performed to read 512 additional bytes from the area after the last buffer address. Be careful not to make this area inaccessible.

37.5.7 Intermediate Control Stream

An intermediate control stream is required when starting the VLCS and CE. It indicates encoded information about macroblocks for each CE.

An intermediate control stream is a fixed-length data stream consisting of 64 bits/MB for buffering data between the VLCS and CE. It occupies a buffer area whose size is 64 bits × MB count per frame. Figure 27.7 shows the format for intermediate control streams during normal processing (i.e., when ERR = 0). Figure 27.11 shows the format for intermediate control streams when an error occurs (i.e., when ERR = 1).

An intermediate control stream is input for encoding by the VLCS and output for decoding by the VLCS. It is output for encoding by the CE and input for decoding by the CE. An intermediate control stream is required for each CE. For the VPU5HG, two memory areas are required. An intermediate control stream consists of 64 bits/MB and its size depends on the picture size. A data area whose size is the number of macroblocks to be processed × 64 bits is accessed for each CE.

The start address of the intermediate control stream buffer should be aligned on a 32-byte boundary. The intermediate control stream data area should be established in 256-byte units.

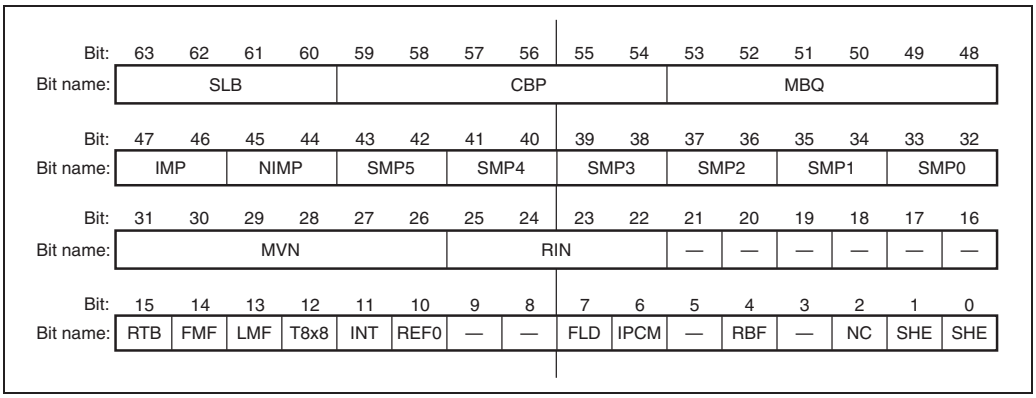


Figure 27.7 Intermediate Control Stream Format (for Normal Processing: H.264)

Bit	Bit Name	Description
63 to 60	SLB	Slice bound (0 to 15) MB slice boundary information (Bit 3: Left MB, Bit 2: Upper left MB, Bit 1: Upper MB, Bit 0: Upper right MB)
59 to 54	CBP	Coded Block Pattern (0 to 63) Coded block pattern ({CHROMA[1:0], Y3, Y2, Y1, Y0})
53 to 48	MBQ	MB Quant (0 to 51) MB quant value
47, 46	IMP	00: MB division is intra_16 × 16. (Only intra 16 × 16 is selected.) 01: MB division is intra_4 × 4. Inter_4 × 4 conversion is performed for inter MBs. 10: MB division is intra_8 × 8. Inter_8 × 8 conversion is performed for inter MBs. 11: Reserved
45, 44	NIMP	00: MB division is inter_16 × 16. 01: MB division is inter_16 × 8. 10: MB division is inter_8 × 16. 11: MB division is inter_8 × 8.

Bit	Bit Name	Description
43, 42	SMP5	Sub MB part5 00: Block 5 subMB division is 8 × 8. 01: Block 5 subMB division is 8 × 4. 10: Block 5 subMB division is 4 × 8. 11: Block 5 subMB division is 4 × 4.
41, 40	SMP4	Sub MB part4 00: Block 4 subMB division is 8 × 8. 01: Block 4 subMB division is 8 × 4. 10: Block 4 subMB division is 4 × 8. 11: Block 4 subMB division is 4 × 4.
39, 38	SMP3	Sub MB part3 00: Block 3 subMB division is 8 × 8. 01: Block 3 subMB division is 8 × 4. 10: Block 3 subMB division is 4 × 8. 11: Block 3 subMB division is 4 × 4.
37, 36	SMP2	Sub MB part2 00: Block 2 subMB division is 8 × 8. 01: Block 2 subMB division is 8 × 4. 10: Block 2 subMB division is 4 × 8. 11: Block 2 subMB division is 4 × 4.
35, 34	SMP1	Sub MB part1 00: Block 1 subMB division is 8 × 8. 01: Block 1 subMB division is 8 × 4. 10: Block 1 subMB division is 4 × 8. 11: Block 1 subMB division is 4 × 4.
33, 32	SMP0	Sub MB part0 00: Block 0 subMB division is 8 × 8. 01: Block 0 subMB division is 8 × 4. 10: Block 0 subMB division is 4 × 8. 11: Block 0 subMB division is 4 × 4.

Bit	Bit Name	Description
31 to 26	MVN	nv num 0: MV is not added. 1 to 32: MV count (for H or V set)
25 to 22	RIN	ref_idx num 0: ref_idx is not added. 1 to 8: ref_idx count.
21 to 16	—	reserved
15	RTV	reference table 0: Reference table is not added. 1: Reference table is added.
14	FMF	First MacroBlock flag 0: MB in the slice other than the first MB 1: First MB in the slice
13	LMF	Last MacroBlock flag 0: MB in the slice other than the last MB 1: Last MB in the slice.
12	T8 × 8	transform_size_8 × 8_flag 0: Transform is 4 × 4. 1: Transform is 8 × 8.
11	INT	Intra/Inter 0: Intra MB coding 1: Inter MB coding
10	REF0	Ref0 flag 0: Normal processing 1: Reference plane for all blocks is ref0.
9, 8	—	reserved
7	FLD	Field Pred 0: Frame MB 1: Field MB
6	IPCM	Intra_PCM 0: Normal MB 1: I_PCM MB

Bit	Bit Name	Description
5	—	reserved
4	RBF	ref_bottom_filed 0: ref_bottom_filed is not added. 1: ref_bottom_filed is added.
3	—	resered
2	NC	Not coded 0: Coded MB 1: Not coded MB
1	SLH	Slice Header Exist 0: Slice header is not added. 1: Slice header is added.
0	ERR	Error Flag 0: Normal MB 1: Error MB. If the error MB is 1, the bit field is the one shown in figure 27.9.

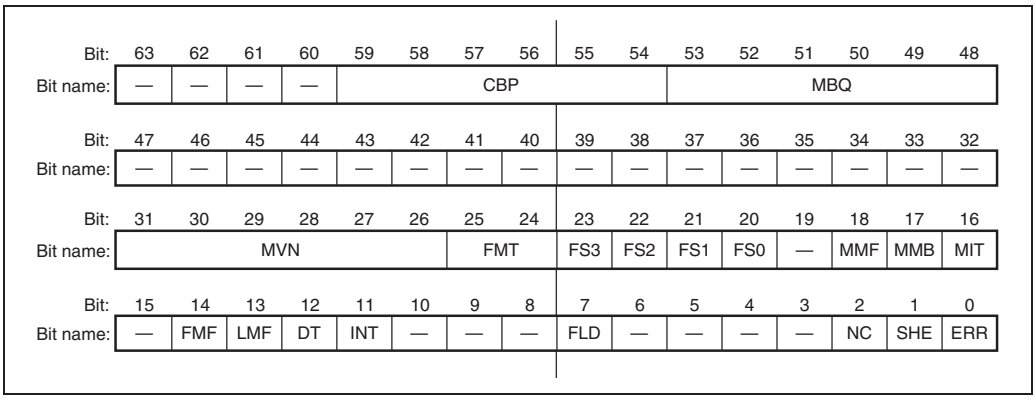


Figure 27.8 Intermediate Control Stream Format (for Normal Processing: MPEG-2)

Bit	Bit Name	Description
63 to 60	—	reserved
59 to 54	CBP	Coded Block Pattern (0 to 63) Coded block pattern ({Y0, Y1, Y2, Y3, Cb, Cr})
53 to 48	MBQ	MB Quant (1 to 31) MB quant value
47 to 32	—	reserved
31 to 26	MVN	Mv num 0: MV is not added. 1 to 4: MV count (for H or V set)

25, 24	FMT	FMT (0 to 3)
		(frame/field)_motion_type value. It is set to 0 if there is not macroblock_motion_forward/backward for the MB (INTRA). If no MC is specified, it is processed as described below.
		Additional Description:
		frame_motion_type is used for field pictures and field_motion_type is used for frame picture as the FMT value. Whether they are field or frame pictures can be determined as follows:
		if(macroblock_motion_forward||macroblock_motion_backward){ i
		f(picture_structue=='Frame'){
		if(frame_pred_frame_dct==0)
		frame_motion_type
		}else{
		field_motion_type
		}
		}
		
		In this determination, if frame_motion_type/field_motion_type cannot be found, field and frame pictures are processed as frame-based and field-based respectively.

23	FS3	Motion Vertical field Select 3 motion_vertical_field_select[Second-MV][BWD]
22	FS2	Motion Vertical field Select 2 motion_vertical_field_select[Second-MV][FWD]

Bit	Bit Name	Description
21	FS1	Motion Vertical field Select 1 motion_vertical_field_select[First-MV][BWD]
20	FS0	Motion Vertical field Select 0 motion_vertical_field_select[First-MV][BWD]
19	—	reserved
18	MMF	Macroblock Motion Forward macroblock_motion_forward value
17	MMB	Macroblock Motion Backward macroblock_motion_backward value
16	MIT	Macroblock Motion Intra macroblock_motion_intra value. MB mode can be selected by setting combination with MIT, MMF and MMB as listed in table 27.28.
15	—	reserved
14	FMF	First MacroBlock flag 0: MB in the slice other than the first MB 1: First MB in the slice
13	LMF	Last MacroBlock flag 0: MB in the slice other than the last MB 1: Last MB in the slice.
12	DT	DCT Type 0: Frame DCT 1: Field DCT
11	INT	Intra/Inter 0: Intra MB coding 1: Inter MB coding
10 to 8	—	reserved
7	FLD	Field Pred 0: Frame MB 1: Field MB
6 to 3	—	reserved

Bit	Bit Name	Description
2	NC	Not coded 0: Coded MB 1: Not coded MB
1	SHE	Slice Header Exist 0: Slice header is not added. 1: Slice header is added.
0	ERR	Error Flag 0: Normal MB 1: Error MB. If the error MB is 1, the bit field is the one shown in figure 27.9.

Table 27.30 MB Type

MIT	MMF	MMB	MB Type
1	0	0	INTRA
0	1	0	FWD-pred
0	0	1	BWD-pred
0	1	1	Interp-pred

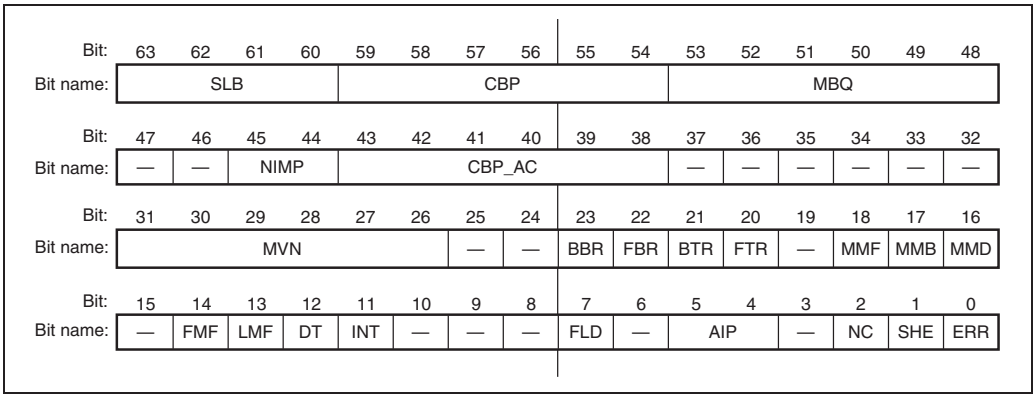


Figure 27.9 Intermediate Control Stream Format (for Normal Processing: MPEG-4)

Bit	Bit Name	Description
63 to 60	SLB	Slice bound (0 to 15) MB slice boundary information (Bit 3: Left MB, Bit 2: Upper left MB, Bit 1: Upper MB, Bit 0: Upper right MB)
59 to 54	CBP	Coded Block Pattern (0 to 63) Coded block pattern ({Y0, Y1, Y2, Y3, Cb, Cr})
53 to 48	MBQ	MB Quant (1 to 31) MB quant value
47, 46	—	reserved
45, 44	NIMP	Intra MB part 00: MB division is inter_16 × 16. 01: MB division is inter_16 × 8. 10: MB division is inter_8 × 16. 11: MB division is inter_8 × 8.
43, 38	CBPAC	Coded Block Pattern AC (0 to 63) Coded Block Pattern of AC component ({Y0, Y1, Y2, Y3, Cb, Cr})
37 to 32	—	reserved
31 to 26	MVN	mv num 0: MV is not added. 1 to 4: MV count (for H or V set)
25, 24	—	reserved

Bit	Bit Name	Description
23	BBR	backward Bottom field Reference forward_bottom_field_reference value (refer to BWD-bot MV 0:Top, 1:Bottom)
22	FBR	backward Bottom field Reference forward_bottom_field_reference value (refer to FWD-bot MV 0:Top, 1:Bottom)
21	BTR	backward Bottom field Reference forward_bottom_field_reference value (refer to BWD-top MV 0:Top, 1:Bottom)
20	FTR	backward Bottom field Reference forward_bottom_field_reference value (refer to FWD-top MV 0:Top, 1:Bottom)
19	—	reserved
18	MMF	Macroblock Motion Forward macroblock_motion_forward value
17	MMB	Macroblock Motion Backward macroblock_motion_backward value
16	MMD	Macroblock Motion Direct 0: Macroblock is not Direct prediction. (set 0 o except B-VOP) 1: Macroblock is direct prediction.
15	—	reserved
14	FMF	First MacroBlock flag 0: MB in the slice other than the first MB 1: First MB in the slice
13	LMF	Last MacroBlock flag 0: MB in the slice other than the last MB 1: Last MB in the slice.
12	DT	DCT type 0: Frame DCT 1: Field DCT
11	INT	Intra/Inter 0: Intra MB coding 1: Inter MB coding

Bit	Bit Name	Description
10 to 8	—	reserved
7	FLD	Field Pred 0: Frame MB 1: Field MB
6	—	reserved
5, 4	AIP	Advance Intra Pred flag 00: DC coefficient prediction is performed. 01: Vertical DC/AC coefficient prediction is performed. 10: Horizontal DC/AC coefficient prediction is performed. 11: Reserved
3	—	reserved
2	NC	Not coded 0: Coded MB 1: Not coded MB
1	SHE	Slice Header Exist 0: Slice header is not added. 1: Slice header is added.
0	ERR	Error Flag 0: Normal MB 1: Error MB. If the error MB is 1, the bit field is the one shown in figure 27.9.

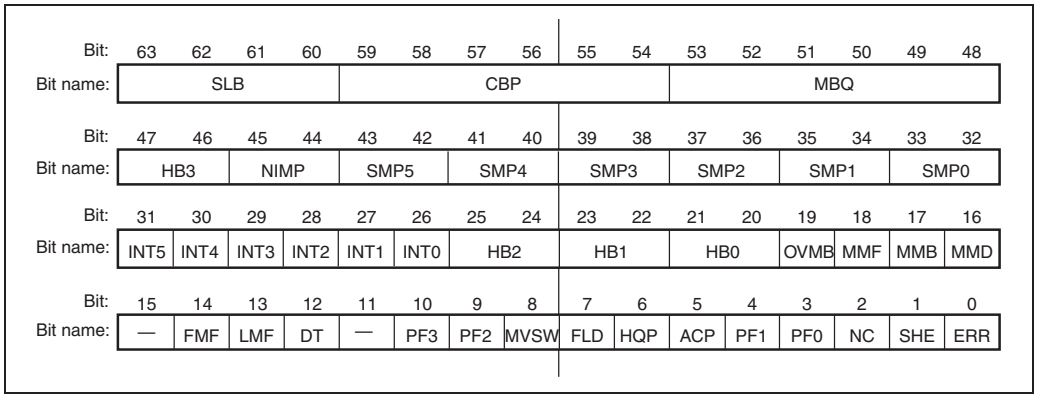


Figure 27.10 Intermediate Control Stream Format (VC-1)

Bit	Bit Name	Description
63 to 60	SLB	MB slice boundary information Bit 3: Left MB Bit 2: Upper left MB Bit 1: Upper MB Bit 0: Upper right MB)
59 to 54	CBP	Coded block pattern in the order of {Y0, Y1, Y2, Y3, Cb, Cr} from the MSB Each bit field in the CBP indicates 1 (coded) for the corresponding block when either DC or AC coefficient is not 0.
53 to 48	MBQ	MB quant value
47, 46	HB3	Hybrid MV Pred 3 00: Hybrid prediction is not used for the Y3 block. predictor_pre is used. 01: Reserved 10: Hybrid prediction is used for the Y3 block. predictor-C is used. 11: Hybrid prediction is used for the Y3 block. predictor-A is used.
45, 44	NIMP	Inter MB Part 00: MB division is inter_16 × 16. 11: MB division is inter_8 × 8 (for 4MV).

Bit	Bit Name	Description
43,42	SMP5	SubMB Part 5/Transform Type Cr for VC-1 00: Block 5 subMB division is 8 × 8. 01: Block 5 subMB division is 8 × 4. 10: Block 5 subMB division is 4 × 8. 11: Block 5 subMB division is 4 × 4.
41, 40	SMP4	SubMB Part 4/Transform Type Cb for VC-1 00: Block 4 subMB division is 8 × 8. 01: Block 4 subMB division is 8 × 4. 10: Block 4 subMB division is 4 × 8. 11: Block 4 subMB division is 4 × 4.
39, 38	SMP3	SubMB Part 3/Transform Type #3 for VC-1 00: Block 3 subMB division is 8 × 8. 01: Block 3 subMB division is 8 × 4. 10: Block 3 subMB division is 4 × 8. 11: Block 3 subMB division is 4 × 4.
37, 36	SMP2	SubMB Part 2/Transform Type #2 for VC-1 00: Block 2 subMB division is 8 × 8. 01: Block 2 subMB division is 8 × 4. 10: Block 2 subMB division is 4 × 8. 11: Block 2 subMB division is 4 × 4.
35, 34	SMP1	SubMB Part 1/Transform Type #1 for VC-1 00: Block 1 subMB division is 8 × 8. 01: Block 1 subMB division is 8 × 4. 10: Block 1 subMB division is 4 × 8. 11: Block 1 subMB division is 4 × 4.
33, 32	SMP0	SubMB Part 0/Transform Type #0 for VC-1 00: Block 0 subMB division is 8 × 8. 01: Block 0 subMB division is 8 × 4. 10: Block 0 subMB division is 4 × 8. 11: Block 0 subMB division is 4 × 4.
31	INT5	Cr Block Inter 0: Intra Cr block coding 1: Inter Cr block coding

Bit	Bit Name	Description
30	INT4	Cb Block Inter 0: Intra Cb block coding 1: Inter Cb block coding
29	INT3	Y Block 3 Inter 0: Intra Y block 3 coding 1: Inter Y block 3 coding
28	INT2	Y Block 2 Inter 0: Intra Y block 2 coding 1: Inter Y block 2 coding
27	INT1	Y Block 1 Inter 0: Intra Y block 1 coding 1: Inter Y block 1 coding
26	INT0	Y Block 0 Inter 0: Intra Y block 0 coding 1: Inter Y block 0 coding
25, 24	HB2	Hybrid MV Pred 2 00: Hybrid prediction is not used for the Y2 block. predictor_pre is used. 01: Reserved 10: Hybrid prediction is used for the Y2 block. predictor-C is used. 11: Hybrid prediction is used for the Y2 block. predictor-A is used.
23, 22	HB1	Hybrid MV Pred 1 00: Hybrid prediction is not used for the Y1 block. predictor_pre is used. 01: Reserved 10: Hybrid prediction is used for the Y1 block. predictor-C is used. 11: Hybrid prediction is used for the Y1 block. predictor-A is used.

Bit	Bit Name	Description
21, 20	HB0	Hybrid MV Pred 0 00: Hybrid prediction is not used for the Y0 block. predictor_pre is used. 01: Reserved 10: Hybrid prediction is used for the Y0 block. predictor-C is used. 11: Hybrid prediction is used for the Y0 block. predictor-A is used.
19	OVMB	OVERFLAGMB 0: Overlapped transform is not used. 1: Overlapped transform is used.
18	MMF	Macroblock Motion Forward 0: The macroblock has no forward-prediction motion vector (such as a skip MB). 1: The macroblock has forward-prediction motion vectors.
17	MMB	Macroblock Motion Backward 0: The macroblock has no forward-prediction motion vector (such as a skip MB). 1: The macroblock has forward-prediction motion vectors.
16	MMD	Macroblock Motion Direct 0: The macroblock is not set to direct prediction mode (always 0 except for B-VOP) 1: The macroblock is set to direct prediction mode
15	-	reserve
14	FMF	First MacroBlock flag 0: MB in the slice other than the first MB 1: First MB in the slice
13	LMF	Last MacroBlock flag 0: MB in the slice other than the last MB 1: Last MB in the slice.
12	DT	DCT Type 0: Frame DCT is used. 1: Field DCT is used.

Bit	Bit Name	Description
10	PF3	PF3 0: The prediction flag for block 3 is 0. 1: The prediction flag for block 3 is 1.
9	PF2	PF2 0: The prediction flag for block 2 is 0. 1: The prediction flag for block 2 is 1.
8	MVSW	MVSW 0: When the motion vector is TOP => BOTTOM, the vector is not reversed. 1: When the motion vector is TOP => BOTTOM, the vector is reversed.
7	FLD	Field Pred 0: Frame prediction MB (Note: The DCT type depends on T8 × 8) 1: Field prediction MB (Note: The DCT type depends on T8 × 8)
6	HQP	Half QP 0: The half QP value for the macroblock is 0 1: The half QP value for the macroblock is 1
5	ACP	AC Pred Flag 0: AC coefficient prediction is not used. 1: AC coefficient prediction is used.
4	PF1	PF1 0: The prediction flag for block 1 is 0. 1: The prediction flag for block 1 is 1.
3	PF0	PF0 0: The prediction flag for block 0 is 0. 1: The prediction flag for block 0 is 1.
2	NC	Not Coded 0: Coded MB 1: P-VOP: Not Coded MB
1	SLH	Slice Header Exist 0: Slice header is not added. 1: Slice header is added.

Bit	Bit Name	Description
0	ERR	Error Flag 0: Normal MB 1: Error MB. If the error flag is 1, the bit field is the one shown in table 27.11.

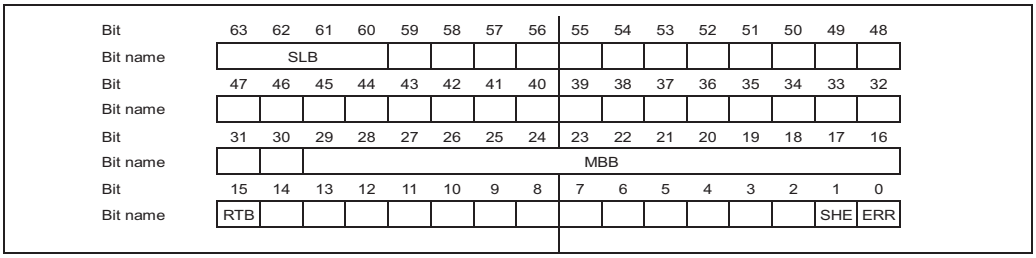


Figure 27.11 Intermeidate Control Stream Format (for Error Macroblocks)

Bit	Bit Name	Description
63 to 60	SLB	Slice bound (0 to 15) MB slice boundary information (Bit 3: Left MB, Bit 2: Upper left MB, Bit 1: Upper MB, Bit 0: Upper right MB)
59 to 30	—	reserved
29 to 16	MBB	Macroblock bit (0 to 16383) Error macroblock coding amount.
15	RTB	refernce table 0: reference table is not added. 1: reference table is added.
14 to 2	—	reserved
1	SHE	Slice Header Exist 0: Slice header not added 1: Slice header added
0	ERR	Error Flag 0: Normal MB. If the ERR is 0, the bit field is the one shown in figure 27.9. 1: Error MB.

37.5.8 Motion Vector

It indicates encoded information about a macroblock.

Direct prediction in a B-VOP/slice requires the motion vector for referenced pictures. Thus, the external RAM should contain 2 buffer areas for each frame (field pair) that hold motion vectors. Two buffer areas are required for each frame (field pair) if PIC_AFF is not used while four buffer areas are required for each frame (field pair) if PIC_AFF is used. For MPEG-4/H.263 encoding which involves one CE, one buffer area is required for each frame (field pair). Each buffer area must be established as a consecutive area. This is because it is to be used as one area for even and odd lines in decoding the frame structure.

The buffer area should be established in 256-byte units with the size that can accommodate the data size shown in table 27.31, aligning to a 32-byte boundary. The data size and number of banks to be established per MB for each picture structure are shown in table 27.32.

Table 27.31 Motion Vector Buffer Size

Picture structure	Buffer area	Data size per buffer
Frame	TOP	MB_DATA_SIZE*mb_width*(mb_height + 1)/2
	BOTTOM	MB_DATA_SIZE*mb_width*(mb_height + 1)/2
Frame (1CE encoding)	—	MB_DATA_SIZE*mb_wdth*mb_height
field	TOP	MB_DATA_SIZE*mb_width*(mb_height + 1)/2
	BOTTOM	MB_DATA_SIZE*mb_width*(mb_height + 1)/2
PIC_AFF	TOP EVEN	MB_DATA_SIZE*mb_width*(mb_height + 3)/4
	TOP ODD	MB_DATA_SIZE*mb_width*(mb_height + 3)/4
	BOTTOM EVEN	MB_DATA_SIZE*mb_width*(mb_height + 3)/4
	BOTTOM ODD	MB_DATA_SIZE*mb_width*(mb_height + 3)/4

Table 27.32 Motion Vector Data Size and Number of Bank

Stream Type (w/Profile Name)	Data size per MB (MB_DATA_SIZE)	Number of bank
H.264 decode	64 Bytes	num_ref_rames + 1
H.264 decode	16 Bytes	num_ref_rames + 1
the others decode	64 Bytes	2
the others decode	16 Bytes	2

When a sequence including a B-VOP/slice is decoded or encoded, a motion vector is output by setting the buffer start address to No. 18 (offset H'090) MV information (write) base address in the base address array and setting the VP5_CE_VLCF mv_info bit (motion vector information output specification) to 1. When a B-VOP/slice is decoded or encoded, the start address of the buffer which contains motion vector output used for decoding or encoding the reference picture (or anchor picture for H.264) is set to No. 20 (offset H'0A0) anchor picture MV information (read) base address. Input and output operations are independent of each other. They might take place at the same time.

Table 27.33 Motion Vector Channel Setting Examples(Decode)

	current Frame Pic		Current Field Pic(Top) *	
	read	write	read	write
col frame Pic	CE0 ch0: BOT EVEN	CE0 ch0: BOT EVEN	CE0 ch0: TOP ODD	CE0 ch0: TOP ODD
	CE0 ch1: BOT ODD	CE0 ch1: BOT ODD	CE0 ch1: BOT ODD	CE1 ch0: TOP EVEN
	CE1 ch0: TOPEVEN	CE1 ch0: TOP EVEN	CE1 ch0: TOP EVEN	
	CE1 ch1: TOP ODD	CE1 ch1: TOP ODD	CE1 ch1: BOT EVEN	
col Field Pic(Tpo) *	CE0 ch0: TOP EVEN	CE0 ch0: BOT EVEN	CE0 ch0: TOP ODD	CE0 ch0: TOP ODD
	CE0 ch1: TOP ODD	CE0 ch1: BOT ODD	CE1 ch0: TOP EVEN	CE1 ch0: TOP EVEN
	CE1 ch0: TOP EVEN	CE1 ch0: TOP EVEN		
	CE1 ch1: TOP ODD	CE1 ch1: TOP ODD		

Note: * TOP/BOT is to be set for the field picture according to respective parity bit.

Table 27.34 Motion Vector Channel Setting Examples(Encode)

	current Frame Pic		Current Field Pic(Top) *	
	read	**write**	**read**	**write**
col frame Pic	CE0 ch0: BOT EVEN	CE0 ch0: TOP EVEN	CE0 ch0: FTOP ODD	CE0 ch0: TOP ODD
	CE0 ch1: BOT ODD	CE0 ch1: TOP ODD	CE0 ch1: BOT ODD	CE1 ch0: TOP EVEN
	CE1 ch0: TOPEVEN	CE1 ch0: BOT EVEN	CE1 ch0: TOP EVEN	
	CE1 ch1: TOP ODD	CE1 ch1: BOT ODD	CE1 ch1: BOT EVEN	
col Field Pic(Tpo) *	CE0 ch0: TOP EVEN	CE0 ch0: TOP EVEN	CE0 ch0: TOP ODD	CE0 ch0: TOP ODD
	CE0 ch1: TOP ODD	CE0 ch1: TOP ODD	CE1 ch0: TOP EVEN	CE1 ch0: TOP EVEN
	CE1 ch0: TOP EVEN	CE1 ch0: BOT EVEN		
	CE1 ch1: TOP ODD	CE1 ch1: BOT ODD		

Note: * TOP/BOT is to be set for the field picture according to respective parity bit.

Below are examples of address settings for motion vectors for H.264 encoding.

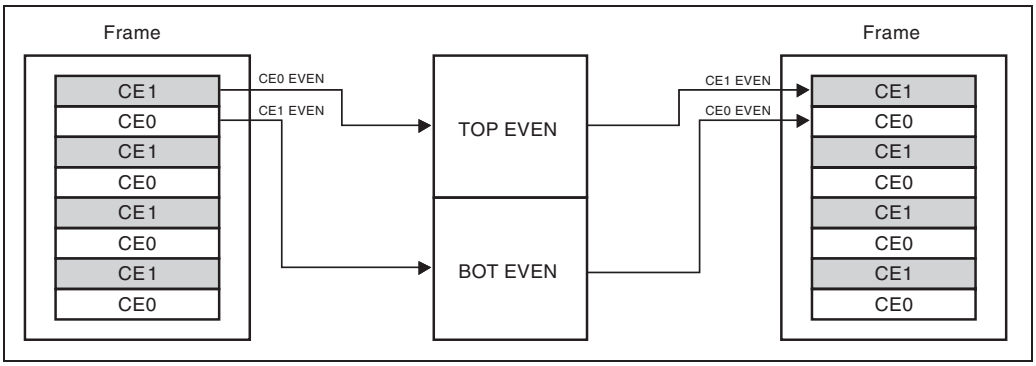


Figure 27.12 Examples of Motion Vector Settings (Current Picture: Frame, Anchor Picture: Frame)

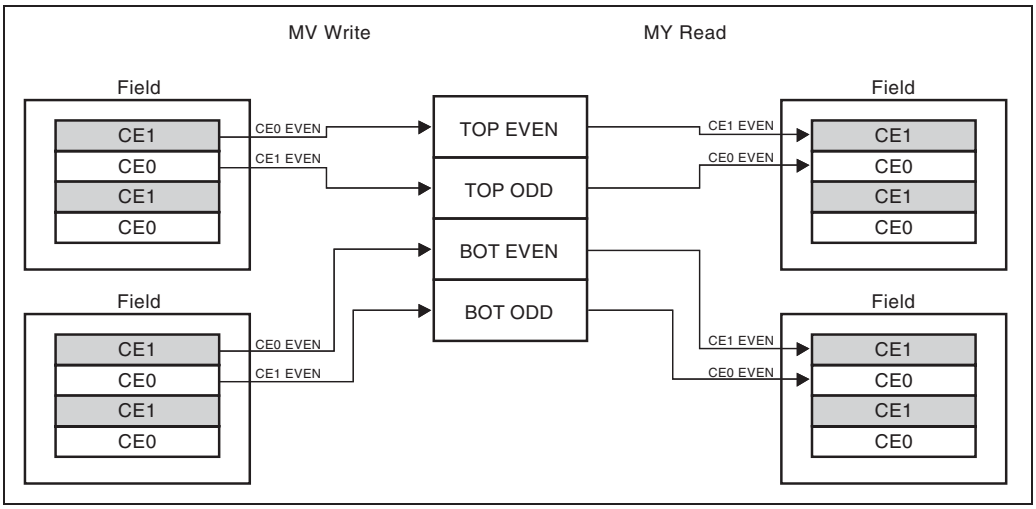


Figure 27.13 Examples of Motion Vector Settings (Current Picture: Field, Anchor Picture: Field)

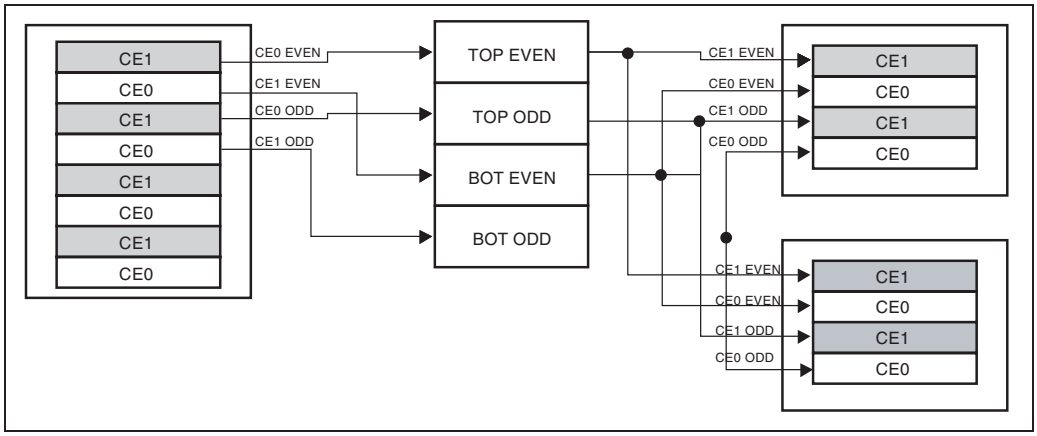


Figure 27.14 Examples of Motion Vector Settings (Current Picture: Field, Anchor Picture: Frame)

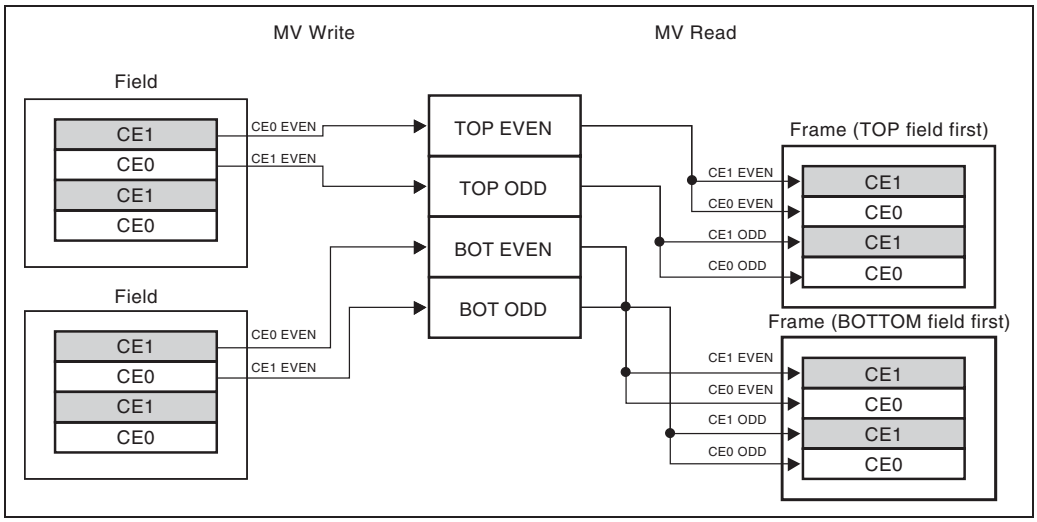


Figure 27.15 Examples of Motion Vector Settings (Current Picture: Frame, Anchor Picture: Field)

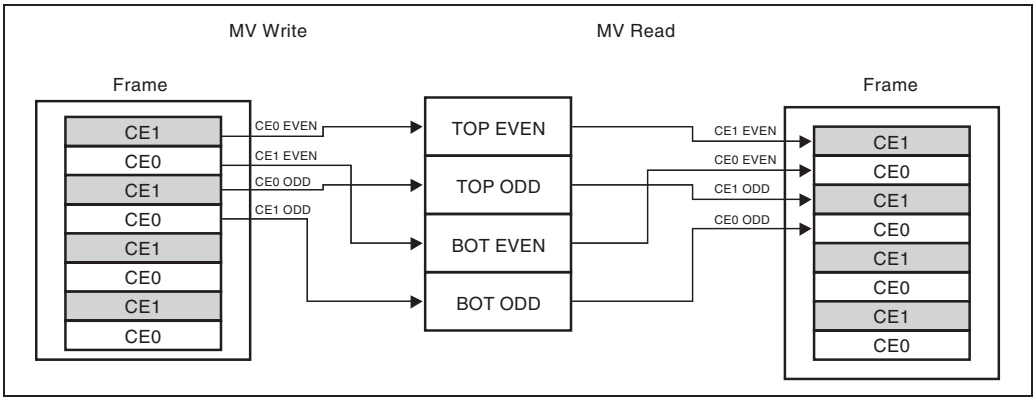


Figure 27.16 Examples of Motion Vector Settings (Current Picture: Frame, Anchor Picture: Frame (frame_mbs_only_flag = 0))

For H.264 decoding, a 32-bit motion vector for each submacroblock and a 64-byte motion vector (16 vectors) for each macroblock are output. For H.264 encoding, a 32-bit motion vector for each 8 × 8 block and a 16-byte motion vector (four vectors) for each macroblock are output.

Figure 27.10 shows the format of one motion vector for H.264/MPEG-2/VC-1 and figure 27.11 shows also the format of one motion vector for MPEG-4/H.263.

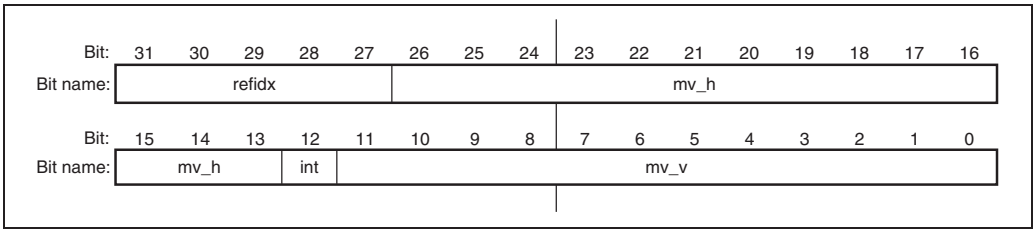


Figure 27.17 Motion Vector format (H.264/MPEG-2/VC-1)

Bit	Bit Name	Description
31 to 27	ref_idx	ref_idx 0: Indicates ref_idx
26 to 13	mv_h	Horizontal Motion Vector 0: Horizontal motion vector (1/4 pixel accuracy)
12	int	Intra/Inter Flag 0: Inter MB encoding 1: Intra MB encoding
11 to 0	mv_v	Vertical Motion Vector 0: Vertical motion vector (1/4 pixel accuracy)

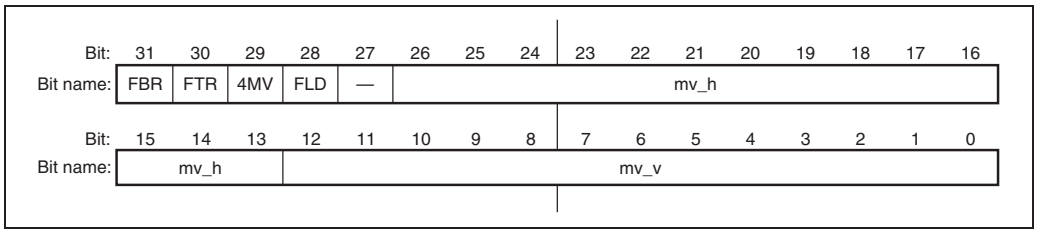


Figure 27.18 Motion Vector format (MPEG-4/H.263)

Bit	Bit Name	Description
31	FBR	forward_bottom_field_reference 0: forward_bottom_field_reference value (refer to FWD-bot MV 0:Top, 1:Bottom)
30	FTR	forward_top_field_reference 0: forward_top_field_reference value (refer to FWD-bot MV 0:Top, 1:Bottom)
29	4MV	4MV 0: 1MV MB 1: 4MV MB
28	FLD	FLD 0: Frame MB 1: Field MB
27	—	reserved
26 to 13	mv_h	Horizontal Motion Vector（-8,192 to 8,191） Horizontal motion vector (1/4 pixel accuracy)
12 to 0	mv_v	Vertical Motion Vector（-4,096 to 4,095） Vertical motion vector (1/4 pixel accuracy)

In the VPU5HG, one CE outputs a motion vector for odd-numbered macroblock lines and the other CE a motion vector for even-numbered macroblock lines. Figure 27.12 shows the motion vector format.

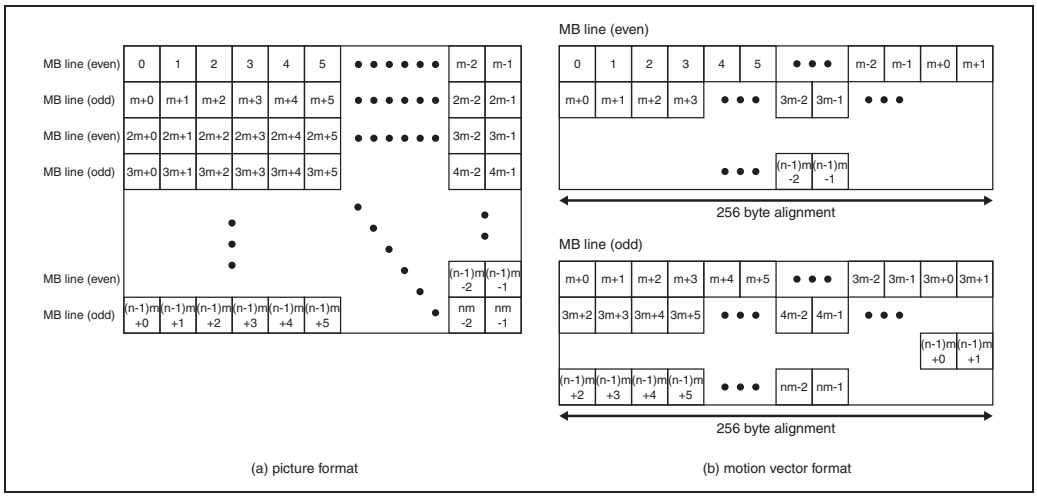


Figure 27.19 Motion Vector Format

37.5.9 Data Partition

If the coding tool data partition is used to improve error durability during MPEG-4 decoding, an area is required to store information on the data partition. The VPU5 accesses this information to reorder encoding data.

The required size for the area is (48 bytes × number of macroblocks + { 8 bytes).Secure a buffer area that accommodates this data size in 256-byte units, aligning to a 32-byte boundary.

37.5.10 Colocation Not Coded Information

When the VLCS processes a sequence including a B-VOP in MPEG-4 decoding, an area for storing the colocation not coded information is needed. The VPU5 outputs information to the area when decoding a P-VOP and inputs information from the area when decoding a B-VOP. An area of ((number of macroblocks + 63) / 64) × 64 bits is required. The buffer area that can contain this size of data should be aligned on a 32-byte boundary and established in 256-byte units.

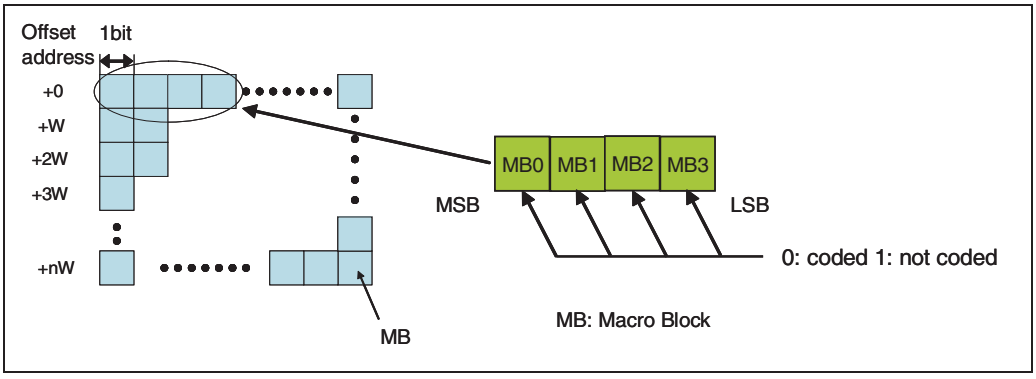


Figure 27.20 Colocation Not Coded Information Format

37.5.11 Bit Plane

A bit plane is required when starting the VLCS for decoding. Its contents are input for decoding by the VLCS. It includes control parameters for each slice.

The size of a bit plane depends on the picture size. Before starting the VLCS, establish a data area for four bits/macroblock.

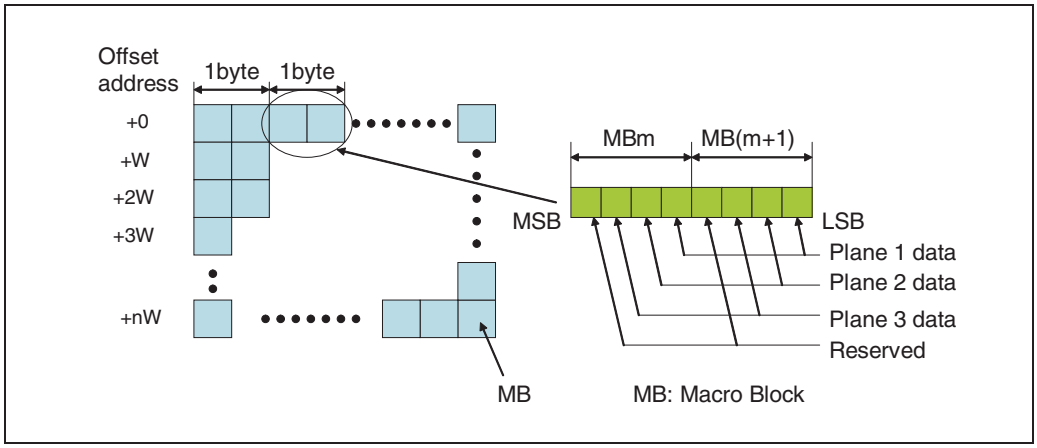


Figure 27.21 4 Bit Plan Data Format

Table 27.35 Relation between the Picture Types in VC-1 and Parameters in a Bit Plane

Picture Type (w/ Profile Name)	ACPRED	OVERFLAGS	MVTYPEMB	SKIPMB	DIRECTMB	FIELDTX	FORWARDMB
Progressive I Simple/Main							
Progressive BI Main							
Progressive I&BI Advanced	o1	o2					
Progressive P Simple/Main			o2	o1			
Progressive P Advanced			o2	o1			
Progressive B Main				o1	o2		
Progressive B Advanced				o1	o2		
Progressive Skipped Advanced							
Frame Interlace I&BI	o1	o2				o3	
Frame Interlace P				o1			
Frame Interlace B				o1	o2		
Field I & BI	o1	o2					
Field P							

Note: The number which follows a white circle indicates the number of a storage position in a bit plane.

37.5.12 MapColToList Information

BPDPREn in the VP5_VLC_MODE (VLCS mode register) is set to 1; that is, when MapColToList is processed in MB line units or MB units. The required area size is size S (bytes) shown in the following × (number of MB lines or MBs). Size S is determined by whether conditions MbAffFlag == 1 and anchor picture = field picture are satisfied.

Note that when MapColToList data is provided for each MB or MB line, an intermediate stream of up to 7,104 bits is added to that MB or MB line. If, for example, MapColToList data is provided for each MB line for a stream produced at 1,920 × 1,080 resolution, up to 68 × 7,104 = 483,072 bits are added for each frame.

Table 27.36 Relationship between Picture Types and Bit Plane Parameters for VC-1 Processing

Number of Reference Frames (num_ref_frames)	MbAffFlag == 1and Anchor Picture = Field Picture	Size S (Bytes)
13 or more	Satisfied	128
13 or more	Not satisfied	64
9 or more	Satisfied	96
9 or more	Not satisfied	48
5 or more	Satisfied	64
5 or more	Not satisfied	32
4 or less	Satisfied	32
4 or less	Not satisfied	16

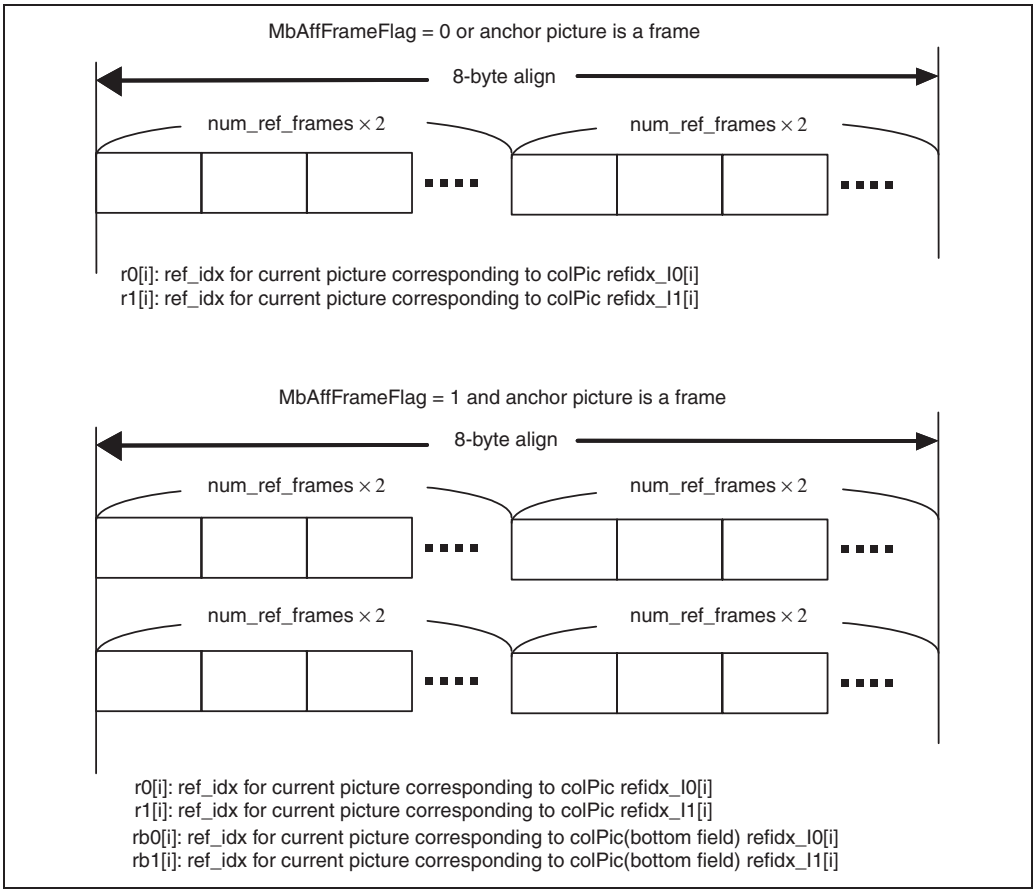


Figure 27.22 MapColToList Format for Each MB or MB Line

37.6 Operational Description

37.6.1 Overview

The VPU5HG is 1-way CODEC hardware IP which implements H.264, MPEG-2, MPEG-4, H.263, and VC-1 encoding and decoding. This section describes the VPU5HG processing flow.

The VPU5HG consists of two modules. One is the VLC responsible for encoding and the other is the CE responsible for picture processing. The modules can operate independently of each other. The VPU5HG performs the processing for the levels shown in table 27.37. Software processing is required for the higher levels.

Table 27.37 VPU5HG Processing Range

Standard	Processing	Encoding	Decoding
H.264	SPS(Sequence Parameter Set)	—	—
	PPS(Picture Parameter Set)	—	—
	SEI(Supplemental Enhancement Information)	—	—
	Access Unit Delimiter	—	—
	End of Sequence	—	—
	End of Stream	—	—
	Filler Data	—	—
	Slice Header	√	—
	Slice Data	√	√
	Macroblock	√	√
	Sub-macroblock	√	√
	Block	√	√
MPEG-4	VOS(Visual Object Sequence)	—	—
H.263	VO(Visual Object)	—	—
	VOL(Video Object Layer)	—	—
	GOV(Group of Video Object Plane)	—	—
	VOP(Video Object Plane)	—	—
	Video Packet / GOB	√	√
	Macroblock	√	√
	Block	√	√

Standard	Processing	Encoding	Decoding
MPEG-2	Sequence Header	—	—
	Extension and User Data	—	—
	Extension Data	—	—
	User Data	—	—
	Sequence Extension	—	—
	Sequence Display Extension	—	—
	Group of Pictures Header	—	—
	Picture Header	—	—
	Picture Coding Extension	—	—
	Quant Matrix Extension	—	—
	Picture Display Extension	—	—
	Copyright Extension	—	—
	Slice	√	√
	Macroblock	√	√
	Block	√	√
VC-1	Sequence Layer	—	—
	Entry-Point Layer	—	—
	Picture Layer	—	—
	Slice Layer	—	—
	Macroblock	—	√
	Block	—	√

Legend: √: Possible to process
—: Not possible to process

37.6.2 VPU5HG Operation Control Setting

To control the VPU5HG operation, it is necessary to combine setting methods shown in table 27.38.

Table 27.38 VPU5HG Operation Setting Methods

No.	Setting method	Description
(1)	Register	The VPU5HG operation control is specified in the register mapped to the host space. This register includes the system settings.
(2)	Initialization routine	Stores into external RAM both the firmware for operating the TRF, FME and DEB, which use the STX and PIPE architectures in the VLCS, and control information from a layer above the picture layer according to the video encoding scheme. After the VPU5HG is activated, it executes the initialization routine. Processing starts when the settings in the external RAM are already downloaded into the internal RAM or register in the VPU5HG. The data format for the initialization routine contains 128-bit data which is a combination of VPU5HG internal space address and data shown in figure 27.23.
(3)	Command stream	The external RAM stores control information included in the slice header for H.264 decoding. After the VPU5HG is activated, the VLCS reads that information from the external RAM for decoding of each slice. Figure 27.24 shows the data format for command streams.

(1) Registers

Necessary data is set in the VPU5HG register mapped to the host space. The VPU5HG register contents can only be accessed as long words (each consisting of 32 bits). Table 27.6 shows the VPU5HG registers.

The VPU5HG registers contain system settings. Information about the operating status and processing results for each process is available from the status register.

(2) Initialization Routine

The setting method which uses the initialization routine involves storing the VPU5HG control parameters into the external RAM.

The setting parameters for the initialization routine excluding the STX and PIPE microcode are called the initialization routine parameters. Their format is shown in figure 27.23.

Figure 27.23 shows the storage format for 32-bit external RAM. Each packet contains a multiple of four words (128 bits). One packet corresponds to one internal register (64 bits). The first one word contains: the VPU address [21:17] of a register shown in section 27.3, Internal Register Descriptions; mask bits for broadcasting (EMASK: H'0 unless otherwise specified) and transfer direction bits (D = 1: Counterclockwise rotation). RSVD is a reserved area which should be set to 0. The second word contains the VPU address [16:0] of a register shown in section 27.3, Internal Register Descriptions. Because the register data length specified by the initialization routine is 64 bits, the low-order three bits (TRM) for the address specified in the second word are always 0. The subsequent two words (64 bits) specify the actual data to be stored. The packets should be in consecutive addresses.

The last packet (end packet) for the initialization routine parameters is VPU address H'0000 1007 (set by DMAC channel 1) or VPU address H'0020 1007 (set by DMAC channel 0). Select 0 for the DATA field. Select 1 for resuming the operation. Tables 27.5 and 27.6 show the internal registers to be set for the initialization routine.

For encoding which involves one CE, only the internal registers of CE0 are used. Select 1 for the DATA field for CE0’s end packet. There is no need to specify the initialization parameters for CE1.

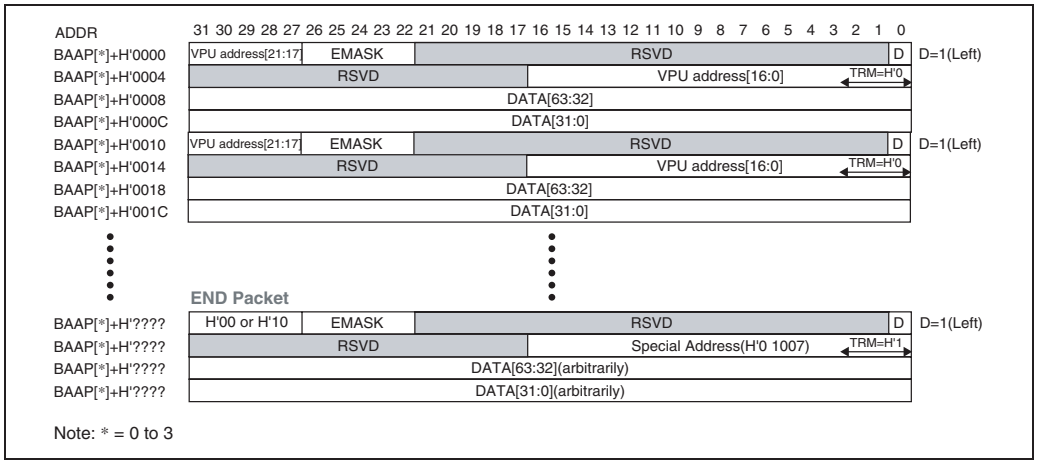


Figure 27.23 Initialization Routine Parameter Format

(3) Command Stream

A command stream is intended to automatically specify the slice setting parameters in the VLCS when starting the slice processing. This stream is available for decoding. If a command stream is enabled, the VLCS reads the stream by using the GDMAC automatic mode when starting the slice processing. Then, it sets the basic parameters for the slice and transfers additional data to the STX data memory.

Note: A command stream containing one frame of slice information should be stored in the external RAM before the VLCS is activated.

A command stream consist of a command header and subsequent data areas required. Figure 27.17 shows the command header configuration. Two or more commands can be given for each slice. The boundary bit (B bit) in the command header in the last command for each slice should be set to 1. The command is prefetched to reduce the overhead involved in reading the command stream on the slice boundary. However, the command capacity should be 128 bytes or less per slice due to the prefetch buffer size. If the command capacity exceeds that limit, the command stream read time cannot be decreased and the performance might be degraded.

One command of command type 0 is always required for each slice. This command should specify the stream start position and start macroblock address. This command should be the first to be specified for each slice. This command contains: the E bit which indicates the last slice to be processed; the S bit which indicates that the slice-level parameter is abbreviated; the I bit which indicates the initial processing of the picture is required; and the T bit which indicates the final processing of the picture is required.

If the E bit is 1, the next slices are not processed. The VLCS processing terminates after the current slice is processed.

If the S bit is 1, the same slice parameter as that for the previous slice is used for addresses other than the macroblock address or stream start address. If any of the parameters excluding this bit are changed, all the slice parameters should be specified.

If the I bit is 1, the current macroblock address is initialized to the address specified in command type 0. The slices are processed in the order of the scanned macroblocks. This bit is set to 0 when an error macroblock is inserted if an absent macroblock is detected. The VLCS manages the position of the currently processed macroblock. If the I bit is 0 and if the macroblock position at the beginning of the slice (i.e., the macroblock address specified in command type 0) differs from the currently processed macroblock position, then an error macroblock is inserted, thereby advancing the current macroblock position to the beginning of the slice.

If the T bit is 1, the VLCS inserts error macroblocks into slices ending with the last one in the picture after the completion of the current slice processing. Typically, this bit is specified for the last slice in the picture.

Table 27.39 shows the functions of the E, S, I and T bits. Table 27.40 shows the normal settings. Use the settings shown in table 27.39 for the VPU5HG.

Table 27.39 Functions of the Operation Control Bits of Command Type 0

Bit name	Function	Description
E	Specification of the last command	0: Does nothing. 1: Terminates the VLCS operation after slice processing.
S	Specification of the use of the same slice parameter	0: Uses the newly specified slice parameter. 1: Uses the same slice parameter as that for the previous slice. (This value should not be selected for the VPU5HG.)
I	Forced specification of the macroblock address	0: Processes the slices after inserting error conceal MBs in the positions between the last MB in the previous slice and the first MB in the current slice. 1: Does nothing. Performs processing after a seek to the start MB address in the slice. (This value should not be selected for the VPU5HG.)
T	Specification of insertion of error macroblocks in MBs ending with the lower right one	0: Does nothing. 1: Inserts error conceal MBs in the positions ending with the lower right one in the picture after slice processing. (This value should be the same as that for the E bit for the VPU5HG.)

Table 27.40 Normal Settings for the Control Bits of Command Type 0

	Bit status			
Slice position	**E**	**S**	**I**	**T**
First slice in the picture	0	0	0	0
Last slice in the picture	1	0	0	1
First and last slices in the picture	1	0	0	1
Other slices	0	0	0	0

Command type 8 is specified after command type 0. Command type 8 is used to specify the stream buffer size and initial buffer offset. The stream buffer size can be specified in units of 256 bytes, and thus the low-order eight bits should always be set to 0. The initial buffer offset can be specified in units of eight bytes, and thus the low-order three bits should always be set to 0. A stream is read starting at a position determined by the specified initial offset. If the VLCS has read an amount of data equal to the specified buffer size, it stops reading the stream. Then, an error is reported via the VP5_VLC_ERRH and VP5_VLC_ERRL registers. The initial offset should be less than the specified buffer size. If interrupts for the stream channel are enabled by the VP5_INT_ENB register settings, the VLCS stops its operation and generates an interrupt which results in continuing the operation.

DMA prefetch occurs when a stream or other data is read. Thus, extra data is read. (This extra data is not processed.)

If the buffer size is infinite, command type 8 can be omitted. However, it should be specified when control such as continuation with the stream buffer size is required. When specifying command type 8 is necessary, it should always be specified for all slices.

Command type 16 is used for storing a set of data in consecutive areas. It should be stored in units of 64 bits. The low-order three bits for the start address should always be 0. The number of 64-bit words should be specified in Length. For command type 16, the command header is followed by a data row with a length equal to the number of 64-bit words specified in Length. Specify 1 in Length when data in one position is to be changed. If the size of stored data is one word, Length should be 1.

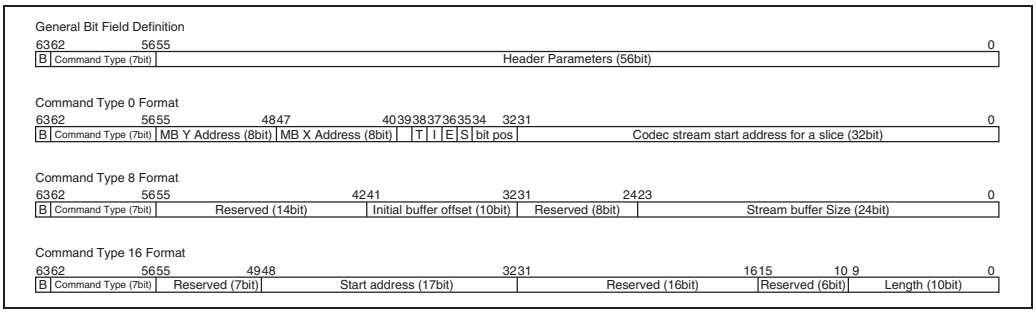


Figure 27.24 Command Header Format

Figure 27.25 shows the overall configuration of a command stream. This stream contains a series of parameters for each slice in a single picture. There are three command headers for each slice: the first of type 0, the second of type 8 and the third of type 16. The command header of type 16 is followed by parameters to be stored in addresses specified in that header. For details about these parameters, refer to the description of the command stream parameters in section 28.4, Command Stream Parameter Descriptions. The command header of type 16 is optional. Usually, one command header of type 16 is required for each slice. Two or more command headers of type 16 can be provided for each slice. The B bit in the last command header for each slice should always be set to 1. By this setting, the VPU5HG VLCS can identify the separation between slices.

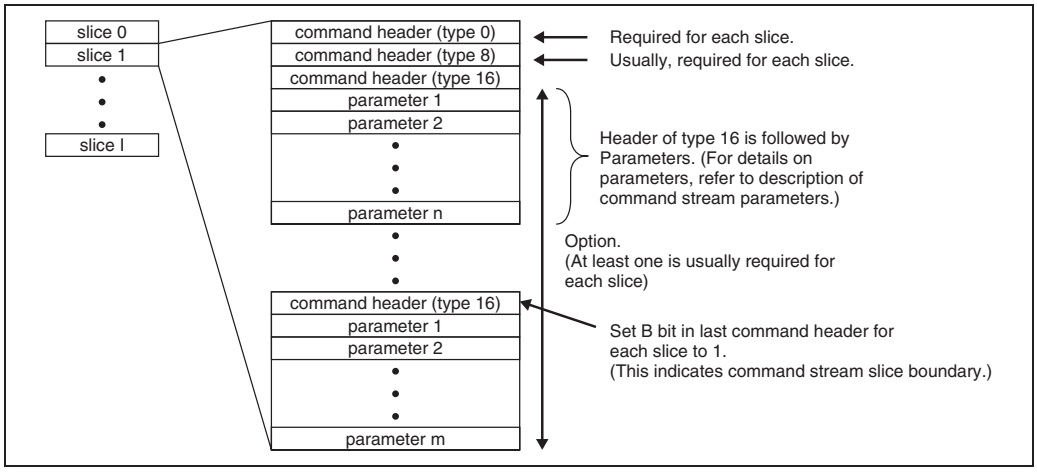


Figure 27.25 Command Stream Configuration

Described below is the stream start position specified in a command stream of type 0. Also described are the related parameters for decoding. These descriptions are based on figure 27.26.

In a command stream of type 0, specify the stream start address as an address of the byte including the start bit for slice data. This address should be Sadr shown in the figure. For bit pos, specify the position of the start bit for slice data. This position should be Sbitpos shown in the figure. Specify the horizontal MB position and vertical MB position for MB X addr and MB Y addr, respectively.

To obtain entirely concealed pictures, set both MB X addr and MB Y addr to 255 for the first slice of each picture. For processing non-H.264 content, set both the E and T bits to 1 at this time so each picture can be processed as one slice. For processing H.264 content, each picture is processed as two irregular slices. Set the E and T bits to 0 for the first slice and set both of them to 1 for the second slice. Except for the values of the E and T bits, all the settings for the second slice should be the same as those for the first slice.

If there is an error in H.264 multi-slice encoding/decoding, make settings as follows.

If the first slice or an intermeidate slice in the frame is missing, set the command stream for the normal slices only. The hardware's concealment feature conceals the starved area. If the last slice in the frame is missing, set the command stream for the last-but-one normal slice. At this time, be sure to set both the E and T bits to 1.

The skip bit in word 1 for the command stream parameter should always be 0. For slice_size, specify the number of bytes between the align address (= AAdr) and end address (= EAdr). If the

system does not wrap around memory addresses for continuing operation, slice_size = EAdr - AAdr +1. Be sure to select 0 when concealing the entire picture for processing non-H.264 content.

Calculate AAdr as follows.

AAdr = SAdr&~H'1F (32-byte align mode (established by setting BAAlign = 1 for VP5_VLCS_MODE))

Using figure 27.27, the following describes the parameters which can be specified for command streams of type 8. Use type 8 for specifying the stream buffer area. If data outside of this area are accessed, the VLCS stops reading from the memory and behaves the same way as it does when internally reading data 0.

Use the Stream Buffer Size parameter to specify the buffer area size in units of 256 bytes. The low-order eight bits should always be 0. Be sure to select 0 when concealing the entire picture for processing non-H.264 content.

Use the Stream Buffer Size parameter to specify the buffer area size in units of 256 bytes. The low-order eight bits should always be 0.

Use the Initial Buffer Offset parameter to specify the number of bytes from the beginning of the buffer whose size is in 256-byte units to the align address (= AAdr). This number is a multiple of eight bytes, and thus the low-order three bits should always be 0. This number should always be smaller than the Stream Buffer Size parameter. The VLCS reads from a memory address which is the number of bytes specified in the Initial Buffer Offset parameter away from the align address. Thus, the buffer area can be correctly specified in the Stream Buffer Size parameter by properly setting the Initial Buffer Offset parameter.

The beginning of the buffer whose size is in 256-byte units should be aligned on a 32-byte boundary. The VLCS does not read from the area which follows the stream buffer. However, note that DMA prefetch results in reading extra data. The total amount of such extra data in the overall VPU5HG configuration is equal to the DMA buffer size (512 bytes for the VPU5HG).

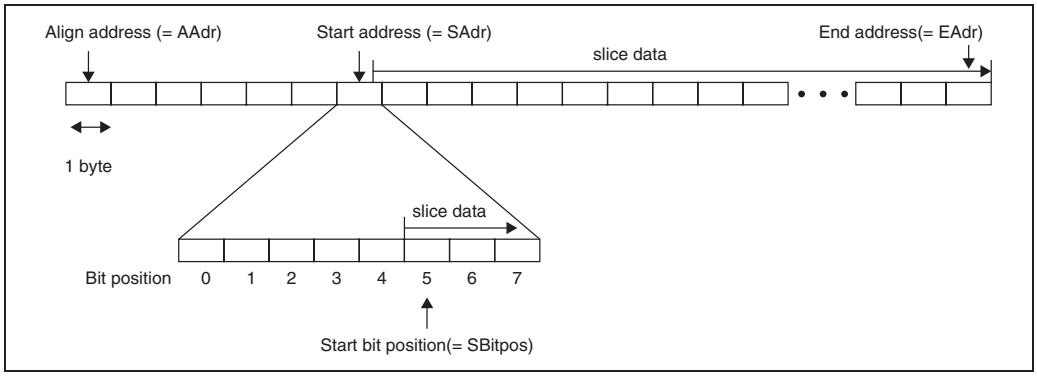


Figure 27.26 Parameters for Specifying a Stream Address for Decoding

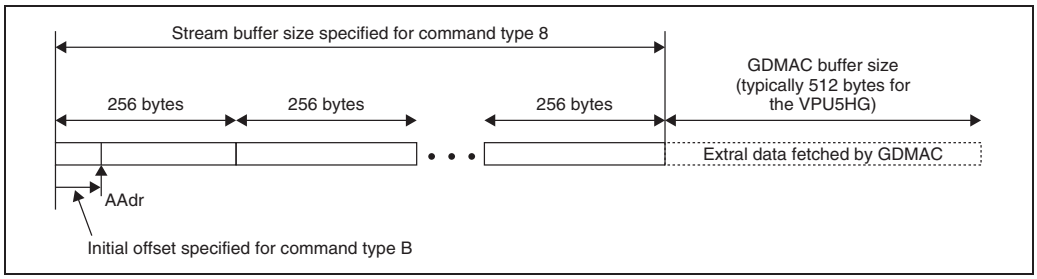


Figure 27.27 Parameters Specified for a Command Stream of Type 8

37.6.3 Encoding

(1) Encoding

The VPU5HG encoding process is divided into two stages. In the first stage, the CE encodes picture data into intermediate data. In the second stage, the VLCS converts the input into variable-length data. First, the CE is activated to perform intra/inter prediction, frequency conversion, etc., thereby converting data into intermediate data. Then, the VLCS is activated to convert the intermediate data into a variable-length encoded bit stream. The CE and VLCS encode data in picture units. A termination interrupt can be output to provide notification when each module terminates its processing.

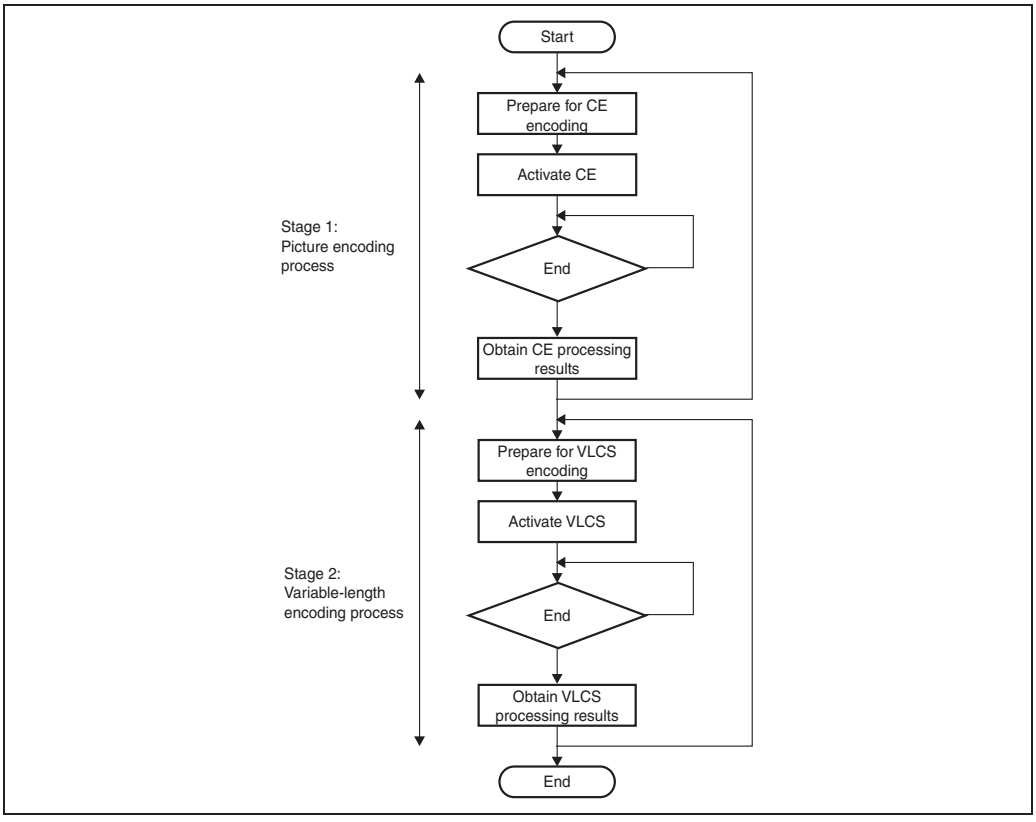


Figure 27.28 Overview of the Encoding Process Flow

(2) Picture Encoding by CE Activation

Encode pictures, reference pictures and encoding control parameters are input for VPU5HG picture encoding by CE activation (stage 1). After this encoding, an intermediate stream and intermediate control stream are output. The CE encodes data in picture units. A termination interrupt can be output to provide notification when the CE terminates its processing.

To encode picture data by CE activation, first set the sequence-level control parameters, picture-level control parameters and encoding mode by using software. Table 27.41 shows the input parameters and data required for this encoding. It also shows the setting methods for the VPU5HG. Table 27.42 shows the output parameters and data for the CE as well as output destinations. The software obtains the control parameters for variable-length encoding (stage 2) by VLCS activation and those for picture encoding (stage 1) by CE activation for the next picture.

Table 27.41 Input Parameters and Data for the CE

Item	Setting method	Description
System settings	Register	Settings for system control of the interrupt, etc., and for execution of the initialization routine
Microcode	Initialization routine	CE microcode
CE operation setting parameter	Initialization routine	Picture-level control parameter and GDMAC settings
Reference picture	External RAM	Reference picture (other than I picture)
Encode picture	External RAM	Picture to be encoded

Table 27.42 Output Parameters and Data for the CE

Item	Output destination	Description
System status	Register	Operation status
Picture status	Register	Encoding result status
Reference picture	External RAM	Reference picture for next-picture encoding
MV information	External RAM	Motion vector information
Intermediate stream	External RAM	Intermediate data stream. (Output for each CE.)
Intermediate control stream	External RAM	Control information required for VLCS processing. (Output for each CE.)

Figure 27.22 shows the software for picture data encoding by CE activation. It also shows the VPU5HG operation flow.

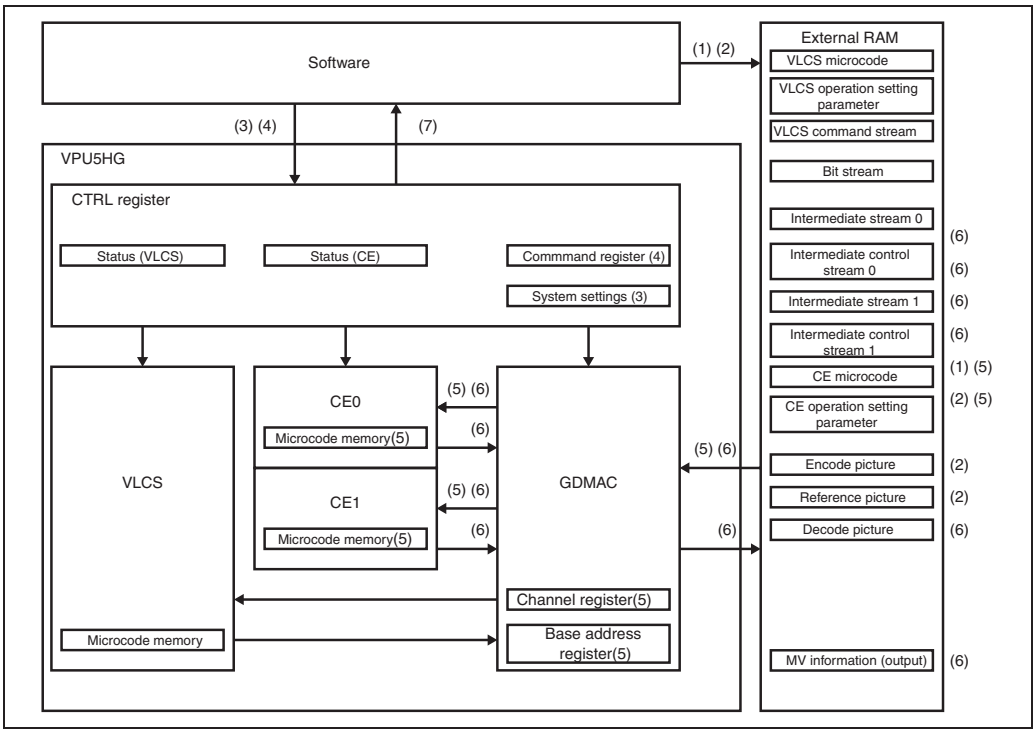


Figure 27.29 Conceptual Diagram of the Software for Picture Encoding and the CE Operation Flow

No.	Encoding Sequence by the CE
(1)	Store predetermined microcode into the external RAM. This code complies with the encoding standard.
(2)	The software stores the encode picture, reference picture, reference picture motion vector and CE operation setting parameters into the external RAM for picture data encoding.
(3)	The software sets the VPU5HG registers for system control and initialization routine execution.
(4)	The software activates the CE by writing 1 to the VPU5HG VP5_CMD register.
(5)	The VPU5HG executes the initialization routine according to the system settings. This routine first downloads the microcode into the microcode memory in the CE. Then, it transfers the CE operation setting parameters to predetermined registers/RAM in the CE and GDMAC.
(6)	After the initialization routine execution, the CE reads the MB-level encoding control parameters, encode picture and reference picture from the external RAM. Then, the it performs the encoding process which includes motion vector detection, frequency conversion, quantization and coefficient prediction. Finally, it outputs an intermediate stream and intermediate control stream. At the same time, it outputs MB and MV information. It may also output MB and MV information to the external RAM depending on the settings.
(7)	After the CE processing, the software checks the encoding result status.

(3) Variable-Length Encoding by VLCS Activation

The intermediate stream is input for VPU5HG variable-length encoding by VLCS activation (stage 2). After this encoding, an encoded bit stream is output. The VLCS encodes data in picture units. A termination interrupt can be output to provide notification when the VLCS terminates its processing.

When encoding involves the use of the VLCS, the software performs encoding above the picture level. After the last data and offset are set as the header information created by the software, the VLCS creates a bit stream which follows the header.

Table 27.44 shows the input parameters and data required for variable-length encoding by VLCS activation. It also shows the setting methods for the VPU5HG. The inputs to the VLCS for encoding are system control information, microcode, picture parameters, GDMAC settings, intermediate streams and intermediate control streams. The picture parameters should be set to the same values as those for CE activation in stage 1. Table 27.45 shows the output parameters and data for the VLCS as well as the output destinations.

Table 27.43 Layers for Bitstream Creation by Hardware

Stream Type(w/ Profile Name)	Layer
MPEG-4	Video packet header or motion shape texture and lower
H.264	Slice data and lower
H.263	gob_layer and lower
MPEG-2	picture_data and lower
MPEG-1	picture_data and lower

Table 27.44 Input Parameters and Data for the VLCS

Item	Setting method	Description
System settings	Register	Settings for system control for interrupts, etc., and for execution of the initialization routine
Microcode	Initialization routine	STX microcode
Operation setting parameter	Initialization routine	Picture-level control parameters and GDMAC settings
Intermediate stream	External RAM	Intermediate data stream (required for each CE)
Intermediate control stream	External RAM	VLCS processing control information (required for each CE)

Table 27.45 Output Parameters and Data for the VLCS

Item	Output destination	Description
System status	Register	Operation status
Picture status	Register	Encoding result status
Bit stream	External RAM	Encoded bit stream

Figure 27.30 shows the software for variable-length encoding by VLCS activation. It also shows the VPU5HG operation flow.

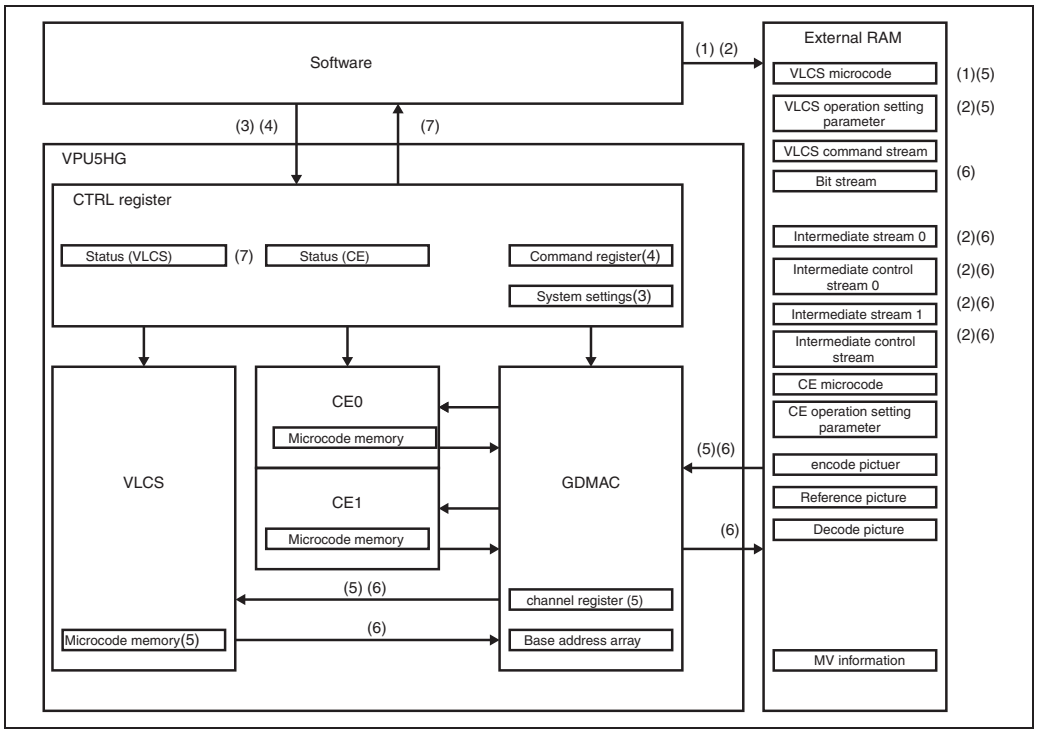


Figure 27.30 Conceptual Diagram of the Software for Variable-Length Encoding and the VLCS Operation Flow

No.	Encoding Sequence by the VLCS
(1)	The software stores predetermined microcode into the external RAM. This code complies with the encoding standard.
(2)	The software stores the VLCS operation setting parameters, intermediate stream and intermediate control stream into the external RAM.
(3)	The software sets the VPU5HG registers for system control and initialization routine execution.
(4)	The software activates the VLCS by writing 1 to VPU5HG VP5_CMD register.
(5)	The VPU5HG executes the initialization routine according to the system settings. This routine first downloads the microcode into the microcode memory in the VLCS. Then, it transfers the VLCS operation setting parameters to predetermined registers/RAM in the VLCS and GDMAC.
(6)	After the initialization routine execution, the VLCS performs variable-length encoding while at the same time reading the intermediate stream and intermediate control stream from the external RAM. The VLCS outputs a bits stream by variable-length encoding.
(7)	After the VLCS processing, the software checks the variable-length encoding result status.

(4) H.264 Encoding Procedures (720 Pixels × 480 Lines Progressive Sequence)

The following describes the steps for H.264 encoding. The examples below assume that the intermediate streams and intermediate control streams are configured with a double buffer. The SDRAM stored data and parameter settings are represented in big endian form. The endian settings for each DMAC channel register and those for VP5_CTRL are 0.

(a) Encoding by the CE (First I Picture)

1. Store the microcode into the external memory. Its base address is H'1000 0000 (set in VP5_CE_MBA) for this example.
2. Create CE0 operation control parameters and store them into the external memory. Their base address is H'1021 0000 (set in VP5_CE_PBA0) for this example.

Table 27.46 Sample CE0 Operation Control Parameters for 720 × 480 I Picture Encoding

Settings																Description
50	00	00	01	00	00	40	40	12	a2	00	00	00	00	00	00	VP5_BAAR0 decode picture luminance base address
50	00	00	01	00	00	40	48	12	aa	00	00	00	00	00	00	VP5_BAAR0 decode picture chrominance base address
50	00	00	01	00	00	40	90	13	db	d3	00	00	00	00	00	VP5_BAAR0 MV information base address
50	00	00	01	00	00	40	b0	13	b7	4f	00	00	00	00	00	VP5_BAAR0 intermediate stream base address
50	00	00	01	00	00	40	b8	13	d5	d5	00	00	00	00	00	VP5_BAAR0 intermediate control stream base address
50	00	00	01	00	00	42	00	12	a2	00	00	00	00	00	00	VP5_BAAR0 reference picture luminance address 0
50	00	00	01	00	00	42	08	12	aa	00	00	00	00	00	00	VP5_BAAR0 reference picture chrominance address 0
50	00	00	01	00	00	00	40	d0	00	00	80	00	00	08	08	VP5_CE_DCHR_DECY0 decode luminance picture DMA channel register 0
50	00	00	01	00	00	00	48	d0	00	00	80	00	00	08	09	VP5_CE_DCHR_DECC0 decode chrominance picture DMA channel register 0
50	00	00	01	00	00	00	60	b0	00	00	80	00	00	02	00	VP5_CE_DCHR_REF reference picture DMA channel register
50	00	00	01	00	00	00	90	c0	00	00	00	00	00	0c	12	VP5_CE_DCHR_MVINFO0 MV information stream DMA channel register 0
50	00	00	01	00	00	00	b0	c0	00	00	00	00	00	10	16	VP5_CE_DCHR_CEIS0 CE intermediate stream DMA channel register 0
50	00	00	01	00	00	00	b8	c0	00	00	00	00	00	10	17	VP5_CE_DCHR_CEIC0 CE intermediate control stream DMA channel register 0
50	00	00	01	00	00	10	38	00	00	00	80	00	00	00	00	VP5_GDMAC_SHWARBT
00	00	00	01	00	00	00	00	00	00	01	42	2d	00	1e	00	VP5_CE_SPAR
00	00	00	01	00	00	00	08	00	00	00	00	00	00	00	00	VP5_CE_PPAR
00	00	00	01	00	00	00	50	01	01	01	01	01	01	00	00	VP5_CE_ENC_WPRED
00	00	00	01	00	00	00	58	00	ff	1f	40	00	00	b0	40	VP5_CE_ENC_CTRL
00	00	00	01	00	00	00	60	22	1a	00	28	00	3c	00	14	VP5_CE_ACQ_CTRL
00	00	00	01	00	00	00	68	00	1a	20	26	2c	31	80	40	VP5_CE_ME_COST
00	00	00	01	00	00	00	a0	00	00	00	00	1e	00	1e	02	VP5_CE_VLCF
00	00	00	01	00	00	00	a8	00	00	00	00	00	00	00	00	VP5_CE_SLC_SIZE
00	00	00	01	00	00	00	b0	00	00	05	46	ff	ff	00	01	VP5_CE_TBIT
00	00	00	01	00	00	00	b8	00	00	85	55	00	00	00	00	VP5_CE_RCDJ
48	00	00	01	00	00	04	40	00	00	00	00	00	1e	86	00	VP5_CE_IS_BS0 CE intermediate stream 0 buffer size register
80	00	00	01	00	00	10	07	00	00	00	00	00	00	00	00	Last packet for the initialization routine

Specify the base addresses in VP5_BAAR0. Set the DMA channel registers for encoding. With hsize in the decode picture and reference picture DMA channel registers, specify 1024/8 which is greater than a horizontal picture size of 720. Set VP5_GDMAC_ARDPR1 and VP5_GDMAC_SHWARBT when starting the CE for the first I picture. Specify num_ref_frame = 1, ce = 1, dec_out_disable = 0, stream_type = 2(H.264), mb_width = H2D (= 720/16) and mb_height = H'1E (= 480/16) in VP5_CE_SPAR. Specify pic_type = 0 and refidx_last0 = 0 in VP5_CE_PPAR. Specify the recommended values in VP5_CE_ENC_WPRED, VP5_CE_ENC_CTRL, VP5_CE_ACQ_CTRL and VP5_CE_ME_COST. Set H'0000 0000 in VP5_CE_FME*n*_QNC*m* and VP5_CE_TRF*n*_QNC*m* (*n* = 0, *m* = 1). Specify VPU address[21:17] = H'00 for the last packet for the CE0 initialization routine.

3. Create CE1 operation control parameters and store them into the external memory. Their base address is H'1013 6400 (set in VP5_CE_PBA1) for this example.

Table 27.47 Sample CE1 Operation Control Parameters for 720 × 480 I Picture Encoding

Setting																Description
d0	00	00	01	00	00	40	40	12	a2	00	00	00	00	00	00	VP5_BAAR1 decode picture luminance base address
d0	00	00	01	00	00	40	48	12	aa	00	00	00	00	00	00	VP5_BAAR1 decode picture chrominance base address
d0	00	00	01	00	00	40	60	12	00	00	00	00	00	00	00	VP5_BAAR1 encode picture luminance base address
d0	00	00	01	00	00	40	68	12	08	00	00	00	00	00	00	VP5_BAAR1 encode picture chrominance base address
d0	00	00	01	00	00	40	90	13	dc	d3	00	00	00	00	00	VP5_BAAR1 MV information base address
d0	00	00	01	00	00	40	b0	13	76	47	00	00	00	00	00	VP5_BAAR1 intermediate stream base address
d0	00	00	01	00	00	40	b8	13	94	cd	00	00	00	00	00	VP5_BAAR1 intermediate control stream base address
d0	00	00	01	00	00	00	40	d0	00	00	80	00	00	08	08	VP5_CE_DCHR_DECY1 decode luminance picture DMA channel register 1
d0	00	00	01	00	00	00	48	d0	00	00	80	00	00	08	09	VP5_CE_DCHR_DECC1 decode chrominance picture DMA channel register 1
d0	00	00	01	00	00	00	68	b0	00	00	80	00	00	00	00	VP5_CE_DCHR_TMP1 ENCODE PICTURE DMA channel register
d0	00	00	01	00	00	00	90	c0	00	00	00	00	00	0c	12	VP5_CE_DCHR_MVINFO1 MV information output DMA channel register 1
d0	00	00	01	00	00	00	b0	c0	00	00	00	00	00	10	16	VP5_CE_DCHR_CEIS1 CE intermediate stream DMA channel register 1
d0	00	00	01	00	00	00	b8	c0	00	00	00	00	00	10	17	VP5_CE_DCHR_CEIC1 CE intermediate control stream DMA channel register 1
c8	00	00	01	00	00	04	40	00	00	00	00	00	1e	86	00	VP5_CE_IS_BS1 CE intermediate stream 1 buffer size register
c0	00	00	01	00	00	00	50	00	00	00	04	00	00	00	00	VP5_CE_DEB_LMDMASR1 DEB1LMDMA synchronous register
00	00	00	01	00	00	10	07	00	00	00	00	00	00	00	00	Late packet for the initialization routine

Specify the base addresses in VP5_BAAR1. Set the DMA channel registers for encoding. Specify VPU address[21:17] = H'00 for the last packet for the CE1 initialization routine.

4. Make settings for system control and initialization routine activation. Then, start the CE. Below are sample register settings. Start the CE with the CME bit = 1 and the CE bit = 1 in the VP5_CTRL register.

```
register_write ( VP5_CTRL,      H'0000 00B5 ); // Overall operation settings
register_write ( VP5_IRQ_ENB,   H'0000 0101 ); // Interrupt enable
register_write ( VP5_CE_MBA,    H'1000 0000 ); // Microcode base address
register_write ( VP5_CE_PBA0,   H'1002 1000 ); // Parameter base address
register_write ( VP5_CE_PBA1,   H'1013 6400 ); // Parameter base address
register_write ( VP5_CMD,       H'0000 0001 ); // Activation
```

where arguments #0 and #1 for register_write() indicate a register name and data to be set, respectively.

5. Check the results.

The CS bit in the VP5_STATUS register indicates the VPU5HG CE is active. When it terminates its operation, this bit is set to 0 and the CE bit in the VP5_IRQ_STA register is set to 1, indicating the termination status.

After the operation, check the following status registers:

VP5_CE_ERR
VP5_CE_INT_TB0

VP5_CE_INT_TB1
VP5_CE_MB_ATTR
VP5_CE_MB_SADA
VP5_CE_MB_SADR
VP5_CE_MB_USAD
VP5_CE_ASUM
VP5_CE_ACT}
VP5_CE_QSUM
VP5_CE_DJS
VP5_CE_YSUM

(b) Encoding by the VLCS (First I Picture)

1. Store the microcode into the external memory. Its base address is H'100a 3000 (set in VP5_CE_MBA) for this example.
2. Store the microcode into the external memory. Its base address is H'100a 3000 (set in VP5_CE_MBA) for this example.

Table 27.48 Sample VLCS DMAC Channel 0 Operation Control Parameters for 720 × 480 I Picture Encoding

Setting																Description
50	00	00	01	00	00	40	c0	13	44	00	00	00	00	00	00	VP5_BAAR0 stream A base address
50	00	00	01	00	00	40	e0	13	76	47	00	00	00	00	00	VP5_BAAR0 VLCS intermediate stream base address
50	00	00	01	00	00	40	e8	13	94	cd	00	00	00	00	00	VP5_BAAR0 VLCS intermediate control stream base address
50	00	00	01	00	00	00	c0	c0	00	00	00	00	00	14	18	VP5_VLC_SCHR_STRA stream A DMA channel register
50	00	00	01	00	00	00	e0	88	a0	70	00	00	00	12	1c	VP5_VLC_DCHR_VLIS0 VLCS intermediate stream DMA channel register 0
50	00	00	01	00	00	00	e8	88	a8	70	00	00	00	12	1d	VP5_VLC_DCHR_VLIC0 VLCS intermediate control stream DMA channel register 0
08	00	00	01	00	00	00	00	00	00	01	42	2d	00	1e	00	VP5_VLC_SPAR
08	00	00	01	00	00	80	00	00	00	00	00	00	00	00	00	VP5_VLC_SH word 0
08	00	00	01	00	00	80	08	00	00	00	00	00	00	00	00	VP5_VLC_SH word 1
08	00	00	01	00	00	80	10	00	00	00	00	00	00	00	00	VP5_VLC_SH word 2
08	00	00	01	00	00	80	18	00	00	00	00	00	00	00	00	VP5_VLC_SH word 3
08	00	00	01	00	00	80	20	00	00	00	00	00	00	00	00	VP5_VLC_SH word 4
08	00	00	01	00	00	80	28	00	02	00	01	00	65	00	01	VP5_VLC_SH word 5
08	00	00	01	00	00	80	30	11	01	00	00	00	00	00	00	VP5_VLC_SH word 6
08	00	00	01	00	00	80	70	00	00	00	00	00	00	05	46	VP5_VLC_SH word 14
08	00	00	01	00	00	0f	50	00	00	00	12	00	01	00	2e	VP5_VLC_MODE
08	00	00	01	00	00	0f	80	00	00	00	00	00	0f	43	00	VP5_VLC_STRA_BS stream buffer size register
08	00	00	01	00	00	0f	a0	00	00	00	00	00	1e	86	00	VP5_VLC_IS_BS0 VLCS intermediate stream 0 buffer size register
08	00	00	01	00	00	0f	b0	00	00	00	00	00	1e	86	00	VP5_VLC_IS_BS1 VLCS intermediate stream 1 buffer size register
80	00	00	01	00	00	10	07	00	00	00	00	00	00	00	00	Last packet for the initialization routine

Specify the base addresses in VP5_BAAR0. Set the base addresses of the intermediate stream and intermediate control stream equal to the addresses output by the CE as follows.

VP5_BAAR0.CEIS0→VP5_BAAR1.VLIS1

VP5_BAAR0.CEIC0→VP5_BAAR1.VLIC1

VP5_BAAR1.CEIS1→VP5_BAAR0.VLIS0

VP5_BAAR1.CEIC1→VP5_BAAR0.VLIC0

Set the DMA channel registers for decoding. Set VP5_GDMAC_ARDPRI and VP5_GDMAC_SHWARBT when activing the VLCS for the first I picture. Specify mode=1 (decoding), num_ref_frame = 1, ce = 1, dec_out_disable = 0, stream_type = 2(H.264), mb_width = H'2d (= 720/16) and mb_height = H'1e (= 480/16) in VP5_VLC_SPAR. Specify EPrevDelEn = 0, EPrevInsEn = 1 and CmdEn = 0 in VP5_VLC_MODE for encoding. Specify VPU address[21:17] = H'10 for the last packet for the DMAC channel 0 initialization routine.

3. Create VLCS operation control parameters and store them into the external memory. Their base address is H'101B 7400 (set in VP5_CE_PBA1) for this example.

Table 27.49 VLCS DMAC Channel Operation Control Parameters for 720 × 480 I Picture Encoding

Setting																Description
d0	00	00	01	00	00	40	e0	13	b7	4f	00	00	00	00	00	VP5_BAAR1 VLCS intermediate stream base address
d0	00	00	01	00	00	40	e8	13	d5	d5	00	00	00	00	00	VP5_BAAR1 VLCS intermediate control stream base address
d0	00	00	01	00	00	00	e0	88	a0	70	00	00	00	12	1c	VP5_VLC_DCHR_VLIS1 VLCS intermediate stream DMA channel register 1
d0	00	00	01	00	00	00	e8	88	a8	70	00	00	00	12	1d	VP5_VLC_DCHR_VLIC1 VLCS intermediate control stream DMA channel register 1
00	00	00	01	00	00	10	07	00	00	00	00	00	00	00	00	Last packet for the initialization routine

Specify the base addresses in VP5_BAAR1. Set the DMA channel registers for decoding. Set the base addresses of the intermediate stream and intermediate control stream equal to the addresses output by the CE as follows.

VP5_BAAR0.CEIS0→VP5_BAAR1.VLIS1

VP5_BAAR0.CEIC0→VP5_BAAR1.VLIC1

VP5_BAAR1.CEIS1→VP5_BAAR0.VLIS0

VP5_BAAR1.CEIC1→VP5_BAAR0.VLIC0

Specify the base addresses in VP5_BAAR1. Set the DMA channel registers for decoding. Specify VPU address[21:17] = H'00 for the last packet for the DMAC channel 1 initialization routine.

4. Make settings for system control and initialization routine activation. Then, start the VLCS. When the VLCS is activated, the CE processing should already be terminated. Below are sample register settings. Start the VLCS with the VME bit = 1 and the VE bit = 1 in the VP5_CTRL register.

```
register_write ( VP5_CTRL,      H'0000 C500 ); // Overall operation settings
register_write ( VP5_IRQ_ENB,   H'0000 0101 ); // Interrupt enable
register_write ( VP5_VLC_MBA,   H'100A 3000 ); // Microcode base address
register_write ( VP5_VLC_PBA0,  H'100B 4000 ); // Parameter base address
register_write ( VP5_VLC_PBA1,  H'101B 7400 ); // Parameter base address
register_write ( VP5_CMD,       H'0000 0001 ); // Activation
```

5. Check the results.

   The VS bit in the VP5_STATUS register indicates the VPU5HG VLCS is active. When it terminates its operation, this bit is set to 0 and the VLE bit in the VP5_IRQ_STA register is set to 1, indicating the termination status.

   After the operation, check the following status registers:

   VP5_VLC_TB
   VP5_VLC_ERRH
   VP5_VLC_ERRL

(c) Encoding by the CE (P Picture)

The following shows an example of encoding by the CE for P pictures.

1. When the CE is used to encode a P picture after an I picture, there is no need to reset the microcode.
2. Create CE0 operation control parameters and store them into the external memory. Their base address is H'1021 0000 (set in VP5_CE_PBA0) for this example

Table 27.50 Sample CE0 Operation Control Parameters for 720 × 480 P Picture Encoding

Setting																Description
50	00	00	01	00	00	40	40	12	d8	00	00	00	00	00	00	VP5_BAAR0 decode picture luminance base address
50	00	00	01	00	00	40	48	12	e0	00	00	00	00	00	00	VP5_BAAR0 decode picture chrominance base address
50	00	00	01	00	00	40	90	13	db	d3	00	00	00	00	00	VP5_BAAR0 MV information base address
50	00	00	01	00	00	40	b0	13	96	cb	00	00	00	00	00	VP5_BAAR0 intermediate stream base address
50	00	00	01	00	00	40	b8	13	b5	51	00	00	00	00	00	VP5_BAAR0 intermediate control stream base address
50	00	00	01	00	00	42	00	12	a2	00	00	00	00	00	00	VP5_BAAR0 reference picture luminance address 0
50	00	00	01	00	00	42	08	12	aa	00	00	00	00	00	00	VP5_BAAR0 reference picture chrominance address 0
50	00	00	01	00	00	00	40	d0	00	00	80	00	00	08	08	VP5_CE_DCHR_DECY0 decode luminance picture DMA channel register 0
50	00	00	01	00	00	00	48	d0	00	00	80	00	00	08	09	VP5_CE_DCHR_DECC0 decode chrominance picture DMA channel register 0
50	00	00	01	00	00	00	60	b0	00	00	80	00	00	02	00	VP5_CE_DCHR_REF reference picture DMA channel register
50	00	00	01	00	00	00	90	c0	00	00	00	00	00	0c	12	VP5_CE_DCHR_MVINFO0 MV information stream DMA channel register 0
50	00	00	01	00	00	00	b0	c0	00	00	00	00	00	10	16	VP5_CE_DCHR_CEIS0 CE intermediate stream DMA channel register 0
50	00	00	01	00	00	00	b8	c0	00	00	00	00	00	10	17	VP5_CE_DCHR_CEIC0 CE intermediate control stream DMA channel register 0
00	00	00	01	00	00	00	00	00	00	01	42	2d	00	1e	00	VP5_CE_SPAR
00	00	00	01	00	00	00	08	20	00	00	00	00	00	00	00	VP5_CE_PPAR
00	00	00	01	00	00	00	50	01	01	01	01	01	01	00	00	VP5_CE_ENC_WPRED
00	00	00	01	00	00	00	58	00	ff	1f	40	00	00	b0	40	VP5_CE_ENC_CTRL
00	00	00	01	00	00	00	60	25	1d	00	24	01	59	00	00	VP5_CE_ACQ_CTRL
00	00	00	01	00	00	00	68	00	1a	20	26	2c	31	72	40	VP5_CE_ME_COST
00	00	00	01	00	00	00	a0	00	00	00	00	1e	00	1e	02	VP5_CE_VLCF
00	00	00	01	00	00	00	a8	00	00	00	00	00	00	00	00	VP5_CE_SLC_SIZE
00	00	00	01	00	00	00	b0	00	00	05	46	ff	ff	00	01	VP5_CE_TBIT
00	00	00	01	00	00	00	b8	00	00	85	55	00	00	00	00	VP5_CE_RCDJ
48	00	00	01	00	00	04	40	00	00	00	00	00	1e	86	00	VP5_CE_IS_BS0 CE intermediate stream 0 buffer size register
80	00	00	01	00	00	10	07	00	00	00	00	00	00	00	00	Last packet for the initialization routine

Specify the base addresses in VP5_BAAR0. This example assumes that the intermediate stream and intermediate control stream are configured with a double buffer, and that the specified base addresses are different from those for the I picture encoding. Set the DMA channel registers for encoding. With hsize in the decode and reference picture DMA channel registers, specify 1024/8 which is greater than a horizontal picture size of 720. Specify num_ref_frame = 1, ce = 1, dec_out_disable = 0, stream_type = 2(H.264), mb_width = H'2D (= 720/16) and mb_height = H'1E (= 480/16) in VP5_CE_SPAR. Specify pic_type = 0 and refidx_last0 = 0 in VP5_CE_PPAR. Specify the recommended values in VP5_CE_ENC_WPRED, VP5_CE_ENC_CTRL, VP5_CE_ACQ_CTRL and VP5_CE_ME_COST. Set H'0000 0000 in VP5_CE_FME*n*_QNC*m*

and VP5_CE_TRF*n*_QNC*m* (*n* = 0, *m* = 1). Specify VPU address[21:17] = H'10 for the last packet for the CE0 initialization routine.

3. Create CE1 operation control parameters and store them into the external memory. Their base address is H'1013 6400 (set in VP5_CE_PBA1) for this example.

Table 27.51 Sample CE0 Operation Control Parameters for 720 × 480 P Picture Encoding

Setting																Description
d0	00	00	01	00	00	40	40	12	d8	00	00	00	00	00	00	VP5_BAAR1 decode picture luminance base address
d0	00	00	01	00	00	40	48	12	e0	00	00	00	00	00	00	VP5_BAAR1 decode picture chrominance base address
d0	00	00	01	00	00	40	60	12	00	00	00	00	00	00	00	VP5_BAAR1 encode picture luminance base address
d0	00	00	01	00	00	40	68	12	08	00	00	00	00	00	00	VP5_BAAR1 encode picture chrominance base address
d0	00	00	01	00	00	40	90	13	dc	d3	00	00	00	00	00	VP5_BAAR1 MV information base address
d0	00	00	01	00	00	40	b0	13	55	c3	00	00	00	00	00	VP5_BAAR1 intermediate stream base address
d0	00	00	01	00	00	40	b8	13	74	49	00	00	00	00	00	VP5_BAAR1 intermediate control stream base address
d0	00	00	01	00	00	00	40	d0	00	00	80	00	00	08	08	VP5_CE_DCHR_DECY1 decode luminance picture DMA channel register 1
d0	00	00	01	00	00	00	48	d0	00	00	80	00	00	08	09	VP5_CE_DCHR_DECC1 decode chrominance picture DMA channel register 1
d0	00	00	01	00	00	00	68	b0	00	00	80	00	00	00	00	VP5_CE_DCHR_TMP1 encode picture DMA channel register
d0	00	00	01	00	00	00	90	c0	00	00	00	00	00	0c	12	VP5_CE_DCHR_MVINFO1 MV information output DMA channel register 1
d0	00	00	01	00	00	00	b0	c0	00	00	00	00	00	10	16	VP5_CE_DCHR_CEIS1 CE intermediate stream 1 buffer size register
d0	00	00	01	00	00	00	b8	c0	00	00	00	00	00	10	17	VP5_CE_DCHR_CEIC1 CE intermediate control stream DMA channel register 1
c8	00	00	01	00	00	04	40	00	00	00	00	00	1e	86	00	VP5_CE_IS_BS1 CE intermediate stream 1 buffer size register
c0	00	00	01	00	00	00	50	00	00	00	04	00	00	00	00	VP5_CE_DEB_LMDMASR1 DEB1LMDMA synchronous register
00	00	00	01	00	00	10	07	00	00	00	00	00	00	00	00	Last packet for the initialization routine

Specify the base addresses in VP5_BAAR1. This example assumes that the intermediate stream and intermediate control stream are configured with a double buffer, and that the specified base addresses are different from those for the I picture encoding. Set the DMA channel registers for encoding. Specify VP5_CE_DEB_LMDMASR1 for the CE1 operation control parameter. Specify VPU address[21:17] = H'00 for the last packet for the CE1 initialization routine.

4. Make settings for system control and initialization routine activation. Then, start the CE. Below are sample register settings. Start the CE with the CME bit = 0 and the CE bit = 1 in the VP5_CTRL register.

```
register_write ( VP5_CTRL,      H'0000 00B1 ); // Overall operation settings
register_write ( VP5_IRQ_ENB,   H'0000 0101 ); // Interrupt enable
register_write ( VP5_CE_PBA0,   H'1002 1000 ); // Parameter base address
register_write ( VP5_CE_PBA1,   H'1013 6400 ); // Parameter base address
register_write ( VP5_CMD,       H'0000 0001 ); // Activation
```

5. Check the results as described for the I picture processing.

(d) Encoding by the VLCS (P Picture)

1. When the VLCS is used to encode a P picture after an I picture, there is no need to reset the microcode.
2. Create VLCS operation control parameters and store them into the external memory. Their base address is H'100B 4000 (set in VP5_CE_PBA0) for this example.

Table 27.52 Sample VLCS DMAC Channel 0 Operation Control Parameters for 720 × 480 P Picture Encoding

Setting																Description
50	00	00	01	00	00	40	c0	13	44	00	00	00	00	00	00	VP5_BAAR0 stream A base address
50	00	00	01	00	00	40	e0	13	55	c3	00	00	00	00	00	VP5_BAAR0 VLCS intermediate stream base address
50	00	00	01	00	00	40	e8	13	74	49	00	00	00	00	00	VP5_BAAR0 VLCS intermediate control stream base address
50	00	00	01	00	00	00	c0	c0	00	00	00	00	00	14	18	VP5_VLC_SCHR_STRA stream A DMA channel register 0
50	00	00	01	00	00	00	e0	88	a0	70	00	00	00	12	1c	VP5_VLC_DCHR_VLIS0 VLCS intermediate stream DMA channel register 0
50	00	00	01	00	00	00	e8	88	a8	70	00	00	00	12	1d	VP5_VLC_DCHR_VLIC0 VLCS intermediate control stream DMA channel register 0
08	00	00	01	00	00	00	00	00	00	01	42	2d	00	1e	00	VP5_VLC_SPAR
08	00	00	01	00	00	80	00	00	00	00	00	00	00	00	00	VP5_VLC_SH word 0
08	00	00	01	00	00	80	08	00	00	00	00	00	00	00	00	VP5_VLC_SH word 1
08	00	00	01	00	00	80	10	00	00	00	00	00	00	00	00	VP5_VLC_SH word 2
08	00	00	01	00	00	80	18	00	00	00	00	00	00	00	00	VP5_VLC_SH word 3
08	00	00	01	00	00	80	20	00	00	00	00	00	00	00	00	VP5_VLC_SH word 4
08	00	00	01	00	00	80	28	00	01	00	0f	00	41	00	01	VP5_VLC_SH word 5
08	00	00	01	00	00	80	30	34	08	00	20	00	00	00	00	VP5_VLC_SH word 6
08	00	00	01	00	00	80	70	00	00	00	00	00	00	05	46	VP5_VLC_SH word 14
08	00	00	01	00	00	0f	50	00	00	00	12	00	01	00	2e	VP5_VLC_MODE
08	00	00	01	00	00	0f	80	00	00	00	00	00	0f	43	00	VP5_VLC_STRA_BS stream buffer size register
08	00	00	01	00	00	0f	a0	00	00	00	00	00	1e	86	00	VP5_VLC_IS_BS0 VLCS intermediate stream 0 buffer size register
08	00	00	01	00	00	0f	b0	00	00	00	00	00	1e	86	00	VP5_VLC_IS_BS1 VLCS intermediate stream 1 buffer size register
80	00	00	01	00	00	10	07	00	00	00	00	00	00	00	00	Late packet for the initialization routine

Specify the base addresses in VP5_BAAR0. Set the base addresses of the intermediate stream and intermediate control stream equal to the addresses output by the CE as follows.

VP5_BAAR0.CEIS0→VP5_BAAR1.VLIS1

VP5_BAAR0.CEIC0→VP5_BAAR1.VLIC1

VP5_BAAR1.CEIS1→VP5_BAAR0.VLIS0

VP5_BAAR1.CEIC1→VP5_BAAR0.VLIC0

Set the DMA channel registers, VP5_VLC_SPAR and VP5_VLC_MODE to the same values as those for the I picture encoding. Specify VPU address[21:17] = H'10 for the last packet for the DMAC channel 0 initialization routine.

3. Create VLCS operation control parameters and store them into the external memory. Their base address is H'101B 7400 (set in VP5_CE_PBA1) for this example.

Table 27.53 Sample VLCS DMAC Channel 1 Operation Control Parameters for 720 × 480 P Picture Encoding

Setting																Description
d0	00	00	01	00	00	40	e0	13	96	cb	00	00	00	00	00	VP5_BAAR1 VLCS intermediate stream base address
d0	00	00	01	00	00	40	e8	13	b5	51	00	00	00	00	00	VP5_BAAR1 VLCS intermediate control stream base address
d0	00	00	01	00	00	00	e0	88	a0	70	00	00	00	12	1c	VP5_VLC_DCHR_VLIS1 VLCS intermediate stream DMA channel register 1
d0	00	00	01	00	00	00	e8	88	a8	70	00	00	00	12	1d	VP5_VLC_DCHR_VLIC1 VLCS intermediate control stream DMA channel register 1
00	00	00	01	00	00	10	07	00	00	00	00	00	00	00	00	Late packet for the initialization routine

Specify the base addresses in VP5_BAAR1. Set the base addresses of the intermediate stream and intermediate control stream equal to the addresses output by the CE as follows.

VP5_BAAR0.CEIS0→VP5_BAAR1.VLIS1

VP5_BAAR0.CEIC0→VP5_BAAR1.VLIC1

VP5_BAAR1.CEIS1→VP5_BAAR0.VLIS0

VP5_BAAR1.CEIC1→VP5_BAAR0.VLIC0

Set the DMA channel registers for decoding. Specify VPU address[21:17] = H'00 for the last packet for the DMAC channel 1 initialization routine.

4. Make settings for system control and initialization routine activation. Then, start the VLCS. When the VLCS is activated, the CE processing should already be terminated. Below are sample register settings. Start the VLCS with the VME bit = 1 and the VE bit = 1 in the VP5_CTRL register.

```
register_write ( VP5_CTRL,      H'0000 C500 ); // Overall operation settings
register_write ( VP5_IRQ_ENB,   H'0000 0101 ); // Interrupt enable
register_write ( VP5_VLC_MBA,   H'100A 3000 ); // Microcode base address
register_write ( VP5_VLC_PBA0,  H'100B 4000 ); // Parameter base address
register_write ( VP5_VLC_PBA1,  H'101B 7400 ); // Parameter base address
register_write ( VP5_CMD,       H'0000 0001 ); // Activation
```

5. Check the results.

37.6.4 Decoding

(1) Overview of Decoding

The VPU5HG decoding process is divided into two stages. In the first stage, the VLCS performs variable-length decoding. In the second stage, the CE performs picture decoding. Figure 27.24 outlines the decoding process flow. First, the VLCS is activated to convert an encoded bit stream into intermediate data by variable-length decoding (stage 1). Then, the CE is activated to decode the picture data (stage 2). During these stages, the VLCS and CE decode data in picture units. They operate independently of each other. This permits forming a pipeline from the two stages. A termination interrupt can be output to provide notification when each module terminates its processing.

To make the VPU5HG work at its maximum processing capacity, the VLCS and CE should operate asynchronously. The CE is activated synchronously with the arrival of a picture.
The performance of the VLCS depends on the bit rate of bit streams, and because of this, the VLCS is activated asychronously with the arrival of a picture. Acquire an intermediate stream buffer large enough to contain an intermediate stream which is decoded by the VLCS before being decoded by the CE (the recommended size of that buffer is four times the VBV buffer size).

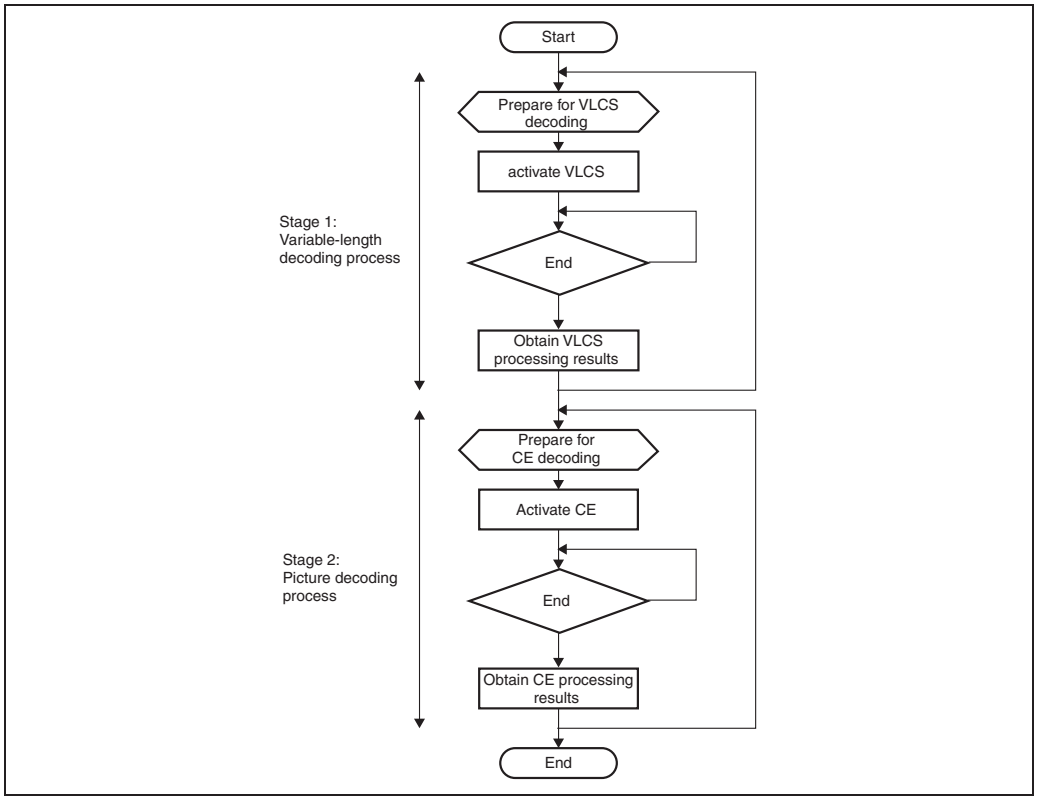


Figure 27.31 Overview of the Decoding Process Flow

(2) Variable-Length Decoding by VLCS Activation

An encoded bits stream is input for VPU5HG variable-length decoding by VLCS activation (stage 1). After this decoding, an intermediate stream is output. The VLCS decodes data in picture units. A termination interrupt can be output to provide notification when the VLCS terminates its processing.

To perform variable-length decoding by VLCS activation, first analyze the layers above the picture header level by using software and obtain the sequence-level and picture-level control parameters for the bit stream which should be decoded. H.264 decoding further involves analyzing the slice header and obtaining the additional control parameters.

Table 27.54 shows the input parameters and data required for variable-length decoding by VLCS activation. It also shows the setting methods for the VPU5HG. The inputs to the VLCS for decoding are system control information, microcode, picture parameters, GDMAC settings, command streams, bit streams and bit streams. The system control information, picture parameters, command streams and bit streams should be based on the results of header analysis by the software. Table 27.55 shows the output parameters and data for the VLCS as well as the output destinations. The software obtains the control parameters for picture decoding (stage 2) by CE activation and those for variable-length decoding (stage 1) by VLCS activation for the next picture.

Table 27.54 Input Parameters and Data for the VLCS

Item	Setting method	Description
System settings	Register	Settings for system control of the interrupt, etc., and for execution of the initialization routine
Microcode	Initialization routine	CE microcode
Operation setting parameter	Initialization routine	Picture-level control parameter and GDMAC settings
Command stream	Command stream	Parameter for the slice settings and the stream start address information
Bit stream	External RAM	Encode bit stream

Table 27.55 Output Parameters and Data for the VLCS

Item	Output destination	Description
System status	Register	Operation status
Picture status	Register	Encoding result status
Intermediate stream	External RAM	Intermediate data stream. (Output for each CE.)
Intermediate control stream	External RAM	Control information required for VLCS processing. (Output for each CE.)

Figure 27.32 shows the software for variable-length decoding by VLCS activation. It also shows the VPU5HG operation flow.

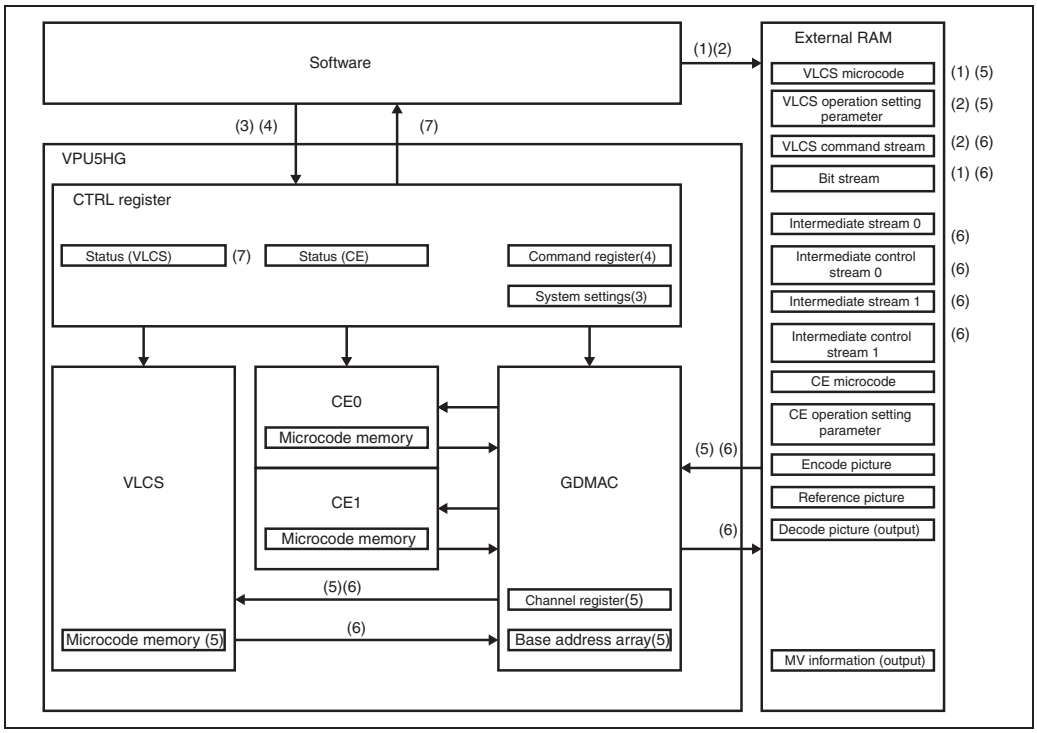


Figure 27.32 Conceptual Diagram of the Software for Variable-Length Decoding and the VLCS Operation Flow

No.	Decoding Sequence by the VLCS
(1)	The software stores the bit stream to be decoded into the external RAM. It also stores predetermined microcode into that memory. This code complies with the encoding standard.
(2)	The software analyzes the upper layers and stores the VLCS operation setting parameters and command streams into the external RAM.
(3)	The software sets the VPU5HG registers for system control and initialization routine execution according to the results of analyzing the upper layers.
(4)	The software activates the VLCS by writing 1 to VPU5HG VP5_CMD register.
(5)	The VPU5HG executes the initialization routine according to the system settings. This routine first downloads the microcode into the microcode memory in the VLCS. Then, it transfers the VLCS operation setting parameters to predetermined registers/RAM in the VLCS and GDMAC.
(6)	After the initialization routine execution, the VLCS performs decoding while at the same time reading the bit stream bit streams and command stream from the external RAM. It outputs an intermediate stream and intermediate control stream by this decoding.
(7)	After the VLCS processing, the software checks the decoding result status.

(3) Picture Decoding by CE Activation

An intermediate stream, subjected to variable-length encoding by the VLCS, is input for VPU5HG picture decoding by CE activation (stage 2). After this decoding, a decoded picture is output. The CE decodes data in picture units. A termination interrupt can be output to provide notification when the CE terminates its processing.

To decode picture data by CE activation, first set the sequence-level and picture-level control parameters for the intermediate stream to be decoded. Use software for setting them. Table 27.56 shows the input parameters and data required for this decoding. It also shows the setting methods for the VPU5HG. The inputs to the CE for decoding are system settings, microcode, CE operation setting parameters, intermediate streams, intermediate control streams, reference pictures and MV information. Table 27.57 shows the output parameters and data for the CE as well as the output destinations. The software obtains the control parameters for variable-length encoding (stage 2) by CE activation for the next picture.

Table 27.56 Input Parameters and Data for the CE

Item	Setting method	Description
System settings	Register	Settings for system control of the interrupt, etc., and for execution of the initialization routine
Microcode	Initialization routine	CE microcode
CE operation setting parameter	Initialization routine	Picture-level control parameters and GDMAC settings
Intermediate stream	External RAM	Intermediate data stream. (Required for each CE.)
Intermediate control stream	External RAM	Control information for CE processing. (Required for each CE.)
MV information	External RAM	Motion vector information (for B picture decoding only)
Reference picture	External RAM	Reference picture

Table 27.57 Output Parameters and Data for the CE

Item	Output destination	Description
System status	Register	Operation status
Picture status	Register	Decoding result status
Decoded picture	External RAM	Picture which is already decoded
MV information	External RAM	Motion vector information

Figure 27.33 shows the software for picture decoding by CE activation. It also shows the VPU5HG operation flow.

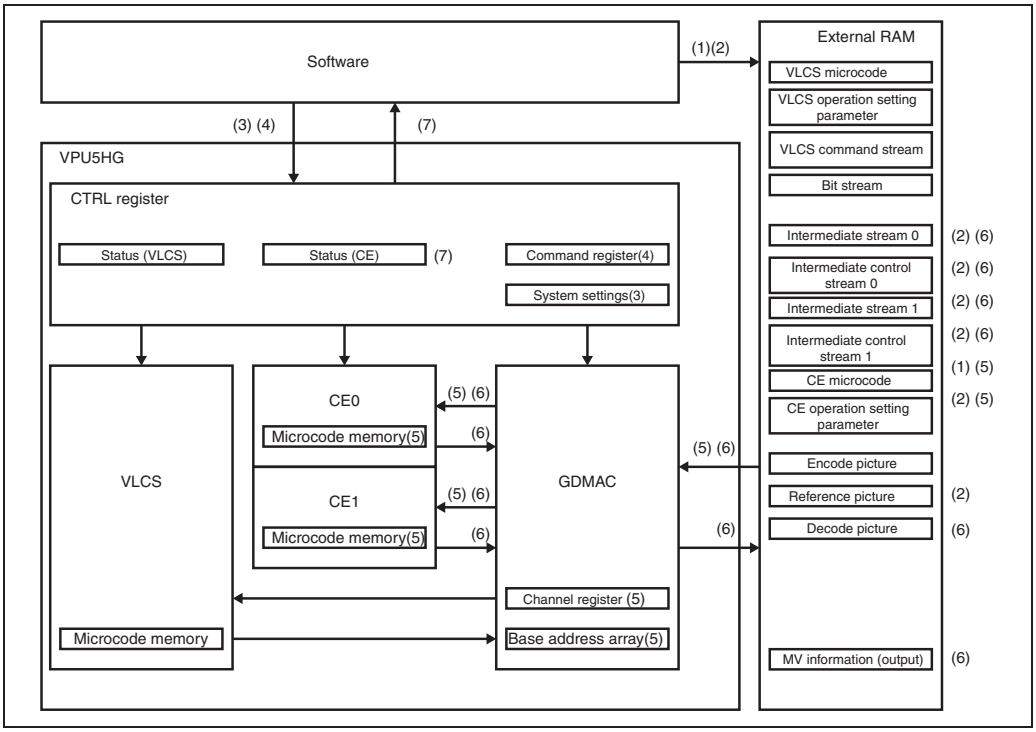


Figure 27.33 Conceptual Diagram of the Software for Picture Decoding and the CE Operation Flow

No.	Decoding Sequence by the CE
(1)	Store predetermined microcode into the external RAM. This code complies with the encoding standard.
(2)	The software stores the encode picture, reference picture, reference picture motion vector and CE operation setting parameters into the external RAM for picture data encoding.
(3)	The software sets the VPU5HG registers for system control and initialization routine execution.
(4)	The software activates the CE by writing 1 to VPU5HG VP5_CMD register.
(5)	The VPU5HG executes the initialization routine according to the system settings. This routine first downloads the microcode into the microcode memory in the CE. Then, it transfers the CE operation setting parameters to predetermined registers/RAM in the CE and GDMAC.
(6)	After the initialization routine execution, the CE reads the intermediate stream, intermediate control stream, reference picture and reference picture motion vector from the external RAM while at the same time performing decoding. The CE outputs a decoded picture after decoding. It also outputs MV information to the external RAM as required.
(7)	After the CE processing, the software checks the decoding result status.

(4) H.264 Decoding Procedures (720 Pixel × 480 Line Progressive Sequence)

The following describes the steps for H.264 decoding. The example below assumes that the stream is placed in H'1200 0000 and that the intermediate streams and intermediate control streams are configured with a double buffer. The SDRAM stored data and parameter settings are represented in big endian form. The endian settings for each DMAC channel register and those for VP5_CTRL are 0.

(a) Decoding by the VLCS (First I Picture)

1. Store the microcode into the external memory. Its base address is H'100A 3000 (set in VP5_CE_MBA) for this example.
2. Create VLCS DMAC channel 0 operation control parameters and store them into the external memory. Their base address is H'100B 4000 (set in VP5_CE_PBA0) for this example.

Table 27.58 Sample VLCS DMAC Channel 0 Operation Control Parameters for 720 × 480 I Picture Decoding

Setting																Description
50	00	00	01	00	00	40	d0	14	55	42	00	00	00	00	00	VP5_BAAR0 command stream base address
50	00	00	01	00	00	40	e0	13	cd	3e	00	00	00	00	00	VP5_BAAR0 VLCS intermediate stream base address
50	00	00	01	00	00	40	e8	14	4d	40	00	00	00	00	00	VP5_BAAR0 VLCS intermediate control stream base address
50	00	00	01	00	00	00	c0	08	a0	70	00	00	00	14	18	VP5_VLC_DCHR_STRAA stream A DMA channel register
50	00	00	01	00	00	00	d0	88	b0	70	00	00	00	14	1a	VP5_VLC_DCHR_CMDDMA command stream DMA channel register 0
50	00	00	01	00	00	00	e0	c0	00	00	00	00	00	12	1c	VP5_VLC_DCHR_VLIS0 VLCS intermediate stream DMA channel register 0
50	00	00	01	00	00	00	e8	c0	00	00	00	00	00	12	1d	VP5_VLC_DCHR_VLIC0 VLCSDMA0 intermediate control stream DMA channel register 0
50	00	00	01	00	00	10	38	00	00	00	80	00	00	00	00	VP5_GDMAC_SHWARBT
08	00	00	01	00	00	00	00	80	00	01	42	2d	00	1e	00	VP5_VLC_SPAR
08	00	00	01	00	00	0f	50	00	00	00	12	00	01	00	5e	VP5_VLC_MODE
08	00	00	01	00	00	0f	80	00	00	00	00	00	40	01	00	VP5_VLC_STRA_BS stream buffer size register
08	00	00	01	00	00	0f	a0	00	00	00	00	00	40	01	00	VP5_VLC_IS_BS0 VLCS intermediate stream 0 buffer size register
08	00	00	01	00	00	0f	b0	00	00	00	00	00	40	01	00	VP5_VLC_IS_BS1 VLCS1 intermediate stream 1 buffer size register
80	00	00	01	00	00	10	07	00	00	00	00	00	00	00	00	Late packet for the initialization routine

Specify the base addresses in VP5_BAAR0. Set the DMA channel registers for decoding. Set VP5_GDMAC_ARDPRI and VP5_GDMAC_SHWARBT when activating the VLCS for the first I picture. Specify mode = 1 (decode), num_ref_frame = 1, ce = 1, dec_out_disable = 0, stream_type = 2(H.264), mb_width = H'2D (= 720/16) and mb_height = H'1E (= 480/16) in VP5_VLC_SPAR. Specify EPrevDelEn = 1, EPrevInsEn = 0 and CmdEn = 1 in VP5_VLC_MODE for decoding. Specify VPU address[21:17] = H'10 for the last packet for the CE0 initialization routine.

3. Create VLCS DMAC channel 1 operation control parameters and store them into the external memory. Their base address is H'101B 7400 (set in VP5_CE_PBA1) for this example.

Table 27.59 Sample VLCS DMAC Channel 1 Operation Control Parameters for 720 × 480 I Picture Decoding

Setting																Description
d0	00	00	01	00	00	40	e0	14	0d	3f	00	00	00	00	00	VP5_BAAR1 VLCS intermediate stream base address
d0	00	00	01	00	00	40	e8	14	4f	41	00	00	00	00	00	VP5_BAAR1 VLCS intermediate control stream base address
d0	00	00	01	00	00	00	e0	c0	00	00	00	00	00	12	1c	VP5_VLC_DCHR_VLIS1 VLCS intermediate stream DMA channel register 1
d0	00	00	01	00	00	00	e8	c0	00	00	00	00	00	12	1d	VP5_VLC_DCHR_VLIC1 VLCS intermediate control stream DMA channel register 1
00	00	00	01	00	00	10	07	00	00	00	00	00	00	00	00	Late packet for the initialization routine

Specify the base addresses in VP5_BAAR1. Set the DMA channel registers for decoding. Specify VPU address[21:17] = H'00 for the last packet for the CE1 initialization routine.

4. Create command streams and store them into the external memory. Their base address is H'1455 4200 (set in VP5_BAAR0) for this example.

Table 27.57 Sampel Command Stream Settings for 720 × 480 I Picture Decoding

Setting																Description
00	00	00	53	12	00	00	1f	08	00	00	00	00	00	00	00	Command header (type0,type8)
90	00	80	00	00	00	00	03	00	00	00	00	00	00	00	00	Command header (type16,Length=3)
00	00	a8	05	1e	00	1e	00	00	00	00	00	00	00	00	00	Command header (type16). Continued from above.

Set the command stream by referring to section 27.5.5. For this example, set the operation control bits for the command headers of type 0 to the values (T = E = 1, S = I = 0) for the first and last slices of the picture. For command type 0, set Stream Start Address to the byte address (H'1200 001F) including the first bit of slice data and set bit_pos to bit position 3. For command headers of type 16, set three words (Length = 3) which are words 0 through 2 included in VP5_VLC_CMD (address H'0 8000). Also, set these words for I picture decoding.

5. Make settings for system control and initialization routine activation. Then, start the VLCS. When the VLCS is activated, the CE processing should already be terminated. Below are sample register settings. Start the VLCS with the VME bit = 1 and the VE bit = 1 in the VP5_CTRL register.

```
register_write ( VP5_CTRL,      H'0000 C500 ); // Overall operation settings
register_write ( VP5_IRQ_ENB,   H'0000 0101 ); // Interrupt enable
register_write ( VP5_VLC_MBA,   H'100C 3000 ); // Microcode base address
register_write ( VP5_VLC_PBA0,  H'100B 4000 ); // Parameter base address
register_write ( VP5_VLC_PBA1,  H'101B 7400 ); // Parameter base address
register_write ( VP5_CMD,       H'0000 0001 ); // Activation
```

6. Check the results.

   The VS bit in the VP5_STATUS register indicates the VPU5HG VLCS is active. When it terminates its operation, this bit is set to 0 and the VLE bit in the VP5_IRQ_STA register is set to 1, indicating the termination status.

   After the operation, check the following status registers:

   VP5_VLC_ERRH
   VP5_VLC_ERRL
   VP5_VLC_INT_TB0
   VP5_VLC_INT_TB1

(b) Decoding by the CE (First I Picture)

1. Store the microcode into the external memory. Its base address is H'1000 0000 (set in VP5_CE_MBA) for this example.
2. Create CE0 operation control parameters and store them into the external memory. Their base address is H'1021 0000 (set in VP5_CE_PBA0) for this example.

Table 27.58 Sample CE0 Operation Control Parameters for 720 × 480 I Picture Decoding

Setting																Description
50	00	00	01	00	00	40	40	12	5a	bc	00	00	00	00	00	VP5_BAAR0 decoding picture luminance base address
50	00	00	01	00	00	40	48	12	62	bd	00	00	00	00	00	VP5_BAAR0 decoding picture chrominance base address
50	00	00	01	00	00	40	90	12	67	73	80	00	00	00	00	VP5_BAAR0 MV information base address
50	00	00	01	00	00	40	b0	13	cd	3e	00	00	00	00	00	VP5_BAAR0 intermediate stream base address
50	00	00	01	00	00	40	b8	14	4d	40	00	00	00	00	00	VP5_BAAR0 intermediate control stream base address
50	00	00	01	00	00	42	00	00	00	00	00	00	00	00	00	VP5_BAAR0 reference picture luminance address 0
50	00	00	01	00	00	42	08	00	00	00	00	00	00	00	00	VP5_BAAR0 reference picture chrominance address 0
50	00	00	01	00	00	00	40	d0	00	00	80	00	00	08	08	VP5_CE_DCHR_DECY0 decode luminance picture DMA channel register 0
50	00	00	01	00	00	00	48	d0	00	00	80	00	00	08	09	VP5_CE_DCHR_DECC0 decode chrominance picture DMA channel register 0
50	00	00	01	00	00	00	60	b0	00	00	80	00	00	02	00	VP5_CE_DCHR_REF reference picture DMA channel register
50	00	00	01	00	00	00	90	c0	00	00	00	00	00	0c	12	VP5_CE_DCHR_MVINFO0 MV information output DMA channel register 0
50	00	00	01	00	00	00	b0	88	80	70	00	00	00	10	16	VP5_CE_DCHR_CEIS0 CE intermediate stream DMA channel register 0
50	00	00	01	00	00	00	b8	88	88	70	00	00	00	10	17	VP5_CE_DCHR_CEIC0 CE intermediate control stream DMA channel register 0
00	00	00	01	00	00	00	00	80	00	01	42	2d	00	1e	00	VP5_CE_SPAR
00	00	00	01	00	00	00	08	00	00	00	00	00	00	00	00	VP5_CE_PPAR
00	00	00	01	00	00	00	a0	00	00	00	00	00	00	00	02	VP5_CE_VLCF
48	00	00	01	00	00	04	40	00	00	00	00	00	40	01	00	VP5_CE_IS_BS0 CE intermediate stream 0 buffer size register
80	00	00	01	00	00	10	07	00	00	00	00	00	00	00	00	Late packet for the initialization routine

Specify the base addresses in VP5_BAAR0. Set the base addresses of the intermediate stream and intermediate control stream equal to the addresses output by the VLCS as follows.

VP5_BAAR0.VLIS0→VP5_BAAR1.CEIS0

VP5_BAAR0. VLIC0→VP5_BAAR1.CEIC0

VP5_BAAR1. VLIS1→VP5_BAAR0.CEIS1

VP5_BAAR1. VLIC1→VP5_BAAR0.CEIC1

Set the DMA channel registers for decoding. Specify num_ref_frame = 1, ce = 1, dec_out_disable = 0, stream_type = 2(H.264), mb_width = H'2D (=720/16) and mb_height = H'1E (=480/16) in VP5_CE_SPAR. Specify pic_type = 0 and refidx_last0 = 0 in VP5_CE_PPAR. Specify VPU address[21:17] = H'10 for the last packet for the CE0 initialization routine.

3. Create CE1 operation control parameters and store them into the external memory. Their base address is H'1013 6400 (set in VP5_CE_PBA1) for this example.

Table 27.59 Sample CE1 Operation Control Parameters for 720 × 480 I Picture Decoding

Setting																Description
d0	00	00	01	00	00	40	40	12	5a	bc	00	00	00	00	00	VP5_BAAR1 decode picture luminance base address
d0	00	00	01	00	00	40	48	12	62	bd	00	00	00	00	00	VP5_BAAR1 decode picture chrominance base address
d0	00	00	01	00	00	40	90	12	66	bd	80	00	00	00	00	VP5_BAAR1 MV information base address
d0	00	00	01	00	00	40	b0	14	0d	3f	00	00	00	00	00	VP5_BAAR1 intermediate stream base address
d0	00	00	01	00	00	40	b8	14	4f	41	00	00	00	00	00	VP5_BAAR1 intermediate control stream base address
d0	00	00	01	00	00	00	40	d0	00	00	80	00	00	08	08	VP5_CE_DCHR_DECY1 decode luminance picture DMA channel register 1
d0	00	00	01	00	00	00	48	d0	00	00	80	00	00	08	09	VP5_CE_DCHR_DECC1 decode chrominance picture DMA channel register 1
d0	00	00	01	00	00	00	90	c0	00	00	00	00	00	0c	12	VP5_CE_DCHR_MVINFO1 MV information output DMA channel register 1
d0	00	00	01	00	00	00	b0	88	80	70	00	00	00	10	16	VP5_CE_DCHR_CEIS1 CE intermediate stream DMA channel register 1
d0	00	00	01	00	00	00	b8	88	88	70	00	00	00	10	17	VP5_CE_DCHR_CEIC1 CE intermediate control stream DMA channel register 1
c8	00	00	01	00	00	04	40	00	00	00	00	00	40	01	00	VP5_CE_IS_BS1 CE intermediate stream 1 buffer size register
c0	00	00	01	00	00	00	50	00	00	00	04	00	00	00	00	VP5_CE_DEB_LMDMASR1 DEB1LMDMA synchronous register
00	00	00	01	00	00	10	07	00	00	00	00	00	00	00	00	Late packet for the initialization routine

Specify the base addresses in VP5_BAAR1. Set the base addresses of the intermediate stream and intermediate control stream equal to the addresses output by the VLCS as follows.

VP5_BAAR0.VLIS0→VP5_BAAR1.CEIS0

VP5_BAAR0. VLIC0→VP5_BAAR1.CEIC0

VP5_BAAR1. VLIS1→VP5_BAAR0.CEIS1

VP5_BAAR1. VLIC1→VP5_BAAR0.CEIC1

Set the DMA channel registers for decoding. Specify VP5_CE_DEB_LMDMASR1 for the CE1 operation control parameter. Specify VPU address[21:17] = H'00 for the last packet for the CE1

4. Make settings for system control and initialization routine activation. Then, start the CE. When the CE is activated, the VLCS processing for the picture should already be terminated. Below are sample register settings. Start the CE with the CEMD bit = 1, the CME bit = 1 and the CE bit = 1 in the VP5_CTRL register.

```
register_write ( VP5_CTRL,      H'0080 00B5 ); // Overall operation settings
register_write ( VP5_IRQ_ENB,   H'0000 0101 ); // Interrupt enable
register_write ( VP5_CE_MBA,    H'1000 0000 ); // Microcode base address
register_write ( VP5_CE_PBA0,   H'1002 1000 ); // Parameter base address
register_write ( VP5_CE_PBA1,   H'1013 6400 ); // Parameter base address
register_write ( VP5_CMD,       H'0000 0001 ); // Activation
```

5. Check the results.
   The CS bit in the VP5_STATUS register indicates the VPU5HG CE is active. When it terminates its operation, this bit is set to 0 and the CE bit in the VP5_IRQ_STA register is set to 1, indicating the termination status.
   After the operation, check the following status register:
   VP5_CE_ERR

(c) Decoding by the VLCS (P Picture)

1. When the VLCS is used to decode a P picture after an I picture, there is no need to reset the microcode.
2. When the VLCS is used to decode a P picture after an I picture, there is no need to reset the microcode.

Table 27.60 Sample VLCS DMAC Channel 0 Operation Control Parameters for 720 × 480 P Picture Decoding

Setting																Description
50	00	00	01	00	00	40	d0	14	55	42	00	00	00	00	00	VP5_BAAR0 command stream base address
50	00	00	01	00	00	40	e0	13	49	3a	00	00	00	00	00	VP5_BAAR0 VLCS intermediate stream base address
50	00	00	01	00	00	40	e8	13	c9	3c	00	00	00	00	00	VP5_BAAR0 VLCS intermediate control stream base address
50	00	00	01	00	00	00	c0	08	a0	70	00	00	00	14	18	VP5_VLC_DCHR_STRA stream A DMA channel register
50	00	00	01	00	00	00	d0	88	b0	70	00	00	00	14	1a	VP5_VLC_DCHR_CMDS command stream DMA channel register
50	00	00	01	00	00	00	e0	c0	00	00	00	00	00	12	1c	VP5_VLC_DCHR_VLIS0 VLCS intermediate stream DMA channel register 0
50	00	00	01	00	00	00	e8	c0	00	00	00	00	00	12	1d	VP5_VLC_DCHR_VLIC0 VLCS intermediate control stream DMA channel register 0
08	00	00	01	00	00	00	00	80	00	01	42	2d	00	1e	00	VP5_VLC_SPAR
08	00	00	01	00	00	0f	50	00	00	00	12	00	01	00	5e	VP5_VLC_MODE
08	00	00	01	00	00	0f	80	00	00	00	00	00	40	01	00	VP5_VLC_STRA_BS stream buffer size register
08	00	00	01	00	00	0f	a0	00	00	00	00	00	40	01	00	VP5_VLC_IS_BS0 VLCS intermediate stream 0 buffer size register
08	00	00	01	00	00	0f	b0	00	00	00	00	00	40	01	00	VP5_VLC_IS_BS1 VLCS intermediate stream 1 buffer size register
80	00	00	01	00	00	10	07	00	00	00	00	00	00	00	00	Late packet for the initialization routine

Specify the base addresses in VP5_BAAR0. This example assumes that the VLCS intermediate stream and VLCS intermediate control stream are configured with a double buffer, and that the specified base addresses are different from those for the I picture decoding. Set the DMA channel register, VP5_VLC_SPAR and VP5_VLC_MODE to the same values as those for the I picture decoding. Specify VPU address[21:17] = H'10 for the last packet for the DMAC channel 0 initialization routine.

3. Create VLCS operation control parameters and store them into the external memory. Their base address is H'101B7 400 (set in VP5_CE_PBA1) for this example.

Table 27.61 Sample VLCS DMAC Channel 1 Operation Control Parameters for 720 × 480 P Picture Decoding

Setting																Description
d0	00	00	01	00	00	40	e0	13	89	3b	00	00	00	00	00	VP5_BAAR1 VLCS intermediate stream base address
d0	00	00	01	00	00	40	e8	13	cb	3d	00	00	00	00	00	VP5_BAAR1 VLCS intermediate control stream base address
d0	00	00	01	00	00	00	e0	c0	00	00	00	00	00	12	1c	VP5_VLC_DCHR_VLIS1 VLCS intermediate stream DMA channel register 1
d0	00	00	01	00	00	00	e8	c0	00	00	00	00	00	12	1d	VP5_VLC_DCHR_VLIC1 VLCS intermediate control stream DMA channel register 1
00	00	00	01	00	00	10	07	00	00	00	00	00	00	00	00	Late packet for the initialization routine

Specify the base addresses in VP5_BAAR1. This example assumes that the VLCS intermediate stream and VLCS intermediate control stream are configured with a double buffer, and that the specified base addresses are different form those for the I picture decoding. Set the DMA channel register for decoding. Specify VPU address[21:17] = H'00 for the last packet for the DMAC channel 1 initialization routine.

4. Create command streams and store them into the external memory. Their base address is H'1455 4200 (set in VP5_BAAR0) for this example.

Table 27.62 Sample Command Stream Settings for 720 × 480 P Picture Decoding

Setting																Description
00	00	00	51	12	00	a8	0e	08	00	00	00	00	00	00	00	Command header (type0,type8)
10	00	80	18	00	00	00	01	00	00	00	00	00	00	00	00	Command header (type16Length=1)
90	00	80	00	00	00	00	03	20	00	00	00	00	00	00	00	Command header (type16Length=3)
00	00	32	c0	1e	00	1e	00	00	00	00	00	00	00	00	00	Command header (type16). Continued from above.

Set the command stream by referring to section 27.5.5, command stream. For this example, set the operation control bits for the command headers of type 0 to the values (T = E = 1, S = I = 0) for the first and last slices of the picture. Also, set Stream Start Address to the byte address (H'1200 00A8) including the first bit of slice data and set bit_pos to bit position 1.

For the first command header of type 16, set one word (Length = 1) included in VP5_VLC_REF_TBL (address H'0 8018). For the remaining command headers of type 16, set three words (Length = 3) which are words 0 through 2 included in VP5_VLC_CMD (address H'0 8000). For the progressive sequence, set word 2 in VP5_VLC_CMD to H'0000 0000.

5. Make settings for system control and initialization routine activation. Then, start the VLCS. Below are sample register settings. Start the VLCS with the VME bit = 0 and the VE bit = 1 in the VP5_CTRL register.

```
register_write ( VP5_CTRL,      H'0000 C100 ); // Overall operation settings
register_write ( VP5_IRQ_ENB,   H'0000 0101 ); // Interrupt enable
register_write ( VP5_VLC_PBA0,  H'100B 4000 ); // Parameter base address
register_write ( VP5_VLC_PBA1,  H'101B 7400 ); // Parameter base address
register_write ( VP5_CMD,       H'0000 0001 ); // Activation
```

6. Check the results as described for the I picture processing.

(d) Decoding by the CE (P Picture)

The following shows an example of decoding by the CE for P pictures.

1. When the CE is used to decode a P picture after an I picture, there is no need to reset the microcode.
2. Create CE0 operation control parameters and store them into the external memory. Their base address is H'10210000 (set in VP5_CE_PBA0) for this example.

Table 27.63 Sample CE0 Operation Control Parameters for 720 × 480 P Picture Decoding

Setting																Description
50	00	00	01	00	00	40	40	12	68	c3	00	00	00	00	00	VP5_BAAR0 decode picture luminance base address
50	00	00	01	00	00	40	48	12	70	c4	00	00	00	00	00	VP5_BAAR0 decode picture chrominance base address
50	00	00	01	00	00	40	90	12	75	7a	80	00	00	00	00	VP5_BAAR0 MV information base address
50	00	00	01	00	00	40	b0	13	49	3a	00	00	00	00	00	VP5_BAAR0 intermediate stream base address
50	00	00	01	00	00	40	b8	13	c9	3c	00	00	00	00	00	VP5_BAAR0 intermediate control stream base address
50	00	00	01	00	00	42	00	12	5a	bc	00	00	00	00	00	VP5_BAAR0 reference picture luminance address 0
50	00	00	01	00	00	42	08	12	62	bd	00	00	00	00	00	VP5_BAAR0 reference picture chrominance address 0
50	00	00	01	00	00	00	40	d0	00	00	80	00	00	08	08	VP5_CE_DCHR_DECY0 decode luminance picture DMA channel register 0
50	00	00	01	00	00	00	48	d0	00	00	80	00	00	08	09	VP5_CE_DCHR_DECC0 decode chrominance picture DMA channel register 0
50	00	00	01	00	00	00	60	b0	00	00	80	00	00	02	00	VP5_CE_DCHR_REF reference picture DMA channel register
50	00	00	01	00	00	00	90	c0	00	00	00	00	00	0c	12	VP5_CE_DCHR_MVINFO0 MV information output DMA channel register 0
50	00	00	01	00	00	00	b0	88	80	70	00	00	00	10	16	VP5_CE_DCHR_CEIS0 CE intermediate stream DMA channel register 0
50	00	00	01	00	00	00	b8	88	88	70	00	00	00	10	17	VP5_CE_DCHR_CEIC0 CE intermediate control stream DMA channel register 0
00	00	00	01	00	00	00	00	80	00	01	42	2d	00	1e	00	VP5_CE_SPAR
00	00	00	01	00	00	00	08	20	00	00	00	00	00	00	01	VP5_CE_PPAR
00	00	00	01	00	00	00	a0	00	00	00	00	00	00	00	02	VP5_CE_VLCF
48	00	00	01	00	00	04	40	00	00	00	00	00	40	01	00	VP5_CE_IS_BS0 CE intermediate stream 0 buffer size register
80	00	00	01	00	00	10	07	00	00	00	00	00	00	00	00	Late packet for the initialization routine

Specify the base addresses in VP5_BAAR0. Set the base addresses of the intermediate stream and intermediate control stream equal to the addresses output by the VLCS as follows.

VP5_BAAR0.VLIS0→VP5_BAAR1.CEIS0
VP5_BAAR0. VLIC0→VP5_BAAR1.CEIC0
VP5_BAAR1. VLIS1→VP5_BAAR0.CEIS1
VP5_BAAR1. VLIC1→VP5_BAAR0.CEIC1

Specify the reference picture address as the decode picture base address for the I picture. Set the DMA channel registers for decoding. Specify pic_type = 1 (P picture) and refidx_last0 = 0 in VP5_CE_PPAR. Specify VPU address[21:17] = H'10 for the last packet for the CE0 initialization routine.

3. Create CE1 operation control parameters and store them into the external memory. Their base address is H'1013 6400 (set in VP5_CE_PBA1) for this example.

Table 27.64 Sample CE1 Operation Control Parameters for 720 × 480 P Picture Decoding

Setting																Description
d0	00	00	01	00	00	40	40	12	68	c3	00	00	00	00	00	VP5_BAAR1 decode picture luminance base address
d0	00	00	01	00	00	40	48	12	70	c4	00	00	00	00	00	VP5_BAAR1 decode picture chrominance base address
d0	00	00	01	00	00	40	90	12	74	c4	80	00	00	00	00	VP5_BAAR1 MV information base address
d0	00	00	01	00	00	40	b0	13	89	3b	00	00	00	00	00	VP5_BAAR1 intermediate stream base address
d0	00	00	01	00	00	40	b8	13	cb	3d	00	00	00	00	00	VP5_BAAR1 intermediate control stream base address
d0	00	00	01	00	00	00	40	d0	00	00	80	00	00	08	08	VP5_CE_DCHR_DECY1 decode luminance picture DMA channel register 1
d0	00	00	01	00	00	00	48	d0	00	00	80	00	00	08	09	VP5_CE_DCHR_DECC1 decode chrominance picture DMA channel register 1
d0	00	00	01	00	00	00	90	c0	00	00	00	00	00	0c	12	VP5_CE_DCHR_MVINFO1 MV information output DMA channel register 1
d0	00	00	01	00	00	00	b0	88	80	70	00	00	00	10	16	VP5_CE_DCHR_CEIS1 CE intermediate stream DMA channel register 1
d0	00	00	01	00	00	00	b8	88	88	70	00	00	00	10	17	VP5_CE_DCHR_CEIC1 CE intermediate control stream DMA channel register 1
c8	00	00	01	00	00	04	40	00	00	00	00	00	40	01	00	VP5_CE_IS_BS1 CE intermediate stream 1 buffer size register
c0	00	00	01	00	00	00	50	00	00	00	04	00	00	00	00	VP5_CE_DEB_LMDMASR1 DEB1LMDMA synchronous register
00	00	00	01	00	00	10	07	00	00	00	00	00	00	00	00	Late packet for the initialization routine

Specify the base addresses in VP5_BAAR1. Set the base addresses of the intermediate stream and intermediate control stream equal to the addresses output by the VLCS as follows.

VP5_BAAR0.VLIS0→VP5_BAAR0.CEIS0
VP5_BAAR0. VLIC0→VP5_BAAR0.CEIC0
VP5_BAAR1. VLIS1→VP5_BAAR1.CEIS1
VP5_BAAR1. VLIC1→VP5_BAAR1.CEIC1

Specify the reference picture address as the decode picture base address for the I picture. Set the DMA channel registers for decoding. Specify VP5_CE_DEB_LMDMASR1 for the CE1 operation control parameter. Specify VPU address[21:17] = H'00 for the last packet for the CE0 initialization routine.

4. Make settings for system control and initialization routine activation. Then, start the CE.
   Below are sample register settings. Start the CE with the CEMD bit = 1, the CME bit = 0 and the CE bit = 1 in the VP5_CTRL register.

```
register_write ( VP5_CTRL,          H'0080 00B1 ); // Overall operation settings
register_write ( VP5_IRQ_ENB,       H'0000 0101 ); // Interrupt enable
register_write ( VP5_CE_PBA0,       H'1002 1000 ); // Parameter base address
register_write ( VP5_CE_PBA1,       H'1013 6400 ); // Parameter base address
register_write ( VP5_CMD,           H'0000 0001 ); // Activation
```

5. Check the results as described for the I picture processing.

37.7 Notes on Usage

Notes on usage of the VPU5HG are described below.

(1) Processing End

When the VPU5 detects a stream error during decoding other than H.264, it skips streams to the next resynchronization marker or start code. Therefore, if the VPU5 detects an error during decoding a stream that does not have the end code at the end of sequence and the error is found after a location, such as the last picture in the sequence, where no resynchronization marker or start code is appended, it may keep trying to find it in the stream forever. To prevent this, add a 4-byte code starting with "H'00" to the end of the stream depending on the stream standard when decoding a stream that has no end code at the end of the sequence of Streams Stream Standard Code to be added.

Stream Standard	Code to be Added
MPEG-2/MPEG-1	H'00 00 01 B7
MPEG-4	H'00 00 01 B1
H.263	H’00 00 FC 00
VC-1	H'00 00 01 0A

(2) Timing of Terminating Operations

In the LSI incorporating the VPU5 and ICB, the ICB may continue accessing memory after the VPU5HG operation is ended; there is a time lag until the end of ICB operation because the ICB buffers the data output from the VPU5HG and then writes it to external memory.

Accordingly, detect the end of VPU5HG operation through an interrupt or status register polling and then confirm that the corresponding status register of the ICBshows the end of ICB operation before checking the operation result.

For the LSI incorporating the VPU5 and ICB, refer to the ICB specifications.

Section 38 Image Extraction Direct Memory Access Controller (2D-DMAC)

This LSI has an image extraction direct memory access controller (2D-DMAC). This module reads the image data in the frame buffer memory, performs image extraction/shift/simple magnification and format conversion, and then rewrites the processed image data to the frame buffer memory.

38.1 Features

- Image extraction
  2D-DMAC extracts an image in the rectangular area from a point (Sx, Sy) shifting from the source image data origin to a point in the frame memory, and then writes the extracted image data to another frame memory. Extraction of data is possible in one-pixel units for YCbCr formats and in one-pixel units for RGB formats. This function is available for image clipping and image motion compensation.
- Image rotation/inversion
  Vertical/horizontal inversion and the 90°/270° rotation can be performed.
- Simple enlargement
  When writing a destination image, it can simply be enlarged twice in the X and Y directions.
- Format conversion
  RGB formats can be converted to each other.
  YCbCr formats (YCbCr4:2:0 and YCbCr4:2:2) can be converted to each other.
  No format conversion is possible between RGB and YCbCr.
  The format conversion method is equivalent to that of VIO.
- Channels
  Settings for eight channels are enabled. For the YCbCr formats, settings for one channel for each Y plane and C plane are enabled. Therefore, concurrent processing is possible for up to four planes (YCbCr formats) or up to eight planes (RGB formats).
  Provided with an outstanding buffer for each channel, even if data transfer of a channel is blocked, 2D-DMAC can continue operation of other channels. Transition of processing between channels is performed upon completion of each line processing.
- Interrupt
  Each channel has interrupt request signals that can be output at the time of data transfer half end and data transfer end respectively.

Figure 38.1 shows a block diagram of 2D-DMAC and figure 38.2 shows a flow for the pixel processing block.

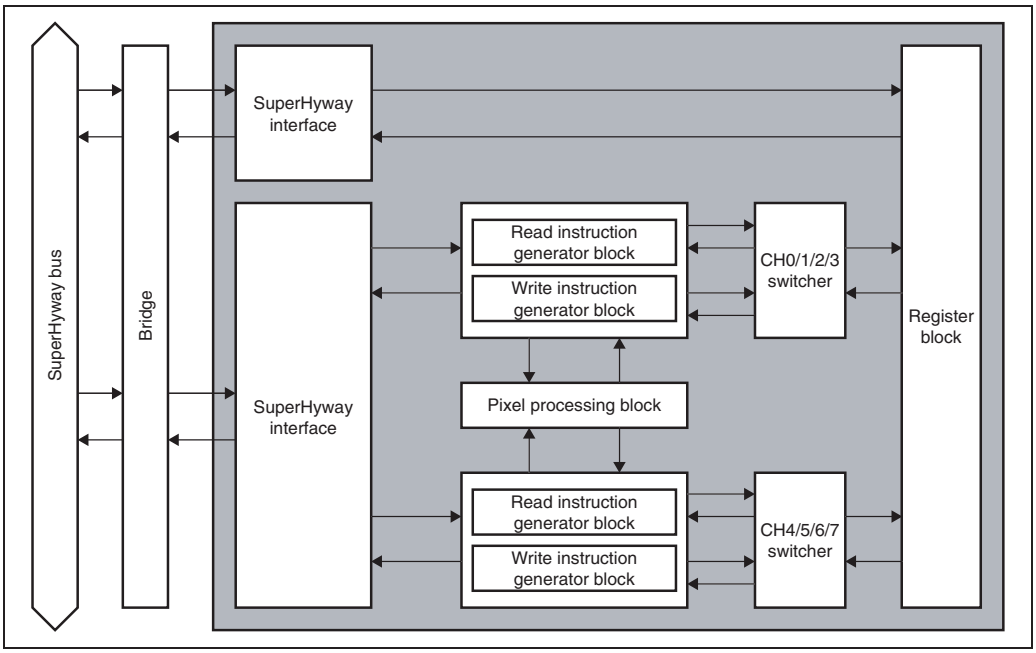


Figure 38.1 Block Diagram of 2D-DMAC

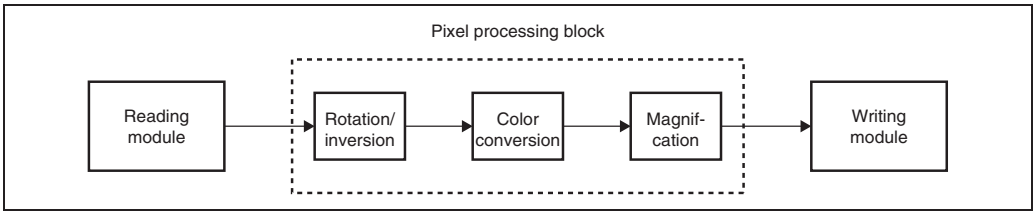


Figure 38.2 Block Flow of Pixel Block

38.2 Register Descriptions

Table 38.1 lists the registers used in 2D-DMAC. Table 38.2 shows the register status in each processing mode.

Table 38.1 Register Configuration

Register Name	Abbreviation	R/W	Address	Access Size
Interrupt status clear register	CHSTCLR	R/W	H'FEA0 0010	32
CH0 control register	CH0CTRL	R/W	H'FEA0 0020	32
CH1 control register	CH1CTRL	R/W	H'FEA0 0024	32
CH2 control register	CH2CTRL	R/W	H'FEA0 0028	32
CH3 control register	CH3CTRL	R/W	H'FEA0 002C	32
CH4 control register	CH4CTRL	R/W	H'FEA0 0120	32
CH5 control register	CH5CTRL	R/W	H'FEA0 0124	32
CH6 control register	CH6CTRL	R/W	H'FEA0 0128	32
CH7 control register	CH7CTRL	R/W	H'FEA0 012C	32
CH0 input swap register	CH0SWAP	R/W	H'FEA0 0030	32
CH1 input swap register	CH1SWAP	R/W	H'FEA0 0034	32
CH2 input swap register	CH2SWAP	R/W	H'FEA0 0038	32
CH3 input swap register	CH3SWAP	R/W	H'FEA0 003C	32
CH4 input swap register	CH4SWAP	R/W	H'FEA0 0130	32
CH5 input swap register	CH5SWAP	R/W	H'FEA0 0134	32
CH6 input swap register	CH6SWAP	R/W	H'FEA0 0138	32
CH7 input swap register	CH7SWAP	R/W	H'FEA0 013C	32
CH0 source address register	CH0SAR	R/W	H'FEA0 0080	32
CH0 destination address register	CH0DAR	R/W	H'FEA0 0084	32
CH0 destination pixel register	CH0DPXL	R/W	H'FEA0 0088	32
CH0 source format register	CH0SFMT	R/W	H'FEA0 008C	32
CH0 destination format register	CH0DFMT	R/W	H'FEA0 0090	32
CH0 source line address register	CH0SARE	R	H'FEA0 0094	32
CH0 destination line address register	CH0DARE	R	H'FEA0 0098	32
CH0 destination pixel processing register	CH0DPXLE	R	H'FEA0 009C	32
CH1****	CH1****	-	H'FEA0 00A0 to H'FEA0 00BC	32
CH2****	CH2****	-	H'FEA0 00C0 to H'FEA0 00DC	32

Register Name	Abbreviation	R/W	Address	Access Size
CH3****	CH3****	-	H'FEA0 00E0 to H'FEA0 00FC	32
CH4****	CH4****	-	H'FEA0 0180 to H'FEA0 019C	32
CH5****	CH5****	-	H'FEA0 01A0 to H'FEA0 01BC	32
CH6****	CH6****	-	H'FEA0 01C0 to H'FEA0 01DC	32
CH7****	CH7****	-	H'FEA0 01E0 to H'FEA0 01FC	32

Table 38.2 Register Status in Each Processing Mode

Abbreviation	Power-on Reset	Module Standby
CHSTCLR	Initialized	Retained
CHnCTRL	Initialized	Retained
CHnSWAP	Initialized	Retained
CHnSAR	Initialized	Retained
CHnDAR	Initialized	Retained
CHnDPXL	Initialized	Retained
CHnSFMT	Initialized	Retained
CHnDFMT	Initialized	Retained
CHnSARE	Initialized	Retained
CHnDARE	Initialized	Retained
CHnDPXLE	Initialized	Retained

n: 0 to 7

38.2.1 Control Registers (CHnCTRL)

CHnCTRL (n = 0 to 7) is a 32-bit readable/writable register that controls transfer mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HMRR	VMRR	ROTL	ROTR	—	MX	—	MY	HIE	HE	TIE	TE	—	—	STP	DMAEN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R/W	R	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	HMRR	0	R/W	Horizontal Inversion (symmetric to the vertical axis) The source image inverted horizontally is output. See table 38.5 details on the relations between this bit and inversion/rotation. 0: Horizontal inversion is not performed. 1: Inverted horizontally source image is output.
14	VMRR	0	R/W	Vertical Inversion (symmetric to the horizontal axis) The source image inverted vertically is output. See table 38.5 details on the relations between this bit and inversion/rotation. 0: Vertical inversion is not performed. 1: Inverted vertically source image is output.
13	ROTL	0	R/W	270° Rotation (clockwise) The source image rotated 270° is output. When this bit is 1, set the ROTR bit to 0. See table 38.5 details on the relations between this bit and inversion/rotation. 0: 270° rotation is not performed. 1: Rotated 270° source image is output.

Bit	Bit Name	Initial Value	R/W	Description
12	ROTR	0	R/W	90° Rotation (clockwise) The source image rotated 90° is output. When this bit is 1, set the ROTR bit to 0. See table 38.5 details on the relations between this bit and inversion/rotation.

				0: 90° rotation is not performed. 1: Rotated 90° source image is output.
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10	MX	0	R/W	Magnify X Direction 0: No magnification 1: Outputs with double magnification in the X direction. When ROTR or ROTL is 1, set this bit to 0.
9	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
8	MY	0	R/W	Magnify Y Direction 0: No magnification 1: Outputs with double magnification in the Y direction. When ROTR or ROTL is 1, set this bit to 0.
7	HIE	0	R/W	Half End Interrupt Enable Specifies whether to output the half end flag as an interrupt request. 0: A half end interrupt is disabled. 1: A half end interrupt is enabled.

Bit	Bit Name	Initial Value	R/W	Description
6	HE	0	R/W	Half End Indicates that data transfer for half the setting lines has been completed. This bit is set to 1 when the DVPXLE bit in CHnDPXLE becomes half (a value of 1-bit right shift) of the DVPXL bit value in CHnDPXL that was set before starting transfer. If CHnCTRL.ROTR=1 or CHnCTRL.ROTL=1, this bit is set to 1 when the DHPXLE bit in CHnDPXLE becomes half of the DHPXL bit value in CHnDPXL that was set before starting transfer. Only clearing to 0 after reading 1 is enabled. Clearing by the CHSTCLR register is also enabled.

5	TIE	0	R/W	Transfer End Interrupt Enable Specifies whether to output the transfer end flag as an interrupt request. 0: A transfer end interrupt is disabled. 1: A transfer end interrupt is enabled.
4	TE	0	R/W	Transfer End This bit is set to 1 when the DVPXL bit in CHxDPXL that was set by the DVPXLE bit in CHxDPXLE before starting transfer and the entire DMA transfer are completed. When this bit is set to 1 while the RPT bit is 0, the DMAEN bit is automatically cleared. Only clearing to 0 after reading 1 is enabled. Clearing by the CHSTCLR register is also enabled.
3, 2	LINK[1:0] (n=0,2,4,6) — (n=1,3,5,7)	00	R/W (n=0,2,4,6) R (n=1,3,5,7)	(n=0,2,4,6) Link Transfer Mode This mode enables alternate block line transfers between a master channel (CHn) and a slave channel (CHn+1). When these bits are set to 10, specify the DVPXL bit in CH(n+1)DPXL equal to half of the DVPXL in CHnDPXL. When these bits are set to 11, specify the DVPXL bit in CH(n+1)DPXL equal to the DVPXL in CHnDPXL. In this mode, start the transfer of the master channel before that of the slave channel. 00: Link transfer mode is disabled. 01: Setting prohibited. 10: A block line transfer of a slave channel is performed every two block line transfers of a master channel. 11: Alternate transfers are performed. (n=1,3,5,6) Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
1	STP	0	R/W	Transfer Stop Stops DMA transfer temporarily. When this bit is set to 1, DMA transfer is suspended upon completion of the line that is being transferred, and the DMAEN bit is cleared to 0. At this time, this bit is also cleared. To restart DMA transfer after that, set the DMAEN bit to 1. To reset the operation of a channel, rewrite data to the SAR, DAR, and DPXL registers of the channel. [Writing] 0: NOP 1: Stops DMA transfer temporarily. [Reading] 0: Transfer is in progress or suspended. 1: Pending until the line being transferred is completed
0	DMAEN	0	R/W	DMA Transfer Enable Enables DMA transfer. Only writing 1 is enabled. This bit shows 1 during transfer, and is automatically cleared when a DMA transfer is completed. Writing 0 to this bit is disabled. A DMA transfer can be suspended by setting the STP bit to 1. [Writing] 0: NOP 1: Performs DMA transfer. [Reading] 0: No DMA transfer is in progress. 1: A DMA transfer is in progress.

38.2.2 Input/Output Swap Register (CHnSWAP)

CHnSWAP (n = 0 to 7) controls 64-bit data swapping in the data input/output section of 2D-DMAC.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	OLS	OWS	OBS	—	ILS	IWS	IBS
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6	OLS	0	R/W	Output Longword Swap Setting In the output section of 2D-DMAC, 64 bits of data are swapped with 32 bits of the MSB and 32 bits of the LSB in longword units. 0: Output longword swap is not performed. 1: Output longword swap is performed.
5	OWS	0	R/W	Output Word Swap Setting In the output section of 2D-DMAC, 64 bits of data are swapped with 32 bits of the MSB and 32 bits of the LSB in word units. 0: Output word swap is not performed. 1: Output word swap is performed.
4	OBS	0	R/W	Output Byte Swap Setting In the output section of 2D-DMAC, 64 bits of data are swapped with 16-bit groups in byte units. 0: Output byte swap is not performed. 1: Output byte swap is performed.

Bit	Bit Name	Initial Value	R/W	Description
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

2	ILS	0	R/W	Input Longword Swap Setting In the input section of 2D-DMAC, 64 bits of data are swapped with 32 bits of the MSB and 32 bits of the LSB in longword units. 0: Input longword swap is not performed. 1: Input longword swap is performed.
1	IWS	0	R/W	Input Word Swap Setting In the input section of 2D-DMAC, 64 bits of data are swapped with 32 bits of the MSB and 32 bits of the LSB in word units. 0: Input word swap is not performed. 1: Input word swap is performed.
0	IBS	0	R/W	Input Byte Swap Setting In the input section of 2D-DMAC, 64 bits of data are swapped with 16-bit groups in byte units. 0: Input byte swap is not performed. 1: Input byte swap is performed.

When the system is operated in little-endian mode, this register should be used to select the swapping method conforming to the input/output format. The data relationships available when swapping methods are set are shown in figure 38.3, figure 38.4, and figure 38.5.

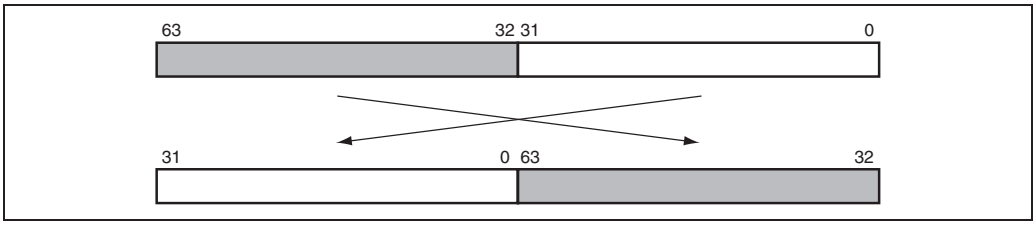


Figure 38.3 Data Relationship Before and After Longword Swapping

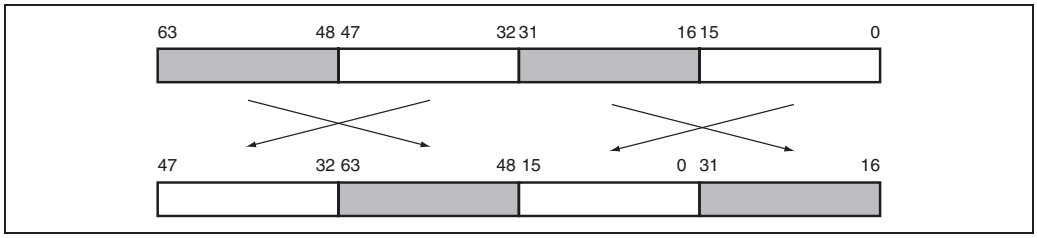


Figure 38.4 Data Relationship Before and After Word Swapping

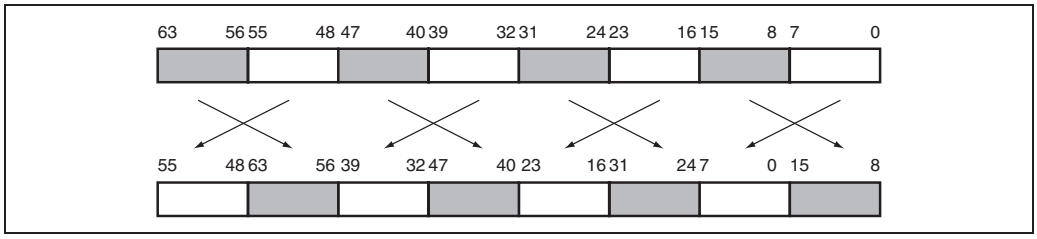


Figure 38.5 Data Relationship Before and After Byte Swapping

38.2.3 Source Format Registers (CHnSFMT)

CHnSFMT (n = 0 to 7) is a 32-bit readable/writable register for setting the source image.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	HWTH[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	MD[1:0]		PKF[4:0]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	HWTH[15:0]	H'0000	R/W	Source Image Horizontal Byte Size Specify the one-line width of the source image in units of bytes. This value should be a multiple of the pack size. When ROTR or ROTL is 1, set these bits to 16n.
15 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6, 5	MD[1:0]	00	R/W	Source Image Format 00: RGB data 01: Y data 10: CbCr data (YcbCr4:2:0) 11: CbCr data (YcbCr4:2:2)
4 to 0	PKF[4:0]	00000	R/W	Source Image RGB Data Packed Format Specify the packed format for source image data in the RGB format. These bits are available only when MD = 00. Table 38.3 shows the packed RGB formats.

Table 38.3 Packed RGB Formats

| PKF [4:0] | Format | Bit Rate [bpp] | Phase | Bit | | |

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SAR[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SAR[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	SAR[31:0]	H'00000000	R/W	Source Image Extraction Start Address Specify the address of the extraction start pixel in the source image data.

When the source image fills CHnSAR≠16n and cutting out effective pixel bytes

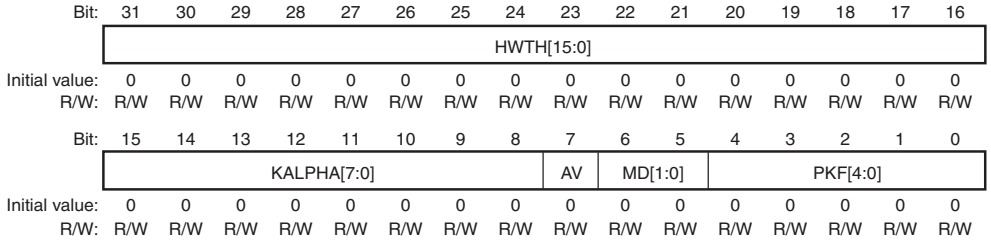
number ≦16byte , line finality access = address where line terminal address is rounded up to 16n + 16byte .

Address where source image final pixel address of cutting out object is rounded up to 16n + 16,

secure it as an input image area.

38.2.5 Destination Format Registers (CHnDFMT)

CHnDFMT (n = 0 to 7) is a 32-bit readable/writable register for setting a destination image format and so on.



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	HWTH[15:0]	H'0000	R/W	Destination Image Horizontal Byte Size Specify the one-line width of the destination image in units of bytes. Set a multiple of 16. When CTRL.MX is 1, set a value after magnification.
15 to 8	KALPHA [7:0]	H'00	R/W	Alpha Value Specify an alpha value used for output when the source image is in a format with or without alpha and the AV bit is set to 1.
7	AV	0	R/W	Alpha Enable 0: Disables the alpha value when the source image is in a format with alpha. When the output is in a format with alpha, the KALPHA value is output. 1: Enables the alpha value when the source image is in a format with alpha, and outputs the alpha value when the output is in a format with alpha.
6, 5	MD[1:0]	00	R/W	Destination Image Format 00: RGB data 01: Y data 10: CbCr data (YCbCr4:2:0) 11: CbCr data (YCbCr4:2:2)

Bit	Bit Name	Initial Value	R/W	Description
4 to 0	PKF[4:0]	00000	R/W	Destination Image RGB Data Packed Format Specify the packed format for destination image data in the RGB format. These bits are available only when MD = 00. Table 38.3 shows the packed RGB formats.

38.2.6 Destination Pixel Registers (CHnDPXL)

CHnDPXL (n = 0 to 7) is a 32-bit readable/writable register for setting the horizontal pixel size and vertical pixel size of the destination image.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DHPXL[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DVPXL[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	DHPXL[15:0]	H'0000	R/W	Destination Image Horizontal Pixel Size Specify the horizontal pixel size of the destination image. When the MX bit in CTRL is 1, set a value before magnification. For the CbCr plane in YCbCr4:2:2 or YCbCr4:2:0, set a value of half of the number of pixels. The minimum pixel size will be 1; set 1 or a larger value.
15 to 0	DVPXL[15:0]	H'0000	R/W	Destination Image Vertical Pixel Size Specify the vertical pixel size of the destination image. When the MX bit in CTRL is 1, set a value before magnification. For the CbCr plane in YCbCr4:2:0, set a value of half of the number of lines. The minimum pixel size will be 1; set 1 or a larger value.

38.2.7 Destination Address Registers (CHnDAR)

CHnDAR (n = 0 to 7) is a 32-bit readable/writable register for setting the transfer start address of the destination image.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DAR[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DAR[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DAR [31:0]	H'00000000	R/W	Specify the start address of the destination image. Only a multiple of 16 can be set. The specified address point is to be changed according to the settings to the VMRR, HMRR, ROTR, ROTL, and MY bits. See the section 38.3.2, Image Rotation/Inversion, for the setting instructions.

38.2.8 Source Line Address Registers (CHnSARE)

CHnSARE (n = 0 to 7) is a 32-bit read-only register that shows the start address of the line in processing of the source image.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SARE[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SARE[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	SARE [31:0]	H'00000000	R	This read-only register used for internal processing shows the start address of the line in processing of the source image.

38.2.9 Destination Line Address Registers (CHnDARE)

CHnDARE (n = 0 to 7) is a 32-bit read-only register that shows the start address of the line in processing of the destination image.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DARE[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DARE[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DARE [31:0]	H'00000000	R	This read-only register used for internal processing shows the start address of the line in processing of the destination image.

38.2.10 Destination Pixel Processing Registers (CHnDPXLE)

CHnDPXLE (n = 0 to 7) is a 32-bit read-only register that shows the number of unprocessed lines of the destination image.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DHPXLE[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DVPXLE[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	DHPXLE [15:0]	H'0000	R	This read-only register used for internal processing shows the number of unprocessed horizontal lines of the destination image.
15 to 0	DVPXLE [15:0]	H'0000	R	This read-only register used for internal processing shows the number of unprocessed vertical lines of the destination image.

38.2.11 Interrupt Status Clear Register (CHSTCLR)

CHSTCLR is a register that indicates the status of HE and TE bits in each channel. By writing 1 in a bit in CHSTCLR, HE or TE bit in the corresponding channel is to be cleared.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CHnHE[7:0]								CHnTE[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 8	CHnHE[7:0]	H'00	R/W	Indicates the status of the HE bit in CHnCTRL (n = 0 to 7). Writing 1 in this bit, the HE bit in corresponding channel is to be cleared. [Writing] 0: NOP 1: HE bit is cleared. [Reading] 0: 0 is set in the HE bit. 1: 1 is set in the HE bit.
7 to 0	CHnTE[7:0]	H'00	R/W	Indicates the status of the TE bit in CHnCTRL (n = 0 to 7). Writing 1 in this bit, the TE bit in corresponding channel is to be cleared. [Writing] 0: NOP 1: TE bit is cleared. [Reading] 0: 0 is set in the TE bit. 1: 1 is set in the TE bit.

38.3 Operation

This module can extract image data of required size from the source image and store it as a destination image, and also can convert the format, rotation/inversion, and magnify the image at that time.

38.3.1 Image Extraction

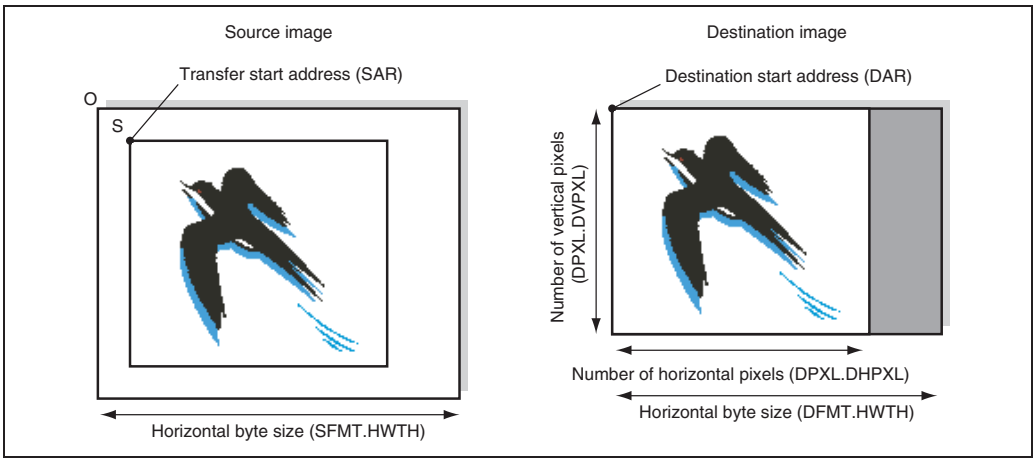


Figure 38.6 Schematic Diagram of Image Extraction

Figure 38.6 shows a schematic diagram of image extraction.

The image format conforms to the YCbCr4:2:0, YCbCr4:2:2, and RGB formats. Extraction of data is possible in two-pixel units for YCbCr formats and in one-pixel units for RGB formats. However, since the Y data and C data are independently stored in the memory in the YCbCr format, set them in different channels respectively.

For source images, the address of extraction start coordinates S and the horizontal byte size must be set in respective registers. Set the start address of the extraction start pixel in SAR. If the X coordinate of extraction start coordinates S (SAR) is an odd number with origin O in the YCbCr format, a deviation is generated between Y data and C data in the horizontal direction. Furthermore, in the YCbCr4:2:0 format, if the Y coordinate of extraction start coordinates S is an odd number with origin O, a deviation is generated between Y data and C data in the vertical direction. For each case, extract image data from the even pixel coordinates where truncation is made.

For destination images, destination start address, numbers of horizontal and vertical pixels, and the horizontal byte size must be set. Set an integer multiple of 16 (≥ DHPXL in DPXL x bytes per pixel) for the horizontal byte size (HWTH in DFMT). Discard the gray area in figure 38.6 as invalid data. For YCbCr formats, set an even number for the number of Y data horizontal pixels. In addition, for the YCbCr4:2:0 format, the number of vertical pixels must also be set to an even number.

Table 38.4 lists these restrictions.

Table 38.4 Restrictions for Each Format

Format	Item	Restrictions
Common	Destination image horizontal byte size (CHnDFMT.HWTH)	Set an integer multiple of 16.
Y data (YCbCr4:2:2)	Source image horizontal extraction start position (CHnSAR.SAR)	In a case that the X-coordinate of starting coordinate-S (SAR) relative to the coordinate origin 0 of source image is odd number, a deviation is generated between Y data and C data in the horizontal direction.
	Destination image horizontal pixel size (CHnDPXL.DHPXL)	In a case that the horizontal pixel size is odd number of the destination image, the invalid data might be generated right side in the image.
Y data (YCbCr4:2:0)	Source image horizontal extraction start position (CHnSAR.SAR)	In a case that the X-coordinate of starting coordinate-S (SAR) relative to the coordinate origin 0 of source image is odd number, a deviation is generated between Y data and C data in the horizontal direction.
	Source image vertical extraction start position (CHnSAR.SAR)	In a case that the Y-coordinate of starting coordinate-S (SAR) relative to the coordinate origin 0 of source image is odd number, the vertical throw between Y and CbCr is to be generated.
	Destination image horizontal pixel size (CHnDPXL.DHPXL)	In a case that the horizontal pixel size is odd number of the destination image, the invalid data might be generated right side in the image.
	Destination image vertical pixel size (CHnDPXL.DVPXL)	In a case that the vertical pixel size is odd number of the destination image, the invalid data might be generated bottom in the image.

38.3.2 Image Rotation/Inversion

Table 38.5 The Combination of the Bits, VMRR, HMRR, ROTL, and ROTR and the Rotation/Inversion

VMRR bit	HMRR bit	ROTL bit	ROTR bit	DAR specified point	Rotation/Inversion Performance
0	0	0	0	A	Rotation/Inversion is not performed
0	0	0	1	C	Clockwise 90 degrees rotation
0	0	1	0	B	Clockwise 270 degrees rotation
0	1	0	1	A	After rotating clockwise 90 degrees, inverse horizontally
1	0	1	0		(After rotating clockwise 270 degrees, inverse vertically)
1	0	0	1	D	After rotating clockwise 90 degrees, inverse vertically
0	1	1	0		(After rotating clockwise 270 degrees, inverse horizontally)
0	1	0	0	C	Inversing horizontally
1	0	0	0	B	Inversing vertically
1	1	0	0	D	180 degrees rotation
Others				—	Setting prohibited

The rotation/inversion performance in 90 degrees units can be executed arbitrarily effects of combination of the bits, VMRR, HMRR, ROTR, and ROTL as shown in table 38.5. Figure 38.7 shows the relations between the source image and the destination image in operating with rotation/inversion performance and Figure 38.8 shows only with inversion performance.

During the rotation/ inversion operating, the address specified point setting in CHnDAR is to be changed according to the setting of the bits, VMRR, HMRR, ROTR, and ROTL. See figure 38.9 for details on the specified address point corresponding to the processing respectively.

Lists the formulas for the address settings as follows.

offset_add	Address at the left above end of the destination image.
dest_hwidth	Horizontal byte size of the destination image (CHnDFMT.DHWTH)
dest_vpxl	Vertical pixel size of the destination image (CHnDPXL.DVPXL)

A DAR = offset_add

B DAR = offset_add + (dest_hwidth × (dest_vpxl − 1))

C DAR = offset_add + dest_hwidth

D DAR = offset_add + (dest_hwidth × dest_vpxl)

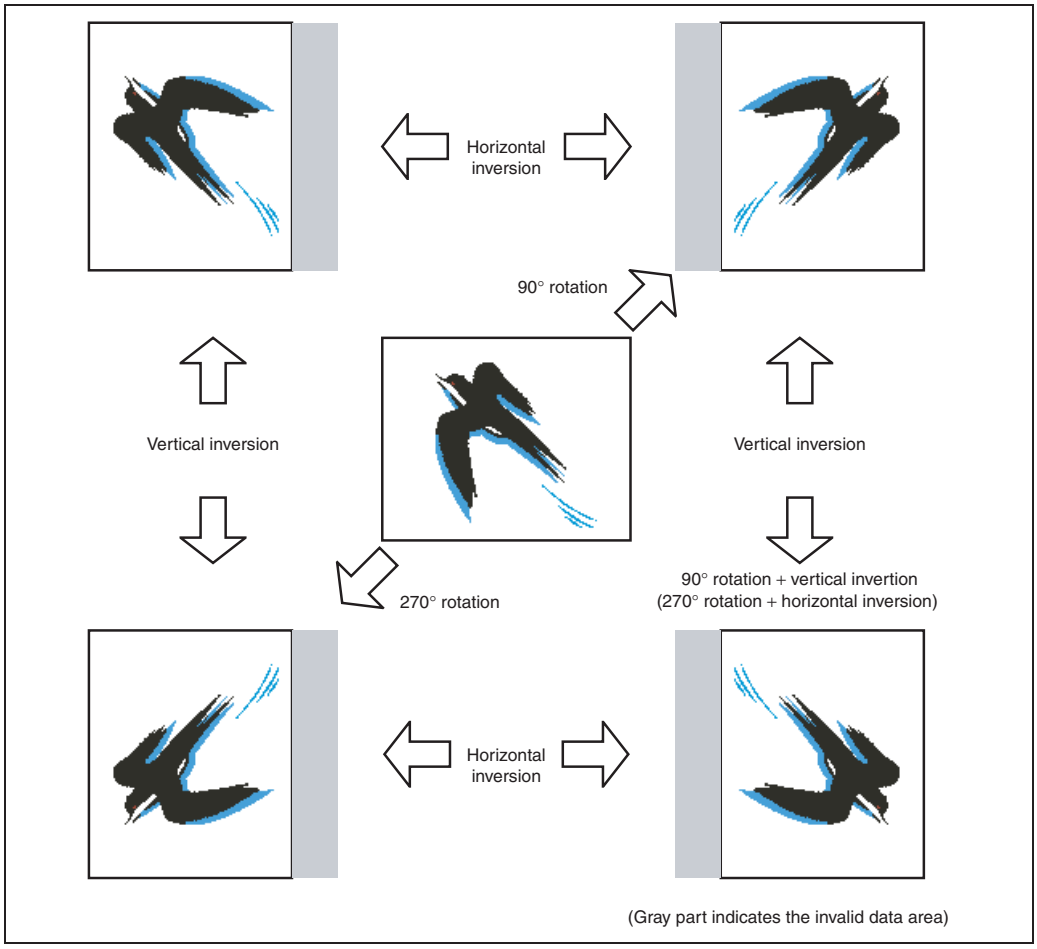


Figure 38.7 Relations between the Source Image and the Destination Image in Operating with Rotation/Inversion Performance

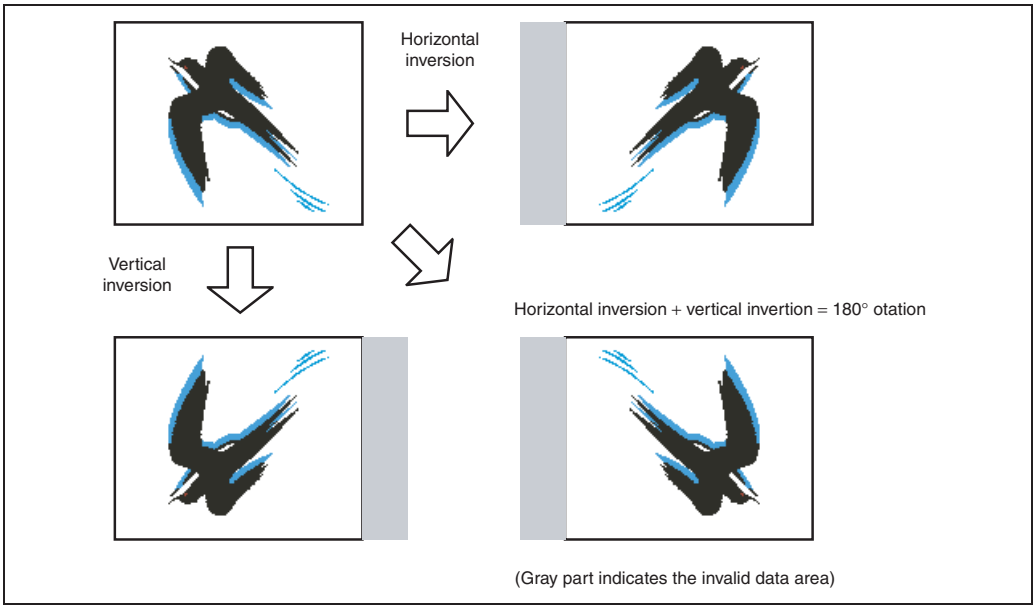


Figure 38.8 Relations between the Source Image and the Destination Image in Operating with Inversion Performance

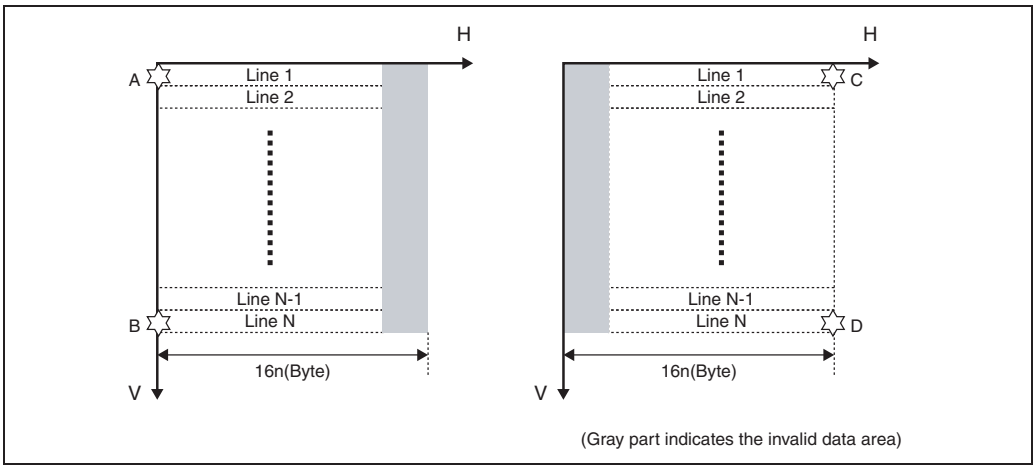


Figure 38.9 The specified Address point of CHnDAR

38.3.3 Format Conversion

Conversions are possible between RGB formats and between YCbCr formats (YCbCr4:2:0 and YCbCr4:2:2). For available RGB formats, see table 38.3. However, no format conversion is possible between RGB and YCbCr.

38.3.4 Simple Magnification

Setting the MX and MY bits in CTRL allows enlarged output in the X and Y directions respectively.

Simple magnification method is used for the magnification processing where the pixels in the source image are copied in the X and Y directions and are then output.

Figure 38.10 is a schematic diagram of simple magnification of pixels.

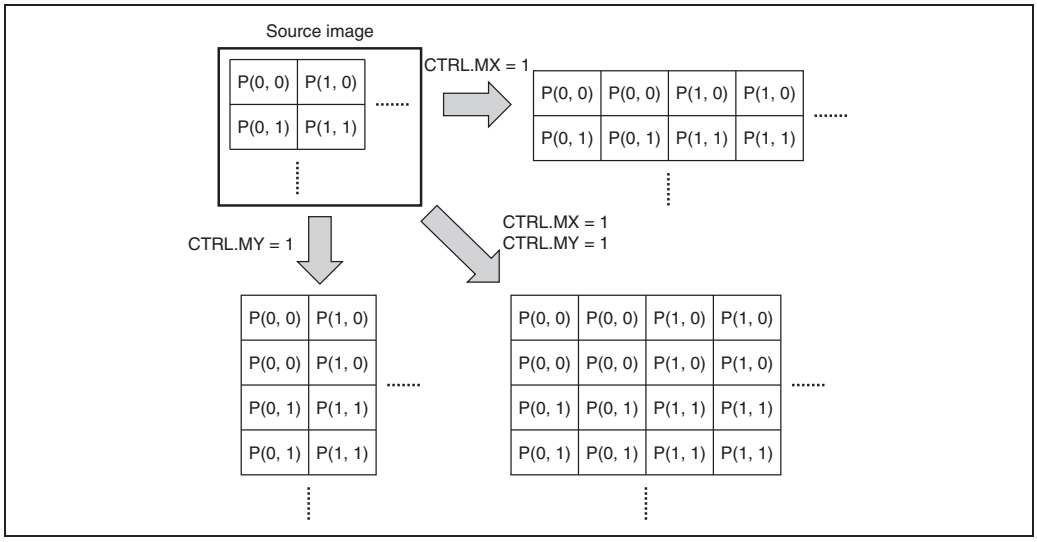


Figure 38.10 Enlarged Output of Pixels

38.4 Transfer Flow

Figure 38.11 shows a flowchart of DMAC transfer using 2D-DMAC.

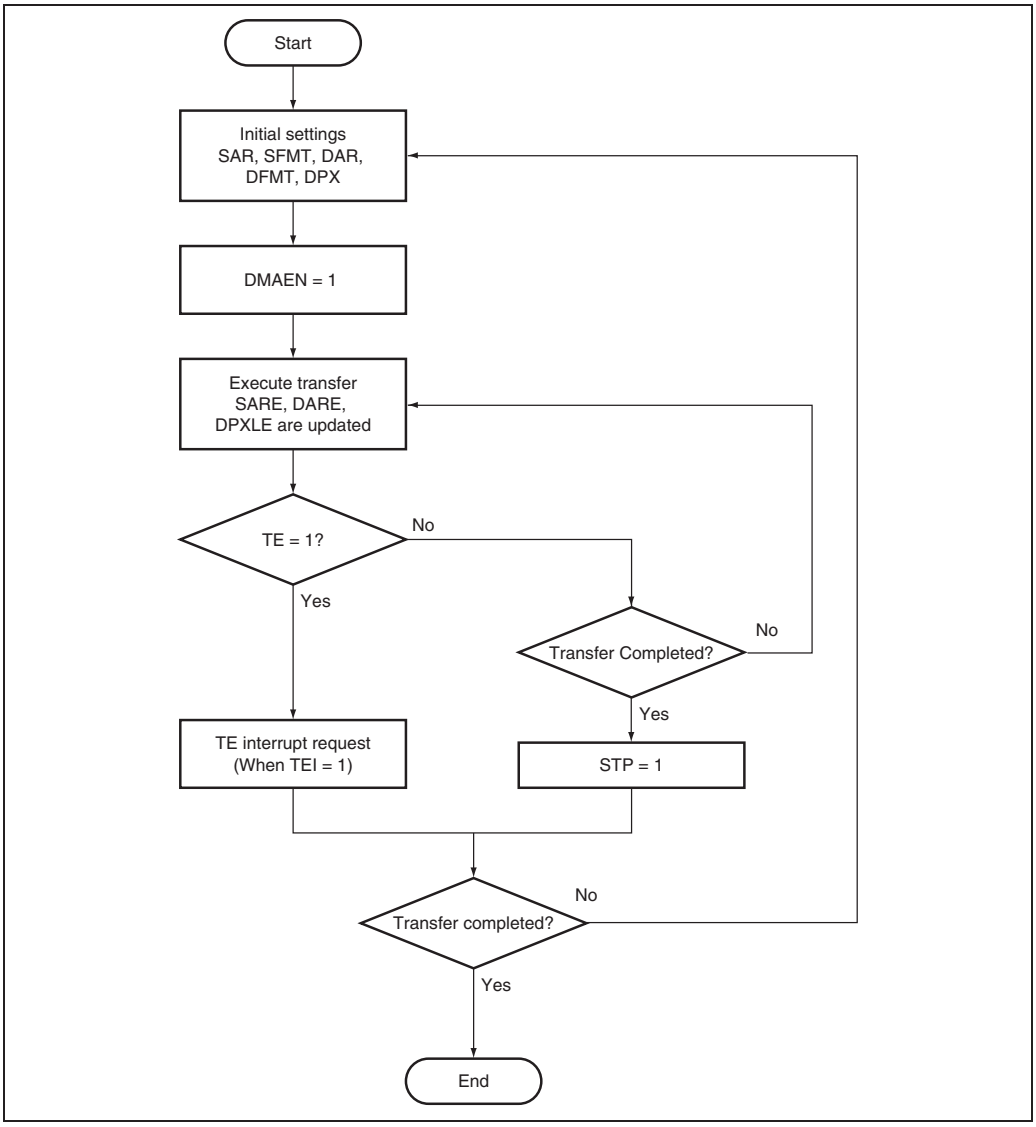


Figure 38.11 Flowchart of DMAC Transfer Using 2D-DMAC

Section 39 Media RAM (MERAM)

This LSI has a 1536-Kbyte media RAM (MERAM). Up to 32 interconnect buffers (ICB) can be defined on the MERAM. Each ICB functions as a read buffer or write buffer for transactions of an image module, and also allows data transmission/reception between image modules through the ICB. The use of ICBs enables the number of accesses to the SDRAM to be reduced and the access efficiency to be improved.

Furthermore, by combining multiple areas in the MERAM, it can be defined as a frame buffer cache. When the LCDC accesses data through the frame buffer cache, the data is cached and the second access and the following accesses are made from the MERAM, which reduces accesses to the SDRAM.

This LSI also has an LCD refresh controller, allowing to temporarily store display data, which is formerly read from the SDRAM in the refresh mode, in the MERAM and to display it on the LCD by simply performing internal bus transfer.

Accesses from the following modules are supported: CEU, CSI-RX, VEU × 4, BEU × 3, 2D-DMAC, ISP, VPU, JPU, DSI-TX × 2, LCDC × 2.

Note: 1. Set the RTMSTPCR007 bit in RTMSTPCR0 of the CPGA to 0 (operation started) in any of the following conditions:

Condition 1	When using any of those modules listed above (or accessing their registers)
Condition 2	When accessing the registers of IPMMU (I)
Condition 3	When directly accessing the MERAM as the internal memory

When all conditions 1 to 3 are not met, RTMSTPCR007 in the RTMSTPCR0 register of the CPGA can be set to 1 (stop).

2. When accessing the MERAM as the internal memory, or when using the interconnect buffer function, set the RTMSTPCR113 bit in the RTMSTPCR1 register to 0 (operation started). Otherwise, set the RTMSTPCR113 bit to 1 (operation stopped). When the LCDC0/1 accesses the MERAM in the LCD refresh mode, the RTMSTPCR113 bit may be 0 (operation started).

39.1 Features

(1) Features of Interconnect Buffers (ICB)

- Up to 32 buffers can be defined.
- Each ICB functions as a read buffer, which prefetches data from the specified area of the SDRAM and then stores the data in the buffer according to read transactions from a module. The ICB can also start reading before a transaction from the module occurs.
- Each ICB also functions as a write buffer, which receives write transactions from a module and stores them in the buffer. Whether to write data back to the SDRAM or not is selectable.
- The write buffer for a module can be used as the read buffer for another module, which allows data transfer in the MERAM. Data write to the SDRAM is also possible.

(2) Features of Frame Buffer Cache

- An area of combined ICBs can be defined as a frame buffer cache.
- Data from the frame buffer within the SRAM is supplied to the LCDC while also being used to fill the frame buffer cache. When the data doesn't change, data is simply supplied from the frame buffer to the LCDC.

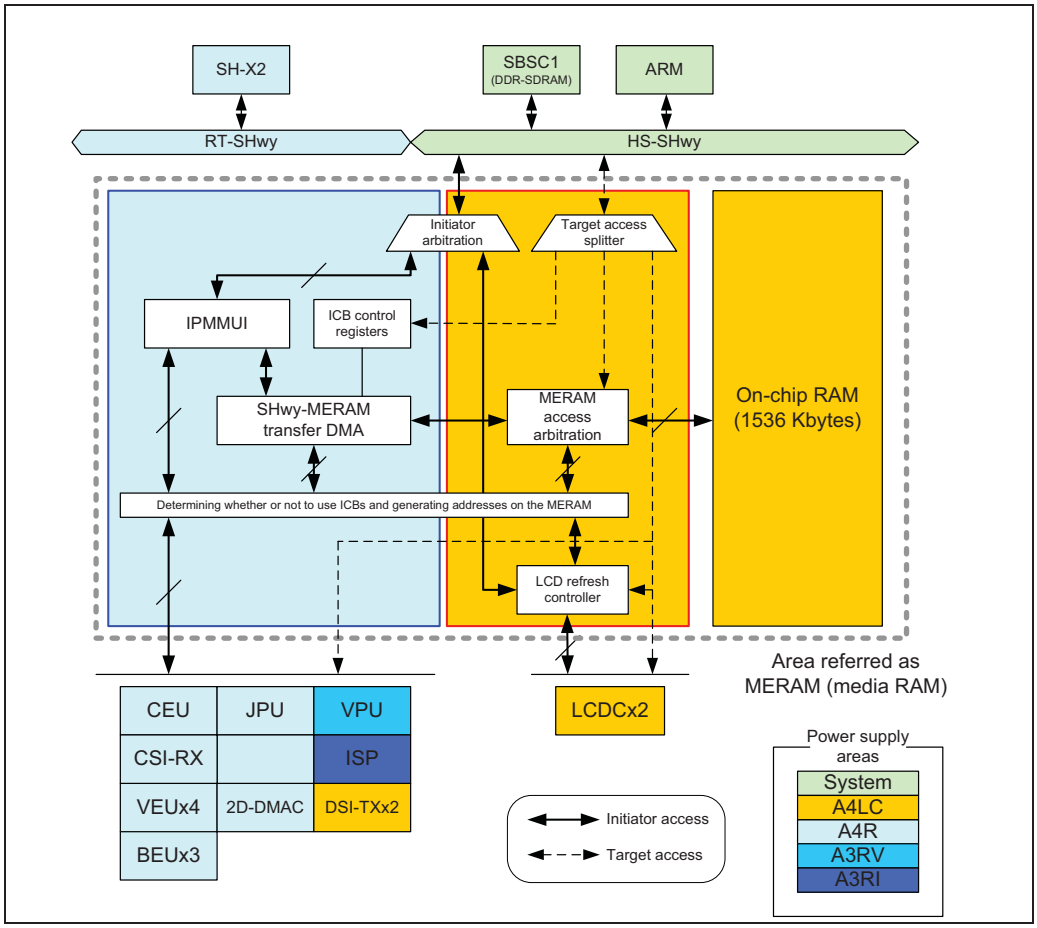


Figure 39.1 Block Diagram of MERAM and Other Modules

39.2 Register Descriptions

Table 39.1 shows the register configuration and memory configuration of the MERAM. Table 39.2 shows the register status in each processing mode.

Table 39.1 Register Configuration and Memory Configuration

Register Name	Abbreviation	R/W	Address	Access Size
ICB control register 0	MEVCR0	R/W	H'E550 0000	32
ICB control register 1	MEVCR1	R/W	H'E550 0004	32
ICB transfer end interrupt set register 0	METEIE0	R/W	H'E550 0008	32
ICB transaction error interrupt control register 0	MEILIE0	R/W	H'E550 000C	32
ICB active status register 0	MEACTST0	R/W	H'E550 0010	32
ICB transfer end status register 0	METEST0	R/W	H'E550 0014	32
ICB write transaction error status register	MEILWST	R/W	H'E550 0018	32
ICB read transaction error status register	MEILRST	R/W	H'E550 001C	32
ICB request queue priority select register 1	MEQSEL1	R/W	H'E550 0040	32
ICB request queue priority select register 2	MEQSEL2	R/W	H'E550 0044	32
Extended ICB active status register 1	MEACTST1	R/W	H'E550 0050	32
Extended ICB transaction error status register1	MEILST1	R/W	H'E550 0054	32
Extended ICB transfer end status register 1	METEST1	R/W	H'E550 0058	32
Extended ICB transfer end interrupt set register 1	METEIE1	R/W	H'E550 005C	32
Extended ICB active status register 2	MEACTST2	R/W	H'E550 0060	32
Extended ICB transaction error status register 2	MEILST2	R/W	H'E550 0064	32
Extended ICB transfer end status register 2	METEST2	R/W	H'E550 0068	32
Extended ICB transaction error interrupt set register 2	METEIE2	R/W	H'E550 006C	32
Extended ICB active status register 3	MEACTST3	R/W	H'E550 0070	32
Extended ICB transaction error status register 3	MEILST3	R/W	H'E550 0074	32
Extended ICB transfer end status register 3	METEST3	R/W	H'E550 0078	32

Register Name	Abbreviation	R/W	Address	Access Size
Extended ICB transaction error interrupt set register 3	METEIE3	R/W	H'E550 007C	32
ICB00 buffer control register	ME00CTRL	R/W	H'E550 0400	32
ICB00 frame size register	ME00BSIZE	R/W	H'E550 0404	32
ICB00 MERAM set register	ME00MCNF	R/W	H'E550 0408	32
ICB00 reserved	—	R	H'E550 040C	32
ICB00 external memory start address register A	ME00SSARA	R/W	H'E550 0410	32
ICB00 external memory start address register B	ME00SSARB	R/W	H'E550 0414	32
ICB00 external memory buffer size register	ME00SBSIZE	R/W	H'E550 0418	32
ICB00 reserved	—	R	H'E550 041C	32
ICBnn buffer control register (nn = 01 to 31)	MEnnCTRL	R/W	H'E550 0400 + H'0020 * nn	32
ICBnn frame size register (nn = 01 to 31)	MEnnBSIZE	R/W	H'E550 0404 + H'0020 * nn	32
ICBnn MERAM set register (nn = 01 to 31)	MEnnMCNF	R/W	H'E550 0408 + H'0020 * nn	32
ICBnn external memory start address register A (nn = 01 to 31)	MEnnSSARA	R/W	H'E550 0410 + H'0020 * nn	32
ICBnn external memory start address register B (nn = 01 to 31)	MEnnSSARB	R/W	H'E550 0414 + H'0020 * nn	32
ICBnn external memory buffer size register (nn = 01 to 31)	MEnnSBSIZE	R/W	H'E550 0418 + H'0020 * nn	32
Extended ICBnn buffer control register (nn = 32 to 127)	MEnnCTRL	R/W	H'E550 0400 + H'0020 * nn	32
Extended ICBnn frame size register (nn = 32 to 127)	MEnnBSIZE	R/W	H'E550 0404 + H'0020 * nn	32
Extended ICBnn MERAM set register (nn = 32 to 127)	MEnnMCNF	R/W	H'E550 0408 + H'0020 * nn	32

Register Name	Abbreviation	R/W	Address	Access Size
Extended ICBnn external memory start address register A (nn = 32 to 127)	MEnnSSARA	R/W	H'E550 0410 + H'0020 * nn	32
Extended ICBnn external memory start address register B (nn = 32 to 127)	MEnnSSARB	R/W	H'E550 0414 + H'0020 * nn	32
Extended ICBnn external memory buffer size register (nn = 32 to 127)	MEnnSBSIZE	R/W	H'E550 0418 + H'0020 *nn	32
MERAM direct access space	—	R/W	H'E558 0000 to H'E56F FFFF	8/16/32

Note: Any address from H'E800 0000 to H'E81F FFFF is also accessible as a mirror address. However, when making an access from the AP-Realtime (AP-RT) Core, only the mirror address range is accessible.

Table 39.2 Register Status in Each Processing Mode

Register Name	Power-On Reset	Module Standby	Sleep
MEVCR0	Initialized	Retained	Retained
MEVCR1	Initialized	Retained	Retained
METEIEn (n = 0 to 3)	Initialized	Retained	Retained
MEILIEn (n = 0 to 3)	Initialized	Retained	Retained
MEACTSTn (n = 0 to 3)	Initialized	Retained	Retained
METESTn (n = 0 to 3)	Initialized	Retained	Retained
MEILWST	Initialized	Retained	Retained
MEILRST	Initialized	Retained	Retained
MEILSTn (n = 1 to 3)	Initialized	Retained	Retained
MEQSEL1	Initialized	Retained	Retained
MEQSEL2	Initialized	Retained	Retained
MEnnCTRL	Initialized	Retained	Retained
MEnnBSIZE	Initialized	Retained	Retained
MEnnMCNF	Initialized	Retained	Retained
MEnnSSARA	Initialized	Retained	Retained
MEnnSSARB	Initialized	Retained	Retained
MEnnSBSIZE	Initialized	Retained	Retained

Note: nn = 00 to 127
For reset conditions, refer to section, 4.2 Reset Range in LSI Information.

39.2.1 ICBnn Control Register (MEnnCTRL)

MEnnCTRL (nn = 00 to 127) specifies operating mode of ICBnn.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	BV	BSZ[2:0]			—	MSAR[10:0]										
Initial value:	0	0	0	0	—	—	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NXT[4:0]					WD[1:0]		WS	CB	WBF	WF	RF	CM	MD[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	BV	0	R/W	Block Line processing Valid This bit is used along with the XBV bit in MEnnMCNF register to specify the unit of transfer between the external memory/corresponding image modules and the MERAM. • If the BV bit in the MEnnCTRL register is 1 and the XBV bit in the MEnnMCNF is 0: The transfer is performed in block line units that is is specified by the BSZ2 to BSZ0 bits in the MEnnCTRL register (block line transfer mode). • If the BV bit in the MEnnCTRL register and the XBV bit in the MEnnMCNF are 1: The transfer is performed in units of blocks into which the block line specified by the BSZ2 to BSZ0 bits in the MEnnCTRL register is divided by up to (2^BSZ[2:0]) horizontally (block transfer mode). • If the BV bit in the MEnnCTRL is 0: The transfer is performed in line units regardless of the setting in the BSZ2 to BSZ0 bits in the MEnnCTRL register (line transfer mode).

Bit	Bit Name	Initial Value	R/W	Description
30 to 28	BSZ[2:0]	000	R/W	Indicate the number of lines that compose a block line. The 2^BSZ2 to BSZ0 line is treated as a block line. These bits specify a block line consisting of 1, 2, 4, 8, 16, 32, 64 lines.
27	—	Undefined	R	Reserved The write value should always be 0.
26 to 16	MSAR[10:0]	H'000	R/W	Specify the start address of a memory area reserved in the MERAM in units of Kbytes (0 to 1535). Set a multiple of the number of block lines specified by bits BSZ2 to BSZ0. For the memory area size used in the MERAM, see section 39.2.3, ICBnnMERAM Set Register (MEnnMCNF).
15 to 11	NXT[4:0] (LNM[4:0])	00000	R/W	Specify the next ICB number when configuring a frame buffer cache. Setting the current buffer number indicates that the buffer is the end buffer of the frame buffer cache. The value of these bits is used only when the MD2 to MD0 bits are B'111. For details, see section 39.4.4, Settings as Frame Buffer Cache. Specify the ICB number for the connection destination in combination with MEnnMCNF.LNM[5:4] when the buffering mode has been enabled.
10, 9	WD[1:0]	00	R/W	Set B'11 in this field to use.
8	WS	0	R/W	Set B'1 in this field to use.
7	CB	0	R/W	Indicates 0 while the ICB is using register set A, and indicates 1 while the ICB is using register set B. The write value should always be 0. Unless otherwise specified with a special application example, the value of this bit will not be used.

Bit	Bit Name	Initial Value	R/W	Description
6	WBF	0	R/W	When the MD2 to MD0 bits are B'001 or B'111, this bit indicates that the data read fill operation in the ICB is completed. When the MD2 to MD0 bits are B'010 or B'011, this bit indicates that the write back operation of the ICB data is completed. The write value should always be 0. If 1 is written while the ICB is operating, the MERAM terminates the operation upon completion of the ongoing read fill or write back operation. Note: If 1 is written to this bit while the ICB is operating, the data written back to the SDRAM and the data filled into the ICB are not guaranteed. When writing 1 to this bit, also write 1 to the WF and RF bits to quit using the buffer.

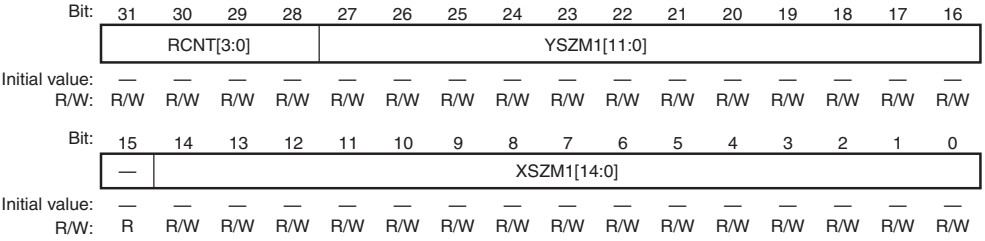
Bit	Bit Name	Initial Value	R/W	Description
5	WF	0	R/W	When the MD2 to MD0 bits are B'010, B'011, or B'100, this bit indicates that the data write operation in the ICB is completed. Upon detection of write operation end by the WD1 and WD0 bits, this bit is automatically set to 1. The write value should always be 0. If 1 is written while the ICB is operating, it is regarded that the completion of data write to the ICB has been notified. For modules that cannot automatically detect write operation end using the WD1 and WD0 bits, write 1 to this bit after receiving the operation completion of the module, and then notify manually that the data write to the ICB is completed. Setting this bit to 1 when the MD2 to MD0 bits are B'010 or B'011 starts write back operation of the data remaining in the ICB. Setting this bit to 1 when the MD2 to MD0 bits are B'011 or B'100 allows data reading up to the last line. When this bit is 1 and the following conditions are met, the use of the ICB is regarded as completed, the ACnn bit in MEACTST is negated, and the TEnn bit in METEST is set to 1. At the same time, the WBF, WF, and RF bits are cleared. [Conditions] When MD2 to MD0 = B'010: The WBF bit is 1 (write back completed). When MD2 to MD0 = B'011: The WBF bit is 1 (write back completed) and the RF bit is 1 (read operation completed). When MD2 to MD0 = B'100: The RF bit is 1 (read operation completed). Note: Even if an address with an offset (line N) has been written as the start address, data including line 0 to N is written back when operation is completed.

Bit	Bit Name	Initial Value	R/W	Description
4	RF	0	R/W	When the MD2 to MD0 bits are B'001, B'011, or B'100, this bit indicates that the data read operation in the ICB is completed. Upon detection of data read completion by the RCNT3 to RCNT0 bits in MEnnBSIZE, this bit is automatically set to 1. The write value should always be 0. If 1 is written while the ICB is operating, it is regarded that the completion of data read from the ICB has been notified. For modules that cannot automatically detect read operation end using the RCNT3 to RCNT0 bits in MEnnBSIZE, write 1 to this bit after receiving the operation completion of the module, and then notify that the data read from the ICB is completed. When this bit is 1 and the following conditions are met, the use of the ICB is regarded as completed, the ACnn bit in MEACTST is negated, and the TEnn bit in METEST is set to 1. At the same time the WBF, WF, and RF bits are cleared. [Conditions] When MD2 to MD0 = B'001: The WBF bit is 1 (read fill completed). When MD2 to MD0 = B'011: The WBF bit is 1 (write back completed) and the WF bit is 1 (write operation completed). When MD2 to MD0 = B'100: The WF bit is 1 (write operation completed). When MD2 to MD0 = B'111: The WBF bit is 1 (read fill completed).

Bit	Bit Name	Initial Value	R/W	Description
3	CM	0	R/W	Consecutive address mode. Specify how addresses are converted to line numbers and in-line offsets. For details, see section 39.3, Making Access to MERAM. 0: XSZM1 in MEnnBSIZE<4096: Bit 11 to bit 0 of the address indicate the in-line offset, and the bits after bit 12 indicate the line number. 4096<=XSZM1 in MEnnBSIZE: Bit 14 to bit 0 of the address indicate the in-line offset, and the bits after bit 15 indicate the line number. 1: XSZM1 in MEnnBSIZE<1024: Bit 9 to bit 0 of the address indicate the in-line offset, and the bits after bit 10 indicate the line number. 1024<=XSZM1 in MEnnBSIZE<2048: Bit 10 to bit 0 of the address indicate the in-line offset, and the bits after bit 11 indicate the line number. 2048<=XSZM1 in MEnnBSIZE<4096: Bit 11 to bit 0 of the address indicate the in-line offset, and the bits after bit 12 indicate the line number. 4096<=XSZM1 in MEnnBSIZE<8192: Bit 11 to bit 0 of the address indicate the in-line offset, and the bits after bit 13 indicate the line number. Note: When CM in MEnnCTRL is 1, set XSZM1 in MEnnBSIZE to less than 8192.
2 to 0	MD[2:0]	000	R/W	Specify ICBnn usage mode. 000: No ICB is used. 001: Read buffer mode 010: Write buffer mode 011: Interconnect buffer (with write back) mode* 100: Interconnect buffer (without write back) mode* 111: Frame buffer cache mode** Note: In block transfer mode, setting other than the read buffer mode and write buffer mode is prohibited. * When using the interconnect buffer mode with extended ICBs, enable the buffering mode. ** Setting prohibited when the extended ICB function is enabled.

39.2.2 ICBnn Frame Size Register (MEnnBSIZE)

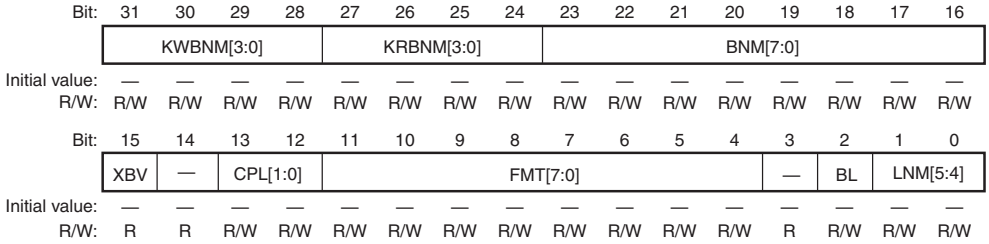
MEnnBSIZE (nn = 00 to 127) specifies the size of the frame buffer corresponding to ICBnn.



Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	Undefined	R	Reserved The write value should always be 0.
28 to 16	YSZM1 [12:0]	Undefined	R/W	Specify the number of lines -1 (nn = 00 to 31: 0 to 4095, nn = 32 to 127: 8192) of the frame buffer corresponding to ICBnn (nn = 00 to 127).
15	—	Undefined	R	Reserved The write value should always be 0.
14 to 0	XSZM1 [14:0]	Undefined	R/W	Specify the actual data size -1 in units of bytes (0 to 32767 bytes) in one line of the frame buffer corresponding to ICBnn (nn = 0 to 127). Note: When CM in MEnnCTRL is 1, set XSZM1 in MEnnBSIZE to less than 8192.

39.2.3 ICBnn MERAM Set Register (MEnnMCNF)

MEnnMCNF (nn = 00 to 127) is used for settings of buffer areas in the MERAM used by ICBnn.



Bit	Bit Name	Initial Value	R/W	Description
31 to 28	KWBNM [3:0]	Undefined	R/W	Specify the number of lines to be retained during writing when the MD2 to MD0 bits in MEnnCTRL are B'010, B'011, or B'100. • Specify the number of lines in units of block lines specified by the BSZ2 to BSZ0 bits in MEnnCTRL, and the number of lines to be retained during writing is treated as (KWBNM3 to KWBNM0 +1) << BSZ2 to BSZ0 in MEnnCTRL. • When the MERAM detects data write to line n, it determines that the data on the line (n - number of lines retained during writing) is fixed, and no more data writing to the line (n - number of lines retained during writing) is generated. Note: The value of these bits depends on the characteristics or operation settings of associated modules. For details, see section 39.5, Setting for Each Associated Module.

Bit	Bit Name	Initial Value	R/W	Description
27 to 24	KRBNM [3:0]	Undefined	R/W	Specify the number of lines to be retained during reading when the MD2 to MD0 bits in MEnnCTRL are B'001, B'011, B'100, or B'111. • Specify the number of lines in units of block lines specified by the BSZ2 to BSZ0 bits in MEnnCTRL, and the number of lines to be retained during reading is treated as (KRBNM3 to KRBNM0 +1) << BSZ2 to BSZ0 in MEnnCTRL. • When the MERAM detects data read on line n, it determines that the data on the line (n - number of lines retained during reading) can be released, and no more data reading on the line (n - number of lines retained during reading) is generated. Note: The value of these bits depends on the characteristics or operation settings of associated modules. For details, see section 39.5, Setting for Each Associated Module.

Bit	Bit Name	Initial Value	R/W	Description
23 to 16	BNM[7:0]	Undefined	R/W	• Line transfer mode, block line transfer mode: Specify the number of lines to be secured in the MERAM. (Lines of the set number +1 are secured.) Specify the number of lines irrespective of the value of the BSZ2 to BSZ0 bits in MEnnCTR. Secure at least the following number of lines. MD = B'001: (Number of lines retained during reading +1: Number of block lines) MD = B'010: (Number of lines retained during writing +1: Number of block lines) MD = B'011, B'100: (Number of lines retained during writing + number of lines retained during reading +1: Number of block lines) MD = B'111: See the following, (1) Calculating Memory Area Reserved in the MERAM. • Block transfer mode: Specify the number of lines to be secured in the MERAM. (Lines of the set number +1 are secured.) Secure at least the following number of lines. MD = B'001: (Number of lines retained during reading +1: Number of block lines) MD = B'010: (Number of lines retained during writing +1: Number of block lines) When YC combining mode is enabled, the number of lines actually secured for the value set by the above-mentioned is YCbCr420: (BNM+1) x 1.5 YCbCr422: (BNM+1) x 2 YCbCr444: (BNM+1) x 3 Please set for (BNM+1) to become an even number for YCbCr420
15	XBV	Undefined	R/W	• Block transfer mode: When both bits, MEnnCTRL.BV and MEnnCTRL.XBV are set to 1, a transfer is performed in every block between the external memory and the MERAM, and also the associated image module and the MERAM. (block transfer mode)

Bit	Bit Name	Initial Value	R/W	Description
14	—	Undefined	R	Reserved The write value should always be 0.
13, 12	CPL[1:0]	Undefined	R/W	YC combining mode When MEnnMCNF.CPL ! = B'00, the values of MEnnSSARA and MEnnSSARB are used as the Y surface address and the C surface address, respectively, to perform transfer in which these surfaces are linked. 00: This mode is not used. 01: YCbCr444 10: YCbCr420 11: YCbCr422
11 to 4	FMT[7:0]	Undefined	R/W	Data packed format Specify the data packed format in the external memory for performing transfer in the YC combining mode. Refer to tables 39.3 and 39.4 for the planar format and packed format, respectively. FMT[7:5] Specify the format for YCbCr data. 000: Semi-planar format 010: Planar-Padding format 011: Planar-Fitting format 100, 101: Packed format Other settings: Prohibited. FMT[4] Exchange the data position of Cb for that of Cr. 0: No effects 1: Exchange the data position of Cb for that of Cr FMT[5], FMT[3:2] Specify the packed format when the packed format mode is selected. FMT[1:0] Reserved The write value shoud always be 0.

Bit	Bit Name	Initial Value	R/W	Description
3	—	Undefined	R	Reserved The write value should always be 0.
2	BL	Undefined	R/W	Buffering mode Must be set when two different ICBnns are used for interconnection. Set this bit to 0 other than when the MD values for these two ICBnns are set to 'B011 or 'B100.
1, 0	LNM[5:4]	Undefined	R/W	Specify the ICB number for the connection destination in combination with MEnnCTRL.LNM[3:0] when the buffering mode has been enabled.

(1) Calculating Memory Area Reserved in the MERAM

The memory area in the MERAM is used as follows:

- Line transfer mode:
  Unit of area used for buffer (KB) = value rounded up (MEnnBSIZE.XSZM1[14:0]+1) to the nearest 2^n KB (including 1 KB)
  Total size of area used for buffer (KB) = (unit of area used for buffer) × (MEnnMCNF.BNM[7:0]+1)
- Block line transfer mode:
  Unit of area used for buffer (KB) = value rounded up (MEnnBSIZE.XSZM1[14:0]+1) to the nearest 2^n KB (including 1 KB) × 2^MEnnCTRL.BSZ[2:0]
  Total size of area used for buffer (KB) = (unit of area used for buffer) × ((MEnnMCNF.BNM[7:0]+1)/(2^MEnnCTRL.BSZ[2:0]))
- Block transfer mode:
  Unit of area used for buffer (KB) = value rounded up (MEnnBSIZE.XSZM1[14:0]+1) to the nearest 2^n KB (including 1 KB) × 2^MEnnCTRL.BSZ[2:0]/MEnnCTRL.BSZ[2:0]
  Total size of area used for buffer (KB) = (unit of area used for buffer) × (MEnnMCNF.BNM[7:0]+1)

  When YCbCr dual transfer mode is enabled, the following memory area is used.

  YCbCr420 : Total size of area used for buffer (KB) = (the size of area calculated for Y data) × 1.5

  YCbCr422 : Total size of area used for buffer (KB) = (the size of area calculated for Y data) × 2

  YCbCr444 : Total size of area used for buffer (KB) = (the size of area calculated for Y data) × 3

When ICBnn is defined the amount of memory area calculated as "Total size of area used for buffer" above which begins with the start address specified by the MSAR10 to MSAR0 bits in MEnnCTRL is secured. Since no detection is performed with respect to whether or not the memory area overlaps with the memory area secured by another ICB, write a multiple of the "total size of area used for buffer" value to the MSAR10 to MSAR0 bits to avoid such an overlap.

Note: Specify a value so that the total number of "lines secured in the MERAM","lines held during reads", and "lines held during writes" is less than 256.

(2) Data Packed Format on External Memory in YC Combining Mode

When YCbCr-format image data is transferred from the external memory to the MERAM via an ICB for which the YC combining mode has been enabled, the format specified in MEnnMCNF.FMT is converted into the semi-planar format that can be processed in image modules, before the data is stored in MERAM. Also, when data is transferred from the MERAM to the external memory via an ICB for which the YC combining mode has been enabled, the semi-planar format of the data stored in the MERAM is converted into the format specified in MEnnMCNF.FMT.

- Semi-planar format

  In this format, Y and CbCr are stored at different addresses. The start addresses of the Y data and the CbCr data must be specified in MEnnSSARA and MEnnSSARB, respectively.
- Planar-Padding format

  In this format, Y, Cb, and Cr are stored at different addresses. The start addresses of the Y data and the Cb data must be specified in MEnnSSARA and MEnnSSARB, respectively. The Cr data is placed from the end of the Cb data, and the start address, SSARC, is calculated using the following expressions:

  YCbCr420 : SSARC = MEnnSSARB + (MEnnSSARB - MEnnSSARA) / 2

  YCbCr422, 444 : SSARC = MEnnSSARB + (MEnnSSARB - MEnnSSARA)
- Planar-Fitting format

  In this format, Y data, Cb data, and Cr data are stored at different addresses. The start addresses of the Y data and the Cb data must be specified in MEnnSSARA and MEnnSSARB, respectively. The Cr data is placed from the end of each line of the Cb data, and the start address, SSARC, is calculated using the following expressions:

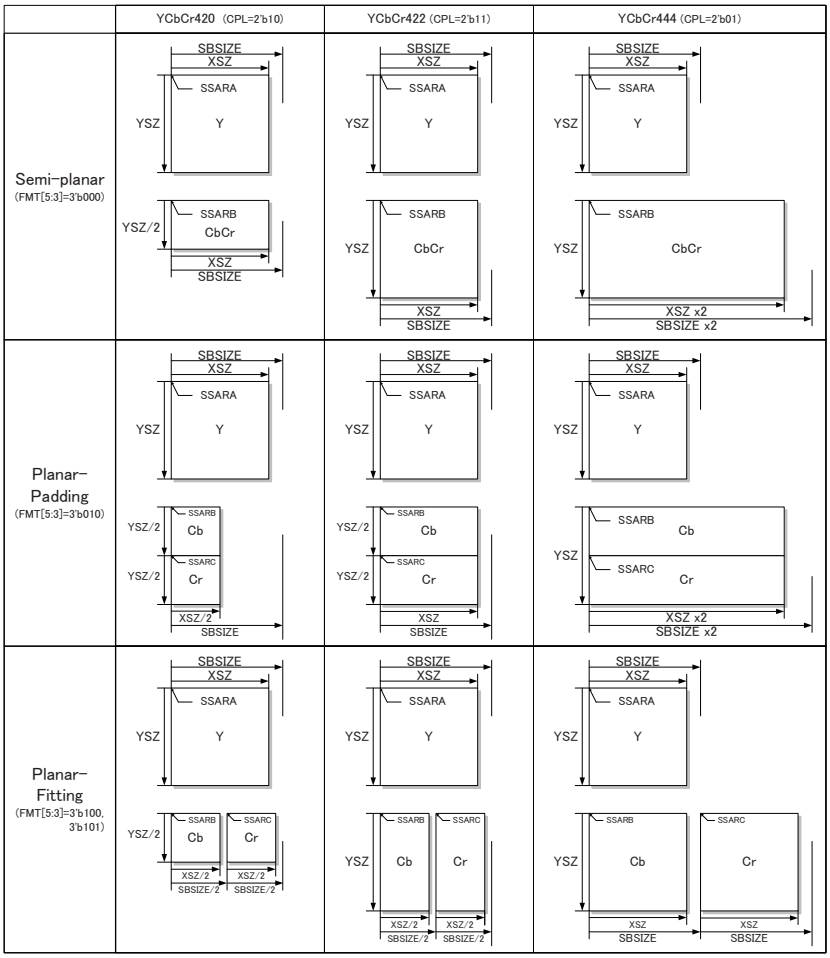
  YCbCr420,422 : SSARC = MEnnSSARB + MEnnSBSIZE / 2

  YCbCr444 : SSARC = MEnnSSARB + MEnnSBSIZE

  Table 39.3 shows the method of storing data in the planar formats.
- Packed format

In this format, Y, Cb, and Cr are packed on a pixel basis and stored at a single address. Table 39.4 shows the corresponding packed format.

Table 39.3 YCbCr Planar Format



XSZ = MEnnBSIZE.XSZM1 + 1, YSZ = MEnnBSIZE.YSZM1 + 1
SSARA = MEnnSSARA, SSARB = MEnnSSARB, SBSIZE = MEnnSBSIZE.SBSIZE
SSARC = SSARB + (SSARB - SSARA) / 2 [YCbCr420, Planar-Padding],
SSARB + SSARB - SSARA [YCbCr422, YCbCr444, Planar-Padding],
SSARB + SBSIZE/2 [YCbCr420, YCbCr422, Planar-Fitting]

SSARB + SBSIZE [YCbCr444, Planar-Fitting]

Note: When FMT[4] has been set to 1'b1, the data position of Cb is exchanged for that of Cr.

Table 39.4 Packed Format for YCbCr

	FMT[5], FMT[3:2]	Phase	Bit			
			31 to 24	23 to 16	15 to 8	7 to 0
YCbCr444 (CPL = 2'b01)	000	0	Y0	Cb0	Cr0	Y1
		1	Cb1	Cr1	Y2	Cb2
		2	Cr2	Y3	Cb3	Cr3
	001	0	Cb0	Y0	Cr0	Cb1
		1	Y1	Cr1	Cb2	Y2
		2	Cr2	Cb3	Y3	Cr3
	010	0	Cb0	Cr0	Y0	Cb1
		1	Cr1	Y1	Cb2	Cr2
		2	Y2	Cb3	Cr3	Y3
YCbCr420 (CPL = 2'b10)	000	–	Y0	Y1	Cb0	Cr0
	001	–	Cb0	Y0	Y1	Cr0
	010	–	Cb0	Cr0	Y0	Y1
	100	–	Y0	Cb0	Y1	Cr0
	110	–	Cb0	Y0	Cr0	Y1
YCbCr422 (CPL = 2'b11)	000	0	Y0	Y1	y0	y1
		1	Cb0	Cr0	Y2	Y3
		2	y2	y3	Cb2	Cr2
	010	0	Cb0	Cr0	Y0	Y1
		1	y0	y1	Cb2	Cr2
		2	Y2	Y3	y2	y3
	100	0	Y0	Y1	Cb0	y0
		1	y1	Cr0	Y2	Y3
		2	Cb2	y2	y3	Cr2
	101	0	Cb0	Y0	Y1	Cr0
		1	y0	y1	Cb2	Y2
		2	Y3	Cr2	y2	y3
	110	0	Y0	Cb0	Y1	y0
		1	Cr0	y1	Y2	Cb2
		2	Y3	y2	Cr2	y3

The capital letter Y and small letter y in YCbCr422 indicate Y data of the upper-layer pixels and the lower-layer pixels, respectively.

Note: When FMT[4] has been set to 1'b1, the data position of Cb is exchanged for that of Cr.

39.2.4 ICBnn External Memory Start Address Register A (MEnnSSARA)

MEnnSSARA (nn = 00 to 127) indicates the start address of the frame buffer (register set A) corresponding to ICBnn in the external memory. The value of the SSARA bits must be a multiple of 16.

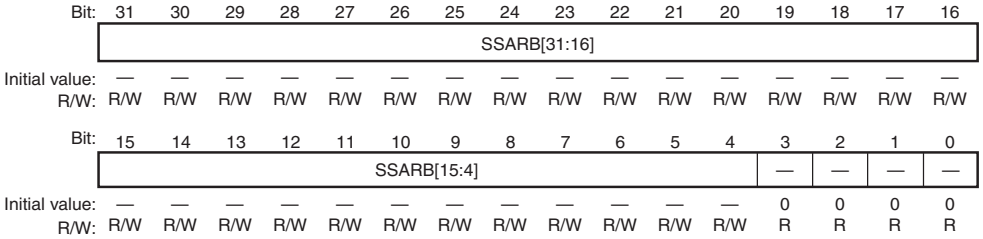
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SSARA[31:16]															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SSARA[15:4]												—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	SSARA [31:4]	Undefined	R/W	Indicate the start address (in 16-byte units) of the frame buffer (register set A) corresponding to ICBnn (nn = 0 to 127) in the external memory. In YCbCr dual transfer mode, indicate the start address of Y data.
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

39.2.5 ICBnn External Memory Start Address Register B (MEnnSSARB)

MEnnSSARB (nn = 00 to 127) indicates the start address of the frame buffer (register set B) corresponding to ICBnn in the external memory. The value of the SSARB bits must be a multiple of 16.



Bit	Bit Name	Initial Value	R/W	Description
31 to 4	SSARB [31:4]	Undefined	R/W	Indicate the start address (in 16-byte units) of the frame buffer (register set B) corresponding to ICBnn (nn = 0 to 127) in the external memory. In YCbCr dual transfer mode, indicate the start address of C data.
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

39.2.6 ICBnn External Memory Buffer Size Register (MEnnSBSIZE)

MEnnSBSIZE (nn = 00 to 127) indicates the one-line width of the frame buffer corresponding to ICBnn in the external memory in units of bytes. The one-line width must be a multiple of 8.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	HDV	HSZ[2:0]			—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SBSIZE[15:4]												—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	HDV	0	R/W	Horizontally-Divided Access setting This bit is valid when the BV bit in the MEnnCTRL register is 1. It allows transfer between a block line or block in the MERAM and the external memory to be performed in units of blocks into which the block line or block is divided horizontally with the size specified by the HSZ2 to HSZ0 bits. If the destination external memory space is specified for T-L conversion by the IPMMU(I), set the HSZ2 to HSZ0 bits to the same horizontal size as the one of a block in the external memory. If these settings do not match, transfer is not performed normally.
30 to 28	HSZ[2:0]	000	R/W	Indicate the horizontal division unit in horizontally-divided access setting. 000: 16 bytes 001: 32 bytes 010: 64 bytes 011: 128 bytes Others: Setting prohibited
27 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
15 to 4	SBSIZE [15:4]	Undefined	R/W	Indicate the one-line width (in 16-byte units) of the frame buffer.
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

39.2.7 ICB Control Register 0 (MEVCR0)

MEVCR0 is a 32-bit read-only register for the future extension. Data write to this register is prohibited.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	—	All 0	R	Reserved Data write to this register is prohibited.

39.2.8 ICB Control Register 1 (MEVCR1)

MEVCR1 initializes ICBs and controls direct writing to the flag registers.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RST	WD	AMD	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	RST	0	R/W	ICB Reset When this bit is set to 1, all ICBs are initialized, and then this bit is automatically cleared. Reset all the modules using an ICB, and then set this bit to 1. Use this bit when an error occurs in the software program that uses an ICB.
30	WD	0	R/W	Write Direction When writing to MEACTSTn, METESTn, MEILWST, or MEILRST, MEILSTn, the bits to which 1 has been written are cleared usually. But when this bit is set to 1, the bits to which 1 has been written are set.
29	AMD1	0	R/W	Address Mode Switch 0: The ICB function is used when the addresses from modules are within H'80000000 to H'BFFF FFFF. 1: The ICB function is used when the addresses from modules are within H'C0000000 to H'DFFF FFFF. For details, see section 39.3, Making Access to MERAM.

Bit	Bit Name	Initial Value	R/W	Description
28	AMD0	0	R/W	Extended ICB Enable 0: The addresses H'E000 0000 to H'EFFF FFFF are output on the SHwy. 1: The extended ICB function is used when the addresses from modules are within H'E0000000 to H'EFFF FFFF. For details, see section 39.3, Making Access to MERAM.
28 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

39.2.9 ICB Transfer End Interrupt Set Register n (METEIEn)

METEIEn (n = 0 to 3) controls interrupt requests made by the transfer end flag (TEnn bits in METEST) of each ICB (nn = 00 to 127).

For modules that cannot detect a write operation, when the WF bit in MEnnCTRL is manually set to 1, the MERAM can wait until the write back operation ends using this interrupt function.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TInn															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TInn															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	TInn (n = 0: nn = 00 to 31 N = 1: nn = 32 to 63 N = 2: nn = 64 to 95 N = 3: nn = 96 to 127)	H'0000 0000	R/W	When any of the TInn (nn = 00 to 127) bits is set to 1, an interrupt occurs while the ICB transfer end flag (TEnn) in METESTn is 1. After an interrupt occurs, it can be canceled by clearing the TEnn flag or the Tinn bits in this register.

39.2.10 ICB Transaction Error Interrupt Set Register n (MEILIEn)

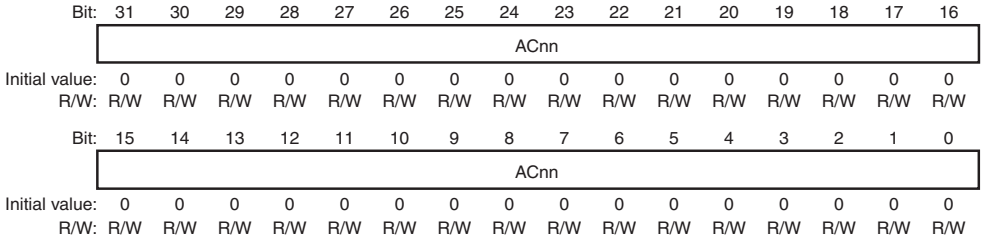
MEILIEn (n = 0 to 3) controls interrupt requests made by the error status flag (IWnn in MEILWST, IRnn in MEILRST, and IWRnn in MEILSTn) of each ICB (nn = 00 to 127). For error status conditions, see the descriptions on the MEILWST and MEILRST and MEILSTn registers.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IInn															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IInn															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	IInn (n = 0: nn = 00 to 31 n = 1: nn = 32 to 63 n = 2: nn = 64 to 95 n = 3: nn = 96 to127)	H'0000 0000	R/W	When any of these bits (nn = 00 to 127) is set to 1 and the error end flag (IWnn or IRnn or IWRnn) of each ICB in MEILWST or MEILRST or MEILST is 1, an interrupt occurs. An interrupt is generated by the flag on the write side or read side. After an interrupt occurs, it can be canceled by clearing the IWnn and IRnn and IWRnn flags or clearing the corresponding IInn bits in this register.

39.2.11 ICB Active Status Register n (MEACTSTn)



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	ACnn (n = 0: nn = 00 to 31 n = 1: nn = 32 to 63 n = 2: nn = 64 to 95 n = 3: nn = 96 to 127)	H'0000 0000	R/W	Indicate that ICBnn (nn = 00 to 127) is in use. When 1 is written to this register while the WD bit in MEVCR1 is 0, the bits to which 1 has been written are cleared and the other bits remain unchanged. When 1 is written to this register while the WD bit in MEVCR1 is 1, the bits to which 1 has been written are set to 1 and the other bits remain unchanged.

(1) State Transitions of ICBnn

The ACnn bits (nn = 00 to 127) indicate that ICBnn (nn = 00 to 127) is in use.

When a transaction occurs successfully from an associated module to ICBnn, the ACnn bit is set to 1 and the ICBnn becomes active.

The active ICBnn must be driven to inactive mode upon completion of processing for one plane. The completion of processing for one plane means the following.

- When MD = B'001 or B'111: The WBF and RF bits in MEnnCTRL are 1.
  The RF bit indicates that the read operation of the module using ICBnn is completed. WBF = 1 shows that the read fill operation for ICBnn is completed up to the last line.

- When MD = B'010: The WBF and WF bits in MEnnCTRL are 1.
  The WF bit indicates that the write operation of the module using ICBnn is completed. WBF = 1 shows that the write back of the data written to ICBnn to the external memory is completed up to the last line.
- When MD = B'011: The WBF, WF, and RF bits in MEnnCTRL are 1.
- When MD = B'100: The WF and RF bits in MEnnCTRL are 1.

When the processing for one plane of ICBnn is completed, the WBF, WF, and RF bits in MEnnCTRL are cleared and the corresponding bit (TEnn) in METESTn is set to 1. At the same time, the corresponding bit (ACnn) in MEACTSTn is cleared and ICBnn enters inactive mode.

The WF and RF bits can be set by manually writing 1 to the WF and RF bits of all active ICBnn when the end interrupt of the associated module occurs. Do not set the WBF bit to 1 to avoid discontinuation of write back operation.

Furthermore, the function to automatically detect the completion of processing for one plane is available for each write and read operation in some cases. For details of the function, see the descriptions on the WD1 and WD0 bits in MEnnCTRL, the WS bit in MEnnCTRL, and the RCNT3 to RCNT0 bits in MEnnBSIZE, and also see section 39.5, Settings for Each Associated Module. When the auto-detect function is available, the WF and RF bits in MEnnCTRL are automatically set to 1 by the execution of the last transaction in the write or read operation, which does not require manual setting.

ICBnn that returns to inactive mode can deal with the next-plane transaction sent from the associated module. If the next-plane transaction is generated while ICBnn is active, a transaction error occurs usually. But the processing can be continued in the following cases.

- When the register set A/register set B specification of a transaction to ICBnn differs from the register set A/register set B indication of the active ICBnn
- When the register set A/register set B specification of a transaction to ICBnn matches the register set A/register set B indication of the active ICBnn, but the transaction line number is 0 and the transaction processing to the last line is already completed and line 0 is not included in the lines to be retained during reading/writing

With these conditions, an occurrence of this transaction is regarded as the completion of use of ICBnn, and therefore the completion processing starts automatically. In the case of a read transaction, the MERAM sets the RF bit in one or two buffers that the module is using for read operation, waits until the buffers become inactive, and then processes the generated transaction. In the case of a write transaction, the MERAM sets the WF bit in one or two buffers that the module is using for write operation, waits until the buffers become inactive, and then processes the generated transaction.

Note: Two or more ICBs are available for reading in the BEU, for reading/writing in the 2D-DMAC. But the completion processing for an ICB used for another purpose may be performed upon occurrence of the next-plane transaction to an ICBnn. For this reason, this function is not available when using two or more ICBs for each read and write operation of the associated module.

When a transaction error is detected, the corresponding bits (IWnn/IRnn/IWRnn) in MEILWST, MEILRST, and MEILSTn are set to 1 and the corresponding bit (ACnn) in MEACTSTn is negated. For transaction errors, see the descriptions on the MEILWST, MEILRST, and MEILSTn registers.

(2) Writing to Register for Active ICB

When writing data to MEACTSTn, the AC bits corresponding to the bits to which 1 has been written are usually negated. When the WD bit in MEVCR1 is 1, the AC bits corresponding to the bits to which 1 has been written are set. Unless otherwise specified with a special application example, the AC bits need not be controlled by writing to this register.

While ACnn is 1, writing to the set register of ICBnn is made as follows:

- During the MEnnCTRL write operation, only writing 1 to the WBF, WF, and RF bits is effective and the other bits remain unchanged. When 0 is written to all the WBF, WF, and RF bits, every bit remains unchanged, but the set register of ICBnn is reevaluated, the buffers are restarted, and the read fill operation is started in advance.

  For restarting the buffers, see the description on clearing the error flag in MEILRST and restarting. For starting the read fill operation in advance of this, see (3) Starting Read Fill Operation in Advance.
- Writing to other set registers of ICBnn is possible, but only the register on the opposite plane from the register (MEnnSSARA or MEnnSSARB) specified by the CB bit in MEnnCTRL can be modified. The other registers should not be modified.

(3) Starting Read Fill Operation in Advance

When the MD2 to MD0 bits in MEnnCTRL is B'001, the read fill operation to the MERAM is started after a read transaction is generated from a module to ICBnn and then the ACnn bit in MEACTSTn is set to 1. Starting the read fill operation before such a read transaction occurs is made possible by the following procedure.

1. Set ICBnn.
2. Set the ACnn bits in MEACTSTn manually with the WD bit in MEVCR1 set to 1.
3. Write 0 to all bits in MEnnCTRL.

Since the ACnn bit in MEACTSTn is 1, no data is written to MEnnCTRL, but the read fill operation is started by reevaluating the ICBnn setting.

Note: When using ICBnn for the first time, write H'00000000 at addresses of MEnnCTRL + H'0C and MEnnCTRL + H'1C in step 1.

39.2.12 ICB Transfer End Status Register n (METESTn)

The TEnn bit (nn = 00 to 127) in this register indicates that the processing for one plane of ICBnn (nn = 00 to 127) is completed.

For the definition of the completion of processing for one plane of ICBnn, see the descriptions on the WF and RF bits in MEnnCTRL.

In writing to METEST, the TE bits corresponding to the bits to which 1 has been written are usually negated. When the WD bit in MEVCR1 is 1, the TE bits corresponding to the bits to which 1 has been written are set.

When the interrupt function of METEIEn is used and an interrupt occurs, clear the bit that generated the interrupt. When the interrupt function is not used, the Tenn bit needs not be cleared.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TEnn															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TEnn															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	TEnn (n = 0: nn = 00 to 31 n = 1: nn = 32 to 63 n = 2: nn = 64 to 95 n = 3: nn = 96 to 127)	H'0000 0000	R/W	Indicate that the processing for one plane of ICBnn (nn = 00 to 127) is completed. The bits in this register to which 1 has been written are cleared.

39.2.13 ICB Write Transaction Error Status Register (MEILWST)

The IWnn bit (nn = 0 to 31) indicates that an unprocessable write transaction to ICBnn (nn = 0 to 31) has occurred. When this bit is set to 1, the ACnn bit in MEACT0 is negated. A write transaction error occurs under the following conditions.

Conditions for write transaction error:

- When a write transaction occurs to ICBnn for which the MD2 to MD0 bits in MEnnCTRL are set to B'000
- When a write transaction occurs to ICBnn in which a read transaction error or write transaction error has already occurred (IRnn bit in MEILRST or IWnn bit in MEILWST is 1)
- When a write transaction occurs to ICBnn in the state where the ACnn bit in MEACTST0 of active ICBnn is negated by writing to MEACTSTn
- When a write transaction occurs to a plane different from the register set A/register set B indication (value of the CB bit in MEnnCTRL) of an active ICBnn (ACnn in MEACTST0 = 1). However, when a module uses the same ICBnn repeatedly, the mismatch of register set A/register set B means the completion of processing for the former plane, which is not an error.

In writing to MEILWST, the IW bits corresponding to the bits to which 1 has been written are usually negated. When the WD bit in MEVCR1 is 1, the IW bits corresponding to the bits to which 1 has been written are set.

When the interrupt function of MEILIE0 is used and an interrupt occurs, clear the bit that generated the interrupt. Although the interrupt function is not used, no transaction to ICBnn for which the IWnn bit is set to 1 is processed after that. Therefore, the IWnn bit needs to be cleared. See section 39.2.14 (1), Clearing the Error Flag and Restarting.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IWnn															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IWnn															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	IWnn	H'0000 0000	R/W	Indicate that an error occurred during a write transaction to ICBnn (nn = 0 to 31). The bits to which 1 has been written are cleared.

39.2.14 ICB Read Transaction Error Status Register (MEILRST)

The IRnn bit (nn = 0 to 31) indicates that an unprocessable read transaction to ICBnn (nn = 0 to 31) has occurred. When this bit is set to 1, the ACnn bit in MEACTST0 is negated. A read transaction error occurs under the following conditions.

Conditions for read transaction error:

- When a read transaction occurs to ICBnn for which the MD2 to MD0 bits in MEnnCTRL are set to B'000
- When a read transaction occurs to ICBnn in which a write transaction error or read transaction error has already occurred (IRnn bit in MEILRST or IWnn bit in MEILWST is 1)
- When a read transaction occurs to ICBnn in the state where the ACnn bit in MEACTST0 of active ICBnn is negated by writing to MEACTST
- When a read transaction occurs to a plane different from the register set A/register set B indication (value of the CB bit in MEnnCTRL) of an active ICBnn (ACnn in MEACTST0 = 1). However, when a module uses the same ICBnn repeatedly, the mismatch of register set A/ register set B means the completion of processing for the former plane, which is not an error.

In writing to MEILRST, the IR bits corresponding to the bits to which 1 has been written are usually negated. When the WD bit in MEVCR1 is 1,the IR bits corresponding to the bits to which 1 has been written are set. When the interrupt function of MEILIE0 is used and an interrupt occurs, clear the bit that generated the interrupt. Although the interrupt function is not used, no transaction to ICBnn for which the IRnn bit is set to 1 is processed after that. Therefore, the IRnn bit needs to be cleared.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IRnn															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IRnn															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	IRnn	H'0000 0000	R/W	Indicate that an error occurred during a read transaction to ICBnn (nn = 0 to 31). The bits to which 1 has been written are cleared.

(1) Clearing the Error Flag and Restarting

A transaction where the IWnn bit in MEILWST or the IRnn bit in MEILRST has been set to 1 remains in the ICB module and is not cleared until the transaction is processed or all ICBs are initialized. Therefore, the error module and all ICBs must be initialized except for the special case where the property of the transaction that has set the error flag can be anticipated.

1. If there is any module that uses an ICB other than ICBnn, change the register setting of the module so as not to use any ICB temporarily.
2. Issue the software reset command to all modules that use ICBnn and may cause an error.
3. Set the RST bit in MEVCR1 to 1 to reset all ICBs.

When the property of the transaction that has set the error flag can be anticipated and the transaction can be completed, the following procedure is available.

[Example] In the case of an error due to issuing of a transaction with the MD2 to MD0 bits in MEnnCTRL set to 000:

1. Set the ICBnn so that the transaction can be handled with the IWnn flag in MEILWST or the IRnn flag in MEILRST set to 1, and then write a value other than B'000 to the MD2 to MD0 bits.
2. Clear the IWnn bit in MEILWST and the IRnn bit in MEILRST.
3. Set the WD bit in MEVCR1 to 1, and then set the corresponding ACnn bit in MEACTST to 1.
4. Write 0 to all bits in MEnnCTRL. Since the ACnn bit is 1, no data writing is made actually, but the ICBnn setting is reevaluated by writing to MEnnCTRL, and the remaining transaction is processed.

39.2.15 ICB Transaction Error Status Register n (MEILSTn)

The IWR bit (nn = 32 to 127) indicates that an unprocessable read transaction or write transaction has occurred in ICBnn (nn = 32 to 127). When this bit is set to 1, the ACnn bit in MEACTSTn is negated.

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	IWRnn (n = 1: nn = 32 to 63 n = 2: nn = 64 to 95 n = 3: nn = 96 to 127)	H'0000 0000	R/W	Indicate that an error occurred during a read or write transaction to ICBnn (nn = 32 to 127). The bits to which 1 has been written are cleared.

39.2.16 ICB Request Queue Priority Select Register 1, 2 (MEQSEL1, 2)

Each ICB buffer makes requests to the external memory for read fill operation or write back operation. These read-fill and write-back requests (hereafter referred to as external memory access requests) are stored in three kinds of queues that have different priority levels.
The QSEL1nn[47:16] bits and QSEL2nn[47:16] bits determine whether external memory access requests from ICB16 to ICB47 are stored in queue 1 or queue 2. For details, refer to 39.2.16 (1) External Memory Access Processing Order.

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	QSEL1nn[31:16] QSEL1nn[47:32]	H'00FF 0000	R/W	Store external memory access requests made by an ICBnn (nn = 16 to 47) in queue 1. The upper 16 bits and the lower 16 bits correspond to nn = 16 to 31 and nn = 32 to 47, respectively. Total 8 bits must be set to 1. It is prohibited to set QSEL1nn and QSEL2nn to 1 for a single buffer at the same time.

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	QSEL2nn[31:16] QSEL2nn[47:32]	H'FF00 0000	R/W	Store external memory access requests made by an ICBnn (nn = 16 to 47) in queue 2. The upper 16 bits and the lower 16 bits correspond to nn = 16 to 31 and nn = 32 to 47, respectively. Total 8 bits must be set to 1. It is prohibited to set QSEL1nn and QSEL2nn to 1 for a single buffer at the same time.

(1) External Memory Access Processing Order

Each ICB buffer makes requests to the external memory for read fill operation or write back operation. The order of processing these read-fill and write-back requests (hereafter referred to as external memory access requests) is described below:

1. External memory access requests made by ICBs are processed on a 1-line basis. After processing for a single line is completed, processing for another ICB is started.
2. External memory access requests made by ICBs are accumulated in three kinds of queues. Once external memory access requests are accumulated in the queues, the next request is prevented from being made until processing for the requests is completed.
   - Queue 2: External memory access requests made by the buffer specified in QSEL2 are accumulated.
   - Queue 1: External memory access requests made by the buffer specified in QSEL1 are accumulated.
   - Queue 0: External memory access requests made by buffers other than above are accumulated.

   Note that requests made by ICBs that are used as a cache buffer in the frame buffer cache mode are accumulated in the queue corresponding to the ICB number of the marker buffer.
3. External memory access requests accumulated in queue 2 are always given the highest priority. While there are no requests accumulated in queue 2, external memory access requests in queue 1 and 0 are processed alternately. The frequency of processing requests in queue 0 is the same as that of processing requests in queue 1. However, the numbers of requests accumulated in queue 0 and 1 are 16 and 8, respectively, and because of the difference between the numbers, requests in queue 1 are processed faster.

   Therefore, the buffer allocated to QSEL2 must have a higher priority than that allocated to QSEL1.

39.3 Making Access to MERAM

39.3.1 Direct Access from Shwy Initiator

The 1536-Kbyte space of the addresses H'E808 0000 to H'E81F FFFF is directly accessible to the MERAM memory. However, accesses are made irrespective of the ICB active status. Therefore, make accesses only to areas that are not used as ICBs.

39.3.2 Direct Access from Associated Image Module

The addresses H'0000 0000 to H'7FFF FFFF and H'C000 0000 to H'FFFF FFFF from an associated module are output on the SHwy. Therefore, when making a direct access from an associated module to the MERAM, specify the 1536-Kbyte space of addresses H'E558 0000 to H'E56F FFFF or H'E808 0000 to H'E81F FFFF. However, accesses are made irrespective of the ICB active status. Therefore, make accesses only to areas that are not used as ICBs.

39.3.3 Access to ICB from Associated Image Module

When AMD1 in MEVCR1 = 0, accesses from an associated module to addresses H'8000 0000 to H'BFFF FFFF are treated as accesses to ICBs (nn = 00 to 31).

When AMD1 in MEVCR1 = 1, accesses from an associated module to addresses H'C000 0000 to H'DFFF FFFF are treated as accesses to ICBs (nn = 00 to 31).

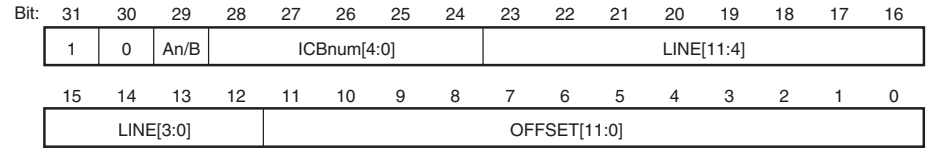
The ICB is used by interpreting the address from an associated image module as follows:

Bit field meaning;

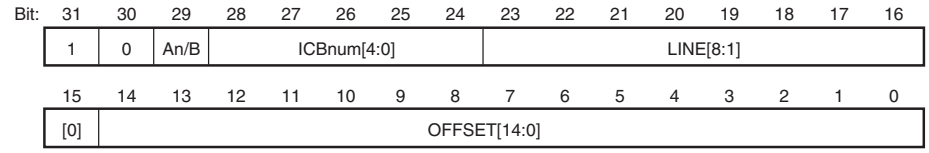
- An/B — Indicates register set A by 0 and register set B by 1. Note, however, that in the YC combining mode, 0 and 1 indicate Y surface indication and C surface indication, respectively.
- ICBnum4 to ICBnum0 — Indicate the ICB buffer number.
- LINEn to LINE0 — Indicate the line number.
- OFFSETm to OFFSET0 — Indicate the in-line offset (in 1-byte units).

(a) AMD1 in MEVCR1=0, CM in MEnnCTRL=0

(a-1) XSZM in MEnnBSIZE < 4096

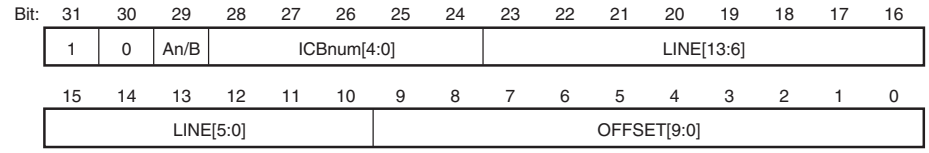


(a-2) 4096 ≤ XSZM in MEnnBSIZE

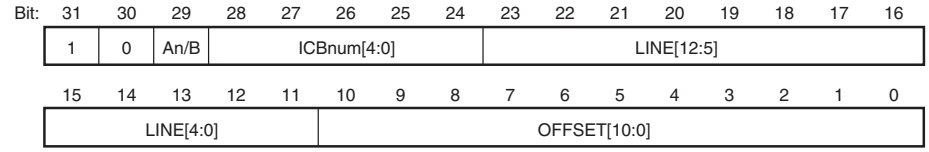


(b) AMD1 in MEVCR1=0, CM in MEnnCTRL=1

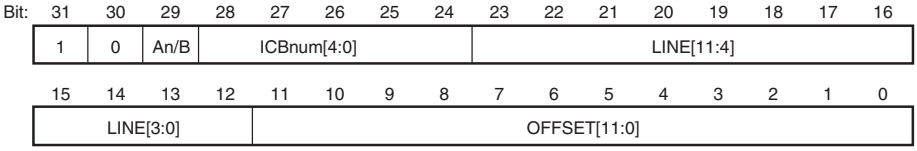
(b-1) XSZM1 in MEnnBSIZE < 1024



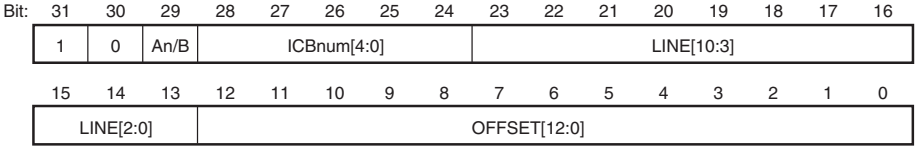
(b-2) 1024 ≤ XSZM1 in MEnnBSIZE < 2048



(b-3) 2048 ≤ XSZM1 in MEnnBSIZE < 4096



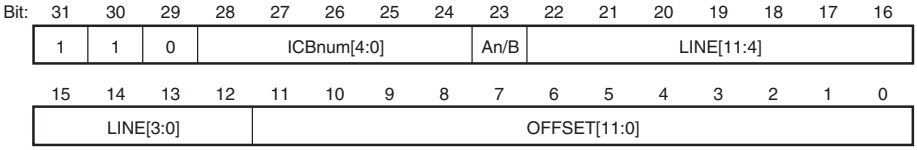
(b-4) 4096 ≤ XSZM1 in MEnnBSIZE < 8192



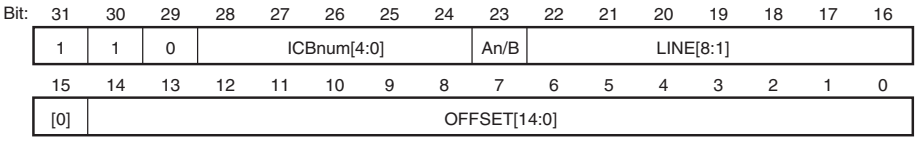
Note: When CM in MEnnCTRL is 1, set XSZM1 in MEnnBSIZE to less than 8192.

(c) AMD1 in MEVCR1 = 1, CM in MEnnCTRL = 0

(c-1) XSZM1 in MEnnBSIZE < 4096

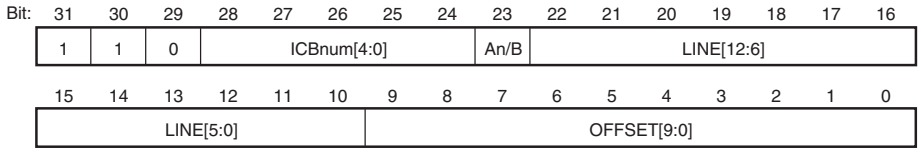


(c-2) 4096 ≤ XSZM1 in MEnnBSIZE

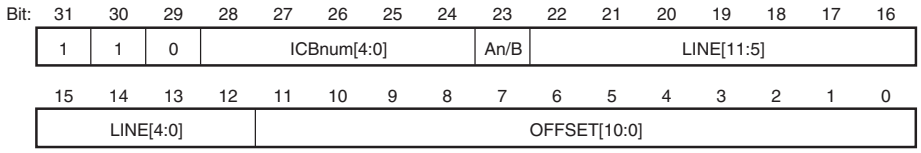


(d) AMD1 in MEVCR1 = 0, CM in MEnnCTRL = 1

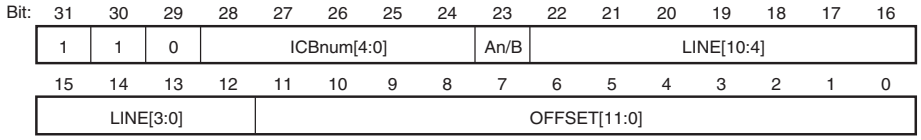
(d-1) XSZM1 in MEnnBSIZE < 1024



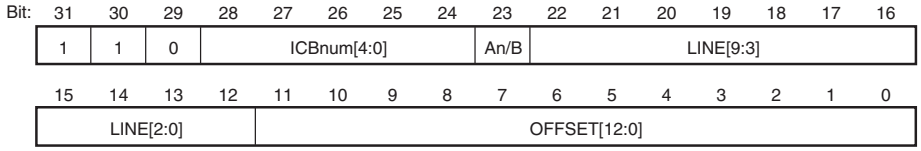
(d-2) 1024 ≤ XSZM1 in MEnnBSIZE 2048



(d-3) 2048 ≤ XSZM1 in MEnnBSIZE<4096



(d-4) 4096 ≤ XSZM1 in MEnnBSIZE<8192



Note: When CM in MEnnCTRL is 1, set XSZM1 in MEnnBSIZE to less than 8192.

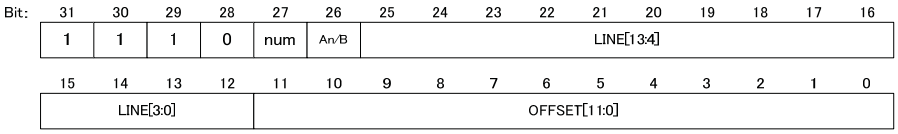
39.3.4 Access to Extended ICB from Associated Image Module

A unique extended ICB (nn = 32 to 127) is allocated to each associated image module. When MEVCR1.AMD0 = 1, accesses to H'E000 0000 to H'EFFF FFFF correspond to those to extended ICBs. Table 39.5 lists the extended ICB numbers corresponding to each image module.

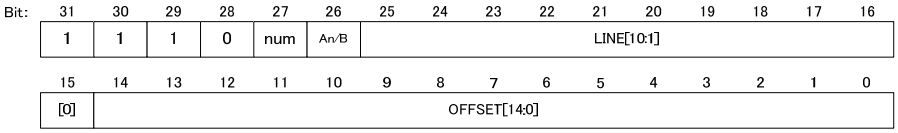
Addresses from image modules are interpreted as follows to use extended ICBs.

(e) AMD0 in MEVCR1 = 1, CM in MEnnCTRL = 0

(e-1) XSZM1 in MEnnBSIZE < 4096

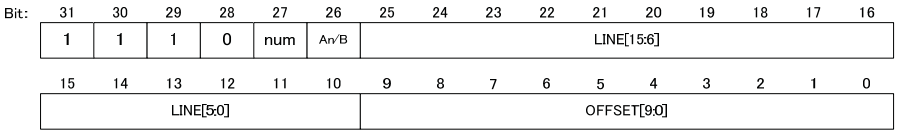


(e-2) 4096 ≤ XSZM1 in MEnnBSIZE

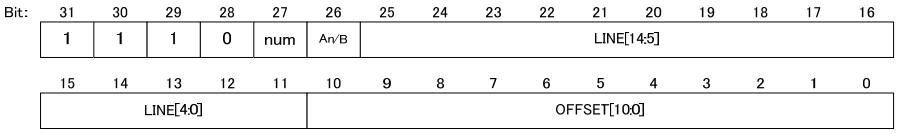


(f) AMD0 in MEVCR1 = 1, CM in MEnnCTRL = 1

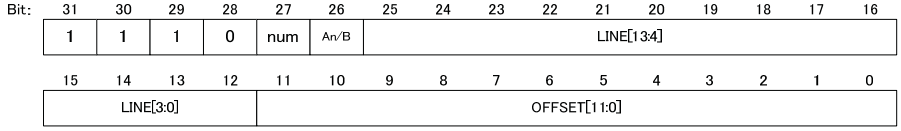
(f-1) XSZM1 in MEnnBSIZE < 1024



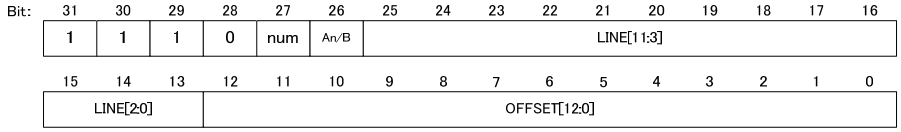
(f-2) 1024 ≤ XSZM1 in MEnnBSIZE < 2048



(f-3) 2048 ≤ XSZM1 in MEnnBSIZE < 4096



(f-4) 4096 ≤ XSZM1 in MEnnBSIZE < 8192



Note: When CM in MEnnCTRL is 1, set XSZM1 in MEnnBSIZE to less than 8192.

Table 39.5 Image Modules and their Corresponding Extended ICB Numbers

Image Module	R/W	Extended ICB number (ICBnn)
CEU, LCDC0, LCDC1 *	W	40, 41
LCDC0 *	R	32, 33
LCDC1 *	R	34, 35
CSI-RX *	W	42, 43
DSI-TX0 *	R	36, 37
DSI-TX1 *	W	38, 39
BEU0	R	48, 49
	W	50, 51
BEU1	R	52, 53
	W	54, 55
BEU2	R	56, 57
	W	58, 59
VEU0	R	64, 65
	W	66, 67
VEU1	R	68, 69
	W	70, 71
VEU2	R	72, 73
	W	74, 75
VEU3	R	76, 77
	W	78, 79
VPU	R	80, 81
	W	82, 83
JPU	R	96, 97
	W	98, 99
2D-DMAC	R	CH0 to 3: 104, 105 CH4 to 7: 106, 107
	W	CH0 to 3: 108, 109 CH4 to 7: 110, 111
ISP (capture, RAW pre-processing)	R	112, 113
	W	114, 115
ISP (YC processing)	R	116, 117
	W	118, 119

* Buffer priority levels can be changed using MEQSEL1 and MEQSEL2.

39.3.5 Additional remarks on line numbers and offset addresses

The descriptions in (a) to (f) above are about how the output addresses from an image module which is not the VPU are interpreted to be used for the ICB function. Addresses are generated in the image module in the following two methods:

(1) Adjusting the stride length of image modules to the interpretation as the ICB function

The modules other than the VPU have registers for setting the stride length. The addresses output from modules can be interpreted as the ICB function by setting H'1000 or H'8000 in these registers ((a-1)(a-2), (c-1)(c-2), (e-1)(e-2)). (Where appropriate, examples are provided in this chapter to assist the description.) The actual data width and stride length are set in XSZM1 in MEnnBSIZE and SBSIZE in MEnnSBSIZE.

In this method, the volume of transfers between the MERAM and external memory is equal to the amount of the screen data set in XSZM1 in MEnnBSIZE and SBSIZE in MEnnSBSIZE. Since a buffer area with a size of 1KB/2KB/4KB. that is obtained by rounding up (XSZM1 in MEnnBSIZE + 1) is secured for each line in the MERAM, some of those areas may be wasted depending on the value of XSZM1 in MEnnBSIZE.

(2) Adjusting the stride length of image modules to the values in the external memory

Set the same value for the stride length of an image module as in the external memory (hereafter called as W). This allows the addresses from the image module to be generated in the form of ICB buffer identifiers and in-frame offsets.

An example below describes how to set values in this method when CM in MEnnCTRL is set to 1 and XSZM1 in MEnnBSIZE = H'3FF and SBSIZE in MEnnSBSIZE = H'400 are set. The ICB interprets the offset from the start of frame contained in the output address from the image module as a line in 1-KB units to perform transfers with the external memory.

In this method, the source of the MERAM to SDRAM transfer includes invalid data areas (W minus H, where H is the actual data width) in the memory. This means that the larger the size of W-H is, the more volume of transfers is wasted. The buffer area in the MERAM is used effectively in 1-KB units except for the invalid data area in it. Consequently, the buffer area in the MERAM can be smaller by using the method (A-2) when W-H is small. The following summarizes how to use the ICB in this method.

- Set CM in MEnnCTRL = 1 to specify the consecutive address mode.
- Set XSZM1 in MEnnBSIZE = H'3FF to specify the line width of ICBs to 1KB.
- Set SBSIZE in MEnnSBSIZE = H'400 to specify the line width of ICBs to 1KB.

- Set YSZM1 in MEnnBSIZE = roundup ((W*(V-1) + H)/1KB)-1 to include the 1-KB that contains the last pixel, where V is the line number in the external memory and roundup(f) is the calculation to round up f to an integer.
- Specify the buffer line number to be secured in BNM in MEnnBSIZE in 1-KB units.
- Set the values calculated as follows in KRBNM in MEnnBSIZE and KWBNM in MEnnBSIZE. Use n as the desired number of lines to be retained for each module that is described in section 39.5, Settings for Each Associated Module.
  - Calculate the desired number of lines to be retained (N) that is converted in 1-KB units, assuming N = roundup(n*W/1KB)+1. Note, however, that in the YC combining mode (YCbCr420), it is necessary to assume N = roundup(n*W/1KB) + 2
  - When 16 ≥ N, assume BSZ in MEnnCTRL = 0 and Ns = N.
  - When 32 ≥ N>16, assume BSZ in MEnnCTRL = 1 and Ns = roundup(N/2).
  - When 64 ≥ N>32, assume BSZ in MEnnCTRL = 2 and Ns = roundup(N/4).
  - (Hereinafter the same applies. Set the BSZ value so that Ns ≤ 16 is satisfied.)
  - Set KRBNM in MEnnBSIZE and KWBNM in MEnnBSIZE to Ns-1.

Note the followings:

- In the last line, access made to the external memory reaches the area that is rounded up the last pixel of an image to a 1-KB boundary. So, make sure to secure areas in the external memory to include the range.

39.4 Setting ICB

Note: The examples described in this section are based on the method listed in section 39.3.4 (1), Adjusting the stride length of image modules to the interpretation as the ICB function. See the section 39.3.4 (2), Adjusting the stride length of image modules to the values in the external memory that is also enable to be used for the setting ICB.

39.4.1 Settings as Read Fill Buffer

The following example shows the setting when ICBs are used as a read buffer for read accesses to the VEU (0).

- ICB00 setting (for Y data)

```
ME00CTRL     =   H'0000 0701 ;// Read fill mode, no completion detection
                             // Allocate the buffer area from H'E808 0000
ME00BSIZE    =   H'005F 007F ;// Vertical 96 lines and horizontal 128 pixels
ME00MCNF =       H'0F1F 0000 ;// Number of lines retained during reading=16, total number
                                 of buffer lines=32
ME00SSARA    =   H'5800 0000 ;// Start address of Y data in the external memory (register
                                 set A)
ME00SSARB    =   H'5900 0000 ;// Start address of Y data in the external memory (register
                                 set B)
ME00SBSIZE   =   H'0000 0080 ;// Screen width in the external memory (128 bytes)
```

- ICB01 setting (for C data)

```
ME01CTRL     =   H'0020 0701 ;// Read fill mode, no completion detection
                             // Allocate the buffer area from H'E808 8000
ME01BSIZE    =   H'005F 007F ;// Vertical 96 lines and horizontal 128 pixels
ME01MCNF     =   H'0F1F 0000 ;// Number of lines retained during reading=16,
                                 total number of buffer lines=32
ME01SSARA    =   H'5800 8000 ;// Start address of C data in the external memory
                                 (register set A)
ME01SSARB    =   H'5900 8000 ;// Start address of C data in the external memory
                                 (register set B)
ME01SBSIZE   =   H'0000 0080 ;// Screen width in the external memory (128 bytes)
```

- VEU(0) setting

```
VE0SSR   =   H'0060 0080  ;   // Vertical 96 lines and horizontal 128 pixels
V0SAYR   =   H'8000 0000  ;   // Use ICB00 (register set A) for reading Y data
V0SACR   =   H'8100 0000  ;   // Use ICB01 (register set A) for reading C data
VE0SWR   =   H'0000 1000  ;   // Set H'1000 as screen width when using ICBs
V0RFSR   =   H'0060 0080  ;   // Clip the output. Vertical 96 lines and horizontal 128
pixels
V0DAYR   =   H'5801 0000  ;   // Start address in the external memory to store Y data
                              (register set A)
V0DACR   =   H'5801 8000  ;   // Start address in the external memory to store C data
                              (register set A)
VE0DWR   =   H'0000 0080  ;   // Screen width in the external memory (128 bytes)
VE0IER   =   H'0000 0001  ;   // Enable interrupts
```

(Other registers should be set according to the desired VEU0 functions.)

After setting these, start the VEU0 by setting VE1STR1 = H'0000 0001. The read access request from the VEU0 points to the addresses using ICB00 (register set A)/ICB01 (register set A), so the MERAM starts a read fill operation from the external memory address (H'5800 0000/H'5800 8000). This read fill operation continues to be performed automatically until all read fill operations for the lines specified in YSZM1 in ME00BSIZE/YSZM1 in ME01BSIZE completes or the buffer areas for the buffer lines specified in BNM in ME00BSIZE/BNM in ME01BSIZE get full.

If the read access request from the VEU0 is to the lines that are already filled into the buffer area, the MERAM returns data to the VEU0. Otherwise, the request is suspended until the lines have been filled into the buffer area.

The VEU0 sometimes performs read fill operations on per-block basis, so the line number is not always incremented serially and the line at up to 16 lines ago may be filled again. For this reason, the numbers of lines retained during reading that are set in KRBNM in ME00MCNF should be more than 16. If the MERAM returns the first n lines corresponding to an access request from the VEU0, the data in "n-(number of lines retained during reading)" lines is considered as unnecessary and discarded from the buffer area. The area is reused for another read fill operation.

When an interrupt from the VEU0 is detected, notify the MERAM of the completion of the read operation to ICB00/ICB01 by setting as follows:

```
ME00CTRL =   H'0000 0711 ;    // RF bit=1
ME01CTRL =   H'0020 0711 ;    // RF bit=1
```

When the RF bits are set, ICB00/ICB01 are freed and the bit 1 to bit 0 in the MEACT register return to 0. This enables the VEU0 to be set for the next operation or ICB00/ICB01 to be set for other modules.

When the start addresses of read operations for the VEU0 are set as follows, data is filled from H'5900 0000/ H'5900 8000 in the external memory:

```
V0SAYR   =   H'A000 0000  ;   // Use ICB00 (register set B) for reading Y data
V0SACR   =   H'A100 0000  ;   // Use ICB01 (register set B) for reading C data
```

By combining with the setting of the VEU0 two-set register can reduce resetting of the MERAM or VEU0 registers.

39.4.2 Settings as Write Back Buffer

The following example shows the setting when ICBs are used as a write back buffer for write accesses to the VEU1.

- ICB02 setting (for Y data)

```
ME02CTRL     =   H'0040 0702 ;// Write back mode, no completion detection
                             // Allocate the buffer area from H'E808 8000
ME02BSIZE    =   H'005F 007F ;// Vertical 96 lines and horizontal 128 pixels
ME02MCNF     =   H'F01F 0000 ;// Number of lines retained during writing=16, total number of
                                 buffer lines=32
ME02SSARA    =   H'5802 0000 ;// Start address in the external memory to store Y data
                                 (register set A)
ME02SSARB    =   H'5902 0000 ;// Start address in the external memory to store Y data
                                 (register set B)
ME02SBSIZE   =   H'0000 0080 ;//Screen width in the external memory (128 bytes)
```

- ICB03 setting (for C data)

```
ME03CTRL     =   H'00600702 ; // Write back mode, no completion detection
                             // Allocate the buffer area from H'E809 0000
ME03BSIZE    =   H'005F007F ; // Vertical 96 lines and horizontal 128 pixels
ME03MCNF     =   H'F01F0000 ; // Number of lines retained during writing=16,
                                 total number of buffer lines=32
ME03SSARA    =   H'58028000 ; // Start address in the external memory to store C data
                                 (register set B)
ME03SSARB    =   H'59028000 ; // Start address in the external memory to store C data
                                 (register set B)
ME03SBSIZE   =   H'00000080 ; // Screen width in the external memory (128 bytes)
```

- VEU(1) setting

```
VE1SSR      =   H'0060 0080  ;// Vertical 96 lines and horizontal 128 pixels
V1SAYR      =   H'580 10000  ;// Start address of Y data in the external memory
                             // (This is an example of setting when the output result from
                                the VEU0 is to be processed further.)
V1SACR      =   H'5801 8000  ;// Start address of C data in the external memory
                             // (This is an example of setting when the output result from
                                the VEU0 is to be processed further.)
VE1SWR      =   H'0000 0080  ;// Screen width in the external memory (128 bytes)
V1RFSR      =   H'0060 0080  ;// Clip the output. Vertical 96 lines and horizontal 128
                                pixels
V1DAYR      =   H'8200 0000  ;// Use ICB02 (register set A) for writing Y data
V1DACR      =   H'8300 0000  ;// Use ICB03 (register set A) for writing C data
VE1DWR      =   H'0000 1000  ;// Set H'1000 as screen width when using ICBs
VE1IER      =   H'0000 0001  ;// Enable interrupts
```

(Other registers should be set according to the desired VEU1 functions.)

After setting these, start the VEU1 by setting VE1STR = H'0000 0001. The write access request from the VEU1 points to the addresses using ICB02 (register set A)/ICB03 (register set A), so the MERAM processes write data in a write operation to the buffer area secured in the MERAM. This write data can be written until the buffer areas for the buffer lines specified in BNM in ME02BSIZE/BNM in ME03BSIZE get full.

The VEU1 sometimes performs write operations on per-block basis, so the target line number is not always incremented serially and the target line at up to 16 lines ago may be written again. For this reason, the numbers of lines retained during writing that are set in KWBNM in ME02MCNF/KWBNM in ME03MCNF should be more than 16. If the MERAM returns the first n lines corresponding to an access request from the VEU1, the data in "n-(number of lines retained during writing)" is considered to have been written and it is written back to the external memory. The area that contains data that has been written back is freed and reused for write data. Thus, processing the write operation from the VEU(1) continues with reusing buffer areas until the last line specified in YSZM1 in ME02BSIZE/YSZM1 in ME03BSIZE is reached.

When an interrupt from the VEU1 is detected, notify the MERAM of the completion of the write operation to ICB02/ICB03 by setting as follows:

```
ME02CTRL =   H'0040 0722 ;    // WF bit=1
ME03CTRL =   H'0060 0722 ;    // WF bit=1
```

When the WF bits are set, ICB02/ICB03 are freed and the bit 3 to bit 2 in the MEACT register return to 0 after the MERAM writes back data that has not been done yet to the external memory (note that the data on the lines to be retained during writing before the last line is not written back unless the WF bit is set). This enables the VEU1 to be set for the next operation or ICB02/ICB03 to be set for other modules.

When the start addresses of write operations for the VEU1 are set as follows, data is written back from H'5902 0000/ H'5902 8000 in the external memory:

```
VSAYR2   =   H'A200 0000  ;   // Use ICB02 (register set B) for writing Y data
VSACR2   =   H'A300 0000  ;   // Use ICB03 (register set B) for writing C data
```

By combining with the setting of the VEU1 two-set register can reduce resetting of the MERAM or VEU1 registers.

39.4.3 Settings as Interconnect Buffer

The following example shows the setting when the VEU0 and VEU1 are interconnected via ICBs.

- ICB04 setting (for Y data)

```
ME04CTRL     =   H'0080 0703 ;// Interconnect mode with write back, no completion detection
                             // Allocate the buffer area from H'E808 0000
ME04BSIZE    =   H'005F 007F ;// Vertical 96 lines and horizontal 128 pixels
ME04MCNF     =   H'FF2F 0000 ;// Number of lines retained during writing=16, number of lines
                                 retained during reading=16,
                             // Total number of buffer lines=32
ME04SSARA    =   H'5801 0000 ;// Start address (register set A) in the external memory to
                                 store the Y data
                             // of the processing result from the VEU0
ME04SSARB    =   H'5901 0000 ;// Start address in the external memory to store Y data
                                 (register set B)
ME04SBSIZE   =   H'0000 0080 ;// Screen width of the processing result from the VEU0 in
                                 the memory (128 bytes)
```

- ICB05 setting (for C data)

```
ME05CTRL     =    H'00A0 0703 ;// Interconnect mode with write back, no completion detection
                               // Allocate the buffer area from H'E808 8000
ME05BSIZE    =    H'005F 007F ;// Vertical 96 lines and horizontal 128 pixels
ME05MCNF     =    H'FF2F 0000 ;// Number of lines retained during writing=16, number of lines
                                  retained during reading=16,
                               // Total number of buffer lines=48
ME05SSARA    =    H'5803 8000 ;// Start address (register set A) in the external memory to
                                  store the Y data
                               // of the processing result from the VEU0
ME05SSARB    =    H'5903 8000 ;// Start address in the external memory to store C data
                                  (register set B)
ME05SBSIZE   =    H'0000 0080 ;// Screen width of the processing result from the VEU0 in
                                  the memory (128 bytes)
```

- VEU(0) setting (differences only)

```
VDAYR1       =    H'84000000  ;  // Use ICB04 (register set A) for writing Y data
VDACR1       =    H'85000000  ;  // Use ICB05 (register set A) for writing C data
VEDWR1       =    H'00001000  ;  // Set H'1000 as screen width when using ICBs
```

- VEU(1) setting (differences only)

```
VSAYR2       =    H'84000000  ;  // Use ICB04 (register set A) for reading Y data
VSACR2       =    H'85000000  ;  // Use ICB05 (register set A) for reading C data
VESWR2       =    H'00001000  ;  // Set H'1000 as screen width when using ICBs
```

After setting these, start the VEU0 and VEU1 by setting VE0STR = H'0000 0001 and VE1STR = H'0000 0001. With these settings, the output data from the VEU0 is input to the VEU1 via buffer areas in the MERAM. The output data from the VEU0 is also written back to the external memory. When MD in ME04CTRL/MD in ME05CTRL are set to 100, the output data from the VEU0 is stored in the MERAM only temporarily and no access is made to the external memory.

The VEU0 completes its operation and an interrupt is generated. But at this point, the data from the VEU0 that is on the lines to be retained during writing before the last line is considered not to be fixed, so the operation for the VEU1 is not complete. When an interrupt from the VEU0 is detected, notify the MERAM of the completion of the write operation to ICB04/ICB05 by setting as follows:

```
ME04CTRL =   H'0080 0723 ;    // WF bit=1
ME05CTRL =   H'00A0 0723 ;    // WF bit=1
```

When the WF bits are set, the MERAM determines that all data is fixed and the VEU1 starts its remaining operation to write back the data that has not been done yet to the external memory. When an interrupt is generated from the VEU1, notify the MERAM of the completion of the read operation to ICB04/ICB05 by setting as follows:

```
ME04CTRL =    H'0080 0713 ;     // RF bit=1
ME05CTRL =    H'00A0 0713 ;     // RF bit=1
```

If the RF bits are set to 1 and the write back to the external memory is complete, ICB04/ICB05 are freed and bit 5 to bit 4 in the MEACT register return to 0. This enables the VEU1 to be set for the next operation or ICB04/ICB05 to be set for other modules.

It is distinguished whether the output result from the VEU0 is written back to the register ser A or B of ICB04/ICB05, but the same register set should be selected for the VEU0/VEU1.

39.4.4 Settings as Interconnect Buffer Using Extended ICBs

Shown below is an example of settings for interconnection between the VEU0 and the VEU1 via extended ICBs.

- ICB66 Setting (for the VEU0 and Y data)

```
ME66CTRL    = H'0080 2703      ; // Interconnect mode with write back, no completion
                                   detection
                                 // Buffer link with ICB68. Allocate the buffer area from
                                   H'E808 0000.
ME66BSIZE   = H'005F 007F      ; // Vertical 96 lines and horizontal 128 pixels
ME66MCNF    = H'F02F 0006      ; // Number of lines retained during writing = 16, total
                                   number of buffer lines = 32
                                 // Enable buffer link mode
ME66SSARA   = H'5801 0000      ; // Start address of an area in the external memory, in which
                                   the Y data of processing result from the VEU0 is to be
                                   stored (A surface)
ME66SSARB   = H'5901 0000      ; // Start address of an area in the external memory, in which
                                   the Y data is to be stored (B surface)
ME66SBSIZE  = H'0000 0080      ; // Screen width of processing result from the VEU0 in the
                                   memory (128 bytes)
```

- ICB67 Setting (for the VEU0 and C data)

```
ME67CTRL    = H'00A0 2F03      ; // Interconnect mode with write back, no completion
                                   detection
                                 // Buffer link with ICB69. Allocate the buffer area from
                                   H'E808 8000.
ME67BSIZE   = H'005F 007F      ; // Vertical 96 lines and horizontal 128 pixels
ME67MCNF    = H'0F2F 0006      ; // Number of lines retained during writing = 16, total
                                   number of buffer lines = 48
                                 // Enable buffer link mode
ME67SSARA   = H'5803 8000      ; // Start address of an area in the external memory, in which
                                   the C data of processing result from the VEU0 is to be
                                   stored (A surface)
ME67SSARB   = H'5903 8000      ; // Start address of an area in the external memory, in which
                                   the C data is to be stored (B surface)
ME67SBSIZE  = H'0000 0080      ; // Screen width of processing result from the VEU0 in the
                                   memory (128 bytes)
```

- ICB68 Setting (for the VEU1 and Y data)

```
ME68CTRL    = H'0080 1703      ; // Interconnect mode with write back, no completion
                                   detection
                                 // Buffer link with ICB66. Allocate the buffer area from
                                   H'E808 0000.
ME68BSIZE   = H'005F 007F      ; // Vertical 96 lines and horizontal 128 pixels
ME68MCNF    = H'0F2F 0006      ; // Number of lines retained during reading = 16, total
                                   number of buffer lines = 32
                                // Enable buffer link mode
ME68SSARA   = H'5801 0000      ; // Start address of an area in the external memory, in which
                                   the Y data of processing result from the VEU0 is to be
                                   stored (A surface)
ME68SSARB   = H'5901 0000      ; // Start address of an area in the external memory, in which
                                   the Y data is to be stored (B surface)
ME68SBSIZE  = H'0000 0080      ; // Screen width of processing result from the VEU0 in the
                                   memory (128 bytes)
```

- ICB69 Setting (for the VEU1 and C data)

```
ME69CTRL    = H'00A0 1F03      ; // Interconnect mode with write back, no completion
                                   detection
                                 // Buffer link with ICB67. Allocate the buffer area from
                                   H'E808 8000.
ME69BSIZE   = H'005F 007F      ; // Vertical 96 lines and horizontal 128 pixels
ME69MCNF    = H'F02F 0006      ; // Number of lines retained during reading = 16, total
                                   number of buffer lines = 48
                                 // Enable buffer link mode
ME69SSARA   = H'5803 8000      ; // Start address of an area in the external memory, in which
                                   the C data of processing result from the VEU0 is to be
                                   stored (A surface)
ME69SSARB   = H'5903 8000      ; // Start address of an area in the external memory, in which
                                   the C data is to be stored (B surface)
ME69SBSIZE  = H'0000 0080      ; // Screen width of processing result from the VEU0 in the
                                   memory (128 bytes)
```

- VEU0 Setting (differences only)

```
V0DAYR      = H'E000 0000      ; // Use ICB66 (A surface) for writing Y data
V0DACR      = H'E800 0000      ; // Use ICB67 (A surface) for writing C data
VE0DWR      = H'0000 1000      ; // Set H'1000 as screen width when using ICBs
```

- VEU1 Setting (differences only)

```
V1SAYR      = H'E000 0000      ; // Use ICB68 (A surface) for reading Y data
V1SACR      = H'E800 0000      ; // Use ICB69 (A surface) for reading C data
VE1SWR      = H'0000 1000      ; // Set H'1000 as screen width when using ICBs
```

When using the interconnection function with extended ICBs, the settings described in section 39.4.3, Settings as Interconnect Buffer cannot be used because a unique ICB is allocated to each module. Enabling the buffering mode allows interconnection between two different ICBs.

39.4.5 Settings as Frame Buffer Cache

ICBs can be used as a frame buffer cache by combining two ICBs. One is called marker buffer, and the other is called cache buffer.

However, when the LCDC handles YCbCr screens, it uses four ICBs in total (two for each Y image and C image). The following descriptions are based on the assumption that the LCDC handles RGB images.

- Marker buffer

  Set the LCDC for using the marker buffer. That is, the addresses that are output from the LCDC include the ICB number of the marker buffer, and therefore it seems that only the marker buffer is accessed. Only ICB28 to ICB31 buffers can be used as the marker buffer. In other words, when MD = B'111 in MEmmCTRL (mm = 28 to 31 in this case) is set for any of ICB28 to ICB31, such an ICB is treated as a marker buffer. Set the corresponding cache buffer number to the NXT4 to NXT0 bits in MEmmCTRL of the marker buffer.
- Cache buffer

  When the line number 0 access is made to the marker buffer, the NXT4 to NXT0 bits in MEmmCTRL are referenced, and the set value (cc) is regarded that ICBcc is used.

  ICBcc functions like the read fill buffer. When the read fill operation for the buffer lines specified by the BNM7 to BNM0 bits in MEccMCNT is completed, the control is shifted to the buffer specified by the NXT4 to NXT0 bits in MEccCTRL so that the filled data remains in the MERAM memory without being overwritten. Specify the marker buffer number (mm) again in the NXT4 to NXT0 bits in MEccCTRL.

When processing shifts from ICBcc to ICBmm, the active bit (ACcc in MEACTST) of ICBcc remains 1. When the ACcc bit in MEACTST is 1 at an access to the cache buffer and the register set A/register set B indication by the CB bit in MEccCTRL matches the register set A/register set B shown at the address accessed, it is regarded that data is already contained in ICBcc, and therefore the read fill operation is not performed. If the register set A/register set B indication does not match or when the ACcc bit in MEACTST is 0, it is regarded that the data is updated or the access is the first one, and therefore the ACTcc bit is set, the CB bit is modified, and the read fill operation is performed again.

If the control is returned to the marker buffer for other than line number 0, the marker buffer continues operation as a read fill buffer. The marker buffer keeps operating to the last line while reusing the MERAM buffers in the same way as the normal read fill buffer. Secure at least two lines for the marker buffer to function as a read fill buffer. The marker buffer is necessary even if the frame buffer for all screens can be secured in the cache buffer.

The following describes settings specific to frame buffer cache mode for the marker buffer and cache buffer.

- Marker buffer settings

MEmmCTRL:	Set the MD2 to MD0 bits to B'111, and the NXT4 to NXT0 bits to cc. Specify the start address of the buffer in the MERAM to be used by the marker buffer in the MSAR8 to MSAR0 bits.
MEmmBSIZE:	Set the total number of lines in minus 1 in the YSZM111 to YSZM10 bits. Set the RCNT3 to RCNT0 bits to 1 to enable to detect the completion of read operation. The completion can also be notified manually.
MEmmMCNF:	Set B'001 or larger (to secure two lines or more) in the BNM7 to BNM0 bits. Specify 0 or larger (to secure one line or more) in the KRBNM3 to KRBNM0 bits.
MEmmSSARA/MEmmSSARB:	Set the start address for each register set A and register set B on the external memory, which cannot be retained in the cache buffer.
MEmmSBSIZE:	Specifies the screen width in the external memory in units of bytes in the same way as other modes.

- Cache buffer settings

MEccCTRL:	Set the MD2 to MD0 bits to B'111, and the NXT4 to NXT0 bits to mm. Specify the start address in units of Kbytes in the MERAM to be secured as a cache area in the MSAR8 to MSAR0 bits.
MEccBSIZE:	Set the total number of lines of the frame buffer (all screens) minus 1 in the YSZM111 to YSZM10 bits. When a cache buffer size enough for the data of the previous screen is secured, set the RCNT3 to RCNT0 bits to 1 to enable detection of the completion of read operation in the cache buffer.
MEccMCNF:	Set the number of lines that can be secured in the MERAM in the BNM7 to BNM0 bits. Specify 0 or larger (to secure one line or more) in the KRBNM3 to KRBNM0 bits.
MEccSSARA/MEccSSARB:	Set the start address each for register set A and register set B on the external memory.
MEccSBSIZE:	Specifies the screen width in the external memory in units of bytes in the same way as other modes.

To perform processing manually for one register set for the frame buffer cache, write 1 to the RF bit in MEmmCTRL of the marker buffer. At this time, the active state ACcc bit in MEACTST of ICBcc is not cleared. To stop using the entire frame buffer cache or to change the frame buffer cache setting, manually clear the ACcc bit in MEACTST.

- Additional Remarks: Reusing a data in the Cash Buffer.

  When a frame buffer dash is to be used in a condition that the image data is still contained in the MERAM, the initial read fill can be skipped by setting the cash buffer for already filled in advance. In this case, addition to the normal setting of the cash buffer is required as follows:

```
MEccCTRL                ← Normal initial setting | H'0000 0040;//WBF bit settings
MEccCTRL + H'0C address  ← H'0000 0000                          ;//
MEccCTRL + H'1C address  ← H'0000 0000                          ;//
MEVCR1          ← H'4000 0000                                   ;//Transit to the set
                                                                   mode in the ACT bit.
MEACTST[CC]     ← B'1                                           ;//Cash buffer active bit
                                                                   settings.
MEVCR1          ← H'0000 0000                                   ;//Returns to the clear
                                                                   mode of the ACT bit.
```

39.5 Setting for Each Associated Module

This section shows the registers that can use the interconnect buffer function and the required parameters to define the associated ICB buffers for each module.

This section is described based on the description in section 39.3.4 (1), Adjusting the stride length of image modules to the interpretation as the ICB function. See also section 39.3.4 (2), Adjusting the stride length of image modules to the values in the external memory since this method is also available.

In addition, this section assumes that line/block line transfer modes are used. Modules that can use block transfer mode are described individually.

Image Module: Indicates the name of the image module.

Usage Condition: Indicates the availability of the ICB function depending on the usage condition of the image module and the usage condition with different parameters defined. For details on the usage condition, refer to the footnotes below the table.

Address Register: Indicates the name of the register that can use the ICB function. The ICB function can be used by setting the address indicating that the function is to be used (refer to section 39.3.3, Access to ICB from Associated Image Module) in this register.

Associated Stride Register: When the register in this column is used as shown in 39.3.4(1), Adjusting the stride length of image modules to the interpretation as the ICB function, specify H'1000 or H'8000 in the register.

R/W: "R" indicates that the register(s) contains the input address. "W" indicates that the register(s) contains the output address.

Number of Lines Retained: Indicates the minimum number of lines required for the ICB buffer associated with the register. The KWBNM or KRBNM field in the MEnnMCNF register should be set to a value so that it is greater than the number of lines retained as shown in table 39.3.

Unit of Processing: The BNM field in the MEnnMCNF register should be set to a value that is obtained by adding at least 1 to the number of lines retained shown in table 39.3. Setting the field to at least "number of lines retained + unit of processing" prevents the image module from being stalled due to waiting for data buffers.

General Notes:

1. When the YCbCr format is used, the Y/C address registers are used. These registers cannot be used in such a way that one of them is set to use the ICB function and the other is set not to use it.
2. As the stride register value is interpreted differently for the YCbCr444 format, it cannot be used as shown in 39.3.4(1), Adjusting the stride length of image modules to the interpretation as the ICB function.

Table 39.6 Settings for Associated Module

Image Module	Conditions	Address Register	Associated Slide Register	R/W	Number of retained line	Process Units
CEU		CDAYR, CDACR	CDWDR	W	1	1
		CDBYR, CDBCR	CDWDR	W	1	1
VEU	V2	VEnSAYR, VEnSACR	VEnSWR	R	*V1	1
		VEnDAYR, VEnDACR	VEnDWR	W	×	×
	V3	VEnSAYR, VEnSACR	VEnSWR	R	*V1	1
	V4	VEnDAYR, VEnDACR	VEnDWR	W	*V1	1
	V5	VEnSAYR, VEnSACR	VEnSWR	R	×	×
		VEnDAYR, VEnDACR	VEnDWR	W	×	×
BEU		BSAYR1, BSACR1	BSMWR1	R	1	1
		BSAYR2, BSACR2	BSMWR2	R	1	1
		BSAYR3, BSACR3	BSMWR3	R	1	1
		BDAYR, BDACR	BDMWR	W	1	1
2D-DMAC	T1	CHnSAR	CHnSFMT.HWTH	R	1	1
		CHnDAR	CHnDFMT.HWTH	W	1	1
	T2	CHnSAR	CHnSFMT.HWTH	R	1	1
		CHnDAR	CHnDFMT.HWTH	W	2	2
	T3	CHnSAR	CHnSFMT.HWTH	R	1	1
		CHnDAR	CHnDFMT.HWTH	W	×	×
	T4	CHnSAR	CHnSFMT.HWTH	R	16	16
		CHnDAR	CHnDFMT.HWTH	W	×	×
JPU		JIFESYA1/2, JIFESYC1/2	JIFESMW	R	8	8
		JIFDDYA1/2, JIFDDYC1/2	JIFDDMW	W	8	8
DSI-TX		CMTIADR0/1/2/3	CMTIADRI0/1/2/3	R	1	1
LCDC	LC1	MLDSA1R, MLDSA2R	MLMLSR	R	1	1

Image Module	Conditions	Address Register	Associated Slide Register	R/W	Number of retained line	Process Units
VPU	VP1	BAAR0/1	DCHCR_DECY0	W	32	32
		BAAR0/1	DCHCR_DECC0	W	16	16
	VP2	BAAR0/1	DCHCR_TMPY0	R	32	32
		BAAR0/1	DCHCR_TMPC0	R	16	16
	VP3	BAAR0/1	DCHCR_REF	R	96/64	32
		BAAR0/1	DCHCR_REF	R	48/32	16

Notes: 1. The usage conditions of VEU are described below.

V1: The number of retained lines may need to be changed depending on whether the YC combining mode is used or not. When the YC combining mode is disabled, the minimum number of retained lines is 1. When it is enabled, make the following settings according to the number of pixels processed by the VEU.
[Reading]
YUV420: (The value obtained by rounding up “512 ÷ VESSR.VHSS”) + 2
YUV422: (The value obtained by rounding up “512 ÷ VESSR.VHSS”) + 1
[Writing]
YUV420: (The value obtained by rounding up “512 ÷ VRFSR.VHCLP”) + 2
YUV422: (The value obtained by rounding up “512 ÷ VRFSR.VHCLP”) + 1

V2: When (VFMCR.VMRR != 0) (When a vertical reverse filter is in use)

V3: When V2 is not met and VENHR.ENH || VENHR.ENHV || (VRFCR!=0) is true (When a zoom-in/out function or an enhancer is in use)

V4: When V2 and V3 are not met and VFMCR.FLTPI = 1 (When performing high-speed processing with a LPF/deblocking filter or a median filter)

V5: When V2, V3, and V4 are not met

2. The usage conditions of the 2D-DMAC are described below.

T1: If (CHnCTRL.ROTR == 0) && : (CHnCTRL.ROTL == 0) && : (CHnCTRL.VMRR == 0), and CHnCTRL.MY == 0

T2: If (CHnCTRL.ROTR == 0) && : (CHnCTRL.ROTL == 0) && : (CHnCTRL.VMRR == 0), and CHnCTRL.MY == 1

T3: If neither T1 nor T2 are applicable, but (CHnCTRL.ROTR == 0) && : (CHnCTRL.ROTL == 0),

T4: When T1, T2, and T3 are not met, processing is performed on a 16-line basis. The block transfer mode is available.

3. LCDC usage conditions
LC1: When using a marker buffer and a cache buffer, set the number of retained lines to 1.

4. The usage conditions from the VPU are described below.

VP1: Block transfer mode is available. When using it, set BSZ = 5 for Y (32 line) and BSZ = 4 for C (16 lines).

VP2: Block transfer mode is available. When using it, set BSZ = 5 for Y (32 line) and BSZ = 4 for C (16 lines).

VP3: The ICB function is available only during encoding or self-recording/playing. The number of referenced planes that can be used in the ICB function is up to 2 (4 planes for Y/C in total). If the area to be searched for is 32 × 32, 96 lines for Y and 48 lines for C should be retained. If the area to be searched for is 16 × 16, 64 lines for Y and 32 lines for C should be retained (block transfer mode is not available).

39.6 LCD Refresh Controller Overview

The MERAM has an LCD refresh mode.

39.7 Description on Registers related to LCD Refresh Controller

Table 39.7 shows the register configuration for the LCD refresh controller. Also, table 39.8 shows the states of registers in each mode.

Table 39.7 Register Configuration

Register Name	Abbr.	R/W	Address	Access Size
LCD refresh control register	LRCTRL	R/W	H'FE94 8000	32
LCD refresh interrupt enable register	LRIER	R/W	H'FE94 8004	32
LCD refresh interrupt source register	LRISR	R/W	H'FE94 8008	32
LCD refresh status register	LRSR	R/W	H'FE94 800C	32
MERAM operation mode set register	LRLPRSR	R/W	H'FE94 8014	32
LCD refresh interrupt address register 1	LRIAR1	R/W	H'FE94 8018	32
LCD refresh interrupt address register 2	LRIAR2	R/W	H'FE94 801C	32
LCD refresh extended address register 2	LRXAR2	R/W	H'FE94 8024	32
LCD refresh memory boundary address register 1	LRMAR1	R/W	H'FE94 8028	32
LCD refresh memory boundary address register 2	LRMAR2	R/W	H'FE94 802C	32
External access control register	LREBUFC	R/W	H'FE94 8030	32
External access read buffer allocation register	LREBUFP	R/W	H'FE94 8034	32
External access address map register 80	LREMAP80	R/W	H'FE94 8040	32
External access address map register 88	LREMAP88	R/W	H'FE94 8044	32
External access address map register 90	LREMAP90	R/W	H'FE94 8048	32
External access address map register 98	LREMAP98	R/W	H'FE94 804C	32
External access address map register A0	LREMAPA0	R/W	H'FE94 8050	32
External access address map register A8	LREMAPA8	R/W	H'FE94 8054	32
External access address map register B0	LREMAPB0	R/W	H'FE94 8058	32
External access address map register B8	LREMAPB8	R/W	H'FE94 805C	32
Virtual MERAM0A allocation register	LRPG0A	R/W	H'FE94 8080	32

Register Name	Abbr.	R/W	Address	Access Size
Virtual MERAM0A external memory address register	LRSD0A	R/W	H'FE94 8084	32
Virtual MERAM0B allocation register	LRPG0B	R/W	H'FE94 8088	32
Virtual MERAM0B external memory address register	LRSD0B	R/W	H'FE94 808C	32
Virtual MERAM1A allocation register	LRPG1A	R/W	H'FE94 8090	32
Virtual MERAM1A external memory address register	LRSD1A	R/W	H'FE94 8094	32
Virtual MERAM1B allocation register	LRPG1B	R/W	H'FE94 8098	32
Virtual MERAM1B external memory address register	LRSD1B	R/W	H'FE94 809C	32
Virtual MERAM2A allocation register	LRPG2A	R/W	H'FE94 80A0	32
Virtual MERAM2A external memory address register	LRSD2A	R/W	H'FE94 80A4	32
Virtual MERAM2B allocation register	LRPG2B	R/W	H'FE94 80A8	32
Virtual MERAM2B external memory address register	LRSD2B	R/W	H'FE94 80AC	32
Virtual MERAM3A allocation register	LRPG3A	R/W	H'FE94 80B0	32
Virtual MERAM3A external memory address register	LRSD3A	R/W	H'FE94 80B4	32
Virtual MERAM3B allocation register	LRPG3B	R/W	H'FE94 80B8	32
Virtual MERAM3B external memory address register	LRSD3B	R/W	H'FE94 80BC	32

Table 39.8 States of Registers in Each Mode

Register Abbreviation	Reset*	Module Standby
LRCTRL	Initialized	Retained
LRIER	Initialized	Retained
LRISR	Initialized	Retained
LRSR	Initialized	Retained
LRLPRSR	Initialized	Retained
LRIAR1	Initialized	Retained
LRIAR2	Initialized	Retained
LRXAR2	Initialized	Retained
LRMAR1	Initialized	Retained
LRMAR2	Initialized	Retained
LREBUFC	Initialized	Retained
LREBUFP	Initialized	Retained
LREMAP80 to B8	Initialized	Retained
LRPGxx	Initialized	Retained
LRSDxx	Initialized	Retained

Note: For reset conditions, refer to section 4.2, Reset Range in LSI Information.

39.7.1 LCD Refresh Control Register (LRCTRL)

LRCTRL switches between the normal operation mode and the refresh mode.

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 8	CRAB1[3:0] CRAB0[3:0]	00	R/W	LCDC use register surface combination switch Switch the register surface used by the LCDC, in synchronization with the LCDC's state transition between the refresh mode and the normal mode. These bits are automatically cleared to B'0000 when state transition is completed. CRAB0 and CRAB1 are set for the LCDC0 and the LCDC1, respectively. CRAB[3]: Specifies the register surface to be used by the sub LCD after a switch between the modes is made. 0: A surface 1: B surface CRAB[2]: Sub LCD switch enable 0: Does not switch the register surface used by the sub LCD. 1: Switches the register surface used by the sub LCD. CRAB[1]: Specifies the register surface to be used by the main LCD after a switch between the modes is made. 0: A surface 1: B surface CRAB[0]: Main LCD switch enable 0: Does not switch the register surface used by the main LCD. 1: Switches the register surface used by the main LCD.

Bit	Bit Name	Initial Value	R/W	Description
7	LROFF1	0	R	LCDC1 normal operation mode select Writing B'1 to this bit switches the LCDC1 to the normal operation mode. Transition is made during a blanking period, and this bit is automatically cleared to B'0 when the transition is completed. 0: NOP 1: Switches the LCDC1 from the refresh mode to the normal mode
6	LRON1	0	R	LCDC1 Refresh Mode Select Writing B'1 to this bit switches the LCDC1 to the refresh mode. Transition is made during a blinking period, and this bit is automatically cleared to B'0 when the transition is completed. 0: NOP 1: Switches the LCDC1 from the normal operation mode to the refresh mode.
5	LROFF0	0	R	LCDC0 normal operation mode select Writing B'1 to this bit switches the LCDC0 to the normal operation mode. Transition is made during a blinking period, and this bit is automatically cleared to B'0 when the transition is completed. 0: NOP 1: Switches the LCDC0 from the refresh mode to the normal operation mode.
4	LRON0	0	R	LCDC0 refresh mode select Writing B'1 to this bit switches the LCDC0 to the refresh mode. Transition is made during a blinking period, and this bit is automatically cleared to B'0 when the transition is completed. 0: NOP 1: Switches the LCDC0 from the normal operation mode to the refresh mode.
3, 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
1	LROFF	0	R/W	Normal operation mode select Writing B'1 to this bit switches the LCDC0 and the LCDC1 to the normal operation mode. Transition is made during a blinking period, and this bit is automatically cleared to B'0 when the transition is completed. 0: NOP 1: Makes the transition from the refresh mode to the normal operation mode
0	LRON	0	R/W	Refresh mode select Writing B'1 to this bit switches the LCDC0 and the LCDC1 to the refresh mode. Transition is made during a blinking period, and this bit is automatically cleared to B'0 when the transition is completed. 0: NOP 1: Makes the transition from the normal operation mode to the refresh mode

Note: Do not set the LROFF bit and the LRON bit to 1 at the same time.

39.7.2 LCD Refresh Interrupt Enable Register (LRIER)

LRIER specifies the start points of interrupts.

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	A2IE	0	R/W	LCDC access address interrupt 2 enable Determines whether to generate an interrupt when the LCDC accesses the address specified in LRIAR2. 0: Does not generate an interrupt when the LCDC accesses the address specified in LRIAR2 1: Generates an interrupt when the LCDC accesses the address specified in LRIAR2
8	AIE	0	R/W	LCDC access address interrupt enable Determines whether to generate an interrupt when the LCDC accesses the address specified in LRIAR. 0: Does not generate an interrupt when the LCDC accesses the address specified in LRIAR 1: Generates an interrupt when the LCDC accesses the address specified in LRIAR
7	OFFIE1	0	R/W	LCDC1 normal operation mode transition completion interrupt enable Determines whether to generate an interrupt when the transition of the LCDC1 to the normal operation mode is completed. 0: Does not generate an interrupt when the transition to the normal operation mode is completed 1: Generates an interrupt when the transition to the normal operation mode is completed

Bit	Bit Name	Initial Value	R/W	Description
6	ONIE1	0	R/W	LCDC1 refresh mode transition completion interrupt enable Determines whether to generate an interrupt when the transition of the LCDC1 to the refresh mode is completed. 0: Does not generate an interrupt when the transition to the refresh mode is completed 1: Generates an interrupt when the transition to the refresh mode is completed
5	OFFIE0	0	R/W	LCDC0 normal operation mode transition completion interrupt enable Determines whether to generate an interrupt when the transition of the LCDC0 to the normal operation mode is completed. 0: Does not generate an interrupt when the transition to the normal operation mode is completed 1: Generates an interrupt when the transition to the normal operation mode is completed
4	ONIE0	0	R/W	LCDC0 refresh mode transition completion interrupt enable Determines whether to generate an interrupt when the transition of the LCDC0 to the refresh mode is completed. 0: Does not generate an interrupt when the transition to the refresh mode is completed 1: Generates an interrupt when the transition to the refresh mode is completed
3, 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	OFFIE	0	R/W	Normal operation mode transition completion interrupt enable Determines whether to generate an interrupt when the transition of the LCDC0 and the LCDC1 to the normal operation mode is completed. 0: Does not generate an interrupt when the transition to the normal operation mode is completed 1: Generates an interrupt when the transition to the normal operation mode is completed

Bit	Bit Name	Initial Value	R/W	Description
0	ONIE	0	R/W	Refresh mode transition completion interrupt enable Determines whether to generate an interrupt when the transition of the LCDC0 and the LCDC1 to the refresh mode is completed. 0: Does not generate an interrupt when the transition to the refresh mode is completed 1: Generates an interrupt when the transition to the refresh mode is completed

39.7.3 LCD Refresh Interrupt Source Register (LRISR)

LRISR indicates the interrupt status.

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	A2IS	0	R/W	LCDC access address interrupt 2 state This bit is B'1 when an LCDC access address interrupt 2 occurs. This bit must be cleared by writing B'0 in an interrupt handling routine. 0: Indicates that an LCDC access address interrupt 2 has not occurred or that notification of completion of handling the interrupt has been received. 1: Indicates that an LCDC access address interrupt 2 has occurred and notification of completion of handling the interrupt has not been received.
8	AIS	0	R/W	LCDC access address interrupt state This bit is B'1 when an LCDC access address interrupt occurs. This bit must be cleared by writing B'0 in an interrupt handling routine. 0: Indicates that an LCDC access address interrupt has not occurred or that notification of completion of handling the interrupt has been received. 1: Indicates that an LCDC access address interrupt has occurred and notification of completion of handling the interrupt has not been received.

Bit	Bit Name	Initial Value	R/W	Description
7	OFFIS1	0	R/W	LCDC1 normal operation mode transition completion interrupt state This bit is B'1 when an LCDC1 normal operation mode transition completion interrupt occurs. This bit must be cleared by writing B'0 in an interrupt handling routine. 0: Indicates that a normal operation mode transition completion interrupt has not occurred or that notification of completion of handling the interrupt has been received. 1: Indicates that a normal operation mode transition completion interrupt has occurred and notification of completion of handling the interrupt has not been received.
6	ONIS1	0	R/W	LCDC1 refresh mode transition completion interrupt state This bit is B'1 when an LCDC1 refresh mode transition completion interrupt occurs. This bit must be cleared by writing B'0 in an interrupt handling routine. 0: Indicates that a refresh mode transition completion interrupt has not occurred or that notification of completion of handling the interrupt has been received. 1: Indicates that a refresh mode transition completion interrupt has occurred and notification of completion of handling the interrupt has not been received.
5	OFFIS0	0	R/W	LCDC0 normal operation mode transition completion interrupt state This bit is B'1 when an LCDC0 normal operation mode transition completion interrupt occurs. This bit must be cleared by writing B'0 in an interrupt handling routine. 0: Indicates that a normal operation mode transition completion interrupt has not occurred or that notification of completion of handling the interrupt has been received. 1: Indicates that a normal operation mode transition completion interrupt has occurred and notification of completion of handling the interrupt has not been received.

Bit	Bit Name	Initial Value	R/W	Description
4	ONIS0	0	R/W	LCDC0 refresh mode transition completion interrupt state This bit is B'1 when an LCDC0 refresh mode transition completion interrupt occurs. This bit must be cleared by writing B'0 in an interrupt handling routine. 0: Indicates that a refresh mode transition completion interrupt has not occurred or that notification of completion of handling the interrupt has been received. 1: Indicates that a refresh mode transition completion interrupt has occurred and notification of completion of handling the interrupt has not been received.
3, 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	OFFIS	0	R/W	Normal operation mode transition completion interrupt state This bit is B'1 when LCDC0 and LCDC1 normal operation mode transition completion interrupt occurs. This bit must be cleared by writing B'0 in an interrupt handling routine. 0: Indicates that a normal operation mode transition completion interrupt has not occurred or that notification of completion of handling the interrupt has been received. 1: Indicates that a normal operation mode transition completion interrupt has occurred and notification of completion of handling the interrupt has not been received.
0	ONIS	0	R/W	Refresh mode transition completion interrupt state This bit is B'1 when LCDC0 and LCDC1 refresh mode transition completion interrupt occurs. This bit must be cleared by writing B'0 in an interrupt handling routine. 0: Indicates that a refresh mode transition completion interrupt has not occurred or that notification of completion of handling the interrupt has been received. 1: Indicates that a refresh mode transition completion interrupt has occurred and notification of completion of handling the interrupt has not been received.

39.7.4 LCD Refresh Status Register (LRSR)

LRSR indicates the status concerning LCD refresh operation.

Bit	Bit Name	Initial Value	R/W	Description
31 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6	MS1	0	R	LCDC1 mode status This bit indicates the LCDC1 operation mode. 0: Normal operation mode 1: LCD refresh mode
5	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
4	MS0	0	R	LCDC0 mode status This bit indicates the LCDC0 operation mode. 0: Normal operation mode 1: LCD refresh mode
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	MS	0	R	Mode status This bit indicates the operation mode of the LCDC0 and the LCDC1. 0: Normal operation mode 1: LCD refresh mode

39.7.5 MERAM Mode Set Register (LRLPRSR)

LRLPRSR specifies the MERAM operation mode. The resume standby mode (RS mode, memory retained, read/write impossible) can be entered by compulsion or in synchronization with the refresh mode.

Bit	Bit Name	Initial Value	R/W	Description
31 to 19	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
18	FRS2	0	R/W	MERAM (1024 to 1536 KB) compulsory RS mode set Selects whether to force the MERAM area (1024 to 1536 KB) to enter the RS mode. 0: Forces the MERAM (1024 to 1536 KB) to enter the normal mode 1: Forces the MERAM (1024 to 1536 KB) to enter the RS mode
17	FRS1	0	R/W	MERAM (512 to 1024 KB) compulsory RS mode set Selects whether to force the MERAM area (512 to 1024 KB) to enter the RS mode. 0: Forces the MERAM (512 to 1024 KB) to enter the normal mode 1: Forces the MERAM (512 to 1024 KB) to enter the RS mode
16	FRS0	0	R/W	MERAM (0 to 512 KB) compulsory RS mode set Selects whether to force the MERAM area (0 to 512 KB) to enter the RS mode. 0: Forces the MERAM (0 to 512 KB) to enter the normal mode 1: Forces the MERAM (0 to 512 KB) to enter the RS mode
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
14	RRS2	0	R/W	MERAM refresh mode synchronize RS mode set Selects whether to allow the MERAM (1024 to 1536 KB) to enter the RS mode in synchronization with the refresh mode. 0: Makes the MERAM (1024 to 1536 KB) enter the normal mode when the transition from the refresh mode to the normal mode is made 1: Makes the MERAM (1024 to 1536 KB) enter the RS mode when the transition from the normal mode to the refresh mode is made
13	RRS1	0	R/W	MERAM refresh mode synchronize RS mode set Selects whether to allow the MERAM (512 to 1024 KB) to enter the RS mode in synchronization with the refresh mode. 0: Makes the MERAM (512 to 1024 KB) enter the normal mode when the transition from the refresh mode to the normal mode is made 1: Makes the MERAM (512 to 1024 KB) enter the RS mode when the transition from the normal mode to the refresh mode is made
12	RRS0	0	R/W	MERAM refresh mode synchronize RS mode set Selects whether to allow the MERAM (0 to 512 KB) to enter the RS mode in synchronization with the refresh mode. 0: Makes the MERAM (0 to 512 KB) enter the normal mode when the transition from the refresh mode to the normal mode is made 1: Makes the MERAM (0 to 512 KB) enter the RS mode when the transition from the normal mode to the refresh mode is made
11 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

39.7.6 Interrupt Address Register (LRIAR)

LRIAR stores the address that serves as a trigger for generating LCDC access address interrupts. When B'1 is written to the LRIER.AIE bit and the LCDC0 or the LCDC1 accesses the address stored in the LRIAR, an LCDC access address interrupt occurs.

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	IA[31:3]	H'FFFF FFF8	R/W	Indicate the address that causes LCDC access address interrupts.
2 to 0	IA[2:0]		R	

39.7.7 Interrupt Address Register2 (LRIAR2)

LRIAR2 stores address 2 that serves as a trigger for generating LCDC access address interrupts. When B'1 is written to the LRIER.A2IE bit and the LCDC0 or the LCDC1 accesses the address stored in the LRIAR2, an LCDC access address interrupt 2 occurs.

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	IA2[31:3]	H'FFFF FFF8	R/W	Indicate the address that causes LCDC access address interrupt2s.
2 to 0	IA2[2:0]			

39.7.8 Extended Address Register2 (LRXAR2)

LRXAR2 stores the SDRAM address at which additional data is stored when the display data size of the LCDC0 or the LCDC1 exceeds the MERAM capacity.

Note: Refer to the notes on the LRMAR2 register.

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	XA2[31:3]	H'FFFF FFF8	R/W	Indicate the extended LCDC address.
2 to 0	XA2[2:0]		R	This address must be 32-byte aligned.

39.7.9 Memory Boundary Address Register1 (LRMAR1)

When the display data size of the LCDC0 or the LCDC1 exceeds the MERAM capacity, LRMAR1 stores the address of the boundary between the SDRAM and the MERAM in which data is stored.

Note: Refer to the notes on the LRMAR2 register.

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	MA1[31:3]	H'E558 0000	R/W	Indicate the LCDC memory boundary address. An address equal to or larger than the value of this register corresponds to a location in the MERAM. The value must be chosen from the MERAM range from H'E558 0000 to H'E56F FFFF. The address must be specified on a 4-KB basis. If it is not specified on a 4-KB basis, it is rounded down to a 4-KB-unit value.
2 to 0	MA1[2:0]		R	

39.7.10 Memory Boundary Address Register2 (LRMAR2)

When the display data size of the LCDC0 or the LCDC1 exceeds the MERAM capacity, LRMAR2 stores the address of the boundary between the SDRAM and the MERAM in which data is stored.

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	MA2[31:3]	H'E570 0000	R/W	Indicate the LCDC memory boundary address. An address equal to or larger than the value of this register corresponds to a location in the MERAM. The value must be chosen from the MERAM range from H'E558 0000 to H'E56F FFFF. The address must be specified on a 4-KB basis. If it is not specified on a 4-KB basis, it is rounded up to a 4-KB-unit value.
2 to 0	MA2[2:0]		R	

Notes: 1. Access by the LCDC0/LCDC1 to virtual addresses H'E5580000 to H'E56F0000 is converted into access to the virtual MERAM space 0A (H'F0000000 to H'F01F0000), and then is converted into access to the internal MERAM or the external memory according to the settings of the LRPG0A and the LRSD0.

2. When any of the values of LRXAR2, LRMAR1, and LRMAR2 is changed, the values of LRPG0A and LRSD0 are updated to ensure appropriate operation. Note, however, that this conversion processing may not be implemented in future products. Therefore, it is recommended to use the LRPG0A and LRSD0A registers instead of the LRXAR2, LRMAR1, and LRMAR2 registers.

3. The relation of the values of LRXAR2, LRMAR1, and LRMAR2 to the automatically converted values of LRPG0A and LRSD0 is as follows:
LRPG0A.MSA[11:0] = INT((LRMAR1-H'e5580000)/4096)
LRPG0A.MSZ[11:0] = ROUNDUP((LRMAR2-H'e5580000)/4096) - LRPG0A.MSA[11:0]
LRSD0A[31:0] = LRXAR2 - LRPG0A.MSZ[11:0]*4096

4. The function, which was defined in LRXAR1 and LRMAR1, to convert access to an MERAM address less than the value of LRMAR1 into access to the external memory is not supported any more. The LRXAR1 register has been removed.

39.7.11 External Access Control Register (LREBUFC)

When the LCDC0 or the LCDC1 is in the LCD refresh mode and the external memory is accessed for read operation, the MERAM performs read fill operation from the external memory to place data in a read buffer area allocated in the internal MERAM. Then, the LCDC0/LCDC1 accesses the data.

This register controls read fill operation from the external memory.

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	PRIF[3:0]	H'9	R/W	Set priority levels for external buses in read fill operation from the external memory. PRIF indicates the priority levels for the first requests in lines, and PRIC indicates the priority levels for the subsequent requests. For details on the priority levels, refer to 6.2 SHwy Bus Functions.
27 to 24	PRIC[3:0]	H'B		
23 to 1	—	All 0	R	Reserved
0	EN	H'1	R/W	Be sure to write 1 to this bit.

39.7.12 External Access Read Buffer Allocation Register (LREBUFP)

When the LCDC0/LCDC1 is in the LCD refresh mode and access to the external memory is required, it is necessary to secure a 4-KB read fill buffer area in the internal MERAM. This register specifies the address of this read fill buffer area.

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	H'0	R	Reserved
27 to 16	RBUF1[11:0]	H'17F	R/W	Specify the address of a read fill buffer for the LCDC1 on a 4-KB basis. The address must be (8n + 4) KB.
15 to 12	—	H'0	R	Reserved
11 to 0	RBUF0[11:0]	H'17E	R/W	Specify the address of a read fill buffer for the LCDC0 on a 4-KB basis. The address must be 8n KB.

39.7.13 External Access Map Register 80 to B8 (LREMAP80 to B8)

When the LCDC0/LCDC1 is in the LCD refresh mode and an attempt to access the external memory is made, the virtual address is converted into a physical address according to the settings of these registers if the virtual address is in the PMB conversion target space (H'8000_0000 to H'BFFF_FFFF).

The virtual address space is converted on a 128-MB basis. xx in a register name (LREMAPxx) corresponds to a virtual page number.

Bit	Bit Name	Initial Value	R/W	Description
31 to 26	PPN [31:26]	*1	R/W	Specify the physical page number to be converted.
25 to 0	—	H'0	R	Reserved

Notes: 1. The initial value of LREMAPxx (xx = 80, 90, a0, and b0) is 0, and that of LREMAPyy (yy = 88, 98, a8, and b8) is 5'b0000_1.
2. The virtual addresses in the range from 32'H00000000 to 32'H7FFF_FFFF are not correctly converted. Therefore, they cannot be used as external access addresses in the LCD refresh mode.
3. Even when MEVCR1.AMD = 0, the virtual addresses in the range from 32'H80000000 to 32'HBFFFFFFF are converted according to the settings of these registers, and these addresses provide access to the external memory.

39.7.14 Virtual MERAM Allocation Registers 0A to 3B (LRPG0A to 3B)

Access by the LCDC0/LCDC1 to the virtual address space from H'F0000000 to H'F3FFFFFF is regarded as access to the virtual MERAM space regardless of whether the LCD refresh mode is being used.

The virtual MERAM space is divided into eight 8-MB pages. Access to each virtual MERAM page (MERAM_xx) is address-converted into the internal MERAM or the external memory space by using the virtual MERAM allocation registers xx (LRPGxx) and the virtual MERAM external address registers xx (LRSDxx).

Also, when a frame buffer cache is in use, the transition to the LCD refresh mode is automatically translated as access to the virtual MERAM space. LRPG0A and LRSD0A manage access to the ICB A surface, and LRPG0A and LRSD0B manage access to the ICB B surface.

Virtual Address Range	Virtual MERAM Page Name
H'F000_0000 to H'F07F_0000	MERAM_0A
H'F080_0000 to H'F0FF_0000	MERAM_0B
H'F100_0000 to H'F17F_0000	MERAM_1A
H'F180_0000 to H'F1FF_0000	MERAM_1B
H'F200_0000 to H'F27F_0000	MERAM_2A
H'F280_0000 to H'F2FF_0000	MERAM_2B
H'F300_0000 to H'F37F_0000	MERAM_3A
H'F380_0000 to H'F3FF_0000	MERAM_3B

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	0	R	Reserved
27 to 16	MSA[11:0]	0	R/W	Specify the start address in the actual MERAM, where the in-page offset == 0 is allocated, on a 4-KB basis.
15 to 12	—	0	R	Reserved
11 to 0	MSZ[11:0]	0	R/W	Specify the data size in the actual MERAM on a 4-KB basis. Access to a range exceeding this size is regarded as access to the external memory. When MSZ = 0, all access to pages is regarded as access to the external memory. In this case, the value of MSA is not used.

39.7.15 Virtual MERAM External Address Registers 0A to 3B (LRSD0A to 3B)

These registers specify the external memory address corresponding to the in-page offset = 0 of the virtual MERAM pages (MERAM_xx, xx = 0A, 0B, 1A, 1B, 2A, 2B, 3A, and 3B), as a physical address.

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PPN[31:0]	0	R/W	Specify the physical address of an external memory address corresponding to the offset (= 0) of the virtual MERAM pages, on a 256-byte basis. Access where the in-page offset address exceeds LRPGxx.MSZ*4KB is converted into access to (LRSDxx.PPN + in-page offset).

Section 40 LCD Controller (LCDC)

The LCD controller (LCDC) reads display data from an external memory . The LCDC uses the palette memory to determine the colors according to the settings and then sends the data to the LCD module. This LCDC allows connection of TFT LCD modules that support the RGB interface or the 80-Series CPU's bus interface (SYS interface) (excludes LCD modules with the NTSC/PAL type or LVDS interface.).

This LSI has two LCD modules (LCDC0, LCDC1).

40.1 Features

(1) Features of the LCDC

- Supports TFT LCD modules
- Supports two types interfaces as LCD module interface
  RGB interface (8/9/12/16/18/24-bit data bus width)
  80-Series CPU's bus interface (SYS interface, 8/9/12/16/18/24-bit data bus width)
- SYS interface supports the following input/output mode for the LCD module
  LCD module: VSYNC input and output modes
- Supports 8/12/16/18/24-bpp display image data formats
- Display image data is read in continuous or one-shot mode: continuous mode where display image data is continuously read according to the refresh rate of the LCD module and one-shot mode where display image data is read at intervals of the frame rate.
- Display image data is read in full or partial screen mode: full screen mode where the size of the display image data to be read depends on the panel size of the LCD module and partial screen mode where the size of the display image data to be read depends on the size of the screen to be updated.
- Each of the RGB colors can be corrected by the 256-entry, 24-bit-input/output internal color palette memory
- Supports inversion of output signals to agree with the LCD module's signal polarity
- Interrupts can be generated every frame or user-specified line
- YCbCr/RGB signals read are converted into YCbCr/RGB signals for output
- Supports tabular mode (display images are doubled horizontally and vertically)
- The child screen can be arranged in four places maximum in the display image data. The alpha blend function can be used in two systems and the ROP3 function be used in two systems.
- The source of the dot clock can be chosen with the bus clock, external input clock, and two interface clock
  LCDC0: the bus clock, MIPI-DSI byte clock, external input clock
  LCDC1: the bus clock, MIPI-DSI byte clock, HDMI clock, external input clock

Tables 40.1 show the LCDC functions respectively.

Table 40.1 LCDC Functions

Item		Function	Remakes
Input data format	8 bpp	RGB 332	
	12 bpp	RGB 444	
	16 bpp	RGB 565	
	18 bpp	RGB 666	
		BGR 666	
	24 bpp	RGB 888	
		BGR 888	
	YCbCr	YCbCr 4:2:0, 4:2:2, 4:4:4	
Output data format	RGB interface	RGB8	3 cycle/pixel
		RGB9	2 cycle/pixel
		RGB12a	2 cycle/pixel
		RGB12b	1 cycle/pixel
		RGB16	1 cycle/pixel
		RGB18	1 cycle/pixel
		RGB24	1 cycle/pixel
		YCbCr 4:2:2 16-bit output	2 cycle/pixel
	SYS interface	SYS8a/8b/8c	3 cycle/pixel
		SYS8d	2 cycle/pixel
		SYS9	2 cycle/pixel
		SYS12	2 cycle/pixel
		SYS16a	1 cycle/pixel
		SYS16b/16c	2 cycle/pixel
		SYS18	1 cycle/pixel
		SYS24	1 cycle/pixel
	Display data write-back	WB8a	• Packed format available • Write-back operation in units of 32 bits • Byte or word swap
		WB8d	
		WB9	
		WB16	
		WB18	
		WB24	

Item		Function	Remakes
LCD driver interface	RGB interface	Interface with HSYNC and VSYNC • Polarity inversion • Output pulse width and position setting	
	SYS interface	80-Series bus interface • Support of VSYNC input/output	
Dot clock	Source clock	Bus clock, external input clock, two peripheral clock	
	Division ratio	n/m m = 60, 54, 48, 42 $1 \leq n \leq m/3, m/2$	
Interrupt	User setting	Interrupt generated when reading of specified lines of data is completed	
	Frame	Interrupt generated when the first pixel data of a frame starts to be output	
		Interrupt generated when output of the last pixel data of a frame is completed	
	VRAM read	Interrupt generated when access to a frame of data in VRAM is completed	
		Interrupt generated when access to a line of data in VRAM is completed	
	VSYNC	Interrupt generated when VSYNC is asserted	
		Interrupt generated when VSYNC is negated	
Display image	Image data read	Image data read depending on the refresh rate of LCD module	
		Image data read depending on the frame rate of display image	
	Display image size	Full screen	
		Only the specified area is updated.	
	Image data processing	Each color of R, G, and B is converted using the color palette • 256 entries • 24-bit input/output	
Format conversion	YCbCr ⇔ RGB	YCbCr data is converted into RGB for output. RGB data is converted into YCbCr for output	

Figures 40.1 is block diagram of the LCDC respectively.

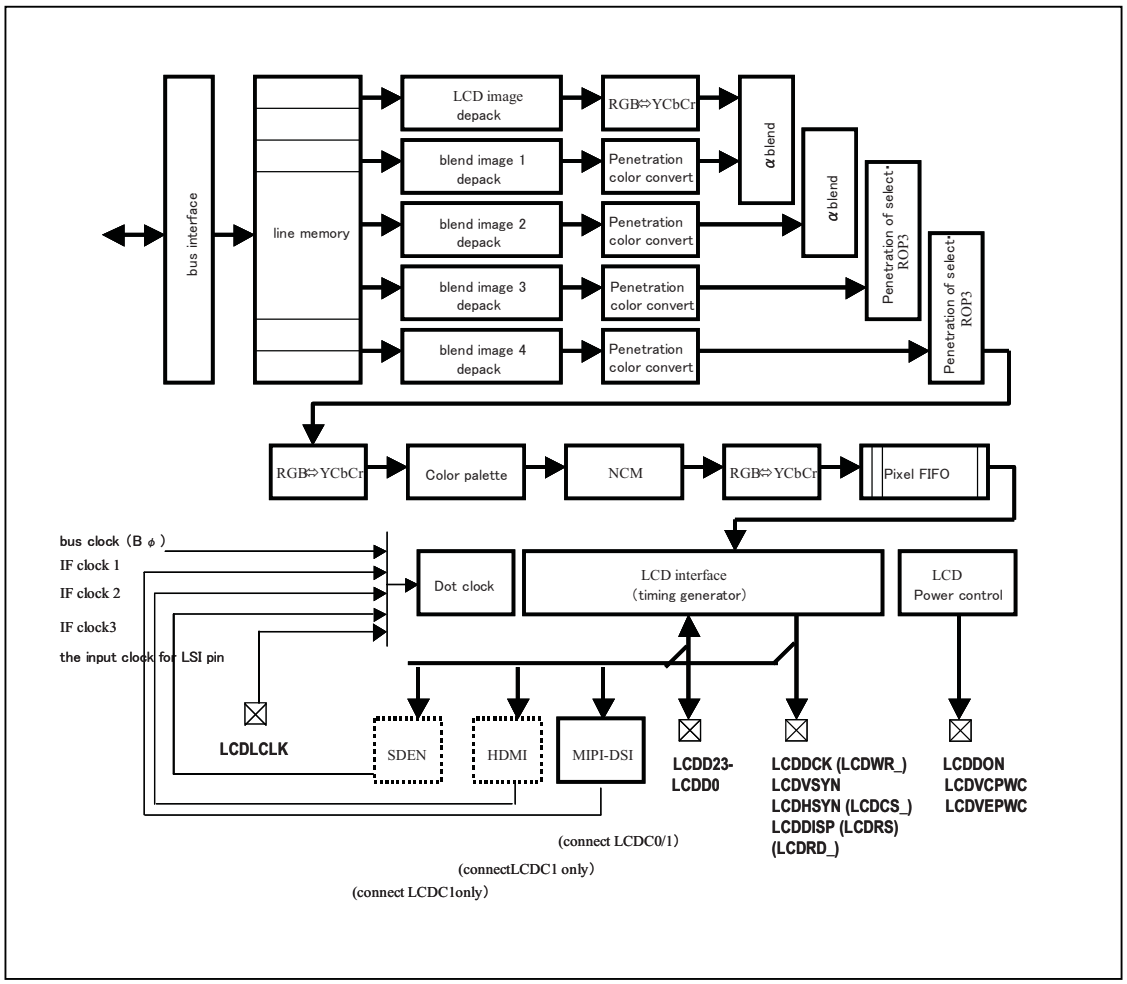


Figure 40.1 Block Diagram of LCDC

40.2 Input/Output Pins

Table 40.2 shows the pin configurations of the LCDC.

Table 40.2 Pin Configurations

Name	Function	I/O	Description
LCDDON	Display on signal	Output	Display start signal (DON) for LCD
LCDVCPWC	Power control	Output	LCD module power control (V_{CC})
LCDVEPWC	Power control	Output	LCD module power control (V_{EE})
LCDDCK/ $\overline{\text{LCDWR}}$	Dot clock/ write strobe	Output	Dot clock signal (RGB interface)/write strobe signal (SYS interface)
LCDVSYN	Vertical sync signal	Output/ I/O	Vertical sync signal (VSYNC) for LCD Output for RGB interface, or I/O for SYS interface
LCDHSYN/ $\overline{\text{LCDCS}}$	Horizontal sync signal/chip select	Output	Horizontal sync signal (RGB interface)/chip select signal for LCD (SYS interface)
LCDDISP/ LCDRS	Display enable/ Register select	Output	Display enable signal (RGB interface)/register select signal (SYS interface)
$\overline{\text{LCDRD}}$	Read strobe	Output	Read strobe signal (SYS interface)
LCDD23 to LCDD0	LCD data bus	Output/ I/O	LCD panel data (output for RGB interface, or I/O for SYS interface)
LCDLCLK	Input clock	Input	LCD source clock (external input, optional)

40.3 Register Descriptions

Table 40.3 shows the register configuration of the LCDC. Table 40.4 shows the states of the registers in each mode.

Most of the LCDC registers have a double-buffered mechanism (register sets A and B, or current and program side). Each register incorporated in the LCDC consists of two sets of registers (excluding some registers). An incorporated register with two sets of registers has a mirror address to access the register set not currently being used. The register which has a name in a register set name makes them one set, and controlled as two structure on a current side and the program side.

*Note

The address of LCDC0 register : H'FE940000 ~ H'FE943FFF
The address of LCDC1 register : H'FE944000 ~ H'FE947FFF

Table 40.3 Register Configurations

- LCDC Register Configurations

			Address			
Register Name	Symbol	R/W	Address (Set A/ current)	Address (Set B/ program)	Mirror Address	Access Size
LCDC palette data registers 00 to FF	LDPR00 to LDPRFF	R/W	H'FE94 0000 to H'FE94 03FC	—	—	32
LCD dot clock pattern set register 1	MLDDCKPAT1R	R/W	H'FE94 0400	—	—	32
LCD dot clock pattern set register 2	MLDDCKPAT2R	R/W	H'FE94 0404	—	—	32
LCDC dot clock register	LDDCKR	R/W	H'FE94 0410	—	—	32
Dot clock stop register	LDDCKSTPR	R/W	H'FE94 0414	—	—	32
LCD module type register 1	MLDMT1R	R/W	H'FE94 0418	H'FE94 1418	H'FE94 2418	32
LCD module type register 2	MLDMT2R	R/W	H'FE94 041C	H'FE94 141C	H'FE94 241C	32
LCD module type register 3	MLDMT3R	R/W	H'FE94 0420	H'FE94 1420	H'FE94 2420	32
LCD data format register	MLDDFR	R/W	H'FE94 0424	H'FE94 1424	H'FE94 2424	32
LCD scan mode register 1	MLDSM1R	R/W	H'FE94 0428	H'FE94 1428	H'FE94 2428	32
LCD scan mode register 2	MLDSM2R	R/W	H'FE94 042C	—	—	32
LCD display data read start address register 1	MLDSA1R	R/W	H'FE94 0430	H'FE94 1430	H'FE94 2430	32
LCD display data read start address register 2	MLDSA2R	R/W	H'FE94 0434	H'FE94 1434	H'FE94 2434	32
LCD display data storing memory line size register	MLDMLSR	R/W	H'FE94 0438	H'FE94 1438	H'FE94 2438	32
LCD write-back data format register	MLDWBFR	R/W	H'FE94 043C	H'FE94 143C	H'FE94 243C	32
LCD write-back control register	MLDWBCNTR	R/W	H'FE94 0440	H'FE94 1440	H'FE94 2440	32
LCD write-back start address register	MLDWBAR	R/W	H'FE94 0444	H'FE94 1444	H'FE94 2444	32
LCD horizontal character number register	MLDHCNR	R/W	H'FE94 0448	H'FE94 1448	H'FE94 2448	32
LCD horizontal sync signal register	MLDHSYNR	R/W	H'FE94 044C	H'FE94 144C	H'FE94 244C	32
LCD vertical line number register	MLDVLNR	R/W	H'FE94 0450	H'FE94 1450	H'FE94 2450	32

Register Name	Symbol	R/W	Address (Set A/ current)	Address (Set B/ program)	Mirror Address	Access Size
			Address			
LCD vertical sync signal register	MLDVSYNR	R/W	H'FE94 0454	H'FE94 1454	H'FE94 2454	32
LCD horizontal partial display register	MLDHPDR	R/W	H'FE94 0458	H'FE94 1458	H'FE94 2458	32
LCD vertical partial display register	MLDVPDR	R/W	H'FE94 045C	H'FE94 145C	H'FE94 245C	32
LCD power management register	MLDPMR	R/W	H'FE94 0460	—	—	32
LCDC palette control register	LDPALCR	R/W	H'FE94 0464	—	—	32
LCDC interrupt register	LDINTR	R/W	H'FE94 0468	—	—	32
LCDC status register	LDSR	R	H'FE94 046C	—	—	32
LCDC control register 1	LDCNT1R	R/W	H'FE94 0470	—	—	32
LCDC control register 2	LDCNT2R	R/W	H'FE94 0474	—	—	32
LCDC register set change control register	LDRCNTR	R/W	H'FE94 0478	—	—	32
LCDC input image data swap register	LDDDSR	R/W	H'FE94 047C	—	—	32
LCDC register set forcible select register	LDRCR	R/W	H'FE94 0484	—	—	32
Tabular mode register	LDDBSLMR	R/W	H'FE94_0490	—	—	32
Horizontal slide number register	LDSLHPNR	R/W	H'FE94_0494	—	—	32
Vertical slide number register	LDSLVLNR	R/W	H'FE94_0498	—	—	32
Slide data register	LDSLRGBR	R/W	H'FE94_049C	—	—	32
LCD horizontal sync signal adjust register	MLDHAJR	R/W	H'FE94 04A0	H'FE94 14A0	H'FE94 24A0	32
LCD vertical sync signal delay register	MLDIVSNR	R/W	H'FE94 04A4	—	—	32
LCDC driver write data register 0	LDDWD0R	R/W	H'FE94 0800	—	—	32
LCDC driver write data register 1	LDDWD1R	R/W	H'FE94 0804	—	—	32
LCDC driver write data register 2	LDDWD2R	R/W	H'FE94 0808	—	—	32
LCDC driver write data register 3	LDDWD3R	R/W	H'FE94 080C	—	—	32
LCDC driver write data register 4	LDDWD4R	R/W	H'FE94 0810	—	—	32
LCDC driver write data register 5	LDDWD5R	R/W	H'FE94 0814	—	—	32
LCDC driver write data register 6	LDDWD6R	R/W	H'FE94 0818	—	—	32
LCDC driver write data register 7	LDDWD7R	R/W	H'FE94 081C	—	—	32
LCDC driver write data register 8	LDDWD8R	R/W	H'FE94 0820	—	—	32
LCDC driver write data register 9	LDDWD9R	R/W	H'FE94 0824	—	—	32
LCDC driver write data register A	LDDWDAR	R/W	H'FE94 0828	—	—	32
LCDC driver write data register B	LDDWDBR	R/W	H'FE94 082C	—	—	32
LCDC driver write data register C	LDDWDCR	R/W	H'FE94 0830	—	—	32
LCDC driver write data register D	LDDWDDR	R/W	H'FE94 0834	—	—	32
LCDC driver write data register E	LDDWDER	R/W	H'FE94 0838	—	—	32
LCDC driver write data register F	LDDWDFR	R/W	H'FE94 083C	—	—	32
LCDC driver read data register	LDDRDR	R/W	H'FE94 0840	—	—	32
LCDC driver write access register	LDDWAR	R/W	H'FE94 0900	—	—	32
LCDC driver read access register	LDDRAR	R/W	H'FE94 0904	—	—	32

Register Name	Symbol	R/W	Address (Set A/ current)	Address (Set B/ program)	Mirror Address	Access Size
			Address			
LCDC coefficient RGB register for color management matrix R	LDCMRKRGBR	R/W	H'FE94 0A00	H'FE94 1A00	H'FE94 2A00	32
LCDC coefficient CMY register for color management matrix R	LDCMRKCMYR	R/W	H'FE94 0A04	H'FE94 1A04	H'FE94 2A04	32
LCDC coefficient of hue circle register for color management matrix R	LDCMRK1R	R/W	H'FE94 0A08	H'FE94 1A08	H'FE94 2A08	32
LCDC coefficient of hue circle register for color management matrix R	LDCMRK2R	R/W	H'FE94 0A0C	H'FE94 1A0C	H'FE94 2A0C	32
LCDC coefficient RGB register for color management matrix G	LDCMGKRGBR	R/W	H'FE94 0A10	H'FE94 1A10	H'FE94 2A10	32
LCDC coefficient CMY register for color management matrix G	LDCMGKCMYR	R/W	H'FE94 0A14	H'FE94 1A14	H'FE94 2A14	32
LCDC coefficient of hue circle register 1 for color management matrix G	LDCMGK1R	R/W	H'FE94 0A18	H'FE94 1A18	H'FE94 2A18	32
LCDC coefficient of hue circle register 2 for color management matrix G	LDCMGK2R	R/W	H'FE94 0A1C	H'FE94 1A1C	H'FE94 2A1C	32
LCDC coefficient RGB register for color management matrix B	LDCMBKRGBR	R/W	H’FE94 0A20	H’FE94 1A20	H’FE94 2A20	32
LCDC coefficient CMY register for color management matrix B	LDCMBKCMYR	R/W	H’FE94 0A24	H’FE94 1A24	H’FE94 2A24	32
LCDC coefficient of hue circle register 1 for color management matrix B	LDCMBK1R	R/W	H’FE94 0A28	H’FE94 1A28	H’FE94 2A28	32
LCDC coefficient of hue circle register 2 for color management matrix B	LDCMBK2R	R/W	H'FE94 0A2C	H'FE94 1A2C	H'FE94 2A2C	32
LCDC peak correction coefficient of hue circle register 1 for color management	LDCMHKPR	R/W	H'FE94 0A30	H'FE94 1A30	H'FE94 2A30	32
LCDC peak correction coefficient of hue circle register 2 for color management	LDCMHKQR	R/W	H'FE94 0A34	H'FE94 1A34	H'FE94 2A34	32
LCDC multiplier coefficient select register for color management	LDCMSELR	R/W	H'FE94 0A38	H'FE94 1A38	H'FE94 2A38	32
LCDC color saturation improvement for color management	LDCMTVR	R/W	H'FE94 0A3C	H'FE94 1A3C	H'FE94 2A3C	32
LCDC color saturation improvement select for color management	LDCMTVSELR	R/W	H'FE94 0A40	H'FE94 1A40	H'FE94 2A40	32
LCDC coefficient dither register for color management	LDCMDTHR	R/W	H'FE94 0A44	H'FE94 1A44	H'FE94 2A44	32
LCDC control register for color management	LDCMCNTR	R/W	H'FE94 0A48	H'FE94 1A48	H'FE94 2A48	32
LCDC control register for color palette expander	LDPALECR	R/W	H’FE940A50	H’FE94 1A50	H’FE94 2A50	32
LCDC color palette data start address register	LDPALADD	R/W	H’FE940A54	H’FE94 1A54	H’FE94 2A54	32

Register Name	Symbol	R/W	Address (Set A/ current)	Address (Set B/ program)	Mirror Address	Access Size
			Address			
blend control register	LDBCR	R/W	H'FE940B00	-	-	32
CH 1 source image format register	LDB1BSIFR	*1	H'FE94 0B20	H'FE94 1B20	H'FE94 2B20	32
CH 1 source size register	LDB1BSSZR	*1	H'FE94 0B24	H'FE94 1B24	H'FE94 2B24	32
CH 1 blend location register	LDB1BLOCR	*1	H'FE94 0B28	H'FE94 1B28	H'FE94 2B28	32
CH 1 source memory width register	LDB1BSMWR	*1	H'FE94 0B2C	H'FE94 1B2C	H'FE94 2B2C	32
CH 1 source address Y register	LDB1BSARY	*1	H'FE94 0B30	H'FE94 1B30	H'FE94 2B30	32
CH 1 source address C register	LDB1BSARC	*1	H'FE94 0B34	H'FE94 1B34	H'FE94 2B34	32
CH 1 source address α register	LDB1BSARA	*1	H'FE94 0B38	H'FE94 1B38	H'FE94 2B38	32
CH 1 penetration color control register	LDB1BPPCR	*1	H'FE94 0B3C	H'FE94 1B3C	H'FE94 2B3C	32
CH 1 back ground color register	LDB1BBGCL	*1	H'FE94 0B10	H'FE94 1B10	H'FE94 2B10	32
CH 2 source image format register	LDB2BSIFR	*1	H'FE94 0B40	H'FE94 1B40	H'FE94 2B40	32
CH 2 source size register	LDB2BSSZR	*1	H'FE94 0B44	H'FE94 1B44	H'FE94 2B44	32
CH 2 blend location register	LDB2BLOCR	*1	H'FE94 0B48	H'FE94 1B48	H'FE94 2B48	32
CH 2 source memory width register	LDB2BSMWR	*1	H'FE94 0B4C	H'FE94 1B4C	H'FE94 2B4C	32
CH 2 source address Y register	LDB2BSARY	*1	H'FE94 0B50	H'FE94 1B50	H'FE94 2B50	32
CH 2 source address C register	LDB2BSARC	*1	H'FE94 0B54	H'FE94 1B54	H'FE94 2B54	32
CH 2 source address α register	LDB2BSARA	*1	H'FE94 0B58	H'FE94 1B58	H'FE94 2B58	32
CH 2 penetration color control register	LDB2BPPCR	*1	H'FE94 0B5C	H'FE94 1B5C	H'FE94 2B5C	32
CH 2 back ground color register	LDB2BBGCL	*1	H'FE94 0B14	H'FE94 1B14	H'FE94 2B14	32
CH 3 source image format register	LDB3BSIFR	*1	H'FE94 0B60	H'FE94 1B60	H'FE94 2B60	32
CH 3 source size register	LDB3BSSZR	*1	H'FE94 0B64	H'FE94 1B64	H'FE94 2B64	32
CH 3 blend location register	LDB3BLOCR	*1	H'FE94 0B68	H'FE94 1B68	H'FE94 2B68	32
CH 3 source memory width register	LDB3BSMWR	*1	H'FE94 0B6C	H'FE94 1B6C	H'FE94 2B6C	32
CH 3 source address Y register	LDB3BSARY	*1	H'FE94 0B70	H'FE94 1B70	H'FE94 2B70	32
CH 3 source address C register	LDB3BSARC	*1	H'FE94 0B74	H'FE94 1B74	H'FE94 2B74	32
CH 3 source address α register	LDB3BSARA	*1	H'FE94 0B78	H'FE94 1B78	H'FE94 2B78	32
CH 3 penetration color control register	LDB3BPPCR	*1	H'FE94 0B7C	H'FE94 1B7C	H'FE94 2B7C	32
CH 3 back ground color register	LDB3BBGCL	*1	H'FE94 0B18	H'FE94 1B18	H'FE94 2B18	32
CH 4 source image format register	LDB4BSIFR	*1	H'FE94 0B80	H'FE94 1B80	H'FE94 2B80	32
CH 4 source size register	LDB4BSSZR	*1	H'FE94 0B84	H'FE94 1B84	H'FE94 2B84	32
CH 4 blend location register	LDB4BLOCR	*1	H'FE94 0B88	H'FE94 1B88	H'FE94 2B88	32
CH 4 source memory width register	LDB4BSMWR	*1	H'FE94 0B8C	H'FE94 1B8C	H'FE94 2B8C	32
CH 4 source address Y register	LDB4BSARY	*1	H'FE94 0B90	H'FE94 1B90	H'FE94 2B90	32
CH 4 source address C register	LDB4BSARC	*1	H'FE94 0B94	H'FE94 1B94	H'FE94 2B94	32
CH 4 source address α register	LDB4BSARA	*1	H'FE94 0B98	H'FE94 1B98	H'FE94 2B98	32
CH 4 penetration color control register	LDB4BPPCR	*1	H'FE94 0B9C	H'FE94 1B9C	H'FE94 2B9C	32
CH 4 back ground color register	LDB4BBGCL	*1	H'FE94 0B1C	H'FE94 1B1C	H'FE94 2B1C	32

*1 the program and mirror are R/W, the current is R/O

Table 40.4 Register States in Each Mode

- LCDC Register

Register Symbol	Power-On Reset	Manual Reset	Module Standby	Sleep
LDPR00 to LDPRFF	Initialized	Initialized	Retained	Retained
MLDDCKPAT1R	Initialized	Initialized	Retained	Retained
MLDDCKPAT2R	Initialized	Initialized	Retained	Retained
LDDCKR	Initialized	Initialized	Retained	Retained
LDDCKSTPR	Initialized	Initialized	Retained	Retained
MLDMT1R	Initialized	Initialized	Retained	Retained
MLDMT2R	Initialized	Initialized	Retained	Retained
MLDMT3R	Initialized	Initialized	Retained	Retained
MLDDFR	Initialized	Initialized	Retained	Retained
MLDSM1R	Initialized	Initialized	Retained	Retained
MLDSM2R	Initialized	Initialized	Retained	Retained
MLDSA1R	Initialized	Initialized	Retained	Retained
MLDSA2R	Initialized	Initialized	Retained	Retained
MLDMLSR	Initialized	Initialized	Retained	Retained
MLDWBFR	Initialized	Initialized	Retained	Retained
MLDWBCNTR	Initialized	Initialized	Retained	Retained
MLDWBAR	Initialized	Initialized	Retained	Retained
MLDHCNR	Initialized	Initialized	Retained	Retained
MLDHSYNR	Initialized	Initialized	Retained	Retained
MLDVLNR	Initialized	Initialized	Retained	Retained
MLDVSYNR	Initialized	Initialized	Retained	Retained
MLDHPDR	Initialized	Initialized	Retained	Retained
MLDVPDR	Initialized	Initialized	Retained	Retained
MLDPMR	Initialized	Initialized	Retained	Retained
LDPALCR	Initialized	Initialized	Retained	Retained
LDINTR	Initialized	Initialized	Retained	Retained
LDSR	Initialized	Initialized	Retained	Retained
LDCNT1R	Initialized	Initialized	Retained	Retained
LDCNT2R	Initialized	Initialized	Retained	Retained
LDRCNTR	Initialized	Initialized	Retained	Retained
LDDDSR	Initialized	Initialized	Retained	Retained
LDRCR	Initialized	Initialized	Retained	Retained
LDDBSLMR	Initialized	Initialized	Retained	Retained
LDSLHPNR	Initialized	Initialized	Retained	Retained
LDSLVLNR	Initialized	Initialized	Retained	Retained
LDSLRGBR	Initialized	Initialized	Retained	Retained
LDDWD0R to LDDWDFR	Initialized	Initialized	Retained	Retained
LDDRDR	Initialized	Initialized	Retained	Retained
LDDWAR	Initialized	Initialized	Retained	Retained

Register Symbol	Power-On Reset	Manual Reset	Module Standby	Sleep
LDDRAR	Initialized	Initialized	Retained	Retained
LDBCR	Initialized	Initialized	Retained	Retained
LDBnBSIFR (n=1～4)	Initialized	Initialized	Retained	Retained
LDBnBSSZR (n=1～4)	Initialized	Initialized	Retained	Retained
LDBnBLOCR (n=1～4)	Initialized	Initialized	Retained	Retained
LDBnBSMWR (n=1～4)	Initialized	Initialized	Retained	Retained
LDBnBSARY (n=1～4)	Initialized	Initialized	Retained	Retained
LDBnBSARC (n=1～4)	Initialized	Initialized	Retained	Retained
LDBnBSARA (n=1～4)	Initialized	Initialized	Retained	Retained
LDBnBPPCR (n=1～4)	Initialized	Initialized	Retained	Retained
LDBnBSIFR (n=1～4)	Initialized	Initialized	Retained	Retained
LDBnBSSZR (n=1～4)	Initialized	Initialized	Retained	Retained

40.3.1 LCDC Palette Data Registers 00 to FF (LDPR00 to LDPRFF)

LDPRnn specifies palette data in the palette memory. To access the palette memory, use these registers. Each 32-bit register has eight bits assigned to each of the R, G, and B colors. For details on the color palette specifications and settings, see section 40.4.2, Color Palette Specifications.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	PALDnn[23:16]							
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PALDnn[15:0]															
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	PALDnn[23:0]	Undefined	R/W	Palette Data

Note: nn = 00 to FF

40.3.2 LCD Dot Clock Pattern Register 1 (MLDDCKPAT1R)

MLDDCKPAT1R specifies the upper 28 bits of a dot clock output pattern for the LCD.

The LCDC operating clock (dot clock) can be generated by dividing the bus clock. For details, see section 40.4.7, Dot Clock Settings.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	DCKPAT1[59:48]											
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DCKPAT1[47:32]															
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
27 to 0	DCKPAT1 [59:32]	H'000 0000	R/W	Dot Clock Pattern 1 [59:32] Specifies the upper 28 bits of the output pattern of the dot clock, which is obtained from the divided source clock. Up to a 60-bit pattern can be specified in combination with these bits and the bits in MLDDCKPAT2R.

40.3.3 LCD Dot Clock Pattern Register 2 (MLDDCKPAT2R)

MLDDCKPAT2R specifies the lower 32 bits of a dot clock output pattern for the LCD.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DCKPAT1[31:16]															
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DCKPAT1[15:0]															
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DCKPAT1 [31:0]	H'0000 0000	R/W	Dot Clock Pattern 1 [31:0] Specifies the lower 32 bits of the output pattern of the dot clock, which is obtained from the divided source clock. A maximum of 60-bit pattern can be specified in combination with these bits and bits in MLDDCKPAT1R.

40.3.4 LCDC Dot Clock Register (LDDCKR)

LDDCKR selects the input clock and specifies the division ratio of the dot clock.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	ICKSEL[2:0]		
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	MOSEL	MDCDR[5:0]					
nitial :	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0
R/W :	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 19	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
18 to 16	ICKSEL [2:0]	All 0	R/W	Input Clock Select These bits select the source of the dot clock for the LCD. 000: bus clock. 001: MIPI-DSI byte clock 010: HDMI clock (LCDC1 only) 011: External terminal clock input 100 to 111: Setting prohibited
15 to 7	—	All 0	R	Reserved This bit is always read as 0. The write value should always be 0.
6	MOSEL	0	R/W	LCD Output Clock Select Selects the division ratio of the dot clock (LCD operating clock) from the 1/1 and value specified by bits in this register. 0: A division ratio specified by bits in this register 1: A division ratio of 1/1
5 to 0	MDCDR [5:0]	111100	R/W	Clock Division Ratio These bits specify the denominator when the division ratio of the source clock of the LCD operating clock is denoted as n/m.

Note: If the same frequency is used for the LCDC operation clock (the bus clock under normal operation; the clock selected by the MCKSEL bit in LRCKR) and the dot clock supply clock (the clock selected by the ICKSEL bit of LDDCKR and the ECKSEL bit in LRCKR), neither SOSEL=1 nor MOSEL=1 can be selected. Divide the dot clock supply clock.

* Selecting ICKSEL=10 selects the clock selected by the ECKSEL2 bit in LRCKR.

- Selecting ICKSEL=10 selects the clock selected by the ECKSEL bit in LRCKR.

40.3.5 Dot Clock Stop Register (LDDCKSTPR)

LDDCKSTPR stops or restarts the LCDC dot clock. When temporarily stopping the dot clock and then restarting it, set the DCKSTP bit to 1, check that the DCKSTS bit becomes 1, make necessary settings, and then restart the dot clock.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	DCKSTS
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	DCKSTP
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	DCKSTS	0	R	Dot Clock Status This bit is set to 1 while the dot clock stops. 0: The dot clock is being supplied. 1: The dot clock has stopped.
15 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	DCKSTP	0	R/W	Dot Clock Stop/Restart Control Stops or restarts the dot clock. 0: Supplies the dot clock. 1: Stops the dot clock.

40.3.6 LCD Module Type Register 1 (MLDMT1R)

MLDMT1R selects the module interface of LCD from the RGB and SYS interfaces and the transfer mode for connection to LCD modules, and controls the signal polarity when the RGB interface is used.

The interface mode, the polarity of control signals, the data bus width, and the number of access cycles for LCD can be specified by LCD module type registers 1 to 3

bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	VPOL	HPOL	DW POL	DI POL	DA POL	–	–	–	–	–	–	HS CNT	DW CNT
initial:	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R/W	R/W

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VSSM	CSM	YM	IFM	–	–	–	–	–	–	–	–	MIFTYP[3:0]			
initial:	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0
R/W:	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28	VPOL	0	R/W	Vertical Sync Signal Polarity Select In VSYNC output mode (when the VSEL bit in MLDMT2R is set to 1), this bit selects the polarity of the VSYNC signal for the main LCD when the RGB or SYS interface is used. In VSYNC input mode (when the VSEL bit in MLDMT2R is cleared to 0), this bit selects whether or not the polarity of the input VSYNC signal is toggled. Note that the polarity of the VSYNC signal is active high. In VSYNC output mode 0: Output VSYNC is active high. 1: Output VSYNC is active low. In VSYNC input mode 0: Polarity is not toggled. 1: Polarity is toggled
27	HPOL	0	R/W	Horizontal Sync Signal Polarity Select Selects the polarity of the HSYNC signal when the RGB interface of the LCD is used. When the RGB interface mode is selected by the IFM bit, this bit is valid. 0: HSYNC signal is active high. 1: HSYNC signal is active low.

Bit	Bit Name	Initial Value	R/W	Description
26	DWPOL	1	R/W	Dot Clock Polarity Select Selects the polarity of the dot clock signal when the RGB interface of the LCD is used. 0: Data latched at the falling edge of the dot clock 1: Data latched at the rising edge of the dot clock
25	DIPOL	0	R/W	Display Enable Polarity Select Selects the polarity of the display enable signal when the RGB interface of the LCD is used. When the RGB interface mode is selected by the IFM bit, this bit is valid. 0: Display enable signal is active high. 1: Display enable signal is active low.
24	DAPOL	0	R/W	Display Data Polarity Select Selects the polarity of display data when the RGB or SYS interface of the LCD is used. The polarity is only for display data and does not affect commands or instructions for connected LCDs. 0: Display data is active high. 1: Display data is active low.
23 to 18	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
17	HSCNT	0	R/W	HSYNC Signal Output Control Controls the HSYNC output signal during vertical blanking. When the RGB interface mode is selected by the IFM bit, this bit is valid. 0: Outputs HSYNC during vertical blanking. 1: Does not output HSYNC during vertical blanking.
16	DWCNT	0	R/W	Dot Clock Control Controls the dot clock signal output during horizontal or vertical blanking when the RGB interface mode is used. 0: Outputs the dot clock signal during horizontal/vertical blanking. 1: Does not output the dot clock signal during horizontal/vertical blanking.
15	VSSM	0	R/W	VSYNC slide output set 0: no slide 1: slide on The delays are set by MLDIVSNR.DLY.
14	CSM	0	R/W	Camera type SYNC output set 0: LCD panel SYNC signal is output 1: Camera SYNC is output (asserted during the data is valid)
13	YM	0	R/W	YCbCr output mode set Selects the YCbCr output mode. 0: RGB output mode 1: YCbCr output mode If this bit is set to 1, please set MIFTYP[3:0] to 4'b1110 or 4'b1111.

Bit	Bit Name	Initial Value	R/W	Description
12	IFM	0	R/W	Interface Mode Set Selects the interface mode for the connected LCD. 0: RGB interface mode 1: SYS interface mode
11 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	MIFTYP [3:0]	1010	R/W	LCD Module Set These bits select the type of the LCD according to the IFM bit. See table 38.6.

Table 40.5 LCD Module Settings

- IFM = B'0

MIFTYP[3:0]	Description
B'0000	RGB8 (24 bpp, three-cycle transfer, 8:8:8)
B'0001	Reserved
B'0010	Reserved
B'0011	Reserved
B'0100	RGB9 (18 bpp, two-cycle transfer, 9:9)
B'0101	RGB12a (24 bpp, two-cycle transfer, 12:12)
B'0110	RGB12b (12 bpp, one-cycle transfer)
B'0111	RGB16 (16 bpp, one-cycle transfer)
B'1000	Reserved
B'1001	Reserved
B'1010	RGB18 (18 bpp, one-cycle transfer)
B'1011	RGB24 (24 bpp, one-cycle transfer)
B'1100 to B'1110	Reserved
B’1111	YCbCr 4:2:2 (16bpp, two-pixel/two-cycle transfer (Y, Cb), (Y, Cr)

- IFM = B'1

MIFTYP[3:0]	Description
B'0000	SYS8a (24 bpp, three-time transfer, 8:8:8)
B'0001	SYS8b (18 bpp, three-time transfer, 8:8:2)
B'0010	SYS8c (18 bpp, three-time transfer, 2:8:8)
B'0011	SYS8d (16 bpp, two-time transfer, 8:8)
B'0100	SYS9 (18 bpp, two-time transfer, 9:9)
B'0101	SYS12 (24 bpp, two-time transfer, 12:12)
B'0110	Reserved
B'0111	SYS16a (16 bpp, one-time transfer)
B'1000	SYS16b (18 bpp, two-time transfer, 16:2)
B'1001	SYS16c (18 bpp, two-time transfer, 2:16)
B'1010	SYS18 (18 bpp, one-time transfer)
B'1011	SYS24 (24 bpp, one-time transfer)
B'1100 to B'1111	Reserved

40.3.7 LCD Module Type Register 2 (MLDMT2R)

MLDMT2R controls the write strobe signal and indicates access status when the SYS interface of LCD is used.

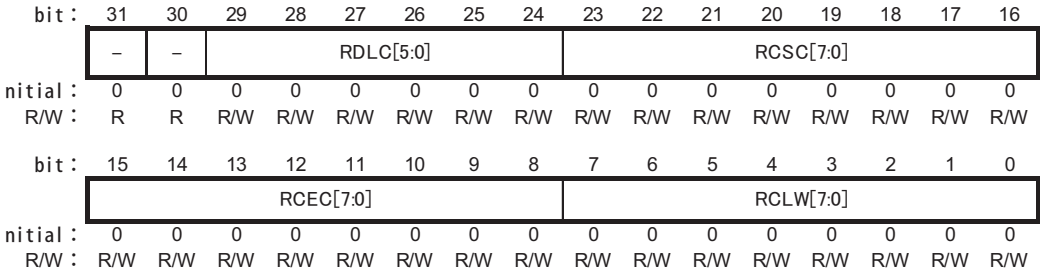
bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	CSUP[2:0]			RSV	VSEL	WCSC[7:0]							
nitial :	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WCEC[7:0]								WCLW[7:0]							
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 26	CSUP[2:0]	001	R/W	Chip Select Setup Time Set These bits specify the setup time of the chip select signal for display data transfer via the SYS interface.
25	RSV	0	R/W	VSYNC Mode Register Select Polarity Set Sets the polarity of the register select signal when display data is transferred via the SYS interface. 0: Register select signal is active low. 1: Register select signal is active high.
24	VSEL	0	R/W	VSYNC I/O Mode Select Selects the input or output mode of the VSYNC signal of the LCD for the SYS interface. This bit is writable when the DO bit in LDCNT2R is cleared to 0. 0: VSYNC output mode (LCDC outputs the VSYNC) 1: VSYNC input mode (LCDC outputs display data or commands according to the VSYNC input from an external device)
23 to 16	WCSC[7:0]	H'00	R/W	Setup Time Set These bits set the setup time of the write strobe signal for the SYS interface on a bus clock basis.
15 to 8	WCEC[7:0]	H'00	R/W	Write Cycle Time Set These bits set the time of a write cycle for the SYS interface on a bus clock basis.
7 to 0	WCLW[7:0]	H'00	R/W	Low Pulse Width Set These bits specify the low level width of the write strobe signal for the SYS interface on a bus clock basis.

40.3.8 LCD Module Type Register 3 (MLDMT3R)

MLDMT3R controls the read strobe signal via the SYS interface of LCD.



Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29 to 24	RDLC[5:0]	000000	R/W	Read Data Latch Set These bits specify the timing of latching data read via the SYS interface on a bus clock basis.
23 to 16	RCSC[7:0]	H'00	R/W	Setup Time Set These bits specify the setup time of the read strobe signal for the SYS interface on a bus clock basis.
15 to 8	RCEC[7:0]	H'00	R/W	Read Cycle Time Set These bits specify the time of a read cycle for the SYS interface on a bus clock basis.
7 to 0	RCLW[7:0]	H'00	R/W	Low Pulse Width Set These bits specify the low level width of the read strobe signal for the SYS interface on a bus clock basis.

40.3.9 LCD Data Format Register (MLDDFR)

MLDDFR sets the type of image data input to LCD.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	CF1	CF0	CC
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	YF[1:0]		–	–	–	PKF[4:0]				
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 19	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
18	CF1	0	R/W	set YCbCr format when the data format in memory is ITU-R YCbCr format 0: ITU-R BT.601 YCbCr format 1: ITU-R BT.709 YCbCr format
17	CF0	0	R/W	Set the range of YCbCr format 0: compressed-range YCbCr format [16, 235/240] 1: full-range YCbCr format [0, 255]
16	CC	0	R/W	Set the data format of display data in memory When the data format of display data in memory is YCbCr, set this bit to 1. 0: RGB format 1: YCbCr format
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9, 8	YF[1:0]	00	R/W	Input Image YCbCr Data Packed Format These bits select the packed format when the input image data format is YCbCr. When the CC bit in MLDDFR is set to 1, this bit is valid. 00: 4:2:0 YCbCr 01: 4:2:2 YCbCr 10: 4:4:4 YCbCr 11: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Description
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4 to 0	PKF[4:0]	00000	R/W	Input Image RGB Data Packed Format These bits select the packed format when the input image data format is RGB. When the CC bit in MLDDFR is cleared to 0, this bit is valid. Tables 40.6 and 40.7 list the packed formats for the YCbCr and RGB, respectively.

Table 40.6 YCbCr Packed Format

YF[1:0]	YCbCr		Bits 31 to 24	23 to 16	15 to 8	7 to 0
B'00	4:2:0	Y data	Y0	Y1	Y2	Y3
		C data	Cb0	Cr0	Cb2	Cr2
B'01	4:2:2	Y data	Y0	Y1	Y2	Y3
		C data	Cb0	Cr0	Cb2	Cr2
B'10	4:4:4	Y data	Y0	Y1	Y2	Y3
		C data	Cb0	Cr0	Cb1	Cr1
B'11	Reserved					

Table 40.7 RGB Packed Format

No	RPKF [4:0]	Bit Rate [bpp]	Phase	Bit 31 ~ 24	23 ~ 16	15 ~ 8	7 ~ 0
0	5b'00000	24	–	A0 A0 A0 A0 A0 A0 A0 A0	R0 R0 R0 R0 R0 R0 R0 R0	G0 G0 G0 G0 G0 G0 G0 G0	B0 B0 B0 B0 B0 B0 B0 B0
1	5b'00001		–	R0 R0 R0 R0 R0 R0 R0 R0	G0 G0 G0 G0 G0 G0 G0 G0	B0 B0 B0 B0 B0 B0 B0 B0	A0 A0 A0 A0 A0 A0 A0 A0
2	5b'00010		0	R0 R0 R0 R0 R0 R0 R0 R0	G0 G0 G0 G0 G0 G0 G0 G0	B0 B0 B0 B0 B0 B0 B0 B0	R1 R1 R1 R1 R1 R1 R1 R1
			1	G1 G1 G1 G1 G1 G1 G1 G1	B1 B1 B1 B1 B1 B1 B1 B1	R2 R2 R2 R2 R2 R2 R2 R2	G2 G2 G2 G2 G2 G2 G2 G2
			2	B2 B2 B2 B2 B2 B2 B2 B2	R3 R3 R3 R3 R3 R3 R3 R3	G3 G3 G3 G3 G3 G3 G3 G3	B3 B3 B3 B3 B3 B3 B3 B3
3	5b'00011	16	–	R0 R0 R0 R0 R0 G0 G0 G0	G0 G0 G0 B0 B0 B0 B0 B0	R1 R1 R1 R1 R1 G1 G1 G1	G1 G1 G1 B1 B1 B1 B1 B1
4	5b'00100	8	–	R0 R0 R0 G0 G0 G0 B0 B0	R1 R1 R1 G1 G1 G1 B1 B1	R2 R2 R2 G2 G2 G2 B2 B2	R3 R3 R3 G3 G3 G3 B3 B3
6	5b'00110	15	–	R0 R0 R0 R0 R0 G0 G0 G0	G0 G0 B0 B0 B0 B0 B0 A0	R1 R1 R1 R1 R1 G1 G1 G1	G1 G1 B1 B1 B1 B1 B1 A0
7	5b'00111	18	–	– – – – – – – –	A0 A0 A0 A0 A0 R0 R0	R0 R0 R0 R0 G0 G0 G0 G0	G0 G0 B0 B0 B0 B0 B0 B0
8	5b'01000	12	–	A0 A0 A0 A0 R0 R0 R0 R0	G0 G0 G0 G0 B0 B0 B0 B0	A1 A1 A1 A1 R1 R1 R1 R1	G1 G1 G1 G1 B1 B1 B1 B1
9	5b'01001	18	0	– – R0 R0 R0 R0 R0 R0	– – G0 G0 G0 G0 G0 G0	– – B0 B0 B0 B0 B0 B0	– – R1 R1 R1 R1 R1 R1
			1	– – G1 G1 G1 G1 G1 G1	– – B1 B1 B1 B1 B1 B1	– – R2 R2 R2 R2 R2 R2	– – G2 G2 G2 G2 G2 G2
			2	– – B2 B2 B2 B2 B2 B2	– – R3 R3 R3 R3 R3 R3	– – G3 G3 G3 G3 G3 G3	– – B3 B3 B3 B3 B3 B3
10	5b'01010	18	0	– – B0 B0 B0 B0 B0 B0	– – G0 G0 G0 G0 G0 G0	– – R0 R0 R0 R0 R0 R0	– – B1 B1 B1 B1 B1 B1
			1	– – G1 G1 G1 G1 G1 G1	– – R1 R1 R1 R1 R1 R1	– – B2 B2 B2 B2 B2 B2	– – G2 G2 G2 G2 G2 G2
			2	– – R2 R2 R2 R2 R2 R2	– – B3 B3 B3 B3 B3 B3	– – G3 G3 G3 G3 G3 G3	– – R3 R3 R3 R3 R3 R3
11	5b'01011	24	0	B0 B0 B0 B0 B0 B0 B0 B0	G0 G0 G0 G0 G0 G0 G0 G0	R0 R0 R0 R0 R0 R0 R0 R0	B1 B1 B1 B1 B1 B1 B1 B1
			1	G1 G1 G1 G1 G1 G1 G1 G1	R1 R1 R1 R1 R1 R1 R1 R1	B2 B2 B2 B2 B2 B2 B2 B2	G2 G2 G2 G2 G2 G2 G2 G2
			2	R2 R2 R2 R2 R2 R2 R2 R2	B3 B3 B3 B3 B3 B3 B3 B3	G3 G3 G3 G3 G3 G3 G3 G3	R3 R3 R3 R3 R3 R3 R3 R3
12	5b'01100	24	–	A0 A0 A0 A0 A0 A0 A0 A0	B0 B0 B0 B0 B0 B0 B0 B0	G0 G0 G0 G0 G0 G0 G0 G0	R0 R0 R0 R0 R0 R0 R0 R0
	Except		–	reserved			

40.3.10 LCD Scan Mode Register 1 (MLDSM1R)

MLDSM1R selects the display data size from full or partial and selects the mode for reading display data from continuous or one-shot. For details of the settings, see section 40.4.4, One-Shot Mode, and section 40.4.5, Partial Screen Mode.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	PRD	–	–	–	–	–	–	–	OS
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	PRD	0	R/W	Partial Size Read Set Selects the size of display data read from external memory. 0: Full screen size (panel size) of data is read. 1: Partial screen size of data is read.
7 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	OS	0	R/W	One-Shot Read Set Selects the mode for reading display data from external memory. 0: Continuous mode (display data is read according to the refresh rate of the panel) 1: One-shot mode (display data is read using the OSTRG bit in MLDSM2R as a trigger)

40.3.11 LCD Scan Mode Register 2 (MLDSM2R)

MLDSM2R sets the one-shot trigger of LCD.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	OSTRG
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	OSTRG	0	R/W	One-Shot Trigger When the one-shot mode is selected for reading display data, setting this bit to 1 starts reading of one frame of data from external memory. This bit is cleared when the display operation is started. 0: — 1: One frame of data read

40.3.12 LCD Display Data Read Start Address Register 1 (MLDSA1R)

MLDSA1R sets the start address of LCD display data in memory. When the data format of display data is YCbCr, these bits set the start address of the luminance signal.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SA[31:16]															
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SA[15:3]													–	–	–
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	SA[31:3]	H'0000 0000	R/W	Display Data Start Address These bits set the start address of the LCD display data in memory. When the data format of display data is YCbCr, these bits set the start address of the luminance signal.
2 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

40.3.13 LCD Display Data Read Start Address Register 2 (MLDSA2R)

MLDSA2R sets the start address of the color difference signal of LCD display data in memory. When the data format of display data is YCbCr, this register is valid.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SA[31:16]															
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SA[15:3]													–	–	–
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	SA[31:3]	H'0000 0000	R/W	Display Data Start Address These bits specify the start address of the color difference signal of the LCD display data in memory. When the data format of display data is YCbCr, these bits are valid.
2 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

40.3.14 LCD Display Data Storing Memory Line Size Register (MLDMLSR)

MLDMLSR specifies the amount of one line of LCD display data in memory. A vertical line number is incremented when the specified size of memory is read. When the data format of display data is YCbCr 4:4:4, twice the size set is used in memory.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LS[15:3]													–	–	–
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 3	LS[15:3]	H'0000	R/W	Line Size These bits set the amount of one line of LCD display data in memory. When the data format of display data is YCbCr 4:4:4, twice the size set is used in memory.
2 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

40.3.15 LCD Write-Back Data Format Register (MLDWBFR)

MLDWBFR specifies the data format of data written back to the LCD. The LCDC handles data with big endian in the default settings.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	AI								WP
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	LS	WS	BS	–	–	–	–	–	WBTYP[2:0]		
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	AI	0	R/W	Address Increment Select Enables or disables incrementing of the start address to

Bit	Bit Name	Initial Value	R/W	Description
				which data is written back. 0: Disables incrementing of the start address. 1: Enables incrementing of the start address.
23 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	WP	0	R/W	Write-Back Data Polarity Select Inverts the polarity of the data to be written back (to support reflective LCD modules). 0: Data is active high. 1: Data is active low.
15 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10	LS	0	R/W	Write-back Longword Swap Select Enables or disables longword swapping on data with the type specified by the WBTYP bits (see figure 38.3). 0: Disables longword swapping. 1: Enables longword swapping.
9	WS	0	R/W	Write-Back Word Swap Select Enables or disables word swapping on data with the type specified by the WBTYP bits (see figure 38.4). 0: Disables word swapping. 1: Enables word swapping.
8	BS	0	R/W	Write-Back Byte Swap Select Enables or disables byte swapping on data with the type specified by the WBTYP bits (see figure 38.5). 0: Disables byte swapping. 1: Enables byte swapping.
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2 to 0	WBTYP [2:0]	010	R/W	Write-Back Type Select These bits specify the type of display data to be written (32-bit Pack). 000: WB8a (max. RGB888) 001: WB8d (max. RGB565) 010: WB9 (max. RGB666) 011: WB16 (max. RGB565) 100: WB18 (max. RGB666) 101: WB24 (max. RGB888)

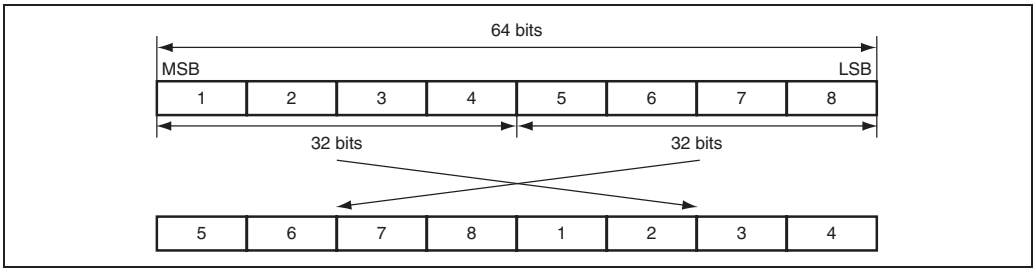


Figure 40.2 Longword Swapping

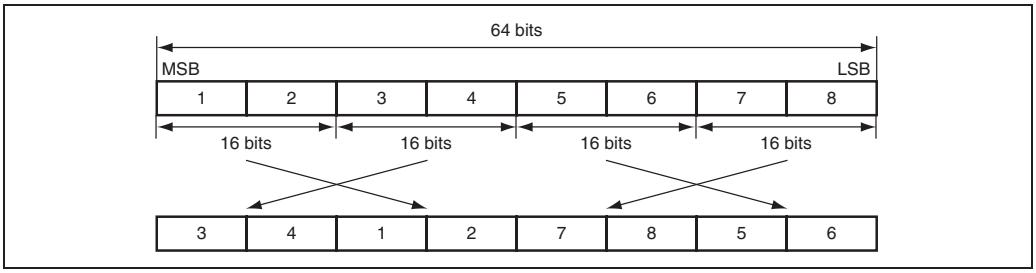


Figure 40.3 Word Swapping

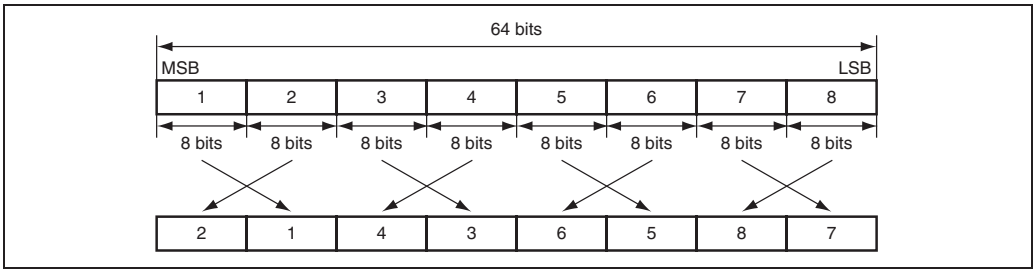


Figure 40.4 Byte Swapping

40.3.16 LCD Write-Back Control Register (MLDWBCNTR)

MLDWBCNTR enables or disables write-back operation to LCD.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	WE
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	WE	0	R/W	Write-Back Enable Enables or disables write-back operation. 0: Disables write-back operation. 1: Enables write-back operation.

40.3.17 LCD Write-Back Start Address Register (MLDWBAR)

MLDWBAR specifies the start address to which display data is written back to the LCD.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	WA[31:16]															
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WA[15:5]											–	–	–	–	–
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	WA[31:5]	H'000 0000	R/W	Write-Back Start Address Specifies the start address to which data is written back.
4 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

40.3.18 LCD Horizontal Character Number Register (MLDHCNR)

MLDHCNR specifies the horizontal size of the LCD and the scan size including the horizontal blanking. This register must be set in units of characters (eight dots).

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	HDCN[7:0]							
nitial :	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0
R/W :	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	HTCN[8:0]								
nitial :	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1
R/W :	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 16	HDCN[7:0]	H'1E	R/W	Horizontal Display Character Count These bits specify the number of horizontal display characters (one character = eight dots). For example, when an LCD module which has 240 pixels horizontally is used, set these bits to H'1E (= 240/8 = 30).
15 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8 to 0	HTCN[8:0]	H'21	R/W	Horizontal Character Count These bits specify the number of horizontal characters (one characters = eight dots). The horizontal blanking is three characters (24 dots) at a minimum.

Notes: 1. The specified size of horizontal display data has no limitation on the function side, but the limitation on the performance side is caused between refresh rate. Please refer to 40.7 directions for details.

2. Specify the HDCN and HTCN bits so that the following expression is satisfied.
   $HTCN \geq HDCN + 3$

3. When LDDBSLMR.DBM is set to 1, please set HDCN to the display size (The data for the pixel count that adjusts HDCN to 1/2 is acquired, it expands by the twice, and it is output).

40.3.19 LCD Horizontal Sync Signal Register (MLDHSYNR)

MLDHSYNR specifies the timing and size of the horizontal sync signal of the LCD.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	HSYNW[3:0]			
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	HSYNP[8:0]								
nitial :	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 20	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
19 to 16	HSYNW [3:0]	H'1	R/W	Horizontal Sync Signal Pulse Width These bits specify the pulse width of the horizontal sync signal in units of characters (one character = eight dots).
15 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8 to 0	HSYNP[8:0]	H'20	R/W	Horizontal Sync Signal Output Position These bits specify the output position of the horizontal sync signal in units of characters (one character = eight dots).

Note: Specify the HSYNW and HSYNP bits so that the following expressions are satisfied.
HTCN ≥ HSYNP + HSYNW
HSYNP ≥ HDCN + 1

40.3.20 LCD Vertical Line Number Register (MLDVLNR)

MLDVLNR specifies the vertical size excluding or including blanking of LCD.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	VDLN[10:0]										
nitial :	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0
R/W :	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	VTLN[10:0]										
nitial :	0	0	0	0	0	0	0	1	0	1	0	0	0	0	1	0
R/W :	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 27	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
26 to 16	VDLN[10:0]	H'140	R/W	Vertical Display Line Count These bits specify the number of display lines in the vertical direction in units of lines. For example, when an LCD having 320 vertical lines is used, set these bits to H'140 = 320.
15 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 0	VTLN[10:0]	H'142	R/W	Vertical Line Total Count These bits specify the total number of lines in the vertical direction in units of lines. The minimum total number of lines is 3.

Notes: 1. Specify the VTLN and VDLN bits so that the following expression is satisfied.
VTLN ≥ VDLN + 1
2. For VSYNC input mode, the interval of the VSYNC input must be shorter than one frame specified by the VTLN bits. The vertical blanking during which commands can be issued is defined from the completion of display operation to the end of the frame specified by the VTLN bits.
3. When LDDBSLMR.DBM is set to 1, please set HDCN to the display size (The data for the pixel count that adjusts HDCN to 1/2 is acquired, it expands by the twice, and it is output).

40.3.21 LCD Vertical Sync Signal Register (MLDVSYNR)

MLDVSYNR specifies the timing and width of the vertical sync signal of LCD.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	VSYNW[3:0]			
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	VSYNP[10:0]										
nitial :	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	1
R/W :	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 20	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
19 to 16	VSYNW [3:0]	H'1	R/W	Vertical Sync Signal Width These bits specify the pulse width of vertical sync signal assertion in units of lines.
15 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 0	VSYNP [10:0]	H'141	R/W	Vertical Sync Signal Output Position These bits specify the output position of the vertical sync signal in units of lines.

Note: Specify the VSYNP bits so that the following expressions is satisfied.
VTLN ≥ VSYNP
VSYNP ≥ VDLN + 1

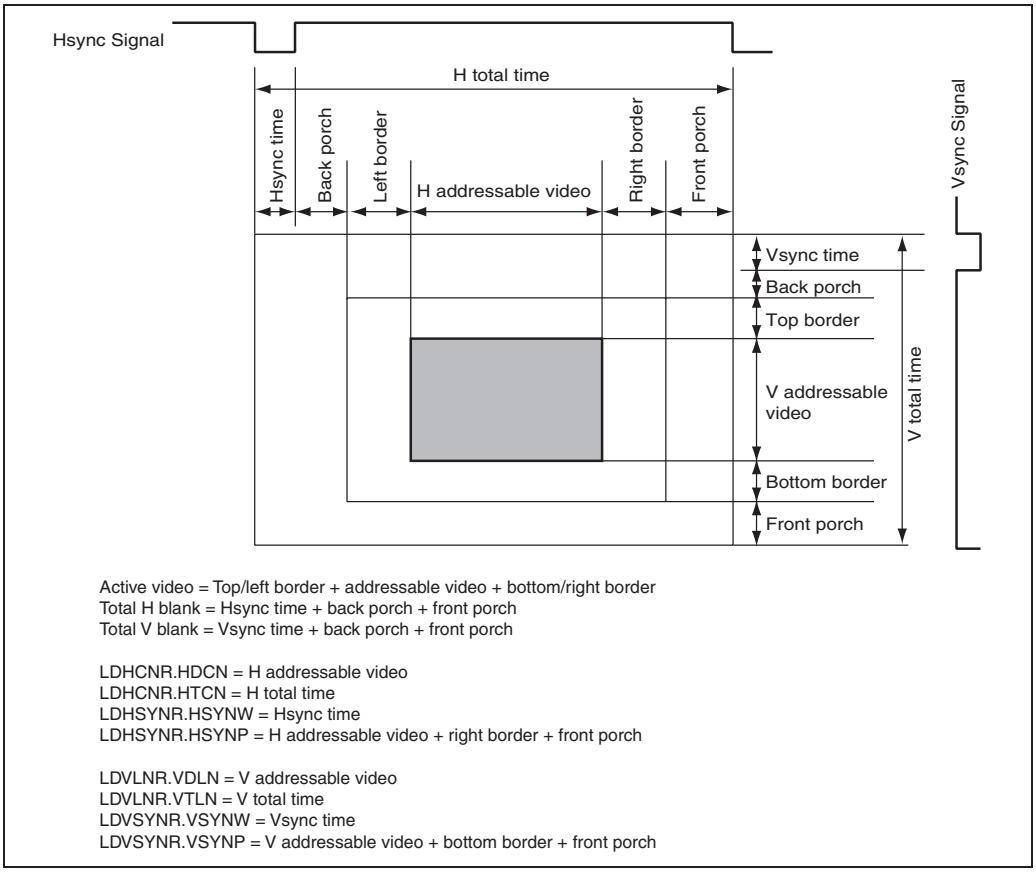


Figure 40.5 Valid Display and Blanking Periods

40.3.22 LCD Horizontal Partial Display Register (MLDHPDR)

MLDHPDR specifies the number of horizontal display characters and the number of offset characters in the LCD partial display mode. For details on settings, see section 40.4.5, Partial Screen Mode.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	HPDCN[7:0]							
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	HPDOCN[7:0]							
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 16	HPDCN [7:0]	H'00	R/W	Horizontal Partial Display Character Count These bits specify the number of horizontal display characters of the partial display in partial display mode (one character = eight dots).
15 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	HPDOCN [7:0]	H'00	R/W	Horizontal Partial Display Offset Character Count These bits specify the horizontal offset of the partial display from the display size in partial display mode in units of characters (one character = eight dots).

40.3.23 LCD Vertical Partial Display Register (MLDVPDR)

MLDVPDR specifies the number of vertical display lines and the number of offset lines in the LCD partial display mode.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	VPDLN[10:0]										
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	VPDOLN[10:0]										
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 27	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
26 to 16	VPDLN [10:0]	H'000	R/W	Vertical Partial Display Line Count These bits specify the number of vertical display lines of the partial display in partial display mode (one character = eight dots).
15 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 0	VPDOLN [10:0]	H'000	R/W	Vertical Partial Display Offset Line Count These bits specify the vertical offset of the partial display from the display size in partial display mode in units of lines.

40.3.24 LCD Power Management Register (MLDPMR)

MLDPMR controls power supply circuits for the LCD. For details, see section 40.4.6, Power Management Function. When the LCD module is not used, be sure to clear this register to H'0000 0000.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ONA[3:0]				ONB[3:0]				ONC[3:0]				OFFD[3:0]			
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OFFE[3:0]				OFFF[3:0]				–	VC	VE	DO	–	–	LPS[1:0]	
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	ONA[3:0]	0000	R/W	LCDC Switching-On Sequence Interval A These bits specify the time in units of frames until the display data (LCDD) and timing signals (LCDHSYN, LCDDCK, LCDDISP, LCDVSYN, and $\overline{\text{LCDRD}}$) start to be output after an assertion of the LCDVCPWC signal in the LCDC switching-on sequence. When the VC bit is cleared to 0, clear these bits to H'0.
27 to 24	ONB[3:0]	0000	R/W	LCDC Switching-On Sequence Interval B These bits specify the time in units of frames until the LCDVEPWC signal is asserted after the display data (LCDD) and timing signals (LCDHSYN, LCDDCK, LCDDISP, LCDVSYN, and $\overline{\text{LCDRD}}$) start to be output in the LCDC switching-on sequence. When the VE bit is cleared to 0, clear these bits to H'0.
23 to 20	ONC[3:0]	0000	R/W	LCDC Switching-On Sequence Interval C These bits specify the time in units of frames from assertion of the LCDVEPWC signal to assertion of the LCDDON signal in the LCDC switching-on sequence.
19 to 16	OFFD[3:0]	0000	R/W	LCDC Switching-Off Sequence Interval A These bits specify the time in units of frames from a negation of the LCDDON signal to a negation of the LCDVEPWC signal in the LCDC switching-off sequence. When the VE bit is cleared to 0, clear these bits to H'0.
15 to 12	OFFE[3:0]	0000	R/W	LCDC Switching-Off Sequence Interval B These bits specify the time in units of frames until the display data (LCDD) and timing signals (LCDHSYN, LCDDCK, LCDDISP, LCDVSYN, and $\overline{\text{LCDRD}}$) stop output after a negation of the LCDVEPWC signal in the LCDC switching-off sequence.
11 to 8	OFFF[3:0]	0000	R/W	LCDC Switching-Off Sequence Interval C These bits specify the time in units of frames until the LCDVCPWC signal is negated after the display data (LCDD) and timing signals (LCDHSYN, LCDDCK, LCDDISP, LCDVSYN, and $\overline{\text{LCDRD}}$) stop output in the LCDC switching sequence. When the VC bit is cleared

Bit	Bit Name	Initial Value	R/W	Description
				to 0, clear these bits to H'0.
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6	VC	0	R/W	LCDVCPWC Signal Enable Enables or disables LCDC switching-on and -off sequences using the LCDVCPWC signal. 0: LCDVCPWC fixed low 1: LCDVCPWC assertion and negation controlled by a given sequence
5	VE	0	R/W	LCDVEPWC Signal Enable Enables or disables LCDC switching-on and -off sequences using the LCDVEPWC signal. 0: LCDVEPWC fixed low 1: LCDVEPWC assertion and negation controlled by a given sequence
4	DO	0	R/W	LCDDON Signal Enable Enables or disables LCDC switching-on and -off sequences using the LCDDON signal. 0: LCDDON fixed low 1: LCDDON assertion and negation controlled by a given sequence
3, 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	LPS[1:0]	00	R	LCD Module Power Supply State These bits indicate the state of the power supply for the LCD module while LCDC switching-on and -off sequences are enabled. 00: Power is not supplied to the LCD module. 11: Power is supplied to the LCD module.

40.3.25 LCDC Palette Control Register (LDPALCR)

LDPALCR specifies the access mode to the palette memory. For details on the color palette specification and settings, see section 40.4.2, Color Palette Specifications.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	MM
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	PE
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	MM	0	R/W	LCD Palette Mode Enables the LCD to use the palette memory. 0: Disables use of the palette memory by the LCD. 1: Enables use of the palette memory (24-bit input and output palette memory) by the LCD.
15 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	PE	0	R/W	Palette Read/Write Enable Specifies the source of access to the palette memory. 0: The LCDC uses the palette memory (display mode). 1: The host (CPU) uses the palette memory (CPU access mode).

40.3.26 LCDC Interrupt Register (LDINTR)

LDINTR specifies the start timing of interrupts and indicates the interrupt status.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	BFS	WRE	CE	UILN[10:0]										
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EE	SE	UE	ME	MHE	FE	VSE	VEE	ES	SS	US	MS	MHS	FS	VSS	VES
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 30	—	All 0	R	Reserved This bit is always read as 0. The write value should always be 0.
29	BFS	0	R/W	Line Buffer Error Status This bit is set to 1 when the data in the line buffer is not supplied to the LCD display block in time (underrun). Write 0 to this bit to clear it.
28	WRE	0	R/W	Write Error Status This bit is set to 1 when data to be written back to the external memory is overwritten before the write operation. Write 0 to this bit to clear it.
27	CE	0	R/W	SYS Error Status This bit is set to 1 when a LCD display operation is triggered during writing or reading the driver. Write 0 to this bit to clear it.
26 to 16	UILN[10:0]	H'000	R/W	User-Specified Interrupt Line Number These bits specify the position to generate a user-specified interrupt. A user-specified interrupt occurs when image data for the specified number of lines has been read from the external memory. The number of lines is specified by this register.
15	EE	0	R/W	Error Interrupt Enable Enables or disables an interrupt to be generated when a BFS, WRE, or CE error occurs. 0: Disables an interrupt. 1: Enables an interrupt.
14	SE	0	R/W	Frame Start Interrupt Enable Enables or disables an interrupt to be generated when the first pixel data of a frame is output to the LCD. This setting is valid only for output frame in one-shot mode. 0: Disables an interrupt when the first pixel data is output to the LCD. 1: Enables an interrupt when the first pixel data is output to the LCD.
13	UE	0	R/W	User-Specified Interrupt Enable Enables or disables an LCDC user-specified interrupt. 0: Disables a user-specified interrupt. 1: Enables a user-specified interrupt.

Bit	Bit Name	Initial Value	R/W	Description
12	ME	0	R/W	Memory Access Interrupt Enable Enables or disables an interrupt to be generated on completion of one frame of data access to external memory. 0: An interrupt is not generated on completion of one-frame data access to external memory. 1: An interrupt is generated on completion of one-frame data access to external memory.
11	MHE	0	R/W	Data Memory Read Interrupt Enable Enables or disables an interrupt to be generated on completion of one line of data access to the external memory. 0: An interrupt is not generated on completion of one-line data access to the external memory. 1: An interrupt is generated on completion of one-line data access to the external memory.
10	FE	0	R/W	Frame End Interrupt Enable Enables or disables an interrupt to be generated when the last pixel of a frame is output to the LCD. 0: Disables an interrupt when the last pixel of a frame is output to the LCD. 1: Enables an interrupt when the last pixel of a frame is output to the LCD.
9	VSE	0	R/W	VSYNC Start Interrupt Enable Enables or disables a VSYNC start interrupt to be generated. 0: A VSYNC start interrupt is not generated. 1: A VSYNC start interrupt is generated.
8	VEE	0	R/W	VSYNC End Interrupt Enable Enables or disables a VSYNC end interrupt to be generated. 0: A VSYNC end interrupt is not generated. 1: A VSYNC end interrupt is generated.
7	ES	0	R/W	Error Interrupt Status This bit is set to 1 when an error interrupt is generated. Write 0 to this bit to clear it.
6	SS	0	R/W	Frame Start Interrupt Status Indicates that a frame start interrupt has been generated. In one-shot mode, an interrupt is generated only for an output frame. Write 0 to this bit to clear it in the frame start interrupt handler. 0: Indicates that a frame start interrupt has not occurred or the interrupt handling has been completed. 1: Indicates that a frame start interrupt has occurred or the interrupt handling has not been completed.

Bit	Bit Name	Initial Value	R/W	Description
5	US	0	R/W	User-Specified Interrupt Status Indicates that a user-specified interrupt has been generated. Write 0 to this bit to clear it in the user-specified interrupt handler. 0: Indicates that a user-specified interrupt has not occurred or the interrupt handling has been completed. 1: Indicates that a user-specified interrupt has occurred or the interrupt handling has not been completed.
4	MS	0	R/W	Memory Access Interrupt Status Indicates that a frame end interrupt has been generated for access to external memory. Write 0 to this bit to clear it in the frame end interrupt handler of the external memory access. 0: Indicates that a frame-end interrupt for external memory access has not been generated or handling of the interrupt has been completed. 1: Indicates that an external memory access has been generated occurred or handling of the interrupt has not been completed.
3	MHS	0	R/W	Data Memory Read Interrupt Status Indicates that a line-end interrupt has been generated for access to external memory. Write 0 to this bit to clear it from in the line-end interrupt handler for the external memory access. 0: Indicates that an external memory access line end interrupt has not occurred or the interrupt handling has been completed. 1: Indicates that an external memory access line end interrupt has occurred or the interrupt handling has not been completed.

Bit	Bit Name	Initial Value	R/W	Description
2	FS	0	R/W	Frame End Interrupt Status Indicates that a frame end interrupt has been generated. In one-shot mode, an interrupt is generated only for an output frame. Write 0 to this bit to clear it in the frame end interrupt handler. 0: Indicates that a frame end interrupt has not occurred or the interrupt handling has been completed. 1: Indicates that a frame end interrupt has occurred or the interrupt handling has not been completed.
1	VSS	0	R/W	VSYNC Start Interrupt Status Indicates that a VSYNC start interrupt has been generated. Write 0 to this bit to clear it in the VSYNC end interrupt handler. 0: Indicates that a VSYNC start interrupt has not occurred or the interrupt handling has been completed. 1: Indicates that a VSYNC start interrupt has occurred or the interrupt handling has not been completed.
0	VES	0	R/W	VSYNC End Interrupt Status Indicates that a VSYNC end interrupt has been generated. Write 0 to this bit to clear it in the VSYNC end interrupt handler. 0: Indicates that a VSYNC end interrupt has not occurred or the interrupt handling has been completed. 1: Indicates that a VSYNC end interrupt has occurred or the interrupt handling has not been completed.

40.3.27 LCDC Status Register (LDSR)

LDSR indicates status related to the LCDC operations.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	MRLS[10:0]										
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	MSS	–	MRS	–	–	–	–	–	–	AS	ST
nitial :	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 27	—	All 0	R	Reserved These bits are always read as 0.
26 to 16	MRLS[10:0]	H'000	R	Memory Read Line Status These bits indicate the number of lines, which have been read from external memory.
15 to 11	—	All 0	R	Reserved These bits are always read as 0.
10	MSS	1	R	Operating LCD Status Indicates which the LCDC is controlling. This bit is changed when one frame of display data is completed (when a frame end interrupt is generated). 0: LCD is in operation. 1: LCD is not in operation.
9	-	0	R	Reserved These bits are always read as 0.
8	MRS	0	R	LCD Register Set Status Indicates the register set of the LCD used by the LCDC. 0: Set A is used. 1: Set B is used.
7 to 2	—	All 0	R	Reserved These bits are always read as 0.
1	AS	0	R	SYS Interface Access Status Indicates the access status of the SYS interface. When the status indicates bus busy, do not issue the next transaction. Otherwise, operation is not guaranteed. 0: Bus idle 1: Bus busy (read or write access is being executed or is waiting)
0	ST	0	R	Indicates the LCDC operating status. 0: LCDC is idle. 1: LCDC is operating.

40.3.28 LCDC Control Register 1 (LDCNT1R)

LDCN1R specifies whether to output display data to an LCD during LCDC operation.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	DE
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	DE	1	R/W	Display Enable Specifies whether to output display data to the LCD during LCDC operation. When only write-back operation is necessary, writing 0 to this bit fixes the data output to the LCD. 0: Does not output display data (fixes output data low or high). 1: Outputs display data.

40.3.29 LCDC Control Register 2 (LDCNT2R)

LDCNT2R specifies a reset and the display operation of the LCD.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	SR	BR	–	–	–	–	–	–	ME	DO
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
9	SR	0	R/W	Software Reset Setting this bit to 1 initializes all internal circuitry of the LCDC other than registers. Bus transactions in progress at the time are guaranteed. However, when the LCDC is operating with the BEU, handshaking between them is not guaranteed. Even if handshaking is in progress, the LCDC is immediately initialized by a reset. Initialization by a software reset must be performed more than once. Thus, when the BEU and LCDC are operating together, the BEU should be initialized before a software reset is issued. Do not set both the SR bit and the BR bit to 1 at the same time. 0: LCDC is in normal operation. 1: Writing 1 initializes the LCDC.
8	BR	0	R/W	Module Reset Setting this bit to 1 initializes all internal circuitry of the LCDC other than registers. Bus transactions in progress at the time are guaranteed. However, when the LCDC is operating with the BEU, handshaking between them is not guaranteed. Even if handshaking is in progress, the LCDC is immediately initialized by a reset. Thus, when the BEU and LCDC are operating together, the BEU should be initialized before a software reset is issued. Do not set both the BR bit and the SR bit to 1 at the same time. 0: LCDC is in normal operation. 1: Writing 1 initializes the LCDC.
7 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	ME	0	R/W	LCD Enable Enables or disables whether the LCDC operates the LCD while the display is turned on. When the ME bits is set to 1, the LCD is operated by time-division multiplexing. 0: LCDC does not operate the LCD. 1: LCDC operates the LCD.
0	DO	0	R/W	Display On Starts or stops the LCDC display operation. The state of the switching-on process can be read from the LPS bit in MLDPMR. When the DO bit is set to 1, set either ME, or SS bit to 1. 0: Stops the LCDC operation (display-off mode). 1: Starts the LCDC operation (display-on mode).

The display switching-on and switching-off sequences for the LCD are shown below.

- Display switching-on sequence (when changing the DO bit from 0 to 1)
  1. Start the LCDC display operation.
  2. Turn on the LCD power according to the method specified by MLDPMR and LDCNT2R.

  When a change from B'00 to B'11 in the LPS bit is confirmed, the switching-on sequence is completed.

  Do not access the DO bit until the completion of the sequence.

- Display switching-off sequence (when changing the DO bit from 1 to 0)

Note: Do not change the ME bit from 1.

1. Turn off the LCD power according to the method specified by MLDPMR and LDCNT2R.
2. Stop the LCDC display operation.

   When a change from B'11 to B'00 in the LPS bit is confirmed, the switching-off sequence is completed.

   Do not access the DO and ME bits until the completion of the sequence.

40.3.30 LCDC Register Set Change Control Register (LDRCNTR)

LDRCNTR specifies register sets of the LCD.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	MRS	MRC
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	MRS	0	R/W	LCD Register Set Select Selects the LCD register set the LCDC uses. Register sets are changed when display of one frame of data is completed. This bit is valid when the MRC bit is cleared to 0. 0: Set A registers are used for the LCD. 1: Set B registers are used for the LCD.
0	MRC	0	R/W	LCD Register Set Change Enable In synchronization with completion of frame display on the sub-LCD, selects the register set for use by the LCDC with the sub-LCD. If this bit is cleared (0), the register set selected by the SRS bit is used. When this bit is set to 1, the sets are toggled. 0: Register set is selected by the MRS bit. 1: Register set is toggled.

40.3.31 LCDC Input Image Data Swap Register (LDDDSR)

LDDDSR enables or disables byte, word, and longword swap on input image data.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	–	LS	WS	BS
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/S	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	LS	0	R/W	Input Image Data Longword Swap Select Enables or disables input image data to be swapped in longwords. This setting is valid for LCD. 0: Disables longword swap. 1: Enables longword swap.
1	WS	0	R/W	Input Image Data Word Swap Select Enables or disables input image data to be swapped in words. This setting is valid for LCD. 0: Disables word swap. 1: Enables word swap.
0	BS	0	R/W	Input Image Data Byte Swap Select Enables or disables input image data to be swapped in bytes. This setting is valid for LCD. 0: Disables byte swap. 1: Enables byte swap.

40.3.32 LCDC Register Set Forcible Select Register (LDRCR)

LDRCR immediately selects the register set when changing register sets.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	MR
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	MR	0	R/W	LCD Register Set Select Selects the LCD register set the LCDC uses. 0: Set A registers are used. 1: Set B registers are used.

40.3.33 Tabular Mode Register (LDDBSLMR)

LDDBSLMR specifies tabular mode or slider mode.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	DBM
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	SLM
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	DBM	0	R/W	Tabular Mode Select Tabular mode doubles display images horizontally and vertically. 0: Normal mode 1: Tabular mode Tabular mode cannot be used with slider mode.
15 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	SLM	0	R/W	Slider Mode Select Slider mode slides display images horizontally and vertically. The area to be blanked by sliding is displayed in the background color. The amount to slide is specified in LDSLHPNR and LDSLVLNR. The background color is specified in LDSLRGBR. 0: Normal mode 1: Slider mode Slider mode cannot be used with tabular mode.

Note: Tabular mode and slider mode are intended to resize still images to smaller sizes.

40.3.34 Horizontal Slide Number Register (LDSLHPNR)

LDSLHPNR specifies the horizontal number of characters to slide in slider mode.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	HC2[7:0]							
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–							HC1[7:0]							
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 16	HC2	0	R/W	The area behind the number of characters set in HC2 is displayed in the background color after sliding images horizontally in slider mode.
15 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	HC1	0	R/W	The area behind the number of characters set in HC1 is displayed in the background color after sliding images horizontally in slider mode. Normal images are displayed adjacent horizontally to the area.

Note: When specifying the numbers of characters (MLDHCNR.HDCN and SLDHCNR.HDCN), the values must include background-colored areas.

40.3.35 Vertical Slide Number Register (LDSLVLNR)

LDSLHPNR specifies the vertical number of lines to slide in slider mode.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	VL2[10:0]										
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–				VL1[10:0]										
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 27	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
26 to 16	VL2	0	R/W	The area behind the number of lines set in VL2 is displayed in the background color after sliding images vertically in slider mode.
15 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 0	VL1	0	R/W	The area behind the number of characters set in VL1 is displayed in the background color after sliding images vertically in slider mode. Normal images are displayed adjacent vertically to the area.

Note: When specifying the numbers of lines (MLDVLNR.VDLN and SLDVLNR.VDLN), the values must include background-colored areas.

40.3.36 Slide Data Register (LDSLRGBR)

LDSLRGBR specifies the background color in slider mode.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	RGB[23:16]							
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RGB[15:0]															
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	RGB	0	R/W	Specifies the background color in RGB888 format.

Note: 1. The overall background color is displayed when setting it to HC1==HC2 and VL1==VL2.
2. Please set the value in order of CrYCb when the output data form is YCbCr form.

40.3.37 LCD Horizontal Sync Signal Adjust Register (MLDHAJR)

MLDHAJR is a register for adjusting in 1-pixel unit the total horizontal width, the horizontal sync signal width, and the horizontal sync signal output point, which are usually specified in 8-pixel unit.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	HDCN_ADPIX[2:0]			–	–	–	–	–	HTCNAJ[2:0]		
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R	R	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	HSYNWAJ[2:0]			–	–	–	–	–	HSYNPAJ[2:0]		
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 27	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
26 to 24	HDCN_ADPIX[2:0]	H'0	R/W	Specifies the display horizontal adjusting size. The display horizontal size is large only in this setting.
23 to 19	—	All 0	R/W	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
18 to 16	HTCNAJ [2:0]	H'0	R/W	Specifies the total horizontal adjusting size. The total horizontal size is large only in this setting.
15 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 8	HSYNWAJ [2:0]	H'0	R/W	Specifies the adjusting width horizontal sync signal. The total horizontal sync signal width is large only in this setting.
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2 to 0	HSYNPAJ [2:0]	H'0	R/W	Specifies the adjusting size of the sync signal output point. The horizontal sync signal output point is delayed.

40.3.38 LCD Vertical Sync Signal Adjustment Register (MLDIVSNR

MLDIVSYNR is a register for setting the VSYNC output delay. This register is enabled when the VSSM bit in MLDMT1R register is 1.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	VSYNC_SLD[13:0]													
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13 to 0	VSYNC_SLD [13:0]	H'0000	R/W	Specifies the VSYNC output lagged

40.3.39 LCDC Color Palette Expander Control Register (LDPALECR)

LDPALECR is a register for controlling the color palette expander. This register is FIFO structure on current side/program side. Writing on a current side is reflected at once, please write it only for the period when LCD has stopped. When the UPD bit on the program side is 1, a set value on the program side is reflected in a current side according to the register reflection timing (display completion of one screen). For details of the settings, see section 40.4.2 Color Palette.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	UPD	UPF	AE	ASWP	–	–	–	–	–	–	–	–	–	–	–	–
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	AB	–	–	–	CB	–	–	–	–	–	–	–	MB
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R/W	R	R	R	R/W	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	UPD	0	R/W	Update permission bit Program side When one is set, a set value on the program side of the LDPALECR register and the LPPALADR register is reflected in a current side according to the register reflection timing. This bit is cleared by the set value reflection on a current side. It is cleared by writing 0. Current side It is always read as 0.
30	UPF	0	R/W	Update completion flag Program side When the register value is reflected in current side, 1 is set. It is cleared by writing 1. Even if 0 is written, the value is not changed. Current side It is always read as 0.
29	AE	0	R/W	Palette data automatic acquisition function operate Palette data is acquired from the address by setting LDPALADR, and stored in the bank by AB. Current side The automatic acquisition function starts at once when 1 is written (LDPALADR on a current side is used). When the acquisition of data is completed, it is cleared to 0. Program side The value of LDPALADR on the program side is copied onto a current side when UPD=1 and AE=1 are set, and the register reflection timing comes, AE bit on the current side is set, and the automatic acquisition function starts. The AE bit on the program side is cleared by the reflection on a current side. Note: Please judge timing that actual data acquisition is completed by AE bit on a current side though AE bit on the program side is cleared by the reflection on a current side.

Bit	Bit Name	Initial Value	R/W	Description
28	ASWP	0	R/W	Palette data swap 1: When the palette data is acquired automatically, data is swapped in each long word. 0: disables long word swapping
27～13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	AB	0	R/W	Palette bank that sets palette data automatically 0: The value is set to bank 0 by the automatic acquisition function. 1: The value is set to bank 1 by the automatic acquisition function.
11～9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	CB	0	R/W	Palette bank that write to CPU and read from CPU 0: bank 0 1: bank 1
7～1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	MB	0	R/W	Palette bank to which LCD refers 0: bank 0 1: bank 1

40.3.40 LCDC Color Palette Address Register (LDPALADR)

LDPALADR specifies the address of color palette data. This register is FIFO structure on current side/program side. Writing on a current side is reflected at once, please write it only for the period when LCD has stopped. When the LDPALECR.UPD bit on the program side is 1, a set value on the program side is reflected in a current side according to the register reflection timing (display completion of one screen). For details of the settings, see section 40.4.2 Color Palette.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PALADR[31:16]															
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PALADR[15:0]															
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PALADR	H'0	R/W	Palette data start address

40.3.41 LCDC Driver Write Data Registers 0 to F (LDDWD0R to LDDWDFR)

LDDWDnR specifies the write data and the register select signal (LCDRS) polarity for the LCD driver.

For details on write data stored in the DWD bits such as bits used as a valid instruction, refer to the specifications for the LCD driver used.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	WDACT	–	–	–	RSW	–	–	–	–	–	–	DWD[17:16]	
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R/W	R	R	R	R/W	R	R	R	R	R	R	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DWD[15:0]															
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28	WDACT	0	R/W	Data Write Select Selects whether write data set in the DWD bits is output when the SYS interface is used. 0: Write data in DWD is not output to the LCD driver. 1: Write data in DWD is output to the LCD driver.
27 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	RSW	0	R/W	Write Register Select Polarity Selects the polarity of the register select signal (LCDRS) when data is written to via the SYS interface by the CPU. 0: Register select signal is active low. 1: Register select signal is active high.
23 to 18	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
17 to 0	DWD[17:0]	H'0	R/W	Write data These bits store data to be written to the LCD driver via the SYS interface.

40.3.42 LCDC Driver Read Data Register (LDDRDR)

LDDRDR specifies the read data and the register select signal (LCDRS) polarity for the LCD driver.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	RSR	–	–	–	–	–	–	DRD[17:16]	
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRD[15:0]															
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	RSR	0	R/W	Read Register Select Polarity Selects the polarity of the register select signal (LCDRS) when data is read by the CPU via the SYS interface. 0: Register select signal is at the low level. 1: Register select signal is at the high level.
23 to 18	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
17 to 0	DRD[17:0]	H'0 0000	R	Read Data These bits store data to be read from the LCD via the SYS interface.

40.3.43 LCDC Driver Write Access Register (LDDWAR)

The LCDC issues a write transaction to an LCD when the WA bit is set to 1. Data stored in the DWD bits in LDDWDnR in which the WDACT bit is set to 1 is used. The data is written to in the following order: LDDWD0R, LDDWD1R, LDDWD2R, when the WDACT bit is read as 0, the write access is stopped. If all the WDACT bits are read as 1, the write access is stopped when a write transaction of LDDWDFR is issued. Before a write transaction is issued, set the WDACT bit in LDDWD0R to 1. After the write transaction is issued, the WA bit is automatically cleared to 0.

Notes: 1. To issue a write transaction to an LCD via the SYS interface during display operation, the vertical blanking time must be equal to two lines or more.

2. To issue a write transaction, specify the vertical blanking time so that access to the LCD can be completed. If a write access is not completed within the vertical blanking time, the CA bit in LDINTR is set to 1.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	WA
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	WA	0	R/W	Write Transaction Issue Issues a write transaction. 0: — 1: A write transaction issued

40.3.44 LCDC Driver Read Access Register (LDDRAR)

The LCDC issues a read transaction to an LCD when the RA bit is set to 1. When this register is accessed, read data is stored in the DRD bits in LDDRDR.

Notes: 1. To issue a read transaction to an LCD via the SYS interface during display operation, the vertical blanking time must be equal to two lines or more.
2. To issue a read transaction, specify the vertical blanking time so that access to the LCD driver can be completed. If a write access is not completed within the vertical blanking time, the CA bit in LDINTR is set to 1.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	RA
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	RA	0	R/W	Read Transaction Issue Issues a read transaction. 0: — 1: A read transaction issued

40.3.45 LCDC RGB Coefficient Register for Color Management Matrix R (LDCMRKRGBR)

LDCMRKRGBR specifies the coefficient RGBCMY of color management matrix R.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	CMRKR[6:0]						
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	CMPKG[6:0]							–	CMRKB[6:0]						
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 23	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
22 to 16	CMRKR[6:0]	H'0	R/W	Coefficient R for color management RGBCMY matrix R These bits specify the R signal correction value for displaying red. The MSB indicates the sign (0: positive ; 1: negative). Specifiable value: -63 to +63
15	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
14 to 8	CMRKG[6:0]	H'0	R/W	Coefficient G for color management RGBCMY matrix R These bits specify the G signal correction value for displaying red. The MSB indicates the sign (0: positive ; 1: negative). Specifiable value: -63 to +63
7	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
6 to 0	CMRKB[6:0]	H'0	R/W	Coefficient B for color management RGBCMY matrix R These bits specify the B signal correction value for displaying red. The MSB indicates the sign (0: positive ; 1: negative). Specifiable value: -63 to +63

40.3.46 LCDC CMY Coefficient Register for Color Management Matrix R (LDCMRKCMYR)

LDCMRKCMYR specifies the coefficient RGBCMY of color management matrix R.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	CMRKC[6:0]							–	CMRKM[6:0]						
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	CMPKY[6:0]							–	CMRKW[6:0]						
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
30 to 24	CMRKC[6:0]	H'0	R/W	Coefficient C for color management RGBCMY matrix R These bits specify the C signal correction value for displaying red. The MSB indicates the sign (0: positive ; 1: negative). Specifiable value: -63 to +63
23	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
22 to 16	CMRKM[6:0]	H'0	R/W	Coefficient M for color management RGBCMY matrix R These bits specify the M signal correction value for displaying red. The MSB indicates the sign (0: positive ; 1: negative). Specifiable value: -63 to +63
15	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
14 to 8	CMRKY[6:0]	H'0	R/W	Coefficient Y for color management RGBCMY matrix R These bits specify the Y signal correction value for displaying red. The MSB indicates the sign (0: positive ; 1: negative). Specifiable value: -63 to +63
7	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
6 to 0	CMRKW[6:0]	H'0	R/W	Coefficient W for color management RGBCMY matrix R These bits specify the W signal correction value for displaying red. The MSB indicates the sign (0: positive ; 1: negative). Specifiable value: -63 to +63

40.3.47 LCDC Coefficient of Hue Circle Register 1 for Color Management Matrix R (LDCMRK1R)

LDCMRK1R specifies the coefficient of hue circle for color management matrix R.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	CMRK0[6:0]						
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	CMRK1[6:0]							–	CMRK2[6:0]						
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 23	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
22 to 16	CMRK0[6:0]	H'0	R/W	Coefficient 0 for color management hue circle matrix R These bits specify the R signal correction value for displaying the color included in hue circle region 0. The MSB indicates the sign (0: positive ; 1: negative). Hue region 0 is a region between two of the six hues(red, yellow, green, cyan, blue, and magenta) and is selected bye the CMSEL bit setting in LDCMSELR. Specifiable value: -63 to +63
15	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
14 to 8	CMRK1[6:0]	H'0	R/W	Coefficient 1 for color management hue circle matrix R These bits specify the R signal correction value for displaying the color included in hue circle region 1. The MSB indicates the sign (0: positive ; 1: negative). Hue region 1 is a region between two of the six hues(red, yellow, green, cyan, blue, and magenta) and is selected bye the CMSEL bit setting in LDCMSELR. Specifiable value: -63 to +63
7	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
6 to 0	CMRK2[6:0]	H'0	R/W	Coefficient 2 for color management hue circle matrix R These bits specify the R signal correction value for displaying the color included in hue circle region 2. The MSB indicates the sign (0: positive ; 1: negative). Hue region 2 is a region between two of the six hues(red, yellow, green, cyan, blue, and magenta) and is selected bye the CMSEL bit setting in LDCMSELR. Specifiable value: -63 to +63

40.3.48 LCDC Coefficient of Hue Circle Register 2 for Color Management Matrix R (LDCMRK2R)

LDCMRK2R specifies the coefficient of hue circle for color management matrix R.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	CMRK3[6:0]						
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	CMRK4[6:0]							–	CMRK5[6:0]						
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 23	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
22 to 16	CMRK3[6:0]	H'0	R/W	Coefficient 3 for color management hue circle matrix R These bits specify the R signal correction value for displaying the color included in hue circle region 3. The MSB indicates the sign (0: positive ; 1: negative). Hue region 3 is a region between two of the six hues(red, yellow, green, cyan, blue, and magenta) and is selected bye the CMSEL bit setting in LDCMSELR. Specifiable value: -63 to +63
15	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
14 to 8	CMRK4[6:0]	H'0	R/W	Coefficient 4 for color management hue circle matrix R These bits specify the R signal correction value for displaying the color included in hue circle region 4. The MSB indicates the sign (0: positive ; 1: negative). Hue region 4 is a region between two of the six hues(red, yellow, green, cyan, blue, and magenta) and is selected bye the CMSEL bit setting in LDCMSELR. Specifiable value: -63 to +63
7	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
6 to 0	CMRK5[6:0]	H'0	R/W	Coefficient 5 for color management hue circle matrix R These bits specify the R signal correction value for displaying the color included in hue circle region 5. The MSB indicates the sign (0: positive ; 1: negative). Hue region 5 is a region between two of the six hues(red, yellow, green, cyan, blue, and magenta) and is selected bye the CMSEL bit setting in LDCMSELR. Specifiable value: -63 to +63

40.3.49 LCDC RGB Coefficient Register for Color Management Matrix G (LDCMGKRGBR)

LDCMGKRGBR specifies the coefficient RGBCMY of color management matrix G.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	CMGKR[6:0]						
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	CMGKG[6:0]							–	CMGKB[6:0]						
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 23	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
22 to 16	CMGKR[6:0]	H'0	R/W	Coefficient R for color management RGBCMY matrix G These bits specify the R signal correction value for displaying red. The MSB indicates the sign (0: positive ; 1: negative). Specifiable value: -63 to +63
15	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
14 to 8	CMGKG[6:0]	H'0	R/W	Coefficient G for color management RGBCMY matrix G These bits specify the G signal correction value for displaying red. The MSB indicates the sign (0: positive ; 1: negative). Specifiable value: -63 to +63
7	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
6 to 0	CMGKB[6:0]	H'0	R/W	Coefficient B for color management RGBCMY matrix G These bits specify the B signal correction value for displaying red. The MSB indicates the sign (0: positive ; 1: negative). Specifiable value: -63 to +63

40.3.50 LCDC CMY Coefficient Register for Color Management Matrix G (LDCMGKCMYR)

LDCMGKCMYR specifies the coefficient RGBCMY of color management matrix G.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	CMGKC[6:0]							–	CMGKM[6:0]						
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	CMGKY[6:0]							–	CMGKW[6:0]						
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
30 to 24	CMGKC[6:0]	H'0	R/W	Coefficient C for color management RGBCMY matrix G These bits specify the C signal correction value for displaying red. The MSB indicates the sign (0: positive ; 1: negative). Specifiable value: -63 to +63
23	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
22 to 16	CMGKM[6:0]	H'0	R/W	Coefficient M for color management RGBCMY matrix G These bits specify the M signal correction value for displaying red. The MSB indicates the sign (0: positive ; 1: negative). Specifiable value: -63 to +63
15	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
14 to 8	CMGKY[6:0]	H'0	R/W	Coefficient Y for color management RGBCMY matrix G These bits specify the Y signal correction value for displaying red. The MSB indicates the sign (0: positive ; 1: negative). Specifiable value: -63 to +63
7	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
6 to 0	CMGKW[6:0]	H'0	R/W	Coefficient W for color management RGBCMY matrix G These bits specify the W signal correction value for displaying red. The MSB indicates the sign (0: positive ; 1: negative). Specifiable value: -63 to +63

40.3.51 LCDC Coefficient of Hue Circle Register 1 for Color Management Matrix G (LDCMGK1R)

LDCMGK1R specifies the coefficient for color management hue circle matrix G.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	CMGK0[6:0]						
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	CMGK1[6:0]							–	CMGK2[6:0]						
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 23	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
22 to 16	CMGK0[6:0]	H'0	R/W	Coefficient 0 for color management hue circle matrix G These bits specify the G signal correction value for displaying the color included in hue circle region 0. The MSB indicates the sign (0: positive ; 1: negative). Hue region 0 is a region between two of the six hues(red, yellow, green, cyan, blue, and magenta) and is selected bye the CMSEL bit setting in LDCMSELR. Specifiable value: -63 to +63
15	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
14 to 8	CMGK1[6:0]	H'0	R/W	Coefficient 1 for color management hue circle matrix G These bits specify the G signal correction value for displaying the color included in hue circle region 1. The MSB indicates the sign (0: positive ; 1: negative). Hue region 1 is a region between two of the six hues(red, yellow, green, cyan, blue, and magenta) and is selected bye the CMSEL bit setting in LDCMSELR. Specifiable value: -63 to +63
7	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
6 to 0	CMGK2[6:0]	H'0	R/W	Coefficient 2 for color management hue circle matrix G These bits specify the G signal correction value for displaying the color included in hue circle region 2. The MSB indicates the sign (0: positive ; 1: negative). Hue region 2 is a region between two of the six hues(red, yellow, green, cyan, blue, and magenta) and is selected bye the CMSEL bit setting in LDCMSELR. Specifiable value: -63 to +63

40.3.52 LCDC Coefficient of Hue Circle Register 2 for Color Management Matrix G (LDCMGK2R)

LDCMGK2R specifies the coefficient for color management hue circle matrix G.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	CMGK3[6:0]						
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	CMGK4[6:0]							–	CMGK5[6:0]						
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 23	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
22 to 16	CMGK3[6:0]	H'0	R/W	Coefficient 3 for color management hue circle matrix G These bits specify the G signal correction value for displaying the color included in hue circle region 3. The MSB indicates the sign (0: positive ; 1: negative). Hue region 3 is a region between two of the six hues(red, yellow, green, cyan, blue, and magenta) and is selected bye the CMSEL bit setting in LDCMSELR. Specifiable value: -63 to +63
15	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
14 to 8	CMGK4[6:0]	H'0	R/W	Coefficient 4 for color management hue circle matrix G These bits specify the G signal correction value for displaying the color included in hue circle region 4. The MSB indicates the sign (0: positive ; 1: negative). Hue region 4 is a region between two of the six hues(red, yellow, green, cyan, blue, and magenta) and is selected bye the CMSEL bit setting in LDCMSELR. Specifiable value: -63 to +63
7	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
6 to 0	CMGK5[6:0]	H'0	R/W	Coefficient 5 for color management hue circle matrix G These bits specify the G signal correction value for displaying the color included in hue circle region 5. The MSB indicates the sign (0: positive ; 1: negative). Hue region 5 is a region between two of the six hues(red, yellow, green, cyan, blue, and magenta) and is selected bye the CMSEL bit setting in LDCMSELR. Specifiable value: -63 to +63

40.3.53 LCDC RGB Coefficient Register for Color Management Matrix B (LDCMBKRGBR)

LDCMBKRGBR specifies the coefficient RGBCMY of color management matrix B.

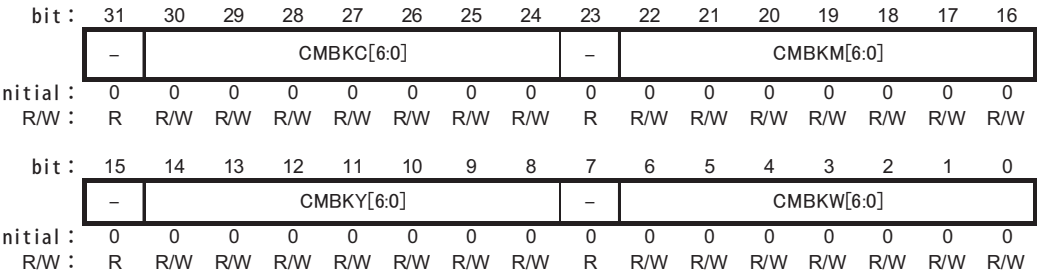
bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	CMBKR[6:0]						
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	CMBKG[6:0]							–	CMBKB[6:0]						
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 23	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
22 to 16	CMBKR[6:0]	H'0	R/W	Coefficient R for color management RGBCMY matrix G These bits specify the R signal correction value for displaying red. The MSB indicates the sign (0: positive ; 1: negative). Specifiable value: -63 to +63
15	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
14 to 8	CMBKG[6:0]	H'0	R/W	Coefficient G for color management RGBCMY matrix B These bits specify the G signal correction value for displaying red. The MSB indicates the sign (0: positive ; 1: negative). Specifiable value: -63 to +63
7	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
6 to 0	CMBKB[6:0]	H'0	R/W	Coefficient B for color management RGBCMY matrix B These bits specify the B signal correction value for displaying red. The MSB indicates the sign (0: positive ; 1: negative). Specifiable value: -63 to +63

40.3.54 LCDC CMY Coefficient Register for Color Management Matrix B (LDCMBKCMYR)

LDCMRKCMYR specifies the coefficient RGBCMY of color management matrix B.



Bit	Bit Name	Initial Value	R/W	Description
31	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
30 to 24	CMBKC[6:0]	H'0	R/W	Coefficient C for color management RGBCMY matrix B These bits specify the C signal correction value for displaying red. The MSB indicates the sign (0: positive ; 1: negative). Specifiable value: -63 to +63
23	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
22 to 16	CMBKM[6:0]	H'0	R/W	Coefficient M for color management RGBCMY matrix B These bits specify the M signal correction value for displaying red. The MSB indicates the sign (0: positive ; 1: negative). Specifiable value: -63 to +63
15	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
14 to 8	CMBKY[6:0]	H'0	R/W	Coefficient Y for color management RGBCMY matrix B These bits specify the Y signal correction value for displaying red. The MSB indicates the sign (0: positive ; 1: negative). Specifiable value: -63 to +63
7	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
6 to 0	CMBKW[6:0]	H'0	R/W	Coefficient W for color management RGBCMY matrix B These bits specify the W signal correction value for displaying red. The MSB indicates the sign (0: positive ; 1: negative). Specifiable value: -63 to +63

40.3.55 LCDC Coefficient of Hue Circle Register 1 for Color Management Matrix B (LDCMBK1R)

LDCMBK1R specifies the coefficient of hue circle for color management matrix B.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	CMBK0[6:0]						
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	CMBK1[6:0]							–	CMBK2[6:0]						
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 23	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
22 to 16	CMBK0[6:0]	H'0	R/W	Coefficient 0 for color management hue circle matrix B These bits specify the B signal correction value for displaying the color included in hue circle region 0. The MSB indicates the sign (0: positive ; 1: negative). Hue region 0 is a region between two of the six hues(red, yellow, green, cyan, blue, and magenta) and is selected bye the CMSEL bit setting in LDCMSELR. Specifiable value: -63 to +63
15	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
14 to 8	CMBK1[6:0]	H'0	R/W	Coefficient 1 for color management hue circle matrix B These bits specify the B signal correction value for displaying the color included in hue circle region 1. The MSB indicates the sign (0: positive ; 1: negative). Hue region 1 is a region between two of the six hues(red, yellow, green, cyan, blue, and magenta) and is selected bye the CMSEL bit setting in LDCMSELR. Specifiable value: -63 to +63
7	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
6 to 0	CMBK2[6:0]	H'0	R/W	Coefficient 2 for color management hue circle matrix B These bits specify the B signal correction value for displaying the color included in hue circle region 2. The MSB indicates the sign (0: positive ; 1: negative). Hue region 2 is a region between two of the six hues(red, yellow, green, cyan, blue, and magenta) and is selected bye the CMSEL bit setting in LDCMSELR. Specifiable value: -63 to +63

40.3.56 LCDC Coefficient of Hue Circle Register 2 for Color Management Matrix B (LDCMBK2R)

LDCMBK2R specifies the coefficient for color management hue circle matrix B.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	CMBK3[6:0]						
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	CMBK4[6:0]							–	CMBK5[6:0]						
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 23	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
22 to 16	CMBK3[6:0]	H'0	R/W	Coefficient 3 for color management hue circle matrix B These bits specify the B signal correction value for displaying the color included in hue circle region 3. The MSB indicates the sign (0: positive ; 1: negative). Hue region 3 is a region between two of the six hues(red, yellow, green, cyan, blue, and magenta) and is selected bye the CMSEL bit setting in LDCMSELR. Specifiable value: -63 to +63
15	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
14 to 8	CMBK4[6:0]	H'0	R/W	Coefficient 4 for color management hue circle matrix B These bits specify the B signal correction value for displaying the color included in hue circle region 4. The MSB indicates the sign (0: positive ; 1: negative). Hue region 4 is a region between two of the six hues(red, yellow, green, cyan, blue, and magenta) and is selected bye the CMSEL bit setting in LDCMSELR. Specifiable value: -63 to +63
7	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
6 to 0	CMBK5[6:0]	H'0	R/W	Coefficient 5 for color management hue circle matrix B These bits specify the B signal correction value for displaying the color included in hue circle region 5. The MSB indicates the sign (0: positive ; 1: negative). Hue region 5 is a region between two of the six hues(red, yellow, green, cyan, blue, and magenta) and is selected bye the CMSEL bit setting in LDCMSELR. Specifiable value: -63 to +63

40.3.57 LCDC Hue Circle Peak Correction Coefficient Register 1 for Color Management (LDCMHKPR)

LDCMHKPR specifies the hue peak correction coefficients.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	CMHKP0[3:0]				CMHKP1[3:0]				CMHKP2[3:0]			
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	CMHKP3[3:0]				CMHKP4[3:0]				CMHKP5[3:0]			
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
27 to 24	CMHKP0[3:0]	H'0	R/W	Hue peak correction coefficient 0 for color management These bits in combination with the CMHKQ0 bits in LDCMHKQR specify the color that produces best correction results in hue region 0. hue region 0 is a region between two of the six hues (red, yellow, green, cyan, blue, and magenta) and is selected by the CMSEL bit setting in LDCMSELR.
23 to 20	CMHKP1[3:0]	0	R/W	Hue peak correction coefficient 1 for color management These bits in combination with the CMHKQ1 bits in LDCMHKQR specify the color that produces best correction results in hue region 1. Hue region 1 is a region between two of the six hues (red, yellow, green, cyan, blue, and magenta) and is selected by the CMSEL bit setting in LDCMSELR.
19 to 16	CMHKP2[3:0]	H'0	R/W	Hue peak correction coefficient 2 for color management These bits in combination with the CMHKQ2 bits in LDCMHKQR specify the color that produces best correction results in hue region 2. Hue region 2 is a region between two of the six hues (red, yellow, green, cyan, blue, and magenta) and is selected by the CMSEL bit setting in LDCMSELR.
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 8	CMHKP3[3:0]	H'0	R/W	Hue peak correction coefficient 3 for color management These bits in combination with the CMHKQ3 bits in LDCMHKQR specify the color that produces best correction results in hue region 3. Hue region 3 is a region between two of the six hues (red, yellow, green, cyan, blue, and magenta) and is selected by the CMSEL bit setting in LDCMSELR.

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	CMHKP4[3:0]	H'0	R/W	Hue peak correction coefficient 4 for color management These bits in combination with the CMHKQ4 bits in LDCMHKQR specify the color that produces best correction results in hue region 4. Hue region 4 is a region between two of the six hues (red, yellow, green, cyan, blue, and magenta) and is selected by the CMSEL bit setting in LDCMSELR.
3 to 0	CMHKP5[3:0]	H'0	R/W	Hue peak correction coefficient 5 for color management These bits in combination with the CMHKQ5 bits in LDCMHKQR specify the color that produces best correction results in hue region 5. Hue region 5 is a region between two of the six hues (red, yellow, green, cyan, blue, and magenta) and is selected by the CMSEL bit setting in LDCMSELR.

40.3.58 LCDC Hue Circle Peak Correction Coefficient Register 2 for Color Management (LDCMHKQR)

LDCMHKQR specifies the hue peak correction coefficients.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	CMHKQ0[3:0]				CMHKQ1[3:0]				CMHKQ2[3:0]			
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	CMHKQ3[3:0]				CMHKQ4[3:0]				CMHKQ5[3:0]			
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
27 to 24	CMHKQ0[3:0]	H'0	R/W	Hue peak correction coefficient 6 for color management These bits in combination with the CMHKQ0 bits in LDCMHKQR specify the color that produces best correction results in hue region 0. hue region 0 is a region between two of the six hues (red, yellow, green, cyan, blue, and magenta) and is selected by the CMSEL bit setting in LDCMSELR.
23 to 20	CMHKQ1[3:0]	0	R/W	Hue peak correction coefficient 7 for color management These bits in combination with the CMHKQ1 bits in LDCMHKQR specify the color that produces best correction results in hue region 1. Hue region 1 is a region between two of the six hues (red, yellow, green, cyan, blue, and magenta) and is selected by the CMSEL bit setting in LDCMSELR.
19 to 6	CMHKQ2[3:0]	H'0	R/W	Hue peak correction coefficient 8 for color management These bits in combination with the CMHKQ2 bits in LDCMHKQR specify the color that produces best correction results in hue region 2. Hue region 2 is a region between two of the six hues (red, yellow, green, cyan, blue, and magenta) and is selected by the CMSEL bit setting in LDCMSELR.
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 8	CMHKQ3[3:0]	H'0	R/W	Hue peak correction coefficient 9 for color management These bits in combination with the CMHKQ3 bits in LDCMHKQR specify the color that produces best correction results in hue region 3. Hue region 3 is a region between two of the six hues (red, yellow, green, cyan, blue, and magenta) and is selected by the CMSEL bit setting in LDCMSELR.
7 to 4	CMHKP4[3:0]	H'0	R/W	Hue peak correction coefficient 10 for color management These bits in combination with the CMHKQ4 bits in LDCMHKQR specify the color that produces best correction results in hue region 4. Hue region 4 is a region between two of the six hues (red, yellow, green, cyan, blue, and magenta) and is selected by the CMSEL bit setting in LDCMSELR.
3 to 0	CMHKP5[3:0]	H'0	R/W	Hue peak correction coefficient 11 for color management These bits in combination with the CMHKQ5 bits in LDCMHKQR specify the color that produces best correction results in hue region 5. Hue region 5 is a region between two of the six hues (red, yellow, green, cyan, blue, and magenta) and is selected by the CMSEL bit setting in LDCMSELR.

40.3.59 LCDC Multiplication Coefficient Select Register for Color Management (LDCMSELR)

LDCMSELR selects multiplication coefficients.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	CMSEL0[2:0]			–	CMSEL1[2:0]			–	CMSEL2[2:0]		
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	CMSEL3[2:0]			–	CMSEL4[2:0]			–	CMSEL5[2:0]		
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 27	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
26 to 24	CMSEL0 [2:0]	H'0	R/W	Coefficient select 0 for color management These bits select the color for hue region 0 among the six hues (red, yellow, green, cyan, blue, and magenta). CMxK0, CMHKP0, and CMHKQ0 are enabled in hue region 0.
23	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
22 to 20	CMSEL1 [2:0]	H'0	R/W	Coefficient select 1 for color management These bits select the color for hue region 1 among the six hues (red, yellow, green, cyan, blue, and magenta). CMxK1, CMHKP1, and CMHKQ1 are enabled in hue region 1.
19	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
18 to 16	CMSEL2 [2:0]	H'0	R/W	Coefficient select 2 for color management These bits select the color for hue region 2 among the six hues (red, yellow, green, cyan, blue, and magenta). CMxK2, CMHKP2, and CMHKQ2 are enabled in hue region 2.
15 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 8	CMSEL3 [2:0]	H'0	R/W	Coefficient select 3 for color management These bits select the color for hue region 3 among the six hues (red, yellow, green, cyan, blue, and magenta). CMxK3, CMHKP3, and CMHKQ3 are enabled in hue region 3.

Bit	Bit Name	Initial Value	R/W	Description
7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6 to 4	CMSEL4 [2:0]	H'0	R/W	Coefficient select 4 for color management These bits select the color for hue region 4 among the six hues (red, yellow, green, cyan, blue, and magenta). CMxK4, CMHKP4, and CMHKQ4 are enabled in hue region 4.
3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2 to 0	CMSEL5 [2:0]	H'0	R/W	Coefficient select 5 for color management These bits select the color for hue region 5 among the six hues (red, yellow, green, cyan, blue, and magenta). CMxK5, CMHKP5, and CMHKQ5 are enabled in hue region 5.

40.3.60 LCDC Color Saturation Improvement Register for Color Management (LDCMTVR)

LDCMTVR specifies color saturation improvement processing and pixel property.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	CMINC1[5:0]						–	–	CMINC2[5:0]					
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMTH1[3:0]				CMTH2[3:0]				–	–	–	–	–	–	CMYSEL[1:0]	
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29 to 24	CMINC1[5:0]	H'0	R/W	Dark part inclination for color saturation improvement in color management These bits specify the dark part inclination for color saturation improvement in color management. Upper 3 bits specify the integral part and lower 3 bits specify the decimal part.
23 to 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
21 to 16	CMINC2[5:0]	H'0	R/W	Light part inclination for color saturation improvement in color management These bits specify the light part inclination for color saturation improvement in color management. Upper 3 bits specify the integral part and lower 3 bits specify the decimal part.
15 to 12	CMTH1[3:0]	H'0	R/W	Dark section threshold for color saturation improvement in color management These bits specify the dark section threshold parameter for color saturation improvement in color management.
11 to 8	CMTH2[3:0]	H'0	R/W	Light section threshold for color saturation improvement in color management These bits specify the light section threshold parameter for color saturation improvement in color management.
7 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1 to 0	CMYSEL[1:0]	H'0	R/W	Pixel property select for color saturation improvement in color management These bits select the pixel property for color saturation improvement in color management 00: largest value among R, G, and B 01: largest value - smallest value among R, G, and B 10: largest value - smallest value/2 among R, G and B 11: largest value - smallest value/2 among R, G and B

40.3.61 LCDC Color Saturation Improvement Select Register for Color Management (LDCMTVSELR)

LDCMTVSELR enables or disables color saturation improvement.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	CMT VSEL
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	CMTVSEL	0	R/W	Color saturation improvement select Enable or disables color saturation improvement processing 0: disables color saturation improvement 1: enables color saturation improvement

40.3.62 LCDC Dithering Coefficient Register for Color Management (LDCMDTHR)

LDCMDTHR specifies the dithering mode and dithering coefficients.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	DTHA0[1:0]		–	–	DTHA1[1:0]		–	–	DTHA2[1:0]		–	–	DTHA3[1:0]	
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	DTHMD[1:0]	
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29 to 28	DTHA0[1:0]	H'0	R/W	Dithering coefficient 0 These bits specify a dithering coefficient
27 to 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25 to 24	DTHA1[1:0]	H'0	R/W	Dithering coefficient 1 These bits specify a dithering coefficient
23 to 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
21 to 20	DTHA2[1:0]	H'0	R/W	Dithering coefficient 2 These bits specify a dithering coefficient
19 to 18	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
17 to 16	DTHA3 [1:0]	H'0	R/W	Dithering coefficient 3 These bits specify a dithering coefficient

Bit	Bit Name	Initial Value	R/W	Description
15 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1 to 0	DTHMD [1:0]	H'0	R/W	Dithering mode These bits specify dithering mode 00: disables the dithering mode 01: disables the dithering mode 10: enables the dithering mode (addition by pixel) 11: enables the dithering mode (addition by frame + pixel)

40.3.63 LCDC Color Management Control Register (LDCMCNTR)

LDCMCNTR enables or disables color management.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	UPD	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	CMT HRU
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	UPD	0	R/W	Register set (CM) related to the color management does the FIFO structure on a current side and the program side. When the UPD bit on the program side is 1, a set value on the program side is reflected in a current side according to the register reflection timing. Program side When 1 is set in this bit, the reflection on a current side from the program side is permitted. It is cleared automatically by the reflection on a current side. When 0 is set, permission is withdrawn. Current side The value of the UPD bit on the program side at the register reflection timing is reflected and displayed. There is no influence in operation.
30 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	CMTHRU	0	R/W	Color management through mode Enables or disables color management 0: disables color management (through output) 1: enables color management

40.4 Operation

40.4.1 LCDC Display Features

- Supported LCD Module
  TFT panel. The RGB interface and 80-Series CPU bus interface (SYS interface) are supported as the module interface.
- Display Colors
  16,777,215 colors max. (24-bit colors)
- Display Color Control
  Each of RGB, it is corresponding to 8-bit data input and 8-bit output the built-in palette memory (two banks).
  The 256-entry palette memory supports 24-bit input and 24-bit output.
- Data Polarity Inversion
  The polarity of the RGB interface signals can be inverted. Display data can also be inverted.

40.4.2 Color Palette Specifications

The LCDC has a color palette function that it is possible to define 8-bit input/output data each of RGB. The palette memory is built into two banks, and the definition of two sets can be retained.

The bank to which LCD refers is set by the LDPALECR.MB bit.

The color palette can be set with CPU and the external memory.

The method of doing with CPU

The color palette must be specified while the LCDC is not operated.

1. set LDPALCR.PE to 1 : the color palette set mode is entered.
2. set LDPALECR.CB to 0, and set bank 0
3. access LDPRnn (nn = H'00~H'FF), and set the data to PALDnn
4. set LDPALECR.CB to 1, and set bank 1
5. access LDPRnn (nn = H'00~H'FF), and set the data to PALDnn
6. set LDPALCR.PE to 0 : the normal display mode is returned.

Figure 40.6 shows a data format of the color palette.

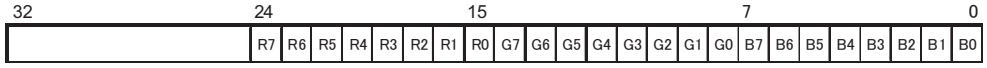


Figure 40.6 Data Format of Color Palette

For PALDnn bits in LDPRnn, bits 23 to 16 correspond to R data, bits 15 to 8 correspond to G data, and bits 7 to 0 correspond to B data. Bits 31 to 24 are reserved.

The setting data from the external memory (the automatic acquisition function)

Please arrange the data which has 256 entries continuously according to Figure 40.6 color palette data format on the external memory. Please make data on the memory as an array of data every 4-bytes, set LDPALECR.ASWP to 1 for the little endian.

Set start address register LDPALADR, and set the bank register LDPALECR.AB, the automatic acquisition function starts at once when 1 is written to LDPALECR.AE. When the acquisition of data is completed, LDPALECR.AE is cleared to 0. Set another bank or another set value is acquired from the same bank, please do it after confirming the AE bit is cleared.

The method of used two side register

LDPALECR and LDPALADR have a two-structure on current side/program side. Please set the value for the period when LCD has stopped on current side. Set the value to the program side when LCD operates, and set 1 to LDPALECR.UPD(program side). The value is reflected in a current side according to the register reflection timing (one screen display is completed).

LDPALECR.AE on program side is cleared when the reflection on current side is done. Actually the acquisition of the palette data is completed when the following display is completed and the AE on current side is cleared according to this timing.

40.4.3 Display Timing Control

The display timing control is specified by the horizontal character number registers (MLDHCNR and SLDHCNR), horizontal sync signal registers (MLDHSYNR and SLDHSYNR), vertical line number registers (MLDVLNR and SLDVLNR), and vertical sync signal registers (MLDVSYNR and SLDVSYNR).

The LCDC dot clock register (LDDCKR) specifies the division ratio. The frame rate of an LCD module is determined by the following factors: the display size and blanking period for a screen, the clock frequency used, and the division ratio.

The LCDC can generate an interrupt when the last pixel data of a frame is output after one frame of data has been read from memory. An interrupt can also be generated at intervals of user-specified lines. The LCDC interrupt register (LDINTR) specifies these settings.

40.4.4 One-Shot Mode

The LCDC supports the one-shot mode in which display data is read depending on the frame rate of the display image.

Examples and notes for use are shown in below.

- Usage example 1
  1. Clear the OS bit in MLDSM1R to 0: continuous mode (initial value) is selected.
  2. Set to the OS bit to 1: a transition to the one-shot mode is made.
  3. Set the OSTRG bit in MLDSM2R to 1 when the image should be displayed: one frame of display data is read.
  4. Repeat step 3.
  5. Clear the OS bit to 0: the continuous mode is returned.

- Usage example 2: When continuously reading display data in one-shot mode
  1. Clear the OS bit in MLDSM1R to 0: continuous mode (initial value) is selected.
  2. Set to the OS bit to 1: a transition to the one-shot mode is made.
  3. Read the frame end interrupt status bit (FS) in LDINTR.
  4. When the FS bit is read as 1, set the OSTRG bit in MLDSM2R to 1: one frame of display data is read.
  5. Clear the FS bit to 0: the frame end interrupt status is cleared.
  6. Repeat steps 3 to 5.
  7. Clear the OS bit to 0: continuous mode is returned.

Note: When an offset (other than a value of H'F) is specified in the ONA, ONB, or ONC bits in MLDPMR, the trigger must be output first. The image data corresponding to the frame is not output.

40.4.5 Partial Screen Mode

The LCDC supports the partial screen mode in which display data only for an area to be updated is read.

Examples and notes for use are shown below.

1. Specify the size of the partial screen through MLDHPDR and MLDVPDR.
2. Clear the PRD bit in MLDSM1R to 0 and set the OS bit to 1: full screen size in one-shot mode.
3. Set the DO bit in LDCNT2R to 1: the LCDC is started.
4. Display data for the full screen size is read in one-shot mode.
5. To use the partial screen mode, set both the PRD and OS bits to 1 while display data is not being read: partial screen in one-shot mode.
6. Set the OSTRG bit in MLDSM2R to 1: display data for the partial screen size is read.
7. Repeat step 6.
8. Clear the PRD bit to 0 and set the OS bit to 1: the full screen size in one-shot mode.

Notes: 1. The screen size obtained from the partial screen size + offset specified in MLDHPDR and MLDVPDR must not exceed the full screen size.
2. Screen size change (a transition between full screen size and partial screen size modes or change of the partial screen sizes) cannot be used in the continuous mode. Read screen sizes can be changed only while the LCDC is stopped (the LPS bits in MLDPMR are cleared to B'00) or while display data is not being read in the one-shot mode.

40.4.6 Power Management Function

The power management function for the LCD is shown below.

Most LCD modules require particular sequences to turn the power on and off. In the LCDC, the LCD power management register (MLDPMMR), LCDC control register 1 (LDCNT1R), and LCDC control register 2 (LDCNT2R) can be specified to control the LCD power supply control pins (LCDVCPWC, LCDVEPWC, and LCDDON) and execute various power control sequences using these pins. Figure 40.7 shows an example of a timing chart for switching-on and switching-off sequences.

The power management function can be used only when the LCDC is in stand-alone operation. The setting of the power management function for the LCD currently not used must be off (MLDPMR = 0 or SLDPMR = 0).

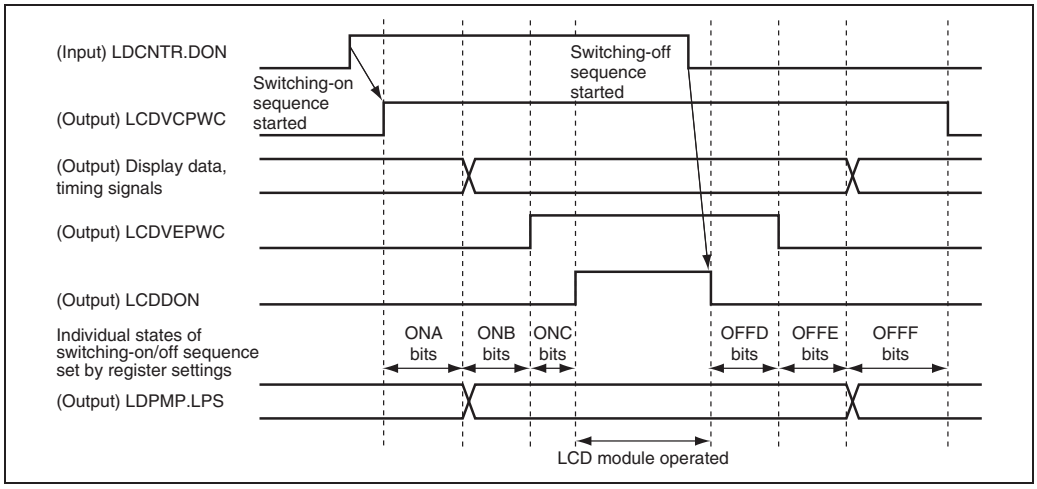


Figure 40.7 Switching-On and -Off Sequences and the LCD Module Operating State

40.4.7 Dot Clock Settings

Setting the dot clock is described. Figure 40.8 shows an example of a dot clock pattern to make the refresh rate 55 MHz. In this example, registers are set to a 33-MHz source clock, 304 dots in the horizontal direction (the HTCN bits in MLDHCNR), and 330 lines in the total vertical direction (the VTLN bit in MLDVLNR). When two or three times transfer mode is used, specify the registers so that the dot clock is two or three times the refresh rate.

The registers to set the dot clock (LDDCKR, MLDDCKPAT1R, and MLDDCKPAT2R) must be accessed while the LCDC stops the operation. Otherwise, the operation is not guaranteed.

33 MHz ÷ (304 × 330 × 55 MHz) = 5.98 ≈ 6 → Specify the division ratio to 10/60.

The MDCDR bits in LDDCKR = H'3C

The DCKPAT1 bits in MLDDCKPAT1R = H'1C71C71

The DCKPAT1 bits in MLDDCKPAT2R = H'C71C71C7

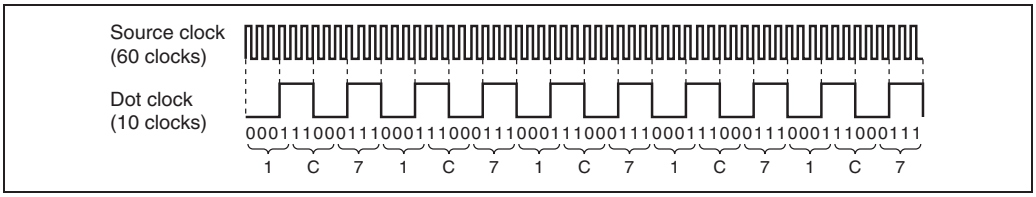


Figure 40.8 Example of Dot Clock Pattern

Note: For the source clock of the dot clock, the bus clock, the peripheral clock, or LRCKR setting clock can be selected. When selecting a clock other than the bus clock, select it so that its frequency is lower than that of the bus clock. (Setting the clock ratio to 1:1 is prohibited.)

40.4.8 Color Management

The LCDC includes a color management unit that supports the functions listed below and enables non-linear color conversions well-suited to the characteristics of the LCD module.

- Enhanced color reproducibility
- Capability for adjusting a hue of interest without affecting other hue.
- Improved color saturation in high-chroma spots

(1) Register setting

The registers of color management have a register set on current side and program side. It is reflected at once when the value on current side is updated, don’t change the value on current side when LCD operates. Please set 1 to LDCMCNTR.UPD after setting the value to program side. The setting on program side is reflected in current side according to the next register reflection timing.

LDCMCNTR.UPD on program side is cleared by 0 automatically when the value is reflected in current side. It clears to 0 by writing 0. After UPD is set to 1, change set value on program side before it reflects, clear it to 0.

UPD on program side is copied and the UPD on current side is expressed as register reflection timing.

(2) Color adjustment functional block

The color adjustment functional block, which enables the adjusting of a hue of interest without affecting any other hues, can flexibly reproduce a wide variety of color conversion characteristics. In addition, computations using data on regions between six hues permit the execution of color transform processing without the risk of a narrowed color reproducibility range.

Matrix computations are performed using the following equation:

$$\begin{bmatrix} Ro \\ Go \\ Bo \end{bmatrix} = \begin{bmatrix} Ri \\ Gi \\ Bi \end{bmatrix} + \begin{bmatrix} cmrkr & cmrkg & cmrkb & cmrkc & cmrkm & cmrky & cmrk\ 0 & \cdots & cmrk\ 5 & cmrkw \\ cmgkr & cmgkg & cmgkb & cmgkc & cmgkm & cmgky & cmgk\ 0 & \cdots & cmgk\ 5 & cmgkw \\ cmbkr & cmbkg & cmbkb & cmbkc & cmbkm & cmbky & cmbk\ 0 & \cdots & cmbk\ 5 & cmbkw \end{bmatrix} \begin{bmatrix} \Delta r \\ \Delta g \\ \Delta b \\ \Delta c \\ \Delta m \\ \Delta y \\ \Delta ih\ 0 \\ \Delta ih\ 1 \\ \Delta ih\ 2 \\ \Delta ih\ 3 \\ \Delta ih\ 4 \\ \Delta ih\ 5 \\ wh \end{bmatrix}$$

Ri, Gi, Bi: input data

Ro, Go, Bo: output data

△r, △g, △b, △c, △m, △y: hue region data valid for red, green, blue, cyan, magenta and yellow respectively

△ih0, △ih1, △ih2, △ih3, △ih4, △ih5: hue region data valid for any of 6 hue regions: red-yellow, yellow-green, green-cyan, cyan-blue, blue-magenta and magenta-red

wh: achromatic color component

(a) Selection of Hue coefficients

Depending on the values assigned to CMSEL0 to CMSEL5 (LDCMSELR), hue regions 0 to 5 are configured as shown in figure 40.9.

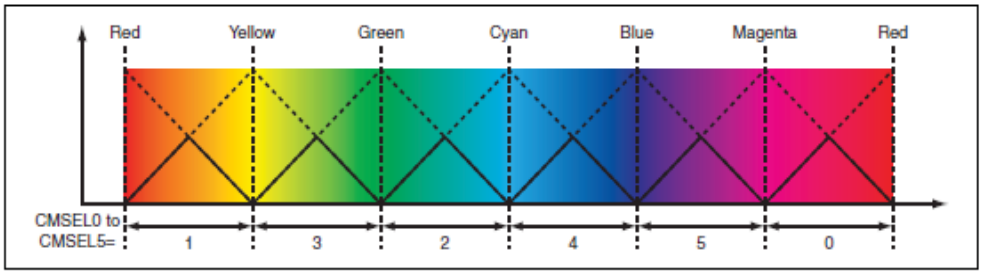


Figure 40.9 Relationship between Values Assigned to CMSEL0 to CMSEL5 (LDCMSELR) and Six Hue Regions that are selected

Select matrix coefficients (for using between hues LDCMxK1R, CDCMxK2R(x=R, G, B)) and hue peak correction coefficients (LDCMHKPR, LDCMHKQR) to be used in matrix computations according to the values of CMSEL0 to CMSEL5 (LDCMSELR), as shown in tables 40.10 and 40.11.

Table 40.10 selecting a hue coefficient and hue peak correction coefficient (1)

	CMSEL0～2（LDCMSELR）							
	1	3	2	4	5	0	6	7
CMxK0～2（LDCMxK1R LDCMxK2R）	coefficient of R-Y(RY)	coefficient of G-Y (GY)	coefficient of G-C(GC)	coefficient of B-C(BC)	coefficient of B-M(BM)	coefficient of R～M(RM)	0	0
CMHKP0～2（LDCMHKPR）	shift the peak value of R-Y toward Y (RYY1)	shift the peak value of G-Y toward Y (GYY1)	shift the peak value of G-C toward C (GCC1)	shift the peak value of B-C toward C (BCC1)	shift the peak value of B-M toward M (BMM1)	shift the peak value of R-M toward M (RMM1)	don't care	don't care
CMHKQ0～2（LDCMHKQR）	shift the peak value of R-Y toward R (RYR1)	shift the peak value of G-Y toward G (GYG1)	shift the peak value of G-C toward G (GCG1)	shift the peak value of B-C toward B (BCB1)	shift the peak value of B-M toward B (BMB1)	shift the peak value of R-M toward R (RMR1)	don't care	don't care

Note: x = R, G, B

Table 40.11 selection hue coefficient and hue peak correction coefficient (2)

	CMSEL3～5（LDCMSELR）							
	1	3	2	4	5	0	6	7
CMxK3～5（LDCMxK1R、LDCMxK2R）	coefficient of R-Y(RY)	coefficient of G-Y (GY)	coefficient of G-C(GC)	coefficient of B-C(BC)	coefficient of B-M(BM)	coefficient of R～M(RM)	0	0
CMHKP3～5（LDCMHKPR）	shift the peak value of R-Y toward Y (RYY2)	shift the peak value of G-Y toward Y (GYY2)	shift the peak value of G-C toward C (GCC2)	shift the peak value of B-C toward C (BCC2)	shift the peak value of B-M toward M (BMM2)	shift the peak value of R-M toward M (RMM2)	don't care	don't care
CMHKQ3～5（LDCMHKQR）	shift the peak value of R-Y toward R (RYR2)	shift the peak value of G-Y toward G (GYG2)	shift the peak value of G-C toward G (GCG2)	shift the peak value of B-C toward B (BCB2)	shift the peak value of B-M toward B (BMB2)	shift the peak value of R-M toward R (RMR2)	don't care	don't care

Notes: 1. x= R, G, B

2. The corresponding values of CMSEL0 to CMSEL2 should be distinct from those of CMSEL3 to CMSEL5.

3. The maximum number of coefficients that can be assigned to hue region is two (one each from CMSEL0 to CMSEL2 and CMSEL3 to CMSEL5).

(b) Hue region data

The six hue region data items, △r, △g, △b, △c, △m, and △y are valid only for red, green, blue, cyan, magenta, and yellow hue regions, respectively.

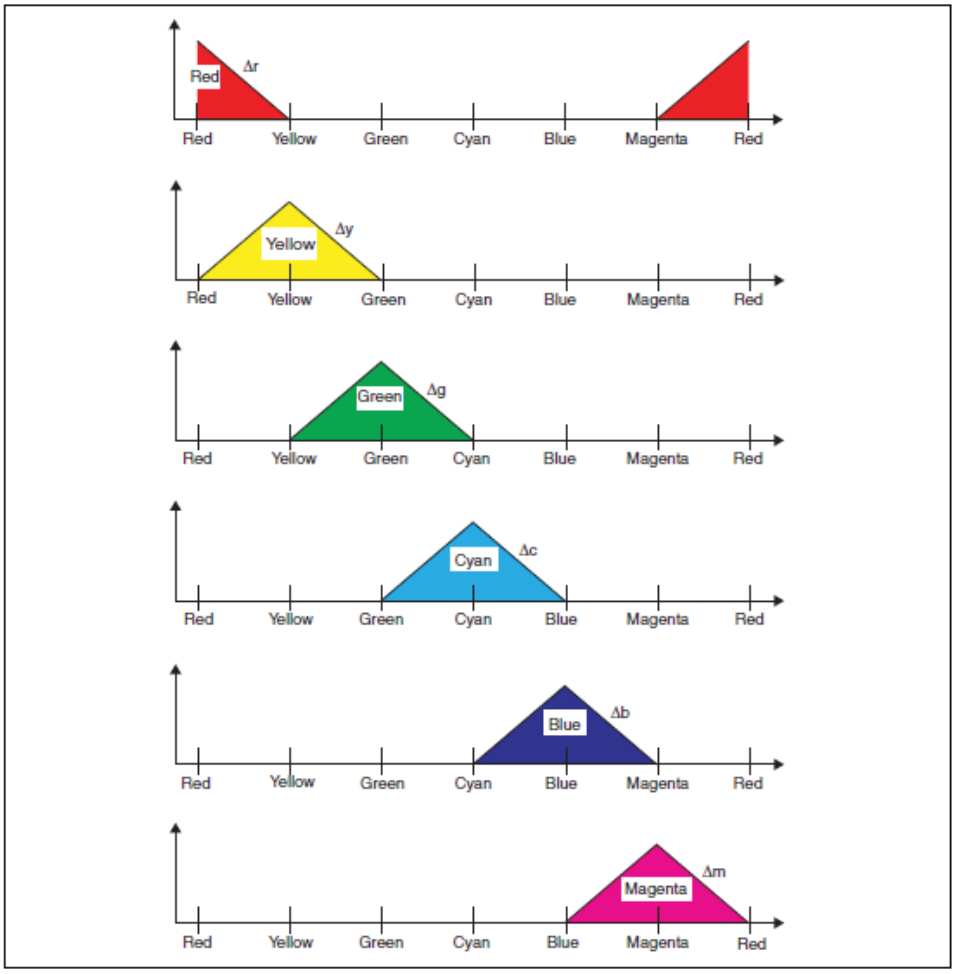


Figure 40.10 The relationship between the six hues and △r, △g, △b, △c, △m, and △y

(c) Hue region data

The six hue region data items △ry, △gy, △gc, △bc, △bm, and △rm are valid only in the six regions that are between two adjacent hues each.

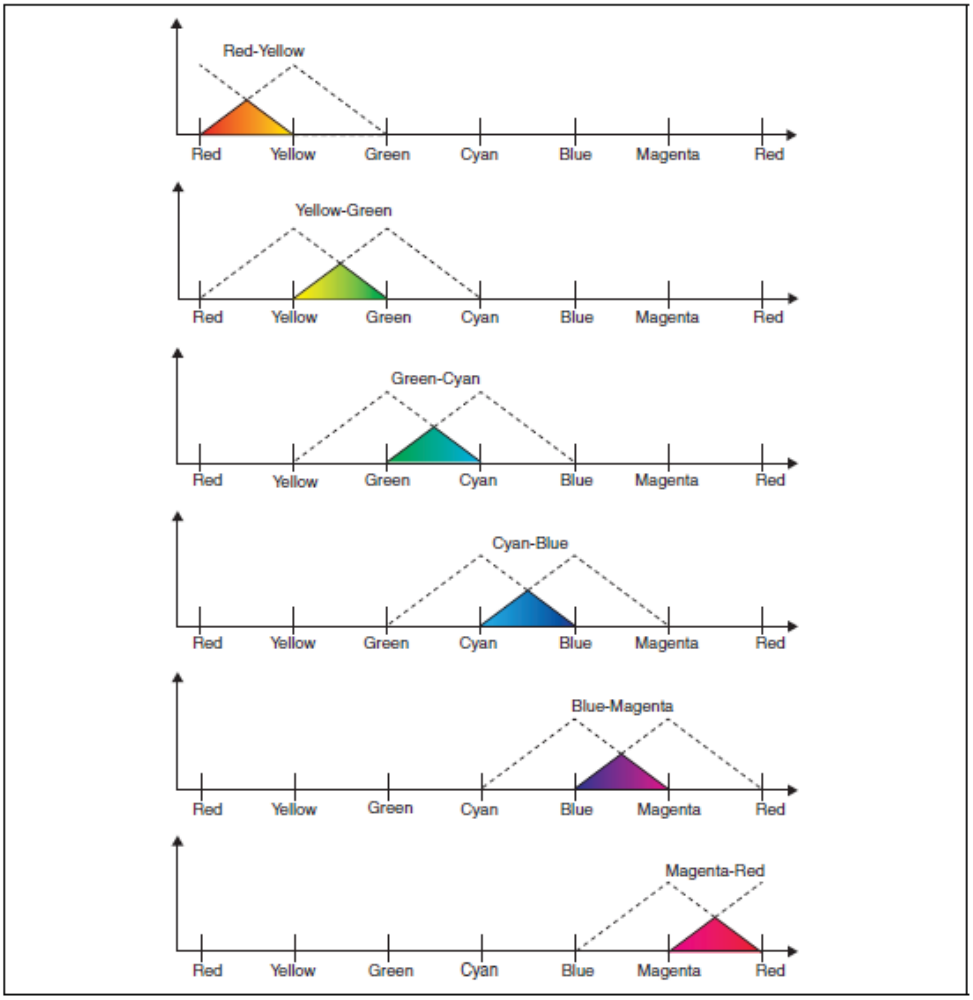


Figure 40.11 The relationship between six hues and △ry,△gy,△gc,△bc,△bm, and △rm

(3) Function of color saturation improvement

The problem of color saturation in high-chroma spots can be improved upon by the extraction of feature information from each pixel and by the control of the amount of correction applied. The color conversion processing with the color saturation improvement function can be expressed by the following formula:

$$\begin{bmatrix} Ro \\ Go \\ Bo \end{bmatrix} = \begin{bmatrix} Ri \\ Gi \\ Bi \end{bmatrix} + f(CA) \begin{bmatrix} \Delta r \\ \Delta g \\ \Delta b \end{bmatrix}$$

CA: feature information (saturation, brightness)

F(CA): correction amount control coefficient

△r, △g,△b: standard correction amount

This processing is designed to control the amount of correction applied by multiplying the correction amount control coefficient determined by feature information CA by a standard correction amount. Figure40.12 shows an example of the relationship between the correction amount control coefficient f(CA) and the feature information CA.

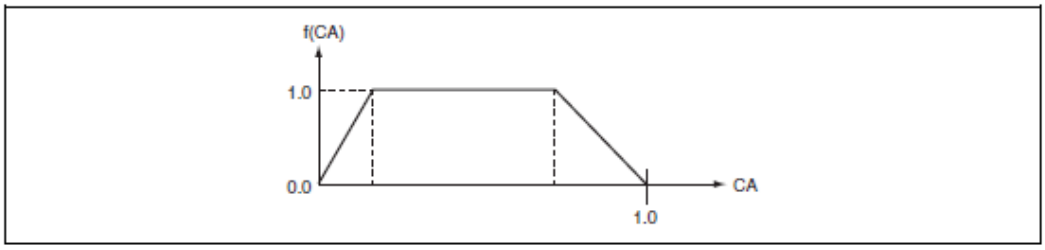


Figure 40.12 example of the relationship between the correction amount control coefficient and the feature information

As a method for calculating a correction amount control coefficient, this circuit uses a polygonal line approximation method with four parameters: a dark part threshold value (LDCMTVR.CMTH1), a dark part slop (LDCMTVR.CMINC1), a bright part threshold value (LDCMTVR.CMTH2), and bright part slope (LDCTVR.CMINC2). If CA is less than the dark part threshold value, then f(CA)=0, and if CA becomes greater than the dark part threshold value, then f(CA) is a slope that is set in terms of a dark-part slope, and it increases up to f(CA)=1 as CA increases. If CA is greater than the bright part threshold value, then f(CA)=0, and when CA declines below the bright part threshold value, f(CA) increases up to f(CA)=1 with a slope that is set in terms of the bright part slope, as CA decreases.

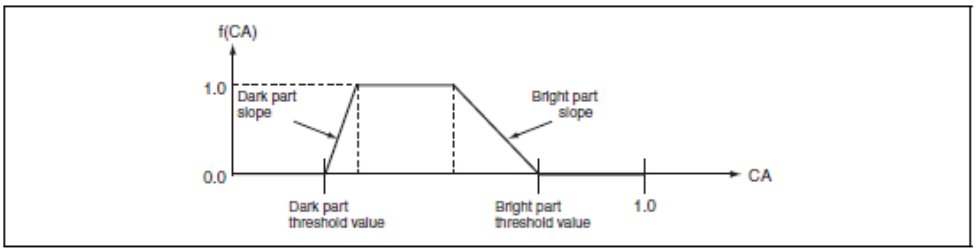


Figure 40.13 parameters for the calculation of a correction amount control coefficient

(4) Dither processing unit

This unit performs dithering processing on the lower 2 bits of the color-converted data.

- Conversion from 8 to 6 bits
- There are two choices to perform this processing: changes the value to be added on a pixel-by-pixel basis, and changes the value to be added for each frame + pixel.
  Pixel-by pixel addition: for LDCMDTHR.DTHA0 = 0, DTHA1 = 1, DTHA2 = 2, DTHA3 = 3.

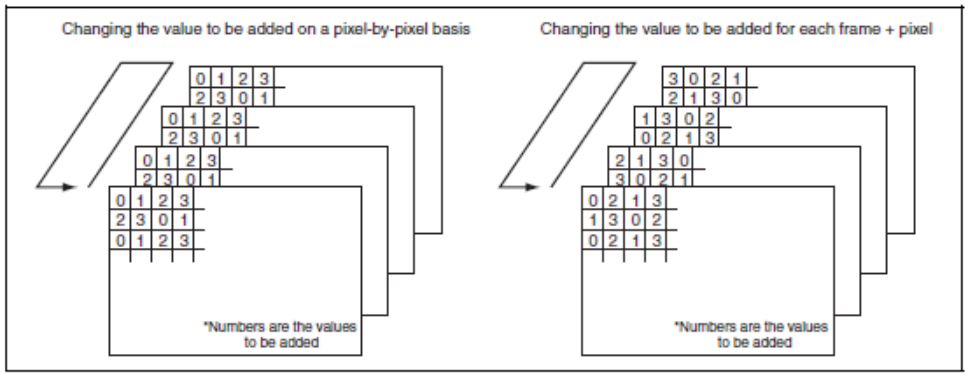


Figure 40.15 dither processing method and example

40.5 Blend Function

This LCDC has a blend function. The image of 4 channels can be operated α-blend or ROP3, and be arranged for the display image of LCD. The blend image of four channels can be overlay mutually, and the LCD display image is processed as an undermost layer in the following order in which to overlay:

LCD display image < channel 1 image < channel 2 image < channel 3 image < channel 4 image

(However, there is a limitation in the amount of overlay between the blend images. Please refer to the note.)

The α-blend or ROP3 operation function can be used in channel-1 and channel-2. In channel-3 or channel-4, all penetration and the display selection function or ROP3 operation functions can be used by the penetration color specification.

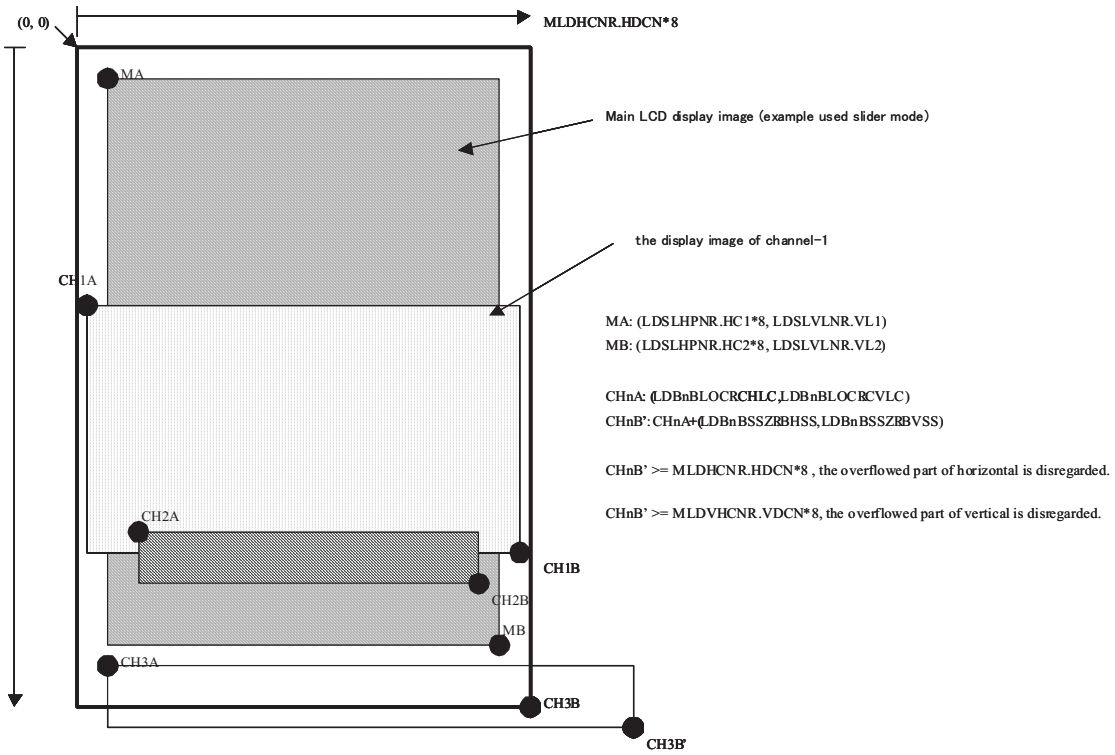


Figure 40.15 LCDC (blend function) Specification

The input image format of 4 channels must all be RGB format or YCbCr format. The input format of LCD can select RGB format or YCbCr format, it is processed according to the input format on blend side attended with the conversion of RGB/YCbCr format as follows.

LCD input format	blend side input format	LCD panel output format	the method processing		
			input conversion	blend processing	output conversion
RGB	Invalidity	RGB	None	RGB format (thought)	None
	RGB		None	RGB format	None
	YCbCr		RGB→YCbCr	YCbCr format	YCbCr→RGB (before palette)
YCbCr	Invalidity		YCbCr→RGB	RGB format (through)	None
	RGB		YCbCr→RGB	RGB format	None
	YCbCr		None	YCbCr format	YCbCr→RGB (before palette)
RGB	Invalidity	YCbCr	None	RGB format	RGB→YCbCr

			(through)	(after NCM)
	RGB	None	RGB format	RGB→YCbCr (after NCM)
	YCbCr	RGB→YCbCr	YCbCr format	None
YCbCr	Invalidity	None	YCbCr format	None
	RGB	YCbCr→RGB	RGB format	RGB→YCbCr (after NCM)
	YCbCr	None	YCbCr format	None

The input format of blend side: be judged the smallest number of the effective channel.

40.6 Blend Register Descriptions

40.6.1 Register Read/Write

The blend register divides into 4-sets (be called BC1~BC4) in each blend side n(n=1~4), and is FIFO structure on current side/program side. The register on current side is shown the setting processing and cannot be written. The register setting does to program side, controls the reflection on current side by LDBCR register.

In the LDBCR register corresponding to register set BC1~4, there is update permission bit (UPDn), update completion flag (UPFn), and update permission cancellation bit (UPCn).

- Update permission bit (UPDn): It is set that 1 is written. It is not cleared even if 0 is written, and the last value is retained. UPDn is set to 1 and the register switch timing is caused, the value on program side of register set BCn is reflected in current side. The UPDn bit is cleared automatically when reflected. Please update register set BCn when UPDn is set 0.
- Update completion flag (UPFn): UPDn is set to 1 and the register switch timing is caused, the value on program side of register set BCn is reflected in current side, it is set 1 automatically. It is cleared by writing 1. It is not cleared even if 0 is written, and the last value is retained.
- Update permission cancellation bit (UPCn): When 1 is written, the corresponding UPDn is cleared. It is usesd to update the value of the register set before the next register switch timing is generated after UPDn is set.

Example: change the setting of blend side 1

The update permission is canceled by UPC1. Write 0 to UPF1.

LDCBR ← 32’h0001_0000

Refer to the UPF1 flat when the distinction whether the last set value was reflected is necessary.

```
If (LDBBCR.UPF1){
  Set the value-1 to LDB1BLOCR
} else {
  Set the value-2 to LDB1BLOCR
}
```

After register set BC1 setting is completed, the UPD1 flag is set. At the same time, UPF1 flag clears and uses it to judge in next time.

LDBCR ← 32’h0000_0101

40.6.2 Blend control register （LDBCR）

LDBCR controls that the value on program side of register set BCn is reflected in current side. For details, see section 40.6.1, Register Read/Write.

bit：	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	UPC4	UPC3	UPC2	UPC1
initial：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W：	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

bit：	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	UPF4	UPF3	UPF2	UPF1	–	–	–	–	UPD4	UPD3	UPD2	UPD1
initial：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W：	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 20	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
19 to 16	UPC4 UPC3 UPC2 UPC1	0	R/W	Update permission cancellation bit Update permission cancel flag When 1 is written, UPDn is cleared, the update permission of register set BCn(n=1~4) is canceled. This bit is always read as 0.
15 to 12	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 8	UPF4 UPF3 UPF2 UPF1	0	R/W	Update completion flag It is set 1 automatically when register set BCn(n=1~4) update is completed. It is cleared by writing 1. It is not cleared even if 0 is written, and the last value is retained.
7 to 4	-	All 0	R	Reserved These bits always read as 0. The write value should always be 0.
3 to 0	UPD4 UPD3 UPD2 UPD1	0	R/W	Update permission bit 1 is written that register set BCn(n=1~4) update is permitted. The last value is retained when writing it 0. It is cleared to 0 automatically when updated.

40.6.3 CHn Source Image Format Register （LDBnBSIFR）

LDBnBSIFR selects the format of input image.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	EN	—	VS	BRSEL	MX	MY	CV[1:0]		LAY[7:0] / ROP3[7:0]							
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	AL[1:0]		—	—	—	SWP[2:0]			RY	—	—	RPKF[4:0] / {3'b000, CHRR[1:0]}				
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	EN	0	R/W	Enable bit 1: enable CHn 0: disable CHn
30	-	0	R	Reserved
29	VS	0	R/W	Virtual screen setting 1: virtual screen mode 0: normal In the virtual screen mode, the value of foreground color1(fg1) is used in LDBnBSAYR register. The value of foreground color 2(fg2) is used in LDBnBSACR register. Data is not fetched from the extrinsic memory, and the CHn screen is generated with the pixel with the value of fg1 and fg2. When the pixel is arranged to be (x,y) that is assumed the parents screen coordinates value, pixel value of each coordinates is set as follows X[0]^y[0] == 0 : fg1 X[0]^y[0] == 1 : fg2 ([0] is shown the LSB of coordinates value)
28	BRSEL	0	R/W	Select blend or ROP3 operation 1: ROP3 operation 0: Blend operation When the blend operation is selected with CH3 or CH4, it is processed as complete penetration when α value is 0, except when α value is 0, it is processed as complete non-penetration.
27 to 26	MX MY	0	R/W	Specify twice expansion with the direction of x and Y 1: twice expansion 0: normal Specify the size after it expands for LDBnBSSZR(source size specification register) by the even number. Specify LDBnBLOCR(blend of offset register) by the even number when expansion mode.
25 to 24	CV[1:0]	00	R/W	Penetration color control 00 : normal 01 : the penetration color specification with CHnBPCR is effective 11 : the penetration color specification with CHnBPCR and CHnBSARA is effective (it is effective only at AL[1] = 0) 10 : it is replaced with CHnBPCCR2 when the data match CHnBPCCR (it is effective only at AL[1] = 0)

Bit	Bit Name	Initial Value	R/W	Description
23 to 16	LAY[7:0]	8'b0	R/W	Set layer α-value or specify ROP3 operator
	ROP3[7:0]			Set layer α-value
				Set the value of 8-bits defined as follows to ROP3 operator.
				Pixel α-value P[7:0]
				Each pixel value S[7:0]
				Each background pixel value D[7:0]
				Pixel value [n] = ROP3 operator [{P[n], S[n], D[n]}] (n=0~7)
15 to 14	AL[1:0]	000	R/W	Specify the each pixel α-value
				00 : set 1 to α-value only 1 bit
				01 : enable the α-value of αRGB format. Accuracy depends on the format(1/4/5/6/8 bit accuracy). α-value is set 1 of the 1-bit accuracy with none α-value format of RGB or YCbCr.
				10 : plane 1 bit-α is read, and it is assumed pixel α-value of 1 bit accuracy.
				11 : plane 8 bit-α is read, and it is assumed pixel α-value of 8 bit accuracy.
				When pixel obtained α is compared with the layer α, and pixel α is larger than the layer α, it is clipped by layer α.(It is effective only at BRSEL = 0)
13 to 11	-	000	R	Reserved
10 to 8	SWP[2:0]	000	R/W	Specify the swap parameter of RGB/Y, C plane.
				The α plane is used 000 at SWP[2:0] = 000, and 111 at SWP[2:0] !=000.
				[2] = 1 : data is swapped by long word
				[1] = 1 : data is swapped by word
				[0] = 1 : data is swapped by byte
7	RY	0	R/W	Specify the input format
				0: YCbCr format
				1: RGB format
6~5	-	00	R	Reserved
4～0	RPKF[4:0]	00000	R/W	The input format is RGB:
	or			RPKF[4:0] specifies the input data of RGB back.
	000,			For details, see figure 40.7
	CHRR[1:0]			
				The input format is YCbCr:
				CHRR[1:0] specifies the input data of YCbCr back.
				00: YCbCr 4:4:4
				01: YCbCr 4:2:2
				10: YCbCr 4:2:0
				Note:
				1: when the input format is YCbCr, MLDDFR.CF1 and MLDDFR.CF0 specify ITU-R BT.601/ITU-R BT.709 and full-range YCbCr/compressed-range YCbCr.
				2: CHRR[1:0] is different with MLDDFR.YF[1:0].

40.6.4 CHn Source Size Register （LDBnBSSZR）

LDBnBSSZR specifies the input size of image (n=1~4).

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	BVSS[11:0]											
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	BHSS[11:0]											
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	-	All 0	R	Reserved
27 to 16	BVSS[11:0]	H'000	R/W	Set the number of vertical pixels read. These bits set the number of vertical read pixels of the source image. When input n is YCbCr 4:2:0, these bits can be set in 2-pixel units. For other formats, these bits can be set in 1-pixel units.
15 to 12	-	All 0	R	Reserved
11 to 0	BHSS[11:0]	H'000	R/W	Set the number of horizontal pixels read These bits set the number of horizontal read pixels of the source image. When input n is YCbCr 4:2:2 or YCbCr 4:2:0, these bits can be set in 2-pixel units. For other formats these bits can be set in 1-pixel units.

40.6.5 CHn Blend Location Register （LDBnBLOCR）

LDBnBLOCR specifies the location for input n(n=1~4).

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	CVLC[11:0]											
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	CHLC[11:0]											
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	-	All 0	R	Reserved
27 to 16	CVLC[11:0]	H'000	R/W	Specify the number of pixels for the vertical offset from the base point as the blending start location of input n (1-pixel units).
15 to 12	-	All 0	R	Reserved
11 to 0	CHLC[11:0]	H'000	R/W	Specify the number of pixels for the horizontal offset from the base point as the blending start location of input n (1-pixel units).

40.6.6 CHn Source Memory Width Register LDBnBSMWR）

LDBnBSMWR set the memory width of the source memory areas of input n(n=1~4).

bit：	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	BSMWA[15:0]															
initial：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W：	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit：	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BSMW[15:0]															
initial：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W：	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	BSMWA [15:0]	H'0000	R/W	Set the α source memory area width by long word units.
15 to 0	BSMW [15:0]	H'0000	R/W	Set the source memory area width by long word units. These bits set the horizontal width of the source memory area where the source image is located. For YCbCr 4:4:4 format, the setting is doubled because the data size of C plane is twice as large as Y plane.

40.6.7 CHn Source Address Y Register （LDBnBSAYR）

This register function changes by LDBnBSIFR.VS.

- LDBnBSIFR.VS = 0

Set the start address for the Y/RGB plane of the images read.

bit：	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	BSAY[31:16]															
initial：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W：	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit：	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BSAY[15:0]															
initial：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W：	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	BSAY[31:0]	H'0000_ 0000	R/W	Set the start address for the Y/RGB plane Set the start address for Y plane when input format is YCbCr. Set the start address for RGB plane when input format is RGB.

- LDBnBSFR.VS = 1

Set the pixel value of foreground color fg1.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	FG1A[7:0]								FG1R[7:0]							
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FG1G[7:0]								FG1B[7:0]							
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	FG1A[7:0]	H'00	R/W	Set the α value of foreground color fg1
23 to 16	FG1R[7:0]	H'00	R/W	Set the R/Cr value of foreground color fg1
15 to 8	FG1G[7:0]	H'00	R/W	Set the G/Y value of foreground color fg1
7 to 0	FG1B[7:0]	H'00	R/W	Set the B/Cb value of foreground color fg1

40.6.8 CHn Source Address C Register (LDBnBSACR)

This register changes by LDBnBSIFR.VS.

- LDBnBSIFR.VS = 0

Set the start address of C plane.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	BSAC[31:16]															
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BSAC[15:0]															
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	BSAC[31:0]	H'00	R/W	Set the start address of C plane. This register is not used when the input format is RGB.

- LDBnBSIFR.VS = 1

Set the pixel value of foreground color fg2.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	FG2A[7:0]								FG2R[7:0]							
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FG2G[7:0]								FG2B[7:0]							
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	FG2A[7:0]	H'00	R/W	Set the α value of foreground color fg2
23 to 16	FG2R[7:0]	H'00	R/W	Set the R/Cr value of foreground color fg2

Bit	Bit Name	Initial Value	R/W	Description
15 to 8	FG2G[7:0]	H'00	R/W	Set the G/Y value of foreground color fg2
7 to 0	FG2B[7:0]	H'00	R/W	Set the B/Cb value of foreground color fg2

40.6.9 CHn Source address α/CHn Penetration Color Control register 2 (LDBnBSAAR/LDBnBPCCR2)

This register changes by LDBnBSIFR.AL[1].

- LDBnBSIFR.AL[1] = 1

Set the start address of α plane.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	BSAA[31:16]															
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BSAA[15:0]															
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	BSAA[31:0]	H'0000_0000	R/W	Set the start address of α plane

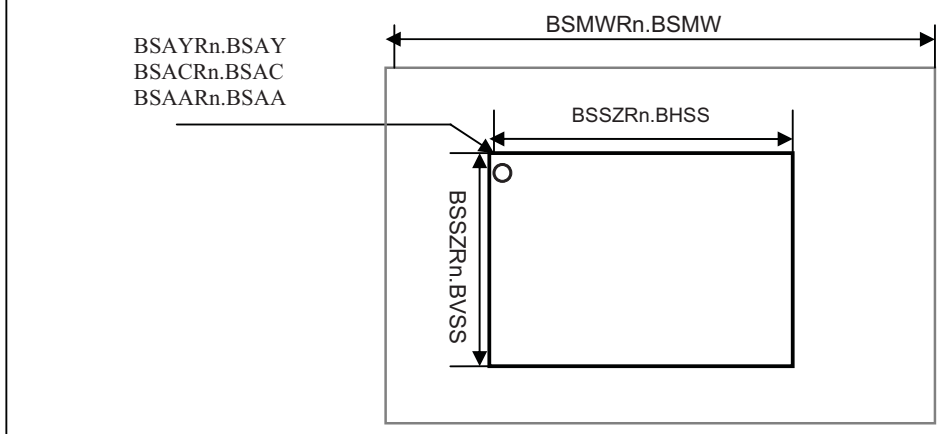
- LDBnBSIFR.AL[1] = 0

Set the value of transparent color 2. For details, see LDBnBPCCR.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	AP[7:0]								R[7:0]							
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GY[7:0]								B[7:0]							
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	AP[7:0]	H'00	R/W	Set the α-value used at a data comparison match
23 to 16	R[7:0]	H'00	R/W	Compare data R(RGB)
15 to 8	GY[7:0]	H'00	R/W	Compare data G(RGB) or Y(YCbCr)
7 to 0	B[7:0]	H'00	R/W	Compare data B(RGB)



Note : n = 1~4

Figure 40.16 the number of input pixels and start address

40.6.10 CHn Transparent Color Control Register（LDBnBPCCR）

LDBnBPCCR set the compare data used in transparent color comparison and the alpha value.

When the input format is RGB, the input data is compared with LDnBPCCR.R, GY, and B, the alpha value is replaced with LDBnBPCCR.AP that matched. It is compared between the setting of LDBnBPCCR and the value that enhances of input data to 8 bit when the packing form of less than 8 bit. This enhancing is done by the form that supplements the MSB bit. For example, the input data that RGB565 packing form is r[7:3], g[7:3], b[7:0], as follows:

r[7:0] = {r[7:3], r[7], r[7], r[7]}

g[7:0] = {g[7:3], g[7], g[7], g[7]}

b[7:0] = {b[7:3], b[7], b[7], b[7]}

Note that only the Y component is to be compared in case of YCbCr format. The alpha value is replaced with LDBnBPPCCR.AP at Y data comparison match LDBnBPCCR.GY.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	AP[7:0]								R[7:0]							
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GY[7:0]								B[7:0]							
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	AP[7:0]	H'00	R/W	Set the α-value used at a data comparison match

Bit	Bit Name	Initial Value	R/W	Description
23 to 16	R[7:0]	H'00	R/W	Compare data R(RGB)
15 to 8	GY[7:0]	H'00	R/W	Compare data G(RGB) or Y(YCbCr)
7 to 0	B[7:0]	H'00	R/W	Compare data B(RGB)

40.6.11 CHn Background Color Register （LDBnBBGCL）

LDBnBBGCL specifies the pixel value outside the image range of input. The area specified by this register is all the areas outside the image area, and is blended. The initial alpha value of background color (BGA[7:0]) is 0, and it doesn't contribute to the generation of the display image.

bit：	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	BGA[7:0]								BGR[7:0]							
initial：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W：	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit：	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BGG[7:0]								BGB[7:0]							
initial：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W：	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	BGA[7:0]	H'00	R/W	Alpha value of the outside area
23 to 16	BGR[7:0]	H'00	R/W	R/Cr value of the outside area
15 to 8	BGY[7:0]	H'00	R/W	G/Y value of the outside area
7 to 0	BGB[7:0]	H'00	R/W	B/Cb value of the outside area

40.6.12 Other Register Settings

(a) Frame Buffer Settings (for Setting to the LCD)

If the data format for frame data is YCbCr, you need to set both MLDSA1R and MLDSA2R. For the data format is RGB, set only MLDSA1R.

The horizontal size of image data on the frame buffer should be set in MLDLSR. The setting value should have a size that enables one line of data to be saved.

- Data format: YCbCr422, extension-type RGB conversion
  Y data head address: H'4000 0000
  CbCr data head address: H'4000 1000
  Horizontal image size: 480
  MLDDFR = H'0001 0100
  MLDSA1R = H'4000 0000
  MLDSA2R = H'4000 1000
  MLDLSR = H'0000 01E0[*1]
- Data format: RGB packform = 0 (32bpp)

Data address: H'E558 0000
Horizontal image size: 240
MLDDFR = H'0000 0000
MLDSA1R = H'E558 0000
MLDLSR = H'0000 03C0*2

Note: 1. The data size per pixel in the YCbCr data format is Ydata 1byte, Cdata 1byte (2 bytes in the 4:4:4 format). Set a value larger than "1 byte x horizontal size" in MLDMLSR, taking the Ydata size into consideration.
1 byte × 480 pixels = 480 = 1E0h
2. The data size per pixel in the RGB data format is as follows:
When MLDDFR.PKF[4:0]= 5'b00000, 5'b00001, 5'b00111, 5'b01100, or 5'b01101: 4 bytes
When MLDDFR.PKF[4:0]= 5'b00010, 5'b01001, 5'b01010, or 5'b01011 : 3 bytes
When MLDDFR.PKF[4:0]= 5'b00011, 5'b00101, 5'b00110, or 5'b01000 : 2 bytes
When MLDDFR.PKF[4:0]= 5'b00100 :1 byte
Set a value larger than the value multiplied by the horizontal size above.
In this case (RGB packform = 00000), it should be 4 bytes x 240 pixels = 960 = 3C0h.

40.6.13 Two-Set Register Switching

The LCDC has two sets of LCD registers.

Register sets are changed when the LCD completes its display of one frame of data and a frame end interrupt occurs.

Figure 40.17 shows an example of the timing when register sets are changed and frame end interrupts occur. Specify a register set for the next frame every time a frame end interrupt occurs.

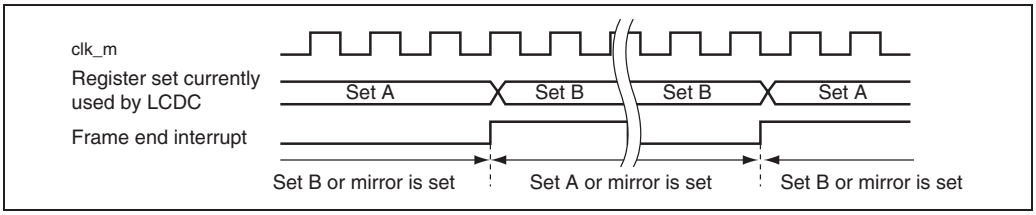


Figure 40.17 Timing of Interrupts and Register Settings

40.6.14 Autonomous Clock Stop

The LCDC stops supplying a clock to the blocks that do not need clock in standby mode and autonomously restarts supplying a clock to them when the LCDC is activated.

40.6.15 Examples of Clock and LCD Data Signals

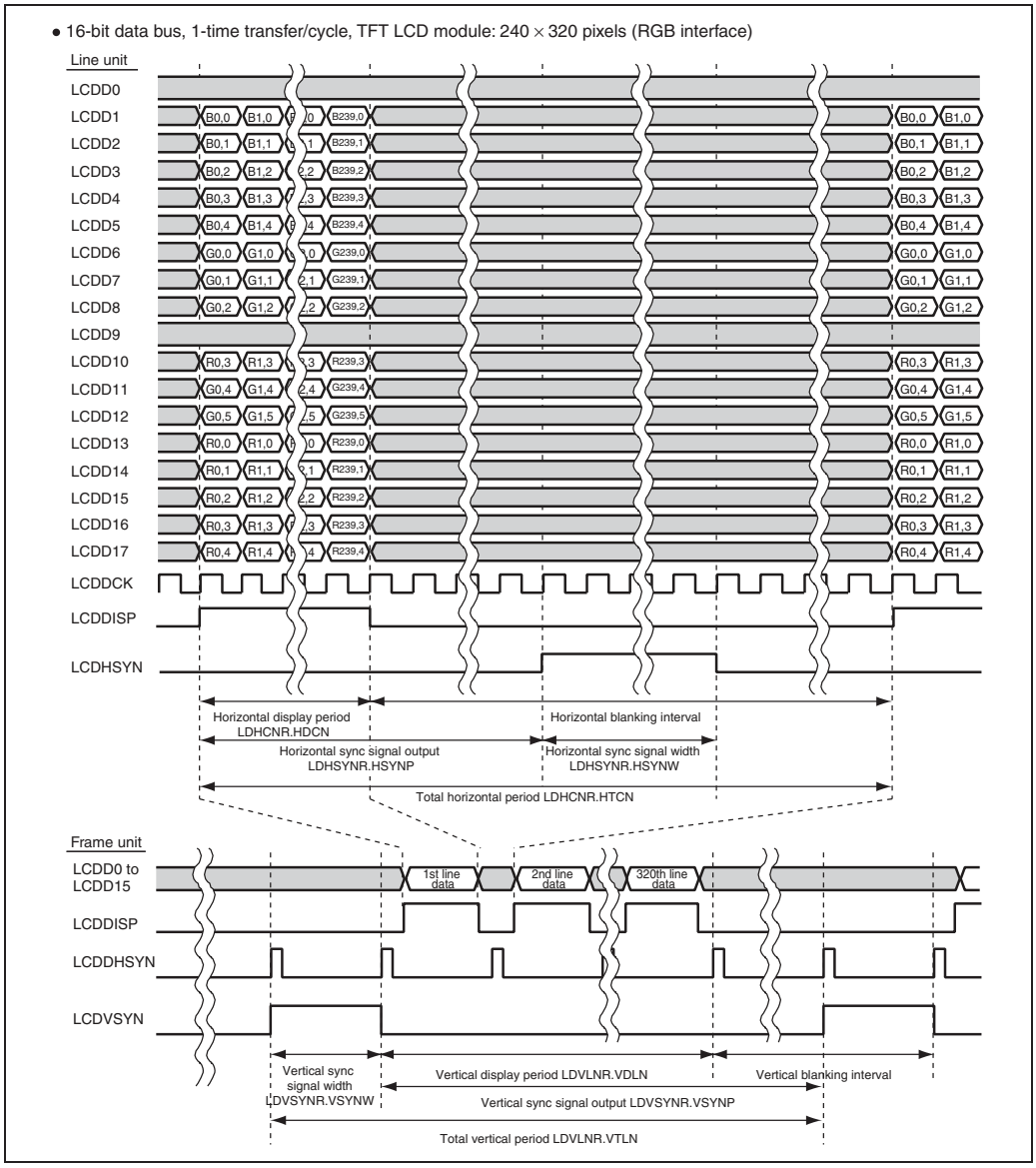


Figure 40.18 An Example of Clock and LCD Data Signals (1)

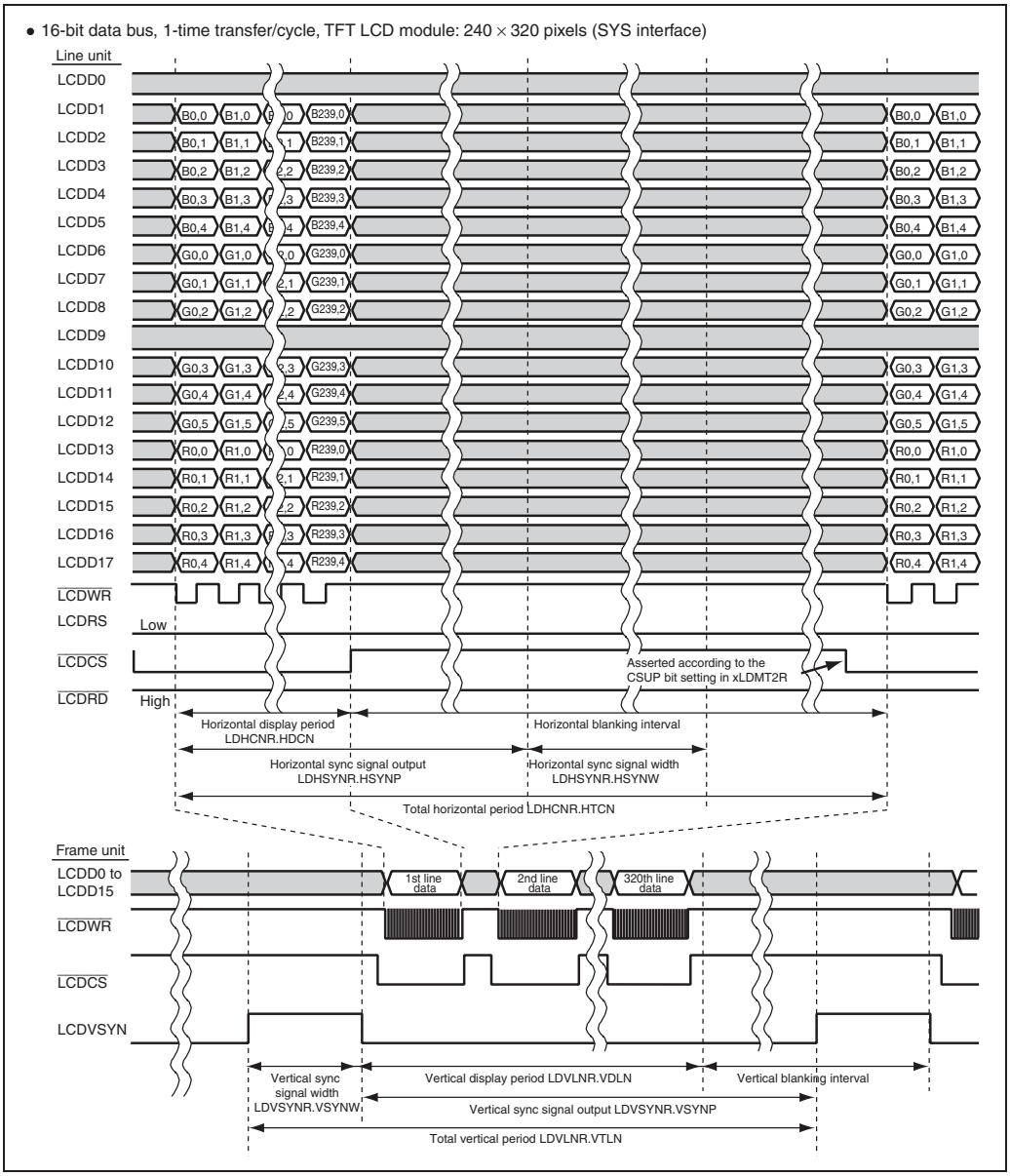


Figure 40.19 An Example of Clock and LCD Data Signals (2)

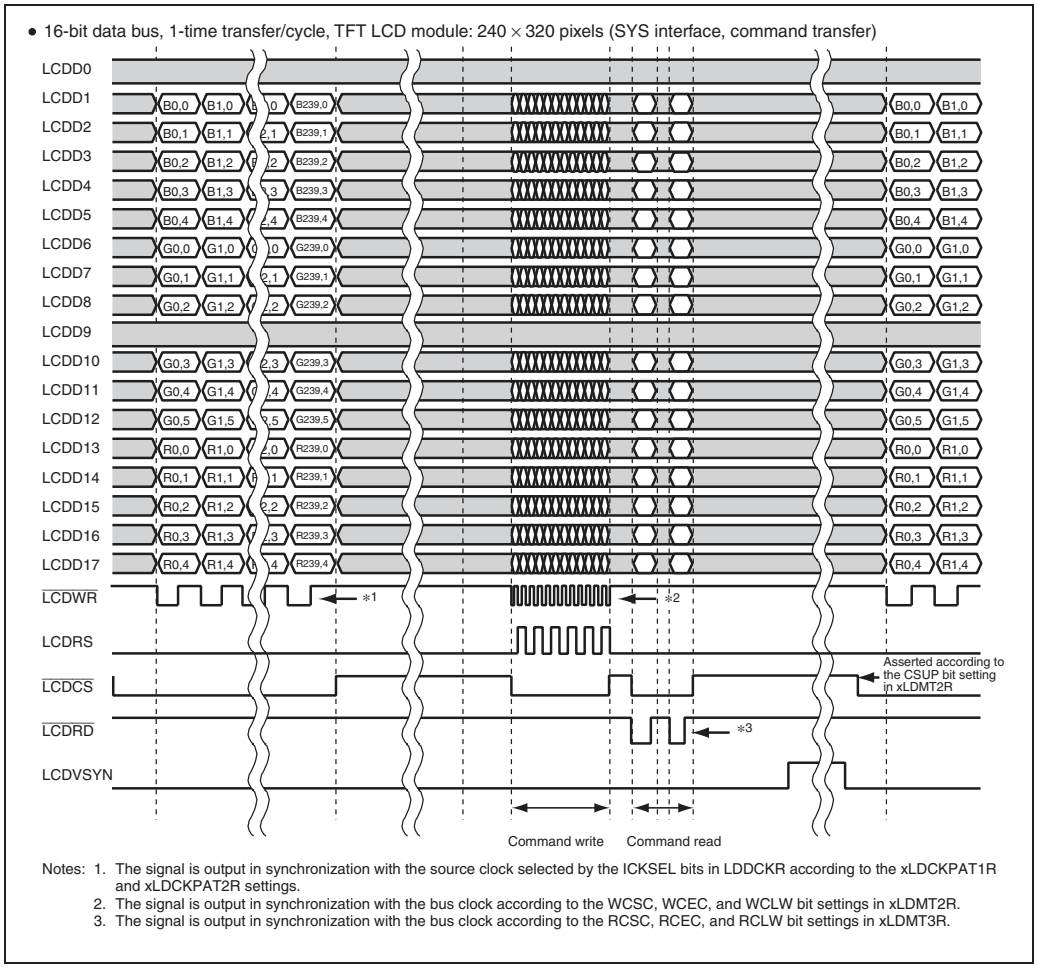


Figure 40.20 An Example of Clock and LCD Data Signals (3)

40.6.16 Data Format

(1) Main LCD Output Data Format

Figure 40.21 shows the format of the data output to the main LCD module.

Output data		DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
SYS8a (1st)	24 bpp							R7	R6	R5	R4	R3	R2	R1	R0										
SYS8a (2nd)								G7	G6	G5	G4	G3	G2	G1	G0										
SYS8a (3rd)								B7	B6	B5	B4	B3	B2	B1	B0										
SYS8b (1st)	18 bpp							R7	R6	R5	R4	R3	R2	G7	G6										
SYS8b (2nd)								G5	G4	G3	G2	B7	B6	B5	B4										
SYS8b (3rd)														B3	B2										
SYS8c (1st)	18 bpp													R7	R6										
SYS8c (2nd)								R5	R4	R3	R2	G7	G6	G5	G4										
SYS8c (3rd)								G3	G2	B7	B6	B5	B4	B3	B2										
SYS8d (1st)	16 bpp							R7	R6	R5	R4	R3	G7	G6	G5										
SYS8d (2nd)								G4	G3	G2	B7	B6	B5	B4	B3										
SYS9 (1st)	18 bpp							R7	R6	R5	R4	R3	R2	G7	G6	G5									
SYS9 (2nd)								G4	G3	G2	B7	B6	B5	B4	B3	B2									
SYS12 (1st)	24 bpp							R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4						
SYS12 (2nd)								G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0						
SYS16a (1st)	16 bpp							R7	R6	R5	R4	R3	G7	G6	G5		G4	G3	G2	B7	B6	B5	B4	B3	
SYS16b (1st)	18 bpp							R7	R6	R5	R4	R3	R2	G7	G6		G5	G4	G3	G2	B7	B6	B5	B4	
SYS16b (2nd)								B3	B2																
SYS16c (1st)	18 bpp							R7	R6																
SYS16c (2nd)								R5	R4	R3	R2	G7	G6	G5	G4		G3	G2	B7	B6	B5	B4	B3	B2	
SYS18 (1st)	18 bpp							R7	R6	R5	R4	R3	R2	G7	G6	G5	G4	G3	G2	B7	B6	B5	B4	B3	B2
SYS24 (1st)	24 bpp	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
RGB8 (1st)	24 bpp							R7	R6	R5	R4	R3	R2	R1	R0										
RGB8 (2nd)								G7	G6	G5	G4	G3	G2	G1	G0										
RGB8 (3rd)								B7	B6	B5	B4	B3	B2	B1	B0										
RGB9 (1st)	18 bpp							R7	R6	R5	R4	R3	R2	G7	G6	G5									
RGB9 (2nd)								G4	G3	G2	B7	B6	B5	B4	B3	B2									
RGB12a (1st)	24 bpp							R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4						
RGB12a (2nd)								G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0						
RGB12b (1st)	12 bpp							R7	R6	R5	R4	G7	G6	G5	G4	B7	B6	B5	B4						
RGB16 (1st)	16 bpp							R7	R6	R5	R4	R3	G7	G6	G5		G4	G3	G2	B7	B6	B5	B4	B3	
RGB18 (1st)	18 bpp							R7	R6	R5	R4	R3	R2	G7	G6	G5	G4	G3	G2	B7	B6	B5	B4	B3	B2
RGB24 (1st)	24 bpp	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
YCbCr422(1回目)	Cb7	Cb6	Cb5	Cb4	Cb3	Cb2	Cb1	Cb0	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0								
YCbCr422(2回目)	Cr7	Cr6	Cr5	Cr4	Cr3	Cr2	Cr1	Cr0	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0								

Figure 40.21 LCD Output Data Format

(2) Write-Back Data Format

Figure 40.22 shows the data format when the display data is written back.

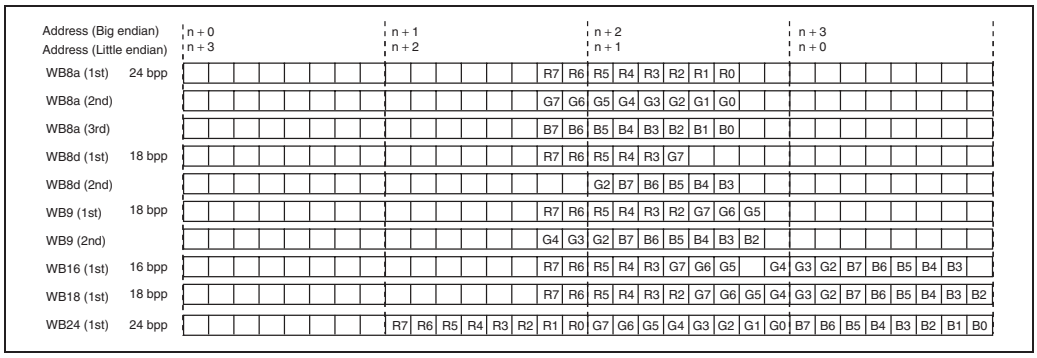


Figure 40.22 Write-Back Data Format

40.7 Usage Note

LCDC acquires all data of the LCD display every on horizontal line and the data of CHn on this line from extrinsic memory. The dot clock is high-speed, and the underflow might be caused when there is a lot of maximum data on one line.

LCD display and the blend CHn image is used by MERAM function (read flied buffer/ frame buffer cash), the MERAM direct access or LCD refresh function. LCDC must be used on the condition that the acquisition data gross weight of one line (the maximum value of the entire image, include the LCD display data) divides by 1HD period is less than 800MB/s.

Section 41 Camera Serial Interface (CSI2)

The Camera Serial Interface (CSI2) receives image data from an external camera compliant with the MIPI (Mobile Industry Processor Interface)-CSI2 standard via a high-speed differential serial interface.

41.1 Features

The CSI2 has the following major features:

This LSI mounts two CSI2 module. It is CSI2C and CSI2I.

- Performs serial-to-parallel conversion of data from a camera . And CSI2C passes parallel data to CEU2 (Camera Engine Unit) . CSI2I passes parallel data to ISP(Image Signal Processor) .
- Compliant with the MIPI-CSI2 standard
- Up to 850 Mbps (HS) transfer rate per channel
  Frequency of the serial clock is 850-200MHz.
- CSI2C is supported up to 2 lanes. CSI2I is supported up to 4 lanes.
- CSI2C mounts ECC function and CRC function. CSI2I doesn't mount them.
- Format that can receive CSI2C is YUV422,YUV420,Embedded 8bit Data, and UserDefine 8bit Data. Format that can receive CSI2I is RAW8,RAW10, and RAW12.

Connection diagram of the CSI2 is shown in figure 41.1.

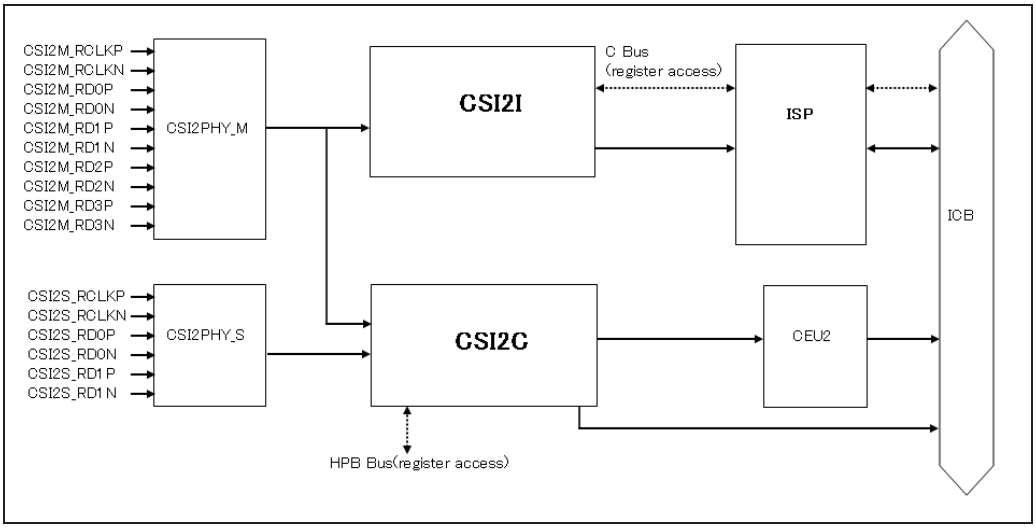


Figure 41.1 CSI2 Connection Diagram

41.2 Pin Configuration

Table 41.1 shows the CSI2 pin configuration.

Table 41.1 Pin Configuration

Pin Name	Function	I/O Type	Description
CSI2M_RCLKP CSI2S_RCLKP	CSI2 CLK differential pin (Plus)	Input	The differential signal pin (Plus) of clock input.
CSI2M_RCLKN CSI2S_RCLKN	CSI2 CLK differential pin (Minus)	Input	The differential signal pin (Minus) of clock input.
CSI2M_RD0P CSI2M_RD1P CSI2M_RD2P CSI2M_RD3P CSI2S_RD0P CSI2S_RD1P	CSI2 DATA differential pin (Plus)	Input	The differential signal pin (Plus) of data input.
CSI2M_RD0N CSI2M_RD1N CSI2M_RD2N CSI2M_RD3N CSI2S_RD0N CSI2S_RD1N	CSI2 DATA differential pin (Minus)	Input	The differential signal pin (Minus) of data input.

41.3 CSI2C Register Description

Table 41.2 shows the CSI2C register configuration. Table 41.3 shows the register states in each operating mode.

Table 41.2 Register Configuration

Register Name	Abbreviation	R/W	Address	Access Size
Control timing select register	CSI2_TREF	R/W	H'FFC9 0000	32
Software reset register	CSI2_SRST	R/W	H'FFC9 0004	32
PHY operation control register	CSI2_PHYCNT	R/W	H'FFC9 0008	32
Checksum control register	CSI2_CHKSUM	R/W	H'FFC9 000C	32
Channel data type select register	CSI2_VCDT	R/W	H'FFC9 0010	32
Embedded Data capture control register	CSI2_CAP	R/W	H'FFC9 0018	32
Field detect control register	CSI2_FLD	R/W	H'FFC9 001C	32
Monitor control register	CSI2_MONCNT	R/W	H'FFC9 0020	32
Output control register	CSI2_OUT	R/W	H'FFC9 0024	32
Long DataType setting register0	CSI2LNGDT0	R/W	H'FFC9 0028	32
Long DataType setting register1	CSI2LNGDT1	R/W	H'FFC9 002C	32
Interrupt enable register	CSI2_INTEN	R/W	H'FFC9 0030	32
Interrupt status monitor register	CSI2_INTSTATE	R/W	H'FFC9 0038	32
Short packet data register	CSI2SHPDAT	R	H’FFC9 0040	32
Short packet count register	CSI2SHPCNT	R	H’FFC9 0044	32
Direct dump control register 1	CSI2DDCNT1	R/W	H’FFC9 0050	32
Destination address register 1A	CSI2DESTADR1A	R/W	H'FFC9 0060	32
Destination address register 1B	CSI2DESTADR1B	R/W	H'FFC9 0064	32
Destination space width register 1	CSI2DESTWDT1	R/W	H'FFC9 0068	32
Direct dump reload register 1	CSI2DDRLD1	R/W	H'FFC9 006C	32
Embedded Data receive byte count register	CSI2_EBDBCUNT	R/W	H'FFC9 0154	32
Embedded Data monitor register	CSI2_EBDMON0 to 2047	R	H'FFC9 2000 to H'FFC9 3FFC	32

Table 41.3 Register States in Each Operating Mode

Register Abbreviation	Reset *	Module Standby
CSI2_TREF	Initialized	Retained
CSI2_SRST	Initialized	Retained
CSI2_PHYCNT	Initialized	Retained
CSI2_CHKSUM	Initialized	Retained
CSI2_VCDT	Initialized	Retained
CSI2_CAP	Initialized	Retained
CSI2_FLD	Initialized	Retained
CSI2_MONCNT	Initialized	Retained
CSI2_OUT	Initialized	Retained
CSI2LNGDT0	Initialized	Retained
CSI2LNGDT1	Initialized	Retained
CSI2_INTEN	Initialized	Retained
CSI2_INTSTATE	Initialized	Retained
CSI2SHPDAT	Initialized	Retained
CSI2SHPCNT	Initialized	Retained
CSI2DDCNT1	Initialized	Retained
CSI2DESTADR1A	Initialized	Retained
CSI2DESTADR1B	Initialized	Retained
CSI2DESTWDT1	Initialized	Retained
CSI2DDRLD1	Initialized	Retained
CSI2_EBDBCUNT	Initialized	Retained
CSI2_EBDMON0 to 2047	Initialized	Retained

* For details, refer to section 1-D Overview of reset.

41.3.1 Control Timing Select Register (CSI2_TREF)

CSI2_TREF selects the reflection timing for the CSI2 registers.

It covers the following registers:

- Channel data type select register (CSI2_VCDT)
- Embedded Data capture control register (CSI2_CAP)
- Field detect control register (CSI2_FLD)
- Monitor control register (CSI2_MONCNT)
- Output control register (CSI2_OUT)

The setting of this register is effective immediately after it is configured (immediately reflected).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TREF
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	TREF	0	R/W	Register Reflection Timing Select Bit 0: Upon completion of frame processing 1: Immediately

"Upon completion of frame processing" refers to when the CSI-2 completes outputting frames (the falling edge of CSIR_VD). The hardware has a double-buffer structure consisting of HPB access register and CSI2 control register.

The sequence to set the TREF bit is as follows:

1. Set the adequate registers during initialization (the TREF bit should remain B'1).
2. Then, set the TREF bit to B'0.

This sequence allows the register setting to be changed even during data processing (while the CSI-2 is operating).

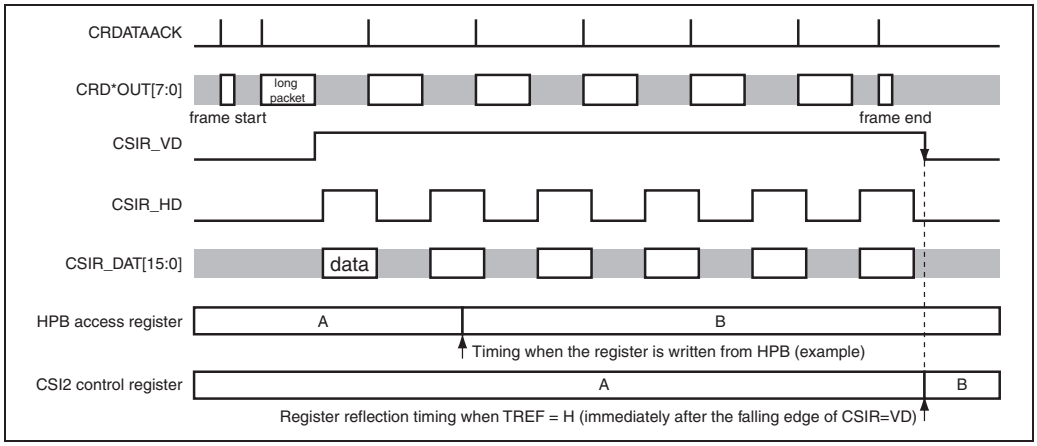


Figure 41.2 Reflection Timing on Registers

41.3.2 Software Reset Register (CSI2_SRST)

CSI2_SRST resets the CSI2C block control circuit. Note that the CSI2C register settings are not initialized by a software reset.

The setting of this register is effective immediately after it is configured (immediately reflected).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SRST
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	SRST	0	R/W	Software Reset Control Bit Set to B'1 to reset. Make sure to re-set to B'0 to clear the reset. 0: Normal operation 1: Reset

41.3.3 PHY Operation Control Register (CSI2_PHYCNT)

CSI2_PHYCNT controls the operation of the PHY.

The setting of this register is effective immediately after it is configured (immediately reflected). The setting should be configured while data input is stopped (the sensor is stopped). Changing the register setting during operating is prohibited.

	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MS_SEL	–	–	–	–	–	–	–	–	–	–	CRCLKENH	–	–	CRD1ENH	CRD0ENH
initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	MS_SEL	H'00	R/W	Select Main/Sub PHY 0: Sub PHY select 1: Main PHY select
14 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	CRCLKENH	0	R/W	Clock Lane Operation Enable Bit This bit turns on/off the PHY of clock lane. Set to B'1 to enable operation. Operation should be enabled while the CSI2 is operating. 0: Operation disabled 1: Operation enabled
3,2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
1	CRD1ENH	0	R/W	Data Lane 2 Operation Enable Bit This bit turns on/off the PHY of data lane 2. Set to B'1 to enable operation. Operation should be enabled when two lanes are used. The clock lane and data lane 1 should also be enabled via the CRCLKENH and CRD0ENH bits respectively. 0: Operation disabled 1: Operation enabled
0	CRD0ENH	0	R/W	Data Lane 1 Operation Enable Bit This bit turns on/off the PHY of data lane 1. Set to B'1 to enable operation. In this case, the clock lane should also be enabled via the CRCLKENH bit. 0: Operation disabled 1: Operation enabled

41.3.4 Checksum Control Register (CSI2_CHKSUM)

CSI2_CHKSUM controls checksum processing.

The setting of this register is effective immediately after it is configured (immediately reflected). The setting should be configured while data input is stopped (the sensor is stopped). Changing the register setting during operating is prohibited.

	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ECC_EN	CRC_EN
initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	ECC_EN	1	R/W	ECC Processing Control Bit This bit controls ECC processing of packet headers in Low Level Protocol (LLP). Set to B'1 to enable ECC. When this bit is set to B'0, packet headers are always considered to have no error and no error correction is made. 0: OFF 1: ON
0	CRC_EN	1	R/W	CRC Processing Control Bit This bit controls checksum processing of long packet data in Low Level Protocol (LLP). Set to B'1 to enable CRC checksum. When this bit is set to B'0, long packet data are always considered to have no error. 0: OFF 1: ON

41.3.5 Channel Data Type Select Register (CSI2_VCDT)

CSI2_VCDT selects a channel on which data are captured and the data type.

The reflection timing of this register can be set in the CSI2_TREF register (double-buffer scheme).

	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	SEL_VC[1:0]		–	–	SEL_DT[5:0]					
initial value :	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0
R/W :	R	R	R	R	R	R	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9, 8	SEL_VC[1:0]	00	R/W	Channel Select Bit These bit specify a channel (Virtual Channel) on which data are captured. Four channels from B'00 to B'11 are available for selection.
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5 to 0	SEL_DT[5:0]	H'1E	R/W	Data Type Select Bit These bits specify the data type of data to be captured. There are limitations on data types (refer to table 41.4). Available data types are YUV4:2:2, YUV4:2:0 (excluding Legacy), and User-Defined 8-bit Data.

Table 41.4 Summary of Data Types and Their Availabilities

Data Type	Function/Data Format	Availability	Remarks
H'00 to H'0F	Short Packet (data and no packet footers)		
H'10	Null		
H'11	Blanking Data		
H'12	Embedded 8-bit non Image Data	√	*
H'13 to H'17	Reserved		
H'18	YUV420 8-bit	√	
H'19	YUV420 10-bit		
H'1A	Legacy YUV420 8-bit		
H'1B	Reserved		
H'1C	YUV420 8-bit (Chroma Shifted Pixel Sampling)	√	
H'1D	YUV420 10-bit (Chroma Shifted Pixel Sampling)		
H'1E	YUV422 8-bit	√	
H'1F	YUV422 10-bit		
H'20	RGB444		
H'21	RGB555		
H'22	RGB565		
H'23	RGB666		
H'24	RGB888		
H'25 to H'27	Reserved		
H'28	RAW6		
H'29	RAW7		
H'2A	RAW8		
H'2B	RAW10		
H'2C	RAW12		
H'2D	RAW14		
H'2E to H'2F	Reserved		
H'30	User Defined 8-bit Data Type 1	√	Such as JPEG
H'31	User Defined 8-bit Data Type 2	√	Such as JPEG
H'32	User Defined 8-bit Data Type 3	√	Such as JPEG
H'33	User Defined 8-bit Data Type 4	√	Such as JPEG

Data Type	Function/Data Format	Availability	Remarks
H'34 to H'37	Reserved		
H'38 to H'3F	Reserved		

Note: * A separate setting is required for capturing.

41.3.6 Embedded Data Capture Control Register (CSI2_CAP)

CSI2_CAP controls capturing of Embedded Data.

The reflection timing of this register can be set in the CSI2_TREF register (double-buffer scheme).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	CAP_EBD
initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	CAP_EBD	1	R/W	Embedded Data Capture Control Bit This bit controls capturing of Embedded Data. Embedded Data appear before (as the first part) or after (as the last part) a valid line during a frame period. Set this bit to B'1 to enable capturing. Embedded Data are transferred to dedicated SRAM (8 kbytes) and can be monitored from HPB. Embedded Data more than 8 kbytes per channel cannot be stored. 0: Capturing disabled 1: Capturing enabled

41.3.7 Field Detect Control Register (CSI2_FLD)

CSI2_FLD controls detection of the first field in an interlaced image.

The reflection timing of this register can be set in the CSI2_TREF register (double-buffer scheme).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	FLD_NUM[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FLD_EN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	FLD_NUM[15:0]	H'0000	R/W	First Field Number Set Bit The setting is used to detect the first field in an interlaced image. To detect it, the WC value (16 bits) in a Frame Start packet is referenced. If the WC value matches the setting, it is detected as the first field. The CSIR_FLD signal is driven High during the corresponding frame period. Set a value within a range from 0 to 3. Otherwise, normal operation is not guaranteed.
15 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	FLD_EN	0	R/W	First Field Detect Control Bit This bit is used to turn on/off detection of the first field. Set to B'1 to turn on detection. 0: Detection of the first field is turned off. 1: Detection of the first field is turned on.

41.3.8 Monitor Control Register (CSI2_MONCNT)

CSI2_MONCNT controls monitoring of Embedded Data.

The setting of this register is effective immediately after it is configured (immediately reflected).

The CAP_EBD bit in the CSI2_CAP register should be set to B'1 before monitoring is enabled. Enable monitoring after one frame of Embedded Data is captured.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EBD_MON_EN	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	EBD_MON_EN	0	R/W	Embedded Data Monitor Enable Bit This bit enables monitoring of Embedded Data. Disable monitoring (set to B'0) while Embedded Data are being captured. Enable it (set to B'0) when they are read. Embedded Data cannot be read with monitoring disabled. 0: Monitoring is disabled (normal setting). 1: Monitoring is enabled.
0	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.

41.3.9 Output Control Register (CSI2_OUT)

CSI2_OUT sets the CSI2 output horizontal blanking period and enables/disables the CSI2 output.

The reflection timing of this register can be set in the CSI2_TREF register (double-buffer scheme).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	OUT_BLANK[15:0]															
initial value:	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

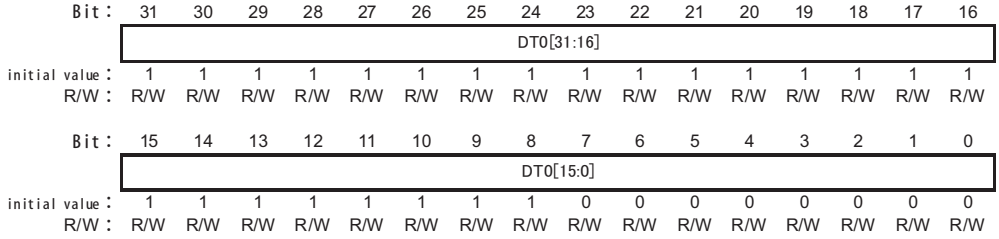
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	OUT_STOP
initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	OUT_BLANK [15:0]	H'0080	R/W	Output Horizontal Blanking Period Control Bit These bits set the CSI2C output horizontal blanking period (minimum value) in YUV420 mode. This setting is invalid for other data formats. The period is specified in CLKCSI clock cycles. The specified period is calculated as a half of the CSI output clock CSIR_CLK with the fraction rounded up. A value of 0 cannot be specified. Specifying a value larger than needed causes an overflow during YUV420 conversion, resulting in incorrect data.
15 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	OUT_STOP	0	R/W	Output Disable Control Bit This bit disables/enables the CSI2C output. When it is disabled, To CEU2 signal's are fixed to Low. 0: Output enabled 1: Output disabled

41.3.10 Long DataType setting register0 (CSI2LNGDT0)

Long/short packet of each data type (0x1f – 0x00) is set.

The initial value conforms to the standard of CSI2.

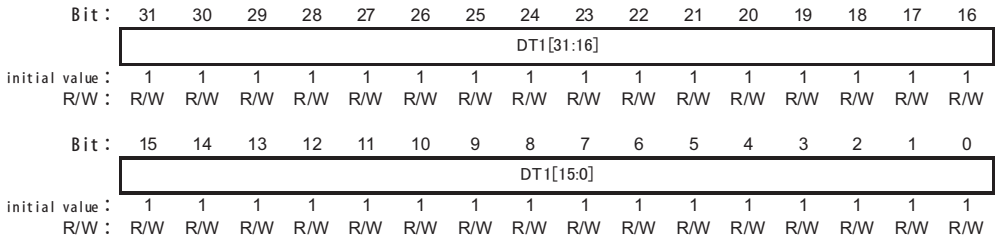


Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DT0 [31:0]	H'FFFF_ FF00	R/W	Setting Long or Short. DT0[31] corresponds to "0x1F" of the DataType. DT0[0] corresponds to "0x00" of the DataType. 0 : short packet 1 : long packet

41.3.11 Long DataType setting register1 (CSI2LNGDT1)

Long/short packet of each data type (0x3f – 0x20) is set.

The initial value conforms to the standard of CSI2.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DT1 [31:0]	H'FFFF_ FFFF	R/W	Setting Long or Short. DT1[31] corresponds to "0x3F" of the DataType. DT1[0] corresponds to "0x20" of the DataType. 0 : short packet 1 : long packet

41.3.12 Interrupt Enable Register (INT_EN)

INT_EN controls interrupts.

Interrupts (INT31 to INT00) can be enabled or disabled individually. If enabled, they can output to the INT_CSI port. INT_CSI is a signal in which INT31 to INT00 are tied together as one bit and is meaningful when it is Low. The source of each interrupt can be checked in the interrupt status register.

The setting of this register is effective immediately after it is configured (immediately reflected).

Bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	INT31	INT30	–	–	–	INT26	INT25	INT24	–	–	–	–	–	–	INT17	INT16
initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R	R	R	R/W	R/W	R/W	R	R	R	R	R	R	R/W	R/W

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INT15	INT14	–	INT12	INT11	INT10	INT9	INT8	–	INT6	–	INT4	–	–	INT1	INT0
initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R	R/W	R	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	INT31	0	R/W	Interrupt 31 (INT_RELOAD1_AB) Enable Bit When setting it as CSI2DDRLD1.E_AB=1, It is showing interrupt as for changing the output address to CSI2DESTADR1B from CSI2DESTADR1A. 0: Interrupt disabled 1: Interrupt enabled
30	INT30	0	R/W	Interrupt 31 (INT_RELOAD1_BA) Enable Bit When setting it as CSI2DDRLD1.E_BA=1, It is showing interrupt as for changing the output address to CSI2DESTADR1A from CSI2DESTADR1B. 0: Interrupt disabled 1: Interrupt enabled
29 to 27	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
26	INT26	0	R/W	Interrupt 26 (INT_VD_START) Enable Bit VD output start (start of frame) interrupt from the CSI2. This interrupt is issued synchronously with the rising edge of the CSIR_VD signal. 0: Interrupt disabled 1: Interrupt enabled
25	INT25	0	R/W	Interrupt 25 (INT_VD_END) Enable Bit VD output end (end of frame) interrupt from the CSI2. This interrupt is issued synchronously with the falling edge of the CSIR_VD signal. 0: Interrupt disabled 1: Interrupt enabled
24	INT24	0	R/W	Interrupt 24 (INT_EBD_WR_END) Enable Bit Embedded Data write end interrupt. This interrupt is issued on the basis of frame. 0: Interrupt disabled 1: Interrupt enabled
23 to 18	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
17	INT17	0	R/W	Interrupt 17 (INT_SHP_STB) Enable Bit Short packet receive interrupt. This interrupt is issued when a short packet such as Frame Start and Frame End is received. 0: Interrupt disabled 1: Interrupt enabled
16	INT16	0	R/W	Interrupt 16 (INT_LNP_STB) Enable Bit Long packet receive interrupt . This interrupt is issued when a long packet such as YUV data and Embedded Data is received. 0: Interrupt disabled 1: Interrupt enabled

Bit	Bit Name	Initial Value	R/W	Description
15	INT15	0	R/W	Interrupt 15 (INT_BUF_ERR) Enable Bit Buffer error interrupt. This interrupt is issued when an overflow occurs during converting from YUV420 to YUV422. The causes of overflow include short blanking period between packets or inadequate (too large) OUT_BLANK value. 0: Interrupt disabled 1: Interrupt enabled
14	INT14	0	R/W	Interrupt 14 (INT_CRC_ERR) Enable Bit CRC error interrupt. This interrupt is issued when there is a data error in long packets. To enable CRC check, set the CRC_EN bit in the CSI2_CHKSUM register to B'1. 0: Interrupt disabled 1: Interrupt enabled
13	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	INT12	0	R/W	Interrupt 12 (INT_HD_WC_ZERO) Enable Bit WC zero interrupt. This interrupt is issued when the WC (Word Count) value in the packet header of a long packet is 0. 0: Interrupt disabled 1: Interrupt enabled
11	INT11	0	R/W	Interrupt 11 (INT_FRM_SEQ_ERR1) Enable Bit Frame sequence error 1 interrupt. This interrupt is issued when an invalid Frame End packet is received. 0: Interrupt disabled 1: Interrupt enabled The sequence error may be caused in the following cases, in which it is assumed that the same channel is used: A Frame End packet is received without receiving a Frame Start packet. More than one Frame End packets are received serially.

Bit	Bit Name	Initial Value	R/W	Description
10	INT10	0	R/W	Interrupt 10 (INT_FRM_SEQ_ERR0) Enable Bit Frame sequence error 0 interrupt. This interrupt is issued when an invalid Frame Start packet is received. 0: Interrupt disabled 1: Interrupt enabled The sequence error may be caused in the following case, in which it is assumed that the same channel is used: More than one Frame Start packets are received serially.
9	INT09	0	R/W	Interrupt 09 (INT_ECC_ERR) Enable Bit ECC error interrupt. This interrupt is issued when there are more than one bit of error in a packet header detected during ECC processing or when there is an error in the ECC code. To enable ECC processing, set the ECC_EN bit in the CSI2_CHKSUM register to B'1. 0: Interrupt disabled 1: Interrupt enabled
8	INT08	0	R/W	Interrupt 08 (INT_ECC_CRCT_ERR) Enable Bit ECC1 bit correction interrupt. This interrupt is issued when a single bit error is corrected during ECC processing. To enable ECC processing, set the ECC_EN bit in the CSI2_CHKSUM register to B'1. 0: Interrupt disabled 1: Interrupt enabled
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6	INT06	0	R/W	Interrupt 06 (INT_DERR1B_SYNC) Enable Bit SYNC code 1 bit error interrupt. This interrupt is issued when the CRDATAERR1B input becomes High. 0: Interrupt disabled 1: Interrupt enabled

Bit	Bit Name	Initial Value	R/W	Description
5	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
4	INT04	0	R/W	Interrupt 04 (INT_LP11ERR_PSCK) Enable Bit Clock lane PHY state error interrupt. This interrupt is issued when LP-11 is input in an incorrect sequence during maintaining PHY states. 0: Interrupt disabled 1: Interrupt enabled
3, 2	—	00	R	Reserved These bits are always read as 0. The write value should always be 0.
1	INT01	0	R/W	Interrupt 01 (INT_LP11ERR_PSDT1) Enable Bit Data lane 2 PHY state error interrupt. This interrupt is issued when LP-11 is input in an incorrect sequence during maintaining PHY states. 0: Interrupt disabled 1: Interrupt enabled
0	INT00	0	R/W	Interrupt 00 (INT_LP11ERR_PSDT0) Enable Bit Data lane 1 PHY state error interrupt. This interrupt is issued when LP-11 is input in an incorrect sequence during maintaining PHY states. 0: Interrupt disabled 1: Interrupt enabled

41.3.13 Interrupt Status Monitor Register (INT_STATE)

INT_STATE is used to monitor interrupt sources.

INT_STATE holds B'1 when an interrupt occurs and is cleared by a write to clear (writing B'1) from CPU.

The interrupt sources are held regardless of the interrupt enable (INT_EN) settings.

The setting of this register is effective immediately after it is configured (immediately reflected).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IST31	IST30	–	–	–	IST26	IST25	IST24	–	–	–	–	–	–	IST17	IST16
initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R	R	R/W	R/W	R/W	R	R	R	R	R	R	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IST15	IST14	–	IST12	IST11	IST10	IST9	IST8	–	IST6	–	IST4	–	–	IST1	IST0
initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R	R/W	R	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	IST31	0	R/W	Interrupt 31 (IST_RELOAD1_AB) Monitor Bit Cleared by WRITE access: 1: Interrupt is cleared. Functions as a status monitor in READ access: 0: Operating normally 1: Interrupt has occurred.
30	IST30	0	R/W	Interrupt 30 (IST_RELOAD1_BA) Monitor Bit Cleared by WRITE access: 1: Interrupt is cleared. Functions as a status monitor in READ access: 0: Operating normally 1: Interrupt has occurred.
29 to 27	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
26	IST26	0	R/W	Interrupt 26 (IST_VD_START) Monitor Bit Cleared by WRITE access: 1: Interrupt is cleared. Functions as a status monitor in READ access: 0: Operating normally 1: Interrupt has occurred.
25	IST25	0	R/W	Interrupt 25 (IST_VD_END) Monitor Bit Cleared by WRITE access: 1: Interrupt is cleared. Functions as a status monitor in READ access: 0: Operating normally 1: Interrupt has occurred.
24	IST24	0	R/W	Interrupt 24 (IST_EBD_WR_END) Monitor Bit Cleared by WRITE access: 1: Interrupt is cleared. Functions as a status monitor in READ access: 0: Operating normally 1: Interrupt has occurred.
23 to 18	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
17	IST17	0	R/W	Interrupt 17 (IST_SHP_STB) Monitor Bit Cleared by WRITE access: 1: Interrupt is cleared. Functions as a status monitor in READ access: 0: Operating normally 1: Interrupt has occurred.

Bit	Bit Name	Initial Value	R/W	Description
16	IST16	0	R/W	Interrupt 16 (IST_LNP_STB) Monitor Bit Cleared by WRITE access: 1: Interrupt is cleared. Functions as a status monitor in READ access: 0: Operating normally 1: Interrupt has occurred.
15	IST15	0	R/W	Interrupt 15 (IST_BUF_ERR) Monitor Bit Cleared by WRITE access: 1: Interrupt is cleared. Functions as a status monitor in READ access: 0: Operating normally 1: Interrupt has occurred.
14	IST14	0	R/W	Interrupt 14 (IST_CRC_ERR) Monitor Bit Cleared by WRITE access: 1: Interrupt is cleared. Functions as a status monitor for READ access: 0: Operating normally 1: Interrupt has occurred.
13	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
12	IST12	0	R/W	Interrupt 12 (IST_HD_WC_ZERO) Monitor Bit Cleared by WRITE access: 1: Interrupt is cleared. Functions as a status monitor for READ access: 0: Operating normally 1: Interrupt has occurred.
11	IST11	0	R/W	Interrupt 11 (IST_FRM_SEQ_ERR1) Monitor Bit Cleared by WRITE access: 1: Interrupt is cleared. Functions as a status monitor for READ access: 0: Operating normally 1: Interrupt has occurred.

Bit	Bit Name	Initial Value	R/W	Description
10	IST10	0	R/W	Interrupt 10 (IST_FRM_SEQ_ERR0) Monitor Bit Cleared by WRITE access: 1: Interrupt is cleared. Functions as a status monitor for READ access: 0: Operating normally 1: Interrupt has occurred.
9	IST09	0	R/W	Interrupt 09 (IST_ECC_ERR) Monitor Bit Cleared by WRITE access: 1: Interrupt is cleared. Functions as a status monitor for READ access: 0: Operating normally 1: Interrupt has occurred.
8	IST08	0	R/W	Interrupt 08 (IST_ECC_CRCT_ERR) Monitor Bit Cleared by WRITE access: 1: Interrupt is cleared. Functions as a status monitor for READ access: 0: Operating normally 1: Interrupt has occurred.
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6	IST06	0	R/W	Interrupt 06 (IST_DERR1B_SYNC) Monitor Bit Cleared by WRITE access: 1: Interrupt is cleared. Functions as a status monitor for READ access: 0: Operating normally 1: Interrupt has occurred.
5	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
4	IST04	0	R/W	Interrupt 04 (IST_LP11ERR_PSCK) Monitor Bit Cleared by WRITE access: 1: Interrupt is cleared. Functions as a status monitor for READ access: 0: Operating normally 1: Interrupt has occurred.
3, 2	—	00	R	Reserved These bits are always read as 0. The write value should always be 0.
1	IST01	0	R/W	Interrupt 01 (IST_LP11ERR_PSDT1) Monitor Bit Cleared by WRITE access: 1: Interrupt is cleared. Functions as a status monitor for READ access: 0: Operating normally 1: Interrupt has occurred.
0	IST00	0	R/W	Interrupt 00 (IST_LP11ERR_PSDT0) Monitor Bit Cleared by WRITE access: 1: Interrupt is cleared. Functions as a status monitor for READ access: 0: Operating normally 1: Interrupt has occurred.

41.3.14 Short packet data register (CSI2SHPDAT)

The received short packet is stored. FrameStart, FrameEnd and EOT(DataType=0x08) is excepted. It is FIFO structure, and it stores it up to 9. Whenever leading, the following data is displayed.

Bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ECC[7:0]								WC[15:8]							
initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WC[7:0]								VC[1:0]		DT[5:0]					
initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	ECC[7:0]	H'00	R	Corrected ECC
23 to 8	WC[15:0]	H’0000	R	Received data
7,6	VC[1:0]	H’0	R	Virtual channel
5 to 0	DT[5:0]	H’00	R	Data Type

41.3.15 Short packet count register (CSI2SHPCNT)

The number of short packet stored in FIFO of CSI2SHPDAT is shown.

Bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	OVF
initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	NUM[3:0]			
initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	OVF	H'0	R	It is shown that FIFO becomes full, and there is an annulled packet.
15 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	NUM[3:0]	H'0	R	Number of short packets stored in FIFO . The maximum is 9.

41.3.16 Direct dump control register 1 (CSI2DDCNT1)

The function to output data is provided directly without CEU2.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CONTI	–	–	–	–	–	ST_EN1	I_EN1	–	ST_AB1	CH_AB1	DR_AB1	–	SWAP1[2:0]		
initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R/W	R/W	R	R	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	CONTI	H'0	R/W	In the standard of CSI2, only one HS-packet can be received for the HS period of one time. The continuous reception of HS-packet becomes possible by making this bit "1". However, there is a limitation. (1)The data length of Long-packet is every 4 bytes. (2)The maximum packet size is 8kbyte. (3) It is not possible to use it together with the output function to CEU2. (4) It is necessary to add the EOT packet(DT='h08) at the end of the packet group. (5)CSI2DDCNT1.ST_EN1 = 0
14 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
9	ST_EN1	H'0	R/W	Output address computational method 0: Continuous mode All the packet data is output to a consecutive address. 1: Stride mode The data of each packet is output to the address where the value of CSI2DESTWDT1 was added every one packet.
8	I_EN1	H'0	R/W	Direct output function enable 0: disable 1: enable
7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6	ST_AB1	H'0	R	Use side of destination base address 0: CSI2DESTADR1A 1: CSI2DESTADR1B
5	CH_AB1	H'0	R/W	Auto change output base address 0: Not change 1: Changes at each reception completion of the frame.
4	DR_AB1	H'0	R/W	Select Start base address 0: CSI2DESTADR1A 1: CSI2DESTADR1B
3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2 to 0	SWAP1[2:0]	H'0	R/W	Output data swap setting Bit2 : long word swap Bit1: word swap Bit0: byte swap

41.3.17 Destination address register 1A (CSI2DESTADR1A)

The base address to which the packet data is output is set. It is side A in two address settings.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ADR[31:16]															
initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ADR[15:0]															
initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	ADR[31:4]	H'0000000	R/W	Destination address A side
	ADR[3:0]	H'0	R	

41.3.18 Destination address register 1B (CSI2DESTADR1B)

The base address to which the packet data is output is set. It is side B in two address settings.

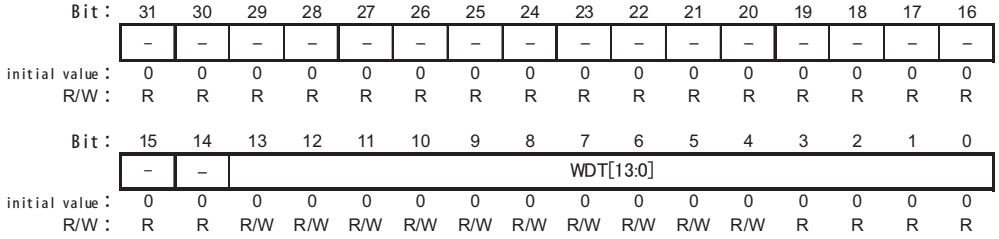
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ADR[31:16]															
initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ADR[15:0]															
initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	ADR[31:4]	H'0000000	R/W	Destination address B side
	ADR[3:0]	H'0	R	

41.3.19 Destination space width register (CSI2DESTWDT1)

The width of the storage space of about one packet is set.



Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13 to 0	WDT[13:4]	H'000	R/W	Width of storage space
	WDT[3:0]	H'0	R	

41.3.20 Direct dump reload register1 (CSI2DDRLD1)

The upper limit of storage space is set.

When it reaches limit, Change of address and reload, or stop is set.

Bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RL_EN	–	E_AB	E_BA	–	–	–	–	LIMIT[23:16]							
initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LIMIT[15:0]															
initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	RL_EN	0	R/W	Reload enable 0 : Limit setting of storage space is invalid. 1 : Limit setting of storage space is effective.
30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29	E_AB	0	R/W	When it reached limit, If the address use side is CSI2DESTADR1A, 0 : Stop store 1 : address change(-> CSI2DESTADR1B) and restart.
28	E_BA	0	R/W	When it reached limit, If the address use side is CSI2DESTADR1B, 0 : Stop store 1 : address change(-> CSI2DESTADR1A) and restart.
27 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23to 0	LIMIT [23:4]	H'00000	R/W	Limit of storage space.
	LIMIT[3:0]	H'0	R	

41.3.21 Embedded Data Receive Byte Count Register (EBD_BCUNT)

EBD_BCUNT monitors the number of received Embedded Data bytes.

Though the maximum value of the byte counter is H'FFFF FFFF, an overflow occurs when the byte count exceeds H'0000 2000 because the Embedded Data monitor register is 8 Kbytes (8192 bytes) in size. If the value exceeds the maximum counter value, it is clipped at H'FFFF FFFF.

EBD_BCUNT is refreshed when writing of Embedded Data is complete.

Bytes are counted on the basis of frame. After a frame is written, the byte count for the next frame starts.

To receive Embedded Data, set the CAP_EBD bit in the CSI2_CAP register to B'1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	EBD_BCUNT[31:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EBD_BCUNT[31:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	EBD_BCUNT [31:0]	H'0000 0000	R	Embedded Data Received Byte Count These bits are used to monitor the number of received Embedded Data bytes on the basis of frame.

41.3.22 Embedded Data Monitor Register (EBD_MONn)

EBD_MONn is an 8-Kbyte (8192-byte) register that is used to monitor Embedded Data.

To capture Embedded Data, set up the registers as follows:

1. Set the CAP_EBD bit in the CSI2_CAP register to B'1.
2. Set the EBD_MON_EN bit in the MON_CNT register to B'0.

After these setting, a data stream (in one byte units) is written from the MSB side. With these setting, data cannot be read out. Data are held on the basis of frame. When a frame is refreshed, data are overwritten from address H'A4D0 2000.

Once the amount of data written exceeds 8 Kbytes, writing of the 8193th and following bytes s is stopped.

To read the data, set the EBD_MON_EN bit in the MON_CNT register to B'1. With this setting, no Embedded Data is written.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	EBD_MON (4n+3)								EBD_MON (4n+2)							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EBD_MON (4n+1)								EBD_MON (4n)							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	EBD_MON (4n+3)	H'00	R	Embedded Data Monitor Bit
23 to 16	EBD_MON (4n+2)	H'00	R	Embedded Data Monitor Bit
15 to 8	EBD_MON (4n+1)	H'00	R	Embedded Data Monitor Bit
7 to 0	EBD_MON (4n)	H'00	R	Embedded Data Monitor Bit

Note: n: History number (0 to 2047)

41.4 CSI2C control procedure

41.4.1 Control procedure of starting

There is a possibility of doing the incorrect data in capture when a differential terminal starts CSI2 in the indetermination. Therefore, please start CSI2 after fixing all differential pins.

41.4.2 Direct dump function

The following notes exist for the direct dump function(used CSI2DDCNT1).

(1) The received data packet is stored without converting format.

(2) Y and C cannot be separated by the data of YUVformat. It is stored in the same area.

(3) The FrameStart packet is necessary ahead of the data packet.
The FrameEnd packet is necessary behind the data packet.

(4) When using it with Continuous mode(CSI2DDCNT1.ST_EN1 = 0), All receive data might not be output at once. The stay data is the maximum and is 24 bytes.
This stay data is output by pushing it out by the following receive data. Or, it is output by receiving the FrameEnd packet.

It is similar for reload mode(CSI2DDRLD1.RN_EN1=1).
For example,
It is assumed that it is set as CSI2DDRLD1.LIMIT[23:0] == 00_0190h(400byte), and received the packet in 400 bytes. At this time, 384 bytes are output, and 16 bytes stay. Moreover, interrupt(INT_STATE.IST31,IST30) not occur.

The following packet is received, interrupt occurs when 400 bytes in total are output.

41.5 CSI2C Limitations

41.5.1 Set limitation of CEU2

There is a limitation in the setting of the register of CEU2 when using it by CSI2 and synchronization. And, a special setting is necessary.

- CEU2.CAMCR.VDPOL=0 :
  The polarity of the VD signal is assumed to be a positive polarity.
- CEU2.CAMCR.HDPOL=0 :
  The polarity of the HD signal is assumed to be a positive polarity.
- CEU2.CAMOR.HOFST[12:0], CEU2.CAPWR.HWDTH[13:0]:
  Special setting is necessary. Please refer to the manual of CEU2 for details.

41.5.2 Data size limitations

There is a limitation in the data size at each data format.

- YUV422/ YUV420

  Maximum horizontal size is 8188 pixels(Maximum packet size is 16376 bytes). The pixel count should be an even number. The pixel count should be constant for one frame period.

- User Define 8-bit Data

  Maximum date size is 9900 byte. The pixel count should be constant for one frame period.

- Embedded Data

  It is 8192 bytes or less one frame

.

41.6 CSI2I Register Description

Table 41.5 shows the CSI2I register configuration. Table 41.6 shows the register states in each operating mode.

Table 41.5 Register Configuration

Register Name	Abbreviation	R/W	Address	Access Size
Control timing select register	CSI2I_TREF	R/W	H'FE8F 7000	32
Software reset register	CSI2I_SRST	R/W	H'FE8F 7004	32
PHY operation control register1	CSI2I_PHYCNT1	R/W	H'FE8F 7008	32
Control register1	CSI2I_CNT1	R/W	H'FE8F 7020	32
Pixel size register	CSI2I_SIZE	R/W	H'FE8F 7024	32
Control register2	CSI2I_CNT2	R/W	H'FE8F 7060	32
Field detect control register	CSI2I_FLD	R/W	H'FE8F 7064	32
Interrupt clear register	CSI2I_INTCLR	R/W	H'FE8F 7070	32
Interrupt enable register	CSI2I_INTEN	R/W	H'FE8F 7074	32
Interrupt monitor register	CSI2I_INTMON	R/W	H'FE8F 707C	32

Table 41.3 Register States in Each Operating Mode

Register Abbreviation	Reset *	Module Standby
CSI2I_TREF	Initialized	Retained
CSI2I_SRST	Initialized	Retained
CSI2I_PHYCNT1	Initialized	Retained
CSI2I_CNT1	Initialized	Retained
CSI2I_SIZE	Initialized	Retained
CSI2I_CNT2	Initialized	Retained
CSI2I_FLD	Initialized	Retained
CSI2I_INTCLR	Initialized	Retained
CSI2I_INTEN	Initialized	Retained
CSI2I_INTMON	Initialized	Retained

* For details, refer to section 1-D Overview of reset.

41.6.1 Control Timing Select Register (CSI2I_TREF)

CSI2I_TREF selects the reflection timing for the CSI2I registers.

It covers the following registers:

- CSI2I_SIZE
- CSI2I_CNT1
- CSI2I_CNT2
- CSI2I_FLD

The setting of this register is effective immediately after it is configured (immediately reflected).

Bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	TREF
initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	TREF	1	R/W	Register Reflection Timing Select Bit 0: Upon completion of frame processing 1: Immediately

41.6.2 Software reset register (CSI2I_SRST)

It is a control register of soft reset.

Bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	–	RSTR	RSTC	RSTP
initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	RSTR	0	R/W	Register block reset bit 0: Normality 1: Reset This bit is not cleared by the automatic operation. Please clear by software.
1	RSTC	0	R/W	Control block reset bit 0: Normality 1: Reset This bit is not cleared by the automatic operation. Please clear by software.
0	RSTP	0	R/W	PHY-control block reset bit 0: Normality 1: Reset This bit is not cleared by the automatic operation. Please clear by software.

41.6.3 PHY operation control register1 (CSI2I_PHYCNT1)

It is PHY-control register.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	CLKENH	D3ENH	D2ENH	D1ENH	D0ENH
initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	CLKENH	0	R/W	Clock Lane Operation Enable Bit 0: Operation disabled 1: Operation enabled
3	D3ENH	0	R/W	Data Lane 3 Operation Enable Bit 0: Operation disabled 1: Operation enabled
2	D2ENH	0	R/W	Data Lane 2 Operation Enable Bit 0: Operation disabled 1: Operation enabled
1	D1ENH	0	R/W	Data Lane 1 Operation Enable Bit 0: Operation disabled 1: Operation enabled
0	D0ENH	0	R/W	Data Lane 0 Operation Enable Bit 0: Operation disabled 1: Operation enabled

The setting of CSI2I_PHYCNT is decided by CSI2I_CNT1.CHLN[1:0].

- Case of CSI2I_CNT1.CHLN[1:0]=2'b00 :
  CSI2I_PHYCNT.{CLKENH,D3ENH,D2ENH,D1ENH,D0ENH} = 5'b10001
- Case of CSI2I_CNT1.CHLN[1:0]=2'b01 :
  CSI2I_PHYCNT.{CLKENH,D3ENH,D2ENH,D1ENH,D0ENH} = 5'b10011
- Case of CSI2I_CNT1.CHLN[1:0]=2'b10 :
  CSI2I_PHYCNT.{CLKENH,D3ENH,D2ENH,D1ENH,D0ENH} = 5'b10111
- Case of CSI2I_CNT1.CHLN[1:0]=2'b11:
  CSI2I_PHYCNT.{CLKENH,D3ENH,D2ENH,D1ENH,D0ENH} = 5'b11111

Other combinations are set prohibitions.

41.6.4 Control register1 (CSI2I_CNT1)

It is CSI2I control register.

Bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	PEGM	–	–	–	PSEL	–	–	CHNL[1:0]	
initial value :	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
R/W :	R	R	R	R	R	R	R	R/W	R	R	R	R/W	R	R	R/W	R/W

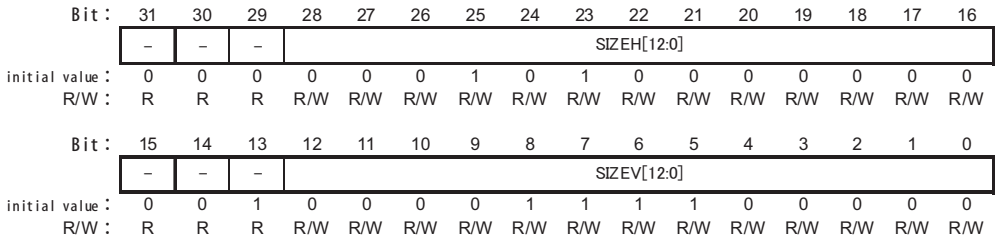
Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	DT[5:0]						–	–	–	–	–	–	–	IPEN
initial value :	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	PEGM	0	R/W	Pixel Enable generate Bit Generating PE during horizontal blanking. 0: Generate (Setting prohibited) 1: Not Generate

Bit	Bit Name	Initial Value	R/W	Description
23 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	PSEL	1	R/W	Protocol Select Bit 0: Setting prohibited 1: CSI2 select
19,18	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
17,16	CHLN[1:0]	0	R/W	Channel Lane Number Bit 2’b00: 1lane 2’b01: 2lane 2’b10: 3lane 2’b11: 4lane
15,14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13 to 8	DT[5:0]	6’h2C	R/W	Data Type Bit DT of the CSI2 standard is set. 6’h2A : 8bit Raw 6’h2B : 10bit Raw 6’h2C : 12bit Raw
7 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	IPEN	0	R/W	CSI2I Operation Enable Bit 0: Operation disabled 1: Operation enabled

41.6.5 Picture size register (CSI2I_SIZE)

It is picture size register.



Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 16	SIZEH[12:0]	13'h0280	R/W	Horizontal picture size Set
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 0	SIZEV[12:0]	13'h01E0	R/W	Vertical picture size Set

41.6.6 Control register2 (CSI2I_CNT2)

It is CSI2I control register.

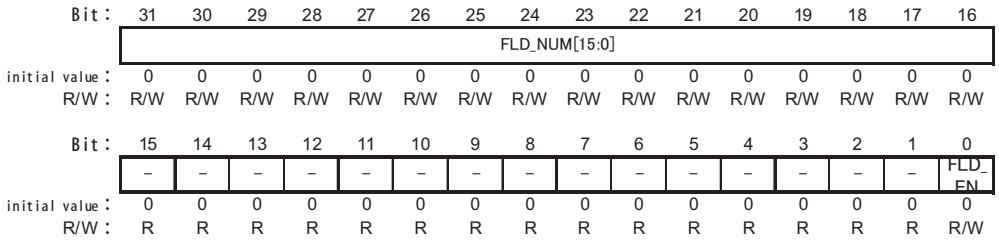
Bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	VC[1:0]		–	–	–	–
initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5,4	VC[1:0]	2'b00	R/W	Virtual channel Set
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

41.6.7 Field detect control register (CSI2I_FLD)

It is CSI2I control register.



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	FLD_NUM [15:0]	H'0000	R/W	First Field Number Set Bit The setting is used to detect the first field in an interlaced image. To detect it, the WC value (16 bits) in a Frame Start packet is referenced. If the WC value matches the setting, it is detected as the first field. The CSIR_FLD signal is driven High during the corresponding frame period. Set a value within a range from 0 to 3. Otherwise, normal operation is not guaranteed.
15 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	FLD_EN	0	R/W	First Field Detect Control Bit This bit is used to turn on/off detection of the first field. Set to B'1 to turn on detection. 0: Detection of the first field is turned off. 1: Detection of the first field is turned on.

41.6.8 Interrupt clear register (CSI2I_INTCLR)

It is CSI2I interrupt clear register.

Bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	MON	CLR
initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	MON	’b0	R	Interrupt monitor bit 0: There is no interrupt. 1: There is interrupt.
0	CLR	‘b0	R/W	Interrupt clear bit When this bit is made "1", all causes of interrupts are cleared. This bit is not cleared by the automatic operation. Please clear by software.

41.6.9 Interrupt enable register (CSI2I_INTEN)

It is CSI2I interrupt enable setup register.

Bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	INT31	INT30	–	–	–	–	–	–	–	INT22	–	INT20	–	–	–	–
initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R	R	R	R	R	R	R	R/W	R	R/W	R	R	R	R

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	INT31	‘b0	R/W	VD start interrupt enable It is asserted by the VD output beginning(frame start) from CSI2I. 0: disable 1: enable
30	INT30	’b0	R/W	VD end interrupt enable It is asserted by the VD output end(frame end) from CSI2I. 0: disable 1: enable
29 to 23	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
22	INT22	‘b0	R/W	Horizontal size error interrupt enable When the reception packet contradicts the setting of CSI2I_SIZE.HSIZE, it is asserted. 0: disable 1: enable

Bit	Bit Name	Initial Value	R/W	Description
21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	INT20	'b0	R/W	Vertical size error interrupt enable When the reception packet contradicts the setting of CSI2I_SIZE.VSIZE, it is asserted. 0: disable 1: enable
19 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

41.6.10 Interrupt monitor register (CSI2I_INTMON)

It is CSI2I interrupt monitor register.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	INS31	INS30	–	–	–	–	–	–	–	INS22	–	INS20	–	–	–	–
initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	INS31	‘b0	R	VD start interrupt 0: Operating normally 1: Interrupt has occurred.
30	INS30	’b0	R	VD end interrupt 0: Operating normally 1: Interrupt has occurred.
29 to 23	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
22	INS22	‘b0	R	Horizontal size error interrupt 0: Operating normally 1: Interrupt has occurred.
21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	INS20	‘b0	R	Vertical size error interrupt 0: Operating normally 1: Interrupt has occurred.
19 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

41.7 CSI2I control procedure

41.7.1 Control procedure of starting

There is a possibility of doing the incorrect data in capture when a differential terminal starts CSI2 in the indetermination. Therefore, please start CSI2 after fixing all differential pins.

41.7.2 CSIR_CLK setup

The clock set by the FRQCRA.CSIRFC[3:0] register of CPG is named CSIR_CLK.
CSI2I uses CSIR_CLK for the state(LowPower or HighSpeed) transition.
The frequency of CSIR_CLK is decided according to the frequency of receive clock as follows.

Receive clock	CSIR_CLK	FRQCRA.CSIFRC[3:0]
850-500MHz	37.5MHz	4'b1001
500-320MHz	16.6MHz	4'b1101
320-200MHz	12.5MHz	4'b1110

41.8 CSI2I Limitations .

41.8.1 Data size limitations

- Horizontal pixel count restriction

  It should be an even number for RAW12.

  It should be a multiple of four for RAW10.

- Maximum picture size : 4800x3600

Section 42 Display Serial Interface(DSI-Tx)

The DSI-Tx is a module that performs serial communications with LCD panels, which is compliant with the MIPI (Mobile Industry Processor Interface) Display Serial Interface specification.

42.1 Features

- Compliant with MIPI Alliance Standard for Display Serial Interface Draft Version 1.01.00 Release 09
- Compliant with the MIPI Alliance Specification for D-PHY v0.90.00
  - Functions as a DSI host processor (Tx) device.
  - Support for 4/3/2/1 lanes (HS mode)
  - Transfer mode:
    - High-speed (HS) unidirectional communication
    - Low power (LP) bidirectional communication
  - Support for video mode:
    - Non-burst mode with sync pulses
    - Non-burst mode with sync events
    - Burst mode
  - Support for command mode:
    - Command packet generation registers Long packets; 4 channels, short packets; 1 channel
    - Tearing effect (TE) trigger receive
  - Support for ultra low power mode
  - Data integrity mechanism
    - ECC/CRC code generation/addition to transmit packets
    - ECC/CRC check on receive packets
  - Virtual channel
    - 4 virtual channel supported
- Function outside DSI-Tx regulations
  - YUV422/YUV420 format transmission in the video mode
  - Data0/Data1 switching function while transmitting VsyncStart packets

Figure 42.1 shows the block diagram of DSITx0.

DSITX0 receives data from LCDC0 at the video mode, and outputs data with 4lane.

DSITX1 receives data from LCDC1 at the video mode, and outputs data with 2lane.Data .

An internal composition of DSITX1 is the same as DSITX0.

LPCLK and DSIPCLK of the figure below are about 80MHz, and from 10MHz to 50MHz respectively. Please set the rate of dividing frequency of PLL in CPG.

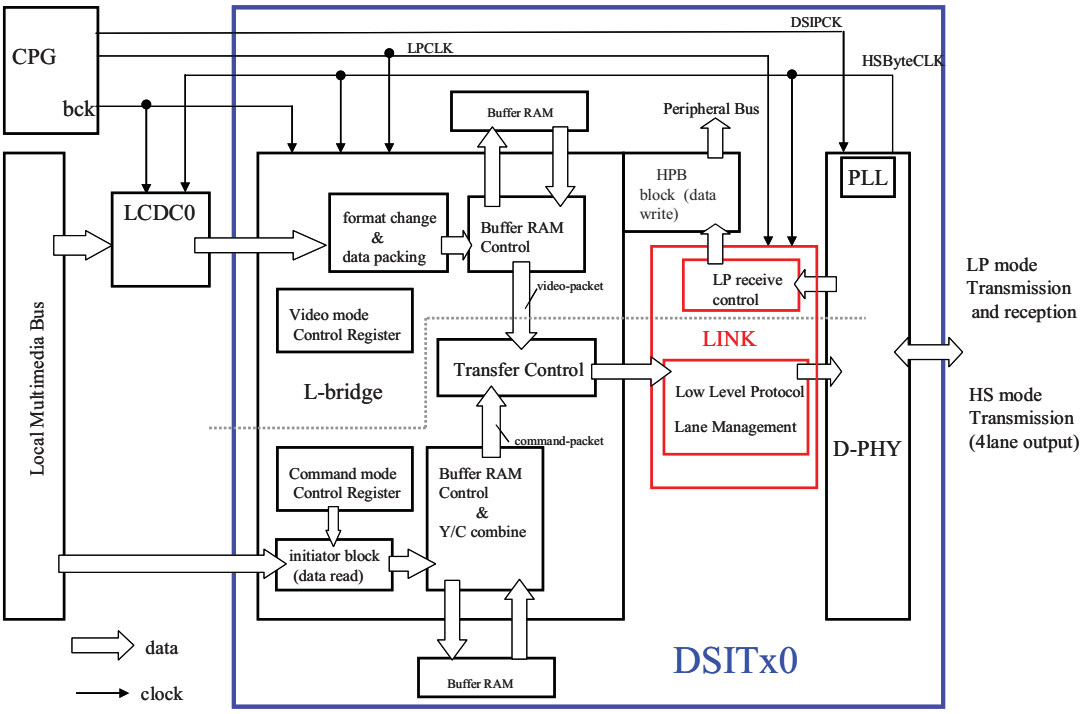


Figure 42.1 Block Diagram of DSITx0

42.1.1. block composition

The DSI-TX consists of the three major blocks:

1) D-PHY block that has Differential terminal and PLL
2) LINK block that has a direct connection with the D-PHY
3) L-bridge block that performs overall data processing

As these are practically separated modules, they may be noted individually in the description.

42.1.2. Terminology

In this document, many terms in the MIPI specification are used. For details on them, see the specification. Local terms other than those are defined as follows:

- HS byte clock: Clock that is eight dividing the high-speed serial communications clock.
  It is generated in D-PHY as follows.
  DSIPφ(DSIPCLK) (MIPI DSI PHY, 10MHz～50MHz)
  ↓
  Multiply by D-PHY(×12～×30) (PHYCTRL.PLLDS[3:0])
  ↓ ← High-speed serial communications clock(120～850Mbps)
  eight dividing
  ↓
  HS byte clock
- LP PHY clock: It is a clock that works in PHY of the LP control, and a frequency of 1/4 of LPCLK. It is generated with “AND” of LPCLK and internal enable signal.
- BLLP1: Indicates the BLLP period of VSA, VBP, and VFP lines excluding BLLP3.
- BLLP2: Indicates the BLLP period of VACT lines in the burst mode.
- BLLP3: Indicates the BLLP period immediately before the LPM of VFP lines.

42.2 Terminal composition

Table 42.1 shows the terminal composition of DSITx0.

Table 42.2 shows the terminal composition of DSITx1.

Table 42.1 DSITx0 Pin Configuration

Name	Function	I/O	Description
DSIM_TCLKP,DSIM_TCLKN	Differential clock	Output	Differential clock output
DSIM_TD0P,DSIM_TD0N	lane0 data	InOut	High-speed differential data output, LP data input/output.
DSIM_TD1P,DSIM_TD1N	lane1 data	Output	High-speed differential data output.
DSIM_TD2P,DSIM_TD2N	lane2 data	Output	High-speed differential data output.
DSIM_TD3P,DSIM_TD3N	lane3 data	Output	High-speed differential data output.

Table 42. 2 DSITx1 Pin Configuration

Name	Function	I/O	Description
DSIS_TCLKP,DSIS_TCLKN	Differential clock	Output	Differential clock output
DSIS_TD0P,DSIS_TD0N	lane0 data	InOut	High-speed differential data output, LP data input/output.
DSIS_TD1P,DSIS_TD1N	lane1 data	Output	High-speed differential data output.

42.3 Register Descriptions

Table 42.3 shows the resistor configuration of DSITx0. The resistor configuration of DSITx1 is similar to DSITx0 , though the address becomes H 'FFC7 *.

Table 42.3 Register Configuration

Register name	Abbreviation	R/W	DSI-Tx Address	Access Size
System Control Register	SYSCTRL	R/W	H'FFC60000	32
System Configuration Register	SYSCONF	R/W	H'FFC60004	32
Transition Timing Parameter Setting Register	TIMSET	R/W	H'FFC60008	32
Transmission Packet Type Setting Register 0	PTYPESET0	R/W	H'FFC60010	32
Transmission Packet Type Setting Register 1	PTYPESET1	R/W	H'FFC60014	32
Response Request Setting Register 0	RESREQSET0	R/W	H'FFC60018	32
Response Request Setting Register 1	RESREQSET1	R/W	H'FFC6001C	32
HS Transmission Time-out Setting Register	HSTTOVSET	R/W	H'FFC60020	32
LP Reception Time-out Setting Register	LPRTOVSET	R/W	H'FFC60024	32
Turn Around Time-out Setting Register	TATOVSET	R/W	H'FFC60028	32
Peripheral Reset Time-out Value Setting Register	PRTOVSET	R/W	H'FFC6002C	32
DSI-LINK Control Register	DSICTRL	R/W	H'FFC60030	32
Reception Packet Type Setting Register 0	RPTYPESET0	R/W	H'FFC60038	32
Reception Packet Type Setting Register 1	RPTYPESET1	R/W	H'FFC6003C	32
DSI-LINK Status Register	DSIS	R	H'FFC60040	32
DSI-LINK Interrupt Status Register	DSIINT	R/W	H'FFC60050	32
DSI-LINK Interrupt Enable Register	DSIINTE	R/W	H'FFC60060	32
PHY Control Register	PHYCTRL	R/W	H'FFC60070	32
DSI-L-Bridge Control Register	DTCTR	R/W	H'FFC68000	32
DSI-L-Bridge Status Register	DTST	R	H'FFC68004	32
DSI-L-Bridge Status Clear Register	DTSTCL	R/W	H'FFC68008	32
DSI-L-Bridge Interrupt Enable Register	DTIRQEN	R/W	H'FFC6800C	32
Video Mode Control Register 1	VMCTR1	R/W	H'FFC68020	32
Video Mode Control Register 2	VMCTR2	R/W	H'FFC68024	32
Video Mode Data Length Register 1	VMLEN1	R/W	H'FFC68028	32
Video Mode Data Length Register 2	VMLEN2	R/W	H'FFC6802C	32
Video Mode Data Length Register 3	VMLEN3	R/W	H'FFC68030	32
Video Mode Data Length Register 4	VMLEN4	R/W	H'FFC68034	32
Video Mode Short Packet Data Register 1	VMSDAT1	R/W	H'FFC68038	32
Video Mode Short Packet Data Register 2	VMSDAT2	R/W	H'FFC6803C	32
Command Mode Reception Control Register	CMRCTR	R/W	H'FFC68040	32
Command Mode Reception Data Register	CMRDAT	R	H'FFC68044	32

Register name	Abbreviation	R/W	DSI-Tx Address	Access Size
Command Mode Reception Header Register	CMRHEAD	R	H'FFC68048	32
Tearing Effect Request Register	CMRTEREQ	R/W	H'FFC6804C	32
Command Mode Transmission Long Packet Request CH0 Register	CMTLNGREQ0	R/W	H'FFC68060	32
Command Mode Transmission Long Packet Request CH1 Register	CMTLNGREQ1	R/W	H'FFC68064	32
Command Mode Transmission Long Packet Request CH2 Register	CMTLNGREQ2	R/W	H'FFC68068	32
Command Mode Transmission Long Packet Request CH3 Register	CMTLNGREQ3	R/W	H'FFC6806C	32
Command Mode Transmission Short Packet Request Register	CMTSRTREQ	R/W	H'FFC68070	32
Command Mode Transmission Initiator Address CH0 Register	CMTIADR0	R/W	H'FFC68080	32
Command Mode Transmission Initiator Address CH1 Register	CMTIADR1	R/W	H'FFC68084	32
Command Mode Transmission Initiator Address CH2 Register	CMTIADR2	R/W	H'FFC68088	32
Command Mode Transmission Initiator Address CH3 Register	CMTIADR3	R/W	H'FFC6808C	32
Command Mode Transmission Initiator Total Data CH0 Register	CMTITTL0	R/W	H'FFC68090	32
Command Mode Transmission Initiator Total Data CH1 Register	CMTITTL1	R/W	H'FFC68094	32
Command Mode Transmission Initiator Total Data CH2 Register	CMTITTL2	R/W	H'FFC68098	32
Command Mode Transmission Initiator Total Data CH3 Register	CMTITTL3	R/W	H'FFC6809C	32
Command Mode Transmission Initiator Address Increment CH0 Register	CMTIADRI0	R/W	H'FFC680A0	32
Command Mode Transmission Initiator Address Increment CH1 Register	CMTIADRI1	R/W	H'FFC680A4	32
Command Mode Transmission Initiator Address Increment CH2 Register	CMTIADRI2	R/W	H'FFC680A8	32
Command Mode Transmission Initiator Address Increment CH3 Register	CMTIADRI3	R/W	H'FFC680AC	32
Command Mode Transmission Initiator Repeat	CMTIRN0	R/W	H'FFC680B0	32

Register name	Abbreviation	R/W	DSI-Tx Address	Access Size
Number CH0 Register				
Command Mode Transmission Initiator Repeat Number CH1Register	CMTIRN1	R/W	H'FFC680B4	32
Command Mode Transmission Initiator Repeat Number CH2 Register	CMTIRN2	R/W	H'FFC680B8	32
Command Mode Transmission Initiator Repeat Number CH3 Register	CMTIRN3	R/W	H'FFC680BC	32
Command Mode Transmission Long Packet Control CH0 Register	CMTLNGCTR0	R/W	H'FFC680C0	32
Command Mode Transmission Long Packet Control CH1 Register	CMTLNGCTR1	R/W	H'FFC680C4	32
Command Mode Transmission Long Packet Control CH2 Register	CMTLNGCTR2	R/W	H'FFC680C8	32
Command Mode Transmission Long Packet Control CH3 Register	CMTLNGCTR3	R/W	H'FFC680CC	32
Command Mode Transmission Short Packet Control Register	CMTSRTCTR	R/W	H'FFC680D0	32
Command Mode Transmission Long Packet Data Type CH0 Register	CMTLNGDT0	R/W	H'FFC680E0	32
Command Mode Transmission Long Packet Data Type CH1 Register	CMTLNGDT1	R/W	H'FFC680E4	32
Command Mode Transmission Long Packet Data Type CH2 Register	CMTLNGDT2	R/W	H'FFC680E8	32
Command Mode Transmission Long Packet Data Type CH3 Register	CMTLNGDT3	R/W	H'FFC680EC	32

42.3.1. System Control Register (SYSCTRL)

It is a register that resets the Link block.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	SWRST
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial value	R/W	Description
31 to 1	-	All 0	R	Reserved
0	SWRST	0	R/W	Resets the LINK block. After a reset by writing 1, write 0 to clear the reset. This bit should be set for the Clock 100 cycle with the lowest frequency among the bus clock, HS byte clock, and LP clock . “1” is read for the SWRST set period. After SWRST is cleared, “0” is read. 0: Clears the LINK block reset (initial value). 1: Resets the LINK block.

42.3.2. System Configuration Register (SYSCONF)

It is a register concerning the transmission data and receive data that variously sets it.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	L123ULPSE	CONEN	CLSTPM	EOTEN	CRCCEN	ECCCEN	–	–	–	–	LANEEN[3:0]			
nitial :	0	0	1	1	0	1	1	1	0	0	0	0	0	0	0	0
R/W :	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial value	R/W	Description

Bit	Bit Name	Initial value	R/W	Description
31 to 14	-	H'00000	R	Reserved
13	L123ULPSEN	1	R/W	The ULPS transition outputs of lanes 1, 2, and 3 are set , disabling or enable. When this is enable, the ULPS transition is output . When this is disable, the LP-11 is output. Please set this bit only by initialization. 0: ULPS of lanes 1, 2, and 3 is disabled. 1: ULPS of lanes 1, 2, and 3 is enabled. (initial value)
12	CONEN	1	R/W	Enables and disables contention detection. Please set this bit only by initialization. 0: Contention detection disabled 1: Contention detection enabled (initial value)
11	CLSTPM	0	R/W	Used in the LP mode to output the HS clock (clock lane software control mode) or stop it (clock lane hardware control mode). Please set this bit only by initialization. 0: Clock lane hardware control mode (initial value) 1: Clock lane software control mode
10	EOTEN	1	R/W	Enable and disables EoT packet transmission in HS transmission. Please set this bit only by initialization. 0: EoT packet transmission disabled 1: EoT packet transmission enabled (initial value)
9	CRCCEN	1	R/W	Enables and disables CRC check in LP reception. Please set this bit only by initialization. 0: CRC check disabled 1: CRC check enabled (initial value)

Bit	Bit Name	Initial value	R/W	Description
8	ECCCEN	1	R/W	Enables and disables ECC check in LP reception. Please set this bit only by initialization. 0: ECC check disabled 1: ECC check enabled (initial value)
7 to 4	-	0000	R	Reserved
3 to 0	LANEEN[3:0]	0000	R/W	Enables and disables individual lanes. Bit[0], bit[1], bit[2], and bit[3] correspond to lane1, lane2, lane3, and lane 4 respectively. Do not set any values other than 4'b0001, 4'b0011, 4'b0111, and 4'b1111. Please set this bit only by initialization. 0000: All lanes are disabled (Initial value) 0001: Lane1 0011: Lane 2 0111: Lane 3 1111: Lane 4

42.3.3. Transition Timing Parameter Setting Register (TIMSET)

It is a register that sets the transition timing provided for by the MIPI D-PHY standard.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	WKUPVL[14:0]														
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HSTRVL[3:0]				–	HSPPVL[2:0]			CKTRVL[3:0]				–	CKPPVL[2:0]		
nitial :	1	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial value	R/W	Description

31	-	0	R	Reserved
30 to 16	WKUPVL[14:0]	All 0	R/W	Set a value for T_{WAKEUP}. This value * the LP clock period * 4 is used as the T_{WAKEUP} value. Set a value so that this value is equal to or greater than 1 ms. The operation guarantee when other values are set cannot be done. Please set this bit only by initialization.
15 to 12	HSTRVL[3:0]	1001	R/W	Set a value for $T_{HS-TRAIL}$. (This value -2.5) * the HS byte clock period is used as the $T_{HS-TRAIL}$ value. Set a value so that (this value-2.5) * the HS byte clock period fills $T_{HS-TRAIL}$ and T_{EOT}. The operation guarantee when other values are set cannot be done. Please set this bit only by initialization.
11	-	0	R	Reserved
10 to 8	HSPPVL[2:0]	000	R/W	Set a value for $T_{HS-PREPARE}$. This value multiplied by the HS byte clock period is used as the $T_{HS-PREPARE}$ value. Set a value so that this value multiplied by the HS byte clock period is between 40 ns + 4 UI and 85 ns + 6 UI. The operation guarantee when other values are set cannot be done. Please set this bit only by initialization. UI indicates one-cycle period of the high-speed serial communications clock. It becomes a unit defined in written standards of MIPI D-PHY.

7 to 4	CKTRVL[3:0]	1000	R/W	Set a value for T_{CLK_TRAIL} . This value multiplied by the HS byte clock period is used as the T_{CLK_TRAIL} value. Set a value so that this value multiplied by the HS byte clock period fills $T_{CLK\text{-}TRAIL}$ and T_{EOT}. The operation guarantee when other values are set cannot be done. Please set this bit only by initialization.
3	-	0	R	Reserved
2 to 0	CKPPVL[2:0]	000	R/W	Set a value for $T_{CLK\text{-}PREPARE}$. This value multiplied by the HS byte clock period is used as the $T_{CLK\text{-}PREPARE}$ value. Set a value so that this value multiplied by the HS byte clock period is between 38 ns and 95 ns. The operation guarantee when other values are set cannot be done. Please set this bit only by initialization.

42.3.4. Transmission Packet Type Setting Register 0 (PTYPESET0)

It is a register that sets the packet type (long packet / short packet)
of each Data Type (from 00 0000 to 01 1111) of the transmission packet.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PTS[31:16]															
nitial :	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	1
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PTS[15:0]															
nitial :	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	1
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PTS[31:0]	H'FFC1_FE81	R/W	Sets the packet type (short or long packet) of each data type. It is a set prohibition to the bit 8 excluding 0. Bit 0 corresponds to the data type 00 0000 and bit 31 to 01 1111. Please set this bit only by initialization. 0: The corresponding data type is short packet. 1: The corresponding data type is long packet.

42.3.5. Transmission Packet Type Setting Register 1 (PTYPSET1)

It is a register that sets the packet type (long packet / short packet) of each Data Type (from 10 0000 to 11 1111) of the transmission packet.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PTS[31:16]															
nitial :	1	1	1	1	1	1	1	1	0	1	1	1	1	0	0	1
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

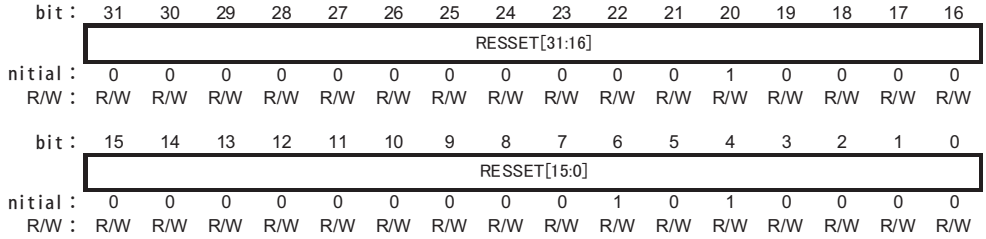
bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PTS[15:0]															
nitial :	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	1
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

.

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PTS[31:0]	H'FF79_FFE1	R/W	Sets the packet type (short or long packet) of each data type. Bit 0 corresponds to the data type 10 0000 and bit 31 to 11 1111. Please set this bit only by initialization. 0: The corresponding data type is short packet. 1: The corresponding data type is long packet.

42.3.6. Response Request Setting Register 0 (RESREQSET0)

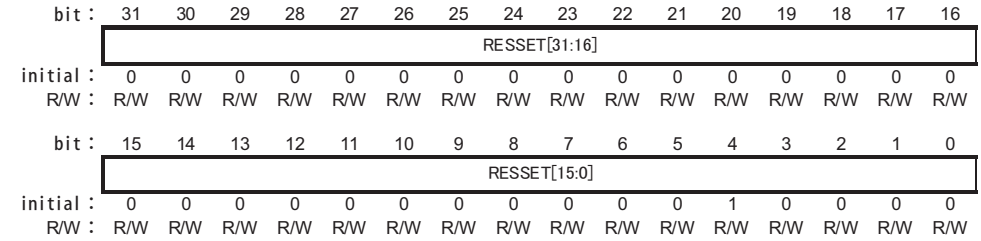
It is a register that sets the response demand of the packet of Data Type(from 00 0000 to 01 1111).



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	RESSET[31:0]	H'0010_0050	R/W	Specifies whether or not packets of the specified data type request response. Bit 0 corresponds to the data type 00 0000 and bit 31 to 01 1111. Please set this bit only by initialization. 0: The packet with corresponding data type does not request a response. 1: The packet with corresponding data type requests a response.

42.3.7. Response Request Setting Register 1 (RESREQSET1)

It is a register that sets the response demand of the packet of Data Type(from 10 0000 to 11 1111).



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	RESSET[31:0]	H'0000_0010	R/W	Specifies whether or not packets of the specified data type request response. Bit 0 corresponds to the data type 10 0000 and bit 31 to 11 1111. Please set this bit only by initialization. 0: The packet with corresponding data type does not request a response. 1: The packet with corresponding data type requests a response.

42.3.8. HS Transmission Time-out Setting Register (HSTTOVSET)

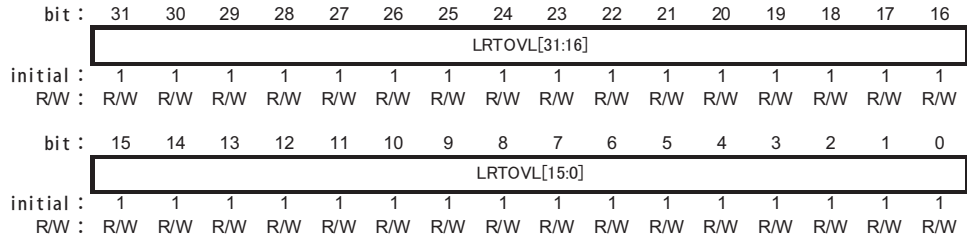
It is a register that sets the HS transmission time-out value.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	HTTOVL[31:16]															
initial :	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HTTOVL[15:0]															
initial :	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	HTTOVL[31:0]	All 1	R/W	Sets the HS transmit timeout value. This value multiplied by the HS byte clock period is used as the HS transmit timeout value. From bit31 to bit8 are recordable. From bit7 to bit0 are 1 fixed. Therefore, the minimum value that can be set becomes 255(h'FF).

42.3.9. LP Reception Time-out Setting Register (LPRTOVSET)

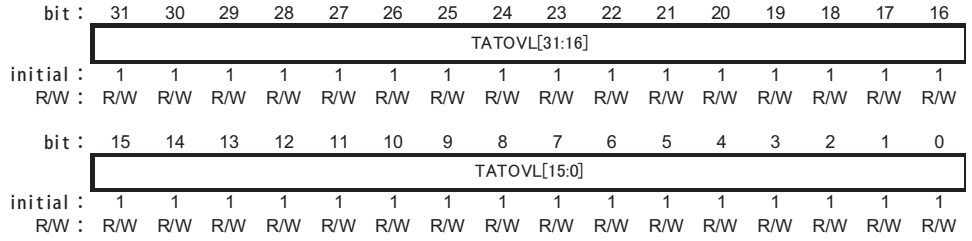
It is a register that sets the LP reception time-out value.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	LRTOVL[31:0]	All 1	R/W	Sets the LP reception timeout value. This value * LP clock period * 4 is used as the LP reception timeout value. Please set this bit only by initialization.

42.3.10. Turn Around Time-out Value Setting Register (TATOVSET)

It is a register that sets the turnaround time out value.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	TATOVL[31:0]	All 1	R/W	Sets the turn around timeout value. This value * LP clock period * 4 is used as the turn around timeout value. Please set this bit only by initialization.

42.3.11. Peripheral Reset Time-out Value Setting Register (PRTOVSET)

It is a register that sets the peripheral reset time-out value.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PRTOVL[31:16]															
initial :	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PRTOVL[15:0]															
initial :	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PRTOVL[31:0]	All 1	R/W	Sets the peripheral reset timeout value. This value multiplied by the LP PHY clock period is used as the turn around timeout value. Please set this bit only by initialization.

42.3.12. DSI-LINK Control Register (DSICTRL)

It is a set register to control the Link block.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	PRTOS RQ	TATOE N	LPRTO EN	HSTTO EN	—	HTTOR C	—	RSTRR Q	—	ULENR Q	—	CLHER Q
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R/W	R/W	R/W	R/W	R	R/W	R	R/W	R	R/W	R	R/W

Bit	Bit Name	Initial Value	R/W	Description

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	−	All 0	R	Reserved
11	PRTOSRQ	0	R/W	Requests to start counting of the peripheral reset timeout timer. Only 1 can be written. When this bit is 1, the start of counting is being requested, and no write access to it is allowed.
10	TATOEN	0	R/W	TA timeout timer count enable. This bit should be set only during initial setting. Please set it after setting TATOVSET.TATOVL. 0: Disables TA timeout timer counting (initial value). 1: Enables TA timeout timer counting.
9	LPRTOEN	0	R/W	LP reception timeout timer count enable. This bit should be set only during initial setting. Please set it after setting LPRTOVSET.LRTOVL. 0: Disables LP reception timeout timer counting (initial value). 1: Enables LP reception timeout timer counting.
8	HSTTOEN	0	R/W	HS transmission timeout timer count enable. This bit should be set only during initial setting. Please set it after setting HSTTOVSET.HTTOVL. 0: Disables HS transmission timeout timer counting (initial value). 1: Enables HS transmission timeout timer counting.
7	-	0	R	Reserved
6	HTTORC	0	R/W	When a HS transmit timeout occurs, the HS byte clock block is reset. Use this bit to clear the reset. Only 1 can be written. When this bit is 1, no write access is allowed. 1 is writable only that DSIINT.HSTXTOINTS=1 or DSIS.HTTORS=1. 0: Writing 1 access enabled 1: Clears the HS transmission timeout reset (writing 1 access disabled)
5	-	0	R	Reserved

Bit	Bit Name	Initial Value	R/W	Description
4	RSTRRQ	0	R/W	Requests a reset trigger transmission. Only 1 can be written. When this bit is 1, no write access is allowed. 0: Writing 1 access enabled 1: Reset trigger transmission requested (writing 1 access disabled)
3	-	0	R	Reserved
2	ULENRQ	0	R/W	Requests a transition to and from ULPS. Writing 1 requests a transition to ULPS and writing 0 requests a transition from ULPS. 0: Transmission request from ULPS 1: Transmission request to ULPS
1	-	0	R	Reserved
0	CLHERQ	0	R/W	Requests the clock lanes transmission to HS mode. Writing 1 requests a transition to HS mode and writing 0 requests a transition from HS mode. 1 is writable only at DSIS.CLHENS=0. 0 is writable only at DSIS.CLHENS=1 0: Clock lane transmission from HS mode requested 1: Clock lane transmission to HS mode requested

42.3.13. Reception packet type setting register0 (RPTYPESET0)

It is a register that sets each packet type (long packet / short packet).
of each Data Type (from 00 0000 to 01 1111) of the reception packet.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RPTS[31:16]															
initial :	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RPTS[15:0]															
initial :	1	1	1	1	1	1	1	0	1	1	1	1	1	0	1	1
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	RPTS[31:0]	H'FFF9_FEFB	R/W	The packet type (long packet / short packet) of each Data Type of the reception packet set. It is a set prohibition to the eighth bit excluding 0. The 0th bit corresponds in Data Type 000000 and the 31st bit corresponds to 011111. Please set this bit only by initialization. 0: Corresponding Data Type is a short packet. 1: Corresponding Data Type is a long packet.

42.3.14. Reception packet type setting register1 (RPTYPESET1)

It is a register that sets each packet type (long packet / short packet).
of each Data Type (from 10 0000 to 11 1111) of the reception packet.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RPTS[31:16]															
initial :	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RPTS[15:0]															
initial :	1	1	1	1	1	1	1	0	1	1	1	1	1	0	0	1
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	RPTS[31:0]	H'FFFF_FEF9	R/W	The packet type (long packet / short packet) of each Data Type of the reception packet set. The 0th bit corresponds in Data Type 100000 and the 31st bit corresponds to 111111. Please set this bit only by initialization. 0: Corresponding Data Type is a short packet. 1: Corresponding Data Type is a long packet.

42.3.15. DSI-LINK Status Register (DSIS)

It is a status register of the Link block.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	TXMODE	HTTORS	STOPS	—	—	ULPSNS	—	CLHENS
initial :	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	-	All 0	R	Reserved
7	TRMODE	0	R	Indicates whether the direction of lane 0 is Tx or Rx. 0: Lane 0 is set as Tx (initial value). 1: Lane 0 is set as Rx.
6	HTTORS	0	R	Indicates the status of the reset caused by a HS transmit timeout. 0: The HS transmit timeout reset is being cleared (initial value). 1: The HS transmit timeout reset is in progress.
5	STOPS	1	R	Indicates that the valid lanes have transitioned to Stop State (LP-11). 0: The valid lanes are not in Stop State. 1: The valid lanes are in Stop State (initial value).
4 , 3	-	00	R	Reserved
2	ULPSENS	0	R	Indicates that both clock and data lanes have transitioned to ULPS. 0: Neither of clock and data lanes are not in the ULPS state or either of the data or clock lanes are not in the ULPS state (initial value). 1: Both clock and data lanes have transitioned to the ULPS state.
1	-	0	R	Reserved
0	CLHENS	0	R	Indicates that clock lanes have transitioned to HS mode. This status bit should be referenced only when the CLSTPM bit in the SYSCONF register is 1. 0: Clock lanes have not transitioned to HS mode (initial value). 1: Clock lanes have transitioned to HS mode.

42.3.16. DSI-LINK Interrupt Status Register (DSIINT)

It is a status register of the Link block. OR of each bit of this register is assumed to be an interrupt signal. It is allocated in DSITX1 as an interrupt factor in INTC.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	DPHYC INTS	ULPSC INTS	RSTTR INTS	RSHOR TINTS	CRCCE RINTS	ECCME RINTS	ECCSE RINTS	ULPT1INT	LDSYE RINTS	PLCTE RINTS	EMENE RINTS
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	HCOTE ERINT	LCOTE ERINT	TATOT NTS	TATOT NTS	LPRXT OINTS	HSTXT OINTS	—	—	—	—	ULPSE XINTS	ULPSE NINTS	CLHEX INTS	CLHEN INTS
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description

Bit	Bit Name	Initial Value	R/W	Description
31 to 27	-	All 0	R	Reserved
26	DPHYCINTS	0	R/W	Indicates that the D-PHY defined code of any of the command pattern "10011111" (Undefine-1), "11011110" (Undefine-2), or "10100000" (Unknown-5) has been received. To clear this bit, write 0 to it. 0: The D-PHY defined code has not been received (initial value). 1: The D-PHY defined code has been received.
25	ULPSCINTS	0	R/W	Indicates that a command of the command pattern "00011110" (ULPS) has been received. To clear this bit, write 0 to it. 0: ULPS command has not been received (initial value). 1: ULPS command has been received.
24	RSTTRINTS	0	R/W	Indicates that a trigger of the command pattern "01100010" (Reset) has been received. To clear this bit, write 0 to it. 0: Reset trigger has not been received (initial value). 1: Reset trigger has been received.
23	RSHORTINTS	0	R/W	It is shown to have received LP11 of the reception end without receiving the reception packet to the last minute. To clear this bit, write 0 to it. 0: Reception packet byte shortage error has not been detected.(initial value) 1: Reception packet byte shortage error is detected.
22	CRCCERINTS	0	R/W	Indicates that a CRC error has been detected in the receive packet. To clear this bit, write 0 to it. 0: CRC error has not been detected (initial value). 1: CRC error has been detected.
21	ECCMERINTS	0	R/W	Indicates that ECC multi-bit error has been detected in the receive packet. To clear this bit, write 0 to it. 0: ECC multi-bit error has not been detected (initial value).

Bit	Bit Name	Initial Value	R/W	Description
				1: ECC multi-bit error has been detected.
20	ECCSERINTS	0	R/W	Indicates that a single-bit ECC error has been detected in the receive packet. To clear this bit, write 0 to it. 0: Single-bit ECC error has not been detected (initial value). 1:Single-bit ECC error has been detected.
19	UELP11INTS	0	R/W	Indicates that unexpected LP11 has been detected during reception. To clear this bit, write 0 to it. 0: Unexpected LP11 has not been detected (initial value). 1: Unexpected LP11 has been detected.
18	LDSYERINTS	0	R/W	Indicates that a protocol error (LPDT sync error) has been detected in the receive packet. To clear this bit, write 0 to it. 0: LPDT sync error has not been detected (initial value). 1: LPDT sync error has been detected.
17	FLCTERINTS	0	R/W	Indicates that a protocol error (false control error) has been detected in the receive packet. To clear this bit, write 0 to it. 0: False control error has not been detected (initial value). 1: False control error has been detected.
16	EMENERINTS	0	R/W	Indicates that a protocol error (escape mode entry error) has been detected in the receive packet. To clear this bit, write 0 to it. 0: Escape mode entry error has not been detected (initial value). 1: Escape mode entry error has been detected.
15, 14	-	00	R	Reseved
13	HCOTEERRINTS	0	R/W	Indicates that a LP High fault contention error has been detected. To clear this bit, write 0 to it. 0: LP High fault contention error has not been detected (initial value). 1:LP High fault contention error has been detected.

Bit	Bit Name	Initial Value	R/W	Description
12	LCOTEERRINTS	0	R/W	Indicates that a LP Low fault contention error has been detected. To clear this bit, write 0 to it. 0: LP Low fault contention error has not been detected (initial value). 1:LP Low fault contention error has been detected.
11	PRTOINTS	0	R/W	Indicates that a peripheral reset timer timeout has been detected. To clear this bit, write 0 to it. 0: Peripheral reset timer timeout has not been detected (initial value). 1: Peripheral reset timer timeout has been detected.
10	TATOINTS	0	R/W	Indicates that a turn around timeout has been detected. To clear this bit, write 0 to it. 0: Turn around timeout has not been detected (initial value). 1: Turn around timeout has been detected.
9	LPRXTOINTS	0	R/W	Indicates that a LP reception timeout has been detected. To clear this bit, write 0 to it. 0: LP reception timeout has not been detected (initial value). 1: LP reception timeout has been detected.
8	HSTXTOINTS	0	R/W	Indicates that a HS transmission timeout has been detected. To clear this bit, write 0 to it. 0: HS transmission timeout has not been detected (initial value). 1: HS transmission timeout has been detected.
7 to 4	-	0000	R	Reserved
3	ULPSEXINTS	0	R/W	Indicates that both clock and data lanes are detected to have transitioned from ULPS. To clear this bit, write 0 to it. 0: Both clock and data lanes are not detected to have transitioned from ULPS or either of them is not detected to have transitioned from ULPS. 1: Both clock and data lanes are detected to have transitioned from ULPS.
2	ULPSENINTS	0	R/W	Indicates that both clock and data lanes are detected to have transitioned to ULPS. To clear

Bit	Bit Name	Initial Value	R/W	Description
				this bit, write 0 to it. 0: Both clock and data lanes are not detected to have transitioned to ULPS or either of them is not detected to have transitioned to ULPS. 1: Both clock and data lanes are detected to have transitioned to ULPS.
1	CLHSEXINTS	0	R/W	Indicates that clock lanes are detected to have transitioned from HS mode. Refer this status bit only when SYSCONF.CLSTPM = 1. To clear this bit, write 0 to it. 0: Clock lanes are not detected to have transitioned from HS mode (initial value). 1: Clock lanes are detected to have transitioned from HS mode.
0	CLHSENINTS	0	R/W	Indicates that clock lanes are detected to have transitioned to HS mode. Refer this status bit only when SYSCONF.CLSTPM = 1. To clear this bit, write 0 to it. 0: Clock lanes are not detected to have transitioned to HS mode (initial value). 1: Clock lanes are detected to have transitioned to HS mode.

42.3.17. DSI-LINK Interrupt Enable Register (DSIINTE)

It is a register that sets an enable interruption of each bit of the DSIINT register.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	DPHYC INTEN	ULPSC INTEN	RSTTR INTEN	RSHOR TINTE	CRCCE RINTE	ECCME RINTE	ECCSE RINTE	ULPT1 INTE	LDSTE RINTE	FLCTE RINTE	EMENE RINTE
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	HCOTE ERINT	LCOTE ERINT	PRTOT NTEN	TATOT NTEN	LPRXT OINTE	HSTXT OINTE	—	—	—	—	ULPSE XINTE	ULPSE NINTE	CLHEX INTEN	CLHEN INTEN
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description

Bit	Bit Name	Initial Value	R/W	Description
31 to 27	-	ALL 0	R	Reserved
26	DPHYCINTEN	0	R/W	Enables the D-PHY defined code reception interrupt. 0: D-PHY standard code reception interrupt disabled (initial value) 1: D-PHY standard code reception interrupt enabled
25	ULPSCINTEN	0	R/W	Enables the ULPS command reception interrupt. 0: ULPS command reception interrupt disabled (initial value) 1: ULPS command reception interrupt enabled
24	RSTTRINTEN	0	R/W	Enables the reset trigger reception interrupt. 0: Reset trigger reception interrupt disabled (initial value) 1: Reset trigger reception interrupt enabled
23	RSHORTINTEN	0	R/W	Reception byte shortage error reception interrupt is done enable. 0: Reception byte shortage error reception interrupt is disabled (initial value). 1: Reception byte shortage error reception interrupt is enable.
22	CRCCERINTEN	0	R/W	Enables the CRC error reception interrupt. 0: CRC error reception interrupt disabled (initial value) 1:CRC error reception interrupt enabled
21	ECCMERINTEN	0	R/W	Enables the ECC multi-bit error reception interrupt. 0: ECC multi-bit error reception interrupt disabled (initial value) 1: ECC multi bit error reception interrupt enabled
20	ECCSERINTEN	0	R/W	Enables the ECC single-bit reception interrupt. 0: ECC single-bit error reception interrupt disabled (initial value)

Bit	Bit Name	Initial Value	R/W	Description
				1: ECC single bit error reception interrupt enabled
19	UELP11INTEN	0	R/W	Enables the Unexpected LP11 reception interrupt 0: Unexpected LP11 reception interrupt disabled (initial value) 1: Unexpected LP11 reception interrupt enabled
18	LDSYERINTEN	0	R/W	Enables the LPDT sync error interrupt 0: LPDT sync error interrupt disabled (initial value) 1: LPDT sync error interrupt enabled
17	FLCTERINTEN	0	R/W	Enables the `false` control error interrupt 0: false control error interrupt disabled (initial value) 1: false control error interrupt enabled
16	EMENERINTEN	0	R/W	Enables the escape mode entry error interrupt 0: Escape mode entry error interrupt disabled (initial value) 1: escape mode entry error interrupt enabled
15, 14	-	00	R	Reserved
13	HCOTEERINTEN	0	R/W	Enables the LP high fault contention error interrupt 0: LP high fault contention error interrupt disabled (initial value) 1: LP high fault contention error interrupt enabled
12	LCOTEERINTEN	0	R/W	Enables the LP low fault contention error interrupt 0: LP low fault contention error interrupt disabled (initial value) 1: LP low fault contention error interrupt enabled
11	PRTOINTEN	0	R/W	Enables the peripheral reset timeout interrupt 0: Peripheral reset timeout interrupt

Bit	Bit Name	Initial Value	R/W	Description
				disabled (initial value) 1: Peripheral reset timeout interrupt enabled
10	TATOINTEN	0	R/W	Enables the turn around timeout interrupt 0: Turn around timeout interrupt disabled (initial value) 1: Turn around timeout interrupt enabled
9	LPRXTOINTEN	0	R/W	Enables the LP reception timeout interrupt 0: LP reception timeout interrupt disabled (initial value) 1:LP reception timeout interrupt enabled
8	HSTXTOINTEN	0	R/W	Enables the HS transmission timeout interrupt 0: HS transmission timeout interrupt disabled (initial value) 1: HS transmission timeout interrupt enabled
7 to 4	-	0000	R	Reserved
3	ULPSEXINTEN	0	R/W	Enables the ULPS exit interrupt 0: ULPS exit interrupt disabled (initial value) 1:ULPS exit interrupt enabled
2	ULPSENINTEN	0	R/W	Enables the ULPS entry interrupt 0: ULPS entry interrupt disabled (initial value) 1: ULPS entry interrupt enabled
1	CLHSEXINTEN	0	R/W	Enables the clock lane HS exit interrupt 0: Clock lane HS exit interrupt disabled (initial value) 1: Clock lane HS exit interrupt enabled
0	CLHSENINTEN	0	R/W	Enables the clock lane HS entry interrupt 0: Clock lane HS entry interrupt disabled (initial value) 1: clock lane HS entry interrupt enabled

42.3.18. PHY Control Register (PHYCTRL)

It is a set register that controls D-PHY.
First of all, bit0:BIPDWN is set.
Please open the period afterwards more than after 100us, and set other bits.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	CLKPDWN	PSRST	—	—	—	—	—	PLLRST	PLLPDWN	PLLBYPS
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	PLLDS[3:0]				–	–	–	–	–	–	–	BIPDWN
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description

Bit	Bit Name	Initial Value	R/W	Description
31 to 26	-	ALL 0	R	Reserved
25	CKPDWN	0	R/W	Puts the clock lane into the power-down state. This bit is not reset by software reset, and maintained. 0: Clock lane is reset (initial value) 1: Clock lane reset is canceled
24	PSRST	0	R/W	Resets the parallel/serial circuit. This bit is not reset by software reset, and maintained. 0: Parallel/serial circuit is reset (initial value). 1: Parallel/serial circuit reset is cleared.
23 to 19	-	ALL 0	R	Reserved
18	PLLRST	0	R/W	Resets the PLL. This bit is not reset by software reset, and maintained. 0: PLL is reset (initial value) 1: PLL reset is cleared.
17	PLLPDWN	0	R/W	Puts the PLL into the power-down state. This bit is not reset by software reset, and maintained. Please set “1” to this bit when you transmit HS. 0: PLL is in the power down state (initial value) 1: PLL Is power on
16	PLLBYPS	0	R/W	On/off in the bypass circuit of PLL is set. 0: The reference clock is output. (initial value) 1: Multiplication clock is output
15 to 12	-	0000	R	Reserved
11 to 8	PLLDS[3:0]	0000	R/W	Set the PLL multiplication ratio(The setting of less than six is prohibited.) This bit is not reset by software reset, and maintained. From 13 Multiplication to 31 Multiplication(Only the odd number) setting is possible. It becomes like the following expressions. Multiplication = 2 * PLLDS[3:0] + 1
7 to 1	-	ALL 0	R	Reserved
0	BIPDWN	0	R/W	Puts the bias circuit in the DSI-Tx block into the power-down state. 0: Bias circuit in the DSI-Tx block is in the power-down

Bit	Bit Name	Initial Value	R/W	Description
				state.
				1: Bias circuit in the DSI-Tx block is power-on.

42.3.19. DSI-L-Bridge Control Register (DTCTR)

It is a control register of L-Bridge block.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	STRST	–	MTEN	FLEN	VMEN
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved
4	STRST	0	R/W	The transmission control state machine is reset when setting it to 1. Please write 0 to release the reset state.
3	—	0	R	Reserved
2	MTEN	0	R/W	Enables the all packets transmission function. Please set 1 when you transmit the command. 0: Transmission disabled 1:Transmission enabled
1	FLEN	0	R/W	Specifies whether or not to transit to LPS every time HS packet transmission is completed. 0: Not to transit to LPS every at HS packet transmission completion. 1: Transit to LPS every at HS transmission completion.
0	VMEN	0	R/W	Enables video_mode. 0: Data input via LCDC prohibited. This enables the consecutive command transmission. 1: Data input via LCDC enable. This prohibits the consecutive command transmission.

42.3.20. DSI-L-Bridge Status Register (DTST)

It is an interrupt status register of L-Bridge.

OR of each bit of this register is assumed to be an interrupt signal. It is allocated in DSITX0 as an interrupt factor in INTC.

[31]DBSY and [15:8]HSCD are the monitor signals of the debugging usage, and interrupt cannot be generated.

When [28]CTPE and [23:20]DTE * are 1, the completion of the L-bridge block is shown.

In addition, after [28]CTPE and [23:20]DTE * is becoming 1, completion in the LINK block requires the next cycle number (HS byte clock conversion).

1lane output:27cycles 2lane output:15cycles

3lane output:11cycles 4lane output:10cycles

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DBSY	–	–	CTPE	–	–	–	–	DTE0	DTE1	DTE2	DTE3	FHEX	LPTAK	LPAK	FDEX
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HSCD[7:0]								HFOV	LFOV	ERPT	IRVE	–	–	–	–
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description

Bit	Bit Name	Initial Value	R/W	Description
31	DBSY	0	R	It becomes 1 while DSITX's being transmitting data or receiving it.
30 to 29	—	00	R	Reserved
28	CTPE	0	R	This bit is set to 1 when command transmission of one packet is completed. It becomes active only at DTCTR.VMEN=0. Please write 1 in DTSTCL. CTPEC to return this bit to 0 from 1
27 to 24	—	0000	R	Reserved
23	DTE0	0	R	This bit is set to 1 when all packets for Long packet transmission [CH0] have been transmitted. It becomes active only at CMTLNGCTR0.TXSEL=1 and DTCTR.VMEN=0. Please write 1 in DTSTCL. DTE0C to return this bit to 0 from 1.
22	DTE1	0	R	This bit is set to 1 when all packets for Long packet transmission [CH1] have been transmitted. It becomes active only at CMTLNGCTR0.TXSEL=1 and DTCTR.VMEN=0. Please write 1 in DTSTCL. DTE1C to return this bit to 0 from 1.
21	DTE2	0	R	This bit is set to 1 when all packets for Long packet transmission [CH2] have been transmitted. It becomes active only at CMTLNGCTR0.TXSEL=1 and DTCTR.VMEN=0. Please write 1 in DTSTCL. DTE2C to return this bit to 0 from 1.
20	DTE3	0	R	This bit is set to 1 when all packets for Long packet transmission [CH3] have been transmitted. It becomes active only at CMTLNGCTR0.TXSEL=1 and DTCTR.VMEN=0. Please write 1 in DTSTCL. DTE3C to return this bit to 0 from 1.
19	FHEX	0	R	This bit is set to 1 when there is data in the header information FIFO for command reception (LP). Please write 1 in DTSTCL. FHEXC to return this bit to 0 from 1.

Bit	Bit Name	Initial Value	R/W	Description
18	LPTAK	0	R	This bit is set to 1 when a tearing effect trigger is received. Please write 1 in DTSTCL. LPTAKC to return this bit to 0 from 1.
17	LPAK	0	R	This bit is set to 1 when the Acknowledge is received. Please write 1 in DTSTCL. LPAKC to return this bit to 0 from 1.
16	FDEX	0	R	This bit is set to 1 when there is data in the data FIFO for command reception (LP). Please write 1 in DTSTCL. FDEXC to return this bit to 0 from 1.
15 to 8	HSCD[7:0]	0	R	It is a value of { VCID[1:0] ,DataType [5:0]} when HS output from L-Bridge is transmitted.
7	HFOV	0	R	HS transmission data count mismatch error Please write 1 in DTSTCL. HFOVC to return this bit to 0 from 1
6	LFOV	0	R	LP transmission data count mismatch error Please write one in DTSTCL. LFOVC to return this bit to 0 from one.
5	ERPT	0	R	Acknowledge with Error Report is received at command reception (LP). Please write one in DTSTCL. ERPTC to return this bit to 0 from one.
4	IRVE	0	R	Video mode command transmission error (error of interleave function) Please write one in DTSTCL. IRVEC to return this bit to 0 from one.
3 to 0	—	0000	R	Reserved

42.3.21. DSI−L−Bridge Status Clear Register (DTSTCL)

It is a register that clears the interrupt status of the DTST register.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	CTPEC	–	–	–	–	DTE0C	DTE1C	DTE2C	DTE3C	FHEXC	LPTAKC	LPAKC	FDEXC
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	HFOVC	LFOVC	ERPTC	IRVEC	–	–	–	–
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R/W	R/W	R	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	000	R	Reserved
28	CTPEC	0	R/W	DTST.CTPE is cleared when written to 1. After one cycle, it becomes 0.
27 to 24	—	0000	R	Reserved
23	DTE0C	0	R/W	DTST.DTE0 is cleared when written to 1. After one cycle, it becomes 0.
22	DTE1C	0	R/W	DTST.DTE1 is cleared when written to 1. After one cycle, it becomes 0.
21	DTE2C	0	R/W	DTST.DTE2 is cleared when written to 1. After one cycle, it becomes 0.
20	DTE3C	0	R/W	DTST.DTE3 is cleared when written to 1. After one cycle, it becomes 0.
19	FHEXC	0	R/W	DTST.FHEX is cleared when written to 1. After one cycle, it becomes 0.
18	LPTAKC	0	R/W	DTST.LPTAK is cleared when written to 1. After one cycle, it becomes 0.
17	LPAKC	0	R/W	DTST.LPAK is cleared when written to 1. After one cycle, it becomes 0.
16	FDEXC	0	R/W	DTST.FDEX is cleared when written to 1. After one cycle, it becomes 0.
15 to 8	—	ALL 0	R	Reserved
7	HFOVC	0	R/W	DTST.HFOV is cleared when written to 1. 0 is always read.
6	LFOVC	0	R/W	DTST.LFOV is cleared when written to 1. After one cycle, it becomes 0.
5	ERPTC	0	R/W	DTST.ERPT is cleared when written to 1. After one cycle, it becomes 0.
4	IRVEC	0	R/W	DTST.IRVE is cleared when written to 1. After one cycle, it becomes 0.
3 to 0	—	0000	R	Reserved

42.3.22. DSI-L-Bridge Interrupt Enable Register (DTIRQEN)

It is an interrupt enable register of the DTST register.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	CTPEIE	–	–	–	–	DTE0IE	DTE1IE	DTE2IE	DTE3IE	FHEXIE	LPTAKIE	LPAKIE	FDEXIE
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	HFOVIE	LFOVIE	ERPTIE	IRVEIE	–	–	–	–
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R/W	R/W	R	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	000	R	Reserved
28	CTPEIE	0	R/W	Asserts an interrupt when the condition DTST.CTPE= 1 is satisfied. 0: Interrupt disabled 1: Interrupt enabled
27 to 24	—	0000	R	Reserved
23	DTE0IE	0	R/W	Asserts an interrupt when the condition DTST.DTE0= 1 is satisfied. 0: Interrupt disabled 1: Interrupt enabled
22	DTE1IE	0	R/W	Asserts an interrupt when the condition DTST.DTE1= 1 is satisfied. 0: Interrupt disabled 1: Interrupt enabled
21	DTE2IE	0	R/W	Asserts an interrupt when the condition DTST.DTE2= 1 is satisfied. 0: Interrupt disabled 1: Interrupt enabled
20	DTE3IE	0	R/W	Asserts an interrupt when the condition DTST.DTE3= 1 is satisfied. 0: Interrupt disabled 1: Interrupt enabled
19	FHEXIE	0	R/W	Asserts an interrupt when the condition DTST.FHEX = 1 is satisfied. 0: Interrupt disabled 1: Interrupt enabled
18	LPTAKIE	0	R/W	Asserts an interrupt when the condition DTST.LPTAK = 1 is satisfied. 0: Interrupt disabled 1: Interrupt enabled
17	LPAKIE	0	R/W	Asserts an interrupt when the condition DTST.LPAK = 1 is satisfied. 0: Interrupt disabled 1: Interrupt enabled
16	FDEXIE	0	R/W	Asserts an interrupt when the condition

Bit	Bit Name	Initial Value	R/W	Description
				DTST.FDEX = 1 is satisfied. 0: Interrupt disabled 1: Interrupt enabled
15 to 8	—	ALL 0	R	Reserved
7	HFOVIE	0	R/W	Asserts an interrupt when the condition DTST.HFOV = 1 is satisfied. 0: Interrupt disabled 1: Interrupt enabled
6	LFOVIE	0	R/W	Asserts an interrupt when the condition DTST.LFOV = 1 is satisfied. 0: Interrupt disabled 1: Interrupt enabled
5	ERPTIE	0	R/W	Asserts an interrupt when the condition DTST.ERPT is satisfied. 0: Interrupt disabled 1: Interrupt enabled
4	IRVEIE	0	R/W	Asserts an interrupt when the condition DTST.IRVE = 1 is satisfied. 0: Interrupt disabled 1: Interrupt enabled
3 to 0	—	0000	R	Reserved

42.3.23. Video Mode Control Register 1 (VMCTR1)

This register is used for video mode control. It is mainly used to configure transmission packets.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	FSS	VSYNW[3:0]				BKM
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PCTYPE[3:0]				–	–	–	–	VCID[1:0]		DT[5:0]					
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description

Bit	Bit Name	Initial Value	R/W	Description
31 to 22	—	ALL 0	R	Reserved
21	FSS	0	R/W	Selects the source of the signal from which an Odd/Even field is determined. 0: DSI-Tx 1: LCDC Refer to the descriptions for VMCTR1 for details.
20 to 17	VSYNW[3:0]	0000	R/W	Vertical Sync Signal Width. (unit of line) Please set it when you set VMCTR2.BL1BM=1 and VMCTR2.VSEE=1. Set the same value as in MLDVSYNR.VSYNW[3:0] of LCDC.
16	BKM	0	R/W	LCD Data Reception Clock Selection 0: HS byte clock 1: bck When the HS byte clock is selected, the LCDC dot clock should be set to the HS byte clock. Please set 0 to this bit when as much as one Blanking Packet is selected in VMCTR2[5:0]. note: Please set the clock selection of this bit earlier than DTCTR.VMEN.
15 to 12	PCTYPE[3:0]	0000	R/W	The LCDC supplies RBG888 (24 bits) or YUV422 (16 bits) data. Select the packet format into which this data is converted. Conversion from RGB888: 4'b0000: Not converting (RGB888) 4'b0001: RGB565 4'b0010: RGB666 (loosely packed) 4'b0011: RGB666 4'b1000: BGR888 4'b1001: BGR565 4'b1010: BGR666 (loosely packed) 4'b1011: BGR666 Conversion from YUV422: 4'b0100: YUV422 (Y1, U1, Y2, V1, ……)

Bit	Bit Name	Initial Value	R/W	Description
				4'b0101: YUV422 (U1, Y1, V1, Y2, ……) 4'b0110: YUV420 legacy*[1] 4'b0111: YUV420*[2] Note: *1 U and V uses the data of odd-line and even-line respectively. Note: *2 U and V use the even-line data.
11 to 8	—	0000	R	Reserved
7, 6	VCID[1:0]	00	R/W	Set the virtual channel for the video mode output.
5 to 0	DT[5:0]	ALL 0	R/W	Set the data type for the video mode output.

42.3.24. Video Mode Control Register 2 (VMCTR2)

This register is used for video mode control.

It specifies whether sync event packets are transmitted or HSA or BLLP periods are allowed depending on Non-Burst Mode with Sync Pulses, Non-Burst Mode with Sync Events, or Burst mode.

It also allows or disallows command transmission during the BLLP period.

In addition, it specifies whether to transition to LPS or to hold HS transmission (transmit blanking packets) during the HSA, HBP, HFP, and BLLP periods.

When you set one even by one at 5:0 of this registers, please assume VMCTR1.BKM=0, and give the dot clock to me as HS byte clock.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	VSEE	HSEE	HSAE	–	–	–	BL2E	–
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R/W	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	BL1IEN	BL2IEN	BL3IEN	–	–	HSABM	HBPBM	HFPBM	BL1BM	BL2BM	BL3BM
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	RW	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	ALL 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23	VSEE	0	R/W	Sets the VSE output 0: VSE is not output. 1: VSE is output.
22	HSEE	0	R/W	Sets the HSE output 0: HSE is not output. 1: HSE is output.
21	HSAE	0	R/W	HSA period 0: HSA period is not allowed. 1: HSA period is allowed.
20 to 18	—	000	R	Reserved
17	BL2E	0	R/W	BLLP2 period 0: BLLP2 is not allowed. 1: BLLP2 is allowed.
16 to 11	—	ALL 0	R	Reserved
10	BL1IEN	0	R/W	Command transmission during BLLP1 period 0: Disabled 1: Enabled Note: When set 1 in this bit, the BL1BM bit need to be set to 0.
9	BL2IEN	0	R/W	Command transmission during BLLP2 period 0: Disabled 1: Enabled Note: When set 1 in this bit, the BL2BM bit need to be set to 0.
8	BL3IEN	0	R/W	Command transmission during BLLP3 period 0: Disabled 1: Enabled Note: When set 1 in this bit, the BL3BM bit need to be set

Bit	Bit Name	Initial Value	R/W	Description
				to 0.
7,6	—	00	R	Reserved
5	HSABM	0	R/W	State setting during HSA period. Please usually set 0, and set 1 only when it is not possible to change to LPS. 0: LPS 1: Blanking packet transmission
4	HBPBM	0	R/W	State setting during HBP period. Please usually set 0, and set 1 only when it is not possible to change to LPS. 0: LPS 1: Blanking packet transmission
3	HFPBM	0	R/W	State setting during HFP period. Please usually set 0, and set 1 only when it is not possible to change to LPS. 0: LPS 1: Blanking packet transmission
2	BL1BM	0	R/W	State setting during BLLP1 period. Please usually set 0, and set 1 only when it is not possible to change to LPS. 0: LPS 1: Blanking packet transmission
1	BL2BM	0	R/W	State setting during BLLP2 period. Please usually set 0, and set 1 only when it is not possible to change to LPS. 0: LPS 1: Blanking packet transmission
0	BL3BM	0	R/W	State setting during BLLP3 period. Please usually set 0, and set 1 only when it is not possible to change to LPS. 0: LPS 1: Blanking packet transmission

Lists the settings at the each mode as follows:

- Non-burst mode with sync pulses: VSEE = 1, HSEE = 1, HSAE = 1, BL2E = 0
- Non-burst mode with sync events: VSEE = 0, HSEE = 0, HSAE = 0, BL2E = 0
- Burst mode: VSEE = 0, HSEE = 0, HSAE = 0, BL2E = 1

42.3.25. Video Mode Data Length Register 1 (VMLEN1)

This register is used for video mode control.

The volume of data at image data and HSA period (Blanking) is set.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RGBLEN[15:0]															
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HSALEN[15:0]															
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	RGBLEN[15:0]	H'0001	R/W	Please set volume of data (byte) of the image data of one line. When VMCTR1.PCTYPE[3:0]=4'b0111, please set the volume of data of odd line . At this time, Volume of data of odd line = volume of data of even line / 2.
15 to 0	HSALEN[15:0]	H'0001	R/W	Please set volume of data (byte) of Blanking Packet at the HSA period. It becomes effective only at VMCTR2.HSABM=1.

42.3.26. Video Mode Data Length Register 2 (VMLEN2)

This register is used for video mode control.

The volume of data at HBP period (Blanking) and HFP period (Blanking) is set.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	HBPLEN[15:0]															
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HFPLEN[15:0]															
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	HBPLEN[15:0]	H'0001	R/W	Set volume of data (byte) of Blanking Packet at the HBP period. It becomes effective only at VMCTR2. HBPBM=1.
15 to 0	HFPLEN[15:0]	H'0001	R/W	Set volume of data (byte) of Blanking Packet at the HFP period. It becomes effective only at VMCTR2. HFPBM=1.

42.3.27. Video Mode Data Length Register 3 (VMLEN3)

This register is used for video mode control.
The volume of data at BLLP1 period (Blanking) and BLLP2 period (Blanking) is set.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	BL1LEN[15:0]															
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BL2LEN[15:0]															
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	BL1LEN[15:0]	H'0001	R/W	Set volume of data (byte) of Blanking Packet at the bllp1 period. It becomes effective only at VMCTR2. BL1BM=1.
15 to 0	BL2LEN[15:0]	H'0001	R/W	Set volume of data (byte) of Blanking Packet at the bllp2 period. It becomes effective only at VMCTR2. BL2BM=1.

42.3.28. Video Mode Data Length Register 4 (VMLEN4)

This register is used for video mode control.
The volume of data at BLLP3 period (Blanking) is set.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	BL3LEN[15:0]															
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	BL3LEN[15:0]	H'0001	R/W	Set volume of data (byte) of Blanking Packet at the bllp3 period. It becomes effective only at VMCTR2. BL3BM=1.
15 to 0	—	ALL 0	R	Reserved

42.3.29. Video Mode Short Packet Data Register 1 (VMSDAT1)

This register sets values for the data portion (Data0,Data1) of VsyncStart packets.
The values can be set for states A and B individually.
States A and B can be switched via the FSS bit in the VMCTR1 register.

- When the FSS bit in VMCTR1 register is 0:
  States A and B are switched every time one frame is transmitted.
  This register is initialized to state A when the VMEN bit in the DTCTR register is set to 0.

・When the FSS bit in the VMCTR1 register is 1:
The state depends on the LCDC plane to be used (A or B).

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VSSAD[15:0]															
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VSSBD[15:0]															
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	VSSAD[15:0]	ALL 0	R/W	These bits set the VsyncStart data value in state A.
15 to 0	VSSBD[15:0]	ALL 0	R/W	These bits set the VsyncStart data value in state B.

42.3.30. Video Mode Short Packet Data Register 2 (VMSDAT2)

The data value of VSyncEnd, HSyncStart, and HSyncEnd is set.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VMSRTD[15:0]															
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	ALL 0	R	Reserved
15 to 0	VMSRTD[15:0]	ALL 0	R/W	These bits set the data value for VsyncEnd, HsyncStart, and HsyncEnd.

42.3.31. Command Mode Reception Control Register (CMRCTR)

This register sets the overall LP reception operation.

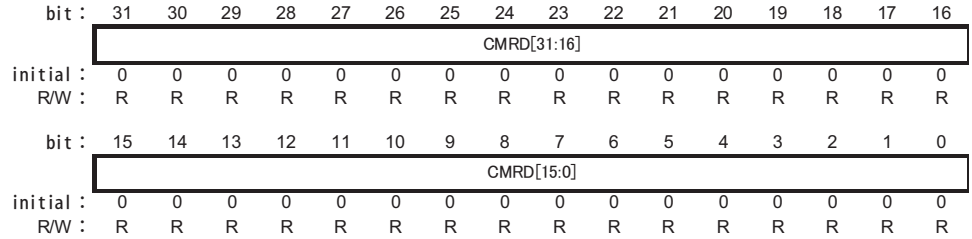
bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	FRST	–	–	–	–	–	CRXEN	DMAEN	FIFOS
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	FHNM[2:0]			FDNM[3:0]			
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	ALL 0	R	Reserved
24	FRST	0	R/W	When 1 setting , Data in reception FIFO for the data and Data in reception FIFO for the header is deleted. Please use it to delete the unnecessary data that has been stored in FIFO when ECC multi-bit error happens. This function cannot be used while receiving data. After 1 cycle with the bus clock , this bit returns to 0 .
23 to 19	—	ALL 0	R	Reserved
18	CRXEN	0	R/W	Reception enable 0: Disables LP reception. Transmitted data is discarded. 1: Enables LP reception.
17	DMAEN	0	R/W	Setting of method of reading data that exists in reception FIFO for data 0: Received data is read by the CPU (software operation). 1: Received data is read by the DMA.
16	FIFOS	0	R/W	Whether PH information is stored in reception FIFO for data is selected. 0: PH information is stored only in reception FIFO for the header. 1: PH information is stored in reception FIFO for the header and reception FIFO for data.
15 to 7	—	0	R	Reserved
6 to 4	FHNM[2:0]	000	R	Indicates the number of data (up to 7) in the receive FIFO for headers. Every time the CPU read CMRHEAD register, this bit value is decremented by 1.
3 to 0	FDNM[3:0]	0000	R	Indicates the number of data (up to 15) in the receive FIFO for datas. Every time the CPU or DMA read CMRDAT register, this bit value is decremented by 1.

42.3.32. Command Mode Reception Data Register (CMRDAT)

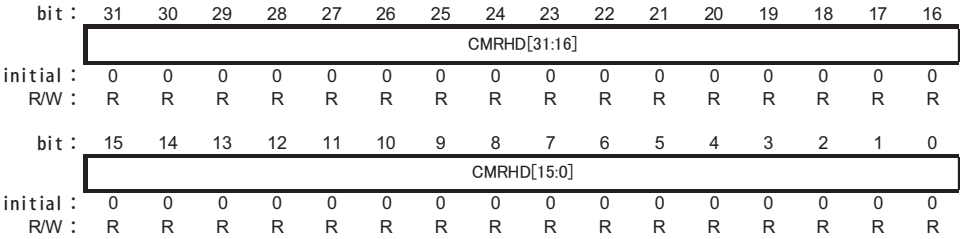
This register indicates the data value received during LP reception.
It has a 15-stage FIFO configuration.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	CMRD[31:0]	ALL 0	R	Show the received data value. When read by the CPU or DMA, the value in the next-stage FIFO is shown in the next cycle.

42.3.33. Command Mode Reception Header Register (CMRHEAD)

This register indicates the PH value received during LP reception.
It has a 7-stage FIFO configuration.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	CMRHD[31:0]	ALL 0	R	Show the received PH(packet header) value. When read by the CPU, the value in the next-stage FIFO is shown in the next cycle.

42.3.34. Tearing Effect Request Register (CMRTEREQ)

The tearing effect request is set.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	TEREQ
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	ALL 0	R	Reserved
0	TEREQ	0	R/W	Requests the tearing effect for a peripheral (LCD panel). After setting 1 , when the clock putting changing into LPCLK is completed, it becomes 0.

42.3.35. Command Mode Transmission Long Packet Request CH0 Register (CMTLNGREQ0)

This is a command packet generation register. It sets the transmission request for CH0.
There are four channels of registers that are related to generating long command packets. All of them have the same function, so only CH0 will be described.

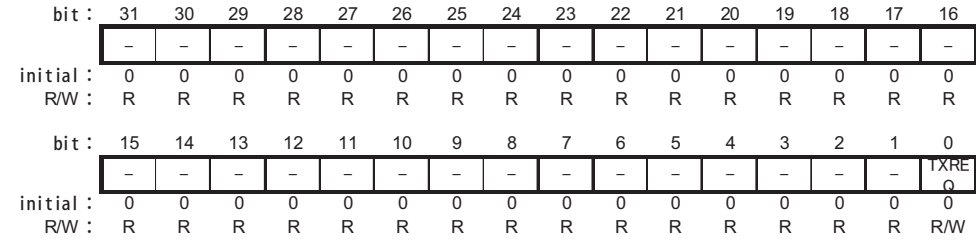
bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	TXWAIT	TXREQ
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	ALL0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	TXWAIT	0	R/W	Transmit stop setting Set TXWAIT to 1 to stop the packet transmission temporarily when TXRERQ is 1. The transmission is stopped after the current packet transmission is completed. When tx_wait is set to 0, the transmission is resumed.
0	TXREQ	0	R/W	Transmission request setting When written to 1, a transmission request is issued and command-packet transmission is started according to the settings of CMTIADR0, CMTITTL0, CMTIADRI0, CMTIRN0, CMTLNGCTR0, and CMTLNGDT0. When all packets are transmitted, this bit changes to 0. Writing 0 to this bit while transmission is in progress (it is 1) cancels the transmission. If there are packets being transmitted, this bit is 0 after the packets are transmitted. If there is no packet being transmitted (packets for other channels are being transmitted), this bit changes to 0 immediately. The values of other registers (CMTIADR0, CMTITTL0, CMTIADRI0, CMTIRN0, CMTLNGCTR0, CMTLNGDT0) related to command-packet transmission must be changed only when this bit is 0. Please go after confirming this bit is 0 when the following command is transmitted.

42.3.36. Command Mode Transmision Short Packet Request Register (CMTSRTREQ)

This register is related to command-packet transmission.
It sets up the transmission request for short packets

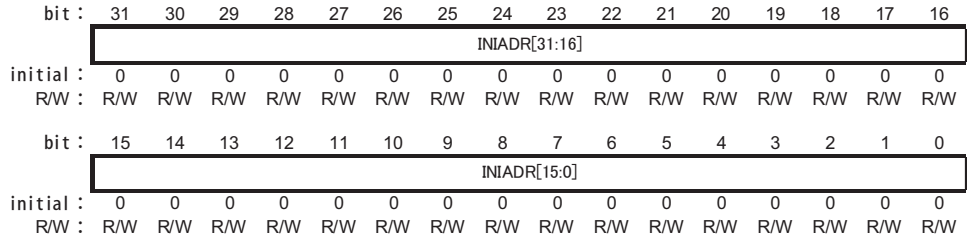


Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	TXREQ	0	R/W	Transmission request setting When 1 is written to this bit, a transmission request is issued and command-packet transmission is started according to the CMTSRTCTR setting. When the packet transmission is completed, this bit changes to 0. Please go after confirming this bit is 0 when the following command is transmitted.

42.3.37. Command Mode Transmission Initiator Address CH0 Register (CMTIADR0)

This is a command packet generation register. It sets the source address of transmit data for CH0.

Only CH0 is described.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	INIADR[31:0]	ALL 0	R/W	Source address setting These bits function as an address register when CMTLNGCTR0. TXSEL is 1.In this case, the lower 3 bits should be fixed to 0. When CMTLNGCTR0. TXSEL is 0, all bits are used because they function as a data storage register.

42.3.38. Command Mode Transmission Initiator Total Data CH0 Register (CMTITTL0)

This is a command packet generation register.
The volume of data of 1 line is set. Only CH0 is described.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	INITTAL[31:16]															
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INITTAL[15:0]															
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	INITTAL[31:0]	ALL 0	R/W	Data amount specification Set the amount of data per line when CMTLNGCTR0.TXSEL is 1. When CMTLNGCTR0.TXSEL is 0, these bits function as a data storage register.

42.3.39. Command Mode Transmission Initiator Address Increment CH0 Register (CMTIADRI0)

This is a command packet generation register.
A stride amount of every 1 line is set. Only CH0 is described.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	INIADRINC[31:16]															
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INIADRINC[15:0]															
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	INIADRINC[31:0]	ALL 0	R/W	Set the stride amount per line when CMTLNGCTR0. TXSEL is 1. When the data for multiple lines is transferred, this register value is added for each line to the address. In this case, the lower 3 bits should be fixed to 0. When CMTLNGCTR0. TXSEL is 0, all bits are used because they function as a data storage register.

42.3.40. Command Mode Transmission Initiator Repeat Number CH0 Register (CMTIRN0)

This is a command packet generation register. It sets the number of lines of transmit data for CH0. Only CH0 is described.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	INIRPTNUM[31:16]															
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INIRPTNUM[15:0]															
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	INIRPTNUM[31:0]	ALL 0	R/W	Line size setting When CMTLNGCTR0. TXSEL is 1, set the number of lines. When data to be transmitted is not image data such as JPEG code, set to 1. When CMTLNGCTR0. TXSEL is 0, these bits function as a data storage register.

42.3.41. Command Mode Transmission Long Packet Control CH0 Register (CMTLNGCTR0)

This is a command packet generation register. This register provides transmission control for CH0. Only CH0 is described.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VCID[1:0]		DT[5:0]						–	–	–	–	LENG[11:8]			
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LENG[7:0]								–	–	–	–	–	–	TXSE	HSSE
initial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R/W	R/W

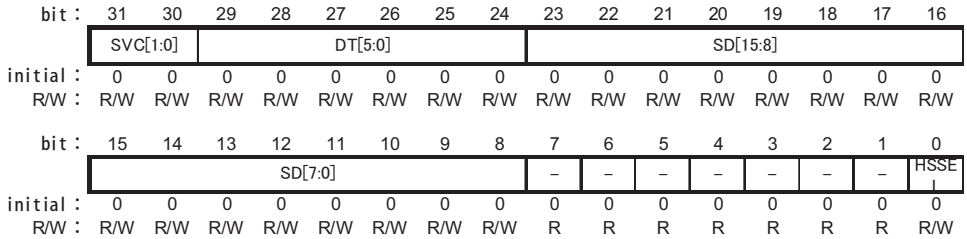
Bit	Bit Name	Initial Value	R/W	Description
31, 30	VCID[1:0]	00	R/W	Set the VC of command-packet.
29 to 24	DT[5:0]	ALL 0	R/W	Set the data type of command-packet.
23 to 20	—	0000	R	Reserved
19 to 8	LENG[11:0]	ALL 0	R/W	Set the payload size of command-packet in these bits. The lower 3 bits should be fixed to 0 when the TXSEL bit is 1. The maximum payload size is 2 Kbytes.*
7 to 2	—	ALL 0	0	Reserved
1	TXSEL	0	R/W	Data select 0: Transmits the data stored in the 4 data registers. 1: Transmits the data read from the memory.
0	HSSEL	0	R/W	Transmission speed select 0: Low power (LP) transmission 1: High speed (HS) transmission

Note:*

If a format conversion is to be performed by setting CMTLNGDT0.RGBCNV and YUVCNV , WordCount of transmit packets is processed. For RGB666, the packet length is 3/4 of the original data. The size is limited to 2 Kbytes before processing.

42.3.42. Command Mode Transmission Short Packet Control Register (CMTSRTCTR)

This register is related to command-packet transmission. It sets up short packet data to be transmitted.



Bit	Bit Name	Initial Value	R/W	Description
31, 30	SVC[1:0]	00	R/W	Set the VC of command-packet.
29 to 24	DT[5:0]	All 0	R/W	Set the data type of command-packet. 0x08 is a set prohibition.
23 to 8	SD[15:0]	All 0	R/W	Set the Data0 and Data1 of short packet.
7 to 1	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	HSSEL	0	R/W	Transmission speed select 0: Low power (LP) transmission 1: High speed (HP) transmission

42.3.43. Command Mode Transmission Long Packet Data Type CH0 Register (CMTLNGDT0)

This is a command packet generation register. It sets up special control for CH0.
Only CH0 is described.

bit :	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	RGBCNV[2:0]			YUVCNV[3:0]				–	COMTLS	COMTWS	COMTBS	–	–	AFSFE	MULDTEN
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R/W	R/W

bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	MDT[5:0]						–	–	FDT[5:0]					
nitial :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	—	0	R	Reserved
30 to 28	RGBCNV[2:0]	000	R/W	Selects the packet format into which RGB data is converted. 3'b000: Not converting (RGB888) 3'b001: RGB565 3'b010: RGB666 (loosely packed) 3'b011: RGB666 3'b100: BGR888 3'b101: BGR565 3'b111: BGR666 For RGB888 and BGR888, the original data must be RGB888 (3 bytes/pixel). For RGB666 (LP), RGB666, and BGR666, the original data must be RGB888 and RGB666 (3 bytes/pixel for both of them). For RGB565 and BGR565, the original data must be RGB565 (2 bytes/pixel).
27 to 24	YUVCNV[3:0]	0000	R/W	When data in the YUV format is transmitted, Y data and UV data stored in separate area can be transmitted by combining them. Bit 3: Combining setting 0: Not be combined 1: Combined Bit2: Source data setting 0: YUV420 1: YUV422 Bit1, 0: Transmission format setting 2'b0: Setting prohibited 2'b01: YUV422 (U1, Y1, V1, Y2) 2'b10: YUV420 (legacy) 2'b11: YUV420 Note: This function uses two channels of command packet generation registers. These include channel the CH0 and CH1 pair and the CH2 and CH3 pair.

Bit	Bit Name	Initial Value	R/W	Description
				Y data is specified by CH0 and CH2. UV data is specified by CH1 and CH3.
23	—	0	R	Reserved
22	COMTLS	0	R/W	When this bit is set to 1, the command data is swapped in longword units.
21	COMTWS	0	R/W	When this bit is set to 1, the command data is swapped in word units.
20	COMTBS	0	R/W	When this bit is set to 1, the command data is swapped in byte units.
19 to 18	—	00	R	Reserved
17	AFSFE	0	R/W	Appends FrameStart and FrameEnd short packets before and after the original transmit data automatically .
16	MULDTEN	0	R/W	Makes DTs for the start, intermediate, and end packets configurable when a group of data is to be divided into packets for transmission. 0: Uses the CMTLNGCTR0.DT[5:0] value as DT regardless of whether it is for the start, intermediate, or end packet. 1: Uses the CMTLNGCTR0.DT[5:0], CMTLNGDT0.MDT[5:0], and CMTLNGDT0.FDT[5:0] values for the start, intermediate, and end packets respectively.
15, 14	—	00	R	Reserved
13 to 8	MDT[5:0]	ALL 0	R/W	These bits specify DT for the intermediate packet.
7, 6	—	00	R	Reserved
5 to 0	FDT[5:0]	ALL 0	R/W	These bits specify DT for the end packet.

42.4 Operating Mode

The L-bridge has two operating modes as internal status: video mode and command mode, which are switched by the VMEN in the DTCTR register.

In the video mode, video-packets (Note 1) take precedence in transmission and transmission of command-packets (Note 2) is restricted.

In the command mode, video-packets cannot be transmitted, but transmission of command-packets is not restricted.

Note1:Packet that is generated by processing the input data from the LCDC in the upper stage in figure 42.1.

Note2:Packet that is generated by processing the data from the register in the lower stage in figure 42.1 or from the external memory

42.4.1. Video Mode

Transmission in the video mode cannot be performed without the cooperation of the LCDC.

Please start in order of DSI-Tx → LCDC.

Please stop in order of DSI-Tx → LCDC.

The start of above-mentioned DSI shows DTCTR.VMEN=1 and the stop of DSI shows DTCTR.VMEN=0.

Figure 42.2 shows the example of the image data output when the number of each lane is set.

(The header and the footer are omitted. Beginning of the output of the data of the LINK block actually requires more cycles number from beginning of the output of the data of the L-bridge block.)

The number of lanes is set by SYSCONF.LANEEN[3:0] register.

The output of the image data of the L-bridge block makes the DISP signal from LCDC a trigger, and outputs the image data from one LCDC of the previous line.

At this time, even if it is the same number of packets, output cycle of image data number is different as shown in Figure 42.2 according to the setting of the number of lanes.

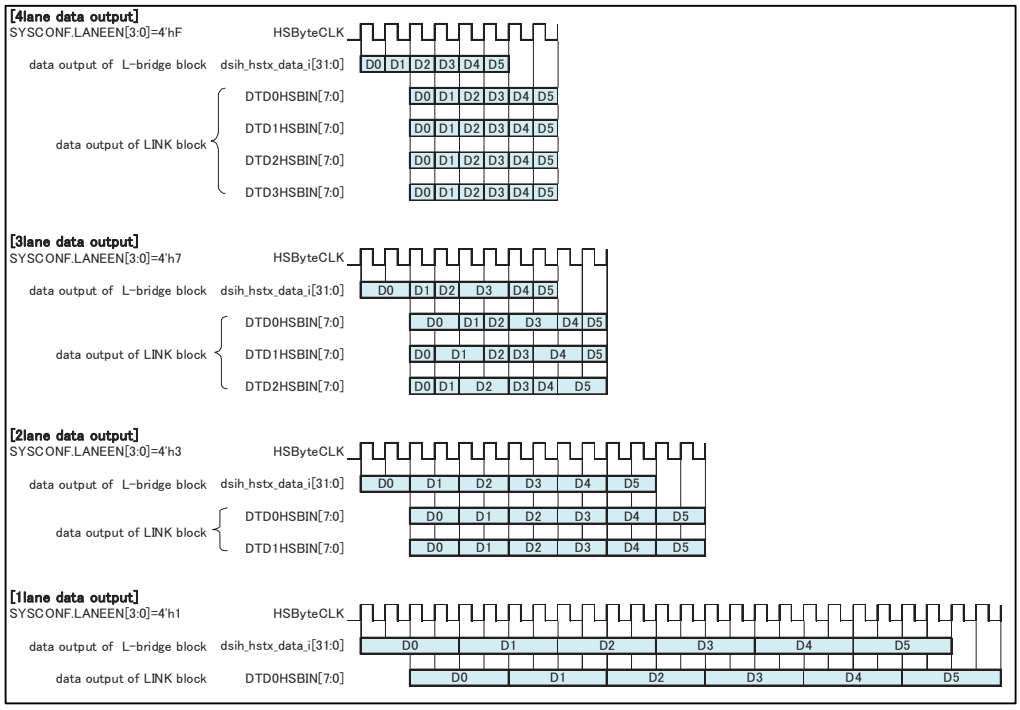


Figure 42.2 Output of data of number of each lane

Please see Figure 42.3.

Before becoming active the following Hsync from LCDC, The image data output, the BLLP2 period, and the HFP period of the L-bridge block must end. Please set LCDC with room enough for that.

It becomes impossible to secure operation because it becomes impossible to output the HSS packet when image data output period + BLLP2 period + HFP period is the following Hsync and comes in succession.

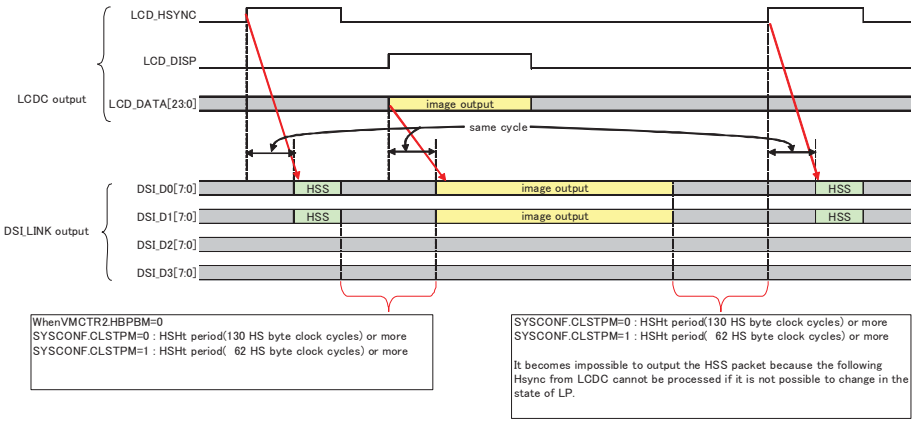


Figure 42.3 Relation between sync signal and output of image

42.4.2. Blanking Packet

It takes a certain time (HSHt) between transitions from HS transmission to LPS to HS transmission.

To transmit HS packets continuously within HSHt in the video mode, the HS transmission state should be maintained by sending a blanking packet because there is not enough time to transition to LPS.

HSHt is 130 HS byte clock cycles (62 cycles if the CLSTPM bit in the SYSCONF register is 1).

The payload of a blanking packet varies depending on the number of lanes and the periods to be inserted (HSA, HBP, HFP, BLLP).

It can be calculated by the following expression:

The following waiting cycle becomes cycle when HS byte clock was converted number for each period of the output signal of LCDC of Figure 42.4.

LPM becomes LP period from the BLLP3 period end to standing up of the following vsync.

Please calculate the waiting cycle from the setting of the register of LCDC value.

If HSA, HBP, BLLP1, and BLLP3 are to be inserted;

Payload(byte) = (Number of lanes × wait cycle) – 10

Figure 42.5 shows the example of calculating the payload length of HSA that uses the above-mentioned type at the BlankingPacket period.

10(byte) subtracted in the above-mentioned type is a value in which HSS(4byte), header (4byte), and footer (2byte) are totaled in Figure 42.5.

If HFP and BLLP2 are to be inserted,

Payload(byte) = (Number of lanes × wait cycle) – 12

Figure 42.6 shows the example of calculating the payload length of HFP that uses the above-mentioned type at the BlankingPacket period.

12(byte) subtracted in the above-mentioned type is a value in which header (4byte) of the image data and CheckSum(2byte) of the image data and header (4byte) of HFP and footer (2byte) of HFP is totaled in Figure 42.6.

Note:

Being able to use the above-mentioned type as it is becomes seeing when RGB888, RGB666(loosely packed), BGR888, and BGR666(loosely packed) are selected as image output format in setting VMCTR1. PCTYPE[3:0].

At other image output format., the length of bit of about one pixel of the image data of the DSI output is smaller than the LCDC output.

So it is necessary to add the volume of data of the difference to the above-mentioned type.

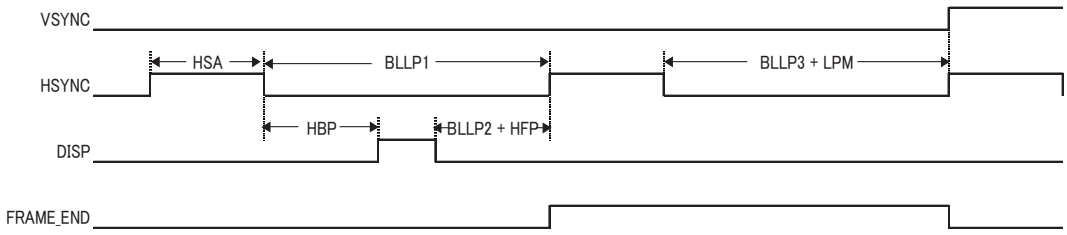
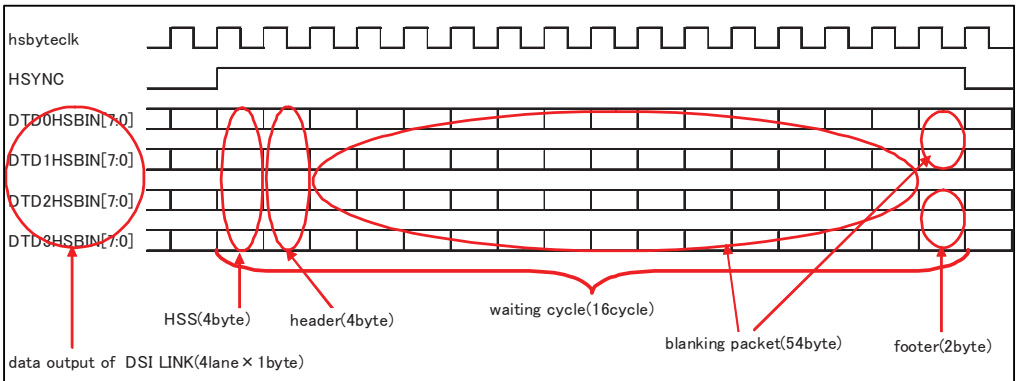


Figure 42.4 Period of waiting cycle



Example of calculating amount of HSA BlankingPacket payload

<Register setting>
LCDC register MLDHSYNR. HSYNW[3:0]= 2 Character(16dot)
SYSCONF.LANEEN[3:0]=4'hF(4lane) => 4byte data output/1cycle

<Calculation of waiting cycle of HSA>
waiting cycle of HSA = LCDC register MLDHSYNR. HSYNW[3:0] × 8 × 1cycle(ns) of dotclock ÷ 1cycle(ns) of HSBYTECLK
Because 1cycle(ns) of dotclock = 1 cycle(ns) of HSBYTECLK , it becomes the following.
(Refer to the explanation for VMCTR1.BKM)
= LCDC register MLDHSYNR. HSYNW[3:0] × 8
= 2 × 8
= 16cycle

<calculating amount of HSA BlankingPacket payload>
amount of HSA BlankingPacket payload = (Number of lanes × waiting cycle of HSA) − 10
= 4 × 16 − 10
= 54byte

Figure 42.5 Example of calculating payload length of HSA at BlankingPacket period

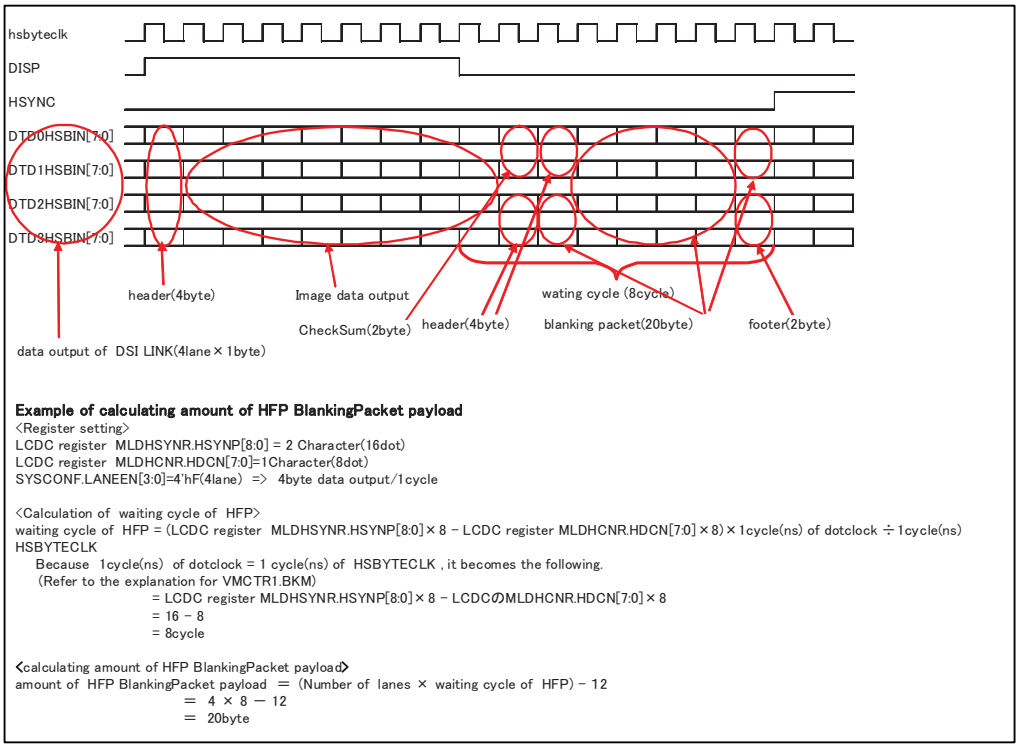


Figure 42.6 Example of calculating payload length of HFP at BlankingPacket period

42.4.3. LCDC Setting

When the DSI-TX is connected with the LCDC, the following limitations are applied to the LCDC setting in order to match the input format of the DIS-TX:

- Use the main LCD setting.
- LDDCKR.MOSEL =1: The divided clock cannot be used.
- MLDMT1R.VPOL = 0, HPOL=0, DIPOL=0: The Vsync, Hsync, and DSIP signals are set to positive.
- MLDMT1R.HSCNT =0: Hsync is kept being output.
- MLDMT1R.IFM=0, MIFTYP[3:0]=4'b1011: Data is output in 24bpp RGB mode.

or

MLDMT1R.YM=1, MLDMT1R.IFM=0, MIFTYP[3:0]=4'b1111: Data is output in the YUV422 format.

- MLDMT2R.VSEL=0: Vsync is set for output mode.
- Set the VSYNP[10:0] in the MLDVSYNR register so that they are one smaller than the actual output to the LCD panel.
  (This is because data is needed one line earlier in order to buffer data within the DSI-Tx.)
- MLDVLNR.VTLN[10:0] – MLDVSYNR.VSYNP[10:0] ≥ 2 :
  (Vertical front-porth periods are needed for proper control.)
- Please set MLDHSYNR.HSYNW[3:0] to two or more at SYSCONF.LANEEN[3:0]=4'h1 (one lane).
  It becomes impossible to set the payload length of BlankingPacket of HSA when one is set.
  Because it comes to transmit ten bytes(ten cycles) of HSS(4byte) + header (4byte) + footer (2byte) in total for the period of HSA (eight cycles).

42.4.4. Transmitting Command-Packets in Video Mode

In the video mode, command-packets are transmitted during BLLP periods between video-packets.

Command-packet transmission is allowed in BLLP1 by using the VMCTR2.BL1IEN.

Command-packet transmission is allowed in BLLP2 by using the VMCTR2.BL2IEN.

Command-packet transmission is allowed in BLLP3 by using the VMCTR2.BL3IEN.

Only one command-packet can be transmitted during a BLLP period. When transmission is completed, a transition to LPS occurs.

Note: Command-packet transmission is prohibited beyond a BLLP period.

Figure 42.7 shows how a command-packet is transmitted during BLLP1.

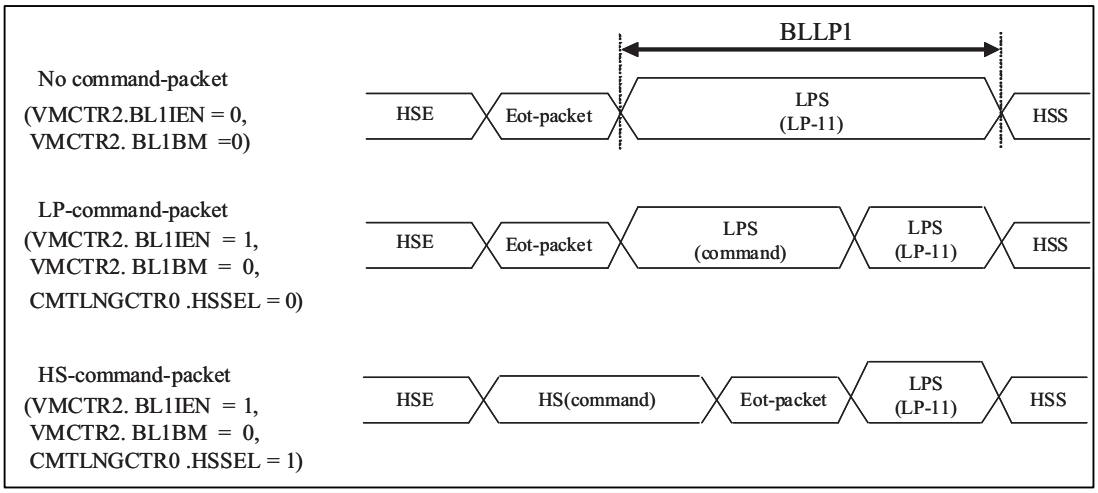


Figure 42.7 Command transmission at Video mode

42.4.5. Command-packet transmission at command mode

When command-packet are transmitted in HighSpeed transmission, the behavior changes depending on the FLEN bit in the DTCTR register.

If the FLEN bit in the DTCTR register is 0, transmission continues as long as there is a command transmission request.

If the FLEN bit in the DTCTR register is 1, a transition to LPS occurs even if there is a command transmission request.

42.4.6. Command-Packet Transmission for Small Data

If the data length to be transmitted is less than 16 bytes, the data can be transmitted from a register.

Data is loaded into CMTIADRx, CMTITTLx, CMTIADRIx, and CMTIRNx in order.

If the TXSEL bit in CMTLNGCTRx register is set to 0 and the TXREQ bit in the CMTLNGREQx register to 1, packets are transmitted in units of the data length specified in the LENG[11:0] bit in CMTLNGCTRx register.

Note: A lowercase "x" in a register name denotes 0 to 3.

Moreover, when it is short packet in two bytes in the transmitted data length, command can transmit by setting the following registers.

- It sets to DTCTR.MTEN=1, and the command mode is enabled.
- According to the CMTSRTCTR register, transmitted virtual channel, Datatype, and short packet data and HS transmission/LP transmission are selected .
- It is assumed CMTSRTREQ. TXREQ=1, and starts the command transmission.

Note:

If you want to do the video mode continuously after this, after becoming CMTSRTREQ. TXREQ=0, and completing the transmission of the command mode, set the register of the video mode and the register of LCDC.

42.4.7. Transmitting Command Packets

Command packet generation registers (4 channels for long packets and 1 channel for short packets) transmit one packet at a time in the order of short, long 0, long 1, long2, long 3, and short packets.

If specific channel data is to take precedence in transmitting, cancel operations for the other channels (set the TXREQ bit in CMTLNGREQx register to 0 or suspend them (set the TXWAIT bit in CMTLNGREQx register to 1).

42.4.8. Dividing Transmit Data

If the value in the INITTAL[31:0] in CMTITTLx register is greater than the one in the LENG[11:0] in CMTLNGCTRx register, transmit data is to be transmitted by dividing into multiple packets.

It is transmitted as packets each of which has the payload length specified in the LENG[11:0] in CMTLNGCTRx register.

Fractional data is transmitted in the last packet.

42.4.9. Example of Command Mode Transmission Setting

An example of the setting when the following data1 and data2 are transmitted in parallel is shown below.

data1:
Image data (1280 for the width × 800 for the height, RGB888 format)
It is stored from address 0x0c000000 at 0x00001000 interval by lines.
The ID information of the transmit packet is set as VC=2, start DT=0Ah, intermediate DT=0Bh, end DT=0C.

data2:
JPEG code (size: 25,001 bytes)
It is stored from address 0x0d000000.
The ID information of the transmit packet is set as VC=0, DT=0Dh.

```
CMTIADR0      = 0x0C000000
CMTITTL0      = 0x00000F00    ← 1280 pixels × 3 bytes/pixel
CMTIADRI0     = 0x00001000
CMTIRN0       = 0x00000320    ← 800 lines
CMTLNGCTR0 = 0x8A080003    ← 1 packet = 2048 bytes, HS transmission
CMTLNGDT0   = 0x00010B0C

CMTIADR1      = 0x0D000000
CMTITTL1      = 0x0003d091    ← 250001 bytes
CMTIADRI1     = 0x00000000
CMTIRN1       = 0x00000001    ← 1 transmission
CMTLNGCTR0  = 0x0D040003    ← 1 packet = 1024 bytes, HS transmission
```

CMTLNGDT0 = 0x00000000

CMTLNGREQ0 = 0x00000001
CMTLNGREQ1 = 0x00000001

The header information of packets to be output with this setting is shown in figure 42.8.

It shows the output order of command packets.

```
No  VC    DT    WC
-----------------------------------------------------------------
1   VC=2  DT=0A  WC=0800  <- data1 first_line
2   VC=0  DT=0D  WC=0400  <- data2 first_data
3   VC=2  DT=0B  WC=0700  <- data1 first_line_end
4   VC=0  DT=0D  WC=0400
5   VC=2  DT=0B  WC=0800  <- data1 2nd_line
6   VC=0  DT=0D  WC=0400
7   VC=2  DT=0B  WC=0700
8   VC=0  DT=0D  WC=0400
9   VC=2  DT=0B  WC=0800  <- data1 2nd_line
10  VC=0  DT=0D  WC=0400
11  VC=2  DT=0B  WC=0700
12  VC=0  DT=0D  WC=0400
        .
        .
        .
485 VC=2  DT=0B  WC=0800  <- data1 122th_line
486 VC=0  DT=0D  WC=0400
487 VC=2  DT=0B  WC=0700
488 VC=0  DT=0D  WC=0400
489 VC=2  DT=0B  WC=0800  <- data1 123th_line
490 VC=0  DT=0D  WC=0091  <- data2 final_data  -> DTST.tx_data_end_ch1=1
481 VC=2  DT=0B  WC=0700
492 VC=2  DT=0B  WC=0800  <- data1 124th_line
493 VC=2  DT=0B  WC=0700
494 VC=2  DT=0B  WC=0800  <- data1 125th_line
495 VC=2  DT=0B  WC=0700
        .
        .
        .
1842 VC=2  DT=0B  WC=0800  <- data1 799th_line
1843 VC=2  DT=0B  WC=0700
1844 VC=2  DT=0B  WC=0800  <- data1 800th_line
1845 VC=2  DT=0C  WC=0700   <- data1 final_data  -> DTST.tx_data_end_ch0=1
```

Figure 42.8 Example of the order of outputting command packet

42.4.10. Register Settings When Combining YUV

When the command of the YUV mixture is transmitted, the command packet generation register group is used by two channels.

The setting of two channels is as follows.

```
CMTIADR2      = 0x0E000000   ← Y data source address
CMTITTL2      = 0x00000F00   ← Number of the horizontal data
CMTIADRI2     = 0x00001000   ← Stride amount
CMTIRN2       = 0x00000004   ← Number of the line
CMTLNGCTR2    = 0xCA080003   ←1 packet = 2048 bytes, HS transmission
CMTLNGDT2     = 0x0D000000   ←Source data: YUV422, transmission data: YUV422

CMTIADR3      = 0x0E400000   ← C data source address
CMTITTL3      = 0x00000F00   ← Set the same value as in CH2
CMTIADRI3     = 0x00001000   ← Stride amount
CMTIRN3       = 0x00000004   ← Number of the line*
CMTLNGCTR3    = 0x2A080003   ← Set the same value as in CH2
CMTLNGDT3     = 0x0D000000   ←Set the same value as in CH2

CMTLNGREQ3 = 0x00000001      ← These channels can issue requests in either order.
CMTLNGREQ2 = 0x00000001
```

Note: * Set the same value as CH0 if the original data is YUV422. Set 1/2 of CH0 if the original data is YUV420.

42.4.11. DSI control procedure

Figure 42.9 shows the control procedure of DSI.

Showing in the chart becomes a control procedure at the video mode of synchronization with LCDC.

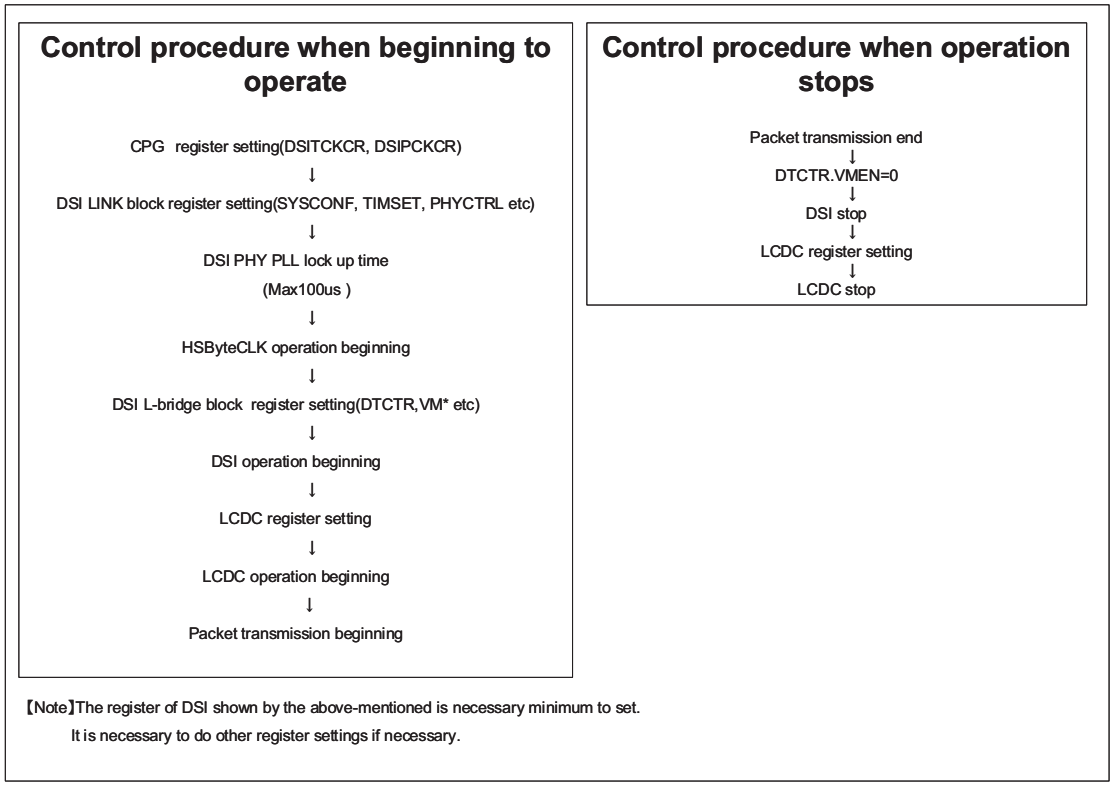


Figure 42.9 DSI control procedure

42.5. Operation sequence

The operation sequences related to the LINK block are described below.

However, 42.5.7 chiefly becomes explanations concerning the L-bridge block.

42.5.1 Power-on Reset Sequence

All FFs in the LINK block are initialized and all lanes transition to LP-11 immediately after reset.

Each register should be set after that.

The lanes disabled by the LANEEN[3:0] bit in the SYSCONF register transition to LP-00.

42.5.2 HS Transmission Sequence (Clock Lane Software Control Mode)

The clock lane software control mode is a mode in which the HS byte clock is kept being output after a transition to LPS. In this case, the clock is turned on/off by software.

The clock lane software control mode is entered by writing 1 to the CLSTPM bit in SYSCONF register and a transition to the HS mode of clock lanes is started by writing 1 to the CLHERQ bit in DSICTRL register. When the CLHERQ bit in DSICTRL register is 1, changing the CLSTPM bit in SYSCONF register is prohibited. Changing the CLSTPM bit in SYSCONF register is also prohibited during transmission within a frame. This is because when a transition from the HS mode to LPS (or vice versa) should occur is changed by turning clock lanes on and off so the output timing of sync event packets (Hsync and Vsync) is changed.

For a clock lane to transition to LPS, the CLHERQ bit in the DSICTRL register should be written to 0.

42.5.3 Reset Trigger Transmission Sequence

The reset trigger transmission sequence is described below.

Write 1 to the RSTRRQ bit in DSICTRL register when there is no transmission request for all video and command modes.

This causes the LINK block to initiate a transition to LPDT and to transmit a reset trigger.

After the transmission is completed, it changes to the LP-11 state.

Then, it waits for peripheral devices to be initialized by using the peripheral reset timer.

Set a timeout value in the PRTOVSET register and write 1 to the PRTOSRQ bit in DSICTRL register to start counting up of the peripheral timer.

When a timeout set in PRTOVSET register occurs, an interrupt is generated if enabled.

42.5.4 ULPS Transition Sequence

The ULPS transition sequence is described below.

Write 1 to the ULENRQ bit in DSICTRL register when there is no transmission request for all video and command modes.

This causes the LINK block to initiate a transition to ULPS.

When the transition to ULPS is completed, in the ULPSENS bit in DSIS register and the ULPSENINTS bit in DSIINT register are asserted to 1 and an interrupt is generated if enabled.

For a transition from ULPS to LP-11 to occur, the ULEXRQ bit in DSICTRL register should be written to 0.

42.5.5 Tearing Effect Sequence

The tearing effect sequence is described below.

When the TEREQ bit in CMRTEREQ register is set to 1, the DSI-Tx transitions to the Rx Stop state (reception wait state).

Then, it waits for a tearing effect trigger from peripheral devices.

When a tearing effect trigger is received, the LPTAK bit in DTST register is set to 1 and an interrupt is generated if enabled.

42.5.6 Recovery Sequence When a Contention is detected

The recovery sequence when a contention is detected is described below.

When a contention is detected, the HCOTEERINTS bit in DSIINT register or the LCOTEERINTS bit in DSIINT register is asserted and an interrupt is generated if enabled.

Then, issue a software reset (set the SWRST bit in SYSCTRL register to 1) or hardware reset. This reset causes a transition to the Tx Stop state (transmission wait state).

42.5.7 Command reception sequence

It explains the sequence when the command is received.

When the command is received at CMRCTR.CRXEN=1, DSI is stored in reception FIFO according to the setting of the CMRCTR register.

When it is a long packet, the part PH (packet header) and the data division are stored in each FIFO.

Moreover, when it is a short packet, the received command is stored in FIFO as a part PH (packet header).

Figure 42.10 shows the storage order to FIFO of receive data.

The received command doesn't store in FIFO and be annulled when FIFO is full.

FIFO1	data 4[7:0]	data 3[7:0]	data 2[7:0]	data 1[7:0]
FIFO2	data 8[7:0]	data 7[7:0]	data 6[7:0]	data 5[7:0]
FIFO3	data12[7:0]	data11[7:0]	data10[7:0]	data 9[7:0]
・	・	・	・	・
・	・	・	・	・
FIFO14	data56[7:0]	data55[7:0]	data54[7:0]	data53[7:0]
FIFO15	data60[7:0]	data59[7:0]	data58[7:0]	data57[7:0]

Figure 42.10 The storage order to FIFO of receive data

- PH (packet header) division

When one or more data is stored in reception FIFO for the header, DTST.FHEX is set ,and the data number in FIFO is displayed to CMRCTR.FHNM [2:0]

Please read data in FIFO from the CMRHEAD register with CPU.

Moreover, when it is CMRCTR.FIFOS=1, the received part PH (packet header) is stored in both reception FIFO for the header and reception FIFO for data..

- Data division

When one or more data is stored in reception FIFO for data , DTST.FDEX is set, and the data number in FIFO is displayed to CMRCTR.FDNM[3:0].

When it is CMRCTR.DMAEN=0, read data in FIFO from the CMRDAT register with CPU

When it is CMRCTR.DMAEN=1, specify the CMRDAT register for the source address of DMAC and read it by DMA forwarding.

When there is one or more data in reception FIFO for data , DREQ is made active from DSI, and the DMA forwarding is done according to the setting of the register of DMAC.

Moreover, when ECC multi-bit error happens to receive data , it doesn't store in FIFO until the packet ends and it is annulled.

When unnecessary data of the packet in which ECC multi-bit error happens remains in FIFO,make FIFO empty by reading with CPU or setting CMRCTR.FRST, and put it into the state that the following receive data can be stored in FIFO.

Section 43 JPEG Processing Unit (JPU)

The JPEG processing unit (JPU) incorporates the JPEG codec with an encoding and decoding function conforming to the JPEG baseline process, so that the JPU can encode image data and decode JPEG data quickly.

For the encoding and decoding processes, frame buffers or line buffers for raster block conversion are necessary in an external buffer space, such as an SDRAM externally connected to the LSI.

43.1 Features

The JPU has the following features.

- Conforming specification: JPEG baseline
- Operating precision: Conforming to JPEG Part 2, ISO-IEC10918-2
- Color format: YCbCr 4:2:2 (H = 2:1:1, V = 1:1:1), YCbCr 4:2:0 (H = 2:1:1, V = 2:1:1)
- Four quantization tables provided
- Four Huffman tables provided (two AC tables, two DC tables)
- Markers supported: Start of image (SOI), start of frame type 0 (SOF0), start of scan (SOS), define quantization tables (DQT), define Huffman tables (DHT), define restart interval (DRI), restart (RSTm), end of image (EOI)
- Image data rate: Maximum 108 Mbytes/s (54 MHz operation)
- The frame buffer size in the RAM area, such as SDRAM, can be reduced by using line buffer mode.

  This mode cannot be used with some pixel clock frequencies of the camera sensor or RAM configuration.
- Image rotation (by 90°, 180°, or 270°) can be performed in the encoding process (only in frame buffer mode).
- In reload mode, address toggling at every transfer of a specified amount of data during stream reading and writing is supported so that the buffer capacity can be reduced.
- Processing unit: 8-byte address boundary, 4-byte data length

  Note that the output data size during encoding is determined by the 16-byte boundary at the end of the address.
- Processable image size: From 16 × 16 to 4092 × 4092 pixels (horizontal × vertical)

  Image is processed in 4-pixel units.

Note: Do not perform unsupported color formatting or encoding or decoding of an image with an unsupported size.

Figure 43.1 shows the connection between the JPU and peripheral modules.

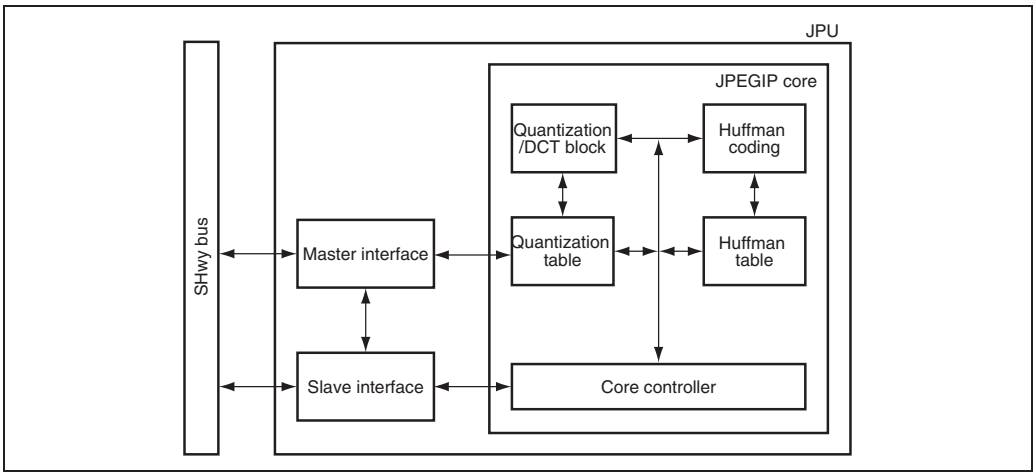


Figure 43.1 Connection between JPU and Peripheral Modules

43.2 Register Descriptions

Table 43.1 shows the JPU registers. Table 43.2 shows the register state in each processing mode.

These registers are 32-bit access registers. When modifying the reserved bits or read-only bits, write 0 to the bits. However, when clearing the bits in the JPEG interrupt status register (JINTS), write 0 only to the bits to be cleared and write 1 to the other bits. If register access which is not specified is performed, operation cannot be guaranteed.

Table 43.1 Register Configuration

Register Name	Abbreviation	R/W	Address	Access Size
JPEG code mode register	JCMOD	R/W	H'FE98 0000	32
JPEG code command register	JCCMD	R/W	H'FE98 0004	32
JPEG code status register	JCSTS	R	H'FE98 0008	32
JPEG code quantization table number register	JCQTN	R/W	H'FE98 000C	32
JPEG code Huffman table number register	JCHTN	R/W	H'FE98 0010	32
JPEG code DRI upper register	JCDRIU	R/W	H'FE98 0014	32
JPEG code DRI lower register	JCDRID	R/W	H'FE98 0018	32
JPEG code vertical size upper register	JCVSZU	R/W	H'FE98 001C	32
JPEG code vertical size lower register	JCVSZD	R/W	H'FE98 0020	32
JPEG code horizontal size upper register	JCHSZU	R/W	H'FE98 0024	32
JPEG code horizontal size lower register	JCHSZD	R/W	H'FE98 0028	32
JPEG code data count upper register	JCDTCU	R	H'FE98 002C	32
JPEG code data count middle register	JCDTCM	R	H'FE98 0030	32
JPEG code data count lower register	JCDTCD	R	H'FE98 0034	32
JPEG interrupt enable register	JINTE	R/W	H'FE98 0038	32
JPEG interrupt status register	JINTS	R/W	H'FE98 003C	32
JPEG code decode error register	JCDERR	R/W	H'FE98 0040	32
JPEG code reset register	JCRST	R	H'FE98 0044	32
JPEG interface encoding control register	JIFECNT	R/W	H'FE98 0070	32
JPEG interface encode source Y address register 1	JIFESYA1	R/W	H'FE98 0074	32
JPEG interface encode source C address register 1	JIFESCA1	R/W	H'FE98 0078	32

Register Name	Abbreviation	R/W	Address	Access Size
JPEG interface encode source Y address register 2	JIFESYA2	R/W	H'FE98 007C	32
JPEG interface encode source C address register 2	JIFESCA2	R/W	H'FE98 0080	32
JPEG interface encode source memory width register	JIFESMW	R/W	H'FE98 0084	32
JPEG interface encode source vertical size register	JIFESVSZ	R/W	H'FE98 0088	32
JPEG interface encode source horizontal size register	JIFESHSZ	R/W	H'FE98 008C	32
JPEG interface encode destination address register 1	JIFEDA1	R/W	H'FE98 0090	32
JPEG interface encode destination address register 2	JIFEDA2	R/W	H'FE98 0094	32
JPEG interface encode data reload size register	JIFEDRSZ	R/W	H'FE98 0098	32
JPEG interface decoding control register	JIFDCNT	R/W	H'FE98 00A0	32
JPEG interface decode source address register 1	JIFDSA1	R/W	H'FE98 00A4	32
JPEG interface decode source address register 2	JIFDSA2	R/W	H'FE98 00A8	32
JPEG interface decode data reload size register	JIFDDRSZ	R/W	H'FE98 00AC	32
JPEG interface decode destination memory width register	JIFDDMW	R/W	H'FE98 00B0	32
JPEG interface decode destination vertical size register	JIFDDVSZ	R	H'FE98 00B4	32
JPEG interface decode destination horizontal size register	JIFDDHSZ	R	H'FE98 00B8	32
JPEG interface decode destination Y address register 1	JIFDDYA1	R/W	H'FE98 00BC	32
JPEG interface decode destination C address register 1	JIFDDCA1	R/W	H'FE98 00C0	32
JPEG interface decode destination Y address register 2	JIFDDYA2	R/W	H'FE98 00C4	32
JPEG interface decode destination C address register 2	JIFDDCA2	R/W	H'FE98 00C8	32

Register Name	Abbreviation	R/W	Address	Access Size
JPEG code quantization table 0 register	JCQTBL0	R/W	H'FE99 0000 to H'FE99 003C	32
JPEG code quantization table 1 register	JCQTBL1	R/W	H'FE99 0040 to H'FE99 007C	32
JPEG code quantization table 2 register	JCQTBL2	R/W	H'FE99 0080 to H'FE99 00BC	32
JPEG code quantization table 3 register	JCQTBL3	R/W	H'FE99 00C0 to H'FE99 00FC	32
JPEG code Huffman table DC0 register	JCHTBD0	R/W	H'FE99 0100 to H'FE99 010C	32
JPEG code Huffman table DC0 register	JCHTBD0	R/W	H'FE99 0110 to H'FE99 0118	32
JPEG code Huffman table AC0 register	JCHTBA0	R/W	H'FE99 0120 to H'FE99 012C	32
JPEG code Huffman table AC0 register	JCHTBA0	R/W	H'FE99 0130 to H'FE99 01D0	32
JPEG code Huffman table DC1 register	JCHTBD1	R/W	H'FE99 0200 to H'FE99 020C	32
JPEG code Huffman table DC1 register	JCHTBD1	R/W	H'FE99 0210 to H'FE99 0218	32
JPEG code Huffman table AC1 register	JCHTBA1	R/W	H'FE99 0220 to H'FE99 022C	32
JPEG code Huffman table AC1 register	JCHTBA1	R/W	H'FE99 0230 to H'FE99 02D0	32

Note: For the settings of the JPEG code quantization table and JPEG code Huffman table, see section 43.3.1 (6), Table Setting.

Table 43.2 Register State in Each Processing Mode

Register Abbreviation	Power-On Reset	Manual Reset	Module Standby	Sleep
JCMOD	Initialized	Initialized	Retained	Retained
JCCMD	Initialized	Initialized	Retained	Retained
JCSTS	Initialized	Initialized	Retained	Retained
JCQTN	Initialized	Initialized	Retained	Retained
JCHTN	Initialized	Initialized	Retained	Retained
JCDRIU	Initialized	Initialized	Retained	Retained
JCDRID	Initialized	Initialized	Retained	Retained
JCVSZU	Initialized	Initialized	Retained	Retained
JCVSZD	Initialized	Initialized	Retained	Retained
JCHSZU	Initialized	Initialized	Retained	Retained
JCHSZD	Initialized	Initialized	Retained	Retained
JCDTCU	Initialized	Initialized	Retained	Retained
JCDTCM	Initialized	Initialized	Retained	Retained
JCDTCD	Initialized	Initialized	Retained	Retained
JINTE	Initialized	Initialized	Retained	Retained
JINTS	Initialized	Initialized	Retained	Retained
JCDERR	Initialized	Initialized	Retained	Retained
JCRST	Initialized	Initialized	Retained	Retained
JIFECNT	Initialized	Initialized	Retained	Retained
JIFESYA1	Initialized	Initialized	Retained	Retained
JIFESCA1	Initialized	Initialized	Retained	Retained
JIFESYA2	Initialized	Initialized	Retained	Retained
JIFESCA2	Initialized	Initialized	Retained	Retained
JIFESMW	Initialized	Initialized	Retained	Retained
JIFESVSZ	Initialized	Initialized	Retained	Retained
JIFESHSZ	Initialized	Initialized	Retained	Retained
JIFEDA1	Initialized	Initialized	Retained	Retained
JIFEDA2	Initialized	Initialized	Retained	Retained

Register Abbreviation	Power-On Reset	Manual Reset	Module Standby	Sleep
JIFEDRSZ	Initialized	Initialized	Retained	Retained
JIFDCNT	Initialized	Initialized	Retained	Retained
JIFDSA1	Initialized	Initialized	Retained	Retained
JIFDSA2	Initialized	Initialized	Retained	Retained
JIFDDRSZ	Initialized	Initialized	Retained	Retained
JIFDDMW	Initialized	Initialized	Retained	Retained
JIFDDVSZ	Initialized	Initialized	Retained	Retained
JIFDDHSZ	Initialized	Initialized	Retained	Retained
JIFDDYA1	Initialized	Initialized	Retained	Retained
JIFDDCA1	Initialized	Initialized	Retained	Retained
JIFDDYA2	Initialized	Initialized	Retained	Retained
JIFDDCA2	Initialized	Initialized	Retained	Retained
JCQTBL0	Undefined	Undefined	Retained	Retained
JCQTBL1	Undefined	Undefined	Retained	Retained
JCQTBL2	Undefined	Undefined	Retained	Retained
JCQTBL3	Undefined	Undefined	Retained	Retained
JCHTBD0	Undefined	Undefined	Retained	Retained
JCHTBD0	Undefined	Undefined	Retained	Retained
JCHTBA0	Undefined	Undefined	Retained	Retained
JCHTBA0	Undefined	Undefined	Retained	Retained
JCHTBD1	Undefined	Undefined	Retained	Retained
JCHTBD1	Undefined	Undefined	Retained	Retained
JCHTBA1	Undefined	Undefined	Retained	Retained
JCHTBA1	Undefined	Undefined	Retained	Retained

43.2.1 JPEG Code Mode Register (JCMOD)

JCMOD sets the operating mode before the JPU starts operation.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	SOIC	PCTR	MSKIP[1:0]		CCNT	DSP	REDU[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	SOIC	0	R/W	SOI Marker Delete This bit is valid when the MSKIP bit is B'00. In this mode, the amount of coded data indicated by registers JCDTCU, JCDTDM, and JCDTCD includes the SOI (2 bytes). 0: SIO marker exists 1: SOI marker deleted
7	PCTR	0	R/W	Image Data Input Control This bit should be fixed to 1.
6, 5	MSKIP[1:0]	00	R/W	Marker Skip Mode 00: Marker output 01: No marker output Other than above: Setting prohibited
4	CCNT	0	R/W	Code Amount Count Mode (This bit is valid only in decoding.) 0: Code amount count mode disabled 1: Code amount count mode enabled

Bit	Bit Name	Initial Value	R/W	Description
3	DSP	0	R/W	Encoding/Decoding Set 0: Encoding process 1: Decoding process
2 to 0	REDU[2:0]	000	R/W (Encoding) R (Decoding)	Subsampling Set 001: 4:2:2 010: 4:2:0 Other than above: Setting prohibited (in encoding) Error (JPU cannot process normally in decoding.)

43.2.2 JPEG Code Command Register (JCCMD)

JCCMD sets commands. Bits of this register need not be cleared to 0 after setting a command.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	SRST	RWCMD	RRCMD	LCMD1	LCMD2	BRST	—	—	—	—	JEND	JRST	JSRT
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R*/W	R*/W	R*/W	R*/W	R*/W	R	R	R	R	R*/W	R*/W	R*/W

Note: * Values read from these bits are undefined.

Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
12	SRST	0	R/W	Software Reset Setting this bit to 1 resets the JPU. This bit holds 1 until the transfer between the CPU bus and the JPU is completed; it is cleared to 0 when the transfer is completed. After a software reset is specified, do not specify another software reset or a bus reset before this bit is cleared to 0. For details, refer to section 43.6, Software Reset Processing.
11	RWCMD	0	R*/W	Reload Buffer Write Restart Command This bit is valid during the encoding process in reload mode. The JPU stops writing the data to be coded to a reload buffer after one buffer of data specified by JIFEDRSZ has been transferred. Though the encoding process automatically stops, the first two reload buffers of data are automatically written. However, when JIFEDA1 is equal to JIFEDA2, only one reload buffer operates and the JPU stops writing the data to be coded after the first one buffer of data has been transferred. Restart writing the data to be coded by writing 1 to this bit.
10	RRCMD	0	R*/W	Reload Buffer Read Restart Command This bit is valid during decoding in reload mode. The JPU stops reading the coded data from a reload buffer after one buffer of data specified by JIFDDRSZ has been transferred. Restart reading the coded data by writing 1 to this bit. JPU continues reading coded data as long as the end of the code is not detected.
9	LCMD1	0	R*/W	External Line Buffer Processing Restart Command This bit is valid only for subsampling setting 4:2:0 in line buffer mode. JPU stops transferring the image data after transfer of the lines of data specified by JIFDCNT or JIFECNT is completed. Though the JPU automatically stops processing, the first two lines of data are automatically written. However, when JIFDDYA1 is equal to JIFDDYA2 and JIFDDCA1 is equal to JIFDDCA2, only one line buffer operates and the JPU stops writing the image data after the first one buffer of data has been transferred. Restart transferring by writing 1 to this bit in both the encoding and decoding processes.

Bit	Bit Name	Initial Value	R/W	Description
8	LCMD2	0	R*/W	External Line Buffer Process Restart Command This bit is valid only for subsampling setting 4:2:2 in line buffer mode. JPU stops transferring the mage data after transfer of the lines of data specified by JIFDCNT or JIFECNT is completed. Though the JPU automatically stops processing, the first two lines of data are automatically written. However, when JIFDDYA1 is equal to JIFDDYA2 and JIFDDCA1 is equal to JIFDDCA2, only one line buffer operates and the JPU stops writing the image data after the first one buffer of data has been transferred. Restart transferring by writing 1 to this bit in both the encoding and decoding processes.
7	BRST	0	R*/W	Bus Reset Setting this bit to 1 resets internal circuits. While the JPU is in operation (from JPEG core process start command setting to JINTS data transfer end interrupt occurrence), do not set this bit to 1. For the bus reset processing, see section 43.5, Bus Reset Processing.
6 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	JEND	0	R*/W	Interrupt Signal Clear Command This bit is valid for interrupt sources bits INS6, INS5, and INS3 in the JINTS register. To clear an interrupt signal, set this bit to 1.
1	JRST	0	R*/W	JPEG Core Processing-Stopped Revoke Command To clear the processing-stopped state because of requests to read the image size and subsampling setting (the INT3 bit in the JINTE register), set this bit to 1. (This bit is valid only in decoding.)
0	JSRT	0	R*/W	JPEG Core Process Start Command To start JPEG core processing, set this bit to 1. Do not write this bit to 1 again before the JPU is not completely activated.

Note: * Values read from these bits are undefined.

43.2.3 JPEG Code Status Register (JCSTS)

JCSTS indicates the internal state of the JPU.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	STS
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0.
0	STS	0	R	Operating State This bit indicates the operating state of the JPEG core in the JPU. If its state is indicated as not in operation, the JPU may not have transferred data completely. To check whether the data has been completely transferred, use the transfer end interrupt through the JINTS register. 0: Not in operation 1: Encoding or decoding

43.2.4 JPEG Code Quantization Table Number Register (JCQTN)

JCQTN sets the quantization table number before encoding is started.

- To use quantization table No. 0 (JCQTBL0) as the first color component, set QT1 to B'00
- To use quantization table No. 1 (JCQTBL1) as the first color component, set QT1 to B'01
- To use quantization table No. 2 (JCQTBL2) as the first color component, set QT1 to B'10
- To use quantization table No. 3 (JCQTBL3) as the first color component, set QT1 to B'11

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	QT3[1:0]		QT2[1:0]		QT1[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5, 4	QT3[1:0]	00	R/W	Quantization table number for the third color component
3, 2	QT2[1:0]	00	R/W	Quantization table number for the second color component
1, 0	QT1[1:0]	00	R/W	Quantization table number for the first color component

43.2.5 JPEG Code Huffman Table Number Register (JCHTN)

JCHTN sets the Huffman table number (AC/DC) before encoding is started.

- To use DC/AC Huffman table No. 0 (JCHTBD0 and JCHTBA0) as the first color component, set bits HTA1 and HTD1 to B'0
- To use DC/AC Huffman table No. 1 (JCHTBD1 and JCHTBA1) as the first color component, set bits HTA1 and HTD1 to B'1

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	HTA3	HTD3	HTA2	HTD2	HTA1	HTD1
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R\W	R\W	R\W	R\W	R\W	R\W

Bit	Bit Name	Initial Value	R/W	Description
31 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	HTA3	0	R/W	Huffman table number (AC) for the third color component
4	HTD3	0	R/W	Huffman table number (DC) for the third color component
3	HTA2	0	R/W	Huffman table number (AC) for the second color component
2	HTD2	0	R/W	Huffman table number (DC) for the second color component
1	HTA1	0	R/W	Huffman table number (AC) for the first color component
0	HTD1	0	R/W	Huffman table number (DC) for the first color component

43.2.6 JPEG Code DRI Upper Register (JCDRIU)

JCDRIU sets the upper bytes of the minimum coded units (MCUs) preceding an RST marker.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	DRIU[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	DRIU[7:0]	H'00	R/W	Upper Bytes of MCUs Preceding RST Marker When both upper and lower bytes are set to H'00, neither a DRI nor an RST marker is placed. (These bits are valid only in encoding.)

43.2.7 JPEG Code DRI Lower Register (JCDRID)

JCDRID sets the lower bytes of MCUs preceding an RST marker.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	DRID[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	DRID[7:0]	H'00	R/W	Lower Bytes of MCUs Preceding RST Marker When both upper and lower bytes are set to H'00, neither a DRI nor an RST marker is placed. (These bits are valid only in encoding.)

43.2.8 JPEG Code Vertical Size Upper Register (JCVSZU)

JCVSZU sets the upper bytes of the vertical image size. When rotating the image in encoding, set the size of the rotated image in this register.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	VSZU[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	VSZU[7:0]	H'00	R/W	Upper Bytes of Vertical Image Size Up to 4092 pixels can be set as the vertical image size. In the decoding process, a downloaded value from the JPEG coded data is set. When the vertical image size exceeds 2048 pixels, it is treated as an error.

43.2.9 JPEG Code Vertical Size Lower Register (JCVSZD)

JCVSZD sets the lower bytes of the vertical image size. When rotating the image in encoding, set the size of the rotated image in this register.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	VSZD[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	VSZD[7:0]	H'00	R/W	Lower Bytes of Vertical Image Size In the decoding process, a downloaded value from the JPEG coded data is set.

43.2.10 JPEG Code Horizontal Size Upper Register (JCHSZU)

JCHSZU sets the upper bytes of the horizontal image size. When rotating the image in encoding, set the size of the rotated image in this register.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	HSZU[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	HSZU[7:0]	H'00	R/W	Upper Bytes of Horizontal Image Size Up to 4092 pixels can be set as the horizontal image size. In the decoding process, a downloaded value from the JPEG coded data is set. When the horizontal image size exceeds 4092 pixels, it is treated as an error.

43.2.11 JPEG Coded Horizontal Size Lower Register (JCHSZD)

JCHSZD sets the lower bytes of the horizontal image size. When rotating the image in encoding, set the size of the rotated image in this register.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	HSZD[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	HSZD[7:0]	H'00	R/W	Lower Bytes of Horizontal Image Size In the decoding process, a downloaded value from the JPEG coded data is set.

43.2.12 JPEG Code Data Count Upper Register (JCDTCU)

The upper bytes for the counted amount of data to be encoded are set to JCDTCU. This register is valid only in an encoding process. The values of this register are reset before encoding starts.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	DCU[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	DCU[7:0]	H'00	R	Upper bytes for the counted amount of data to be encoded

43.2.13 JPEG Code Data Count Middle Register (JCDTCM)

The middle bytes for the counted amount of data to be encoded are set to JCDTCM. This register is valid only in an encoding process. The values of this register are reset before encoding starts.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	DCM[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	DCM[7:0]	H'00	R	Middle bytes for the counted amount of data to be encoded

43.2.14 JPEG Code Data Count Lower Register (JCDTCD)

The lower bytes for the counted amount of data to be encoded are set to JCDTCD. This register is valid only in an encoding process. The values of this register are reset before encoding starts.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	DCD[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	DCD[7:0]	H'00	R	Lower bytes of the counted amount of data to be encoded

43.2.15 JPEG Interrupt Enable Register (JINTE)

JINTE enables interrupts.

When bits INT7 to INT5 are set to B'1, the INS5 bit in JINTS which indicates the error status is set to B'1, and the ERR bit in JCDERR indicates the particular error code.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	INT14	INT13	INT12	INT11	INT10	—	—	INT7	INT6	INT5	—	INT3	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R	R/W	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 15	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
14	INT14	0	R/W	This flag sets whether an interrupt is generated at every address reloading for coded data reading. (This bit is valid only when reload mode is enabled.)
13	INT13	0	R/W	This flag sets whether an interrupt is generated at every address reloading for coded data writing. (This bit is valid only when reload mode is enabled.)
12	INT12	0	R/W	This flag sets whether an interrupt is generated at every transmission completion of Y components in multiples of 16 lines and C components in multiples of 8 lines. (This bit is valid only when line buffer mode is enabled.)
11	INT11	0	R/W	This flag sets whether an interrupt is generated at every transmission completion of Y components in multiples of 8 lines and C components in multiples of 8 lines. (This bit is valid only when line buffer mode is enabled.)
10	INT10	0	R/W	This flag sets whether an interrupt of transfer to the external buffer end is generated.
9, 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
7	INT7	0	R/W	This flag sets whether an interrupt is generated when the number of data in the restart interval of the Huffman-coding segment is not correct. When this flag is not set, an error code is not returned. (This bit is valid only in decoding.)
6	INT6	0	R/W	This flag sets whether an interrupt is generated when the total number of data in the Huffman-coding segment is not correct. When this flag is not set, an error code is not returned. (This bit is valid only in decoding.)
5	INT5	0	R/W	This flag sets whether an interrupt is generated when the last MCU number in the Huffman-coding segment is not correct. When this flag is not set, an error code is not returned. (This bit is valid only in decoding.)
4	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
3	INT3	0	R/W	This flag sets whether an interrupt is generated when it has been determined that the image size and the subsampling setting of the encoded data can be read through analyzing the data.
2 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

43.2.16 JPEG Interrupt Status Register (JINTS)

JINTS identifies the interrupt sources.

The interrupts of bits INS10 to INS14 and INS3 are generated when the corresponding bits in the JINTE register are set to B'1. When the interrupt sources are bits INS14 to INS10, the interrupt signal can be negated by clearing the corresponding interrupt status bits to 0. When the interrupt sources are bits INS6, INS5, or INS3 (JPEG core), the interrupt signal can be negated by clearing the corresponding interrupt status bits to 0 and setting the JCCMD register appropriately.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	INS14	INS13	INS12	INS11	INS10	—	—	—	INS6	INS5	—	INS3	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W*	R/W*	R/W*	R/W*	R/W*	R	R	R	R/W*	R/W*	R	R/W*	R	R	R

Note: * When the bit is read as 1, write 0 to clear it.
When the bit is read as 0, write 1 to it.

Bit	Bit Name	Initial Value	R/W	Description
31 to 15	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
14	INS14	0	R/W*	This bit is set to 1 every time the address is reloaded during stream data reading. (This bit is valid only when reload mode is enabled.)
13	INS13	0	R/W*	This bit is set to 1 every time the address is reloaded during stream data writing. (This bits is valid only when reload mode is enabled.)
12	INS12	0	R/W*	This bit is set to 1 when transfer of Y components in multiples of 16 lines and C components in multiples of 8 lines to the line buffer is completed. (Subsampling setting: 4:2:0, This bit is valid only when line buffer mode is enabled.)

Bit	Bit Name	Initial Value	R/W	Description
11	INS11	0	R/W*	This bit is set to 1 when transfer of Y components in multiples of 8 lines and C components in multiples of 8 lines to the line buffer is completed. (Subsampling setting: 4:2:2, This bit is valid only when line buffer mode is enabled.)
10	INS10	0	R/W*	This bit is set to 1 after all data on the result of JPU encoding and decoding have been completely transferred.
9 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6	INS6	0	R/W*	This bit is set to 1 when the JPEG completes the encoding process normally.
5	INS5	0	R/W*	This bit is set to 1 when an encoded data error occurs. (This bit is valid only in decoding.)
4	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
3	INS3	0	R/W*	This bit is set to 1 when the image size and subsampling setting can be read. (This bit is valid only in decoding.) When an interrupt occurs, the JPU stops processing and the state is indicated by the JCRST register. To make the JPU resume processing, set the JPEG core processing-stopped release command (JRST bit in the JCCMD register).
2 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Note: * When the bit is read as 1, write 0 to clear it.
When the bit is read as 0, write 1 to it.

43.2.17 JPEG Code Decode Error Register (JCDERR)

Through the error code, JCDERR identifies the type of error which occurred in the encoded data analysis for decoding. The values of this register are reset before the JPU starts decoding.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	ERR[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R	Reserved These bits are always read as 0.
3 to 0	ERR[3:0]	1010	R/W	Error Code (See tables 43.4 and 43.5.)

43.2.18 JPEG Code Reset Register (JCRST)

JCRST indicates a processing-stopped state due to requests to read the image size and subsampling setting (the INTS3 bit in the JINTE register) (available in decoding). To resume processing, set the JPEG core processing-stopped release command (the JRST bit in the JCCMD register).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RST
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0.
0	RST	0	R	Operating State 0: State other than below 1: Suspended state caused by JINTE interrupt source

43.2.19 JPEG Interface Encoding Control Register (JIFECNT)

JIFECNT controls the encoding process. Note that the SWAP bit is used also in the decoding process.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	PU[11:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	RE LOAD	SWAP[1:0]		ROT[1:0]		BUF	INFT
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
27 to 16	PU[11:0]	H'000	R/W	Processing Unit (These bits are valid only in line buffer mode.) [YCbCr 4:2:2 processing] Set the number of lines in vertical Y and C components (in multiples of 8: H'008 units). (Write 0 to the bits PU[2:0].) [YCbCr 4:2:0 processing] Set the number of lines in vertical Y components (in multiples of 16: H'010 units). (Write 0 to the bits PU[3:0].) A value equal to half of the number of lines in vertical Y components is automatically set as the number of lines in vertical C components. Note: The maximum number of settable lines is 2048 and the minimum number is 16. Values outside of this range should not be set.
15 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
6	RELOAD	0	R/W	Reload Mode 0: Reload mode disabled 1: Reload mode enabled
5, 4	SWAP[1:0]	00	R/W	Byte/Word Swap (see the JIFDCNT register) Data transferred to the JPU is swapped (image data in encoding; coded data in decoding). 00: (1) (2) (3) (4) 01: (2) (1) (4) (3) [Byte swap] 10: (3) (4) (1) (2) [Word swap] 11: (4) (3) (2) (1) [Word - byte swap]
3, 2	ROT[1:0]	00	R/W	Rotated Read Mode (These bits are valid only in frame buffer mode.) 00: 0° 01: 90° 10: 180° 11: 270°
1	BUF	0	R/W	Buffer Mode 0: Frame buffer mode 1: Line buffer mode
0	INFT	0	R	Subsampling Setting 0: YCbCr 4:2:2 1: YCbCr 4:2:0

Note: Bits other than SWAP can be modified only when the DSP bit in JCMOD is 0 (encoding process).

43.2.20 JPEG Interface Encode Source Y Address Register 1 (JIFESYA1)

JIFESYA1 sets the source address of the Y component.

This register should be set in 8-pixel units. When reading of an image rotated by 90°, 180°, or 270° is specified, set the origin address for the rotated image. Note that a rotated image can be read only in frame buffer mode (see section 43.3.1 (7), Rotated Read Mode Setting).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ESYA1[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ESYA1[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	ESYA1[31:3]	H'0000 0000	R/W	Y Component Source Address (in 8-pixel units)
2 to 0	ESYA1[2:0]		R	The lower three bits should be set to 0.

43.2.21 JPEG Interface Encode Source C Address Register 1 (JIFESCA1)

JIFESCA1 sets the source address of the C component.

This register should be set in 8-pixel units. When reading of an image rotated by 90°, 180°, or 270° is specified, set the origin address for the rotated image. Note that a rotated image can be read only in frame buffer mode (see section 43.3.1 (7), Rotated Read Mode Setting).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ESCA1[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ESCA1[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	ESCA1[31:3]	H'0000 0000	R/W	C Component Source Address (in 8-pixel units)
2 to 0	ESCA1[2:0]		R	The lower three bits should be set to 0.

43.2.22 JPEG Interface Encode Source Y Address Register 2 (JIFESYA2)

JIFESYA2 sets the source address of the Y component, and is valid in line buffer mode.

Set the start address in 8-pixel units. The source address of the Y component, which is used by the JPU, changes automatically in specified line buffer units: JIFESYA1 → JIFESYA2 → JIFESYA1 → . . . .

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ESYA2[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ESYA2[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	ESYA2[31:3]	H'0000 0000	R/W	Y Component Source Address (These bits are valid in line buffer mode. in 8-pixel units)
2 to 0	ESYA2[2:0]		R	The lower three bits should be set to 0.

43.2.23 JPEG Interface Encode Source C Address Register 2 (JIFESCA2)

JIFESCA2 sets the source address of the C component, and is valid in line buffer mode.

Set the start address in 8-pixel units. The source address of the C component, which is used by the JPU, changes automatically in specified line buffer units: JIFESCA1 → JIFESCA2 → JIFESCA1 → . . . .

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ESCA2[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ESCA2[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	ESCA2[31:3]	H'00000 0000	R/W	C Component Source Address (These bits are valid in line buffer mode. in 8-pixel units)
2 to 0	ESCA2[2:0]		R	The lower three bits should be set to 0.

43.2.24 JPEG Interface Encode Source Memory Width Register (JIFESMW)

JIFESMW sets the buffer memory width in which the image data is stored (see section 43.3.3, Storing Image Data). Set this register in 8-pixel units. The maximum settable width is 4092 pixels and the minimum is 16 pixels. Sizes outside of this range should not be set.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	ESMW[11:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 3	ESMW[11:3]	H'000	R/W	Buffer memory width in which image data is stored (in 8-pixel units)
2 to 0	ESMW[2:0]		R	The lower three bits should be set to 0.

43.2.25 JPEG Interface Encode Source Vertical Size Register (JIFESVSZ)

JIFESVSZ sets the vertical size of the image transferred from the external buffer (see section 43.3.3, Storing Image Data). Set the image size in 4-pixel units. The maximum settable width is 4092 pixels and the minimum is 16 pixels. Sizes outside of this range should not be set.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	ESVSZ[11:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 2	ESVSZ[11:2]	H'000	R/W	Vertical size of the image transferred from the external buffer (in 4-pixel units)
1, 0	ESVSZ[1:0]		R	The lower two bits should be set to 0.

43.2.26 JPEG Interface Encode Source Horizontal Size Register (JIFESHSZ)

JIFESHSZ sets the horizontal size of the image transferred from the external buffer (see section 43.3.3, Storing Image Data). Set the image size in 4-pixel units. The maximum settable width is 4092 pixels and the minimum is 16 pixels. Sizes outside of this range should not be set.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	ESHSZ[11:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 2	ESHSZ[11:2]	H'000	R/W	Horizontal size of the image transferred from the external buffer (in 4-pixel units).
1, 0	ESHSZ[1:0]		R	The lower two bits should be set to 0.

43.2.27 JPEG Interface Encode Destination Address Register 1 (JIFEDA1)

JIFEDA1 sets the destination address of the coded data. Set the start address in 8-pixel units.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	EDA1[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EDA1[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	EDA1[31:3]	H'0000 0000	R/W	Coded data destination address (in 8-pixel units)
2 to 0	EDA1[2:0]		R	The lower three bits should be set to 0.

43.2.28 JPEG Interface Encode Destination Address Register 2 (JIFEDA2)

JIFEDA2 sets the destination address of the coded data.

Set the start address in 8-pixel units. The coded data destination address, which is used by the JPU, changes every time the data transfer specified by JIFEDRSZ is completed: JIFEDA1 → JIFEDA2 → JIFEDA1 → . . . . (This register is valid only in auto-reload mode.)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	EDA2[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EDA2[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	EDA2[31:3]	H'0000 0000	R/W	Coded data destination address (in 8-pixel units)
2 to 0	EDA2[2:0]		R	The lower three bits should be set to 0.

43.2.29 JPEG Interface Encode Data Reload Size Register (JIFEDRSZ)

JIFEDRSZ sets the number of data (in 256-byte units) before the target address is switched. This register is valid only in auto-reload mode. This register should be set to H'0000 0000 in code amount count mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	EDRSZ[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EDRSZ[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 8	EDRSZ[23:8]	H'00 0000	R/W	Coded data destination address (in 256-byte units)
7 to 0	EDRSZ[7:0]		R	The lower eight bits should be set to 0.

43.2.30 JPEG Interface Decoding Control Register (JIFDCNT)

JIFDCNT controls the decoding process. Note that the SWAP bit is also used in the encoding process.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	PU[11:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	RE LOAD	SWAP[1:0]		BMS
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
27 to 16	PU[11:0]	H'000	R/W	Processing Unit (These bits are valid only in line buffer mode.) [YCbCr 4:2:2 processing] Set the number of lines in vertical Y and C components (in multiples of 8: H'008 units). (Write 0 to the bits PU[2:0].) [YCbCr 4:2:0 processing] Set the number of lines in vertical Y components (in multiples of 16: H'010 units). (Write 0 to the bits PU[3:0].) A value equal to half of the number of lines in vertical Y components is automatically set as the number of lines in vertical C components. Note: The maximum number of settable lines is 2048 and the minimum number is 16. Values outside of this range should not be set.
15 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3	RELOAD	0	R/W	Reload Mode 0: Reload mode disabled 1: Reload mode enabled

Bit	Bit Name	Initial Value	R/W	Description
2, 1	SWAP[1:0]	00	R/W	Byte/Word Swap (see the JIFECNT register) Data transferred from the JPU is swapped (coded data in encoding, image data in decoding). 00: (1) (2) (3) (4) 01: (2) (1) (4) (3) [Byte swap] 10: (3) (4) (1) (2) [Word swap] 11: (4) (3) (2) (1) [Byte - word swap]
0	BMS	0	R/W	Buffer Mode 0: Frame buffer mode 1: Line buffer mode

Note: Bits other than SWAP can be modified only when the DSP bit in JCMOD is 1 (decoding process).

43.2.31 JPEG Interface Decode Source Address Register 1 (JIFDSA1)

JIFDSA1 sets the source address of the coded data. Set the start address of the coded data in 8-pixel units.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DSA1[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DSA1[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	DSA1[31:3]	H'0000 0000	R/W	Coded data source address (in 8-pixel units)
2 to 0	DSA1[2:0]		R	The lower three bits should be set to 0.

43.2.32 JPEG Interface Decode Source Address Register 2 (JIFDSA2)

JIFDSA2 sets the source address of the coded data. Set the start address in 8-pixel units. The source address of the coded data, which is used by the JPU, changes automatically every time the data transfer specified by JIFDDRSZ is completed: JIFDSA1 → JIFDSA2 → JIFDSA1 → . . . . (This register is valid only in auto-reload mode.)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DSA2[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DSA2[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	DSA2[31:3]	H'0000 0000	R/W	Coded data source address (in 8-pixel units)
2 to 0	DSA2[2:0]		R	The lower three bits should be set to 0.

43.2.33 JPEG Interface Decode Data Reload Size Register (JIFDDRSZ)

JIFDDRSZ sets the number of data (256-byte units) transferred before the address is changed (This register is valid only in auto reload mode).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	DDRSZ[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DDRSZ[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 8	DDRSZ[23:8]	H'00 0000	R/W	Number of data to be transferred before the address is changed (in 256-byte units)
7 to 0	DDRSZ[7:0]		R	The lower eight bits should be set to 0.

43.2.34 JPEG Interface Decode Destination Memory Width Register (JIFDDMW)

JIFDDMW sets the memory width of the data written to the external buffer (see 43.3.3, Storing Image Data).

Set this register in 8-pixel units. The maximum settable size is 4092 pixels and the minimum is 16 pixels. Sizes outside of this range should not be set

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DDMW[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DDMW[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	DDMW[31:3]	H'0000 0000	R/W	Memory width of image data stored in external buffer (in 8-pixel units)
2 to 0	DDMW[2:0]		R	The lower three bits should be set to 0.

43.2.35 JPEG Interface Decode Destination Vertical Size Register (JIFDDVSZ)

JIFDDVSZ indicates the vertical size of the image written to the external buffer.

This register is valid only in decoding. Treat the image size as an error if the size exceeds the processable size.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DDVSZ[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 0	DDVSZ [15:0]	H'0000	R	Vertical size of image written to external buffer After the JPEG coded data is analyzed, the values of JCVSZU and JCVSZD are automatically set to these bits in 4-pixel units.

43.2.36 JPEG Interface Decode Destination Horizontal Size Register (JIFDDHSZ)

JIFDDHSZ indicates the horizontal size of the image written to the external buffer. This register is valid only in decoding. Treat the image size as an error if the size exceeds the processable size.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DDHSZ[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 0	DDHSZ [15:0]	H'0000	R	Horizontal size of image written to external buffer After the JPEG coded data is analyzed, the values of JCHSZU and JCHSZD are automatically set to these bits in 4-pixel units.

43.2.37 JPEG Interface Decode Destination Y Address Register 1 (JIFDDYA1)

JIFDDYA1 sets the destination address of the Y component. Set the address in 8-pixel units.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DDYA1[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DDYA1[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	DDYA1[31:3]	H'0000 0000	R/W	Y component destination address (in 8-pixel units)
2 to 0	DDYA1[2:0]		R	The lower three bits should be set to 0.

43.2.38 JPEG Interface Decode Destination C Address Register 1 (JIFDDCA1)

JIFDDCA1 sets the destination address of the C component. Set the address in 8-pixel units.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DDCA1[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DDCA1[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	DDCA1[31:3]	H'0000 0000	R/W	C component destination address (in 8-pixel units)
2 to 0	DDCA1[2:0]		R	The lower three bits should be set to 0.

43.2.39 JPEG Interface Decode Destination Y Address Register 2 (JIFDDYA2)

JIFDDYA2 sets the destination address of the Y component. This register is valid only in line buffer mode.

Set the address in 8-pixel units. The destination address of the Y component, which is used by the JPU, changes automatically every time the data transfer specified by JIFDDRSZ is completed: JIFDDYA1 → JIFDDYA2 → JIFDDYA1 → . . . .

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DDYA2[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DDYA2[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	DDYA2[31:3]	H'0000 0000	R/W	Y component destination address (in 8-pixel units)
2 to 0	DDYA2[2:0]		R	The lower three bits should be set to 0.

43.2.40 JPEG Interface Decode Destination C Address Register 2 (JIFDDCA2)

JIFDDCA2 sets the destination address of the C component. This register is valid only in line buffer mode.

Set the address in 8-pixel units. The destination address of the C component, which is used by the JPU changes automatically every time the data transfer specified by JIFDDRSZ is completed: JIFDDCA1 → JIFDDCA2 → JIFDDCA1 → . . . .

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DDCA2[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DDCA2[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	DDCA2[31:3]	H'0000 0000	R/W	C Component Destination Address (in 8-pixel units)
2 to 0	DDCA2[2:0]		R	The lower three bits should be set to 0.

43.3 Operation

43.3.1 Encoding

(1) Overview of Processing

The encoding process flows are described below.

(a) Frame Buffer Mode

1. One frame of image data is transferred to the external buffer.
2. The JPEG core is activated.
   A marker is output. (After a marker is output, image data can be input.)
   Approximately 30000 cycles (necessary for making SOI to SOS markers) in normal mode
   Approximately 300 cycles (necessary for making SOS marker) in marker skip mode
3. Image data is transferred in MCUs from the external buffer to the JPU.
4. Image data is input to the JPEG core.
   The input data is processed in MCUs at any time in the JPEG core, and encoded data is output.
5. An interrupt is generated after frame data is processed completely.
   An interrupt is generated after the specified amount of data is reloaded in reload mode.

(b) Line Buffer Mode

1. The JPEG core is activated.
   A marker is output. (After a marker is output, image data can be input.)
   Approximately 30000 cycles (necessary for making SOI to SOS markers) in normal mode
   Approximately 300 cycles (necessary for making SOS marker) in marker skip mode
2. Y and C components of the image data are transferred to the external line buffer: Y components in multiples of 8 lines and C components in multiples of 8 lines (YCbCr 4:2:2), or Y components in multiples of 16 lines and C components in multiples of 8 lines (YCbCr 4:2:0).
   After transfer has been completed, a transfer end command is issued to the JPU.
   Every time the transfer to the external buffer is completed, a transfer end command is issued to the JPU.
3. Image data is transferred in MCUs from the external buffer to the JPU.
4. Image data is input to the JPEG core.
   The input data is processed in MCUs at any time in the JPEG core, and the encoded data is output.

5. After the JPU has read one external line buffer of the image data, the rest of the image data is transferred to the external line buffer.

   After all of the image data is transferred, a transfer end command is issued to the JPU (go to step 3).
6. After specified frame data processing is completed, an interrupt is generated.

   An interrupt is generated after the specified amount of data is reloaded in reload mode.

(2) Frame Buffer Mode (Encoding)

After the initial settings are completed, input image data in the external buffer and activate the JPU by setting the JSRT bit in JCCMD to B'1. After the JPU has been activated, the JPEG markers (SOI to SOS) are generated and output. It takes approximately 30000 cycles to generate the markers.

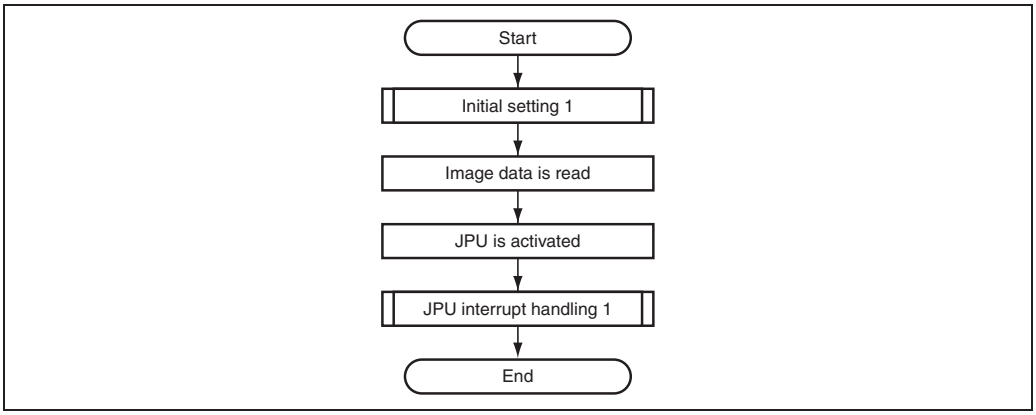


Figure 43.2 Flow of Encoding in Frame Buffer Mode

After a reset, set all necessary registers before the JPU is activated.

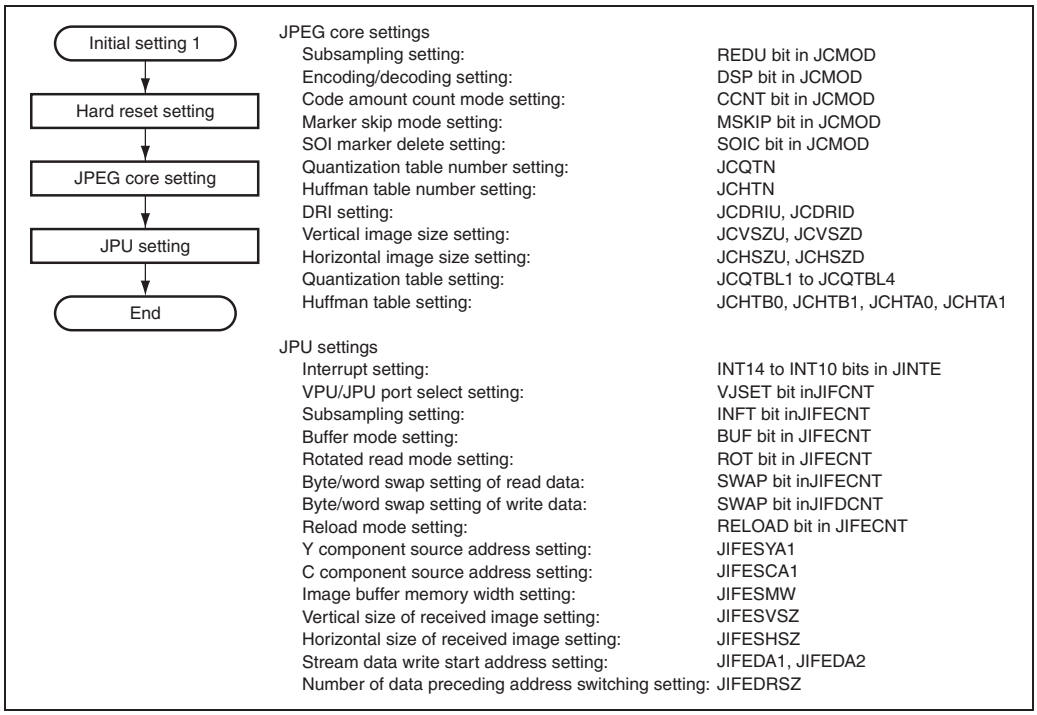


Figure 43.3 Flow of Initial Setting 1

Figure 43.4 shows the interrupt handling flow in frame buffer mode (encoding). When multiple interrupts occur (also when multiple interrupts that are not shown in figure 43.4 occur), process all interrupt sources.

- When the INS6 bit in the interrupt status register JINTS is set to B'1, the JPEG encoding has been completed. Though the JPU continues processing since the coded data to be transferred remains, the INS10 bit will be set to B'1 after the last coded data is transferred. The signal asserted by this interrupt source cannot be negated by clearing the corresponding interrupt status bit to 0. Issue an interrupt signal clear command (set the JEND bit in JCCMD to B'1) to clear the interrupt signal.

- When the INS10 bit in the interrupt status register JINTS is set to B'1, all coded data has been transferred and the JPU has completed encoding; transfer the coded data outside the JPU. When reload mode is set, transfer the rest of the coded data. When the total size of the coded data transferred to the reload buffer matches the number of the coded data set by the JIFEDRSZ, bits INS10 and INS13 are simultaneously set to B'1. This interrupt occurs when the INT10 bit in the interrupt enable register JINTE is set to B'1.
- In encoding with reload mode, when the INS13 bit in the interrupt status register JINTS is set to B'1, it indicates that the number of coded data set by the JIFDDRSZ have been transferred. When the first interrupt occurs, transfer the coded data stored in the reload buffer to the other memory area. When the second and subsequent interrupts occur, transfer the coded data and set a command for restarting transfer to the reload buffer.

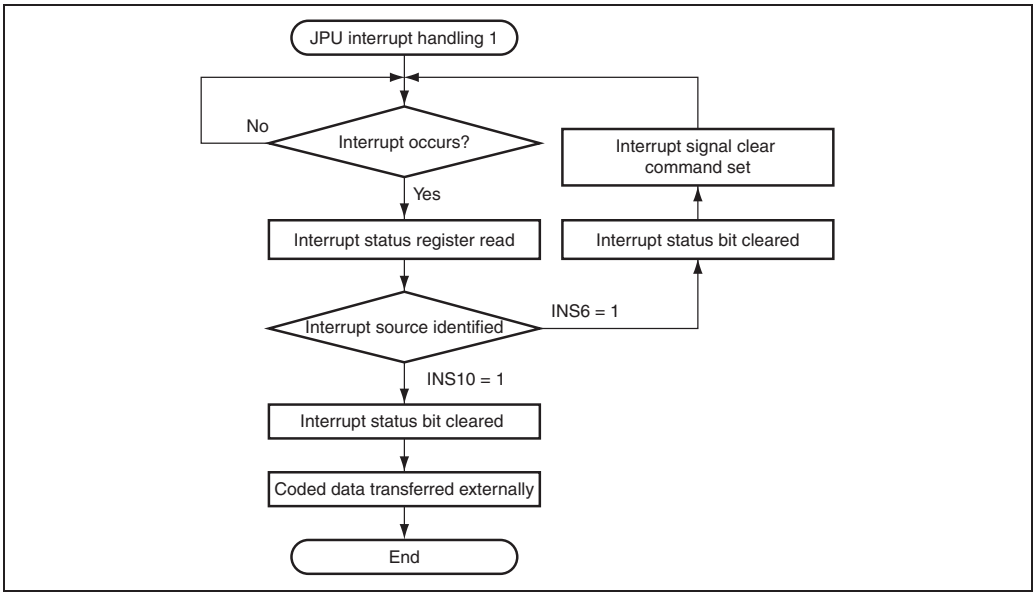


Figure 43.4 Flow of JPU Interrupt Handling 1 in Encoding

(3) Line Buffer Mode (Encoding)

After the initial settings are completed, activate the JPU by setting the JSRT bit in JCCMD to B'1. After the JPU has been activated, the JPEG markers (SOI to SOS) are generated and output. It takes approximately 30000 cycles to generate the markers. After the image data is stored in the external buffer and a line buffer write end command is issued, the JPU loads the image data from the external buffer and starts encoding it.

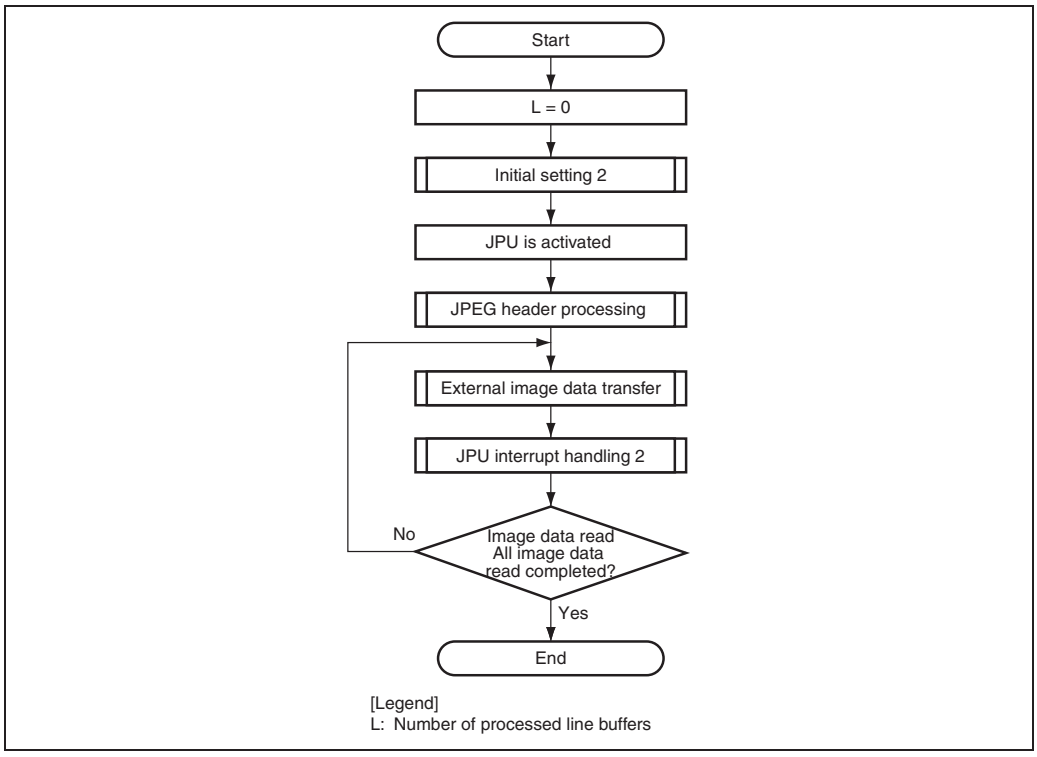
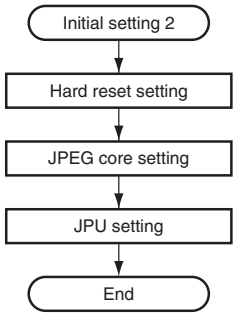


Figure 43.5 Flow of Encoding in Line Buffer Mode

After a reset, set all necessary registers before the JPU is activated.



JPEG core settings

Subsampling setting:	REDU bit in JCMOD
Encoding/decoding setting:	DSP bit in JCMOD
Code amount count mode setting:	CCNT bit in JCMOD
Marker skip mode setting:	MSKIP bit in JCMOD
SOI marker delete setting:	SOIC bit in JCMOD
Quantization table number setting:	JCQTN
Huffman table number setting:	JCHTN
DRI setting:	JCDRIU, JCDRID
Vertical image size setting:	JCVSZU, JCVSZD
Horizontal image size setting:	JCHSZU, JCHSZD
Quantization table setting:	JCQTBL1 to JCQTBL4
Huffman table setting:	JCHTB0, JCHTB1, JCHTA0, JCHTA1

JPU settings

Interrupt setting:	INT14 to INT10 bits in JINTE
VPU/JPU port select setting:	VJSET bit in JIFCNT
Subsampling setting:	INFT bit in JIFECNT
Buffer mode setting:	BUF bit in JIFECNT
Rotated read mode setting:	ROT bit in JIFECNT
Byte/word swap setting of read data:	SWAP bit in JIFECNT
Byte/word swap setting of write data:	SWAP bit in JIFDCNT
Reload mode setting:	RELOAD bit in JIFECNT
Processing unit setting:	PU bit in JIFECNT
Y component source address setting:	JIFESYA1, JIFESYA2
C component source address setting:	JIFESCA1, JIFESYA2
Image buffer memory width setting:	JIFESMW
Vertical size of received image setting:	JIFESVSZ
Horizontal size of received image setting:	JIFESHSZ
Stream data write start address setting:	JIFEDA1, JIFEDA2
Number of data preceding address switching setting:	JIFEDRSZ

Figure 43.6 Flow of Initial Setting 2

In line buffer mode, set the line buffer processing restart command after activating the JPU. Transferring the image data to the line buffer can be done before the JPU is activated. Two line buffers are provided: one for the data to be output to the JPU and the other for the data to be transferred from the external modules. Thus, transfer the image data to the line buffer after confirming that the data stored in the buffer for outputting data to the JPU has been transferred to the JPU through interrupts.

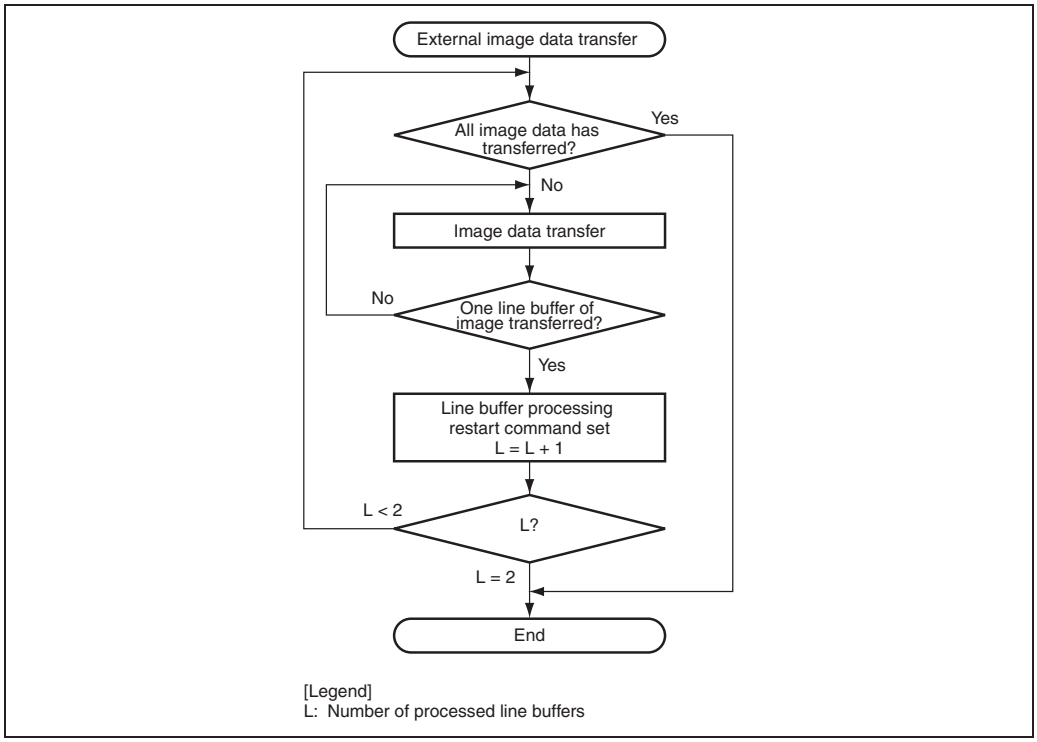


Figure 43.7 Flow of External Image Data Transfer

When multiple interrupts occur (also when multiple interrupts that are not shown in figure 43.8 occur), process all interrupt sources.

- When the INS12 bit or INS11 bit in the interrupt status register JINTS is set to B'1, the transfer of one line buffer of image data has been completed. Thus transfer new data to the line buffer. This interrupt occurs when the INT12 or INT11 bit in the interrupt enable register JINTE is set to B'1.
- When the INS6 bit in the interrupt status register JINTS is set to B'1, the JPEG encoding has been completed. Though the JPU continues processing since coded data to be transferred remains, the INS10 bit will be set to B'1 after the last coded data is transferred. The signal which is asserted by this interrupt source cannot be negated by clearing the corresponding interrupt status bit to 0. Issue an interrupt signal clear command (set the JEND bit in JCCMD to B'1) to negate the interrupt signal.

- When the INS10 bit in the interrupt status register JINTS is set to B'1, all coded data has been transferred and the JPU has completed encoding; transfer the coded data outside the JPU. When reload mode is set, transfer the rest of the coded data. When the total size of the coded data transferred to the reload buffer matches the number of coded data set by JIFEDRSZ, bits INS10 and INS13 are simultaneously set to B'1. This interrupt occurs when the INT10 bit in the interrupt enable register JINTE is set to B'1.
- In encoding with reload mode, when the INS13 bit in the interrupt status register JINTS is set to B'1, it indicates that the number of coded data set by JIFDDRSZ have been transferred. When the first interrupt occurs, transfer the coded data stored in the reload buffer to the other memory area. When the second and subsequent interrupts occur, transfer the coded data and set a command for restarting transfer to the reload buffer.

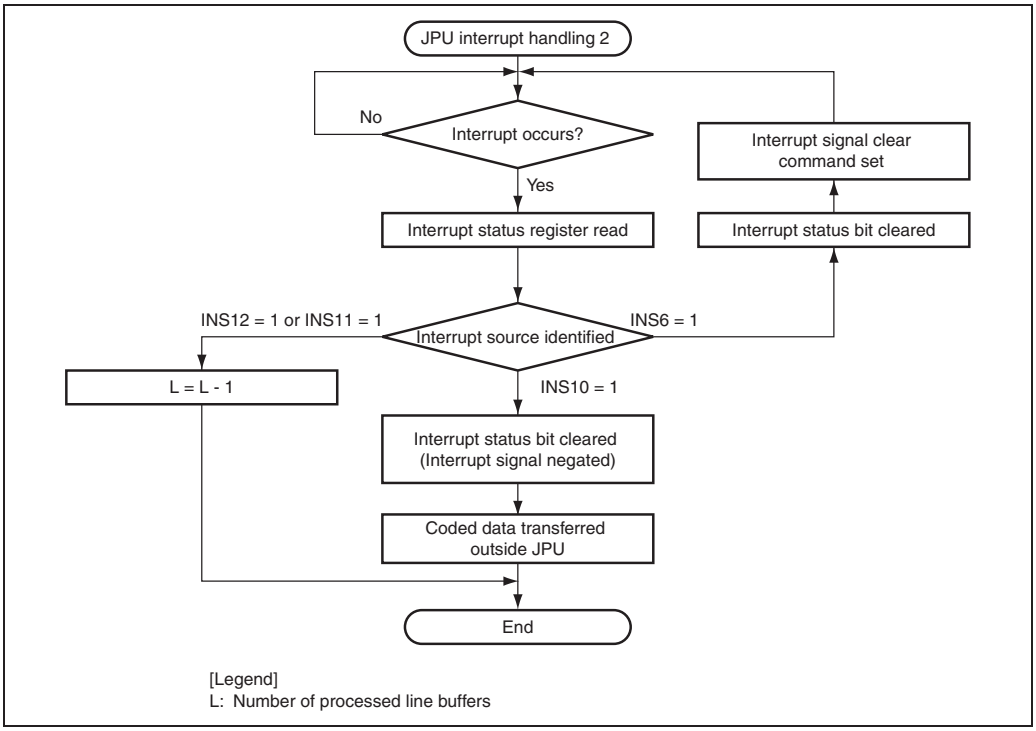


Figure 43.8 Flow of JPU Interrupt Handling 2

(4) JPEG Coded Data Format

Figure 43.9 shows the data output stream in encoding. The amount of coded data from SOI to EOI is indicated by the JCDTCU, JCDTCM, and JCDTCD registers. When the JCDRIU and JCDRID registers are set to H'0000 0000, the following markers are not output.

- DRI marker
- RST marker (in encoded image data)

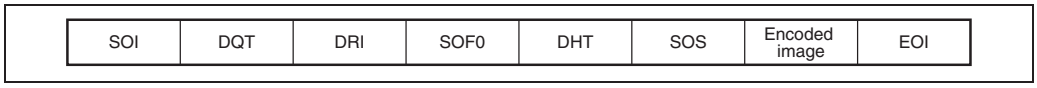


Figure 43.9 JPEG Coded Data Format

DQT: Not output for unused table

DHT: Output in order DC0, AC, DC1, and AC1. Not output for unused table.

SOF0: Component identifiers are C1 = first component, C2 = second component, and C3 = third component

SOS: Scan component selectors are CS1 = first component, CS2 = second component, and CS3 = third component

Header Volume (Reference)

- SOI: 2 bytes (FFD8)
- DQT: 134 bytes when two quantization tables are used, 199 bytes when three quantization tables are used (±65 bytes/table increase or decrease)
- DRI: 6 bytes
- SOF0: 19 bytes (4:2:2)
- DHT: 420 bytes (two tables are used)
- SOS: 14 bytes (4:2:2)
- EOI: 2 bytes (FFD9)

(a) JPEG Coded Data Format when Marker Skip Mode is Set

When MSKIP bits in JCMOD are set to B'01, SOI to DHT markers are not output. The RST marker output depends on the settings of the DRI upper and DRI lower registers. The amount of coded data from SOS to EOI is indicated by the JCDTCU, JCDTCM, and JCDTCD registers.

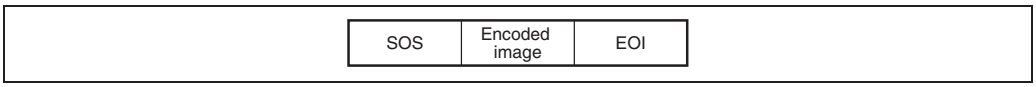


Figure 43.10 JPEG Coded Data Format when Marker Skip Mode is Set

(b) JPEG Coded Data Format when SOI Marker is Deleted

When the SOIC bit in JCMOD is set to B'1, the SOI marker is not output. This setting is valid when marker skip mode is not set. The amount of coded data from DQT to EOI equals the value indicated by JCDTCU, JCDTCM, and JCDTCD – 2.

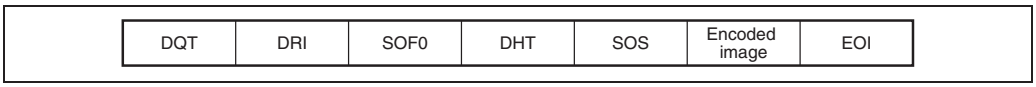


Figure 43.11 JPEG Coded Data Format when SOI Marker is Deleted

(c) Outputting End of JPEG Coded Data

The JPU transfers data as it ends at a 16-byte boundary. When the end of the coded data (the EOI marker) is not placed at the 16-byte boundary, H'FF is inserted into the data and the JPU outputs it. An H'FF byte is not included in the amount of the coded data indicated by the JCDTCU, JCDTCM, and JCDTCD registers.

(5) Code Amount Count Mode

In this mode, only the amount of coded data is counted. In encoding, set the CCNT bit in JCMOD to B'1 and enable reload mode, and set the JIFEDRSZ register (the number of data before the target address is switched) to 0; thus, the JPEG coded data is not output.

(6) Table Setting

(a) Quantization Table Specification

The order of addresses shown in 8 × 8 blocks corresponds to that of the register addresses. Do not access this table while the JPU is in processing.

Table 43.3 Quantization Table

00	01	02	03	04	05	06	07
08	09	0A	0B	0C	0D	0E	0F
10	11	12	13	14	15	16	17
18	19	1A	1B	1C	1D	1E	1F
20	21	22	23	24	25	26	27
28	29	2A	2B	2C	2D	2E	2F
30	31	32	33	34	35	36	37
38	39	3A	3B	3C	3D	3E	3F

JCQTBL0 (H'FE99 0000) = H'0001 0203
JCQTBL0 (H'FE99 0004) = H'0405 0607
:
JCQTBL0 (H'FE99 003C) = H'3C3D 3E3F

(b) Huffman Table Specification

Examples of the Huffman table specification given in the ITU-T T81 Annex K.3.3 recommended by JPEG are shown below. In encoding, the following settings must be specified for all codes so that Huffman codes can be generated for all group numbers.

- DC Huffman table: The number of codes for each code length is 12 codes.
  The group numbers in order of frequency of occurrence are 12.
- AC Huffman table: The number of codes for each code length is 162 codes.
  The zero run length/the group numbers in order of frequency of occurrence are 162.

Do not access the following tables while the JPU is in processing.

- Table K.3/T81
  JCHTBD0 (H’FE99 0100) = H'0001 0501
  JCHTBD0 (H’FE99 0104) = H'0101 0101
  JCHTBD0 (H’FE99 0108) = H'0100 0000
  JCHTBD0 (H’FE99 010C) = H'0000 0000
  JCHTBD0 (H’FE99 0110) = H'0001 0203
  JCHTBD0 (H’FE99 0114) = H'0405 0607
  JCHTBD0 (H’FE99 0118) = H'0809 0A0B

- Table K.4/T81
  JCHTBD1 (H’FE99 0200) = H'0003 0101
  JCHTBD1 (H’FE99 0204) = H'0101 0101
  JCHTBD1 (H’FE99 0208) = H'0101 0100
  JCHTBD1 (H’FE99 020C) = H'0000 0000
  JCHTBD1 (H’FE99 0210) = H'0001 0203
  JCHTBD1 (H’FE99 0214) = H'0405 0607
  JCHTBD1 (H’FE99 0218) = H'0809 0A0B

- Table K.5/T81
  JCHTBA0 (H’FE99 0120) = H'0002 0103
  JCHTBA0 (H’FE99 0124) = H'0302 0403
  JCHTBA0 (H’FE99 0128) = H'0505 0404
  JCHTBA0 (H’FE99 012C) = H'0000 017D
  JCHTBA0 (H’FE99 0130) = H'0102 0300
  JCHTBA0 (H’FE99 0134) = H'0411 0512
  JCHTBA0 (H’FE99 0138) = H'2131 4106
  JCHTBA0 (H’FE99 013C) = H'1351 6107
  JCHTBA0 (H’FE99 0140) = H'2271 1432
  JCHTBA0 (H’FE99 0144) = H'8191 A108
  :
  JCHTBA0 (H’FE99 01C0) = H'E3E4 E5E6
  JCHTBA0 (H’FE99 01C4) = H'E7E8 E9EA
  JCHTBA0 (H’FE99 01C8) = H'F1F2 F3F4
  JCHTBA0 (H’FE99 01CC) = H'F5F6 F7F8
  JCHTBA0 (H’FE99 01D0) = H'F9FA 0000

- Table K.6/T81
  JCHTBA1 (H'FE99 0220) = H'0002 0102
  JCHTBA1 (H'FE99 0224) = H'0404 0304
  JCHTBA1 (H'FE99 0228) = H'0705 0404
  JCHTBA1 (H'FE99 022C) = H'0001 0277
  JCHTBA1 (H'FE99 0230) = H'0001 0203
  JCHTBA1 (H'FE99 0234) = H'1104 0521
  JCHTBA1 (H'FE99 0238) = H'3106 1241
  JCHTBA1 (H'FE99 023C) = H'5107 6171
  JCHTBA1 (H'FE99 0240) = H'1322 3281
  JCHTBA1 (H'FE99 0244) = H'0814 4291
  :
  JCHTBA1 (H'FE99 02C0) = H'E2E3 E4E5
  JCHTBA1 (H'FE99 02C4) = H'E6E7 E8E9
  JCHTBA1 (H'FE99 02C8) = H'EAF2 F3F4
  JCHTBA1 (H'FE99 02CC) = H'F5F6 F7F8
  JCHTBA1 (H'FE99 02D0) = H'F9FA 0000

(7) Rotated Read Mode Setting

In encoding with frame buffer mode, image rotation processing can be performed (set the ROT bit in JIFECNT). When this processing is specified, set the source addresses shown in figure 43.12 in the JIFESYA1 and JIFECYA1 registers.

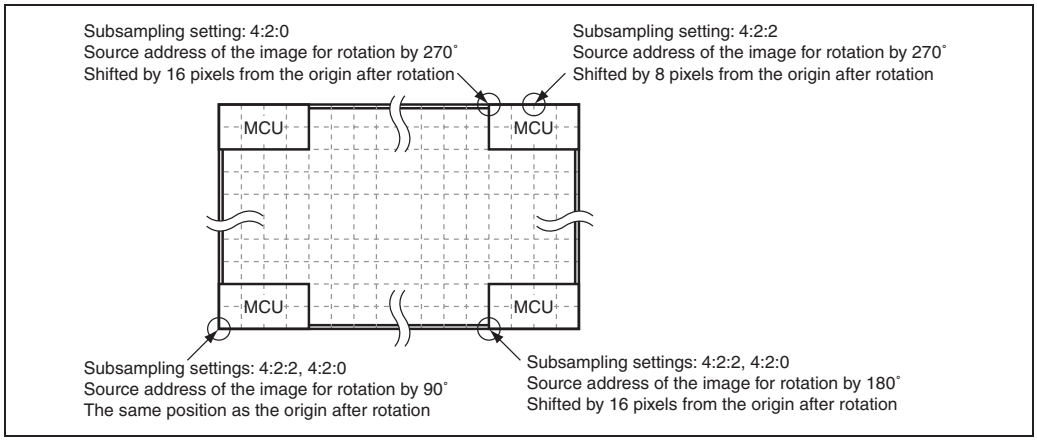


Figure 43.12 Position of Source Addresses for Rotation

43.3.2 Decoding

(1) Overview of Processing

The decoding process flows are described below.

(a) Frame Buffer Mode

1. JPEG core processing (decoding)
   Interrupts are generated every time the specified amount of data has been reloaded in reload mode.
2. Decoding data and transferring
   One frame of data can be processed at anytime and transferred.
3. An interrupt is generated after all of the processing is completed.

(b) Line Buffer Mode

1. JPEG core processing (decoding)
   Interrupts are generated every time the specified amount of data has been reloaded in reload mode.
2. Decoding data and transferring
3. Y and C components of the decoded data are transferred to the external buffer: Y components in multiples of 8 lines and C components in multiples of 8 lines (YCbCr 4:2:2), or Y components in multiples of 16 lines and C components in multiples of 16 lines (YCbCr 4:2:0).
   Every time when the transfer to the external buffer is completed, a transfer end command is issued to the JPU.
4. An interrupt is generated after all of the processing is completed.

(2) Frame Buffer Mode (Decoding)

After the initial setting is completed, activate the JPU by setting the JSRT bit in JCCMD to B'1. After the JPU has been activated, it obtains the coded data from the external buffer and starts decoding it. When multiple interrupts occur (also when multiple interrupts that are not shown in figure 43.13 occur), process all interrupt sources.

- When the INS14 bit in the interrupt status register JINTS is set to B'1, the coded data in the reload buffer has been transferred. This interrupt occurs when the INT14 bit in the interrupt enable register JINTE is set to B'1.

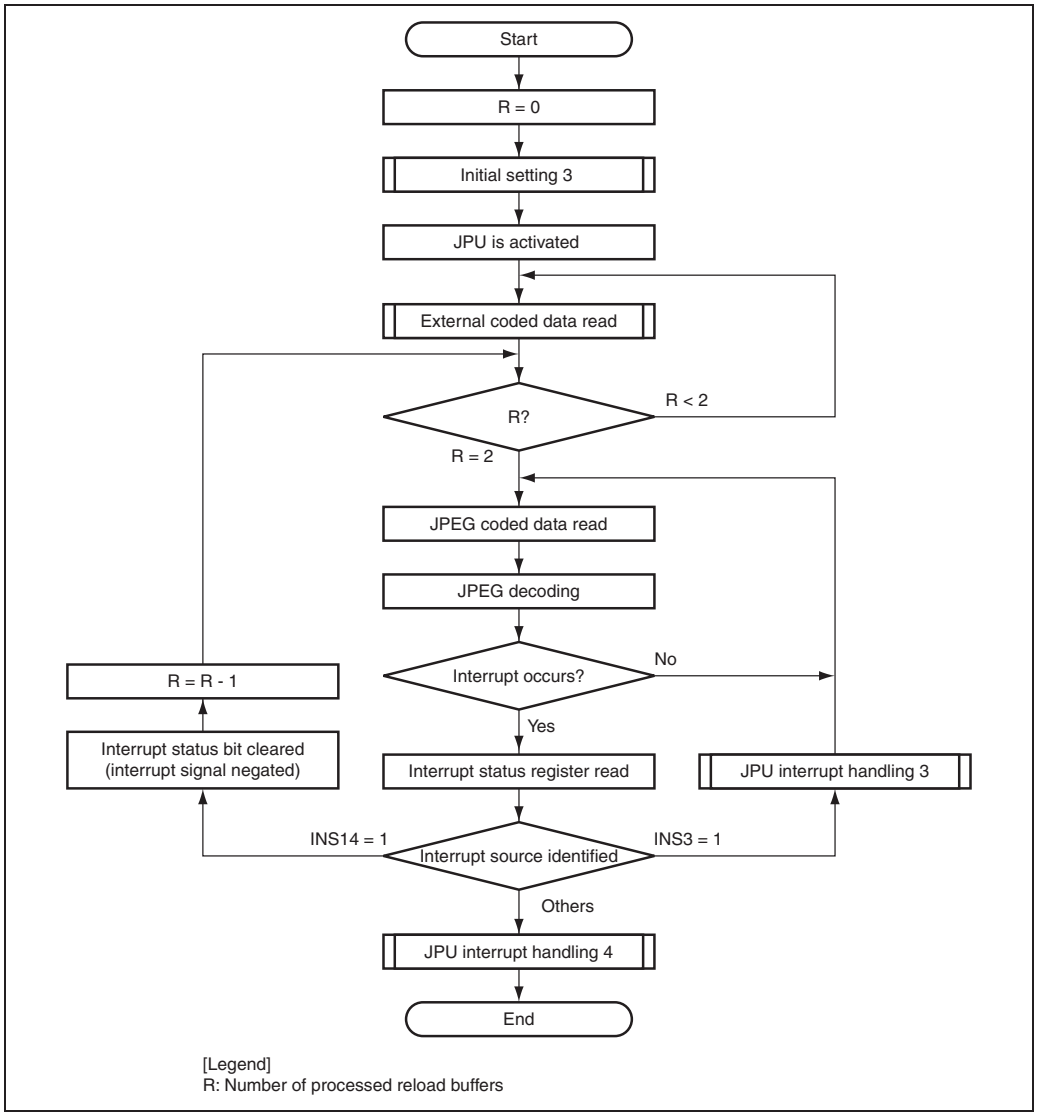


Figure 43.13 Flow of Decoding in Frame Buffer Mode

After a reset, set all necessary registers before the JPU is activated.

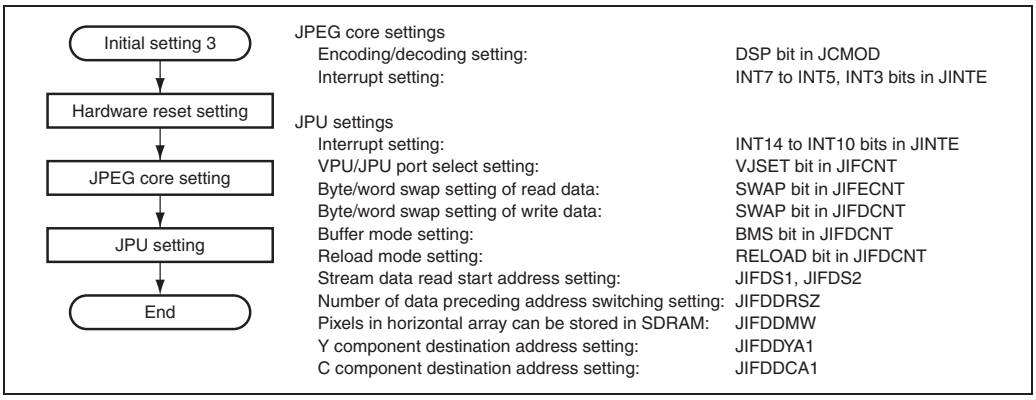


Figure 43.14 Flow of Initial Setting 3

Before the JPU is activated, prepare the coded data since the JPU starts reading the data immediately after being activated when reload mode is not set. If not all of the coded data is prepared, transfer the coded data to the buffer sequentially so that the JPU can read the data smoothly.

When reload mode is set, set a reload transfer write end command after the JPU is activated. The coded data can be transferred to the reload buffer before the JPU is activated. Two reload buffers are provided: one is used for the data to be output to the JPU and the other is for the data to be transferred from the external modules. Thus, transfer the data to the reload buffer after confirming that the data stored in the buffer used to output the data to the JPU has been transferred to the JPU through interrupts.

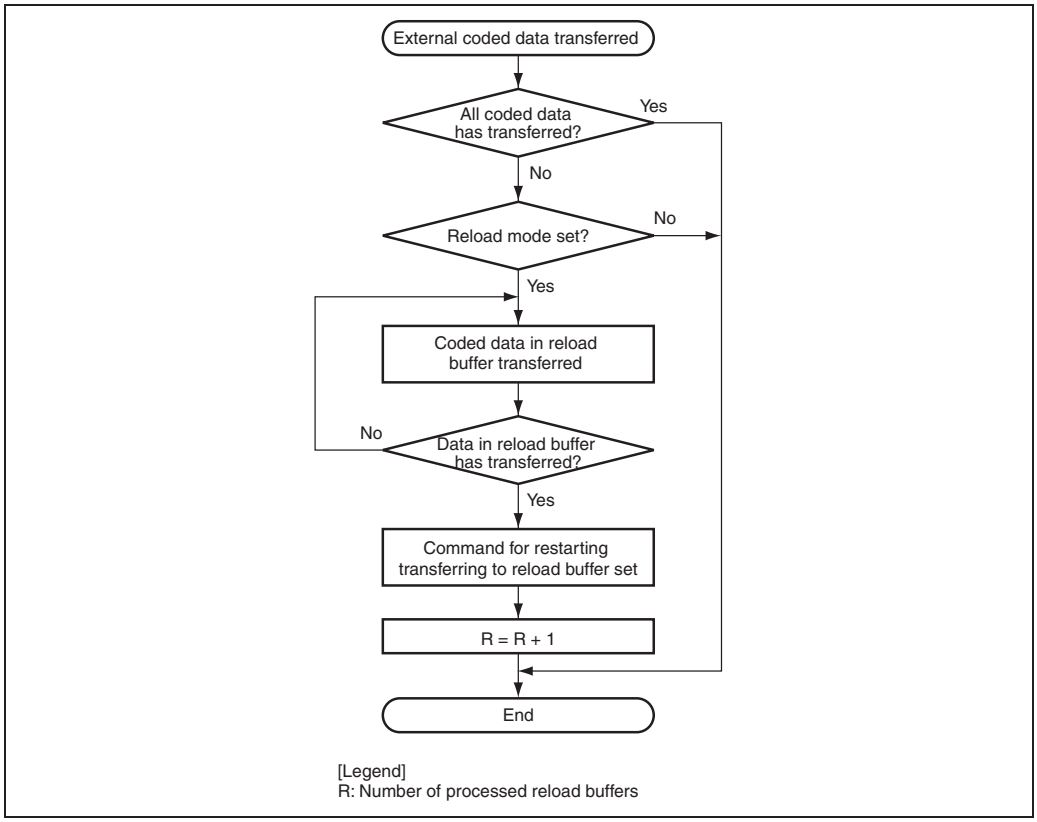


Figure 43.15 Flow of Transferring External Coded Data

When multiple interrupts occur (also when multiple interrupts that are not shown in figure 43.16 occur), process all interrupt sources.

- When the INS3 bit in the interrupt status register JINTS is set to B'1, the JPEG coded data is prepared and its image size and subsampling setting can be read. After reading of all necessary registers, set the command for revoking the processing-stopped state to resume decoding. This interrupt occurs when the INT3 bit in the interrupt enable register JINTE is set to B'1. The interrupt signal which is asserted by this interrupt source cannot be negated through clearing the corresponding interrupt status bit to 0. Issue an interrupt signal clear command (set the JEND bit in JCCMD to B'1) to clear the interrupt signal.

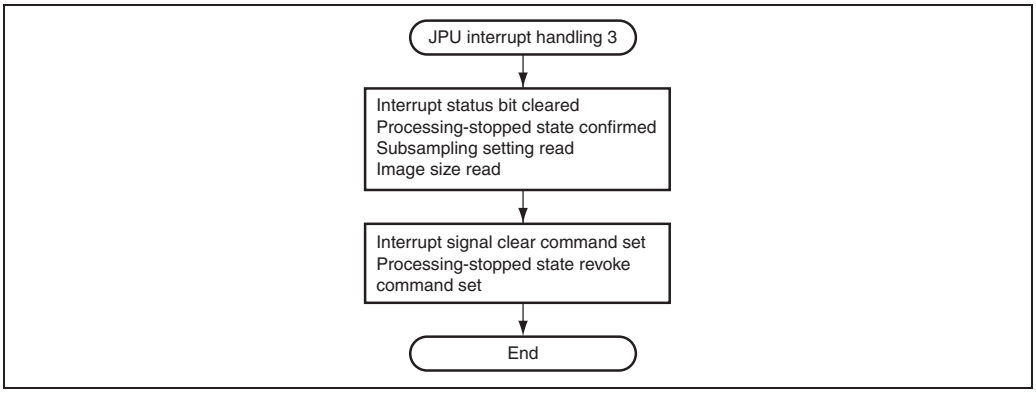


Figure 43.16 Flow of JPU Interrupt Handling 3

Figure 43.17 shows the interrupt handling flow in decoding. When multiple interrupts occur (also when multiple interrupts that are not shown in figure 43.17 occur), process all interrupt sources.

- When the INS5 bit in the interrupt status register JINTS is set to B'1, the input JPEG coded data has an error and the JPU stops the decoding process. Read ERR bits in JCDERR and identify its error source. The interrupt signal which is asserted by this interrupt source cannot be negated by clearing the corresponding interrupt status bit. Issue an interrupt signal clear command (set the JEND bit in JCCMD to B'1) to clear the interrupt signal.
- When the INS6 bit in the interrupt status register JINTS is set to B'1, the JPEG decoding process is completed. When the INS10 bit is set to B'1, all of the image data is transferred and JPU completes decoding. The interrupt signal which is asserted by this interrupt source cannot be negated by clearing the corresponding interrupt status bit. Issue an interrupt signal clear command (set the JEND bit in JCCMD to B'1) to clear the interrupt signal.

- When the INS10 bit in the interrupt status register JINTS is set to B'1, all of the image data has been transferred and the JPU has completed decoding; transfer the image data outside the JPU. This interrupt occurs when the INT10 bit in the interrupt enable register JINTE is set to B'1.

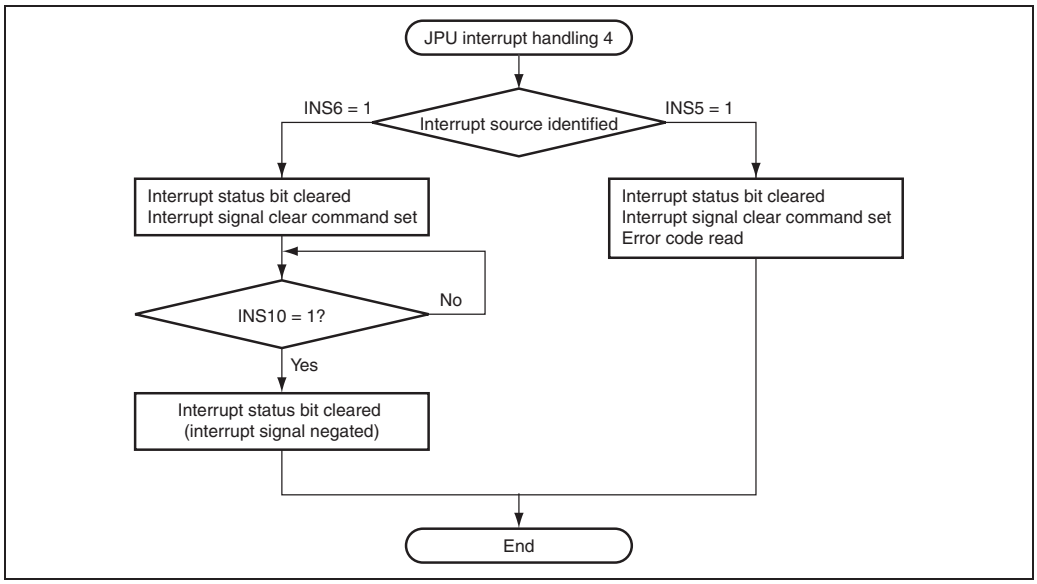


Figure 43.17 Flow of JPU Interrupt Handling 4

(3) Line Buffer Mode (Decoding)

After the initial settings are completed, activate the JPU by setting the JSRT bit in JCCMD to B'1. After the JPU has been activated, transfer the coded data to the external buffer. After the coded data has been stored in the external buffer, the JPU reads the data from the external buffer and starts decoding it.

When multiple interrupts occur (also when multiple interrupts that are not shown in figure 43.18 occur), process all interrupt sources.

- When the INS14 bit in the interrupt status register JINTS is set to B'1, the coded data in the reload buffer has been transferred. This interrupt occurs when the INT14 bit in the interrupt enable register JINTE is set to B'1.

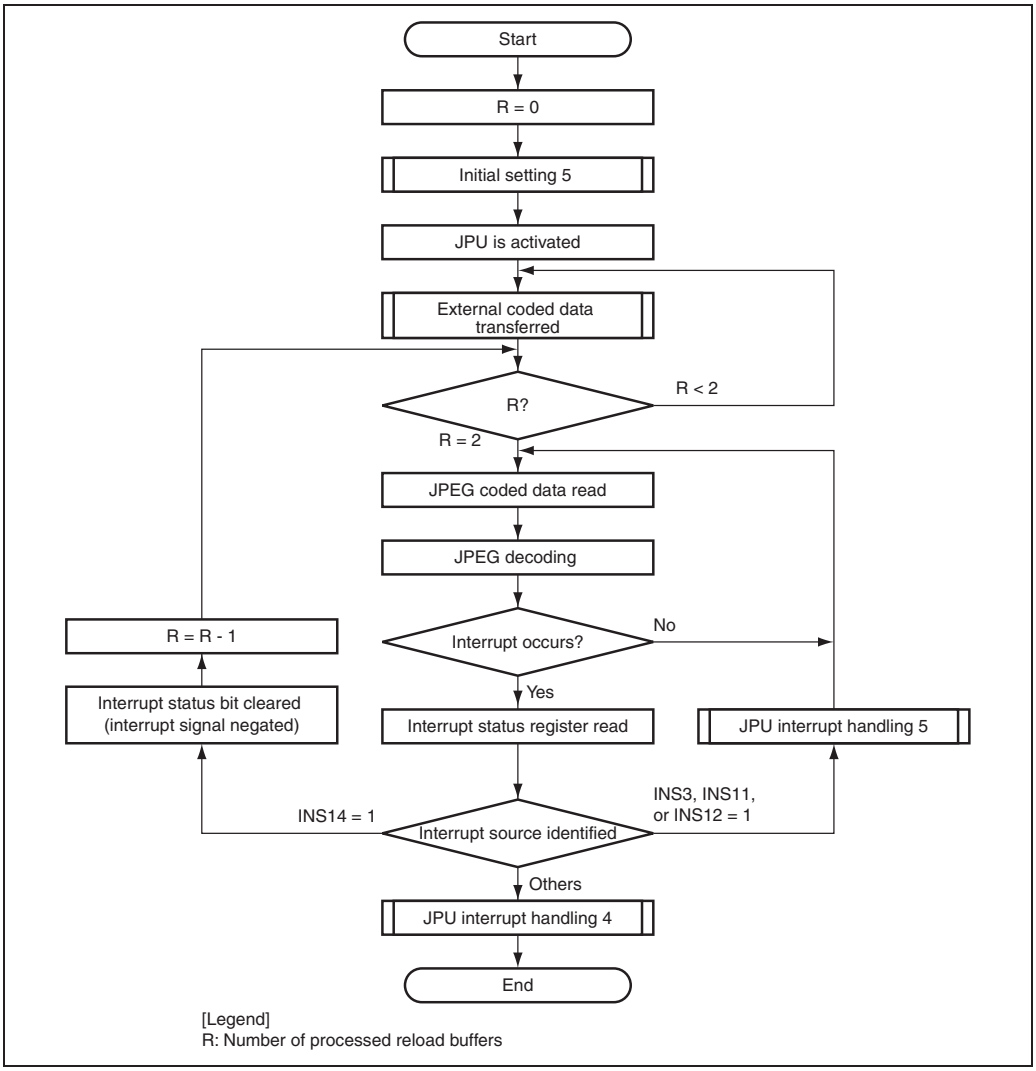


Figure 43.18 Flow of Decoding Process in Line Buffer Mode

After a reset, set all necessary registers before the JPU is activated.

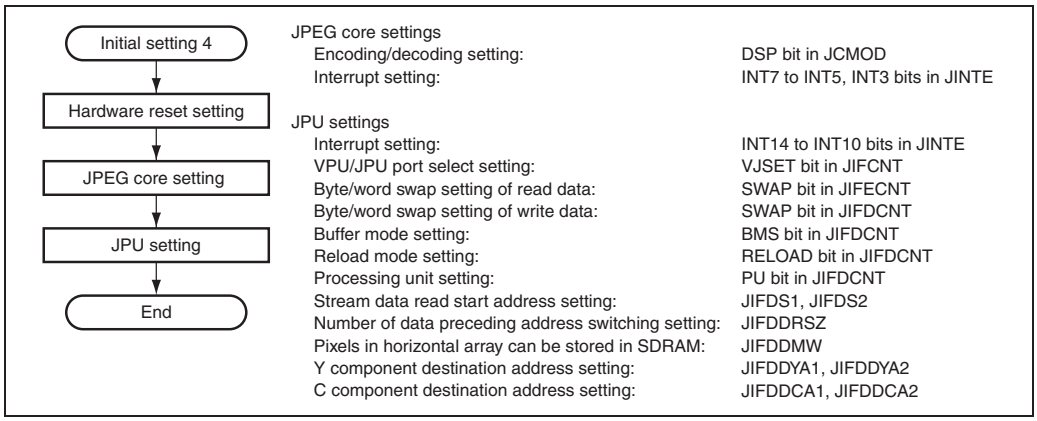


Figure 43.19 Flow of Initial Setting 4

When multiple interrupts occur (also when multiple interrupts that are not shown in figure 43.20 occur), process all interrupt sources.

- When the INS3 bit in the interrupt status register JINTS is set to B'1, the JPEG coded data is prepared and its image size and subsampling setting can be read. After reading all necessary registers, set the command for revoking the processing-stopped state to resume decoding. This interrupt occurs when the INT3 bit in the interrupt enable register JINTE is set to B'1. The interrupt signal which is asserted by this interrupt source cannot be negated by clearing the corresponding interrupt status bit to 0. Issue an interrupt signal clear command (set the JEND bit in JCCMD to B'1) to clear the interrupt signal.
- When the INS11 or INS12 bit in the interrupt status register JINTS is set to B'1, one line buffer of image data has been transferred. When the first interrupt occurs, transfer the image data stored in the line buffer to the other memory area. When the second and subsequent interrupts occur, transfer the image data and set a command for restarting transfer to the line buffer. This interrupt occurs when the INT11 or INT12 bit in the interrupt enable register JINTE is set to B'1.

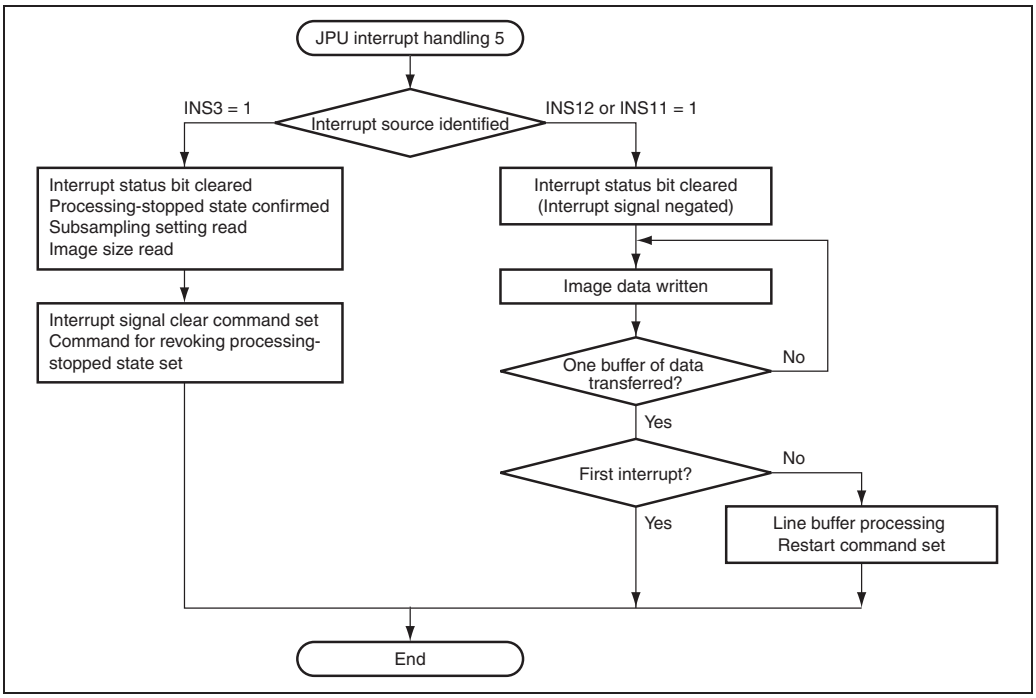


Figure 43.20 Flow of JPU Interrupt Handling 5

(4) Input JPEG Coded Data

Markers to be processed in decoding are SOS, SOF0, SOS, DQT, DHT, DRI, RSTm, and EOI. Other markers except for the error markers shown below are ignored even if they are read.

(5) JPEG Decoding Errors

(a) Error Marker

If an error marker is found while analyzing encoded data for decoding, identify the error type by the code and set the code (shown in table 43.4) to ERR bits in JCDERR. When an error is detected, the JPU generates an interrupt signal and stops decoding. The stored code is 1010 (default value) at the start of processing for the next frame or after a bus reset.

Table 43.4 Decoding Error Codes

Code	Description
0000	Normal
0001	SIO not detected: SIO not detected until EOI detected
0010	SOF1 to SOFF detected
0011	Subsampling setting other than YCbCr 4:4:4 (H = 1:1:1, V = 1:1:1)/YCbCr 4:2:2 (H = 2:1:1, V = 1:1:1)/YCbCr 4:1:1 (H = 4:1:1, V = 1:1:1)/YCbCr 4:2:0 (H = 2:1:1, V = 2:1:1) detected
0100	SOF accuracy error: Other than 8 detected
0101	DQT accuracy error: Other than 0 detected
0110	Component error 1: The number of SOF0 header components detected is other than 1, 3, or 4
0111	Component error 2: The number of components differs between SOF0 header and SOS
1000	SOF0, DQT, and DHT not detected when SOS detected
1001	SOS not detected: SOS not detected until EOI detected
1010	EOI not detected (default)
1011	Restart interval data number error detected
1100	Image size error detected
1101	Last MCU data number error detected
1110	Block data number error detected

(b) Huffman Coded Segment Error

In decoding, if it is determined that the increase or decrease in the number of data to be decoded is caused by an error such as bit inversion or a lack of data in the Huffman coded segment through analysis of the encoded data, the error type is identified and the error code is set in ERR bits in JCDFRR. When a necessary bit among INT7 to INT5 in JINTE is set to B'1, the error code is set and decoding is terminated by an interrupt signal generation. The code to be stored is 1010 (default value) at the start of processing for the next frame or after a bus reset.

In this error detection, an increase or decrease in the number of data to be decoded is detected; an error is not detected even when any other error occurs in the Huffman coded segment and the error does not cause an increase or decrease in the number of data to be decoded.

[Example]

The number of data in a Huffman coded segment with subsampling setting 4:2:2, DRI = 2, X = 80 pixels, and Y = 8 pixels

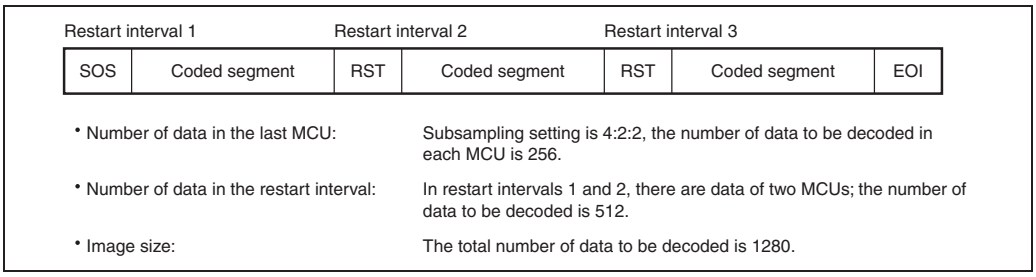


Figure 43.21 Huffman Coded Segment

Table 43.5 Segment Error Codes

Code	Description
0000	Normal
1011	Restart interval data number error: The number of data in each interval is compared with the number of data specified by the DRI marker. If an interval has more or less data that is specified by the DRI marker, the decoding error code (1011) is set. The last interval which is shorter than the restart interval is not compared. If the DRI marker segment is not placed or the specified number is 00, an error is not detected even if the RSTm marker is placed. Also an m which indicates the order of RSTm marker modulo 8 (m = 0 to 7) is exempt from the error detection analysis. When the INT7 bit in JINTE is set to B'0, this error is not detected.
1100	Image size error: The data number of an image which is calculated from the number of lines specified by the frame parameter and the number of samples per line is compared with the total number of data from SOS to EOI (in pixel units). If the numbers of data do not match, the decoding error code (1100) is set. When the INT6 bit in JINTE is set to B'0, this error is not detected. The data number of an image is shown in MCU units. Thus the number of lines and the number of samples per line need to be shown in MCU units.
1101	Last MCU data number error: Whether the number of data in the MCUs at the EOI detection is shown in MCU units is checked and fractions are detected. If error (1100) occurs simultaneously, error (1100) has priority. When the INT5 bit in JINTE is set to B'0, this error is not detected.
1110	Block data number error: Whether a block is an 8×8 array is checked; the check is performed for fractions. When bits INT7 to INT5 in JINTE are set to B'0, this error is not detected.

43.3.3 Storing Image Data

Storing the image data in the buffer and transferring the data to or from the JPU are described below.

(1) Frame Buffer Mode
(VGA: 640 × 480, Image data area ⇔ QVGA: Transferring image data 320 × 240)

- Example of register settings

	VGA → VGA
JIFESMW/JIFDDMW: H'0000 0280 (640)	H'0000 0280
JIFESYAI/JIFDDYAI: H'0001 2CA0 (76960)	H'0000 0000
JIFESHSZ/JIFDDHSZ: H'0000 0140 (320)	H'0000 0280
JIFESVSZ/JIFDDVSZ: H'0000 00F0 (240)	H'0000 01E0
JIFESCAI/JIFDDCA1: H'0005 DCA0 (384160)	H'0004 B000

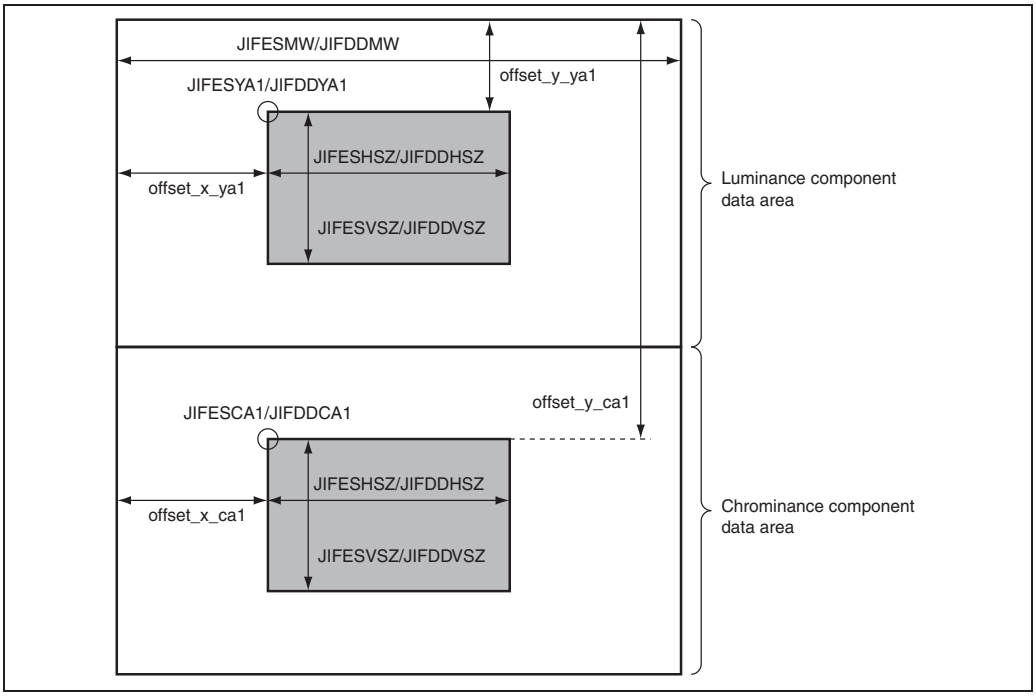


Figure 43.22 Data Allocation Image in Frame Buffer

(2) Storing Image Data

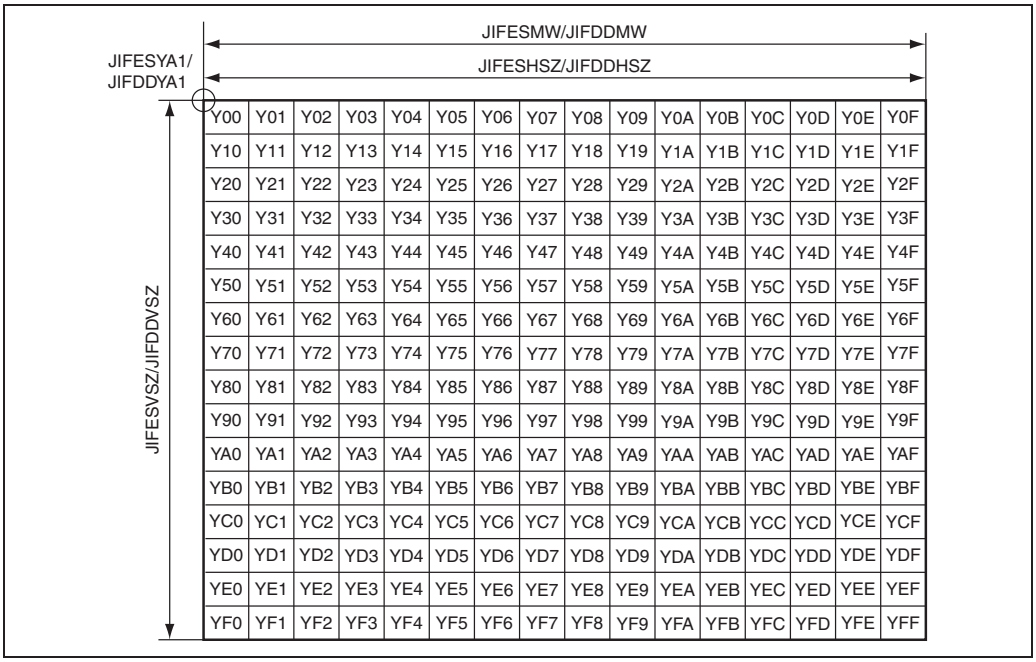
(a) Luminance component data

Specify JIFESYA1/JIFDDYA1 (JIFESYA2/JIFDDYA2) as the origin of the image. Transfer the data in the area specified by JIFESHSZ/JIFDDHSZ and JIFESVSZ/JIFDDVSZ.

- Register setting value:
  JIFESMW/JIFDDMW: H'0000 0010 (16)
  JIFESYA1/JIFDDYA1: H'0000 0000 (0)
  JIFESHSZ/JIFDDHSZ: H'0000 0010 (16)
  JIFESVSZ/JIFDDVSZ: H'0000 0010 (16)

- Data stored in buffer:
  H'0000 0000 = Y00, Y01, Y02, Y03
  H'0000 0004 = Y04, Y05, Y06, Y07
  H'0000 0008 = Y08, Y09, Y0A, Y0B
  H'0000 000C = Y0C, Y0D, Y0E, Y0F
  :
  H'0000 00F0 = YF0, YF1, YF2, YF3
  H'0000 00F4 = YF4, YF5, YF6, YF7
  H'0000 00F8 = YF8, YF9, YFA, YFB
  H'0000 00FC = YFC, YFD, YFE, YFF

- Transferring data to the JPU:
  Burst transfer is performed in 1-MCU units in the line direction. One line is 16 bytes.



Y00	Y01	Y02	Y03	Y04	Y05	Y06	Y07	Y08	Y09	Y0A	Y0B	Y0C	Y0D	Y0E	Y0F
Y10	Y11	Y12	Y13	Y14	Y15	Y16	Y17	Y18	Y19	Y1A	Y1B	Y1C	Y1D	Y1E	Y1F
Y20	Y21	Y22	Y23	Y24	Y25	Y26	Y27	Y28	Y29	Y2A	Y2B	Y2C	Y2D	Y2E	Y2F
Y30	Y31	Y32	Y33	Y34	Y35	Y36	Y37	Y38	Y39	Y3A	Y3B	Y3C	Y3D	Y3E	Y3F
Y40	Y41	Y42	Y43	Y44	Y45	Y46	Y47	Y48	Y49	Y4A	Y4B	Y4C	Y4D	Y4E	Y4F
Y50	Y51	Y52	Y53	Y54	Y55	Y56	Y57	Y58	Y59	Y5A	Y5B	Y5C	Y5D	Y5E	Y5F
Y60	Y61	Y62	Y63	Y64	Y65	Y66	Y67	Y68	Y69	Y6A	Y6B	Y6C	Y6D	Y6E	Y6F
Y70	Y71	Y72	Y73	Y74	Y75	Y76	Y77	Y78	Y79	Y7A	Y7B	Y7C	Y7D	Y7E	Y7F
Y80	Y81	Y82	Y83	Y84	Y85	Y86	Y87	Y88	Y89	Y8A	Y8B	Y8C	Y8D	Y8E	Y8F
Y90	Y91	Y92	Y93	Y94	Y95	Y96	Y97	Y98	Y99	Y9A	Y9B	Y9C	Y9D	Y9E	Y9F
YA0	YA1	YA2	YA3	YA4	YA5	YA6	YA7	YA8	YA9	YAA	YAB	YAC	YAD	YAE	YAF
YB0	YB1	YB2	YB3	YB4	YB5	YB6	YB7	YB8	YB9	YBA	YBB	YBC	YBD	YBE	YBF
YC0	YC1	YC2	YC3	YC4	YC5	YC6	YC7	YC8	YC9	YCA	YCB	YCC	YCD	YCE	YCF
YD0	YD1	YD2	YD3	YD4	YD5	YD6	YD7	YD8	YD9	YDA	YDB	YDC	YDD	YDE	YDF
YE0	YE1	YE2	YE3	YE4	YE5	YE6	YE7	YE8	YE9	YEA	YEB	YEC	YED	YEE	YEF
YF0	YF1	YF2	YF3	YF4	YF5	YF6	YF7	YF8	YF9	YFA	YFB	YFC	YFD	YFE	YFF

Figure 43.23 Luminance Data

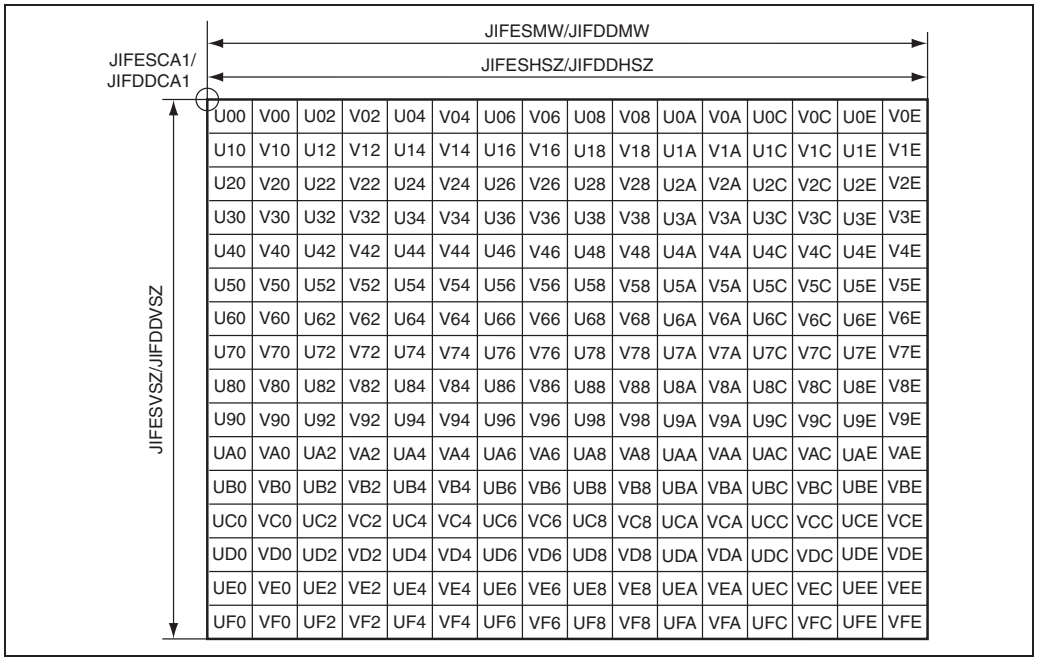
(b) Chrominance Component Data (Cb: U, Cr: V)

Specify JIFESCA1/JIFDDCA1 (JIFESCA2/JIFDDCA2) as the origin of the image, and transfer the data in the area specified by JIFESHSZ/JIFDDHSZ and JIFESVSZ/JIFDDVSZ.

- Register setting value:
  JIFESMW/JIFDDMW: H'0000 0010 (16)
  JIFESCA1/JIFDDCA1: H'0000 0100 (256)
  JIFESHSZ/JIFDDHSZ: H'0000 0010 (16)
  JIFESVSZ/JIFDDVSZ: H'0000 0010 (16)

- Data stored in buffer:
  H'0000 0010 = U00, V00, U02, V02
  H'0000 0104 = U04, V04, U06, V06
  H'0000 0108 = U08, V08, U0A, V0A
  H'0000 010C = U0C, V0C, U0E, V0E
  :
  H'0000 01F0 = UF0, VF0, UF2, VF2
  H'0000 01F4 = UF4, VF4, UF6, VF6
  H'0000 01F8 = UF8, VF8, UFA, VFA
  H'0000 01FC = UFC, VFC, UFE, VFE

- Transferring data to the JPU:
  Burst transfer is performed in 1-MCU units in the line direction. One line is 16 bytes.



U00	V00	U02	V02	U04	V04	U06	V06	U08	V08	U0A	V0A	U0C	V0C	U0E	V0E
U10	V10	U12	V12	U14	V14	U16	V16	U18	V18	U1A	V1A	U1C	V1C	U1E	V1E
U20	V20	U22	V22	U24	V24	U26	V26	U28	V28	U2A	V2A	U2C	V2C	U2E	V2E
U30	V30	U32	V32	U34	V34	U36	V36	U38	V38	U3A	V3A	U3C	V3C	U3E	V3E
U40	V40	U42	V42	U44	V44	U46	V46	U48	V48	U4A	V4A	U4C	V4C	U4E	V4E
U50	V50	U52	V52	U54	V54	U56	V56	U58	V58	U5A	V5A	U5C	V5C	U5E	V5E
U60	V60	U62	V62	U64	V64	U66	V66	U68	V68	U6A	V6A	U6C	V6C	U6E	V6E
U70	V70	U72	V72	U74	V74	U76	V76	U78	V78	U7A	V7A	U7C	V7C	U7E	V7E
U80	V80	U82	V82	U84	V84	U86	V86	U88	V88	U8A	V8A	U8C	V8C	U8E	V8E
U90	V90	U92	V92	U94	V94	U96	V96	U98	V98	U9A	V9A	U9C	V9C	U9E	V9E
UA0	VA0	UA2	VA2	UA4	VA4	UA6	VA6	UA8	VA8	UAA	VAA	UAC	VAC	UAE	VAE
UB0	VB0	UB2	VB2	UB4	VB4	UB6	VB6	UB8	VB8	UBA	VBA	UBC	VBC	UBE	VBE
UC0	VC0	UC2	VC2	UC4	VC4	UC6	VC6	UC8	VC8	UCA	VCA	UCC	VCC	UCE	VCE
UD0	VD0	UD2	VD2	UD4	VD4	UD6	VD6	UD8	VD8	UDA	VDA	UDC	VDC	UDE	VDE
UE0	VE0	UE2	VE2	UE4	VE4	UE6	VE6	UE8	VE8	UEA	VEA	UEC	VEC	UEE	VEE
UF0	VF0	UF2	VF2	UF4	VF4	UF6	VF6	UF8	VF8	UFA	VFA	UFC	VFC	UFE	VFE

Figure 43.24 Chrominance Data

43.3.4 Storing Coded Data

Storing the coded data in the buffer and transferring the coded data to or from the JPU are described below.

(1) Coded Data Sample: Coded length (SOI to EOI) is 592 bytes

Table 43.6 Coded Data Sample

ADDRESS	000102030405060708090A0B0C0D0E0F	101112131415161718191A1B1C1D1E1F
0000 00	FFD8FFDB008400100B0C0E0C0A100E0D	0E1211101318281A181616183123251D
0000 20	283A333D3C3933383740485C4E404457	453738506D51575F626768673E4D7179
0000 40	7064785C65676301111212181 5182F1A	1A2F6342384263636363636363636363
0000 60	6363636363636363636363636363636363	6363636363636363636363636363636363
0000 80	6363636363636363FFC000110801E002	800301210002110103110 1FFC401A200
0000 A0	000105010101010101000000000000000	000102030405060708090A0B10000201
0000 C0	030302040305050404000001 7D010203	000411051221314106135161072271 14
0000 E0	328191A1082342B1C11552D1F0243362	7282090A161718191A25262728292A34
0001 00	35363738393A434445464748494A5354	55565758595A636465666768696A7374
0001 20	75767778797A838485868788898A9293	9495969798999AA2A3A4A5A6A7A8A9AA
0001 40	B2B3B4B5B6B7B8B9BAC2C3C4C5C6C7C8	C9CAD2D3D4D5D6D7D8D9DAE1E2E3E4E5
0001 60	E6E7E8E9EAF1F2F3F4F5F6F7F8F9FA01	000301010101010101010000000000
0001 80	000102030405060708090A0B11000201	020404030407050404000102770001 02
0001 A0	031104052131061241510761711322 32	8108144291A1B1C109233352F0156272
0001 C0	D10A162434E125F11718191A26272829	2A35363738393A434445464748494A53
0001 E0	5455565758595A636465666768696A73	7475767778797A828384858687888 98A
0002 00	92939495969798999AA2A3A4A5A6A7A8	A9AAB2B3B4B5B6B7B8B9BAC2C3C4C5C6
0002 20	C7C8C9CAD2D3D4D5D6D7D8D9DAE2E3E4	E5E6E7E8E9EAF2F3F4F5F6F7F8F9FAFF
0002 40	DA000C03010002110311003F0000FFD9	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

(2) Transferring Data at the End of Coded Data

[Encoding]

Insert H'FF up to a 16-byte address boundary.

CC: Coded data, FF-D9: EOI markers

- CC-CC-FF-D9 Insert H'FF up to a 16-byte boundary
- CC-FF-D9-FF Insert H'FF up to a 16-byte boundary
- FF-D9-FF-FF Insert H'FF up to a 16-byte boundary

[Decoding]

- The JPU continues reading until the JPU core detects the EOI marker. The JPU may read other data in addition to coded data.

(3) Reload Mode Disabled

A way of storing the data is shown in table 43.6, Coded Data Sample.

- JIFEDA1/JIFDSA1: H'0000 0000

  As shown in table 43.6, Coded Data Sample, the address of coded data is incremented from the start and then stored.

- JIFEDA1/JIFDSA1: H'0000 0004

```
ADDRESS    000102030405060708090A0B0C0D0E0F   101112131415161718191A1B1C1D1E1F
0000 00    XXXXXXXXFFD8FFDB008400100B0C0E0C   0A100E0D0E1211101318281A18161618
0000 20    3123251D283A333D3C3933383740485C   4E404457453738506D51575F62676867
           :
0002 20    C3C4C5C6C7C8C9CAD2D3D4D5D6D7D8D9   DAE2E3E4E5E6E7E8E9EAF2F3F4F5F6F7
0002 40    F8F9FAFFDA000C030100021103110003F   0000FFD9FFFFFFFFFFFFFFFFFFFFFF
```

- JIFEDA1/JIFDSA1: H'0000 0008

```
ADDRESS    000102030405060708090A0B0C0D0E0F   101112131415161718191A1B1C1D1E1F
0000 00    XXXXXXXXXXXXXXXXFFD8FFDB00840010   0B0C0E0C0A100E0D0E1211101318281A
0000 20    181616183123251D283A333D3C393338   3740485C4E404457453738506D51575F
           :
0002 20    B8B9BAC2C3C4C5C6C7C8C9CAD2D3D4D5   D6D7D8D9DAE2E3E4E5E6E7E8E9EAF2F3
0002 40    F4F5F6F7F8F9FAFFDA000C0301000211   0311003F0000FFD9FFFFFFFFFFFFFFFF
```

- JIFEDA1/JIFDSA1: H'0000 000C

```
ADDRESS    000102030405060708090A0B0C0D0E0F   101112131415161718191A1B1C1D1E1F
0000 00    XXXXXXXXXXXXXXXXXXXXXXXXFFD8FFDB   008400100B0C0E0C0A100E0D0E121110
0000 20    1318281A181616183123251D283A333D   3C3933383740485C4E40445745373850
           :
0002 20    B4B5B6B7B8B9BAC2C3C4C5C6C7C8C9CA   D2D3D4D5D6D7D8D9DAE2E3E4E5E6E7E8
0002 40    E9EAF2F3F4F5F6F7F8F9FAFFDA000C03   0100021103110003F0000FFD9FFFFFFFF
```

(4) Reload Mode Enabled

- JIFEDA1/JIFDSA1: H'0000 0000
  JIFEDA2/JIFDSA2: H'0000 0100
  JIFEDRSZ/JIFDDRSZ: H'0000 0100

```
ADDRESS    000102030405060708090A0B0C0D0E0F  101112131415161718191A1B1C1D1E1F
(Reload buffer 1)
0000 00    FFD8FFDB008400100B0C0E0C0A100E0D  0E1211101318281A181616183123251D
           :
0000 E0    328191A1082342B1C11552D1F0243362  7282090A161718191A25262728292A34
(Reload buffer 2)
0001 00    35363738393A434445464748494A5354  55565758595A636465666768696A7374
           :
0001 E0    5455565758595A636465666768696A73  7475767778797A828384858687888 98A
(Reload buffer 1)
0000 00    929394959697 98999AA2A3A4A5A6A7A8  A9AAB2B3B4B5B6B7B8B9BAC2C3C4C5C6
0000 20    C7C8C9CAD2D3D4D5D6D7D8D9DAE2E3E4  E5E6E7E8E9EAF2F3F4F5F6F7F8F9FAFF
0000 40    DA000C03010002110311003F0000FFD9  XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
```

43.3.5 Fractional Data Processing

The JPU can encode or decode the image in 4-pixel units, and sometimes it is needed to process the image that partially fills MCU (fractional data processing).

When the size of the image for coding by the JPU leaves one or more MCUs only partially filled, those MCUs are completed by filling the areas at the right and bottom relative to the origin of the image with black data (Y: H'00, CbCr: H'80). The image thus completed is then coded. When rotation is selected, MCUs are completed by filling the right and bottom areas relative to the post-rotation origin of the image with black data.

In decoding, if the image size information (parameter in the SOF0 marker) in the JPEG coded data leaves one or more MCUs only partially filled, the JPU only transfers the portions that contain actual data to the external buffer, e.g. in SDRAM. Thus, when the JPU decodes JPEG coded data that has been produced by the JPU coding data which did not completely fill all MCUs, the black data in the right and bottom areas of the incompletely filled MCUs are not transferred.

43.4 Interrupt Handling Flow

Interrupts for the JPU can be classified into interrupts for encoding/decoding and interrupts for transferring data. The way to clear an interrupt signal differs according to the interrupt sources.

43.4.1 Interrupts for Encoding and Decoding

Bits INS6, INS5, and INS3 in the interrupt status register JINTS are the interrupt sources for the JPEG core incorporated in the JPU. The interrupt signals which are asserted by these interrupt sources cannot be negated by clearing the corresponding interrupt status bits. Issue an interrupt signal clear command (set the JEND bit in JCCMD to B'1) to clear the interrupt signal.

(1) Encoding

- JPEG encoding process end
  When the INS6 bit in the interrupt status register JINTS is set to B'1, the JPEG encoding process is completed. After all of the coded data is transferred, the JPU ends the encoding process.

(2) Decoding

- JPEG decoding process end
  When the INS6 bit in the interrupt status register JINTS is set to B'1, the JPEG decoding process is completed. After all of the image data is transferred, JPU completes decoding.
- JPEG decoding error occurrence
  When the INS5 bit in the interrupt status register JINTS is set to B'1, the input JPEG coded data has an error and the JPU stops the decoding process. Read the error code (ERR bits in JCDERR) and identify the error source.
- Request for reading the image size and subsampling setting
  When the INS3 bit in the interrupt status register JINTS is set to B'1, JPEG coded data is input and information regarding its size and subsampling can be read. Since the JPEG decoding process is suspended, start the JPEG decoding process by setting the command to revoke the processing-stopped state after accessing the necessary registers. This interrupt occurs when the INT3 bit in the interrupt enable register JINTE is set to B'1.

43.4.2 Interrupts for Transferring Data

Bits INS14 to INS10 in the interrupt status register JINTS are the interrupt sources for transferring the image data and coded data. The interrupt signals asserted by these interrupt sources can be negated by clearing the corresponding interrupt status bits to 0.

(1) Encoding

- Occurs after data of one line buffer has been transferred (in line buffer mode)

  When the INS12 or INS11 bit in the interrupt status register JINTS is set to B'1, one line buffer of image data has been transferred; transfer the rest of the image data to the line buffer and resume transferring the data from the line buffer. This interrupt occurs when the INT12 or INT11 bit in the interrupt enable register JINTE is set to B'1.
- Occurs after the specified number of data have been reloaded

  When the INS13 bit in the interrupt status register JINTS is set to B'1, the coded data specified by JIFEDRSZ has been transferred. When the first interrupt occurs, transfer the coded data stored in the reload buffer to the other memory area. When the transfer is completed and the next reload interrupt occurs, transfer the coded data and set a command to restart the transfer to the reload buffer. The data is transferred to the first two reload buffers automatically and interrupts occur. These interrupts occur when the INT13 bit in the interrupt enable register JINTE is set to B'1.
- Occurs after all processes are completed

  When the INS10 bit in the interrupt status register JINTS is set to B'1, all of the coded data has been transferred and the JPU has completed encoding; transfer the coded data outside the JPU. When reload mode is set, transfer the rest of the coded data. When the total size of the coded data transferred to the reload buffer matches the number of coded data set by the JIFEDRSZ, bits INS10 and INS13 in JINTS are simultaneously set to B'1. This interrupt occurs when the INT10 bit in the interrupt enable register JINTE is set to B'1.

(2) Decoding

- Occurs after data of one line buffer has been transferred (in line buffer mode)

  When the INS12 or INS11 bit in the interrupt status register JINTS is set to B'1, one line buffer of image data has been transferred. When the first interrupt occurs, transfer the image data stored in the line buffer to the other memory area. When the transfer is completed and the next reload buffer interrupt occurs, transfer the image data and set a command to restart the transfer to the line buffer. The data is transferred to the first two reload buffers automatically and interrupts occur. These interrupts occur when the INT12 or INT11 bit in the interrupt enable register JINTE is set to B'1.

- Occurs after the specified number of data have been reloaded
  When the INS14 bit in the interrupt status register JINTS is set to B'1, the coded data in the reload buffer has been transferred; transfer the rest of the coded data to the reload buffer and set a command to resume transferring the data from the reload buffer. This interrupt occurs when the INT14 bit in the interrupt enable register JINTE is set to B'1.
- Occurs after all processes are completed
  When the INS10 bit in the interrupt status register JINTS is set to B'1, all of the image data has been transferred and the JPU has completed decoding; transfer the image data outside the JPU. This interrupt occurs when the INT10 bit in the interrupt enable register JINTE is set to B'1.

43.5 Bus Reset Processing

Issuing the bus reset command (setting the BRST bit in JCCMD to 1) causes a bus reset.

When the JPU is in operation, the bus reset command should not be issued. Registers other than below are initialized by a bus reset.

- JPEG code mode register (JCMOD)
- JPEG code command register (JCCMD)
- JPEG code quantization table number register (JCQTN)
- JPEG code Huffman table number register (JCHTN)
- JPEG code DRI upper register (JCDRIU)
- JPEG code DRI lower register (JCDRID)
- JPEG code vertical size upper register (JCVSZU)
- JPEG code vertical size lower register (JCVSZD)
- JPEG code horizontal size upper register (JCHSZU)
- JPEG code horizontal size lower register (JCHSZD)
- JPEG interrupt enable register (JINTE)
- JPEG interface control register (JIFCNT)

43.6 Software Reset Processing

Issuing the software reset command (setting the SRST bit in JCCMD to 1) causes a software reset.

After a software reset is specified, the SRST bit in JCCMD holds 1 until the current transfer in the JPU is completed. After the software reset processing, the following registers are initialized.

- JPEG code status register (JCSTS)
- JPEG code data count upper register (JCDTCU)
- JPEG code data count middle register (JCDTCM)
- JPEG code data count lower register (JCDTCD)
- JPEG interrupt status register (JINTS)
- JPEG code decode error register (JCDERR)
- JPEG code restart register (JCRST)
- JPEG interface control register (JIFCNT)

Section 44 3D Graphics Accelerator (3DG)

This LSI has a 3D graphics accelerator, the PowerVR™* Series SGX540; Imagination Technologies' 3D graphics core.

44.1 Features

- Universal Scalable Shader Engine (USSE) ™*
- Programmable architecture
- Latency tolerant architecture
- Internal True Colour ™*
- Video processing for multi-standard video decode and encode
- API support: Open GL ES 1.1/2.0, OpenVG, Direct3D Mobile

Note: * PowerVR™, Universal Scalable Shader Engine (USSE) ™ and Internal True Colour ™ are trademarks or registered trademark of Imagination Technologies Limited, U.K.

44.2 Block Diagram

Figure 42.1 shows a block diagram of the SGX540.

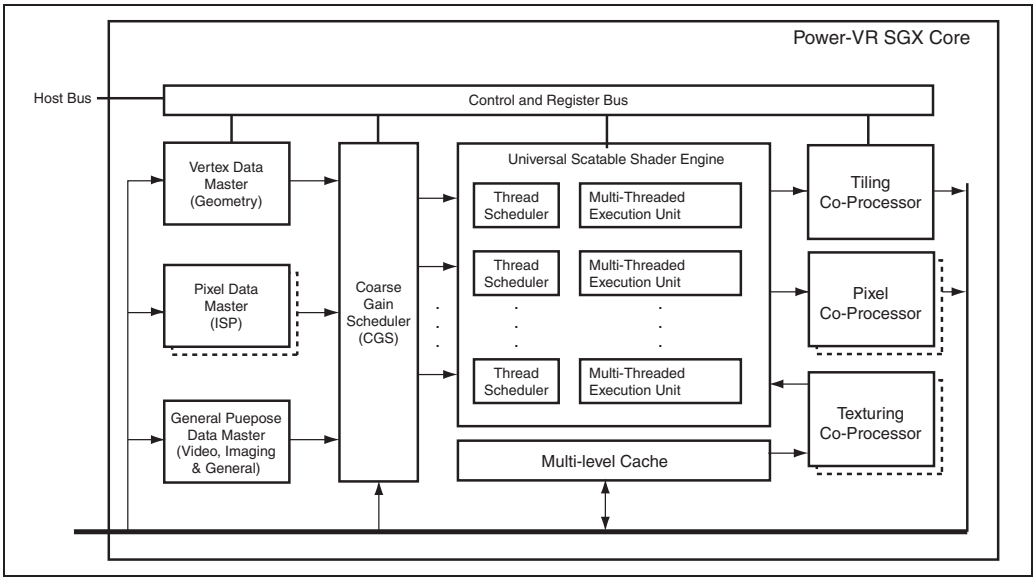


Figure 44.1 Block Diagram

Section 46 Camera ISP

46.1 Features

The image signal processor (ISP) handles processing to turn the output from a camera sensor into image signals. The external camera sensor module is connected to the pins for the MIPI-CSI2 physical layer interface (MIPI-CSI2 PHY module). The MIPI-CSI2 link layer interface (MIPI-CSI2 LINK module: CSI2I) that is connected to the MIPI-CSI2 PHY module handles conversion of the data received from the sensor module into the required raw image format. The ISP applies various processing to this raw image data and then finally stores the result as image data in SDRAM.

The ISP has the following functionality.

- Handles up to 16-Mpixel sensors
- Various kinds of processing to adjust for defective sensor elements
- Processing for various kinds of optical adjustment, including adjustment for shading and adjustment for distortion
- Processing for various kinds of filtering, including noise reduction
- Processing of a wide dynamic range to enhance gradations in images
- Three-A (automatic focus, automatic exposure, and automatic white balance) processing
- Handles HD moving images

46.1.1 ISP Signal Processing System Outline

The ISP's peripheral blocks are shown in figure 46.1 and the outline of the functional blocks in table 46.1.

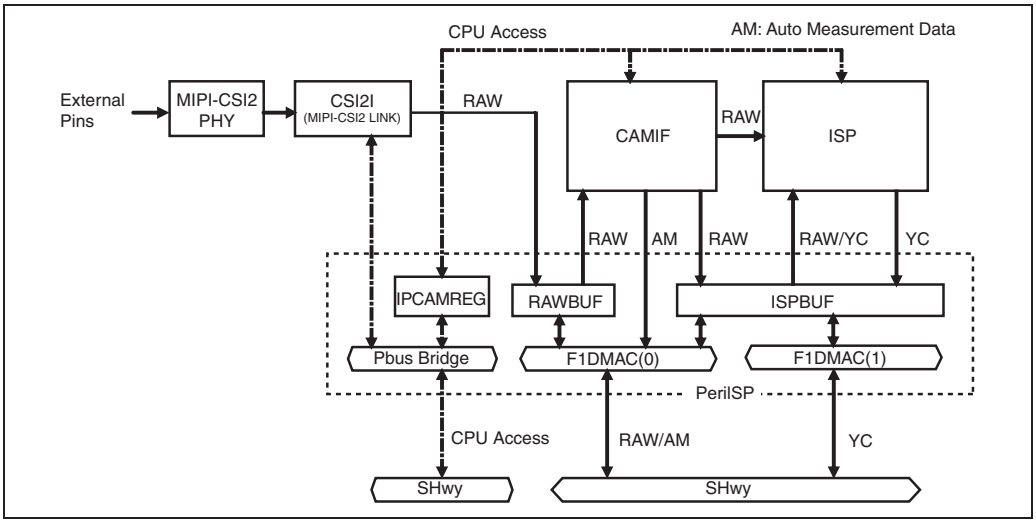


Figure 46.1 ISP Peripheral Block Diagram

Table 46.1 Functional Block Summary

Name	Function	Description
CAMIF	Camera I/F	Contains the sensor I/F, the block that corrects the imaging signal, and the blocks that perform computations necessary for the image correction.
ISP	Image signal processor block	Contains the blocks that performs various types of image processing based on the signal that is corrected by the CAMIF and the results of computations performed in the CAMIF. Note that some references to the ISP in this manual actually refer to all peripheral modules, including the ISP.
IPCAMREG	Signal processing CPUI/F	Serves as the CPU I/F for the CAMIF and ISP. Also contains registers that are common to the CAMIF and ISP.
CSI2I	MIPI-CSI2 LINK layer	A MIPI-CSI2 LINK module. The CSI2I converts the data output from the MIPI-CSI2's physical layer (PHY) block into the raw data format.
RAWBUF	Raw data buffer	Feeds raw data from the CSI2I or SDRAM to the CAMIF. This block is part of the ISP peripheral group module (PeriISP).
ISPBUF	ISP data buffer	Serves as the buffer for the raw data from the CAMIF and the raw/YC data to and from the ISP. This block is part of the PeriISP.
PbusBridge	CPU bus bridge	This is the bus bridge to the CPU. As well as handling CPU access to the IPCAMREG block for CPU access to the CAMIF and ISP blocks, this block also takes care of access to the CPU by CSI2I and the other blocks within the PeriISP (this block is part of the PeriISP).
F1DMAC	Data bus bridge	Arbitrates the data transfers from the CAMIF and ISP and transfers the data to the higher-level bus. The F1DMAC also has various DMA related functions. This block is part of the PeriISP.

46.1.2 CAMIF and ISP Internal Configuration Overview

(1) CAMIF internal configuration overview

The CAMIF consists of the block that corrects the imaging signal and the blocks that perform computations necessary for the image correction. It achieves these types of processing while interfacing with the sensor module and other peripheral circuits. The outline of the CAMIF configuration is shown in figure 46.2.

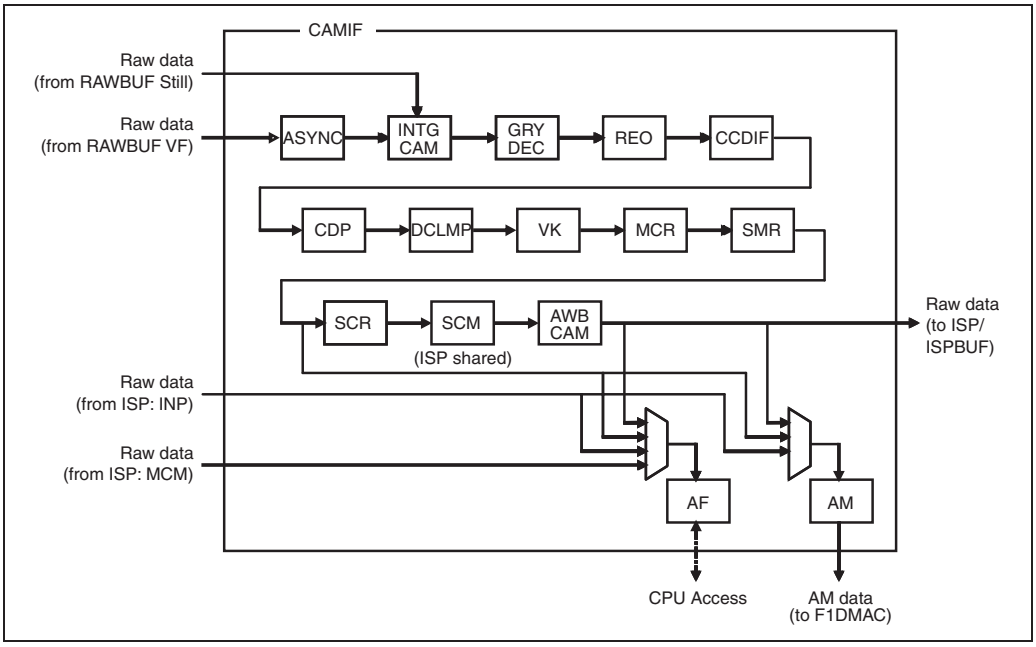


Figure 46.2 CAMIF Internal Configuration

The major functional blocks of the CAMIF are given below.

(Function 1) INTGCAM (CAMIF internal timing generator)

- CAMIF output: Supports 12-bit raw data.
- ISPBUF output: Supports 16-bit YCbCr (4:2:2/4:2:0) and 12-bit raw data.

(Function 2) GRYDEC (Graycode decoder) * Not available in this product.

- Converts the camera head clock to the system clock.
- Handles 12- or 10-bit input.

(Function 3) REO (Pixel array reordering)

- 12-bit input, 12-bit output

(Function 4) CCDIF (CCD interface) * Not available in this product.

- Handles up to 15 fields.
- Sets up the SMR area.

(Function 5) CDP (Defective pixel correction)

- 12-bit input, 12-bit output
- Defective pixel position (horizontal/vertical coordinates) setting register (510 maximum definable pixels)
- Correction method: Horizontal linear interpolation

(Function 6) DCLMP (Digital clamping)

- 12-bit input, 12-bit output
- Clamping method: Horizontal clamping (vertical OB reflection)
- OB accumulation method: Weighted average

(Function 7) VK (Correction processing for a line of defective pixels in the vertical direction)

- 12-bit input, 12-bit output
- Detects integral values for pixels in 64 areas.
- 32 definable defects (horizontal and vertical coordinates)

(Function 8) MCR (Sensor mixed color correction)

- 12-bit input, 12-bit output
- Corrects mixed colors of Gr/Gb pixels using peripheral R/B pixels.

(Function 9) SMR (Smear correction)

- 12-bit input, 12-bit output
- Detects smears in the OB areas and performs smear correction.
- Smear detection mode selectable as upper OB or lower OB.
- Smear detection processing corresponds to processing for horizontal OB averaging and vertical OB averaging.
- Can perform smear correction independently on the 4 color components (R/Gr/Gb/B).

(Function 10) SCR (Shading correction)

- 12-bit input, 12-bit output
- Calculates the optical shading correction coefficients according to the distance from the optical center (arbitrarily definable).
- Corrects each pixel using the optical shading correction coefficients.
- Can correct axial shadings simultaneously and independently.

(Function 11) SCM (Mesh shading correction)

- 12-bit input, 12-bit output
- Correction coefficients are arranged in a 36 (horizontal) × 36 (vertical) mesh configuration.
- Can perform correction on the AWBIP output in the ISP block (mutually exclusively performed in the CAMIF and ISP).

(Function 12) AWBCAM (CAMIF Automatic White Balance)

- WB gain correction calculation (12-bit input, 12-bit output)
  Independent WB gain coefficients for each color: 12 bits (unsigned, integral part: 3 bits, fractional part: 9 bits)
- Gain correction calculation (12-bit input, 12-bit output)
  Gain coefficients common to all colors: 12 bits (unsigned, integral part: 4 bits, fractional part: 8 bits)

(Function 13) AF (Automatic Focus)

- Input: 12-bit raw data * 8-bit raw or 8-bit Y signal depending on the measurement path
- References the upper 8 bits of the input signal.
- Number of windows: 16 floating windows or 32 (horizontal) × 1 (vertical) split windows
- Detection system: Horizontal detection (2-stage filter configuration possible in 32 (horizontal) × 1 (vertical) split window mode)

- Number of bands: 1 band per 8 windows × 2 * 1 band in 32 (horizontal) × 1 (vertical) split window mode

(Function 14) AM (Automatic Measurement)

- Calculates color signals independently (AE, AWB).
- 12-bit input *8-bit raw depending on the measurement path
- References the upper 8 bits of the input signal.
- Calculation targets: R, Gr, Gb, B (signal accumulation processing, threshold accumulation processing, accumulated threshold value counting processing, maximum/minimum measurement)
- Number of split windows: 32 horizontal × 1 vertical
  (Same number of pixels in all windows. Line count specified repeatedly in vertical direction)
- Full-screen measurement
- Detects flickers in the screen (16 lines accumulated independently).
- Accumulation performed on a field basis only.
- The split window accumulated values can be output to SDRAM by DMA transfer.

(2) ISP internal configuration overview

The ISP consists of blocks for displaying images and other blocks that perform various types of image processing based on the signal that is corrected by the CAMIF and the results of computations performed in the CAMIF. The block configuration of the ISP is shown in figure 46.3.

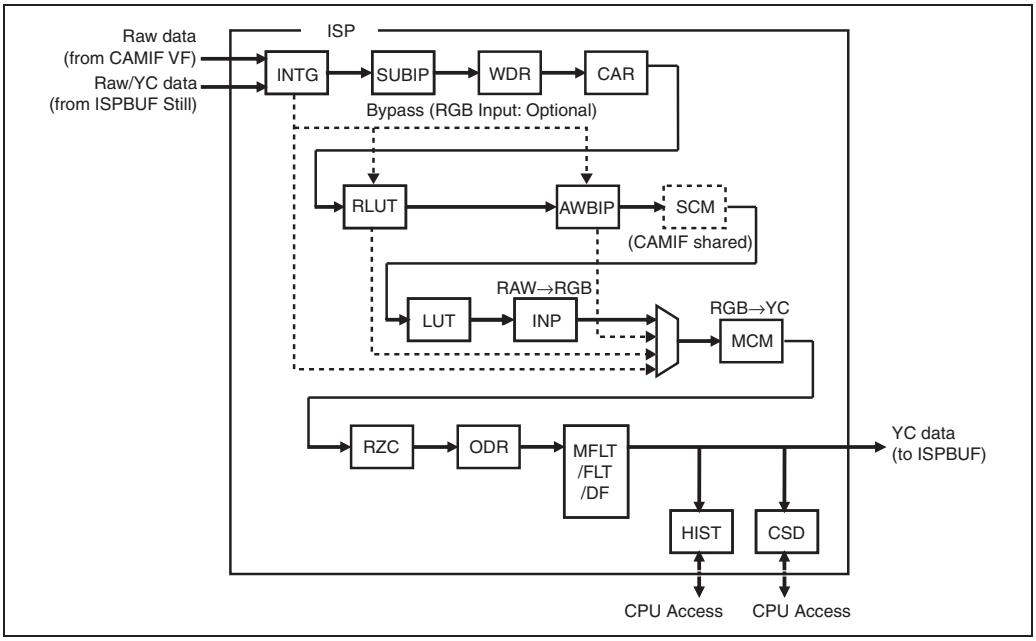


Figure 46.3 ISP Internal Configuration

The major functional blocks of the ISP are given below.

(Function 1) INTG (Internal timing generator)

- CAMIF output: Supports 12-bit raw data.
- ISPBUF output: Supports 16-bit YCbCr (4:2:2) and 12-bit raw data.

(Function 2) SUBIP (ISP block horizontal shrinking)

- CAMIF output: Supports 12-bit raw data.
- 12-bit input, 12-bit output

- Raw data horizontal shrinking processing
  (Shrinking ratio M/N where M and N are integers, $1 \leqq M \leqq 15$, $2 \leqq N \leqq 16$, $M < N$)

(Function 3) WDR (Wide dynamic range processing)

- ISPBUF output: Supports 12-bit raw data (2 images).
- 12-bit input, 12-bit output (input need be an image to which the WB coefficients have been applied.)
- Synthesizes two images at a precision equal to the synthesis ratio (0.0 to 1.0, 10-bit fractional part).
- Performs correction processing on the 2 input images according to the exposure time (12-bit input — 18-bit output, implemented using a 16-line approximation LUT)
- Performs gradation compression processing the synthesized image (19-bit input — 12-bit output, implemented using a 16-line approximation LUT)

(Function 4) CAR (Chromatic aberration correction processing)

- 12-bit input, 12-bit output
- Corrects chromatic aberrations caused by lens aberrations.

(Function 5) RLUT (Raw/RGB gradation correction processing)

- 12-bit input/output LUT (linear approximation curve (32-line approximation))
- 24-bit RGB input/output LUT (linear approximation curve (32-line approximation), mutually exclusive with the other functions of the ISP block)

(Function 6) AWBIP (Image processing block, Automatic White Balance)

- Gain correction calculation (12-bit input, 12-bit output)
  Gain coefficient: 12 bits (unsigned, integral part: 3 bits, fractional part: 9 bits)

(Function 7) LUT (Gradation correction: Look Up Table)

- 12-bit input, 8-bit output
- Linear approximation curve (32-line approximation)
  Y-axis only set up independently for R, G, and B; X-axis set up commonly for the 3 colors.

(Function 8) INP (Color interpolation: Interpolation)

- 8-bit input, 24-bit output (8 bits for each of R, G, and B)
- False color suppression
- Edge smoothing
- Luminance isolated point elimination
- Pixel mixture

(Function 9) MCM (Color correction)

- 24-bit input (8 bits for each of RGB), 24-bit output (8 bits for each of YCbCr)
- Controls hue, chroma, and luminance independently of one another.
- Number of hues: 24 (24 hues selected out of 256 hues), adjustable
- Specific color correction (controls chroma and luminance for each hue.)
- Chroma balance adjustment

(Function 10) RZC (Resolution conversion)

- 24-bit input , 24-bit output
  Can convert the resolution conversion factor from 1% up to 1000%.
  (The resolution conversion factor is specified in the format of numerator/denominator.)
  Supports horizontal reversion (mirror mode).

(Function 11) ODR (Optical distortion correction)

- 24-bit input (YCbCr = 4:4:4), 16-bit output (YCbCr = 4:2:2)
- Corrects optical distortions caused by lens aberrations.

* Enabled only in still image processing modes.

(Function 12) FLT (Filter: edge correction/noise rejection/digital focus/matrix filter)

- 16-bit input, 16-bit output(YCbCr = 4:2:2)
- Noise reduction (luminance/color difference)
- Luminance signal
  - Multiband processing (3 bands set)
    HPF (High Pass Filter), BPF (Band Pass Filter), LPF (Low Pass Filter)
  - BNC (Base level Noise Clip), HC (High level Clip)
  - Peripheral resolution correction
- Color difference signal
  LPF (Low Pass Filter)
- Digital focus processing

(Function 13) HIST (Histogram)

- 8-bit input, 128-grayscale output
- Data to be measured: ISP block output data (after subjected to ring pixel cutoff)

(Function 14) CSD (Camera shake detection processing)

- Input Y: 8 bits
- Maximum number of measured windows: 256
- Maximum window size: 128 × 128 pixels
- Generates horizontal and vertical displacements and detection accuracy index for each window.

46.1.3 Image Processing Data Flows

This section explains the typical image processing flows for the ISP.

(1) View finder processing and moving image shooting flow

The processing flow diagram for view finder processing (VF) and moving image shooting are shown in figure 46.4. The image data output from the sensor is input to the CAMIF via the RAWBUF. The raw data are subjected to various types of correction processes in the CAMIF and passed directly to the ISP. The raw data input in the ISP is subjected to RGB interpolation, YC conversion, and other correction and filtering processes, after which it is stored in SDRAM via the ISPBUF and F1DMAC.

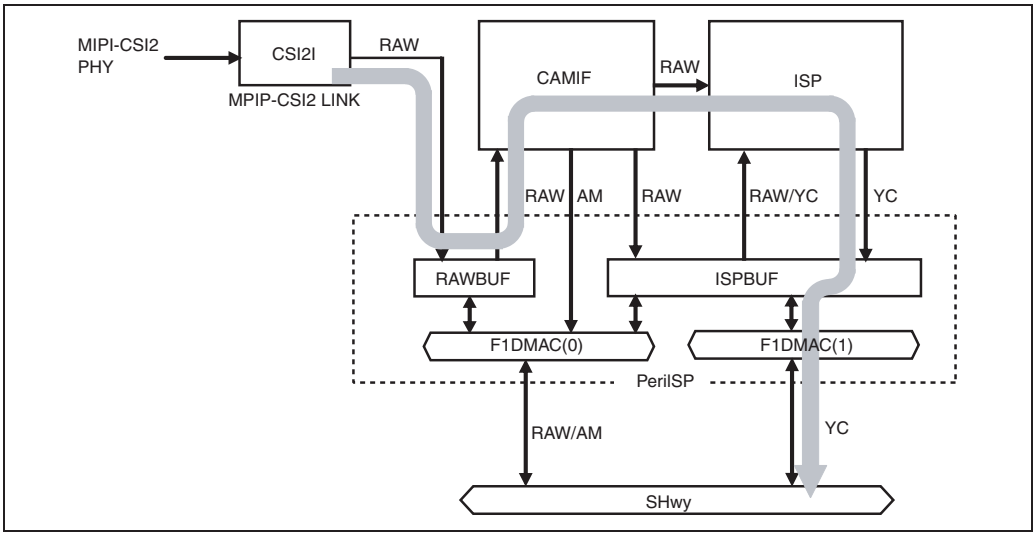


Figure 46.4 Moving Image Shooting Processing Flow

(2) Still image shooting processing flow

The processing flow diagram for still image processing is shown in figure 46.5. The still image shooting processing is divided into three processing passes.

Path (1): Capture processing

The data from the MIPI-CSI2 LINK block is temporarily stored in SDRAM via the RAWBUF and F1DMAC. Although the data could be sent directly to the CAMIF in this case as in moving image shooting processing, is simply transferred to SDRAM for the reasons (1) The size of image to be shot is great and (2) as high as possible an imaging rate need be established to prevent shakes.

Path (2): Raw preprocessing

The raw data which is stored during capture processing is read into the CAMIF and subjected to optical, defective pixel, and other correction processing as well as various measurement processing for AE, AF, and AWB in the CAMIF. The raw data which is preprocessed in this way is stored in SDRAM again.

Pass (3): YC strip processing

The preprocessed raw data are reread and subjected by the ISP to RGB interpolation, YC conversion, and various types filtering and correction processes. In this case, since the ISP is subject to restrictions as to the horizontal size, it is necessary to split the preprocessed raw data for any image with a large image size in the vertical direction into two or more strips of data and process them sequentially. When all of these data strips are processed, they are stored in SDRAM as a single sheet of image.

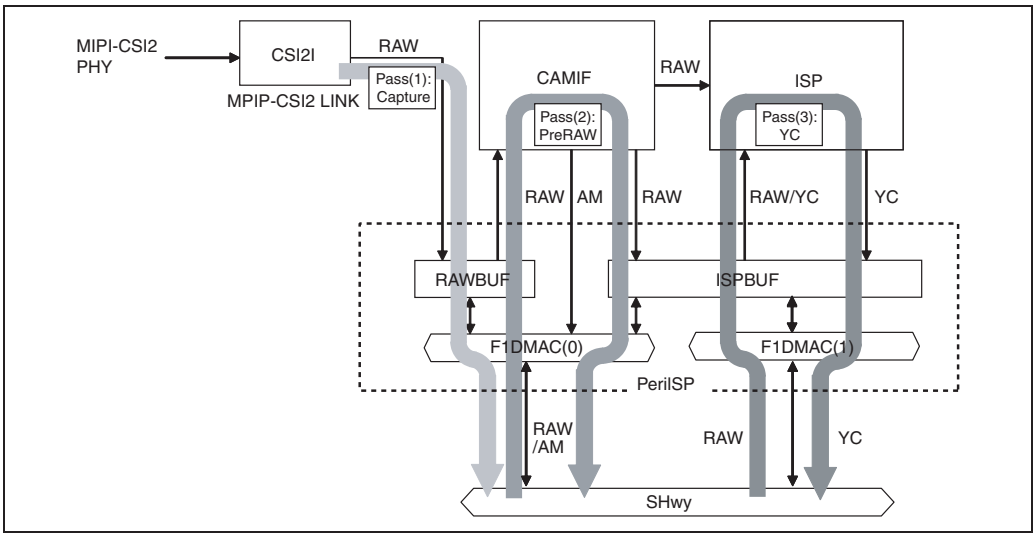


Figure 46.5 Still Image Shooting Processing Flow

46.2 ISP Image Processing Buffer (ISPBUF)

The ISP image processing buffer (ISPBUF) is a module that interfaces between the ISP/CAMIF and F1DMAC and places image data on the bus. The ISPBUF temporarily holds data from the ISP/CAMIF and transfers data through the F1 bus I/F. It also controls the active/inactive state of the other ISP peripheral modules as well as exercises INT control.

Features

The ISPBUF has the following functions:

- Image data transfer of sizes from 1 to 128 64-bit data sizes
- Raw noise reduction (NR) using two blocks of raw data
- Active/inactive state control of the other ISP peripheral modules
- INT monitoring for the other ISP peripheral modules

46.2.1 ISPBUF Function Summary

Table 46.2 summarizes the functions of the ISPBUF.

Table 46.2 Function Summary

Item	Function Implemented	Description
Input format	12-bit raw YCbCr (4:2:2/4:2:0)	
Output format	12-bit raw YCbCr (4:2:2/4:2:0)	
Data size	64 bits/1 to 128	In each YC format data transfer, data are transferred in the order of Y data followed by C data. The data size is the same for the Y and C data.
ISP peripheral module Active/Inactive control	ISP peripheral module clock control	Provides on/off control of the clocks to the other ISP peripheral modules.
ISP peripheral module INT monitoring	ISP peripheral module INT monitoring	Monitors the interrupts occurring in the other ISP peripheral modules.

46.2.2 ISPBUF Internal Configuration

The internal configuration of the ISPBUF is shown in figure 46.6.

- CIFIBUF: The buffer that takes in the raw data (shot image) from SDRAM and merges it with the data output (black image) from the CAMIF for RAWNR processing.
- CIFOBUF: The buffer used to transfer the raw data output from the CAMIF to SDRAM.
- ISPIBUF: The buffer used to transfer raw or YC data from SDRAM to the ISP.
- ISPOBUF: The buffer used to transfer the YC data output from the ISP to SDRAM.
- RAWBUF/AM: Accesses to the F1DMAC are accomplished via the ISPBUF during RAWBUF (buffer for captured raw data output and CAMIF input) and CAMIF's AM (accumulated values for AE and AWB) data output processing. During these accesses, byte/word swap occurs in the raw or AM data. The RAWBUF contains 3 types of buffers, i.e., RAWIBUF, RAWOBUF, and RAWDIRBUF.
- Data path switching: Data transfers to the bus from the RAWIBUF, CIFOBUF, and CIFIBUF are done normally via the F1DMAC(0). The data may be directed through the F1DMAC(1) by making necessary configuration. This makes it easy to secure the F1DMAC(0)'s band which becomes necessary at capture time.

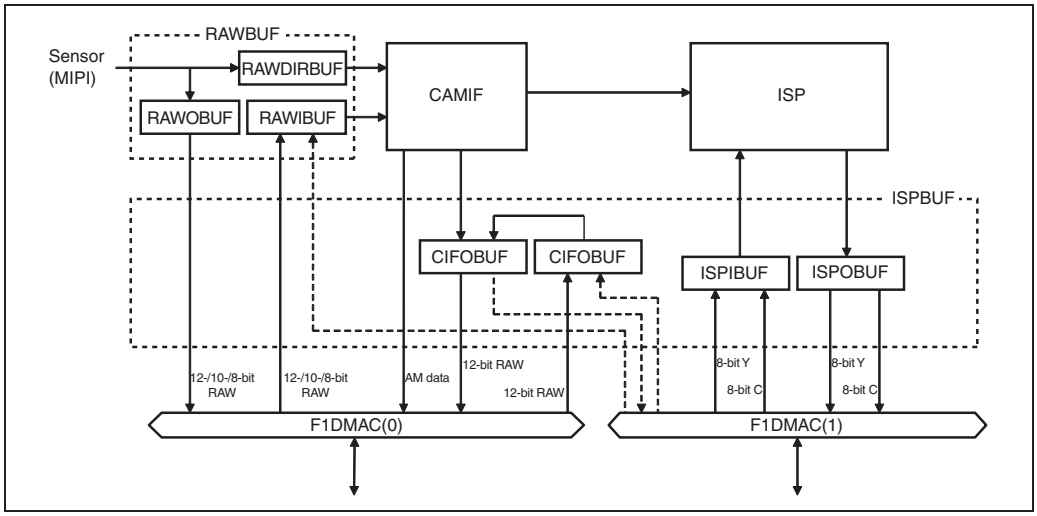


Figure 46.6 ISPBUF Internal Configuration

46.2.3 DMA Source Assignments

The AM outputs from the ISPBUF, RAWBUF, and CAMIF are assigned F1DAMC's input/output data ports with the source numbers listed in the tables given below. The number of the sources to be used must be specified in the DCTG request source select bits of the DMA control registers A: F1DMAC(0/1)_DMCNTAn (n corresponds to channel numbers 0 to 7) in the F1DMAC.

Table 46.3 F1DMAC(0) Source Assignments

F1DMAC(0)	Normal mode	When the path is switched using the data flow select register (ISPBUF_AD_F1SEL)
Source number 1	RAWOBUF	←
Source number 2	CIFOBUF	(Reserved)
Source number 3	CIFIBUF	(Reserved)
Source number 4	RAWIBUF	(Reserved)
Source number 5	AMO	←

Table 46.4 F1DMAC(1) Source Assignments

F1DMAC(1)	Normal mode	When the path is switched using the data flow select register (ISPBUF_AD_F1SEL)
Source number 1	(reserved)	CIFOBUF
Source number 2	(reserved)	CIFIBUF
Source number 3	(reserved)	RAWIBUF
Source number 4	ISPOBUF(Y)	←
Source number 5	ISPOBUF(C)	←
Source number 6	ISPIBUF(Y)	←
Source number 7	ISPIBUF(C)	←

46.2.4 Register Description

(1) Register read/write restrictions

Restrictions on register reads and writes are given below. The system operation may fail if the integrity of the following register operations is not guaranteed:

1. Writing 1 into any read-only register bit or reserved area is prohibited. Do not set any value other than the specified values.
2. There are cases in which a nonzero value is read from a read-only bit. Such a value must not be rewritten.
3. Writing into any registers (bits) that are disallowed for writes during operation is prohibited while some operation is in progress (reads are allowed). The operating state of the ISPBUF can be identified by reading the ISPBUF operation register or by identifying the end of the F1DMAC transfer.
4. All of the ISPBUF registers must be allocated to a non-cache area.

(2) Terms and abbreviations used in this document

A term that is used in this document is explained below.

1. "Software reset" refers to a forced reset into the ISPBUF internal circuit. This means that any attempt to effect a module reset while the ISPBUF is running normally might place the ISPBUF peripheral hardware into an inoperative state.

(3) List of Registers

The register configuration of the ISPBUF registers is summarized in table 46.5. The relationship between the processing modes and register states is given in table 46.6.

Table 46.5 ISPBUF Register Configuration

Register Name	Abbreviation	R/W	Address	Access Size
ISPBUF buffer operation control register	ISPBUF_AD_BUFSTR	R/W	H'FE8F 6000	32
ISPBUF software reset control register	ISPBUF_AD_SFTRST	R/W	H'FE8F 6004	32
ISPBUF continuous operation control	ISPBUF_AD_CONTI	R/W	H'FE8F 600C	32
ISPBUF buffer status monitor register	ISPBUF_AD_BUFSTATUS	R	H'FE8F 6010	32
ISPBUF buffer full monitor register	ISPBUF_AD_BUFFULL	R	H'FE8F 6014	32
ISPBUF buffer empty monitor register	ISPBUF_AD_BUFEMP	R	H'FE8F 6018	32
ISPBUF error flag monitor register	ISPBUF_AD_ERR	R	H'FE8F 6020	32
ISPBUF error flag clear register	ISPBUF_AD_ERRCLR	R/W	H'FE8F 6024	32
ISPBUF operand transfer data count register	ISPBUF_AD_OPESEL	R/W	H'FE8F 6040	32
ISPBUF wait request control register	ISPBUF_AD_REQWAITON	R/W	H'FE8F 6044	32
ISPBUF CIF wait cycle setting register	ISPBUF_AD_WAITCYC_CIF	R/W	H'FE8F 6048	32
ISPBUF ISP wait cycle setting register	ISPBUF_AD_WAITCYC_ISP	R/W	H'FE8F 604C	32
ISPBUF raw data noise reduction control register	ISPBUF_AD_RAWNR	R/W	H'FE8F 6060	32
ISPBUF F1DMAC data flow select register	ISPBUF_AD_F1SEL	R/W	H'FE8F 6070	32
ISPBUF RAWBUF data swap control register	ISPBUF_AD_SWP_RAW	R/W	H'FE8F 6080	32
ISPBUF CAMIF data swap control register	ISPBUF_AD_SWP_CIF	R/W	H'FE8F 6084	32
ISPBUF ISP data swap control register	ISPBUF_AD_SWP_ISP	R/W	H'FE8F 6088	32
ISPBUF buffer reservation size register	ISPBUF_AD_FIFOSLACK	R/W	H'FE8F 60B0	32
ISPBUF ISP peripheral module activation control register	ISPBUF_AD_MSTP	R/W	H'FE8F 6100	32
ISPBUF interrupt monitor register	ISPBUF_AD_INT_ALL	R/W	H'FE8F 6110	32
ISPBUF interrupt status register 0	ISPBUF_AD_INT_STAT0	R/W	H'FE8F 6118	32
ISPBUF interrupt status register 1	ISPBUF_AD_INT_STAT1	R/W	H'FE8F 611C	32
ISPBUF interrupt monitor mask register	ISPBUF_AD_INT_MASK0	R/W	H'FE8F 6120	32
ISPBUF CAMIF control register	ISPBUF_AD_CAMIF1	R/W	H'FE8F 6134	32

Register Name	Abbreviation	R/W	Address	Access Size
ISPBUF CMOSIF control register 0	ISPBUF_AD_CMOSIF0	R/W	H'FE8F 6140	32
ISPBUF CMOSIF control register 1	ISPBUF_AD_CMOSIF1	R/W	H'FE8F 6144	32
ISPBUF CIFI byte count register	ISPBUF_AD_BC_CIFI	R	H'FE8F 6150	32
ISPBUF CIFO byte count register	ISPBUF_AD_BC_CIFO	R	H'FE8F 6154	32
ISPBUF ISPI_Y byte count register	ISPBUF_AD_BC_ISPIY	R	H'FE8F 6160	32
ISPBUF ISPI_C byte count register	ISPBUF_AD_BC_ISPIC	R	H'FE8F 6164	32
ISPBUF ISPO_Y byte count register	ISPBUF_AD_BC_ISPOY	R	H'FE8F 6168	32
ISPBUF ISPO_C byte count register	ISPBUF_AD_BC_ISPOC	R	H'FE8F 616C	32

Table 46.6 Processing Modes and Register States

Abbreviation	Reset	Module Standby
ISPBUF_AD_BUFSTR	Initialized	Retained
ISPBUF_AD_SFTRST	Initialized	Retained
ISPBUF_AD_CONTI	Initialized	Retained
ISPBUF_AD_BUFSTATUS	Initialized	Retained
ISPBUF_AD_BUFFULL	Initialized	Retained
ISPBUF_AD_BUFEMP	Initialized	Retained
ISPBUF_AD_ERR	Initialized	Retained
ISPBUF_AD_ERRCLR	Initialized	Retained
ISPBUF_AD_OPESEL	Initialized	Retained
ISPBUF_AD_REQWAITON	Initialized	Retained
ISPBUF_AD_WAITCYC_CIF	Initialized	Retained
ISPBUF_AD_WAITCYC_ISP	Initialized	Retained
ISPBUF_AD_RAWNR	Initialized	Retained
ISPBUF_AD_F1SEL	Initialized	Retained
ISPBUF_AD_SWP_RAW	Initialized	Retained
ISPBUF_AD_SWP_CIF	Initialized	Retained
ISPBUF_AD_SWP_ISP	Initialized	Retained
ISPBUF_AD_FIFOSLACK	Initialized	Retained
ISPBUF_AD_MSTP	Initialized	Retained
ISPBUF_AD_INT_ALL	Initialized	Retained
ISPBUF_AD_INT_STAT0	Initialized	Retained

Abbreviation	Reset	Module Standby
ISPBUF_AD_INT_STAT1	Initialized	Retained
ISPBUF_AD_INT_MASK0	Initialized	Retained
ISPBUF_AD_CAMIF1	Initialized	Retained
ISPBUF_AD_CMOSIF0	Initialized	Retained
ISPBUF_AD_CMOSIF1	Initialized	Retained
ISPBUF_AD_BC_CIFI	Initialized	Retained
ISPBUF_AD_BC_CIFO	Initialized	Retained
ISPBUF_AD_BC_ISPIY	Initialized	Retained
ISPBUF_AD_BC_ISPIC	Initialized	Retained
ISPBUF_AD_BC_ISPOY	Initialized	Retained
ISPBUF_AD_BC_ISPOC	Initialized	Retained

46.2.5 ISPBUF Buffer Operation Control Register (ISPBUF_AD_BUFSTR)

ISPBUF_AD_BUFSTR enables or disables FIFO operations in the ISPBUF. It is normally cleared at the end of processing on one frame. It is not cleared, however, if continuous operation is specified by the ISPBUF_AD_CONTI register.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	cifibuf_on	—	—	—	cifobuf_on
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	ispibuf_on	—	—	—	ispobuf_on
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
20	cifibuf_on	B'0	R/W	CIFIBUF operation register 0: Disabled 1: Enabled
19 to 17	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
16	cifobuf_on	B'0	R/W	CIFOBUF operation register 0: Disabled 1: Enabled
15 to 5	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
4	ispibuf_on	B'0	R/W	ISPIBUF operation register 0: Disabled 1: Enabled
3 to 1	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
0	ispobuf_on	B'0	R/W	ISPOBUF operation register 0: Disabled 1: Enabled

46.2.6 ISPBUF Software Reset Control Register (ISPBUF_AD_SFTRST)

ISPBUF_AD_SFTRST controls the forced reset operation of the ISPBUF's internal circuit. Writing this register during operation is prohibited. Note that any attempt to effect a module reset while the ISPBUF is running normally might place the ISPBUF peripheral modules into an inoperative state.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	srst_cifi	—	—	—	srst_cifo
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	srst_ispi	—	—	—	srst_ispo
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
20	srst_cifi	B'0	R/W	CIFIBUF software reset bit 0: NOP 1: Software reset
19 to 17	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
16	srst_cifo	B'0	R/W	CIFOBUF software reset bit 0: NOP 1: Software reset

Bit	Bit Name	Initial Value	R/W	Description
15 to 5	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
4	srst_ispi	B'0	R/W	ISPIBUF software reset bit 0: NOP 1: Software reset
3 to 1	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
0	srst_ispo	All 0	R/W	ISPOBUF software reset bit 0: NOP 1: Software reset

46.2.7 ISPBUF Continuous Operation Control Register (ISPBUF_AD_CONTI)

ISPBUF_AD_CONTI controls the termination of the ISPBUF. When this register is enabled, neither the pertinent buffer is stopped nor the ISPBUF_AD_BUFSTR register is cleared. When stopping the buffer operation, disable this register during the processing of the last frame in the continuous processing mode or effect software reset after the F1DMAC transfer is ended.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	conti_cif
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	conti_isp
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
16	conti_cif	B'0	R/W	CIFIBUF/CIFOBUF continuous operation 0: Disabled 1: Enabled
15 to 1	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
0	conti_isp	B'0	R/W	ISPIBUF/ISPOBUF continuous operation 0: Disabled 1: Enabled

46.2.8 ISPBUF Buffer Status Monitor Register (ISPBUF_AD_BUFSTATUS)

ISPBUF_AD_BUFSTATUS is a register that indicates the operating status of the ISPBUF.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	bufbusy_cifi	—	—	—	bufbusy_cifo
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	bufbusy_ispi	—	—	—	bufbusy_ispo
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
20	bufbusy_cifi	B'0	R	CIFIBUF buffer busy 0: Idle 1: Busy

Bit	Bit Name	Initial Value	R/W	Description
19 to 17	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
16	bufbusy_cifo	B'0	R	CIFOBUF buffer busy 0: Idle 1: Busy
15 to 5	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
4	bufbusy_ispi	B'0	R	ISPIBUF buffer busy 0: Idle 1: Busy
3 to 1	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
0	bufbusy_ispo	B'0	R	ISPOBUF buffer busy 0: Idle 1: Busy

46.2.9 ISPBUF Buffer Full Monitor Register (ISPBUF_AD_BUFFULL)

ISPBUF_AD_BUFFULL is a register that indicates whether the buffers in the ISPBUF are full.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	buffull_cifi	—	—	—	buffull_cifo
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	buffull_ispi_c	—	—	—	buffull_ispi_y	—	—	—	—	—	—	—	buffull_ispo
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
20	buffull_cifi	B'0	R	CIFIBUF buffer full flag 0: Normal 1: Full
19 to 17	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
16	buffull_cifo	B'0	R	CIFOBUF buffer full flag 0: Normal 1: Full
15 to 13	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
12	buffull_ispi_c	B'0	R	ISPIBUF (C plane) buffer full flag 0: Normal 1: Full
11 to 9	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
8	buffull_ispi_y	B'0	R	ISPIBUF (Y plane) buffer full flag 0: Normal 1: Full
7 to 1	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
0	buffull_ispo	B'0	R	ISPOBUF buffer full flag 0: Normal 1: Full

46.2.10 ISPBUF Buffer Empty Monitor Register (ISPBUF_AD_BUFEMP)

ISPBUF_AD_BUFEMP is a register that indicates whether the buffers in the ISPBUF are empty.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	bufemp_cifi	—	—	—	bufemp_cifo
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	bufemp_ispi_c	—	—	—	bufemp_ispi_y	—	—	—	—	—	—	—	bufemp_ispo
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
20	bufemp_cifi	B'0	R	CIFIBUF empty flag 0: Normal 1: Empty
19 to 17	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
16	bufemp_cifo	B'0	R	CIFOBUF empty flag 0: Normal 1: Empty
15 to 13	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
12	bufemp_ispi_c	B'0	R	ISPIBUF (C plane) empty flag 0: Normal 1: Empty
11 to 9	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
8	bufemp_ispi_y	B'0	R	ISPIBUF (Y plane) empty flag 0: Normal 1: Empty
7 to 1	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
0	bufemp_ispo	B'0	R	ISPOBUF empty flag 0: Normal 1: Empty

46.2.11 ISPBUF Error Flag Monitor Register (ISPBUF_AD_ERR)

ISPBUF_AD_ERR is a register that indicates the error state of the buffers in the ISPBUF. 1 in a bit in this register indicates that an overflow (or underflow) has occurred in the corresponding buffer.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	err_buf_cifi	—	—	—	err_buf_cifo
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	err_buf_ispo
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
20	err_buf_cifi	B'0	R	CIFIBUF error flag 0: Normal 1: Error
19 to 17	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
16	err_buf_cifo	B'0	R	CIFOBUF error flag 0: Normal 1: Error
15 to 1	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
0	err_buf_ispo	B'0	R	ISPOBUF error flag 0: Normal 1: Error

46.2.12 ISPBUF Error Flag Clear Register (ISPBUF_AD_ERRCLR)

ISPBUF_AD_ERRCLR is a register that is used to initialize the ISPBUF error flag monitor register (ISPBUF_AD_ERR).

This register is automatically cleared after the error flags are initialized.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	errclr_cifi	—	—	—	errclr_cifo
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	errclr_ispo
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
20	errclr_cifi	B'0	R/W	CIFIBUF error clear bit 0: NOP 1: Clears the error flag.
19 to 17	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
16	errclr_cifo	B'0	R/W	CIFOBUF error clear bit 0: NOP 1: Clears the error flag.
15 to 1	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
0	errclr_ispo	B'0	R/W	ISPOBUF error clear bit 0: NOP 1: Clears the error flag.

46.2.13 ISPBUF Operand Transfer Data Count Register (ISPBUF_AD_OPESEL)

ISPBUF_AD_OPESEL is a register used to specify the number of blocks (operand size) of data required to complete a single transfer operation. Note that one data block is composed of 8 bytes.

Writing this register during operation is prohibited.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	opesel_cifi			—	opesel_cifo		
Initial value:	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	opesel_ispi			—	opesel_ispo		
Initial value:	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 23	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
22 to 20	opesel_cifi [2:0]	H'2	R/W	CIFIBUF operand transfer data count select (data blocks, 1 data block = 8 bytes) 000: 1 001: 2 010: 4 011: 8 100: 16 101: 32 110: 64 111: 128
19	—	B'0	R	Reserved. This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
18 to 16	opesel_cifo [2:0]	H'2	R/W	CIFOBUF operand transfer data count select (data blocks, 1 data block = 8 bytes) 000: 1 001: 2 010: 4 011: 8 100: 16 101: 32 110: 64 111: 128
15 to 7	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
6 to 4	opesel_ispi [2:0]	H'2	R/W	ISPIBUF operand transfer data count select (data blocks, 1 data block = 8 bytes) 000: 1 001: 2 010: 4 011: 8 100: 16 101: 32 110: 64 111: 128
3	—	B'0	R	Reserved. This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
2 to 1	opesel_ispo [2:0]	H'2	R/W	ISPOBUF operand transfer data count select (data blocks, 1 data block = 8 bytes) 000: 1 001: 2 010: 4 011: 8 100: 16 101: 32 110: 64 111: 128

46.2.14 ISPBUF Wait Request Control Register (ISPBUF_AD_REQWAITON)

ISPBUF_AD_REQWAITON is a register used to specify whether wait processing is to be performed when the ISPBUF makes a request to the F1DMAC. The interval of waiting is specified using the ISPBUF_AD_WAITCYC_CIF and ISPBUF_AD_WAITCYC_ISP registers.

Writing this register during operation is prohibited.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	reqwait_on_cifi	—	—	—	reqwait_on_cifo
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	reqwait_on_ispi_c	—	—	—	reqwait_on_ispi_y	—	—	—	reqwait_on_ispo_c	—	—	—	reqwait_on_ispo_y
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
20	reqwait_on_cifi	B'0	R/W	CIFIBUF wait processing enable 0: Disabled 1: Enabled

Bit	Bit Name	Initial Value	R/W	Description
19 to 17	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
16	reqwait_on_cifo	B'0	R/W	CIFOBUF wait processing enable 0: Disabled 1: Enabled
15 to 13	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
12	reqwait_on_ispi_c	B0	R/W	ISPIBUF (C plane) wait processing enable 0: Disabled 1: Enabled
11 to 9	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
8	reqwait_on_ispi_y	B'0	R/W	ISPIBUF (Y plane) wait processing enable 0: Disabled 1: Enabled
7 to 5	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
4	reqwait_on_ispo_c	B'0	R/W	ISPOBUF (C plane) wait processing enable 0: Disabled 1: Enabled
3 to 1	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
0	reqwait_on_ispo_y	B'0	R/W	ISPOBUF (Y plane) wait processing enable 0: Disabled 1: Enabled

46.2.15 ISPBUF CIF Wait Cycle Setting Register (ISPBUF_AD_WAITCYC_CIF)

ISPBUF_AD_WAITCYC_CIF is used to specify the interval of waiting when the CIFIBUF or SIFOBUF in the ISPBUF makes a request to the F1DMAC. Counting is started immediately after the request is accepted. The buffers make no request during the specified interval. Values are in the range from 0 to 255 cycles. Whether wait processing is to be performed is controlled using the ISPBUF_AD_REQWAITON register.

Writing this register during operation is prohibited.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	waitcyc_cifi							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

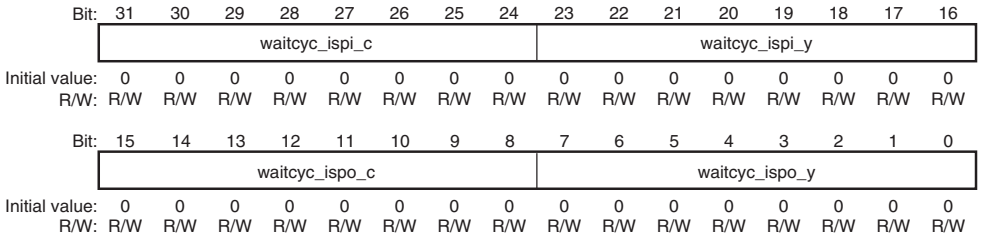
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	waitcyc_cifo							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
23 to 16	waitcyc_cifi [7:0]	H'00	R/W	CIFIBUF wait interval setting 0 to 255 cycles
15 to 8	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
7 to 0	waitcyc_cifo [7:0]	H'00	R/W	CIFOBUF wait interval setting 0 to 255 cycles

46.2.16 ISPBUF ISP Wait Cycle Setting Register (ISPBUF_AD_WAITCYC_ISP)

ISPBUF_AD_WAITCYC_ISP is used to specify the interval of waiting when the ISPIBUF or ISPOBUF in the ISPBUF makes a request to the F1DMAC. Counting is started immediately after the request is accepted. The buffers make no request during the specified interval. Values are in the range from 0 to 255 cycles. Whether wait processing is to be performed is controlled using the ISPBUF_AD_REQWAITON register.

Writing this register during operation is prohibited.



Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	waitcyc_ispi_c								waitcyc_ispi_y							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	waitcyc_ispo_c								waitcyc_ispo_y							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	waitcyc_ispi_c [7:0]	H'00	R/W	ISPIBUF (C plane) wait interval setting 0 to 255 cycles
23 to 16	waitcyc_ispi_y [7:0]	H'00	R/W	ISPIBUF (Y plane) wait interval setting 0 to 255 cycles
15 to 8	waitcyc_ispo_c [7:0]	H'00	R/W	ISPOBUF (C plane) wait interval setting 0 to 255 cycles
7 to 0	waitcyc_ispo_y [7:0]	H'00	R/W	ISPOBUF (Y plane) wait interval setting 0 to 255 cycles

46.2.17 ISPBUF Raw Data Noise Reduction Control Register (ISPBUF_AD_RAWNR)

ISPBUF_AD_RAWNR sets up the RAWNR function that achieves noise reduction using differential processing on the shot image data that is read by the ISPIBUF from SDRAM and the data image data output from the CAMIF.

Writing this register during operation is prohibited.

The determination algorithm for identifying the output data from the NR circuit is given below. The variables in the expressions are shot image: DataA(x,y), black image: DataB(x,y), output data: DataOut(x,y), and threshold value NLVLK(12 bits, defined in a register).

if (DataA(x,y) < DataB(x,y)) then DataOut(x,y) = DataB(x,y)

else if (first 2 pix's of the line) then DataOut(x,y) = DataA(x,y) - DataB(x,y)

else if (DataB(x,y) > NLVLK) then DataOut(x,y) = DataOut(x - 2,y)

else DataOut(x,y) = DataA(x,y) - DataB(x,y)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	NRCNT
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	NLVLK											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
16	NRCNT	B'0	R/W	Raw data noise reduction control 0: Disabled 1: Enabled
15 to 12	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
11 to 0	NLVLK[11:0]	H'000	R/W	Raw data noise level setting

46.2.18 ISPBUF F1DMAC Data Flow Select Register (ISPBUF_AD_F1SEL)

ISPBUF_AD_F1SEL is a register that specifies to which of F1DMAC(0) or F1DMAC(1) data are to be transferred from RAWIBUF, CIFIBUF, or CIFOBUF, or vice versa.

Writing this register during operation is prohibited.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	f1sel_rawi	—	—	—	f1sel_cifi	—	—	—	f1sel_cifo
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
24	f1sel_rawi	B'0	R/W	RAWIBUF data destination select 0: F1DMAC(0) 1: F1DMAC(1)

Bit	Bit Name	Initial Value	R/W	Description
23 to 21	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
20	f1sel_cifi	B'0	R/W	CIFIBUF data source select 0: F1DMAC(0) 1: F1DMAC(1)
19 to 17	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
16	f1sel_cifo	B'0	R/W	CIFOBUF data destination select 0: F1DMAC(0) 1: F1DMAC(1)
15 to 0	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.

46.2.19 ISPBUF Raw Data Swap Control Register (ISPBUF_AD_SWP_RAW)

ISPBUF_AD_SWP_RAW is a register that specifies whether data are to be swapped on a longword (32 bits), word (16 bits), or byte (8 bits) basis during RAWBUF data transfer.

Writing this register during operation is prohibited.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	lwswap_rawi	wswap_rawi	bswap_rawi	—	—	—	—	—	lwswap_rawo	wswap_rawo	bswap_rawo
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 11	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
10	lwswap_rawi	B'0	R/W	RAWIBUF long word swap control 0: No swap 1: Longword swap
9	wswap_rawi	B'0	R/W	RAWIBUF word swap control 0: No swap 1: Word swap
8	bswap_rawi	B'0	R/W	RAWIBUF byte swap control 0: No swap 1: Byte swap
7 to 3	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
2	lwswap_rawo	B'0	R/W	RAWOBUF long word swap control 0: No swap 1: Longword swap

Bit	Bit Name	Initial Value	R/W	Description
1	wswap_rawo	B'0	R/W	RAWOBUF word swap control 0: No swap 1: Word swap
0	bswap_rawo	B'0	R/W	RAWOBUF byte swap control 0: No swap 1: Byte swap

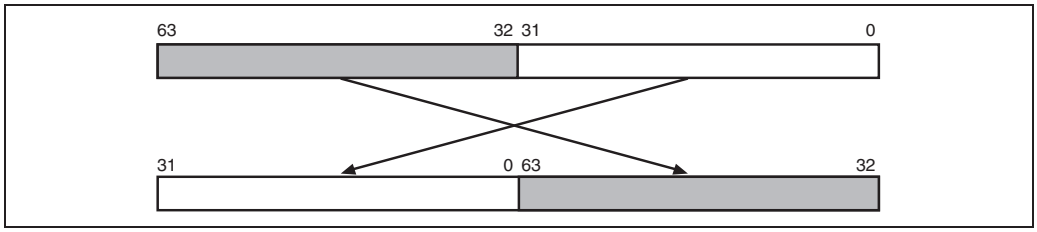


Figure 46.7 Data Arrangement before and after a Longword Swap

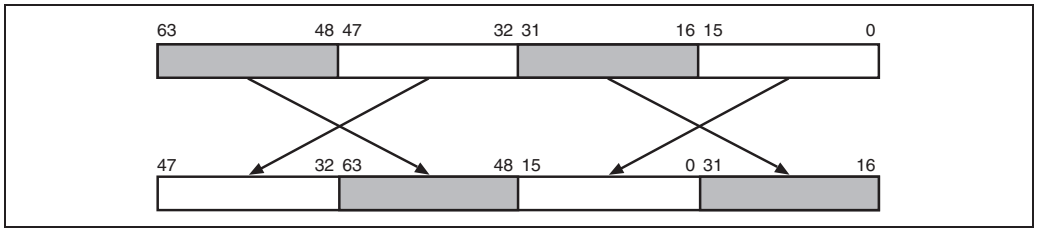


Figure 46.8 Data Arrangement before and after a Word Swap

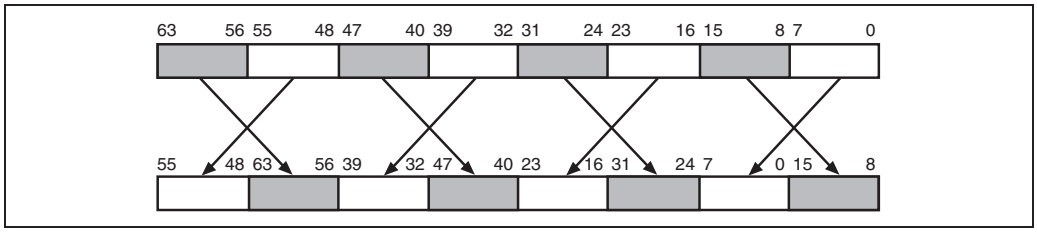


Figure 46.9 Data Arrangement before and after a Byte Swap

46.2.20 ISPBUF CIF Data Swap Control Register (ISPBUF_AD_SWP_CIF)

ISPBUF_AD_SWP_CIF is a register that specifies whether data are to be swapped on a longword (32 bits), word (16 bits), or byte (8 bits) basis during CIFIBUF/CIFOBUF and AM data transfer.

Writing this register during operation is prohibited.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	lwswap_amo	wswap_amo	bswap_amo
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	lwswap_cifi	wswap_cifi	bswap_cifi	—	—	—	—	—	lwswap_cifo	wswap_cifo	bswap_cifo
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 19	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
18	lwswap_amo	B'0	R/W	AM output longword swap control 0: No swap 1: Longword swap
17	wswap_amo	B'0	R/W	AM output word swap control 0: No swap 1: Word swap
16	bswap_amo	B'0	R/W	AM output byte swap control 0: No swap 1: Byte swap
15 to 11	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
10	lwswap_cifi	B'0	R/W	CIFIBUF longword swap control 0: No swap 1: Longword swap

Bit	Bit Name	Initial Value	R/W	Description
9	wswap_cifi	B'0	R/W	CIFIBUF word swap control 0: No swap 1: Word swap
8	bswap_cifi	B'0	R/W	CIFIBUF byte swap control 0: No swap 1: Byte swap
7 to 3	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
2	lwswap_cifo	B'0	R/W	CIFOBUF longword swap control 0: No swap 1: Longword swap
1	wswap_cifo	B'0	R/W	CIFOBUF word swap control 0: No swap 1: Word swap
0	bswap_cifo	B'0	R/W	CIFOBUF byte swap control 0: No swap 1: Byte swap

46.2.21 ISPBUF ISP Data Swap Control Register (ISPBUF_AD_SWP_ISP)

ISPBUF_AD_SWP_ISP is a register that specifies whether data are to be swapped on a longword (32 bits), word (16 bits), or byte (8 bits) basis during ISPIBUF/ISPOBUF data transfer.

Writing this register during operation is prohibited.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	lwswap_ispi_c	wswap_ispi_c	bswap_ispi_c	—	lwswap_ispi_y	wswap_ispi_y	bswap_ispi_y	—	lwswap_ispo_c	wswap_ispo_c	bswap_ispo_c	—	lwswap_ispo_y	wswap_ispo_y	bswap_ispo_y
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 15	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
14	lwswap_ispi_c	B'0	R/W	ISPIBUF (C plane) longword swap control 0: No swap 1: Longword swap
13	wswap_ispi_c	B'0	R/W	ISPIBUF (C plane) word swap control 0: No swap 1: Word swap
12	bswap_ispi_c	B'0	R/W	ISPIBUF (C plane) byte swap control 0: No swap 1: Byte swap
11	—	All 0	R	Reserved. This bit is always read as 0. The write value should always be 0.
10	lwswap_ispi_y	B'0	R/W	ISPIBUF (Y plane) longword swap control 0: No swap 1: Longword swap

Bit	Bit Name	Initial Value	R/W	Description
9	wswap_ispi_y	B'0	R/W	ISPIBUF (Y plane) word swap control 0: No swap 1: Word swap
8	bswap_ispi_y	B'0	R/W	ISPIBUF (Y plane) byte swap control 0: No swap 1: Byte swap
7	—	0	R	Reserved. This bit is always read as 0. The write value should always be 0.
6	lwswap_ispo_c	B'0	R/W	ISPOBUF (C plane) longword swap control 0: No swap 1: Longword swap
5	wswap_ispo_c	B'0	R/W	ISPOBUF (C plane) word swap control 0: No swap 1: Word swap
4	bswap_ispo_c	B'0	R/W	ISPOBUF (C plane) byte swap control 0: No swap 1: Byte swap
3	—	0	R	Reserved. This bit is always read as 0. The write value should always be 0.
2	lwswap_ispo_y	B'0	R/W	ISPOBUF (Y plane) longword swap control 0: No swap 1: Longword swap
1	wswap_ispo_y	B'0	R/W	ISPOBUF (Y plane) word swap control 0: No swap 1: Word swap
0	bswap_ispo_y	B'0	R/W	ISPOBUF (Y plane) byte swap control 0: No swap 1: Byte swap

46.2.22 ISPBUF Buffer Reservation Size Register (ISPBUF_AD_FIFOSLACK)

ISPBUF_AD_FIFOSLACK is a register that controls buffering in the ISPBUF. It generates a data transfer stop signal to the CAMIF or ISP when the size in data block units of the free space in the buffer falls below the specified value. Data overflow conditions may easily be avoided by specifying a larger value.

Writing this register during operation is prohibited.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	fifoslack_cifo	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	fifoslack_ispo	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 18	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
17 to 16	fifoslack_ cifo[1:0]	H'2	R/W	CIFOBUF buffer size setting Sends a STOP signal to the CAMIF if the free buffer area size is smaller than the value specified in this bit. 0: Setting prohibited 1 to 3: Specifies the threshold free data area size (Transfer size × 1 to 3)
15 to 2	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
1 to 0	fifoslack_ ispo[1:0]	H'2	R/W	ISPOBUF buffer size setting Sends a STOP signal to the CAMIF if the free buffer area size is smaller than the value specified in this bit. 0: Setting prohibited 1 to 3: Specifies the threshold free data area size (Transfer size × 1 to 3)

46.2.23 ISPBUF ISP Peripheral Module Activation Control Register (ISPBUF_AD_MSTP)

ISPBUF_AD_MSTP is a register that activates or deactivates the ISP peripheral modules.

Writing this register during operation is prohibited.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	mstp_n_rawbf	—	—	—	mstp_n_ispbf	—	—	—	mstp_n_f1dmac1	—	—	—	mstp_n_f1dmac0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
12	mstp_n_rawbf	B'0	R/W	RAWBUF module stop reset 0: Stops the module. 1: Resets the module stopped state.
11 to 9	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
8	mstp_n_ispbf	B'0	R/W	ISPBUF module stop reset 0: Stops the module. 1: Resets the module stopped state.
7 to 5	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
4	mstp_n_f1dmac1	B'0	R/W	F1DMAC0 module stop reset 0: Stops the module. 1: Resets the module stopped state.

Bit	Bit Name	Initial Value	R/W	Description
3 to 1	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
0	mstp_n_f1dmac0	B'0	R/W	F1DMAC1 module stop reset 0: Stops the module. 1: Resets the module stopped state.

46.2.24 ISPBUF Interrupt Monitor Register (ISPBUF_AD_INT_ALL)

ISPBUF_AD_INT_ALL is a register that combines the interrupt monitors of the ISP and ISP peripheral modules. It handles the bits that are de-masked by the monitor mask registers (ISPBUF_AD_INT_MASK0/1). Identify the source of the interrupt that is generated with this register and the status registers (ISPBUF_AD_INT_STAT0/1), then access the output source module and reset the interrupt.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	intreq_n_isp
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
0	intreq_n_isp	B'1	R/W	ISP interrupt monitor 0: Interrupt present 1: No Interrupt

46.2.25 ISPBUF Interrupt Status Register 0 (ISPBUF_AD_INT_STAT0)

ISPBUF_AD_INT_STAT0 is the interrupt monitor register for the ISP and ISP peripheral modules. It monitors the interrupts other than those which are excluded by the interrupt monitor mask register (ISPBUF_AD_INT_MASK0).

Each bit is cleared by accessing the output source module and resetting the corresponding interrupt.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	err_buf_cifi_stat	err_buf_cifo_stat	err_buf_ispo_stat	—	GQOSR_ERSTATUS_stat	GCTSRR_CAMINT_stat	GXXSRM_ISPREF_stat	GXXSRM_CAMEND_stat	GXXSRM_IPEND_stat	BFCSR_VD_stat	BFCSR_HD_stat	GAXSR_AWBEND_stat	GAXSR_AFCHK_stat	GWFSR_VKINT_stat	GCASR_CSDINT_stat
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	intreq_n_rawbf_2_stat	intreq_n_rawbf_1_stat	intreq_n_rawbf_0_stat	—	—	—	intreq_n_cmosif_stat	—	—	F1DMINT_ER_N_1_stat	F1DMINTA_N_1_stat	—	—	F1DMINT_ER_N_0_stat	F1DMINTA_N_0_stat
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R	R	R/W	R	R	R/W	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	—	All 0	R	Reserved. This bit is always read as 0. The write value should always be 0.
30	err_buf_cifi_stat	B'0	R/W	CIFIBUF buffer error interrupt monitor This interrupt is generated when an error occurs in the CIFIBUF in the ISPBUF. 0: No interrupt 1: Interrupt present
29	err_buf_cifo_stat	B'0	R/W	CIFOBUF buffer error interrupt monitor This interrupt is generated when an error occurs in the CIFOBUF in the ISPBUF. 0: No interrupt 1: Interrupt present
28	err_buf_ispo_stat	B'0	R/W	ISPOBUF buffer error interrupt monitor This interrupt is generated when an error occurs in the ISPOBUF in the ISPBUF. 0: No interrupt 1: Interrupt present

Bit	Bit Name	Initial Value	R/W	Description
26	GQQSR_ ERSTATUS_stat	B'0	R/W	CAMIF/ISP error interrupt monitor This interrupt is generated when an error occurs in the CAMIF or ISP. 0: No interrupt 1: Interrupt present
25	GCTSRR_ CAMINT_stat	B'0	R/W	CAMIF register update complete interrupt monitor This interrupt is generated when the update of the double-latch register in the CAMIF is completed. 0: No interrupt 1: Interrupt present
24	GXXSRM_ ISPREF_stat	B'0	R/W	CAMIF register update complete interrupt monitor This interrupt is generated when the update of the double-latch register in the ISP is completed. 0: No interrupt 1: Interrupt present
23	GXXSRM_ CAMEND_stat	B'0	R/W	CAMIF processing complete interrupt monitor This interrupt is generated when one screen of processing in the CAMIF is completed. 0: No interrupt 1: Interrupt present
22	GXXSRM_ IPEND_stat	B'0	R/W	ISP processing complete interrupt monitor This interrupt is generated when 1 unit (frame or strip) of processing in the ISP is completed. 0: No interrupt 1: Interrupt present
21	BFCSR_VD_stat	B'0	R/W	Sensor VD signal interrupt monitor This interrupt is generated when a valid edge of the VD signal is input from the sensor. (Not reflected when a CMOS sensor is used.) 0: No interrupt 1: Interrupt present

Bit	Bit Name	Initial Value	R/W	Description
20	BFCSR_HD_stat	B'0	R/W	Sensor HD signal interrupt monitor This interrupt is generated when a valid edge of the HD signal is input from the sensor. (Not reflected when a CMOS sensor is used.) 0: No interrupt 1: Interrupt present
19	GAXSR_ AWBEND_stat	B'0	R/W	AM detection complete interrupt monitor This interrupt is generated when the window detection in the AM module in the CAMIF is completed. 0: No interrupt 1: Interrupt present
18	GAXSR_AFCHK _stat	B'0	R/W	AF detection complete interrupt monitor This interrupt is generated when the window detection in the AF module in the CAMIF is completed. 0: No interrupt 1: Interrupt present
17	GWFSR_VKINT_ stat	B'0	R/W	VK accumulation complete interrupt monitor This interrupt is generated when the accumulation processing in the VK module in the CAMIF is completed. 0: No interrupt 1: Interrupt present
16	GCASR_ CSDINT_stat	B'0	R/W	CSD detection complete interrupt monitor This interrupt is generated when the detection of the CSD module in the ISP is completed. 0: No interrupt 1: Interrupt present
15	—	B'0	R	Reserved. This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
14	intreq_n_rawbf_2_stat	B'0	R/W	RAWBUF interrupt monitor 2 This interrupt is generated when an overflow occurs in the CMOSIF Link I/F buffer. 0: No interrupt 1: Interrupt present
13	intreq_n_rawbf_1_stat	B'0	R/W	RAWBUF interrupt monitor 1 This interrupt is generated when an overflow occurs in the RAWOBUF buffer. 0: No interrupt 1: Interrupt present
12	intreq_n_rawbf_0_stat	B'0	R/W	RAWBUF interrupt monitor 0 This interrupt is generated when an overflow occurs in the DIRBUF buffer. 0: No interrupt 1: Interrupt present
11 to 9	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
8	intreq_n_cmosif_stat	B'0	R/W	CSI2I interrupt monitor This flag is set by an interrupt occurring in the CSI2I module. (See section 41 for the CSI2I interrupt sources.) 0: No interrupt 1: Interrupt present
7 to 6	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
5	F1DMINT_ERN_1_stat	B'0	R/W	F1DMAC(1) error interrupt monitor This flag is set by an error interrupt occurring in the F1DMAC(1). 0: No interrupt 1: Interrupt present

Bit	Bit Name	Initial Value	R/W	Description
4	F1DMINTA_N_1_stat	B'0	R/W	F1DMAC(1) common interrupt monitor This flag is set by a common interrupt occurring in the F1DMAC(1). 0: No interrupt 1: Interrupt present
3 to 2	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
1	F1DMINT_ERN_0_stat	B'0	R/W	F1DMAC(0) error interrupt monitor This flag is set by an interrupt occurring in the F1DMAC(0). 0: No interrupt 1: Interrupt present
0	F1DMINTA_N_0_stat	B'0	R/W	F1DMAC(0) common interrupt monitor This flag is set by a common interrupt occurring in the F1DMAC(0). 0: No interrupt 1: Interrupt present

46.2.26 ISPBUF Interrupt Status Register 1 (ISPBUF_AD_INT_STAT1)

ISPBUF_AD_INT_STAT1 is the interrupt monitor register for the ISP and ISP peripheral modules. It monitors the interrupts other than those which are excluded by the interrupt monitor mask register (ISPBUF_AD_INT_MASK1).

Each bit is cleared by accessing the output source module and reset the corresponding interrupt.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	F1DMINT_N_1_stat							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	F1DMINT_N_0_stat							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
23 to 16	F1DMINT_N_1_stat[7:0]	H'00	R/W	F1DMAC(1) interrupt monitor This interrupt is generated when an interrupt occurs in the corresponding F1DMAC(1) channel. (Bit 7 corresponds to channel 0, …, bit 0 corresponds to channel 7.) 0: No interrupt (each channel) 1: Interrupt present (each channel)
15 to 8	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
7 to 0	F1DMINT_N_0_stat[7:0]	H'00	R/W	F1DMAC(0) interrupt monitor This interrupt is generated when an interrupt occurs in the corresponding F1DMAC(0) channel. (Bit 7 corresponds to channel 0, …, bit 0 corresponds to channel 7.) 0: No interrupt (each channel) 1: Interrupt present (each channel)

46.2.27 ISPBUF Interrupt Monitor Mask Register (ISPBUF_AD_INT_MASK0)

ISPBUF_AD_INT_MASK0 specifies the masks for the ISP and ISP peripheral module interrupts to be monitored. The bits that are masked in this register are reflected in ISPBUF_AD_INT_STAT0 and ISPBUF_AD_INT_ALL. Note that there is no mask register for the F1DMAC peripheral module interrupts. The F1DMAC interrupts must be masked by the mask feature of the F1DMAC proper.

Each bit is cleared by accessing the output source module and resetting the corresponding interrupt.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	err_buf_cifi_msk	err_buf_cifo_msk	err_buf_ispo_msk	—	GQQSR_ERSTATUS_msk	GCTSRR_CAMINT_msk	GXXSRM_ISPREF_msk	GXXSRM_CAMEND_msk	GXXSRM_IPEND_msk	BFCSR_VD_msk	BFCSR_HD_msk	GAXSR_AWBEND_msk	GAXSR_AFCHK_msk	GWFSR_VKINT_msk	GCASR_CSDINT_msk
Initial value:	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	intreq_n_rawbf_2_msk	intreq_n_rawbf_1_msk	intreq_n_rawbf_0_msk	—	—	—	intreq_n_cmosif_msk	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R	R	R/W	R	R	R/W	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	—	B'0	R	Reserved. This bit is always read as 0. The write value should always be 0.
30	err_buf_cifi_msk	B'0	R/W	CIFIBUF buffer error interrupt monitor mask 0: Masked 1: Not masked
29	err_buf_cifo_msk	B'1	R/W	CIFOBUF buffer error interrupt monitor mask 0: Masked 1: Not masked
28	err_buf_ispo_msk	B'1	R/W	ISPOBUF buffer error interrupt monitor mask 0: Masked 1: Not masked
27	—	B'0	R	Reserved. This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
26	GQQSR_ ERSTATUS_msk	B'0	R/W	CAMIF/ISP error interrupt mask 0: Masked 1: Not masked
25	GCTSRR_ CAMINT_msk	B'0	R/W	CAMIF register update complete interrupt mask 0: Masked 1: Not masked
24	GXXSRM_ ISPREF_msk	B'0	R/W	ISP register update complete interrupt monitor mask 0: Masked 1: Not masked
23	GXXSRM_ CAMEND_msk	B'0	R/W	CAMIF processing complete interrupt monitor mask 0: Masked 1: Not masked
22	GXXSRM_ IPEND_msk	B'0	R/W	ISP processing complete interrupt monitor mask 0: Masked 1: Not masked
21	BFCSR_VD_msk	B'0	R/W	Sensor VD signal interrupt monitor mask 0: Masked 1: Not masked
20	BFCSR_HD_msk	B'0	R/W	Sensor HD signal interrupt monitor mask 0: Masked 1: Not masked
19	GAXSR_ AWBEND_msk	B'0	R/W	AM detection complete interrupt monitor mask 0: Masked 1: Not masked
18	GAXSR_AFCHK_ msk	B'0	R/W	AF detection complete interrupt monitor mask 0: Masked 1: Not masked
17	GWFSR_ VKINT_msk	B'0	R/W	VK accumulation complete interrupt monitor mask 0: Masked 1: Not masked

Bit	Bit Name	Initial Value	R/W	Description
16	GCASR_ CSDINT_msk	B'0	R/W	CSD detection complete interrupt mask 0: Masked 1: Not masked
15	—	B'0	R	Reserved. This bit is always read as 0. The write value should always be 0.
14	intreq_n_rawbf_ 2_msk	B'0	R/W	RAWBUF interrupt monitor mask bit 2 0: Masked 1: Not masked
13	intreq_n_rawbf_ 1_msk	B'0	R/W	RAWBUF interrupt monitor mask bit 1 0: Masked 1: Not masked
12	intreq_n_rawbf_ 0_msk	B'0	R/W	RAWBUF interrupt monitor mask bit 0 0: Masked 1: Not masked
11 to 9	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
8	intreq_n_cmosif_ msk	B’0	R/W	CSI2I interrupt monitor mask bit 0: Masked 1: Not masked
7 to 0	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.

46.2.28 ISPBUF CAMIF Control register (ISPBUF_AD_CAMIF1)

ISPBUF_AD_CAMIF1 is a register that controls the CCD interface in the CAMIF. Enabling this register makes the CCD interface available.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CK1X_ CAMC LK0EN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
0	CK1X_ CAMCLK0EN	H'00	R/W	CAMIF CCDI/F control 0: The CAMIF CCD I/F stopped. 1: The CAMIF CCD I/F operates.

46.2.29 ISPBUF CMOSIF Monitor Register 0 (ISPBUF_AD_CMOSIF0)

ISPBUF_AD_CMOSIF0 is a monitor register for the MIPI-CSI Link module (CSI2I). It monitors the information detected by the CSI2I.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	CMOSIF_SIZEH												
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CMOSIF_SIZEV												
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
28 to 16	CMOSIF_ SIZE[12:0]	H'000	R/W	CSI2I horizontal pixel size
15 to 13	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
13 to 0	CMOSIF_ SIZEV[12:0]	H'000	R/W	CSI2I vertical pixel size

46.2.30 ISPBUF CMOSIF Monitor Register 1 (ISPBUF_AD_CMOSIF1)

ISPBUF_AD_CMOSIF1 is a monitor register for the MIPI-CSI Link module (CSI2I). It monitors the information detected by the CSI2I.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	CMOSIF_DPCM_stat	—	—	CMOSIF_FORM_stat					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
8	CMOSIF_ DPCM_stat	B'0	R/W	CSI2I completion format control
7 to 6	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
5 to 0	CMOSIF_ FORM_stat[5:0]	H'00	R/W	CSI2I format control

46.2.31 ISPBUF CIFIBUF Byte Count Register (ISPBUF_AD_BC_CIFI)

ISPBUF_AD_BC_CIFI is a register that indicates the byte count of the data that is transferred through the CIFIBUF.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	BC_CIFI[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BC_CIFI[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	BC_CIFI [31:0]	H'0000 0000	R	CIFIBUF byte count

46.2.32 ISPBUF CIFO Byte Count Register (ISPBUF_AD_BC_CIFO)

ISPBUF_AD_BC_CIFO is a register that indicates the byte count of the data that is transferred through the CIFOBUF.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	BC_CIFO[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BC_CIFO[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	BC_CIFO [31:0]	H'0000 0000	R	CIFOBUF byte count

46.2.33 ISPBUF ISPI_Y Byte Count Register (ISPBUF_AD_BC_ISPIY)

ISPBUF_AD_BC_ISPIY is a register that indicates the byte count of the data that is transferred through the ISPIBUF (Y plane).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	BC_ISPIY[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BC_ISPIY[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	BC_ISPIY [31:0]	H'0000 0000	R	ISPIBUF (Y plane) byte count

46.2.34 ISPBUF ISPI_C Byte Count Register (ISPBUF_AD_BC_ISPIC)

ISPBUF_AD_BC_ISPIC is a register that indicates the byte count of the data that is transferred through the ISPIBUF (C plane).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	BC_ISPIC[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BC_ISPIC[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	BC_ISPIC [31:0]	H'0000 0000	R	ISPIBUF (C plane) byte count

46.2.35 ISPBUF ISPO_Y Byte Count Register (ISPBUF_AD_BC_ISPOY)

ISPBUF_AD_BC_ISPOY is a register that indicates the byte count of the data that is transferred through the ISPOBUF (Y plane).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	BC_ISPOY[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BC_ISPOY[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	BC_ISPOY [31:0]	H'0000 0000	R	ISPOBUF (Y plane) byte count

46.2.36 ISPBUF ISPO_C Byte Count Register (ISPBUF_AD_BC_ISPOC)

ISPBUF_AD_BC_ISPOC is a register that indicates the byte count of the data that is transferred through the ISPOBUF (C plane).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	BC_ISPOC[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BC_ISPOC[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	BC_ISPOC [31:0]	H'0000 0000	R	ISPOBUF (C plane) byte count

46.2.37 Usage Note

(1) Restrictions to be applied during operation

Do not attempt to stop any module while the ISP and ISP peripheral modules are running.

46.3 RAWBUF

The raw data buffer (RAWBUF) is a module that takes in the image data (32-bit packed data) from the CSI2I (CMOSIF-Link) and transfers it to the external memory (SDRAM) through the camera head interface block (CAMIF) in the image processing block or the F1 bus based on the starting and ending information of the line/frame. It also takes in the image data from the external memory (SDRAM) through the F1 bus and transfers it to the camera head interface block (CAMIF) in the image processing block.

The formats of data input from the CMOSIF-Link can be 12-bit, 10-bit, or 8-bit parallel.

46.3.1 RAWBUF Function Summary

Table 46.7 summarizes the functions of the RAWBUF and figure 46.10 shows its internal block diagram.

Table 46.7 RAWBUF Function Summary

Item	Function Summary
Frequency	• CMOSIF-Link IF clock (BCLK_INTR): 166 MHz maximum • CAMIF clock (CAMCLK): 200 MHz maximum • System clock (ICLK): 200 MHz maximum These clocks run in an asynchronous mode in which they are free from any mutual phase restrictions.
CMOSIF-Link input data format	One of the following formats must be selected: • 12-bit parallel data: 12 bits/pixel • 10-bit parallel data: 10 bits/pixel • 8-bit parallel data: 8 bits/pixel (with/without compression) • Minimum line size: 4 pixels • Minimum retrace time: 17 cycles (BCLK_INTR)
DMA bus interface	Conforms to the F1 Bus Specification. • Data bus width: 64 bits • Operand size: RAWOBUF 16/32/64 words : RAWIBUF 16/32 words
Control bus interface	Conforms to the C Bus Specification. • Area: 64K bytes • Word (32 bits) access only

Item	Function Summary
Interrupt request source	• DIRBUF overflow interrupt • RAWOBUF overflow interrupt • CMOSIF overflow interrupt
Available buffer configuration	• DIRBUF: For direct path output 32 bits × 4 words × 1 plane • RAWOBUF: For F1 path output (SRAM) 64 bits × 16/32/64 words × 4 × 8 planes • RAWIBUF: For F1 path input 64 bits × 16/32 words × 2 planes

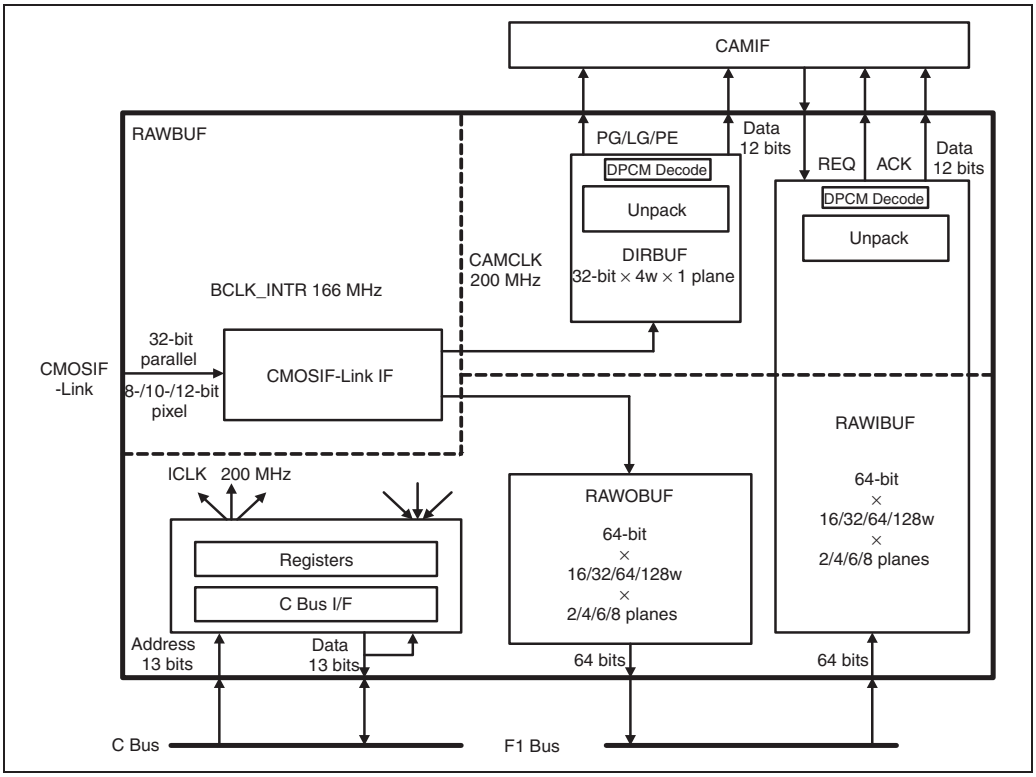


Figure 46.10 RAWBUF Block Diagram

46.3.2 Data Formats

A data format of the input from the CMOSIF-Link is shown in figure 46.11.

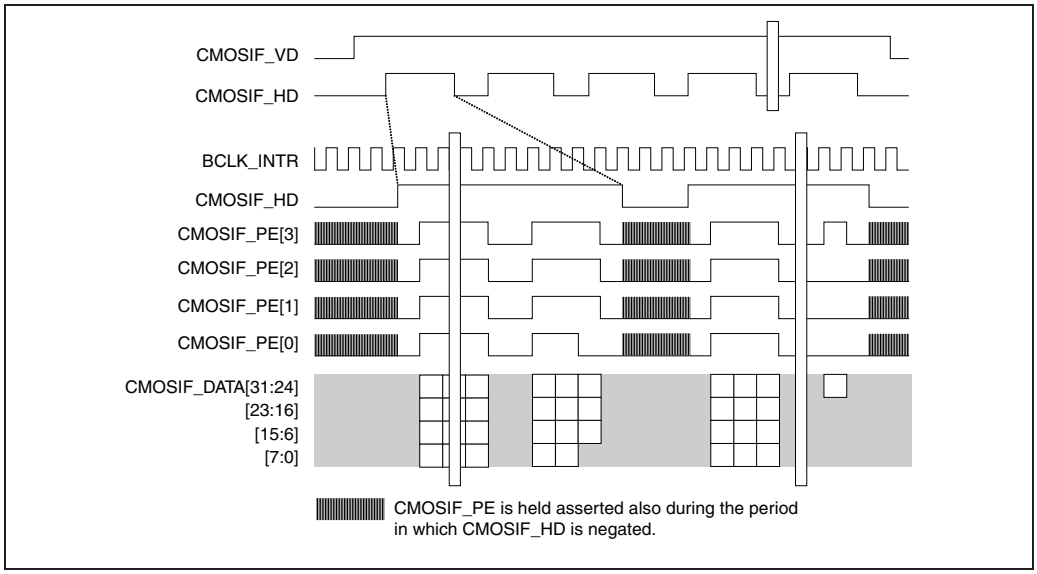


Figure 46.11 Format of the Input from the CMOSIF-Link

(1) 12-bit parallel data

An even number of pixels are always processed, in 8 pixel units with a period of 3 × BCLK_INTR in 12-bit raw packed mode.

Figure 46.12 shows the format (12-bit parallel data) of the data received from the CMOSIF-Link.

The number of pixels is not always a multiple of 8; odd pixels (2/4/6 bytes) can occur. The effective bytes are indicated in CMOSIF_PE.

- Pixels up to pixel 1 are output (CMOSIF_PE[3:1] asserted) when the residue is 2.
- Pixels up to pixel 3 are output (CMOSIF_PE[3:2] asserted) when the residue is 4.
- Pixels up to pixel 5 are output (CMOSIF_PE[3] asserted) when the residue is 6.

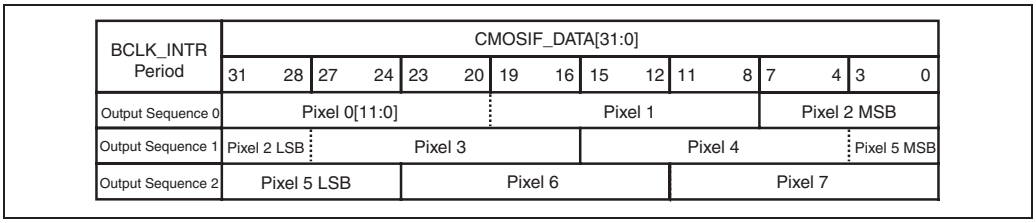


Figure 46.12 Format of Data Received from the CMOSIF-Link (12-Bit Parallel Data)

(2) 10-bit parallel data

A multiple of 4 of pixels are always processed, in 16 pixel units with a period of 5 × BCLK_INTR in 10-bit raw packed mode

Figure 46.13 shows the format (10-bit parallel data) of the data received from the CMOSIF-Link.

The number of pixels is not always a multiple of 16; odd pixels (4/8/12 bytes) can occur. The effective bytes are indicated in CMOSIF_PE.

- Pixels up to pixel 3 are output (CMOSIF_PE[3] asserted) when the residue is 4.
- Pixels up to pixel 7 are output (CMOSIF_PE[3:2] asserted) when the residue is 8.
- Pixels up to pixel 11 are output (CMOSIF_PE[3:1] asserted) when the residue is 12.

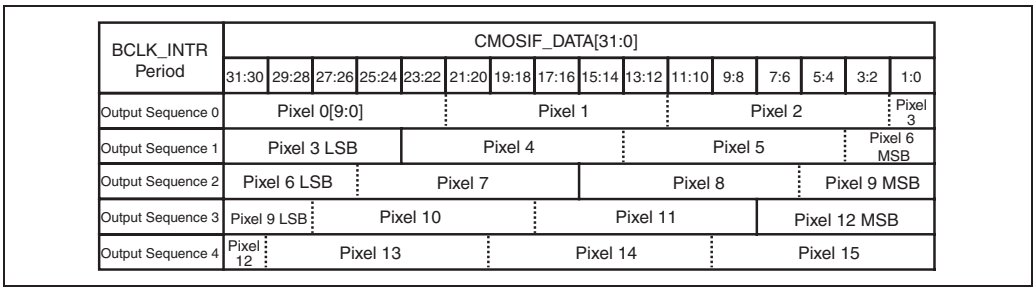


Figure 46.13 Format of Data Received from the CMOSIF-Link (10-Bit Parallel Data)

(3) 8-bit parallel data

In 8-bit packed mode, pixels are processed in 8-bit raw or 10- to 8-bit DPCM/PCM Compression mode, in 4 pixel units with a period of 1 × BCLK_INTR.

Figure 46.14 shows the format (8-bit parallel data) of the data received from the CMOSIF-Link.

The number of pixels is not always a multiple of 4; odd pixels (1/2/3 bytes) can occur. The effective bytes are indicated in CMOSIF_PE.

- Pixels up to pixel 0 are output (CMOSIF_PE[3] asserted) when the residue is 1.
- Pixels up to pixel 1 are output (CMOSIF_PE[3:2] asserted) when the residue is 2.
- Pixels up to pixel 2 are output (CMOSIF_PE[3:1] asserted) when the residue is 3.

BCLK_INTR Period	CMOSIF_DATA[31:0]															
	31	28	27	24	23	20	19	16	15	12	11	8	7	4	3	0
Output Sequence 0	Pixel 0[7:0]				Pixel 1				Pixel 2				Pixel 3			

Figure 46.14 Format of Data Received from the CMOSIF-Link (8-Bit Parallel Data)

Register Description

(1) Register read/write restrictions

Restrictions on register reads and writes are given below. The system operation may fail if the integrity of the following register operations is not guaranteed:

1. Writing a 1 into any read-only register bit or reserved area is prohibited. Do not set any value other than the specified values.
2. There are cases in which a nonzero value is read from a read-only bit. Such a value must not be rewritten.
3. Writing into any registers (bits) that are disallowed for writes during operation is prohibited while some operation is in progress (reads are allowed). The operating state of the RAWBUF can be identified by reading the RAWBUF operation register or by identifying the end of the F1DMAC transfer.

(2) Terms and abbreviations used in this document

A term that is used in this document is explained below.

1. "Software reset" refers to a forced reset into the RAWBUF internal circuit. This means that any attempt to effect a module reset while the RAWBUF is running normally might place the ISPBUF peripheral hardware into an inoperative state.

(3) List of Registers

The register configuration of the RAWBUF registers is summarized in table 46.8. The relationship between the processing modes and register states is given in table 46.9, Processing Modes and Register States.

Table 46.8 RAWBUF Register Configuration

Register Name	Abbreviation	R/W	Address	Access Size
RAWBUF control register	RAWBUF_RBCR	R/W	H'FE8F 0000	32
RAWBUF initialization register	RAWBUF_RBINITR	R/W	H'FE8F 0004	32
RAWBUF operating mode register	RAWBUF_RBMDR	R/W	H'FE8F 0008	32
RAWBUF RAWOBUF DMA operating mode register	RAWBUF_RBOBFMDR	R/W	H'FE8F 000C	32
RAWBUF RAWIBUF DMA operating mode register	RAWBUF_RBIBFMDR	R/W	H'FE8F 0010	32
RAWBUF Interrupt mask register	RAWBUF_RBINTMSKR	R/W	H'FE8F 0014	32
RAWBUF status register	RAWBUF_RBINTSTSR	R/W	H'FE8F 0018	32
RAWBUF raw format error 1 register	RAWBUF_RBFER1R	R/W	H'FE8F 001C	32
RAWBUF raw format error 2 register	RAWBUF_RBFER2R	R/W	H'FE8F 0020	32
RAWBUF prohibited area*[1]	—	—	H'FE8F 0024 to H'FE8F 0030	—
RAWBUF H/V status register	RAWBUF_RBSESTSR	R	H'FE8F 0034	32
RAWBUF RAWOBUF internal status register 1	RAWBUF_RBOBFSTSR1	R	H'FE8F 0038	32
RAWBUF RAWOBUF internal status register 2	RAWBUF_RBOBFSTSR2	R	H'FE8F 003C	32
RAWBUF RAWIBUF internal status register 1	RAWBUF_RBIBFSTSR1	R	H'FE8F 0040	32
RAWBUF RAWIBUF internal status register 2	RAWBUF_RBIBFSTSR2	R	H'FE8F 0044	32
RAWBUF prohibited area*[1]	—	—	H'FE8F 0048 to H'FE8F 00FC	—
RAWBUF buffer access mode register	RAWBUF_RBACCMDR	R/W	H'FE8F 0100	32

Register Name	Abbreviation	R/W	Address	Access Size
RAWBUF prohibited area*1	—	—	H'FE8F 0104 to H'FE8F 01FC	—
RAWBUF RAWIBUF*2	—	R/W	H'FE8F 2000 to H'FE8F 3FFC	32
RAWBUF RAWOBUF*3	—	R/W	H'FE8F 4000 to H'FE8F 5FFC	32

Notes: 1. Normal operation is not guaranteed if an attempt is made to write into any prohibited area.
Reading from a prohibited area will yield an undefined value.
2. The accessible area is limited by the IBUFASP and IOPSZ bits of the RAWIBUF DMA operating mode register.
3. The accessible area is limited by the OBUFASP and OOPSZ bits of the RAWOBUF DMA operating mode register.

Table 46.9 Processing Modes and Register States

Abbreviation	Reset*	Module Standby
RAWBUF_RBCR	Initialized	Retained
RAWBUF_RBINITR	Initialized	Retained
RAWBUF_RBMDR	Initialized	Retained
RAWBUF_RBOBFMDR	Initialized	Retained
RAWBUF_RBIBFMDR	Initialized	Retained
RAWBUF_RBINTMSKR	Initialized	Retained
RAWBUF_RBINTSTSR	Initialized	Retained
RAWBUF_RBFER1R	Initialized	Retained
RAWBUF_RBFER2R	Initialized	Retained
RAWBUF_RBSESTSR	Initialized	Retained
RAWBUF_RBOBFSTSR1	Initialized	Retained
RAWBUF_RBOBFSTSR2	Initialized	Retained
RAWBUF_RBIBFSTSR1	Initialized	Retained
RAWBUF_RBIBFSTSR2	Initialized	Retained
RAWBUF_RBACCMDR	Initialized	Retained

Note: * See section 1-D.

46.3.3 RAWBUF Control Register (RAWBUF_RBCR)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	RAWBUFEN	—	—	OBUFEN	IBUFEN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
4	RAWBUFEN	B'0	R/W	RAWBUF receive enable 0: Disables raw data receive operation. 1: Enables raw data receive operation.
3, 2	—	B'00	R	Reserved. These bits are always read as 0. The write value should always be 0.
1	OBUFEN	B'0	R/W	RAWOBUF start/stop 0: Stops RAWOBUF operation. 1: Starts RAWOBUF operation.
0	IBUFEN	B'0	R/W	RAWIBUF start/stop 0: Stops RAWIBUF operation. 1: Starts RAWIBUF operation.

(1) RAWBUFEN (RAWBUF receive enable) bit (b4)

This bit enables or disables the operation to receive raw data from the CMOSIF-Link.

Clearing this bit to 0 disables the raw data receive operation.

Setting this bit to 1 enables the raw data receive operation.

(2) OBUFEN (RAWOBUF start/stop) bit (b1)

This bit starts or stops the RAWOBUF operation.

Clearing this bit to 0 stops the RAWOBUF operation.

Setting this bit to 1 starts the RAWOBUF operation.

When the RAWOBUF operation is stopped, the RAWBUF neither writes the data input to the RAWOBUF into the FIFO buffer nor issues a DMA request to the F1 bus.

(3) IBUFEN (RAWIBUF start/stop) bit (b0)

This bit starts or stops the RAWIBUF operation.

Clearing this bit to 0 stops the RAWIBUF operation.

Setting this bit to 1 starts the RAWIBUF operation.

When the RAWIBUF operation is stopped, the RAWBUF neither issues a DMA request to the F1 bus nor responds to any data transfer requests from the CAMIF.

Notes on the sequence of setting up the registers

- When using the DIRBUF
  After setting up the RBMDR register, provide intervals of 4 clocks or longer using BCLK and CAMCLK, respectively, before setting the RAWBUFEN bit of this register.
- When using the RAWOBUF
  After setting up the RBMDR register, provide an interval of 4 clocks or longer using BCLK before setting the OBUFEN bit of this register.
- When using the RAWIBUF
  After setting up the RBMDR and RBIBFMDR registers, provide an interval of 4 clocks or longer using CAMCLK before setting the IBUFEN of this register.

46.3.4 RAWBUF Initialization Register (RAWBUF_RBINITR)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RBFRST
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
0	RBFRST	B'0	R/W	RAWBUF reset 0: Does not reset the RAWBUF. 1: Resets the RAWBUF.

(1) RBFRST (RAWBUF reset) bit (b0)

This bit resets the RAWBUF.

Clearing this bit to 0 does not reset the RAWBUF.

Any reset attempt made by setting this bit to 1 cannot be canceled even by clearing this bit to 0.

Setting this bit to 1 resets the RAWBUF. This bit is automatically cleared to 0 when the RAWBUF reset sequence is completed.

Be sure to reset the RAWBUF before restarting it after stopping it.

The following registers are not cleared by this rest function:

(1) RAWBUF Control Register (RAWBUF_RBCR)

(2) RAWBUF Operating Mode Register (RAWBUF_RBMDR)

(3) RAWOBUF DMA Operating Mode Register (RAWBUF_RBOBFMDR)

(4) RAWIBUF DMA Operating Mode Register (RAWBUF_RBIBFMDR)

(5) RAWBUF Interrupt Mask Register (RAWBUF_RBINTMSKR)

(6) RAWBUF Buffer Access Mode Register (RAWBUF_RBACCMDR)

The following registers are cleared by this reset function:

(1) RAWBUF Status Register (RAWBUF_RBINTSTSR)
COVF bit, OOVF bit, DOVF bit

(2) RAW Format Error 1 Register (RAWBUF_RBFER1R)
DERRV bit, DERRH bit

(3) RAW Format Error 2 Register (RAWBUF_RBFER2R)
FERRH bit

(4) RAWBUF Receive Size Register (RAWBUF_RBRXSZR)
PIXSZ bit, LINSZ bit

(5) RAWBUF H/V Status Register (RAWBUF_RBSESTSR)
H bit, V bit

(6) RAWOBUF Internal Status Register 1 (RAWBUF_RBOBFSTSR1)
OFUL bit, OEMP bit, ODRQ bit, ODCPLT bit

(7) RAWOBUF Internal Status Register 2 (RAWBUF_RBOBFSTSR2)
OWPTR bit, ORPTR bit

(8) RAWIBUF Internal Status Register 1 (RAWBUF_RBIBFSTSR1)
IFUL bit, IEMP bit, IDRQ bit, IDCPLT bit

(9) RAWIBUF Internal Status Register 2 (RAWBUF_RBIBFSTSR2)
IWPTR bit, IRPTR bit

46.3.5 RAWBUF Operating Mode Register (RAWBUF_RBMDR)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	RAWPIX[9:8]		—	—	—	—	—	—	—	PTHSEL
Initial value:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
9, 8	RAWPIX[9:8]	B'01	R/W	Raw data pixel size select 00: Sets the size of the raw data input to 12 bits/pixel. 01: Sets the size of the raw data input to 10 bits/pixel. 10: Sets the size of the raw data input to 8 bits/pixel. 11: Sets the size of the raw data input to 8 bits/pixel (DPCM/PCM).
7 to 1	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
0	PTHSEL	B'1	R/W	Raw data output path select 0: Directs the raw data to the F1 bus. 1: Directs the raw data to the CAMIF (initial value).

(1) RAWPIX (Raw data pixel size select) bits (b9, b8)

These bits define the pixel size of the raw data input to the RAWBUF.

Setting these bits to 00 sets the pixel size of the raw data input to 12 bits/pixel.

Setting these bits to 01 sets the pixel size of the raw data input to 10 bits/pixel (initial value).

Setting these bits to 10 sets the pixel size of the raw data input to 8 bits/pixel.

Setting these bits to 11 sets the pixel size of the raw data input to 8 bits/pixel (DPCM/PCM).

(2) PTHSEL (Raw data output path select) bit (b0)

This bit defines the destination of the raw data output.

Clearing this bit to 0 directs the raw data to the F1 bus and from the F1 bus to the CAMIF (F1 path).

Setting this bit to 1 directs the raw data to the CAMIF. The data are not transferred from the F1 bus to the CAMIF (direct path) (initial value).

46.3.6 RAWBUF RAWOBUF DMA Operating Mode Register (RAWBUF_RBOBFMDR)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	OBUFASP[25:24]		—	—	—	ODRQE	—	—	OOPSZ[17:16]	
Initial value:	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R	R/W	R	R	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	OITVLE	ODRITVL[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
25 to 24	OBUFASP[25:24] (RAWOBUF Buffer Aspect)	B'11	R/W	Buffer plane count select 01: Number of planes to be used is 4 planes. 11: Number of planes to be used is 8 planes. Other than the other values: Reserved.
23 to 21	—	B'000	R	Reserved. These bits are always read as 0. The write value should always be 0.
20	ODRQE	B'0	R/W	DMA request enable 0: Disables DMA requests to be issued. 1: Enables DMA requests to be issued.
19 to 18	—	B'00	R	Reserved. These bits are always read as 0. The write value should always be 0.
17 to 16	OOPSZ[17:16]	B'10	R/W	DMA operand size 00: Sets the operand size to 16 data blocks. 01: Sets the operand size to 32 data blocks. 10: Sets the operand size to 64 data blocks. Other than the other values: Reserved.
15 to 9	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
8	OITVLE	B'0	R/W	DMA request interval setting enable 0: Disables the DMA request interval setting. 1: Enables the DMA request interval setting.
7 to 0	ODRITVL[7:0]	All 0	R/W	DMA request interval These bits define the minimum number of cycles required from the time the response (Acknowledge) to the last DMA request is recognized till the time the issuance of the next DMA request is enabled. Set value + 1 = Minimum cycle count (1 cycle to 256 cycles)

(1) OBUFASP (buffer plane count select) bits (b25, b24)

These bits define the number of RAWOBUF buffer planes to be used.

4 planes are used when these bits are set to 01.

8 planes are used when these bits are set to 11 (initial value).

(2) ODRQE (DMA request enable) bit (b20)

This bit enables DMA requests to be issued from the RAWOBUF.

When this bit is cleared to 0, no DMA request is issued even when the DMA request issuance conditions are established.

When this bit is set to 1, a DMA request is issued when the DMA request issuance conditions are established.

(3) OOPSZ (DMA operand size) bits (b17, b16)

These bits define the size of the operands (DMA transfer size) for RAWOBUF DMA transfers.

When these bits are set to 00, DMA transfers occur in units of 16 data blocks (64 bits × 16 words).

When these bits are set to 01, DMA transfers occur in units of 32 data blocks (64 bits × 32 words).

When these bits are set to 10, DMA transfers occur in units of 64 data blocks (64 bits × 64 words) (initial value).

(4) OITVLE (DMA request interval setting enable) bit (b8)

This bit enables or disables the DMA request interval setting that is defined in the ODRITVL bits.

Clearing this bit to 0 disables the DMA request interval setting that is defined in the ODRITVL bits.

Setting this bit to 1 enables the DMA request interval setting that is defined in the ODRITVL bits.

When the DMA request interval setting is disabled, a DMA request is issued immediately when the DMA request issuance conditions for the next DMA request are established after the response (Acknowledge) to the last DMA request is recognized.

(5) ODRITVL (DMA request enable setting) bits (b7 to b0)

These bits define the minimum number of cycles required from the time the response (Acknowledge) to the last DMA request is recognized till the time the issuance of the next DMA request is enabled.(1 to 256 cycles).

The issuance of the next DMA request is enabled before the data transfer for the last DMA request is completed. The setting made in these bits is enabled when the OITVLE bit is set to 1.

46.3.7 RAWBUF RAWIBUF DMA Operating Mode Register (RAWBUF_RBIBFMDR)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	IBUFASP [25:24]		—	—	—	IDRQE	—	—	IOPSZ[17:16]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R	R/W	R	R	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	IITVLE	IDRITVL[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
25 to 24	IBUFASP[25:24] (RAWIBUF Buffer Aspect)	B'00	R/W	Buffer plane count select 00: Number of planes to be used 2 planes Other than the other values: Reserved.
23 to 21	—	B'0000	R	Reserved. These bits are always read as 0. The write value should always be 0.
20	IDRQE	B'0	R/W	DMA request enable 0: Disables DMA requests to be issued. 1: Enables DMA requests to be issued.
19, 18	—	B'00	R	Reserved. These bits are always read as 0. The write value should always be 0.
17, 16	IOPSZ[17:16]	B'01	R/W	DMA operand size 00: Sets the operand size to 16 data blocks. 01: Sets the operand size to 32 data blocks. Others: Reserved.
15 to 9	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
8	IITVLE	B'0	R/W	DMA request interval setting enable 0: Disables the DMA request interval setting. 1: Enables the DMA request interval setting.
7 to 0	IDRITVL[7:0]	All 0	R/W	DMA request interval These bits define the minimum number of cycles required from the time the response (Acknowledge) to the last DMA request is recognized till the time the issuance of the next DMA request is enabled. Set value + 1 = Minimum cycle count (1 cycle to 256 cycles)

(1) IBUFASP (buffer plane count select) bits (b25, b24)

These bits define the number of RAWIBUF buffer planes to be used.

2 planes are used when these bits are set to 00 (initial value).

(2) IDRQE (DMA request enable) bit (b20)

This bit enables DMA requests to be issued from the RAWIBUF.

When this bit is cleared to 0, no DMA request is issued even when the DMA request issuance conditions are established.

When this bit is set to 1, a DMA request is issued when the DMA request issuance conditions are established.

(3) IOPSZ (DMA operand size) bits (b17, b16)

These bits define the size of the operands (DMA transfer size) for RAWIBUF DMA transfers.

When these bits are set to 00, DMA transfers occur in units of 16 data blocks (64 bits × 16 words).

When these bits are set to 01, DMA transfers occur in units of 32 data blocks (64 bits × 32 words) (initial value).

(4) IITVLE (DMA request interval setting enable) bit (b8)

This bit enables or disables the DMA request interval setting that is defined in the IDRITVL bits.

Clearing this bit to 0 disables the DMA request interval setting that is defined in the IDRITVL bits.

Setting this bit to 1 enables the DMA request interval setting that is defined in the IDRITVL bits.

When the DMA request interval setting is disabled, a DMA request is issued immediately when the DMA request issuance conditions for the next DMA request are established after the response (Acknowledge) to the last DMA request is recognized.

(5) IDRITVL (DMA request enable setting) bits (b7 to b0)

These bits define the minimum number of cycles required from the time the response (Acknowledge) to the last DMA request is recognized till the time the issuance of the next DMA request is enabled.(1 to 256 cycles).

The issuance of the next DMA request is enabled before the data transfer for the last DMA request is completed. The setting made in these bits is enabled when the IITVLE bit is set to 1.

46.3.8 RAWBUF Interrupt Mask Register (RAWBUF_RBINTMSKR)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	INTMSK
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
0	INTMSK	B'0	R/W	Interrupt request mask 0: Interrupt requests are not masked. 1: Interrupt requests are masked.

(1) INTMSK (interrupt request mask) bit (b0)

This bit masks or de-masks interrupt requests generated by overflow conditions.

When this bit is cleared to 0, interrupt requests caused by overflow errors are enabled.

When this bit is cleared to 1, interrupt requests caused by overflow conditions are masked on.

Overflow errors are detected by the CMOSIF Link IF, DIRBUF, and RAWOBUF. An interrupt request signal is made available for each of the respective interrupt sources. These interrupt sources are masked or de-masked by this bit alone.

46.3.9 RAWBUF Status Register (RAWBUF_RBINTSTSR)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	ERRT	—	—	—	—	—	—	DT2FMT	DT1FMT
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	COVF	OOVF	DOVF
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
24	ERRT	B'0	R/W	Raw data format error test 0: Normal 1: Enables tests on the DT1FMT bit, DT2FMT bit, and the RAWBUF_RBFER1R and RAWBUF_RBFER1R registers.
23 to 18	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
17	DT2FMT	B'0	R/W	F1 path raw data format error 0: Indicates that no format error has occurred in the raw data. 1: Indicates that a format error has occurred in the raw data.
16	DT1FMT	B'0	R/W	Direct path raw data format error 0: Indicates that no format error has occurred in the raw data. 1: Indicates that a format error has occurred in the raw data.
15 to 3	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
2	COVF	B'0	R/W	CMOSIF Link I/F buffer overflow error 0: Indicates that no overflow error has occurred in the CMOSIF Link I/F buffer. The interrupt request associated with the overflow error by setting this bit to 0. 1: Indicates that an overflow error has occurred in the CMOSIF Link I/F buffer. An interrupt request can be generated by setting this bit to 1 (for testing).
1	OOVF	B'0	R/W	RAWOBUF overflow error 0: Indicates that no overflow error has occurred in the RAWOBUF. The interrupt request associated with the overflow error by setting this bit to 0. 1: Indicates that an overflow error has occurred in the RAWOBUF. An interrupt request can be generated by setting this bit to 1 (for testing).
0	DOVF	B'0	R/W	DIRBUF overflow error 0: Indicates that no overflow error has occurred in the DIRBUF. The interrupt request associated with the overflow error by setting this bit to 0. 1: Indicates that an overflow error has occurred in the DIRBUF. An interrupt request can be generated by setting this bit to 1 (for testing).

(1) ERRT (Raw data format error test) bit (b24)

This bit is used to enable the display for format tests made on the raw data.

Setting this bit to 0 disables the error tests. No error is then displayed when a 1 is written into the DT2FMT or DT1FMT bit. In addition, any value written into the RAWBUF_RBFER1R or RAWBUF_RBFER2R is not displayed.

Setting this bit to 1 enables the pseudo error tests. An error is signaled by writing a 1 into the DT2FMT or DT1FMT bit. Any value written into RBFER1R or RBFER2R is displayed as is (for testing).

(2) DT2FMT (F1 path raw data format error) bit (b17)

This bit indicates if an F1 path raw data format error has occurred.

0 in this bit indicates that no raw data format error has occurred.

1 in this bit indicates that a raw data format error has occurred.

Clearing this bit to 0 clears the error display.

A time equivalent to CAMCLK × 5 clocks + ICLK × 5 clocks is required until this bit is zero-cleared.

Another interval of CAMCLK × 8 clocks + ICLK × 8 clocks or longer is required to rewrite this bit.

An error display is generated when the ERRT bit (b7) is set to 1 and the DT2FMT bit (b14) to 1 (for testing).

(3) DT1FMT (Direct path raw data format error) bit (b16)

This bit indicates if a direct path raw data format error has occurred.

0 in this bit indicates that no raw data format error has occurred.

1 in this bit indicates that a raw data format error has occurred.

Clearing this bit to 0 clears the error display.

A time equivalent to CAMCLK × 5 clocks + ICLK × 5 clocks is required until this bit is zero-cleared.

Another interval of CAMCLK × 8 clocks + ICLK × 8 clocks or longer is required to rewrite this bit.

An error display is generated when the ERRT bit (b7) is set to 1 and the DT1FMT bit (b15) to 1 (for testing).

(4) COVF (CMOSIF Link I/F buffer overflow error) bit (b2)

This bit indicates if an overflow error has occurred in the CMOSIF Link I/F buffer.

A 0 in this bit indicates that no overflow has occurred in the CMOSIF Link I/F buffer.

A 1 in this bit indicates that an overflow has occurred in the CMOSIF Link I/F buffer, in which case an interrupt request is generated according to the state of the interrupt request mask bit.

Clearing this bit to 0 clears the interrupt request associated with the overflow.

A time equivalent to BCLK × 5 clocks + ICLK × 5 clocks is required until this bit is zero-cleared.

Another interval of BCLK × 6 clocks + ICLK × 6 clocks or longer is required to rewrite this bit.

An interrupt request can be generated according to the state of the interrupt request mask bit by setting this bit to 1 (for testing).

The interrupt request mask is set up by the INTMSK bit of the RAWBUF Interrupt Mask Register (RBINTMSKR).

(5) OOVF (RAWOBUF overflow error) bit (b1)

This bit indicates if an overflow error has occurred in the RAWOBUF.

A 0 in this bit indicates that no overflow has occurred in the RAWOBUF.

A 1 in this bit indicates that an overflow has occurred in the RAWOBUF, in which case an interrupt request is generated according to the state of the interrupt request mask bit.

Clearing this bit to 0 clears the interrupt request associated with the overflow.

An interrupt request can be generated according to the state of the interrupt request mask bit by setting this bit to 1 (for testing).

The interrupt request mask is set up by the INTMSK bit of the RAWBUF Interrupt Mask Register (RBINTMSKR).

(6) DOVF (DIRBUF overflow error) bit (b0)

This bit indicates if an overflow error has occurred in the DIRBUF.

A 0 in this bit indicates that no overflow has occurred in the DIRBUF.

A 1 in this bit indicates that a DIRBUF overflow has been caused by the data input initiated by asserting the CMOSIF_PE signal while the CMOSIF_VD and CMOSIF_HD signals are being asserted. In this case, an interrupt request is generated according to the state of the interrupt request mask bit.

Clearing this bit to 0 clears the interrupt request associated with the overflow.

A time equivalent to CAMCLK × 3 clocks + ICLK × 4 clocks is required until this bit is zero-cleared.

Another interval of CAMCLK × 4 clocks + ICLK × 2 clocks or longer is required to rewrite this bit.

An interrupt request can be generated according to the state of the interrupt request mask bit by setting this bit to 1 (for testing).

The interrupt request mask is set up by the INTMSK bit of the RAWBUF Operating Mode Register (RBFMDR).

46.3.10 RAWBUF Raw Format Error 1 Register (RAWBUF_RBFER1R)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	DERRV[28:16]												
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	DERRH[13:0]													
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
28 to 16	DERRV [28:16]	All 0	R/W	Direct path 8-bit DPCM/PCM data format error vertical position Indicate the line position within the frame in which a data format error occurred.
15 to 14	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
13 to 0	DERRH [13:0]	All 0	R/W	Direct path 8-bit DPCM/PCM data format error horizontal position Indicates the pixel position within the line in which a data format error occurred.

(1) DERRV (Direct path 8-bit DPCM/PCM data format error vertical position) bits (b28 to 16)

These bits indicate the position of the line within the frame in which a direct path raw data format error occurred.

These bits are normally read-only and cannot be modified but an arbitrary value can be written into these bits by setting the ERRT bit of the RAWBUF_RBINTSTSR register to 1 (for testing).

(2) DERRH (Direct path 8-bit DPCM/PCM data format error horizontal position) bits (b13 to b0)

These bits indicate the position of the pixel within the line in which a direct path raw data form error occurred.

These bits are normally read-only and cannot be modified but an arbitrary value can be written into these bits by setting the ERRT bit of the RAWBUF_RBINTSTSR register to 1 (for testing).

46.3.11 RAWBUF Raw Format Error 2 Register (RAWBUF_RBFER2R)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	FERRH[13:0]													
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
13 to 0	FERRH [13:0]	All 0	R/W	F1 path 8-bit DPCM/PCM data format error horizontal position Indicates the pixel position within the line in which a data format error occurred.

(1) DERRH (F1 path 8-bit DPCM/PCM data format error horizontal position) bits (b13 to b0)

These bits indicate the position of the pixel within the line in which an F1 path raw data form error occurred.

These bits are normally read-only and cannot be modified but an arbitrary value can be written into these bits by setting the ERRT bit of the RAWBUF_RBINTSTSR register to 1 (for testing).

46.3.12 RAWBUF H/V Status Register (RAWBUF_RBSESTSR)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	H	V	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
2	H	B'0	R	H bit 0: No H signal detected. 1: H signal detected.
1	V	B'0	R	V bit 0: No V signal detected. 1: V signal detected.
0	—	B'0	R	Reserved. This bit is always read as 0. The write value should always be 0.

(1) H (H) bit (b2)

This bit indicates the state of the horizontal sync signal.

A 0 in this bit indicates that the horizontal sync signal is negated.

A 1 in this bit indicates that the horizontal sync signal is asserted.

This is a read-only bit and cannot be modified.

(2) V (V) bit (b1)

This bit indicates the state of the vertical sync signal.

A 0 in this bit indicates that the vertical sync signal is negated.

A 1 in this bit indicates that the vertical sync signal is asserted.

This is a read-only bit and cannot be modified.

46.3.13 RAWBUF RAWOBUF Internal Status Register 1 (RAWBUF_RBOBFSTSR1)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	OFUL	OEMP	—	—	ODRQ	ODCPLT
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 22	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
21	OFUL	B'0	R	Full flag 0: Indicates that the RAWOBUF is not full. 1: Indicates that the RAWOBUF is full.
20	OEMP	B'0	R	Empty flag 0: Indicates that the RAWOBUF is not empty. 1: Indicates that the RAWOBUF is empty.
19 to 18	—	B'00	R	Reserved. These bits are always read as 0. The write value should always be 0.
17	ODRQ	B'0	R	DMA request display 0: Indicates that no DMA request has been issued from the RAWOBUF. 1: Indicates that a DMA request has been issued from the RAWOBUF. This bit is cleared by a response (Acknowledge) to the DMA request.
16	ODCPLT	B'0	R	DMA completion display 0: Indicates that the data transfer in response to a DMA request from the RAWOBUF has been completed. 1: Indicates that there is a response (Acknowledge) to a DMA request from the RAWOBUF but that the data transfer has not yet been completed.

Bit	Bit Name	Initial Value	R/W	Description
15 to 0	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.

(1) OFUL (full flag) bit (b21)

This bit indicates if the RAWOBUF is full.

A 0 in this bit indicates that the RAWOBUF is not full.

A 1 in this bit indicates that the RAWOBUF is full.

This is a read-only bit and cannot be modified.

(2) OEMP (empty flag) bit (b20)

This bit indicates if the RAWOBUF is empty.

A 0 in this bit indicates that the RAWOBUF is not empty.

A 1 in this bit indicates that the RAWOBUF is empty.

This is a read-only bit and cannot be modified.

(3) ODRQ (DMA request display) bit (b17)

This bit indicates if there is a DMA request from the RAWOBUF.

A 0 in this bit indicates that no DMA request has been issued from the RAWOBUF.

A 1 in this bit indicates that a DMA request has been issued from the RAWOBUF. In this case, the bit is cleared by a response (Acknowledge) to the DMA request.

This is a read-only bit and cannot be modified.

(4) ODCPLT (DMA completion display) bit (b16)

This bit indicates whether the data transfer initiated in response to a DMA request from the RAWOBUF has been completed.

A 0 in this bit indicates that the data transfer initiated by a DMA request from the RAWOBUF has been completed.

A 1 in this bit indicates that there is a response (Acknowledge) to a DMA request from the RAWOBUF but that the data transfer has not yet been completed. In this case, the bit is cleared when the transfer of 1 operand is completed.

This bit is set to 1 upon recognition of a response (Acknowledge) to a DMA request from the RAWOBUF and set to 0 when the transfer of one operand data are completed.

This is a read-only bit and cannot be modified.

46.3.14 RAWBUF RAWOBUF Internal Status Register 2 (RAWBUF_RBOBFSTSR2)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	OWPTR[25:16]									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	ORPTR[9:0]									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
25 to 16	OWPTR [25:16]	All 0	R	Write pointer Indicate the value of the write pointer for the RAWOBUF.
15 to 10	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
9 to 0	ORPTR [9:0]	All 0	R	Read pointer Indicate the value of the read pointer for the RAWOBUF.

(1) OWPTR (write pointer) bits (b25 to b16)

These bits represent the write pointer for the RAWOBUF.

The write pointer holds a 64-bit pointer value.

This is a read-only bit and cannot be modified.

(2) ORPTR (read pointer) bits (b9 to b0)

These bits represent the read pointer for the RAWOBUF.

The read pointer holds a 64-bit pointer value.

This is a read-only bit and cannot be modified.

46.3.15 RAWBUF RAWIBUF Internal Status Register 1 (RAWBUF_RBIBFSTSR1)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	IFUL	EEMP	—	—	IDRQ	IDCPLT
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 22	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
21	IFUL	B'0	R	Full flag 0: Indicates that the RAWIBUF is not full. 1: Indicates that the RAWIBUF is full.
20	IEMP	B'0	R	Empty flag 0: Indicates that the RAWIBUF is not full. 1: Indicates that the RAWIBUF is full.
19 to 18	—	B'00	R	Reserved. These bits are always read as 0. The write value should always be 0.
17	IDRQ	B'0	R	DMA request display 0: Indicates that no DMA request has been issued from the RAWIBUF. 1: Indicates that a DMA request has been issued from the RAWIBUF. This bit is cleared by a response (Acknowledge) to the DMA request.
16	IDCPLT	B'0	R	DMA completion display 0: Indicates that the data transfer in response to a DMA request from the RAWIBUF has been completed. 1: Indicates that there is a response (Acknowledge) to a DMA request from the RAWIBUF but that the data transfer has not yet been completed.

Bit	Bit Name	Initial Value	R/W	Description
15 to 0	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.

(1) IFUL (full flag) bit (b21)

This bit indicates if the RAWIBUF is full.

A 0 in this bit indicates that the RAWIBUF is not full.

A 1 in this bit indicates that the RAWIBUF is full.

This is a read-only bit and cannot be modified.

(2) IEMP (empty flag) bit (b20)

This bit indicates if the RAWIBUF is empty.

A 0 in this bit indicates that the RAWIBUF is not empty.

A 1 in this bit indicates that the RAWIBUF is empty.

This is a read-only bit and cannot be modified.

(3) IDRQ (DMA request display) bit (b17)

This bit indicates if there is a DMA request from the RAWIBUF.

A 0 in this bit indicates that no DMA request has been issued from the RAWIBUF.

A 1 in this bit indicates that a DMA request has been issued from the RAWIBUF. In this case, the bit is cleared by a response (Acknowledge) to the DMA request.

This is a read-only bit and cannot be modified.

(4) IDCPLT (DMA completion display) bit (b16)

This bit indicates whether the data transfer initiated in response to a DMA request from the RAWIBUF has been completed.

A 0 in this bit indicates that the data transfer initiated by a DMA request from the RAWIBUF has been completed.

A 1 in this bit indicates that there is a response (Acknowledge) to a DMA request from the RAWIBUF but that the data transfer has not yet been completed. In this case, the bit is cleared when the transfer of 1 operand is completed.

This bit is set to 1 upon recognition of a response (Acknowledge) to a DMA request from the RAWIBUF and set to 0 when the transfer of one operand data are completed.

This is a read-only bit and cannot be modified.

46.3.16 RAWBUF RAWIBUF Internal Status Register 2 (RAWBUF_RBIBFSTSR2)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	IWPTR[25:16]									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	IRPTR[9:0]									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
25 to 16	IWPTR [25:16]	All 0	R	Write pointer Indicate the value of the write pointer for the RAWIBUF.
15 to 10	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
9 to 0	IRPTR[9:0]	All 0	R	Read pointer Indicate the value of the read pointer for the RAWIBUF.

(1) IWPTR (write pointer) bits (b25 to b16)

These bits represent the write pointer for the RAWIBUF.

The write pointer holds a 64-bit pointer value.

This is a read-only bit and cannot be modified.

(2) IRPTR (read pointer) bits (b9 to b0)

These bits represent the read pointer for the RAWIBUF.

The read pointer holds a 64-bit pointer value.

This is a read-only bit and cannot be modified.

If the read pointer is read while the RAWIBUF is running when the frequency of CAMCLK is higher than that of ICLK, the lower bits will not reflect the correct value according to the ratio of the respective frequencies.

46.3.17 RAWBUF Buffer Access Mode Register (RAWBUF_RBACCMDR)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BUFACC
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
0	BUFACC	B'0	R/W	Buffer access bus select 0: RAWIBUF and RAWOBUF are accessed over the F1 bus. 1: RAWIBUF and RAWOBUF are accessed over the C bus.

(1) BUFACC (buffer access bus select) bits (b0)

This bit defines the bus over which the RAWIBUF and RAWOBUF are to be accessed.

Clearing this bit to 0 sets the active access bus to the F1 bus.

Setting this bit to 1 sets the active access bus to the C bus.

When the C bus is selected as the active access bus, no raw data can be placed on the F1 bus.

Even when the C bus is selected as the active access bus, no data can be written into the RAWIBUF or RAWOBUF over the C bus. Data can only be read over the C bus.

To access the RAWIBUF and RAWOBUF over the C bus, allocate the RAWIBUF and RAWOBUF to the following memory areas:

RAWIBUF	:H'FE8F 2000	to	H'FE8F 3FFC
RAWOBUF	:H'FE8F 4000	to	H'FE8F 5FFC

When RAWIBUF and RAWOBUF are to be accessed over the C bus, they must be accessed only on a word (32 bits) basis.

Figures 46.15 and 46.16 show the mapping method for the RAWIBUF and RAWOBUF, respectively.

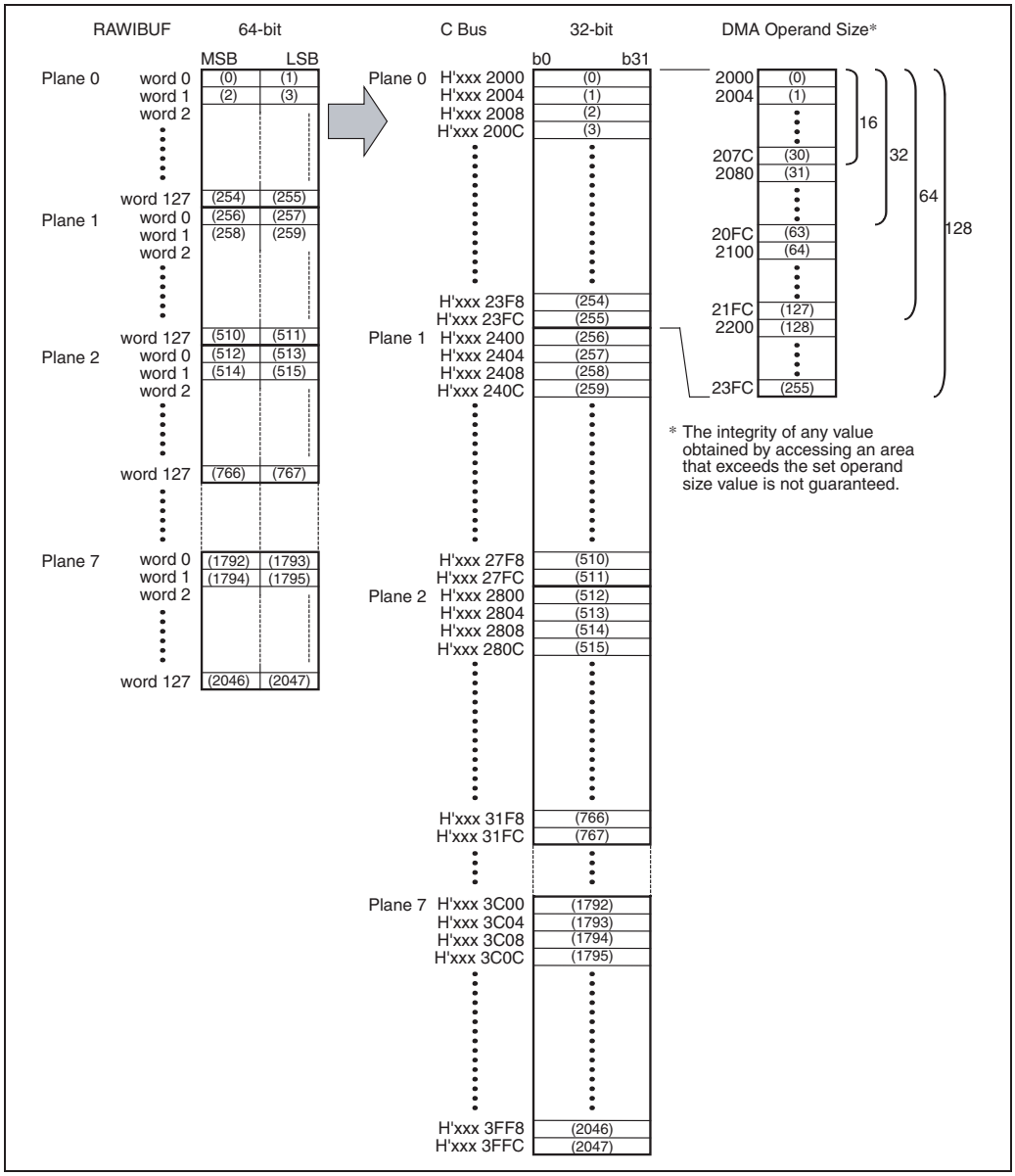


Figure 46.15 RAWIBUF Mapping Method

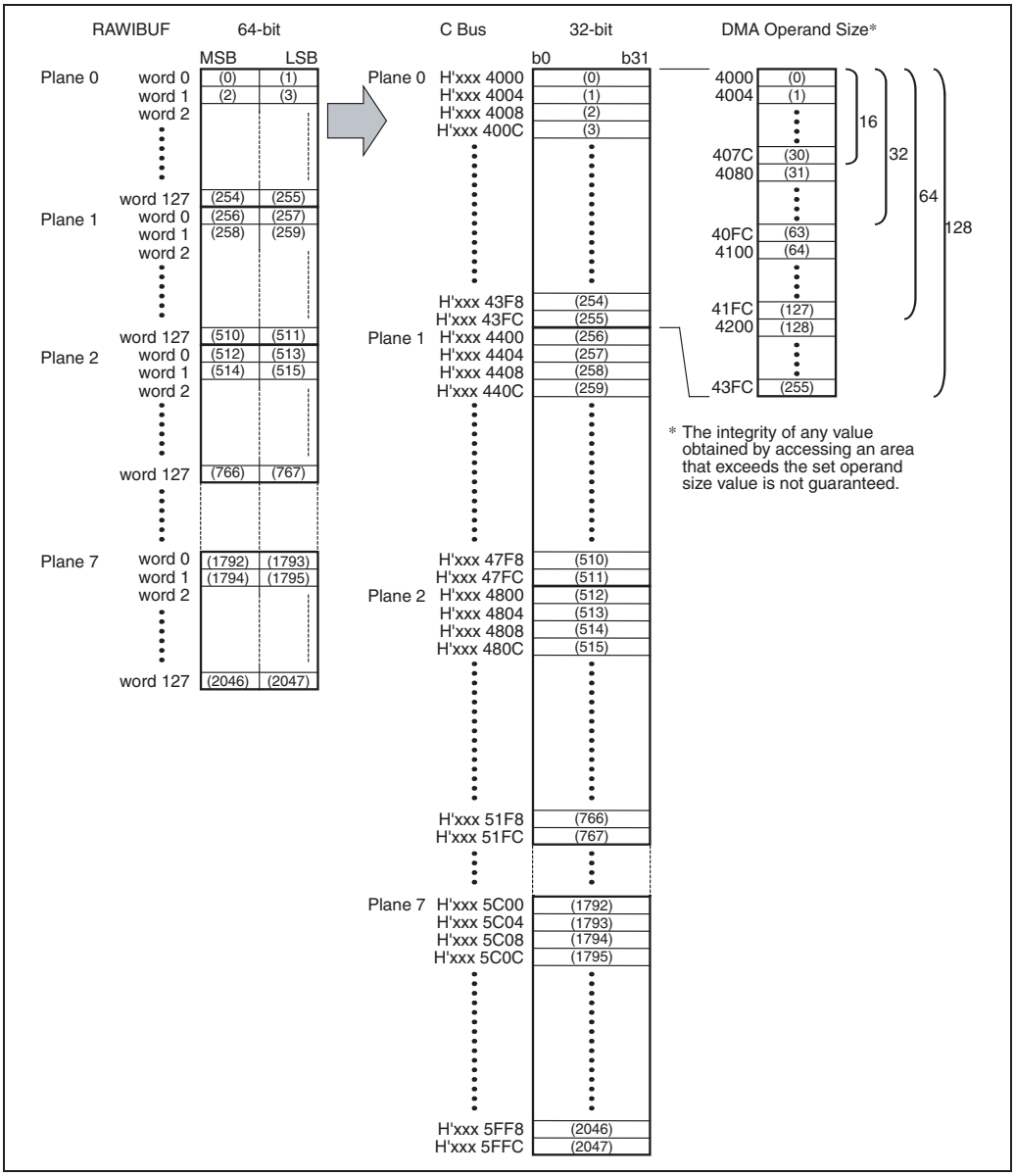


Figure 46.16 RAWOBUF Mapping Method

46.4 F1DMAC

46.4.1 F1DMAC Feature Overview

The DMA controller (F1DMAC) for exclusive use by the ISP is a module that transfers data at high speed bypassing the CPU, as requested by the software or on-chip peripheral I/O device. The ISP contains two of these modules. One is the F1DMAC(0) used mainly for data transfer from the CMAIF or RAWBUF. The other is the F1DMAC(1) responsible for data transfer from the ISP. Table 46.10 shows the F1DMAC features.

Table 46.10 F1DMAC Features

Item	Feature
Number of channels	8
Transfer request	Request from the software trigger or on-chip peripheral I/O device. (There are five factors for the F1DMAC(0) and seven factors for the F1DMAC(1).)
Maximum number of transfer bytes	64 Mbytes
Address space	4 Gbytes
Transfer data size	1-unit transfer: 8, 16, 32, 64 or 128 bits* 1-operand transfer: 1, 2, 4, 8, 16, 32, 64 or 128 data units Non-stop transfer: Performed until the byte count reaches 0.
Transfer mode	Cycle stealing mode (dual-address transfer) Pipeline mode (dual-address transfer) Fly-by mode (single-address transfer)
Maximum transfer rate	Cycle stealing mode: Three or more clock cycles per 1-unit transfer Pipeline mode: One or more clock cycles per 1-unit transfer Fly-by mode: One clock cycle per 1-unit transfer

Item	Feature
Transfer conditions	Single-operand transfer: Several DMA requests are generated, each causing one operand to be transferred. Channel arbitration takes place each time one operand is transferred. Request triggering is required each time one operand is transferred.
	Consecutive-operand transfer: When one DMA request is generated, it causes operands to be transferred one after another until the byte count reaches 0. Channel arbitration takes places each time one operand is transferred. Request triggering is only required at the start of the first transfer.
	Non-stop transfer: Transfer starts upon a DMA request and continues without cessation until the byte count reaches 0. Channel arbitration does not take place during non-stop transfer. Request triggering is only required at the start of this transfer.
Channel priority	Channel 0 > Channel > … > Channel 6 > Channel 7 (fixed priority)
Interrupt requests	When the byte count reaches 0, the following interrupt requests are generated:
	Interrupt request signal for each channel
	Common interrupt request signal shared by the channels
Others	Reload function (for each source address, destination address or byte count)
	Rotate function
	2D addressing
	DMAC suspend/resume/abort function

Note: * Factory fixed at 64 bits for this product.

Notes: The terms used in this document are defined below.

- 1-unit transfer: Transfer driven by the DMAC. This transfer involves one read and one write cycle in dual-address mode. It involves one read or one write cycle in single-address mode.
- 1-operand transfer: Consecutive data transfers executed by the DMAC using one channel. (The data transfer count depends on register settings.)
- 1-DMA transfer: Transfer of a number of bytes specified in the byte count register. They are located between the start address and end address.
- Channel number: n = 0, 1, …, 6, 7
- Request factor number: k = 1, 2, …, 8, m = 0, 1, 2, …, 8

46.4.2 Register Description

(1) Register read/write restrictions

Restrictions on register reads and writes are given below. The system operation may fail if the integrity of the following register operations is not guaranteed:

1. Writing a 1 into any read-only register bit or reserved area is prohibited. Do not set any value other than the specified values.
2. There are cases in which a nonzero value is read from a read-only bit. Such a value must not be rewritten.
3. Writing into any registers (bits) that are disallowed for writes during operation is prohibited while some operation is in progress (reads are allowed). The operating state of the F1DMAC can be identified by reading the F1DMAC operation register or by identifying the end of the F1DMAC transfer.
4. All of the F1DMAC registers must be allocated to non-cache area.

(2) Terms and abbreviations used in this document

A term that is used in this document is explained below.

1. "Software reset" refers to a forced reset into the F1DMAC internal circuit. This means that any attempt to effect a module reset while the F1DMAC is running normally might place the F1DMAC peripheral hardware into an inoperative state.

(3) List of F1DMAC(0/1) Registers

The register configuration of the F1DMAC(0) registers is summarized in table 46.11 and that of the F1DMAC(1) registers is summarized in table 46.12. The relationship between the processing modes and register states is given in table 46.13.

Table 46.11 F1DMAC(0) Register Configurations

Register Name	Abbreviation	R/W	Address	Access Size
F1DMAC0 DMA current source address register 0	F1DMAC0_DMCSADR0	R/W	H'FE8F 8000	32
F1DMAC0 DMA current destination address register 0	F1DMAC0_DMCDADR0	R/W	H'FE8F 8004	32
F1DMAC0 DMA current byte count register 0	F1DMAC0_DMCBCT0	R/W	H'FE8F 8008	32
F1DMAC0 DMA mode register 0	F1DMAC0_DMMOD0	R/W	H'FE8F 800C	32
F1DMAC0 DMA current source address register 1	F1DMAC0_DMCSADR1	R/W	H'FE8F 8010	32
F1DMAC0 DMA current destination address register 1	F1DMAC0_DMCDADR1	R/W	H'FE8F 8014	32
F1DMAC0 DMA current byte count register 1	F1DMAC0_DMCBCT1	R/W	H'FE8F 8018	32
F1DMAC0 DMA mode register 1	F1DMAC0_DMMOD1	R/W	H'FE8F 801C	32
F1DMAC0 DMA current source address register 2	F1DMAC0_DMCSADR2	R/W	H'FE8F 8020	32
F1DMAC0 DMA current destination address register 2	F1DMAC0_DMCDADR2	R/W	H'FE8F 8024	32
F1DMAC0 DMA current byte count register 2	F1DMAC0_DMCBCT2	R/W	H'FE8F 8028	32
F1DMAC0 DMA mode register 2	F1DMAC0_DMMOD2	R/W	H'FE8F 802C	32
F1DMAC0 DMA current source address register 3	F1DMAC0_DMCSADR3	R/W	H'FE8F 8030	32
F1DMAC0 DMA current destination address register 3	F1DMAC0_DMCDADR3	R/W	H'FE8F 8034	32
F1DMAC0 DMA current byte count register 3	F1DMAC0_DMCBCT3	R/W	H'FE8F 8038	32
F1DMAC0 DMA mode register 3	F1DMAC0_DMMOD3	R/W	H'FE8F 803C	32
F1DMAC0 DMA current source address register 4	F1DMAC0_DMCSADR4	R/W	H'FE8F 8040	32
F1DMAC0 DMA current destination address register 4	F1DMAC0_DMCDADR4	R/W	H'FE8F 8044	32
F1DMAC0 DMA current byte count register 4	F1DMAC0_DMCBCT4	R/W	H'FE8F 8048	32
F1DMAC0 DMA mode register 4	F1DMAC0_DMMOD4	R/W	H'FE8F 804C	32
F1DMAC0 DMA current source address register 5	F1DMAC0_DMCSADR5	R/W	H'FE8F 8050	32
F1DMAC0 DMA current destination address register 5	F1DMAC0_DMCDADR5	R/W	H'FE8F 8054	32
F1DMAC0 DMA current byte count register 5	F1DMAC0_DMCBCT5	R/W	H'FE8F 8058	32
F1DMAC0 DMA mode register 5	F1DMAC0_DMMOD5	R/W	H'FE8F 805C	32
F1DMAC0 DMA current source address register 6	F1DMAC0_DMCSADR6	R/W	H'FE8F 8060	32
F1DMAC0 DMA current destination address register 6	F1DMAC0_DMCDADR6	R/W	H'FE8F 8064	32
F1DMAC0 DMA current byte count register 6	F1DMAC0_DMCBCT6	R/W	H'FE8F 8068	32
F1DMAC0 DMA mode register 6	F1DMAC0_DMMOD6	R/W	H'FE8F 806C	32
F1DMAC0 DMA current source address register 7	F1DMAC0_DMCSADR7	R/W	H'FE8F 8070	32
F1DMAC0 DMA current destination address register 7	F1DMAC0_DMCDADR7	R/W	H'FE8F 8074	32

Register Name	Abbreviation	R/W	Address	Access Size
F1DMAC0 DMA current byte count register 7	F1DMAC0_DMCBCT7	R/W	H'FE8F 8078	32
F1DMAC0 DMA mode register 7	F1DMAC0_DMMOD7	R/W	H'FE8F 807C	32
F1DMAC0 area prohibited from use	—	—	H'FE8F 8080 to H'FE8F 81FC	—
F1DMAC0 DMA reload source address register 0	F1DMAC0_DMRSADR0	R/W	H'FE8F 8200	32
F1DMAC0 DMA reload destination address register 0	F1DMAC0_DMRDADR0	R/W	H'FE8F 8204	32
F1DMAC0 DMA reload byte counter register 0	F1DMAC0_DMRBCT0	R/W	H'FE8F 8208	32
F1DMAC0 area prohibited from use	—	—	H'FE8F 820C	—
F1DMAC0 DMA reload source address register 1	F1DMAC0_DMRSADR1	R/W	H'FE8F 8210	32
F1DMAC0 DMA reload destination address register 1	F1DMAC0_DMRDADR1	R/W	H'FE8F 8214	32
F1DMAC0 DMA reload byte counter register 1	F1DMAC0_DMRBCT1	R/W	H'FE8F 8218	32
F1DMAC0 area prohibited from use	—	—	H'FE8F 821C	—
F1DMAC0 DMA reload source address register 2	F1DMAC0_DMRSADR2	R/W	H'FE8F 8220	32
F1DMAC0 DMA reload destination address register 2	F1DMAC0_DMRDADR2	R/W	H'FE8F 8224	32
F1DMAC0 DMA reload byte counter register 2	F1DMAC0_DMRBCT2	R/W	H'FE8F 8228	32
F1DMAC0 area prohibited from use	—	—	H'FE8F 822C	—
F1DMAC0 DMA reload source address register 3	F1DMAC0_DMRSADR3	R/W	H'FE8F 8230	32
F1DMAC0 DMA reload destination address register 3	F1DMAC0_DMRDADR3	R/W	H'FE8F 8234	32
F1DMAC0 DMA reload byte counter register 3	F1DMAC0_DMRBCT3	R/W	H'FE8F 8238	32
F1DMAC0 area prohibited from use	—	—	H'FE8F 823C	—
F1DMAC0 DMA reload source address register 4	F1DMAC0_DMRSADR4	R/W	H'FE8F 8240	32
F1DMAC0 DMA reload destination address register 4	F1DMAC0_DMRDADR4	R/W	H'FE8F 8244	32
F1DMAC0 DMA reload byte counter register 4	F1DMAC0_DMRBCT4	R/W	H'FE8F 8248	32
F1DMAC0 area prohibited from use	—	—	H'FE8F 824C	—
F1DMAC0 DMA reload source address register 5	F1DMAC0_DMRSADR5	R/W	H'FE8F 8250	32
F1DMAC0 DMA reload destination address register 5	F1DMAC0_DMRDADR5	R/W	H'FE8F 8254	32
F1DMAC0 DMA reload byte counter register 5	F1DMAC0_DMRBCT5	R/W	H'FE8F 8258	32
F1DMAC0 area prohibited from use	—	—	H'FE8F 825C	—
F1DMAC0 DMA reload source address register 6	F1DMAC0_DMRSADR6	R/W	H'FE8F 8260	32
F1DMAC0 DMA reload destination address register 6	F1DMAC0_DMRDADR6	R/W	H'FE8F 8264	32
F1DMAC0 DMA reload byte counter register 6	F1DMAC0_DMRBCT6	R/W	H'FE8F 8268	32
F1DMAC0 area prohibited from use	—	—	H'FE8F 826C	—

Register Name	Abbreviation	R/W	Address	Access Size
F1DMAC0 DMA reload source address register 7	F1DMAC0_DMRSADR7	R/W	H'FE8F 8270	32
F1DMAC0 DMA reload destination address register 7	F1DMAC0_DMRDADR7	R/W	H'FE8F 8274	32
F1DMAC0 DMA reload byte counter register 7	F1DMAC0_DMRBCT7	R/W	H'FE8F 8278	32
F1DMAC0 area prohibited from use	—	—	H'FE8F 827C to H'FE8F 83FC	—
F1DMAC0 DMA control register A0	F1DMAC0_DMCNTA0	R/W	H'FE8F 8400	32
F1DMAC0 DMA control register B0	F1DMAC0_DMCNTB0	R/W	H'FE8F 8404	32
F1DMAC0 DMA control register A1	F1DMAC0_DMCNTA1	R/W	H'FE8F 8408	32
F1DMAC0 DMA control register B1	F1DMAC0_DMCNTB1	R/W	H'FE8F 840C	32
F1DMAC0 DMA control register A2	F1DMAC0_DMCNTA2	R/W	H'FE8F 8410	32
F1DMAC0 DMA control register B2	F1DMAC0_DMCNTB2	R/W	H'FE8F 8414	32
F1DMAC0 DMA control register A3	F1DMAC0_DMCNTA3	R/W	H'FE8F 8418	32
F1DMAC0 DMA control register B3	F1DMAC0_DMCNTB3	R/W	H'FE8F 841C	32
F1DMAC0 DMA control register A4	F1DMAC0_DMCNTA4	R/W	H'FE8F 8420	32
F1DMAC0 DMA control register B4	F1DMAC0_DMCNTB4	R/W	H'FE8F 8424	32
F1DMAC0 DMA control register A5	F1DMAC0_DMCNTA5	R/W	H'FE8F 8428	32
F1DMAC0 DMA control register B5	F1DMAC0_DMCNTB5	R/W	H'FE8F 842C	32
F1DMAC0 DMA control register A6	F1DMAC0_DMCNTA6	R/W	H'FE8F 8430	32
F1DMAC0 DMA control register B6	F1DMAC0_DMCNTB6	R/W	H'FE8F 8434	32
F1DMAC0 DMA control register A7	F1DMAC0_DMCNTA7	R/W	H'FE8F 8438	32
F1DMAC0 DMA control register B7	F1DMAC0_DMCNTB7	R/W	H'FE8F 843C	32
F1DMAC0 area prohibited from use	—		H'FE8F 8440 to H'FE8F 84FC	—
F1DMAC0 DMA start control register	F1DMAC0_DMSCNT	R/W	H'FE8F 8500	32
F1DMAC0 area prohibited from use	—		H'FE8F 8504	—
F1DMAC0 DMA interrupt control register	F1DMAC0_DMICNT	R/W	H'FE8F 8508	32
F1DMAC0 DMA common-interrupt control register	F1DMAC0_DMICNTA	R/W	H'FE8F 850C	32
F1DMAC0 DMA interrupt status register	F1DMAC0_DMISTS	R	H'FE8F 8510	32
F1DMAC0 DMA transfer end detect register	F1DMAC0_DMEDET	R/W	H'FE8F 8514	32
F1DMAC0 DMA arbitration status register	F1DMAC0_DMASTS	R/W	H'FE8F 8518	32
F1DMAC0 area prohibited from use	—	—	H'FE8F 851C to H'FE8F 85FC	—
F1DMAC0 DMA 2D column setup register 0	F1DMAC0_DM2DCLM0	R/W	H'FE8F 8600	32

Register Name	Abbreviation	R/W	Address	Access Size
F1DMAC0 DMA 2D row setup register 0	F1DMAC0_DM2DROW0	R/W	H'FE8F 8604	32
F1DMAC0 DMA 2D block setup register 0	F1DMAC0_DM2DBLK0	R/W	H'FE8F 8608	32
F1DMAC0 DMA 2D next-row offset register 0	F1DMAC0_DM2DNROST0	R/W	H'FE8F 860C	32
F1DMAC0 DMA 2D next-block offset register 0	F1DMAC0_DM2DNBOST0	R/W	H'FE8F 8610	32
F1DMAC0 DMA 2D next-line offset register 0	F1DMAC0_DM2DNLOST0	R/W	H'FE8F 8614	32
F1DMAC0 area prohibited from use	—	—	H'FE8F 8618 to H'FE8F 861C	—
F1DMAC0 DMA 2D column setup register 1	F1DMAC0_DM2DCLM1	R/W	H'FE8F 8620	32
F1DMAC0 DMA 2D row setup register 1	F1DMAC0_DM2DROW1	R/W	H'FE8F 8624	32
F1DMAC0 DMA 2D block setup register 1	F1DMAC0_DM2DBLK1	R/W	H'FE8F 8628	32
F1DMAC0 DMA 2D next-row offset register 1	F1DMAC0_DM2DNROST1	R/W	H'FE8F 862C	32
F1DMAC0 DMA 2D next-block offset register 1	F1DMAC0_DM2DNBOST1	R/W	H'FE8F 8630	32
F1DMAC0 DMA 2D next-line offset register 1	F1DMAC0_DM2DNLOST1	R/W	H'FE8F 8634	32
F1DMAC0 area prohibited from use	—	—	H'FE8F 8638 to H'FE8F 863C	—
F1DMAC0 DMA 2D column setup register 2	F1DMAC0_DM2DCLM2	R/W	H'FE8F 8640	32
F1DMAC0 DMA 2D row setup register 2	F1DMAC0_DM2DROW2	R/W	H'FE8F 8644	32
F1DMAC0 DMA 2D block setup register 2	F1DMAC0_DM2DBLK2	R/W	H'FE8F 8648	32
F1DMAC0 DMA 2D next-row offset register 2	F1DMAC0_DM2DNROST2	R/W	H'FE8F 864C	32
F1DMAC0 DMA 2D next-block offset register 2	F1DMAC0_DM2DNBOST2	R/W	H'FE8F 8650	32
F1DMAC0 DMA 2D next-line offset register 2	F1DMAC0_DM2DNLOST2	R/W	H'FE8F 8654	32
F1DMAC0 area prohibited from use	—	—	H'FE8F 8658 to H'FE8F 865C	—
F1DMAC0 DMA 2D column setup register 3	F1DMAC0_DM2DCLM3	R/W	H'FE8F 8660	32
F1DMAC0 DMA 2D row setup register 3	F1DMAC0_DM2DROW3	R/W	H'FE8F 8664	32
F1DMAC0 DMA 2D block setup register 3	F1DMAC0_DM2DBLK3	R/W	H'FE8F 8668	32
F1DMAC0 DMA 2D next-row offset register 3	F1DMAC0_DM2DNROST3	R/W	H'FE8F 866C	32
F1DMAC0 DMA 2D next-block offset register 3	F1DMAC0_DM2DNBOST3	R/W	H'FE8F 8670	32
F1DMAC0 DMA 2D next-line offset register 3	F1DMAC0_DM2DNLOST3	R/W	H'FE8F 8674	32
F1DMAC0 area prohibited from use	—	—	H'FE8F 8678 to H'FE8F 867C	—
F1DMAC0 DMA 2D column setup register 4	F1DMAC0_DM2DCLM4	R/W	H'FE8F 8680	32
F1DMAC0 DMA 2D row setup register 4	F1DMAC0_DM2DROW4	R/W	H'FE8F 8684	32

Register Name	Abbreviation	R/W	Address	Access Size
F1DMAC0 DMA 2D block setup register 4	F1DMAC0_DM2DBLK4	R/W	H'FE8F 8688	32
F1DMAC0 DMA 2D next-row offset register 4	F1DMAC0_DM2DNROST4	R/W	H'FE8F 868C	32
F1DMAC0 DMA 2D next-block offset register 4	F1DMAC0_DM2DNBOST4	R/W	H'FE8F 8690	32
F1DMAC0 DMA 2D next-line offset register 4	F1DMAC0_DM2DNLOST4	R/W	H'FE8F 8694	32
F1DMAC0 area prohibited from use	—	—	H'FE8F 8698 to H'FE8F 869C	—
F1DMAC0 DMA 2D column setup register 5	F1DMAC0_DM2DCLM5	R/W	H'FE8F 86A0	32
F1DMAC0 DMA 2D row setup register 5	F1DMAC0_DM2DROW5	R/W	H'FE8F 86A4	32
F1DMAC0 DMA 2D block setup register 5	F1DMAC0_DM2DBLK5	R/W	H'FE8F 86A8	32
F1DMAC0 DMA 2D next-row offset register 5	F1DMAC0_DM2DNROST5	R/W	H'FE8F 86AC	32
F1DMAC0 DMA 2D next-block offset register 5	F1DMAC0_DM2DNBOST5	R/W	H'FE8F 86B0	32
F1DMAC0 DMA 2D next-line offset register 5	F1DMAC0_DM2DNLOST5	R/W	H'FE8F 86B4	32
F1DMAC0 area prohibited from use	—	—	H'FE8F 86B8 to H'FE8F 86BC	—
F1DMAC0 DMA 2D column setup register 6	F1DMAC0_DM2DCLM6	R/W	H'FE8F 86C0	32
F1DMAC0 DMA 2D row setup register 6	F1DMAC0_DM2DROW6	R/W	H'FE8F 86C4	32
F1DMAC0 DMA 2D block setup register 6	F1DMAC0_DM2DBLK6	R/W	H'FE8F 86C8	32
F1DMAC0 DMA 2D next-row offset register 6	F1DMAC0_DM2DNROST6	R/W	H'FE8F 86CC	32
F1DMAC0 DMA 2D next-block offset register 6	F1DMAC0_DM2DNBOST6	R/W	H'FE8F 86D0	32
F1DMAC0 DMA 2D next-line offset register 6	F1DMAC0_DM2DNLOST6	R/W	H'FE8F 86D4	32
F1DMAC0 area prohibited from use	—	—	H'FE8F 86D8 to H'FE8F 86DC	—
F1DMAC0 DMA 2D column setup register 7	F1DMAC0_DM2DCLM7	R/W	H'FE8F 86E0	32
F1DMAC0 DMA 2D row setup register 7	F1DMAC0_DM2DROW7	R/W	H'FE8F 86E4	32
F1DMAC0 DMA 2D block setup register 7	F1DMAC0_DM2DBLK7	R/W	H'FE8F 86E8	32
F1DMAC0 DMA 2D next-row offset register 7	F1DMAC0_DM2DNROST7	R/W	H'FE8F 86EC	32
F1DMAC0 DMA 2D next-block offset register 7	F1DMAC0_DM2DNBOST7	R/W	H'FE8F 86F0	32
F1DMAC0 DMA 2D next-line offset register 7	F1DMAC0_DM2DNLOST7	R/W	H'FE8F 86F4	32
F1DMAC0 area prohibited from use	—	—	H'FE8F 86F8 to H'FE8F 89FC	—
F1DMAC0 DMA reload 2D column setup register 0	F1DMAC0_DMR2DCLM0	R/W	H'FE8F 8A00	32
F1DMAC0 DMA reload 2D row setup register 0	F1DMAC0_DMR2DROW0	R/W	H'FE8F 8A04	32
F1DMAC0 DMA reload 2D block setup register 0	F1DMAC0_DMR2DBLK0	R/W	H'FE8F 8A08	32

Register Name	Abbreviation	R/W	Address	Access Size
F1DMAC0 DMA reload 2D next-row offset register 0	F1DMAC0_DMR2DNROST0	R/W	H'FE8F 8A0C	32
F1DMAC0 DMA reload 2D next-block offset register 0	F1DMAC0_DMR2DNBOST0	R/W	H'FE8F 8A10	32
F1DMAC0 DMA reload 2D next-line offset register 0	F1DMAC0_DMR2DNLOST0	R/W	H'FE8F 8A14	32
F1DMAC0 area prohibited from use	—	—	H'FE8F 8A18 to H'FE8F 8A1C	—
F1DMAC0	F1DMAC0_	R/W	H'FE8F 8A1C	32
F1DMAC0 DMA reload 2D column setup register 1	F1DMAC0_DMR2DCLM1	R/W	H'FE8F 8A20	32
F1DMAC0 DMA reload 2D row setup register 1	F1DMAC0_DMR2DROW1	R/W	H'FE8F 8A24	32
F1DMAC0 DMA reload 2D block setup register 1	F1DMAC0_DMR2DBLK1	R/W	H'FE8F 8A28	32
F1DMAC0 DMA reload 2D next-row offset register 1	F1DMAC0_DMR2DNROST1	R/W	H'FE8F 8A2C	32
F1DMAC0 DMA reload 2D next-block offset register 1	F1DMAC0_DMR2DNBOST1	R/W	H'FE8F 8A30	32
F1DMAC0 DMA reload 2D next-line offset register 1	F1DMAC0_DMR2DNLOST1	—	H'FE8F 8A34	32
F1DMAC0 area prohibited from use	—		H'FE8F 8A38 to H'FE8F 8A3C	—
F1DMAC0	F1DMAC0_	R/W	H'FE8F 8A3C	32
F1DMAC0 DMA reload 2D column setup register 2	F1DMAC0_DMR2DCLM2	R/W	H'FE8F 8A40	32
F1DMAC0 DMA reload 2D row setup register 2	F1DMAC0_DMR2DROW2	R/W	H'FE8F 8A44	32
F1DMAC0 DMA reload 2D block setup register 2	F1DMAC0_DMR2DBLK2	R/W	H'FE8F 8A48	32
F1DMAC0 DMA reload 2D next-row offset register 2	F1DMAC0_DMR2DNROST2	R/W	H'FE8F 8A4C	32
F1DMAC0 DMA reload 2D next-block offset register 2	F1DMAC0_DMR2DNBOST2	R/W	H'FE8F 8A50	32
F1DMAC0 DMA reload 2D next-line offset register 2	F1DMAC0_DMR2DNLOST2	R/W	H'FE8F 8A54	32
F1DMAC0 area prohibited from use	—	—	H'FE8F 8A58 to H'FE8F 8A5C	—
1DMAC0 DMA reload 2D column setup register 3	F1DMAC0_DMR2DCLM3	R/W	H'FE8F 8A60	32
F1DMAC0 DMA reload 2D row setup register 3	F1DMAC0_DMR2DROW3	R/W	H'FE8F 8A64	32
F1DMAC0 DMA reload 2D block setup register 3	F1DMAC0_DMR2DBLK3	R/W	H'FE8F 8A68	32
F1DMAC0 DMA reload 2D next-row offset register 3	F1DMAC0_DMR2DNROST3	R/W	H'FE8F 8A6C	32
F1DMAC0 DMA reload 2D next-block offset register 3	F1DMAC0_DMR2DNBOST3	R/W	H'FE8F 8A70	32
F1DMAC0 DMA reload 2D next-line offset register 3	F1DMAC0_DMR2DNLOST3	R/W	H'FE8F 8A74	32
F1DMAC0 area prohibited from use	—	—	H'FE8F 8A78 to H'FE8F 8A7C	—
F1DMAC0 DMA reload 2D column setup register 4	F1DMAC0_DMR2DCLM4	R/W	H'FE8F 8A80	32
F1DMAC0 DMA reload 2D row setup register 4	F1DMAC0_DMR2DROW4	R/W	H'FE8F 8A84	32

Register Name	Abbreviation	R/W	Address	Access Size
F1DMAC0 DMA reload 2D block setup register 4	F1DMAC0_DMR2DBLK4	R/W	H'FE8F 8A88	32
F1DMAC0 DMA reload 2D next-row offset register 4	F1DMAC0_DMR2DNROST4	R/W	H'FE8F 8A8C	32
F1DMAC0 DMA reload 2D next-block offset register 4	F1DMAC0_DMR2DNBOST4	R/W	H'FE8F 8A90	32
F1DMAC0 DMA reload 2D next-line offset register 4	F1DMAC0_DMR2DNLOST4	R/W	H'FE8F 8A94	32
F1DMAC0 area prohibited from use	—	—	H'FE8F 8A98 to H'FE8F 8A9C	—
F1DMAC0 DMA reload 2D column setup register 5	F1DMAC0_DMR2DCLM5	R/W	H'FE8F 8AA0	32
F1DMAC0 DMA reload 2D row setup register 5	F1DMAC0_DMR2DROW5	R/W	H'FE8F 8AA4	32
F1DMAC0 DMA reload 2D block setup register 5	F1DMAC0_DMR2DBLK5	R/W	H'FE8F 8AA8	32
F1DMAC0 DMA reload 2D next-row offset register 5	F1DMAC0_DMR2DNROST5	R/W	H'FE8F 8AAC	32
F1DMAC0 DMA reload 2D next-block offset register 5	F1DMAC0_DMR2DNBOST5	R/W	H'FE8F 8AB0	32
F1DMAC0 DMA reload 2D next-line offset register 5	F1DMAC0_DMR2DNLOST5	R/W	H'FE8F 8AB4	32
F1DMAC0 area prohibited from use	—	—	H'FE8F 8AB8 to H'FE8F 8ABC	—
F1DMAC0 DMA reload 2D column setup register 6	F1DMAC0_DMR2DCLM6	R/W	H'FE8F 8AC0	32
F1DMAC0 DMA reload 2D row setup register 6	F1DMAC0_DMR2DROW6	R/W	H'FE8F 8AC4	32
F1DMAC0 DMA reload 2D block setup register 6	F1DMAC0_DMR2DBLK6	R/W	H'FE8F 8AC8	32
F1DMAC0 DMA reload 2D next-row offset register 6	F1DMAC0_DMR2DNROST6	R/W	H'FE8F 8ACC	32
F1DMAC0 DMA reload 2D next-block offset register 6	F1DMAC0_DMR2DNBOST6	R/W	H'FE8F 8AD0	32
F1DMAC0 DMA reload 2D next-line offset register 6	F1DMAC0_DMR2DNLOST6	R/W	H'FE8F 8AD4	32
F1DMAC0 area prohibited from use	—	—	H'FE8F 8AD8 to H'FE8F 8ADC	—
F1DMAC0 DMA reload 2D column setup register 7	F1DMAC0_DMR2DCLM7	R/W	H'FE8F 8AE0	32
F1DMAC0 DMA reload 2D row setup register 7	F1DMAC0_DMR2DROW7	R/W	H'FE8F 8AE4	32
F1DMAC0 DMA reload 2D block setup register 7	F1DMAC0_DMR2DBLK7	R/W	H'FE8F 8AE8	32
F1DMAC0 DMA reload 2D next-row offset register 7	F1DMAC0_DMR2DNROST7	R/W	H'FE8F 8AEC	32
F1DMAC0 DMA reload 2D next-block offset register 7	F1DMAC0_DMR2DNBOST7	R/W	H'FE8F 8AF0	32
F1DMAC0 DMA reload 2D next-line offset register 7	F1DMAC0_DMR2DNLOST7	R/W	H'FE8F 8AF4	32
F1DMAC0 area prohibited from use	—	—	H'FE8F 8AF8 to H'FE8F 8DFC	—
F1DMAC0 F1-DMAC error flag register	F1DMAC0_DMBERR	R	H'FE8F A000	32
F1DMAC0 Data transfer status register	F1DMAC0_DMDTSTS	R	H'FE8F A004	32
F1DMAC0 F1 bus access status register	F1DMAC0_DMF1BASTS	R	H'FE8F A008	32

Register Name	Abbreviation	R/W	Address	Access Size
F1DMAC0 area prohibited from use	—	—	H'FE8F A00C to	—

Table 46.12 F1DMAC(1) Register Configuration

Register Name	Abbreviation	R/W	Address	Access Size
F1DMAC1 DMA current source address register 0	F1DMAC1_DMCSADR0	R/W	H'FE8F C000	32
F1DMAC1 DMA current destination address register 0	F1DMAC1_DMCDADR0	R/W	H'FE8F C004	32
F1DMAC1 DMA current byte count register 0	F1DMAC1_DMCBCT0	R/W	H'FE8F C008	32
F1DMAC1 DMA mode register 0	F1DMAC1_DMMOD0	R/W	H'FE8F C00C	32
F1DMAC1 DMA current source address register 1	F1DMAC1_DMCSADR1	R/W	H'FE8F C010	32
F1DMAC1 DMA current destination address register 1	F1DMAC1_DMCDADR1	R/W	H'FE8F C014	32
F1DMAC1 DMA current byte count register 1	F1DMAC1_DMCBCT1	R/W	H'FE8F C018	32
F1DMAC1 DMA mode register 1	F1DMAC1_DMMOD1	R/W	H'FE8F C01C	32
F1DMAC1 DMA current source address register 2	F1DMAC1_DMCSADR2	R/W	H'FE8F C020	32
F1DMAC1 DMA current destination address register 2	F1DMAC1_DMCDADR2	R/W	H'FE8F C024	32
F1DMAC1 DMA current byte count register 2	F1DMAC1_DMCBCT2	R/W	H'FE8F C028	32
F1DMAC1 DMA mode register 2	F1DMAC1_DMMOD2	R/W	H'FE8F C02C	32
F1DMAC1 DMA current source address register 3	F1DMAC1_DMCSADR3	R/W	H'FE8F C030	32
F1DMAC1 DMA current destination address register 3	F1DMAC1_DMCDADR3	R/W	H'FE8F C034	32
F1DMAC1 DMA current byte count register 3	F1DMAC1_DMCBCT3	R/W	H'FE8F C038	32
F1DMAC1 DMA mode register 3	F1DMAC1_DMMOD3	R/W	H'FE8F C03C	32
F1DMAC1 DMA current source address register 4	F1DMAC1_DMCSADR4	R/W	H'FE8F C040	32
F1DMAC1 DMA current destination address register 4	F1DMAC1_DMCDADR4	R/W	H'FE8F C044	32
F1DMAC1 DMA current byte count register 4	F1DMAC1_DMCBCT4	R/W	H'FE8F C048	32
F1DMAC1 DMA mode register 4	F1DMAC1_DMMOD4	R/W	H'FE8F C04C	32
F1DMAC1 DMA current source address register 5	F1DMAC1_DMCSADR5	R/W	H'FE8F C050	32
F1DMAC1 DMA current destination address register 5	F1DMAC1_DMCDADR5	R/W	H'FE8F C054	32
F1DMAC1 DMA current byte count register 5	F1DMAC1_DMCBCT5	R/W	H'FE8F C058	32
F1DMAC1 DMA mode register 5	F1DMAC1_DMMOD5	R/W	H'FE8F C05C	32
F1DMAC1 DMA current source address register 6	F1DMAC1_DMCSADR6	R/W	H'FE8F C060	32
F1DMAC1 DMA current destination address register 6	F1DMAC1_DMCDADR6	R/W	H'FE8F C064	32
F1DMAC1 DMA current byte count register 6	F1DMAC1_DMCBCT6	R/W	H'FE8F C068	32

Register Name	Abbreviation	R/W	Address	Access Size
F1DMAC1 DMA mode register 6	F1DMAC1_DMMOD6	R/W	H'FE8F C06C	32
F1DMAC1 DMA current source address register 7	F1DMAC1_DMCSADR7	R/W	H'FE8F C070	32
F1DMAC1 DMA current destination address register 7	F1DMAC1_DMCDADR7	R/W	H'FE8F C074	32
F1DMAC1 DMA current byte count register 7	F1DMAC1_DMCBCT7	R/W	H'FE8F C078	32
F1DMAC1 DMA mode register 7	F1DMAC1_DMMOD7	R/W	H'FE8F C07C	32
F1DMAC1 area prohibited from use	—	—	H'FE8F C080 to H'FE8F C1FC	—
F1DMAC1 DMA reload source address register 0	F1DMAC1_DMRSADR0	R/W	H'FE8F C200	32
F1DMAC1 DMA reload destination address register 0	F1DMAC1_DMRDADR0	R/W	H'FE8F C204	32
F1DMAC1 DMA reload byte count register 0	F1DMAC1_DMRBCT0	R/W	H'FE8F C208	32
F1DMAC1 area prohibited from use	—	—	H'FE8F C20C	—
F1DMAC1 DMA reload source address register 1	F1DMAC1_DMRSADR1	R/W	H'FE8F C210	32
F1DMAC1 DMA reload destination address register 1	F1DMAC1_DMRDADR1	R/W	H'FE8F C214	32
F1DMAC1 DMA reload byte count register 1	F1DMAC1_DMRBCT1	R/W	H'FE8F C218	32
F1DMAC1 area prohibited from use	—	—	H'FE8F C21C	—
F1DMAC1 DMA reload source address register 2	F1DMAC1_DMRSADR2	R/W	H'FE8F C220	32
F1DMAC1 DMA reload destination address register 2	F1DMAC1_DMRDADR2	R/W	H'FE8F C224	32
F1DMAC1 DMA reload byte count register 2	F1DMAC1_DMRBCT2	R/W	H'FE8F C228	32
F1DMAC1 area prohibited from use	—	—	H'FE8F C22C	—
F1DMAC1 DMA reload source address register 3	F1DMAC1_DMRSADR3	R/W	H'FE8F C230	32
F1DMAC1 DMA reload destination address register 3	F1DMAC1_DMRDADR3	R/W	H'FE8F C234	32
F1DMAC1 DMA reload byte count register 3	F1DMAC1_DMRBCT3	R/W	H'FE8F C238	32
F1DMAC1 area prohibited from use	—	—	H'FE8F C23C	—
F1DMAC1 DMA reload source address register 4	F1DMAC1_DMRSADR4	R/W	H'FE8F C240	32
F1DMAC1 DMA reload destination address register 4	F1DMAC1_DMRDADR4	R/W	H'FE8F C244	32
F1DMAC1 DMA reload byte count register 4	F1DMAC1_DMRBCT4	R/W	H'FE8F C248	32
F1DMAC1 area prohibited from use	—	—	H'FE8F C24C	—
F1DMAC1 DMA reload source address register 5	F1DMAC1_DMRSADR5	R/W	H'FE8F C250	32
F1DMAC1 DMA reload destination address register 5	F1DMAC1_DMRDADR5	R/W	H'FE8F C254	32
F1DMAC1 DMA reload byte count register 5	F1DMAC1_DMRBCT5	R/W	H'FE8F C258	32
F1DMAC1 area prohibited from use	—	—	H'FE8F C25C	—
F1DMAC1 DMA reload source address register 6	F1DMAC1_DMRSADR6	R/W	H'FE8F C260	32

Register Name	Abbreviation	R/W	Address	Access Size
F1DMAC1 DMA reload destination address register 6	F1DMAC1_DMRDADR6	R/W	H'FE8F C264	32
F1DMAC1 DMA reload byte count register 6	F1DMAC1_DMRBCT6	R/W	H'FE8F C268	32
F1DMAC1 area prohibited from use	—	—	H'FE8F C26C	—
F1DMAC1 DMA reload source address register 7	F1DMAC1_DMRSADR7	R/W	H'FE8F C270	32
F1DMAC1 DMA reload destination address register 7	F1DMAC1_DMRDADR7	R/W	H'FE8F C274	32
F1DMAC1 DMA reload byte count register 7	F1DMAC1_DMRBCT7	R/W	H'FE8F C278	32
F1DMAC1 area prohibited from use	—	—	H'FE8F C27C to H'FE8F C3FC	—
F1DMAC1 DMA control register A0	F1DMAC1_DMCNTA0	R/W	H'FE8F C400	32
F1DMAC1 DMA control register B0	F1DMAC1_DMCNTB0	R/W	H'FE8F C404	32
F1DMAC1 DMA control register A1	F1DMAC1_DMCNTA1	R/W	H'FE8F C408	32
F1DMAC1 DMA control register B1	F1DMAC1_DMCNTB1	R/W	H'FE8F C40C	32
F1DMAC1 DMA control register A2	F1DMAC1_DMCNTA2	R/W	H'FE8F C410	32
F1DMAC1 DMA control register B2	F1DMAC1_DMCNTB2	R/W	H'FE8F C414	32
F1DMAC1 DMA control register A3	F1DMAC1_DMCNTA3	R/W	H'FE8F C418	32
F1DMAC1 DMA control register B3	F1DMAC1_DMCNTB3	R/W	H'FE8F C41C	32
F1DMAC1 DMA control register A4	F1DMAC1_DMCNTA4	R/W	H'FE8F C420	32
F1DMAC1 DMA control register B4	F1DMAC1_DMCNTB4	R/W	H'FE8F C424	32
F1DMAC1 DMA control register A5	F1DMAC1_DMCNTA5	R/W	H'FE8F C428	32
F1DMAC1 DMA control register B5	F1DMAC1_DMCNTB5	R/W	H'FE8F C42C	32
F1DMAC1 DMA control register A6	F1DMAC1_DMCNTA6	R/W	H'FE8F C430	32
F1DMAC1 DMA control register B6	F1DMAC1_DMCNTB6	R/W	H'FE8F C434	32
F1DMAC1 DMA control register A7	F1DMAC1_DMCNTA7	R/W	H'FE8F C438	32
F1DMAC1 DMA control register B7	F1DMAC1_DMCNTB7	R/W	H'FE8F C43C	32
F1DMAC1 area prohibited from use	—		H'FE8F C440 to H'FE8F C4FC	—
F1DMAC1 DMA start control register	F1DMAC1_DMSCNT	R/W	H'FE8F C500	32
F1DMAC1 area prohibited from use	—		H'FE8F C504	—
F1DMAC1 DMA interrupt control register	F1DMAC1_DMICNT	R/W	H'FE8F C508	32
F1DMAC1 DMA common-interrupt control register	F1DMAC1_DMICNTA	R/W	H'FE8F C50C	32
F1DMAC1 DMA interrupt status register	F1DMAC1_DMISTS	R	H'FE8F C510	32
F1DMAC1 DMA transfer end detect register	F1DMAC1_DMEDET	R/W	H'FE8F C514	32
F1DMAC1 DMA arbitration status register	F1DMAC1_DMASTS	R/W	H'FE8F C518	32

Register Name	Abbreviation	R/W	Address	Access Size
F1DMAC1 area prohibited from use	—	—	H'FE8F C51C to H'FE8F C5FC	—
F1DMAC1 DMA 2D column setup register 0	F1DMAC1_DM2DCLM0	R/W	H'FE8F C600	32
F1DMAC1 DMA 2D row setup register 0	F1DMAC1_DM2DROW0	R/W	H'FE8F C604	32
F1DMAC1 DMA 2D block setup register 0	F1DMAC1_DM2DBLK0	R/W	H'FE8F C608	32
F1DMAC1 DMA 2D next-row offset register 0	F1DMAC1_DM2DNROST0	R/W	H'FE8F C60C	32
F1DMAC1 DMA 2D next-block offset register 0	F1DMAC1_DM2DNBOST0	R/W	H'FE8F C610	32
F1DMAC1 DMA 2D next-line offset register 0	F1DMAC1_DM2DNLOST0	R/W	H'FE8F C614	32
F1DMAC1 area prohibited from use	—	—	H'FE8F C618 to H'FE8F C61C	—
F1DMAC1 DMA 2D column setup register 1	F1DMAC1_DM2DCLM1	R/W	H'FE8F C620	32
F1DMAC1 DMA 2D row setup register 1	F1DMAC1_DM2DROW1	R/W	H'FE8F C624	32
F1DMAC1 DMA 2D block setup register 1	F1DMAC1_DM2DBLK1	R/W	H'FE8F C628	32
F1DMAC1 DMA 2D next-row offset register 1	F1DMAC1_DM2DNROST1	R/W	H'FE8F C62C	32
F1DMAC1 DMA 2D next-block offset register 1	F1DMAC1_DM2DNBOST1	R/W	H'FE8F C630	32
F1DMAC1 DMA 2D next-line offset register 1	F1DMAC1_DM2DNLOST1	R/W	H'FE8F C634	32
F1DMAC1 area prohibited from use	—	—	H'FE8F C638 to H'FE8F C63C	—
F1DMAC1 DMA 2D column setup register 2	F1DMAC1_DM2DCLM2	R/W	H'FE8F C640	32
F1DMAC1 DMA 2D row setup register 2	F1DMAC1_DM2DROW2	R/W	H'FE8F C644	32
F1DMAC1 DMA 2D block setup register 2	F1DMAC1_DM2DBLK2	R/W	H'FE8F C648	32
F1DMAC1 DMA 2D next-row offset register 2	F1DMAC1_DM2DNROST2	R/W	H'FE8F C64C	32
F1DMAC1 DMA 2D next-block offset register 2	F1DMAC1_DM2DNBOST2	R/W	H'FE8F C650	32
F1DMAC1 DMA 2D next-line offset register 2	F1DMAC1_DM2DNLOST2	R/W	H'FE8F C654	32
F1DMAC1 area prohibited from use	—	—	H'FE8F C658 to H'FE8F C65C	—
F1DMAC1 DMA 2D column setup register 3	F1DMAC1_DM2DCLM3	R/W	H'FE8F C660	32
F1DMAC1 DMA 2D row setup register 3	F1DMAC1_DM2DROW3	R/W	H'FE8F C664	32
F1DMAC1 DMA 2D block setup register 3	F1DMAC1_DM2DBLK3	R/W	H'FE8F C668	32
F1DMAC1 DMA 2D next-row offset register 3	F1DMAC1_DM2DNROST3	R/W	H'FE8F C66C	32
F1DMAC1 DMA 2D next-block offset register 3	F1DMAC1_DM2DNBOST3	R/W	H'FE8F C670	32
F1DMAC1 DMA 2D next-line offset register 3	F1DMAC1_DM2DNLOST3	R/W	H'FE8F C674	32
F1DMAC1 area prohibited from use	—	—	H'FE8F C678 to H'FE8F C67C	—

Register Name	Abbreviation	R/W	Address	Access Size
F1DMAC1 DMA 2D column setup register 4	F1DMAC1_DM2DCLM4	R/W	H'FE8F C680	32
F1DMAC1 DMA 2D row setup register 4	F1DMAC1_DM2DROW4	R/W	H'FE8F C684	32
F1DMAC1 DMA 2D block setup register 4	F1DMAC1_DM2DBLK4	R/W	H'FE8F C688	32
F1DMAC1 DMA 2D next-row offset register 4	F1DMAC1_DM2DNROST4	R/W	H'FE8F C68C	32
F1DMAC1 DMA 2D next-block offset register 4	F1DMAC1_DM2DNBOST4	R/W	H'FE8F C690	32
F1DMAC1 DMA 2D next-line offset register 4	F1DMAC1_DM2DNLOST4	R/W	H'FE8F C694	32
F1DMAC1 area prohibited from use	—	—	H'FE8F C698 to H'FE8F C69C	—
F1DMAC1 DMA 2D column setup register 5	F1DMAC1_DM2DCLM5	R/W	H'FE8F C6A0	32
F1DMAC1 DMA 2D row setup register 5	F1DMAC1_DM2DROW5	R/W	H'FE8F C6A4	32
F1DMAC1 DMA 2D block setup register 5	F1DMAC1_DM2DBLK5	R/W	H'FE8F C6A8	32
F1DMAC1 DMA 2D next-row offset register 5	F1DMAC1_DM2DNROST5	R/W	H'FE8F C6AC	32
F1DMAC1 DMA 2D next-block offset register 5	F1DMAC1_DM2DNBOST5	R/W	H'FE8F C6B0	32
F1DMAC1 DMA 2D next-line offset register 5	F1DMAC1_DM2DNLOST5	R/W	H'FE8F C6B4	32
F1DMAC1 area prohibited from use	—	—	H'FE8F C6B8 to H'FE8F C6BC	—
F1DMAC1 DMA 2D column setup register 6	F1DMAC1_DM2DCLM6	R/W	H'FE8F C6C0	32
F1DMAC1 DMA 2D row setup register 6	F1DMAC1_DM2DROW6	R/W	H'FE8F C6C4	32
F1DMAC1 DMA 2D block setup register 6	F1DMAC1_DM2DBLK6	R/W	H'FE8F C6C8	32
F1DMAC1 DMA 2D next-row offset register 6	F1DMAC1_DM2DNROST6	R/W	H'FE8F C6CC	32
F1DMAC1 DMA 2D next-block offset register 6	F1DMAC1_DM2DNBOST6	R/W	H'FE8F C6D0	32
F1DMAC1 DMA 2D next-line offset register 6	F1DMAC1_DM2DNLOST6	R/W	H'FE8F C6D4	32
F1DMAC1 area prohibited from use	—	—	H'FE8F C6D8 to H'FE8F C6DC	—
F1DMAC1 DMA 2D column setup register 7	F1DMAC1_DM2DCLM7	R/W	H'FE8F C6E0	32
F1DMAC1 DMA 2D row setup register 7	F1DMAC1_DM2DROW7	R/W	H'FE8F C6E4	32
F1DMAC1 DMA 2D block setup register 7	F1DMAC1_DM2DBLK7	R/W	H'FE8F C6E8	32
F1DMAC1 DMA 2D next-row offset register 7	F1DMAC1_DM2DNROST7	R/W	H'FE8F C6EC	32
F1DMAC1 DMA 2D next-block offset register 7	F1DMAC1_DM2DNBOST7	R/W	H'FE8F C6F0	32
F1DMAC1 DMA 2D next-line offset register 7	F1DMAC1_DM2DNLOST7	R/W	H'FE8F C6F4	32
F1DMAC1 area prohibited from use	—	—	H'FE8F C6F8 to H'FE8F C9FC	—
F1DMAC1 DMA reload 2D column setup register 0	F1DMAC1_DMR2DCLM0	R/W	H'FE8F CA00	32

Register Name	Abbreviation	R/W	Address	Access Size
F1DMAC1 DMA reload 2D row setup register 0	F1DMAC1_DMR2DROW0	R/W	H'FE8F CA04	32
F1DMAC1 DMA reload 2D block setup register 0	F1DMAC1_DMR2DBLK0	R/W	H'FE8F CA08	32
F1DMAC1 DMA reload 2D next-row offset register 0	F1DMAC1_DMR2DNROST0	R/W	H'FE8F CA0C	32
F1DMAC1 DMA reload 2D next-block offset register 0	F1DMAC1_DMR2DNBOST0	R/W	H'FE8F CA10	32
F1DMAC1 DMA reload 2D next-line offset register 0	F1DMAC1_DMR2DNLOST0	R/W	H'FE8F CA14	32
F1DMAC1 area prohibited from use	—	—	H'FE8F CA18 to H'FE8F CA1C	—
F1DMAC1	F1DMAC1_	R/W	H'FE8F CA1C	32
F1DMAC1 DMA reload 2D column setup register 1	F1DMAC1_DMR2DCLM1	R/W	H'FE8F CA20	32
F1DMAC1 DMA reload 2D row setup register 1	F1DMAC1_DMR2DROW1	R/W	H'FE8F CA24	32
F1DMAC1 DMA reload 2D block setup register 1	F1DMAC1_DMR2DBLK1	R/W	H'FE8F CA28	32
F1DMAC1 DMA reload 2D next-row offset register 1	F1DMAC1_DMR2DNROST1	R/W	H'FE8F CA2C	32
F1DMAC1 DMA reload 2D next-block offset register 1	F1DMAC1_DMR2DNBOST1	R/W	H'FE8F CA30	32
F1DMAC1 DMA reload 2D next-line offset register 1	F1DMAC1_DMR2DNLOST1	—	H'FE8F CA34	32
F1DMAC1 area prohibited from use	—		H'FE8F CA38 to H'FE8F CA3C	—
F1DMAC1	F1DMAC1_	R/W	H'FE8F CA3C	32
F1DMAC1 DMA reload 2D column setup register 2	F1DMAC1_DMR2DCLM2	R/W	H'FE8F CA40	32
F1DMAC1 DMA reload 2D row setup register 2	F1DMAC1_DMR2DROW2	R/W	H'FE8F CA44	32
F1DMAC1 DMA reload 2D block setup register 2	F1DMAC1_DMR2DBLK2	R/W	H'FE8F CA48	32
F1DMAC1 DMA reload 2D next-row offset register 2	F1DMAC1_DMR2DNROST2	R/W	H'FE8F CA4C	32
F1DMAC1 DMA reload 2D next-block offset register 2	F1DMAC1_DMR2DNBOST2	R/W	H'FE8F CA50	32
F1DMAC1 DMA reload 2D next-line offset register 2	F1DMAC1_DMR2DNLOST2	R/W	H'FE8F CA54	32
F1DMAC1 area prohibited from use	—	—	H'FE8F CA58 to H'FE8F CA5C	—
1DMAC0 DMA reload 2D column setup register 3	F1DMAC1_DMR2DCLM3	R/W	H'FE8F CA60	32
F1DMAC1 DMA reload 2D row setup register 3	F1DMAC1_DMR2DROW3	R/W	H'FE8F CA64	32
F1DMAC1 DMA reload 2D block setup register 3	F1DMAC1_DMR2DBLK3	R/W	H'FE8F CA68	32
F1DMAC1 DMA reload 2D next-row offset register 3	F1DMAC1_DMR2DNROST3	R/W	H'FE8F CA6C	32
F1DMAC1 DMA reload 2D next-block offset register 3	F1DMAC1_DMR2DNBOST3	R/W	H'FE8F CA70	32
F1DMAC1 DMA reload 2D next-line offset register 3	F1DMAC1_DMR2DNLOST3	R/W	H'FE8F CA74	32
F1DMAC1 Area prohibited from use	—	—	H'FE8F CA78 to H'FE8F CA7C	—

Register Name	Abbreviation	R/W	Address	Access Size
F1DMAC1 DMA reload 2D column setup register 4	F1DMAC1_DMR2DCLM4	R/W	H'FE8F CA80	32
F1DMAC1 DMA reload 2D row setup register 4	F1DMAC1_DMR2DROW4	R/W	H'FE8F CA84	32
F1DMAC1 DMA reload 2D block setup register 4	F1DMAC1_DMR2DBLK4	R/W	H'FE8F CA88	32
F1DMAC1 DMA reload 2D next-row offset register 4	F1DMAC1_DMR2DNROST4	R/W	H'FE8F CA8C	32
F1DMAC1 DMA reload 2D next-block offset register 4	F1DMAC1_DMR2DNBOST4	R/W	H'FE8F CA90	32
F1DMAC1 DMA reload 2D next-line offset register 4	F1DMAC1_DMR2DNLOST4	R/W	H'FE8F CA94	32
F1DMAC1 area prohibited from use	—	—	H'FE8F CA98 to H'FE8F CA9C	—
F1DMAC1 DMA reload 2D column setup register 5	F1DMAC1_DMR2DCLM5	R/W	H'FE8F CAA0	32
F1DMAC1 DMA reload 2D row setup register 5	F1DMAC1_DMR2DROW5	R/W	H'FE8F CAA4	32
F1DMAC1 DMA reload 2D block setup register 5	F1DMAC1_DMR2DBLK5	R/W	H'FE8F CAA8	32
F1DMAC1 DMA reload 2D next-row offset register 5	F1DMAC1_DMR2DNROST5	R/W	H'FE8F CAAC	32
F1DMAC1 DMA reload 2D next-block offset register 5	F1DMAC1_DMR2DNBOST5	R/W	H'FE8F CAB0	32
F1DMAC1 DMA reload 2D next-line offset register 5	F1DMAC1_DMR2DNLOST5	R/W	H'FE8F CAB4	32
F1DMAC1 area prohibited from use	—	—	H'FE8F CAB8 to H'FE8F CABC	—
F1DMAC1 DMA reload 2D column setup register 6	F1DMAC1_DMR2DCLM6	R/W	H'FE8F CAC0	32
F1DMAC1 DMA reload 2D row setup register 6	F1DMAC1_DMR2DROW6	R/W	H'FE8F CAC4	32
F1DMAC1 DMA reload 2D block setup register 6	F1DMAC1_DMR2DBLK6	R/W	H'FE8F CAC8	32
F1DMAC1 DMA reload 2D next-row offset register 6	F1DMAC1_DMR2DNROST6	R/W	H'FE8F CACC	32
F1DMAC1 DMA reload 2D next-block offset register 6	F1DMAC1_DMR2DNBOST6	R/W	H'FE8F CAD0	32
F1DMAC1 DMA reload 2D next-line offset register 6	F1DMAC1_DMR2DNLOST6	R/W	H'FE8F CAD4	32
F1DMAC1 area prohibited from use	—	—	H'FE8F CAD8 to H'FE8F CADC	—
F1DMAC1 DMA reload 2D column setup register 7	F1DMAC1_DMR2DCLM7	R/W	H'FE8F CAE0	32
F1DMAC1 DMA reload 2D row setup register 7	F1DMAC1_DMR2DROW7	R/W	H'FE8F CAE4	32
F1DMAC1 DMA reload 2D block setup register 7	F1DMAC1_DMR2DBLK7	R/W	H'FE8F CAE8	32
F1DMAC1 DMA reload 2D next-row offset register 7	F1DMAC1_DMR2DNROST7	R/W	H'FE8F CAEC	32
F1DMAC1 DMA reload 2D next-block offset register 7	F1DMAC1_DMR2DNBOST7	R/W	H'FE8F CAF0	32
F1DMAC1 DMA reload 2D next-line offset register 7	F1DMAC1_DMR2DNLOST7	R/W	H'FE8F CAF4	32
F1DMAC1 area prohibited from use	—	—	H'FE8F CAF8 to H'FE8F CDFC	—
F1DMAC1 F1-DMAC error flag register	F1DMAC1_DMBERR	R	H'FE8F E000	32

Register Name	Abbreviation	R/W	Address	Access Size
F1DMAC1 Data transfer status register	F1DMAC1_DMDTSTS	R	H'FE8F E004	32
F1DMAC1 F1 bus access status register	F1DMAC1_DMF1BASTS1	R	H'FE8F E008	32
F1DMAC1 area prohibited from use	—	—	H'FE8F E00C to	—

Table 46.13 Processing Modes and Register States

Abbreviation	Reset*	Module Standby
F1DMAC0/1_DMCSADR0	Initialized	Retained
F1DMAC0/1_DMCDADR0	Initialized	Retained
F1DMAC0/1_DMCBCT0	Initialized	Retained
F1DMAC0/1_DMMOD0	Initialized	Retained
F1DMAC0/1_DMCSADR1	Initialized	Retained
F1DMAC0/1_DMCDADR1	Initialized	Retained
F1DMAC0/1_DMCBCT1	Initialized	Retained
F1DMAC0/1_DMMOD1	Initialized	Retained
F1DMAC0/1_DMCSADR2	Initialized	Retained
F1DMAC0/1_DMCDADR2	Initialized	Retained
F1DMAC0/1_DMCBCT2	Initialized	Retained
F1DMAC0/1_DMMOD2	Initialized	Retained
F1DMAC0/1_DMCSADR3	Initialized	Retained
F1DMAC0/1_DMCDADR3	Initialized	Retained
F1DMAC0/1_DMCBCT3	Initialized	Retained
F1DMAC0/1_DMMOD3	Initialized	Retained
F1DMAC0/1_DMCSADR4	Initialized	Retained
F1DMAC0/1_DMCDADR4	Initialized	Retained
F1DMAC0/1_DMCBCT4	Initialized	Retained
F1DMAC0/1_DMMOD4	Initialized	Retained
F1DMAC0/1_DMCSADR5	Initialized	Retained
F1DMAC0/1_DMCDADR5	Initialized	Retained
F1DMAC0/1_DMCBCT5	Initialized	Retained
F1DMAC0/1_DMMOD5	Initialized	Retained
F1DMAC0/1_DMCSADR6	Initialized	Retained
F1DMAC0/1_DMCDADR6	Initialized	Retained
F1DMAC0/1_DMCBCT6	Initialized	Retained
F1DMAC0/1_DMMOD6	Initialized	Retained
F1DMAC0/1_DMCSADR7	Initialized	Retained
F1DMAC0/1_DMCDADR7	Initialized	Retained
F1DMAC0/1_DMCBCT7	Initialized	Retained

Abbreviation	Reset*	Module Standby
F1DMAC0/1_DMMOD7	Initialized	Retained
F1DMAC0/1_DMRSADR0	Initialized	Retained
F1DMAC0/1_DMRDADR0	Initialized	Retained
F1DMAC0/1_DMRBCT0	Initialized	Retained
F1DMAC0/1_DMRSADR1	Initialized	Retained
F1DMAC0/1_DMRDADR1	Initialized	Retained
F1DMAC0/1_DMRBCT1	Initialized	Retained
F1DMAC0/1_DMRSADR2	Initialized	Retained
F1DMAC0/1_DMRDADR2	Initialized	Retained
F1DMAC0/1_DMRBCT2	Initialized	Retained
F1DMAC0/1_DMRSADR3	Initialized	Retained
F1DMAC0/1_DMRDADR3	Initialized	Retained
F1DMAC0/1_DMRBCT3	Initialized	Retained
F1DMAC0/1_DMRSADR4	Initialized	Retained
F1DMAC0/1_DMRDADR4	Initialized	Retained
F1DMAC0/1_DMRBCT4	Initialized	Retained
F1DMAC0/1_DMRSADR5	Initialized	Retained
F1DMAC0/1_DMRDADR5	Initialized	Retained
F1DMAC0/1_DMRBCT5	Initialized	Retained
F1DMAC0/1_DMRSADR6	Initialized	Retained
F1DMAC0/1_DMRDADR6	Initialized	Retained
F1DMAC0/1_DMRBCT6	Initialized	Retained
F1DMAC0/1_DMRSADR7	Initialized	Retained
F1DMAC0/1_DMRDADR7	Initialized	Retained
F1DMAC0/1_DMRBCT7	Initialized	Retained
F1DMAC0/1_DMCNTA0	Initialized	Retained
F1DMAC0/1_DMCNTB0	Initialized	Retained
F1DMAC0/1_DMCNTA1	Initialized	Retained
F1DMAC0/1_DMCNTB1	Initialized	Retained
F1DMAC0/1_DMCNTA2	Initialized	Retained
F1DMAC0/1_DMCNTB2	Initialized	Retained
F1DMAC0/1_DMCNTA3	Initialized	Retained

Abbreviation	Reset*	Module Standby
F1DMAC0/1_DMCNTB3	Initialized	Retained
F1DMAC0/1_DMCNTA4	Initialized	Retained
F1DMAC0/1_DMCNTB4	Initialized	Retained
F1DMAC0/1_DMCNTA5	Initialized	Retained
F1DMAC0/1_DMCNTB5	Initialized	Retained
F1DMAC0/1_DMCNTA6	Initialized	Retained
F1DMAC0/1_DMCNTB6	Initialized	Retained
F1DMAC0/1_DMCNTA7	Initialized	Retained
F1DMAC0/1_DMCNTB7	Initialized	Retained
F1DMAC0/1_DMSCNT	Initialized	Retained
F1DMAC0/1_DMICNT	Initialized	Retained
F1DMAC0/1_DMICNTA	Initialized	Retained
F1DMAC0/1_DMISTS	Initialized	Retained
F1DMAC0/1_DMEDET	Initialized	Retained
F1DMAC0/1_DMASTS	Initialized	Retained
F1DMAC0/1_DM2DCLM0	Initialized	Retained
F1DMAC0/1_DM2DROW0	Initialized	Retained
F1DMAC0/1_DM2DBLK0	Initialized	Retained
F1DMAC0/1_DM2DNROST0	Initialized	Retained
F1DMAC0/1_DM2DNBOST0	Initialized	Retained
F1DMAC0/1_DM2DNLOST0	Initialized	Retained
F1DMAC0/1_DM2DCLM1	Initialized	Retained
F1DMAC0/1_DM2DROW1	Initialized	Retained
F1DMAC0/1_DM2DBLK1	Initialized	Retained
F1DMAC0/1_DM2DNROST1	Initialized	Retained
F1DMAC0/1_DM2DNBOST1	Initialized	Retained
F1DMAC0/1_DM2DNLOST1	Initialized	Retained
F1DMAC0/1_DM2DCLM2	Initialized	Retained
F1DMAC0/1_DM2DROW2	Initialized	Retained
F1DMAC0/1_DM2DBLK2	Initialized	Retained
F1DMAC0/1_DM2DNROST2	Initialized	Retained
F1DMAC0/1_DM2DNBOST2	Initialized	Retained

Abbreviation	Reset*	Module Standby
F1DMAC0/1_DM2DNLOST2	Initialized	Retained
F1DMAC0/1_DM2DCLM3	Initialized	Retained
F1DMAC0/1_DM2DROW3	Initialized	Retained
F1DMAC0/1_DM2DBLK3	Initialized	Retained
F1DMAC0/1_DM2DNROST3	Initialized	Retained
F1DMAC0/1_DM2DNBOST3	Initialized	Retained
F1DMAC0/1_DM2DNLOST3	Initialized	Retained
F1DMAC0/1_DM2DCLM4	Initialized	Retained
F1DMAC0/1_DM2DROW4	Initialized	Retained
F1DMAC0/1_DM2DBLK4	Initialized	Retained
F1DMAC0/1_DM2DNROST4	Initialized	Retained
F1DMAC0/1_DM2DNBOST4	Initialized	Retained
F1DMAC0/1_DM2DNLOST4	Initialized	Retained
F1DMAC0/1_DM2DCLM5	Initialized	Retained
F1DMAC0/1_DM2DROW5	Initialized	Retained
F1DMAC0/1_DM2DBLK5	Initialized	Retained
F1DMAC0/1_DM2DNROST5	Initialized	Retained
F1DMAC0/1_DM2DNBOST5	Initialized	Retained
F1DMAC0/1_DM2DNLOST5	Initialized	Retained
F1DMAC0/1_DM2DCLM6	Initialized	Retained
F1DMAC0/1_DM2DROW6	Initialized	Retained
F1DMAC0/1_DM2DBLK6	Initialized	Retained
F1DMAC0/1_DM2DNROST6	Initialized	Retained
F1DMAC0/1_DM2DNBOST6	Initialized	Retained
F1DMAC0/1_DM2DNLOST6	Initialized	Retained
F1DMAC0/1_DM2DCLM7	Initialized	Retained
F1DMAC0/1_DM2DROW7	Initialized	Retained
F1DMAC0/1_DM2DBLK7	Initialized	Retained
F1DMAC0/1_DM2DNROST7	Initialized	Retained
F1DMAC0/1_DM2DNBOST7	Initialized	Retained
F1DMAC0/1_DM2DNLOST7	Initialized	Retained
F1DMAC0/1_DMR2DCLM0	Initialized	Retained

Abbreviation	Reset*	Module Standby
F1DMAC0/1_DMR2DROW0	Initialized	Retained
F1DMAC0/1_DMR2DBLK0	Initialized	Retained
F1DMAC0/1_DMR2DNROST0	Initialized	Retained
F1DMAC0/1_DMR2DNBOST0	Initialized	Retained
F1DMAC0/1_DMR2DNLOST0	Initialized	Retained
F1DMAC0/1_DMR2DCLM1	Initialized	Retained
F1DMAC0/1_DMR2DROW1	Initialized	Retained
F1DMAC0/1_DMR2DBLK1	Initialized	Retained
F1DMAC0/1_DMR2DNROST1	Initialized	Retained
F1DMAC0/1_DMR2DNBOST1	Initialized	Retained
F1DMAC0/1_DMR2DNLOST1	Initialized	Retained
F1DMAC0/1_DMR2DCLM2	Initialized	Retained
F1DMAC0/1_DMR2DROW2	Initialized	Retained
F1DMAC0/1_DMR2DBLK2	Initialized	Retained
F1DMAC0/1_DMR2DNROST2	Initialized	Retained
F1DMAC0/1_DMR2DNBOST2	Initialized	Retained
F1DMAC0/1_DMR2DNLOST2	Initialized	Retained
F1DMAC0/1_DMR2DCLM3	Initialized	Retained
F1DMAC0/1_DMR2DROW3	Initialized	Retained
F1DMAC0/1_DMR2DBLK3	Initialized	Retained
F1DMAC0/1_DMR2DNROST3	Initialized	Retained
F1DMAC0/1_DMR2DNBOST3	Initialized	Retained
F1DMAC0/1_DMR2DNLOST3	Initialized	Retained
F1DMAC0/1_DMR2DCLM4	Initialized	Retained
F1DMAC0/1_DMR2DROW4	Initialized	Retained
F1DMAC0/1_DMR2DBLK4	Initialized	Retained
F1DMAC0/1_DMR2DNROST4	Initialized	Retained
F1DMAC0/1_DMR2DNBOST4	Initialized	Retained
F1DMAC0/1_DMR2DNLOST4	Initialized	Retained
F1DMAC0/1_DMR2DCLM5	Initialized	Retained
F1DMAC0/1_DMR2DROW5	Initialized	Retained
F1DMAC0/1_DMR2DBLK5	Initialized	Retained

Abbreviation	Reset*	Module Standby
F1DMAC0/1_DMR2DNROST5	Initialized	Retained
F1DMAC0/1_DMR2DNBOST5	Initialized	Retained
F1DMAC0/1_DMR2DNLOST5	Initialized	Retained
F1DMAC0/1_DMR2DCLM6	Initialized	Retained
F1DMAC0/1_DMR2DROW6	Initialized	Retained
F1DMAC0/1_DMR2DBLK6	Initialized	Retained
F1DMAC0/1_DMR2DNROST6	Initialized	Retained
F1DMAC0/1_DMR2DNBOST6	Initialized	Retained
F1DMAC0/1_DMR2DNLOST6	Initialized	Retained
F1DMAC0/1_DMR2DCLM7	Initialized	Retained
F1DMAC0/1_DMR2DROW7	Initialized	Retained
F1DMAC0/1_DMR2DBLK7	Initialized	Retained
F1DMAC0/1_DMR2DNROST7	Initialized	Retained
F1DMAC0/1_DMR2DNBOST7	Initialized	Retained
F1DMAC0/1_DMR2DNLOST7	Initialized	Retained
F1DMAC0/1_DMBERR	Initialized	Retained
F1DMAC0/1_DMDTSTS	Initialized	Retained
F1DMAC0/1_DMF1BAST	Initialized	Retained

Note: * See section 4.2, Reset Ranges, in "LSI Information" for the resetting conditions.

46.4.3 F1DMAC0/1 DMA Current Source Address Register n (F1DMAC0/1_DMCSADRn)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CSA[31:0]															
Initial value:	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CSA[31:0]															
Initial value:	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	CSA[31:0]	H'???? ????	R/W	Source address A31 to A0

This register is intended to set the start address of a transfer source. The value in this register is transferred to the work source address register when a DMA transfer begins. The value might be returned at the end of the operand transfer. This is not done if the rotate option (SAMOD = 011) is selected for the source.

If the source address reload function is enabled, the value in the DMA reload source address register (F1DMAC0/1_DMRSADRn) is returned to this DMA current source address register at the end of a DMA transfer.

This register should be set regardless of whether the reload function is enabled.

Notes:

1. Set this register so that a DMA transfer will use addresses aligned to an appropriate address boundary for the transfer unit size selected with DMMODn.SZSEL.
2. Write to this register only when both these conditions exist:
   (1) The relevant channel is not involved in 1-operand transfer (DMA arbitration status register (F1DMAC0/1_DMASTS) DASTS = 0 for that channel).
   (2) DMA transfer is prohibited (DMA start control register (F1DMAC0/1_DMSCNT) DMST = 0 or DMA control register B (F1DMAC0/1_DMCNTBn) DEN = 0).
   If a write to this register occurs in any other case, proper operation is not guaranteed.

46.4.4 F1DMAC0/1 DMA Current Destination Address Register n (F1DMAC0/1_DMCDADRn)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CDA[31:0]															
Initial value:	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CDA[31:0]															
Initial value:	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	CDA[31:0]	H'???? ????	R/W	Destination address A31 to A0

This register is intended to set the start address of a transfer destination. The value in this register is transferred to the work destination address register when a DMA transfer begins. It might be returned at the end of the operand transfer. This is not done if the rotate option (DAMOD = 011) is selected for the destination.

If the destination address reload function is enabled, the value in the DMA reload destination address register (F1DMAC0/1_DMRDADRn) is returned to this DMA current destination address register at the end of a DMA transfer.

This register should be set regardless of whether the reload function is enabled.

Notes:

1. Set this register so that a DMA transfer will use addresses aligned to an appropriate address boundary for the transfer unit size selected with DMMONDn.SZSEL.
2. Write to this register only when both these conditions exist:
   (1) The relevant channel is not involved in one-operand transfer (DMA arbitration status register (F1DMAC0/1_DMASTS) DASTS = 0 for that channel).
   (2) DMA transfer is prohibited (DMA start control register (F1DMAC0/1_DMSCNT) DMST = 0 or DMA control register B (F1DMAC0/1_DMCNTBn) DEN = 0).
   If a write to this register occurs in any other case, proper operation is not guaranteed.

46.4.5 F1DMAC0/1 DMA Current Byte Count Register n (F1DMAC0/1_DMCBCTn)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	CBC[25:0]									
Initial value:	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CBC[25:0]															
Initial value:	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All ?	R	Reserved These bits are always read as 0. The write value should always be 0.
25 to 0	CBC[25:0]	All ?	R/W	Number of DMA transfer bytes

This register is intended to specify the number of DMA transfer bytes. The value in this register is transferred to the work byte count register when a DMA transfer begins. That value is decremented by the specified number of transfer bytes upon each 1-unit transfer. The decrement values are shown below.

- -1 for a transfer unit size of 8 bits (SZSEL = 000)
- -2 for a transfer unit size of 16 bits (SZSEL = 001)
- -4 for a transfer unit size of 32 bits (SZSEL = 010)
- -8 for a transfer unit size of 64 bits (SZSEL = 011)
- -16 for a transfer unit size of 128 bits (SZSEL = 100)

When the value in the work byte counter register becomes H’000 0000, the DMA transfer ends (due to the byte count = 0). At this time, the associated bit in the DMA transfer end detect register (F1DMAC0/1_DMEDET) is set to 1.

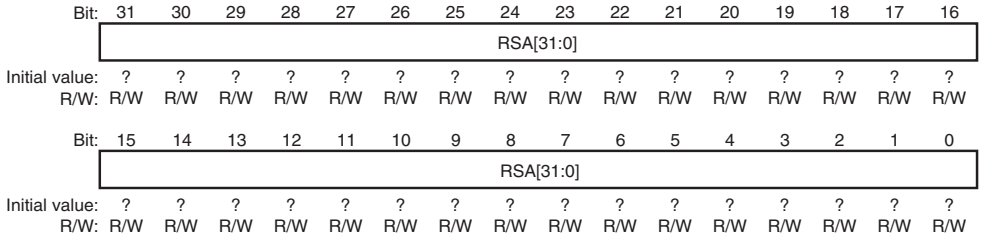
When the channel for DMA transfer is switched or when the DMA transfer ends (while the byte count reload function is disabled), the value in the work byte count register is returned to this register. When the DMA transfer ends (while the byte count reload function is enabled), the value in the DMA reload byte count register (F1DMAC0/1_DMRBCTn) is returned to this register.

This register should be set regardless of whether the reload function is enabled or disabled.

Notes:

1. If H'000 0000 is set, a maximum number of 64 Mbytes are transferred.
2. Set this register so that the byte count will be equal to 0 when the last data are transferred during DMA transfer.
3. Write to this register only when both these conditions exist:
   (1) The relevant channel is not involved in one-operand transfer (DMA arbitration status register (F1DMAC0/1_DMASTS) DASTS = 0 for that channel).
   (2) DMA transfer is prohibited (DMA start control register (F1DMAC0/1_DMSCNT) DMST = 0 or DMA control register B (F1DMAC0/1_DMCNTBn) DEN = 0).
   If a write to this register occurs in any other case, proper operation is not guaranteed.

46.4.6 F1DMAC0/1 DMA Reload Source Address Register n (F1DMAC0/1_DMRSADRn)



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	RSA[31:0]	H'???? ????	R/W	Reload source address A31 to A0

This register is intended to set an address which should be reloaded in the DMA current source address register (F1DMAC0/1_DMCSADRn).

To enable the reload function, set the DMA source address reload function enable bit (SRLOD) of DMA control register A (F1DMAC0/1_DMCNTAn) to 1. Also, set the address in both the DMA current source address register (F1DMAC0/1_DMCSADRn) and DMA reload source address register (F1DMAC0/1_DMRSADRn).

Note: Set this register so that a DMA transfer will use addresses aligned to an appropriate address boundary for the transfer unit size selected with DMMODn.SZSEL.

46.4.7 F1DMAC0/1 DMA Reload Destination Address Register n (F1DMAC0/1_DMRDADRn)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RDA[31:0]															
Initial value:	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RDA[31:0]															
Initial value:	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

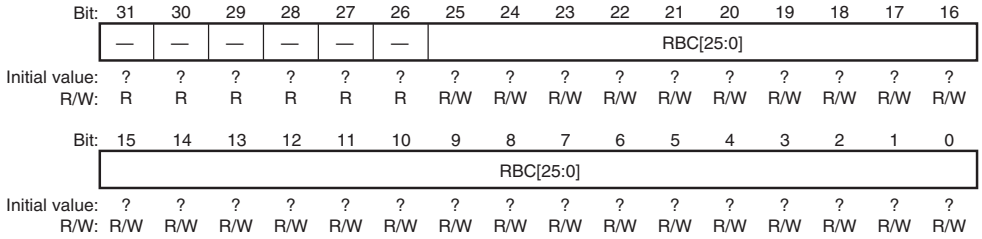
Bit	Bit Name	Initial Value	R/W	Description
31 to 0	RDA[31:0]	H'???? ????	R/W	Reload destination address A31 to A0

This register is intended to set an address which should be reloaded in the DMA current destination address register (F1DMAC0/1_DMCDADRn).

To enable the reload function, set the DMA destination address reload function enable bit (F1DMAC0/1_DRLOD) of DMA control register A (F1DMAC0/1_DMCNTAn) to 1. Also, set the address in both the DMA current destination address register (F1DMAC0/1_DMCDADRn) and DMA reload destination address register (F1DMAC0/1_DMRDADRn).

Note: Set this register so that a DMA transfer will use addresses aligned to an appropriate address boundary for the transfer unit size selected with DMMODn.SZSEL.

46.4.8 F1DMAC0/1 DMA Reload Byte Count Register n (F1DMAC0/1_DMRBCTn)



Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All ?	R	Reserved These bits are always read as 0. The write value should always be 0.
25 to 0	RBC[25:0]	H'???? ????	R/W	Number of DMA reload transfer bytes

This register is intended to set a byte count which should be reloaded in the DMA current byte count register (F1DMAC0/1_DMCBCTn).

To enable the reload function, set the DMA byte count reload function enable bit (F1DMAC0/1_BRLOD) of DMA control register A (F1DMAC0/1_DMCNTAn) to 1. Also, set the byte count in both the DMA current byte count register (F1DMAC0/1_DMCBCTn) and DMA reload byte count register (F1DMAC0/1_DMRBCTn).

Note: Set this register so that the byte count will be 0 when the last data are transferred during DMA transfer.

46.4.9 F1DMAC0/1 DMA Mode Register n (F1DMAC0/1_DMMODn)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	OPSEL[27:24]				—	—	—	—	—	SZSEL[18:16]		
Initial value:	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	SAMOD[14:12]			—	DAMOD[10:8]			—	—	—	—	SACT	DACT	DTCM[1:0]	
Initial value:	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All ?	R	Reserved These bits are always read as 0. The write value should always be 0.
27 to 24	OPSEL[27:24]	H'?	R/W	1-operand transfer data count select 0000: 1 unit 0001: 2 units 0010: 4 units 0011: 8 units 0100: 16 units 0101: 32 units 0110: 64 units 0111: 128 units 1000 - 1111: Prohibited
23 to 19	—	All ?	R	Reserved These bits are always read as 0. The write value should always be 0.
18 to 16	SZSEL [18:16]	B'???	R/W	Transfer Unit Size Select 000: Byte (8 bits) 001: Half word (16 bits) 010: Word (32 bits) 011: Double word (64 bits) 100: Quad word (128 bits) 101 - 111: Prohibited

Bit	Bit Name	Initial Value	R/W	Description
15	—	B'?	R	Reserved These bits are always read as 0. The write value should always be 0.
14 to 12	SAMOD [14:12]	B'???	R/W	Source Address Direction Control 000: Fixed 001: Increment 010: Decrement 011: Rotate 100: 2D addressing 101 - 111: Prohibited
11	—	B'?	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 8	DAMOD[10:8]	B'???	R/W	Destination Address Direction Control 000: Fixed 001: Increment 010: Decrement 011: Rotate 100: 2D addressing 101 - 111: Prohibited
7 to 4	—	All ?	R	Reserved These bits are always read as 0. The write value should always be 0.
3	SACT	B'?	R/W	Source DMA Active-Signal Output Control 0: Does not output the source DMA active signal. 1: Outputs the source DMA active signal at the time of read access.
2	DACT	B'?	R/W	Destination DMA Active-Signal Output Control 0: Does not output the destination DMA active signal. 1: Outputs the destination DMA active signal at the time of write access.

Bit	Bit Name	Initial Value	R/W	Description
1 to 0	DTCM[1:0]	B'??	R/W	DMA End Signal Output Control 00: Stop the TC signal output. 01: Output the TC signal in the last read cycle. 10: Output the TC signal in the last write cycle. 11: Output the TC signal after DMA transfer.

Note: Write to this register only when both these conditions exist:

(1) The relevant channel is not involved in one-operand transfer (DMA arbitration status register (F1DMAC0/1_DMASTS) DASTS = 0 for that channel).

(2) DMA transfer is prohibited (DMA start control register (F1DMAC0/1_DMSCNT) DMST = 0 or DMA control register B (F1DMAC0/1_DMCNTBn) DEN = 0).
If a write to this register occurs in any other case, proper operation is not guaranteed.

(1) OPSEL (1-Operand Transfer Data Count Select) Bits

Use these bits to select a 1-operand transfer data count. The selected number of units of data are repeatedly transferred. Channel arbitration does not take place during any 1-operand transfer.

These bits have no effect if the non-stop transfer option is selected with the DMA transfer condition select bit (DSEL = 11) of DMA control register A (F1DMAC0/1_DMCNTAn).

Note 1: Set the DMA current byte count register (F1DMAC0/1_DMCBCTn) to H000 0000 for the last operand transfer.

- When the transfer unit size is 8 bits (SZSEL = 000):
  Number equal to an integer multiple of the 1-operand transfer data count (× 1, × 2, × 3, etc.)
- When the transfer unit size is 16 bits (SZSEL = 001):
  Number equal to the 1-operand transfer data count times a multiple of 2 (× 2, × 4, × 6, etc.)
- When the transfer unit size is 32 bits (SZSEL = 010):
  Number equal to the 1-operand transfer data count times a multiple of 4 (× 4, × 8, × 12, etc.)
- When the transfer unit size is 64 bits (SZSEL = 011):
  Number equal to the 1-operand transfer data count times a multiple of 8 (× 8, × 16, × 24, etc.)
- When the transfer unit size is 128 bits (SZSEL = 100):
  Number equal to the 1-operand transfer data count times a multiple of 16 (× 16, × 32, × 48, etc.)

If anything else is specified, proper operation is not guaranteed. (see section 46.4.5, F1DMAC0/1 DMA Current Byte Count Register n (F1DMAC0/1_DMCBCTn), and section 46.4.8, F1DMAC0/1 DMA Reload Byte Count Register n (F1DMAC0/1_DMRBCTn), for details).

(2) SZSEL (Transfer Unit Size Select) Bits

Use these bits to select the 1-unit transfer size.

This unit of transfer can be a byte (8 bits), half word (16 bits), word (32 bits), double word (64 bits) or quad word (128 bits).

The selected size should not exceed the bit width of the data bus supported by the source and destination for DMA transfer. This data bus width is specific to hardware.

Note: For fly-by transfer, set the value equal to the bit width of the target SDRAM device (F1 port).

(3) SAMOD (Source Address Direction Control) Bits

Use these bits to select a count direction for the source address.

If these bits are set to 100 (2D addressing), the destination address direction control bits (DAMOD) cannot be set to 100.

Notes: 1. These bits have no effect if the fly-by transfer direction bits (FBDIR) are set to 10 for fly-by mode (i.e., if the F1 bus is selected for the source).
2. For pipeline-mode DMA transfer to the SDRAM device, select only 001 (increment), 011 (rotate) or 100 (2D addressing). Do not select 000 (factory fixed) or 010 (decrement).

(4) DAMOD (Destination Address Direction Control) Bits

Use these bits to select a count direction for the destination address.

If these bits are set to 100 (2D addressing), the source address direction control bits (SAMOD) cannot be set to 100.

Notes: 1. These bits have no effect if the fly-by transfer direction bits (FBDIR) are set to 01 for fly-by mode (i.e., if the F1 bus is selected for the destination).
2. For pipeline-mode DMA transfer to the SDRAM device, select only 001 (increment), 011 (rotate) or 100 (2D addressing). Do not select 000 (factory fixed) or 010 (decrement).

Table 46.14 shows the counter decrement and increment values for the DMA source/destination address register (see section 46.4.40, Rotate Function, for details about the rotate function for addressing mode). If 2D addressing is selected with these bits (SAMOD or DAMOD), the current 2D addressing registers and reload 2D addressing registers are enabled (these registers are described in section 46.4.18 and later).

For pipeline or fly-by transfer to an external device or module which supports burst access, be sure to select 001 (increment), 011 (rotate) or 100 (2D addressing).

Table 46.14 Counter Increment/Decrement Values for the DMA Source/Destination Address Register

	Addressing Mode SAMOD or DAMOD				
Transfer Unit Size Select Bits (SZSEL)	**000 (Factory-fixed)**	**001 (Plus)**	**010 (Minus)**	**011 (Rotate)**	**100 (2D)**
000 (8 bits)	±0	+1	-1	+1	+1
001 (16 bits)	±0	+2	-2	+2	+2
010 (32 bits)	±0	+4	-4	+4	+4
011 (64 bits)	±0	+8	-8	+8	+8
100 (128 bits)	±0	+16	-16	+16	+16

(5) SACT (Source DMA Active-Signal Output Control) Bit

Use this bit to control the output of the source DMA active signal (DMAACTS_N) associated with the request factor specified with the DCTG bits.

If this bit is set to 0, the DMAACTS_N signal is fixed at the "H" level and is not output as a valid signal.

If set to 1, the DMAACTS_N signal is set at the "L" level and output as a valid signal for the second and subsequent DMAC read cycles.

If the software trigger is selected with the DMA request factor select bits (DCTG), the DMAACTS0_N signal is output.

(6) DACT (Destination DMA Active-Signal Output Control) Bit

Use this bit to control the output of the destination DMA active signal (DMAACTD_N) associated with the request factor specified with the DCTG bits.

If this bit is set to 0, the DMAACTD_N signal is fixed at the "H" level and is not output as a valid signal.

If set to 1, the DMAACTD_N signal is set at the "L" level and is output as a valid signal for the second and subsequent DMAC write cycles.

If the software trigger is selected with the DMA request factor select bits (DCTG), the DMAACTD0_N signal is output.

(7) DTCM (DMA End Signal Output Control) Bits

Use these bits to control the output of the DMA end signal (DMATC_N) which is provided when the DMA transfer end condition is detected.

If these bits are set to 00, the DMATC_N signal is fixed at the "H" level and is not output as a valid signal when DMA transfer ends.

If set to 01, the DMATC_N signal is output as a valid signal during the cycle subsequent to the read cycle immediately before the end of DMA transfer.

If set to 10, the DMATC_N signal is output as a valid signal during the cycle subsequent to the write cycle immediately before the end of DMA transfer.

If set to 11, the DMATC_N signal is output as an "L" pulse signal for one clock at the time of DMA transfer end interrupt.

If the software trigger is selected with the DMA request factor select bits (DCTG), the DMATC0_N signal is output.

If a request factor from the on-chip peripheral circuit is selected with the DMA request factor select bits (DCTG), the DMATC_N signal is not output as a valid signal regardless of the settings of the DTCM bits.

If the fly-by mode is selected (MDSEL = 10), set the DTCM bits to 00.

46.4.10 F1DMAC0/1 DMA Control Register An (F1DMAC0/1_DMCNTAn)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	MDSEL[29:28]		—	—	DSEL[25:24]		—	—	FBDIR[21:20]		—	—	STRG[17:16]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	BKEEP	2DRLOD	BRLOD	SRLOD	DRLOD	—	—	DCTG[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 30	—	B'00	R	Reserved These bits are always read as 0. The write value should always be 0.
29 to 28	MDSEL[29:28]	B'00	R/W	DMA transfer mode select 00: Cycle stealing mode 01: Pipeline mode 10: Fly-by mode 11: Setting prohibited
27 to 26	—	B'00	R	Reserved These bits are always read as 0. The write value should always be 0.
25 to 24	DSEL[25:24]	B'00	R/W	DMA transfer condition select 00: Single-operand transfer 01: Consecutive-operand transfer 10: Setting prohibited 11: Non-stop transfer
23 to 22	—	B'00	R	Reserved These bits are always read as 0. The write value should always be 0.
21 to 20	FBDIR[21:20]	B'00	R/W	DMA fly-by transfer direction select 00: Setting prohibited 01: SDRAM device → F1 bus 10: F1 bus → SDRAM device 11: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Description
19 to 18	—	B'00	R	Reserved These bits are always read as 0. The write value should always be 0.
17 to 16	STRG[17:16]	B'00	R/W	Input sense mode select 00: Rising-edge 01: High level 10: Falling-edge 11: Low level
15 to 13	—	B'00	R	Reserved These bits are always read as 0. The write value should always be 0.
12	BKEEP	B'0	R/W	Bus mastership keep function enable 0: Disables the bus mastership keep function. 1: Enables the bus mastership keep function.
11	2DRLOD	B'0	R/W	2D reload function enable 0: Disables the 2D reload function. 1: Enables the 2D reload function.
10	BRLOD	B'0	R/W	DMA byte count reload function enable 0: Disables the DMA byte count reload function. 1: Enables the DMA byte count reload function.
9	SRLOD	B'0	R/W	DMA source address reload function enable 0: Disables the source address reload function. 1: Enables the source address reload function.
8	DRLOC	B'0	R/W	DMA destination address reload function enable 0: Disables the destination address reload function. 1: Enables the destination address reload function.
7 to 6	—	B'00	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
5 to 0	DCTG[5:0]	All 0	R/W	DMA Request Factor Select 000000: Software trigger 000001 - 001000: DMA request signal 001001 and above: Reserved (Refer to table 46.3, F1DMAC(0) Source Assignments and table 46.4, F1DMAC(1) Source Assignments.)

Notes: Change the bits of DMA control register A (F1DMAC0/1_DMCNTAn) other than its reload function enable bits (BRLOD, SRLOD and DRLOD) only when both these conditions exist:

1. The relevant channel is not involved in 1-operand transfer (DMA arbitration status register (F1DMAC0/1_DMASTS) DASTS = 0 for that channel).
2. DMA transfer is prohibited (DMA start control register (F1DMAC0/1_DMSCNT) DMST = 0 or DMA control register B (F1DMAC0/1_DMCNTBn) DEN = 0).
   If a write to this register occurs in any other case, proper operation is not guaranteed.

(1) MDSEL (DMA Transfer Mode Select) Bits

Use these bits to select a DMA transfer mode.

If these bits are set to 00, the cycle stealing mode is selected.

If set to 01, the pipeline mode is selected.

If set to 10, the fly-by mode is selected.

Do not set these bits to 11. If this is done, proper operation is not guaranteed (see 46.4.33, DMA Transfer Modes, for details).

Notes: 1. The non-stop transfer option (DSEL = 11) cannot be selected for pipeline mode (MDSEL = 01) if the source or destination is an SDRAM device.
2. The non-stop transfer option (DSEL = 11) cannot be selected for fly-by mode (MDSEL = 10).

(2) DSEL (DMA Transfer Condition Select) Bits

Use these bits to select a type of DMA transfer.

If these bits are set to 00, a single-operand transfer is performed.

If set to 01, a consecutive-operand transfer is performed.

If set to 11, a non-stop transfer is performed (see section 46.4.34, DMA Transfers, for details).

Do not set these bits to 10. If this is done, proper operation cannot be guaranteed.

(3) FBDIR (DMA Fly-by Transfer Direction Select) Bits

Use these bits to select a fly-by transfer direction.

If these bits are set to 01, a transfer from the SDRAM device to the F1DMAC-connected module is performed.

If set to 10, a transfer from the F1DMAC-connected module to the SDRAM device is performed.

These bits are only valid for fly-by mode (MDSEL = 10).

If a wrong transfer direction is selected, proper operation is not guaranteed.

(4) STRG (Input Sense Mode Select) Bits

Use these bits to select an input sense mode, based on the request factor selected with the DMA request factor select bits (DCTG), for DMA request signals which are input to the DMAC. These bits are valid when the request factor is a DMA request signal (DCTG = 000001 to 111111).

If the software trigger is selected with the request factor select bits (DCTG = 000000), set the STRG bits to 00 for rising-edge sensing.

(5) BKEEP (Bus Mastership Keep Function Enable) Bit

Use this bit, associated with the selected channel, to control whether the request for slave bus mastership should be still valid when there is a subsequent DMA transfer request after the preceding operand transfer.

If this bit is set to 0, the request for bus mastership is negated until the next operand transfer begins. If any other bus master issues an access request while the request is negated, the F1DMACI/F for each slave can accept that access request.

If set to 1, the request for slave bus mastership continues to be valid until the next operand transfer begins. Then, the subsequent operands are transferred one after another. If any other bus master issues an access request while the request is valid, the F1DMACI/F for each slave cannot accept that access request.

This bit is enabled only when the fly by mode is selected (MDSEL = 10).

(6) 2DRLOD (2D Reload Function Enable) Bit

Use this bit to select whether to enable or disable reloading data into the six current 2D addressing registers when the DMA transfer end condition is detected.

If this bit is cleared to 0, no data are reloaded into the six current 2D addressing registers.

If set to 1, the contents of the six 2D addressing registers are reloaded into the current 2D addressing registers when the DMA transfer end condition is detected.

If the 2D addressing function is not implemented, this bit should be always read as 0.

(7) BRLOD (DMA Byte Count Reload Function Enable) Bit

Use this bit to select whether to enable or disable reloading the byte count when the DMA transfer end condition is detected.

If this bit is cleared to 0, no data are reloaded.

If set to 1, the contents of the DMA reload byte count register (F1DMAC0/1_DMRBCTn) are reloaded into the DMA current byte count register (F1DMAC0/1_DMCBCTn) when the DMA transfer end condition is detected.

(8) SRLOD (DMA Source Address Reload Function Enable) Bit

Use this bit to select whether to enable or disable reloading the source address when the DMA transfer end condition is detected.

If this bit is cleared to 0, no data are reloaded.

If set to 1, the contents of the DMA reload source address register (F1DMAC0/1_DMRSADRn) are reloaded into the DMA current source address register (F1DMAC0/1_DMCSADRn) when the DMA transfer end condition is detected.

(9) DRLOD (DMA Destination Address Reload Function Enable) Bit

Use this bit to select whether to enable or disable reloading the destination address when the DMA transfer end condition is detected.

If this bit is cleared to 0, no data are reloaded.

If set to 1, the contents of the DMA reload destination address register (F1DMAC0/1_DMRDADRn) are reloaded into the DMA current destination address register (F1DMAC0/1_DMCDADRn) when the DMA transfer end condition is detected.

(10) DCTG (DMA Request Factor Select) Bits

Use these bits to select a DMA request factor.

(Refer to table 46.3, F1DMAC(0) Source Assignments and table 46.4, F1DMAC(1) Source Assignments.)

46.4.11 F1DMAC0/1 DMA Control Register Bn (F1DMAC0/1_DMCNTBn)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	DEN	—	—	—	—	—	—	—	DREQ
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	ECLR	—	—	—	—	—	—	—	DSCLR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	DEN	B'0	R/W	DMA transfer enable 0: Disables DMA transfer. 1: Enables DMA transfer.
23 to 17	—	B'00	R	Reserved These bits are always read as 0. The write value should always be 0.
16	DREQ	B'0	R/W	DMA request 0: Does not generate a DMA request. 1: Generates a DMA request.
15 to 9	—	B'00	R	Reserved These bits are always read as 0. The write value should always be 0.
8	ECLR	B'0	R/W	DMA transfer enable clear 0: Does not clear the DMA transfer enable bit to 0 when the DMA transfer end condition is detected. 1: Clears the DMA transfer enable bit to 0 when the DMA transfer end condition is detected.
7 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
0	DSCLR	B'0	R/*	DMAC internal status clear Read: This bit is read as 0. Write: 0: Invalid 1: Initializes the DMAC internal status.

Note: If the software trigger is selected as the DMA request factor, the DMA request (DREQ) bit can be set to 1 regardless of the DMA transfer enable (DEN) and DMAC module start (DMST) bit settings and of the operand transfer status. Even if that option is selected, clear the DMA request (DREQ) bit to 0 and write to the DMAC internal status clear (DSCLR) bit only when both these conditions are satisfied:

(1) The relevant channel is not involved in 1-operand transfer (DMA arbitration status register (F1DMAC0/1_DMASTS) DASTS = 0 for that channel).

(2) DMA transfer is prohibited (DMA start control register (F1DMAC0/1_DMSCNT) DMST = 0 or DMA control register B (F1DMAC0/1_DMCNTBn) DEN = 0).
If a write to this register occurs in any other cases, proper operation is not guaranteed.

* Indicate that writing 0 has no effect and that a value of 1 is not held after it is written.

(1) DEN (DMA Transfer Enable) Bit

Use this bit to disable or enable a DMA transfer.

If this bit is set to 0, a DMA transfer via the relevant channel is disabled.

If set to 1, a DMA transfer via the relevant channel is enabled (see section 46.4.35, DMA Startup, for information about the start of DMA transfer).

Even if this bit is 0, the DMA request (DREQ) bit changes due to a DMA request made to the DMAC.

This bit is cleared to 0 automatically when the DMA transfer end condition is detected if the DMA transfer enable (ECLR) bit = 1.

If this bit is cleared to 0 during DMA transfer, the relevant channel can be made inactive after the end of 1-operand transfer (see section 46.4.36 (4), Suspending, Resuming and Aborting a DMA Transfer, for details).

(2) DREQ (DMA Request) Bit

Use this bit to determine the presence or absence of a DMA request.

This bit is available to handle DMA requests if the software trigger is selected with the DMA request factor select bits (DCTG = 000000).

This bit changes depending on the status of the DMA request input to the DMAC regardless of the settings of both DMAC module start bit (DMST) and DMA transfer enable bit (DEN). The conditions which cause the DREQ bit to be set and cleared depend on the settings of both DMA request factor select bit (DCTG) and input sense mode select bit (STRG) as shown below.

<When the Software Trigger Is Selected with the DMA Request Factor Select Bits (DCTG)>

- Setting Condition
  The DREQ bit is set to 1 if 1 is written to it by software. As a result, a DMA request is generated.
- Clearing Condition
  The DREQ bit is cleared to 0 if one of these actions is taken:
  — Write 0 to this bit by software.
  — Start an operand transfer associated with this bit.

<When an Option Other Than the Software Trigger Is Selected with the DMA Request Factor Select Bits (DCTG) and the Level Sense Mode Is Selected>

- Setting Condition

The DREQ bit is set to 1 if there is a match between the level selected with the input sense mode select bit (STRG) and the DMA request input level (i.e., if there is a DMA request).

- Clearing Condition

The DREQ bit is cleared to 0 if there is not a match between the level selected with the input sense mode select bit (STRG) and the DMA request input level (i.e., if there is not a DMA request).

(If there is not a DMA request before it is accepted, then this request is not held and the DMA request bit (DREQ) is cleared. Thus, if the level sense mode is selected, hold a DMA request until it is accepted.

Note: If the selected request factor is not the software trigger, do not write 1 to the DMA request bit (DREQ) by software. If this is done, proper operation is not guaranteed.

<When an Option Other Than the Software Trigger Is Selected with the DMA Request Factor Select Bits (DCTG) and the Edge Sense Mode Is Selected>

- Setting Condition

The DREQ bit is set to 1 if the edge selected with the input sense mode select bit (STRG) is detected (i.e., if there is a DMA request).

After the DREQ bit is set to 1, it remains set regardless of the status of the subsequent DMA request signal until one of the actions for clearing it to 0 is taken.

- Clearing Condition

The DREQ bit is cleared to 0 if one of these actions is taken:

— Write 0 to this bit by software.
— Start an operand transfer associated with this bit.

Notes: 1. If the selected request factor is not the software trigger, do not write 1 to the DMA request bit (DREQ) by software. If this is done, proper operation is not guaranteed.
2. If the DMA request factor select bits (DCTG) and input sense mode select bit (STRG) of the DMA control register (F1DMAC0/1_DMCNTAn) are set, be sure to clear the DMA request bit (DREQ) for the selected channel to 0 and then enable a DMA transfer (with DMST = 1 and DEN = 1).

(3) ECLR (DMA Transfer Enable Clear) Bit

Use this bit to select whether to clear the DMA transfer enable bit (DEN) to 0 when the DMA transfer end condition is detected.

If this bit is cleared to 0, the DMA transfer enable bit (DEN) is not cleared to 0 when the DMA transfer end condition is detected.

If set to 1, the DMA transfer enable bit (DEN) is cleared to 0 when the DMA transfer end condition is detected.

Note: If a write to the DMA transfer enable clear bit occurs while the associated channel is being used for 1-operand transfer, proper operation is not guaranteed.

(4) DSCLR (DMAC Internal Status Clear) Bit

This bit is available to initialize the DMAC internal status by aborting a 1-DMA transfer (before the byte count reaches 0). Writing 1 to this bit clears only the transfer status of the DMA internal circuit and does not initialize each register. This bit is always read as 0.

Note: Write to this bit only when both these conditions are satisfied:

(1) The relevant channel is not involved in 1-operand transfer (DMA arbitration status register (F1DMAC0/1_DMASTS) DASTS = 0 for that channel).
(2) DMA transfer is prohibited (DMA start control register (F1DMAC0/1_DMSCNT) DMST = 0 or DMA control register B (F1DMAC0/1_DMCNTBn) DEN = 0).
If a write to this register occurs in any other case, proper operation is not guaranteed.

46.4.12 F1DMAC0/1 DMA Start Control Register (F1DMAC0/1_DMSCNT)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DMST
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	DMST	B'0	R/W	DMAC module start 0: Stops the DMAC. 1: Starts the DMAC.
15 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

(1) DMST (DMAC Module Start) Bit

Use this bit to start or stop the DMAC module.

If this bit is cleared to 0, the DMAC module becomes inactive.

If set to 1, the DMAC module becomes active (see section 46.4.35, DMA Startup, and section 46.4.36 (4), Suspending, Resuming and Aborting a DMA Transfer, for details).

46.4.13 F1DMAC0/1 DMA Interrupt Control Register (F1DMAC0/1_DMICNT)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DINTM[31:24]								—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	DINTM[31:24]	All 0	R/W	DMA interrupt control 0: Disables interrupts. 1: Enables interrupts.
23 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Note: Bits 31 to 24 correspond to channels 0 to 7.

(1) DINTM (DMA Interrupt Control) Bit

Use this bit to control whether to generate DMA transfer end interrupts to the interrupt controller for each channel.

If this bit is cleared to 0, no interrupt request is generated to the interrupt controller.

If set to 1, an interrupt request can be generated to the interrupt controller when the DMA transfer end condition is detected (see section 46.4.36 (2), DMA Interrupt Requests, for details).

46.4.14 F1DMAC0/1 DMA Common-Interrupt Control Register (F1DMAC0/1_DMICNTA)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DINTA[31:24]								—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	DINTA[31:24]	All 0	R/W	DMA common-interrupt request signal control 0: Does not share an interrupt request. 1: Shares an interrupt request.
23 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Note: Bits 31 to 24 correspond to channels 0 to 7.

(1) DINTA (DMA Common-Interrupt Request Signal Control) Bits

Use these bits to specify whether to share an interrupt request signal among channels.

If one of the bits is set to 1, the signal for the relevant channel is shared as the common interrupt request signal among the channels.

If set to 0, the signal for the relevant channel is not shared as the common interrupt request signal.

If one of these bits is set to 1 for a channel, the DMA interrupt status register (F1DMAC0/1_DMISTS) shows only the status of that channel when the common interrupt request signal is generated (see section 46.4.36 (2), DMA Interrupt Requests, for details).

46.4.15 F1DMAC0/1 DMA Interrupt Status Register (F1DMAC0/1_DMISTS)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DISTS[31:24]								—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	DISTS[31:24]	All 0	R	DMA interrupt request status 0: Interrupt request absent 1: Interrupt request present
23 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Notes: 1. This is a read-only register.
2. Bits 31 to 24 correspond to channels 0 to 7.

(1) DISTS (DMA Interrupt Request Status) Bits

Use these bits to check for the common interrupt request to the interrupt controller.

- Setting Condition

If one of the DMA common interrupt request signal control bits (DINTA) is 1, the channel-associated DISTS bit is set to 1 when the DMA transfer end condition is detected.

These bits are not affected by the DMA interrupt control bit (DINTM) settings.

- Clearing Condition

One of the DMA transfer end condition detect bits (DEDET) of the DMA transfer end detect register (F1DMAC0/1_DMEDET) is associated with the channel where an interrupt occurs. If this DEDET bit is cleared, then the DISTS bit is also cleared to 0 (see section 46.4.36 (2), DMA Interrupt Requests, for details).

46.4.16 F1DMAC0/1 DMA Transfer End Detect Register (F1DMAC0/1_DMEDET)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DEDET[31:24]								—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	DEDET[31:24]	All 0	R/*	DMA transfer end condition detect for reads 0: DMA transfer end condition not detected 1: DMA transfer end condition detected DMA transfer end condition detect and DMA interrupt request status clear for writes 0: Invalid 1: DMA transfer end condition detected and DMA interrupt request status cleared
23 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Notes: Bits 31 to 24 correspond to channels 0 to 7.
* Indicates that writing 0 has no effect and that a value of 1 is not held after it is written.

(1) DEDET (DMA Transfer End Condition Detect) Bits

These bits are available to determine whether the DMA transfer end condition is detected for each channel. This register is not cleared automatically by reading from it. If its bits are set to 1, they always hold the value unless they are cleared by software.

- Setting Condition

If the DMA transfer end condition is detected, the bit is set to 1.

- Clearing Condition

If 1 is written to the bit to be cleared, it is cleared to 0.

Write 0 to the bit which should not be cleared. A write by software does not affect the bit which is 0. It holds the same value before and after that write.

To use a DMA transfer end interrupt, write 1 to the DMA transfer end condition detect bit (DEDET) with the interrupt handler. This bit should be associated with the channel where the interrupt request is generated.

The DMA transfer end condition bit (DEDET) is cleared to 0. Also, the DMA interrupt request status bit (DISTS) is cleared.

46.4.17 F1DMAC0/1 DMA Arbitration Status Register (F1DMAC0/1_DMASTS)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DASTS[31:24]								—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	DASTS[31:24]	All 0	R	DMA arbitration status for reads 0: Operand transfer not underway 1: Operand transfer underway DMA arbitration status clear for writes
23 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Note: Bits 31 to 24 correspond to channels 0 to 7.

(1) DASTS (DMA Arbitration Status) Bits

These bits are available to determine whether the channels are involved in DMA transfer.

- **Setting Condition**
  At the start of 1-operand transfer or non-stop transfer on a channel, the bit associated with the channel is set to 1.

- **Clearing Condition**
  At the end of 1-operand transfer or non-stop transfer over a channel, the bit associated with the channel is cleared to 0.

<Current 2D Addressing Registers>

46.4.18 F1DMAC0/1 DMA 2D Column Setup Register n (F1DMAC0/1_DM2DCLMn)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DCDN[15:0]															
Initial value:	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

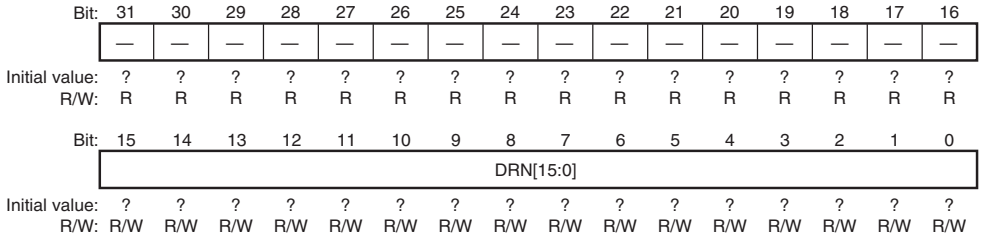
Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	H'????	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 0	DCDN[15:0]	H'????	R/W	DMA block column data count 00000000_00000000: 1 : 11111111_11111111: 65,536

(1) DCDN (DMA Block Column Data Count) Bits

Use these bits to specify the column data count per block.

Note: Set the bits to the data count selected with the 1-operand transfer data count select bits (OPSEL) or to an integer multiple of that data count. If they are set to something else, proper operation is not guaranteed.

46.4.19 F1DMAC0/1 DMA 2D Row Setup Register n (F1DMAC0/1_DM2DROWn)

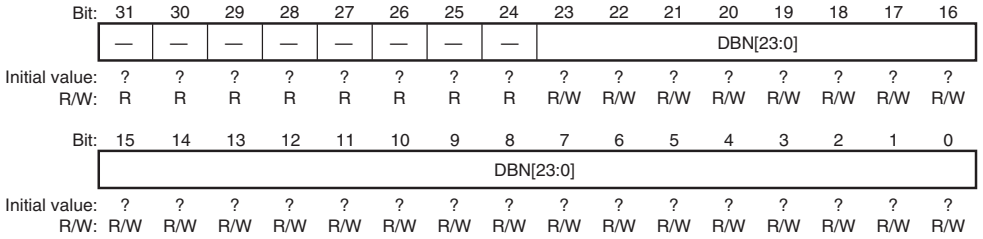


Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	H'????	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 0	DRN[15:0]	H'????	R/W	DMA block row count 00000000_00000000: 1 : 11111111_11111111: 65,536

(1) DRN (DMA Block Row Count) Bits

Use these bits to specify the number of rows per block.

46.4.20 F1DMAC0/1 DMA 2D Block Setup Register n (F1DMAC0/1_DM2DBLKn)



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All ?	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	DBN[23:0]	All ?	R/W	DMA block count 00000000_00000000_00000000: 1 : 11111111_11111111_11111111: 16,777,216

(1) DBN (DMA Block Count) Bits

Use these bits to specify the number of blocks per line.

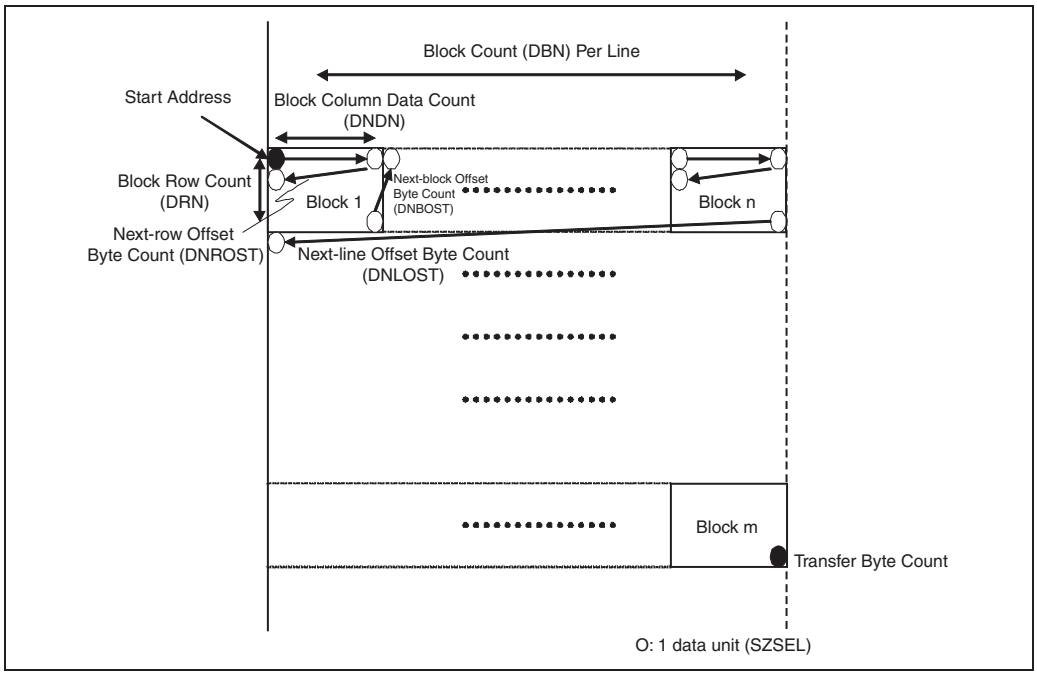
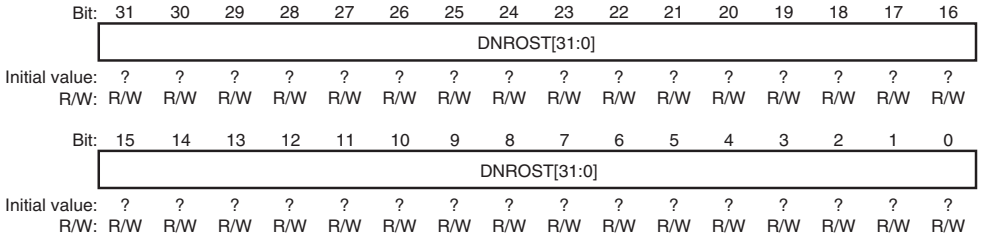


Figure 46.17 2D Block Setup Method

46.4.21 F1DMAC0/1 DMA 2D Next-Row Offset Register n (F1DMAC0/1_DM2DNROSTn)

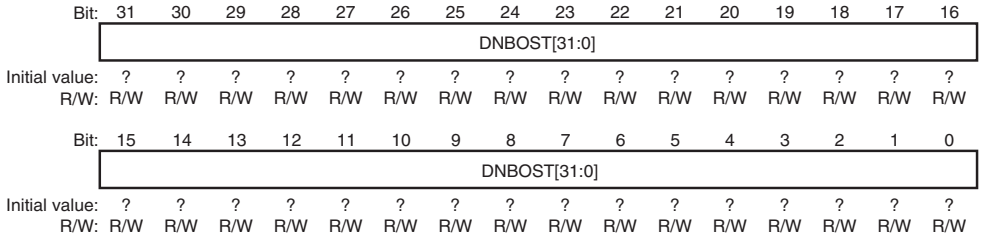


Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DNROST[31:0]	H'???? ????	R/W	DMA2D next-row offset byte count Number of DMA2D next-row offset bytes

(1) DNROST (DMA2D Next-Row Offset Byte Count) Bits

For 2D addressing, use these bits to specify the byte count which will be added to the current source or destination address to calculate the start address of the next row at the end of DMA transfer of one row in one block. The specified byte count should be a two's complement number.

46.4.22 F1DMAC0/1 DMA 2D Block Offset Register n (F1DMAC0/1_DM2DNBOSTn)

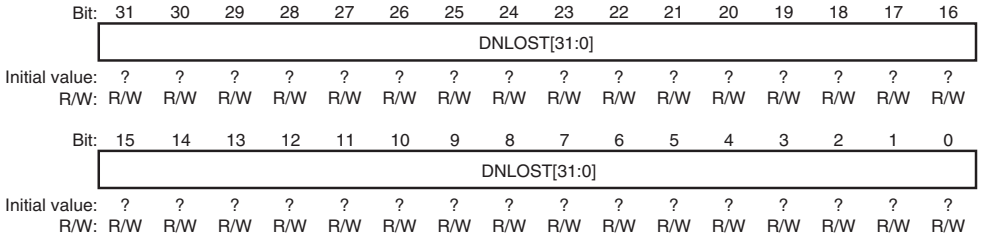


Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DNBOST[31:0]	H'???? ????	R/W	DMA2D next-block offset byte count Number of DMA2D next-block offset bytes

(1) DNBOST (DMA2D Next-Block Offset Byte Count) Bits

For 2D addressing, use these bits to specify the byte count which will be added to the current source or destination address to calculate the start address of the next block at the end of DMA transfer of one block. The specified byte count should be a two's complement number.

46.4.23 F1DMAC0/1 DMA 2D Line Offset Register n (F1DMAC0/1_DM2DNLOSTn)



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DNLOST[31:0]	H'???? ????	R/W	DMA2D next-Line offset data count Number of DMA2D next-line offset bytes

(1) DNLOST (DMA2D Next-Line Offset Byte Count) Bits

For 2D addressing, use these bits to specify the byte count which will be added to the current source or destination address to calculate the start address of the next line at the end of DMA transfer of one line. The specified byte count should be a two’s complement number.

<Reload 2D Addressing Registers>

46.4.24 F1DMAC0/1 DMA Reload 2D Column Setup Register n (F1DMAC0/1_DMR2DCLMn)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRCDN[15:0]															
Initial value:	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	H'????	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 0	DRCDN[15:0]	All ?	R/W	DMA reload block column data count 00000000_00000000: 1 : 11111111_11111111: 65,536

(1) DRCDN (DMA Reload Block Column Data Count) Bits

Use these bits to specify the column data count per block. This count will be reloaded into the DMA 2D column setup register.

Note: Set the bits to the data count selected with the 1-operand transfer data count select bits (OPSEL) or to an integer multiple of that data count. If they are set to something else, proper operation is not guaranteed.

46.4.25 F1DMAC0/1 DMA Reload 2D Row Setup Register n (F1DMAC0/1_DMR2DROWn)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

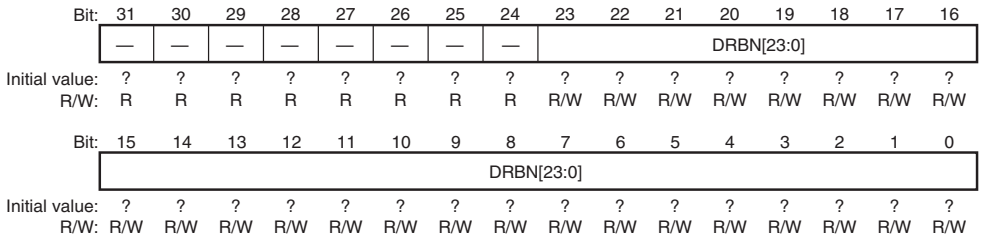
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRRN[15:0]															
Initial value:	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	H'????	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 0	DRRN[15:0]	All ?	R/W	DMA reload block row count 00000000_00000000: 1 : 11111111_11111111: 65,536

(1) DRRN (DMA Reload Block Row Count) Bits

Use these bits to specify the number of rows per block. This count will be reloaded into the DMA 2D row setup register.

46.4.26 F1DMAC0/1 DMA Reload 2D Block Setup Register n (F1DMAC0/1_DMR2DBLKn)



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	H'??	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	DRBN[23:0]	All ?	R/W	DMA reload block count 00000000_00000000_00000000: 1 : 11111111_11111111_111111111: 16,777,216

(1) DRBN (DMA Reload Block Count) Bits

Use these bits to specify the number of blocks per line. This count will be reloaded into the DMA 2D block setup register.

46.4.27 F1DMAC0/1 DMA Reload 2D Next-Row Offset Register n (F1DMAC0/1_DMR2DNROSTn)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DRNROST[31:0]															
Initial value:	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

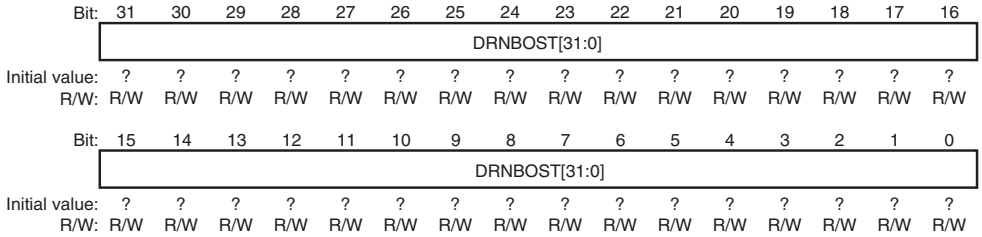
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRNROST[31:0]															
Initial value:	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DRNROST [31:0]	All?	R/W	DMA reload 2D next-row offset byte count

(1) DRNROST (DMA Reload 2D Next-Row Offset Byte Count) Bits

Use these bits to specify the offset byte count which will be reloaded into the DMA 2D next-row offset register. The specified byte count should be a two's complement number.

46.4.28 F1DMAC0/1 DMA Reload 2D Next-Block Offset Register n (F1DMAC0/1_DMR2DNBOSTn)

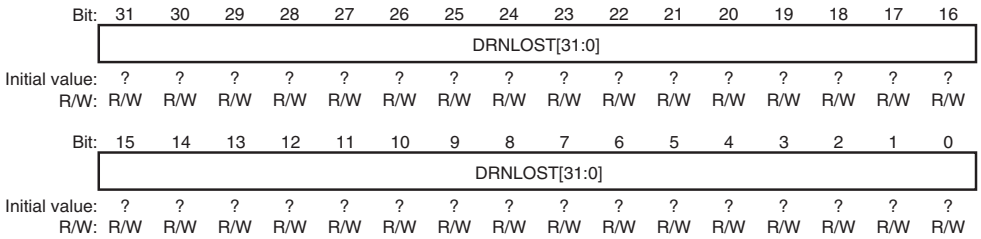


Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DRNBOST [31:0]	All ?	R/W	DMA reload 2D next-block offset byte count Number of DMA reload 2D next-block offset bytes

(1) DRNBOST (DMA 2D Next-Block Offset Byte Count) Bits

Use these bits to specify the offset byte count which will be reloaded into the DMA 2D next-block offset register. The specified byte count should be a two's complement number.

46.4.29 F1DMAC0/1 DMA Reload 2D Line Offset Register n (F1DMAC0/1_DMR2DNLOSTn)



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DRNLOST[31:0]	All ?	R/W	DMA reload 2D next-line offset data count Number of DMA reload 2D next-line offset bytes

(1) DRNLOST (DMA Reload 2D Next-Line Offset Byte Count) Bits

Use these bits to specify the offset byte count which will be reloaded into the DMA 2D next-line offset register. The specified byte count should be a two's complement number.

46.4.30 F1DMAC0/1 Error Flag Register (F1DMAC0/1_DMBERR)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ERST	ERLD
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	—	R	Reserved These bits are always read as 0. The write value should always be 0.
1	ERST	0	R	ST access error detect 0: No error 1: ST command error
0	ERLD	0	R	LD access error detect 0: No error 1: LD command error

(1) ERST (ST Access Error Detect) Bit

If an ST access error is detected on the SHwy bus, this bit is set to 1. It can be cleared to 0 by writing 0 to it.

(2) ERLD (LD Access Error Detect) Bit

If an LD access error is detected on the SHwy bus, this bit is set to 1. It can be cleared to 0 by writing 0 to it.

If ERST = 1 or ERLD = 1, the SHwy error interrupt request (F1DMINT_N) becomes active (set to the "L" level). To clear the interrupt request, clear this bit to 0.

46.4.31 F1DMAC0/1-Data Transfer Status Register (F1DMAC0/1_DMDTSTS)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	F12DSTS	D2F1STS
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	—	R	Reserved These bits are always read as 0. The write value should always be 0.
1	F12DSTS	0	R	Status for data transfer via the F1 bus to the SDRAM 0: There is no request for data transfer via the F1 bus from the F1 read control section to the SDRAM. Also, data transfer is not underway. 1: There is an accepted request for data transfer via the F1 bus from the F1 read control section to the SDRAM. Or else, data transfer is underway.
0	D2F1STS	0	R	Status for data transfer via the F1 bus from the SDRAM 0: There is no request for data transfer via the F1 bus from the SDRAM to the F1 write control section. Also, data transfer is not underway. 1: There is an accepted request for data transfer via the F1 bus from the SDRAM to the F1 write control section. Or else, data transfer is underway.

(1) F12DSTS (Data Transfer Status) Bit for Data Transfer via the F1 Bus to the SDRAM

This bit shows the status of data transfer via the F1 bus to the SDRAM.

(2) D2F1STS (Data Transfer Status) Bit for Data Transfer via the F1 Bus from the SDRAM

This bit shows the status of data transfer via the F1 bus from the SDRAM.

46.4.32 F1DMAC0/1 F1 Bus Access Status Register Data (F1DMAC0/1_DMDTSTS)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	F1RSTS	—	—	F1RFCT[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	F1WSTS	—	—	F1WFCT[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	—	R	Reserved These bits are always read as 0. The write value should always be 0.
21 to 16	F1RSTS	0	R	F1 read access status 0: Operand transfer via the F1 read bus is not underway. 1: Operand transfer via the F1 read bus is underway.
23 to 22	—	—	R	Reserved These bits are always read as 0. The write value should always be 0.
21 to 16	F1RFCT [5:0]	H'00		F1 read bus access request factor number 000000: Software trigger 000001 - 001000: F1-DMA request factor number 001001 and above: Reserved
15 to 9	—	—	R	Reserved These bits are always read as 0. The write value should always be 0.
8	F1WSTS	0		F1 write bus access status 0: Operand transfer via the F1 write bus is not underway. 1: Operand transfer via the F1 write bus is underway.
7 to 6	—	—	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
5 to 0	F1RFCT [5:0]	H'00		F1 write bus access request factor number 000000: Software trigger 000001 to 001000: F1-DMA request factor number 001001 and above: Reserved

46.4.33 DMA Transfer Modes

This processor supports three modes of DMA transfer: cycle stealing, pipeline and fly-by. Any one of these can be selected with the DMA transfer mode select bit (MDSEL) of DMA control register A (F1DMAC0/1_DMCNTAn).

(1) Cycle Stealing Mode

If the DMA transfer mode select bits (MDSEL) are set to 00, the cycle stealing mode is selected.

In this mode, the DMAC idly operates during one or more cycles between the start of read access and that of write access for 1-unit transfer. During this time, the CPU can access the target (source or destination).

(2) Pipeline Mode

If the DMA transfer mode select bits (MDSEL) are set to 01, the pipeline mode is selected.

In this mode, the DMAC continuously accesses the bus (for read/write operation). As a result, the CPU cannot access the target (source or destination) until the end of 1-operand transfer.

(3) Fly-by Mode

If the DMA transfer mode select bits (MDSEL) are set to 10, the fly-by mode is selected.

In this mode, the DMAC performs a single-address transfer by repeatedly starting read or write access. As a result, the CPU cannot access the target (source or destination) until the end of 1-operand transfer.

If the next DMA request is made while one operand is being transferred in fly-by mode, then the 1-operand transfer is followed by DMA transfer without the bus being released if the bus mastership keep function enable bit (BKEEP) for the arbitrated channel is 1.

The non-stop transfer option (DSEL = 11) cannot be selected for DMA fly-by mode.

Note: Pipeline or fly-by transfer across different slave spaces is not allowed. Also, pipeline or fly-by transfer across the SDRAM device channel is not allowed.

46.4.34 DMA Transfers

This processor supports three types of DMA transfer: single-operand, consecutive-operand and non-stop. Any one of these can be selected with the DMA transfer condition select bit (DSEL) of DMA control register A (F1DMAC0/1_DMCNTAn). These types of transfer are described below.

Table 46.15 and figure 46.18 show these types of transfer.

(1) Single-Operand Transfer

If the DMA transfer condition select bits (DSEL) are set to 00, single-operand transfer is performed.

Upon each DMA request, one operand is transferred. The size of each operand is based on the data count selected with the 1-operand transfer data count select bits (OPSEL) of the DMA mode register (F1DMAC0/1_DMMODn).

The 1-operand transfer is repeated. When the byte count reaches 0, the 1-DMA transfer ends.

(2) Consecutive-Operand Transfer

If the DMA transfer condition select bits (DSEL) are set to 01, consecutive-operand transfer is performed.

One DMA request causes operands to be transferred one after another until the 1-DMA transfer ends (i.e., the byte count reaches 0). The size of each operand is based on the data count selected with the 1-operand transfer data count select bit (OPSEL). Each time a 1-operand transfer completes, the channels are arbitrated. The transfer via the current channel continues automatically if no DMA request comes from another higher priority channel.

(3) Non-Stop Transfer

If the DMA transfer condition select bits (DSEL) are set to 11, non-stop transfer is performed.

Upon one DMA request, a non-stop transfer takes place continuously until the 1-DMA transfer ends (i.e., the byte count reaches 0). During this time, the channels are not arbitrated. Any DMA requests from channels with higher priority than the current one are not accepted.

During non-stop transfer, it is impossible to effectively set the 1-operand transfer data count select bits (OPSEL), establish fly-by mode and execute 2D addressing.

Table 46.15 DMA Transfers

DMA Transfer Condition Select Bits (DSEL)	DMA Transfer	Remarks
DSEL = "00"	Single-operand transfer • Upon each DMA request, one operand with a size based on the 1-operand transfer data count (OPSEL) is transferred. • The channels are arbitrated each time a 1-operand transfer completes.	
DSEL = "01"	Consecutive-operand transfer • One DMA request causes operands to be transferred one after another until the byte count reaches 0. • The channels are arbitrated each time a 1-operand transfer completes.	
DSEL = "11"	Non-stop transfer • Upon one DMA request, data are transferred continuously until the byte count reaches 0. • The channels are not arbitrated after the start of transfer.	OPSEL bits are invalid. Fly-by mode is not selectable. 2D addressing is not selectable.

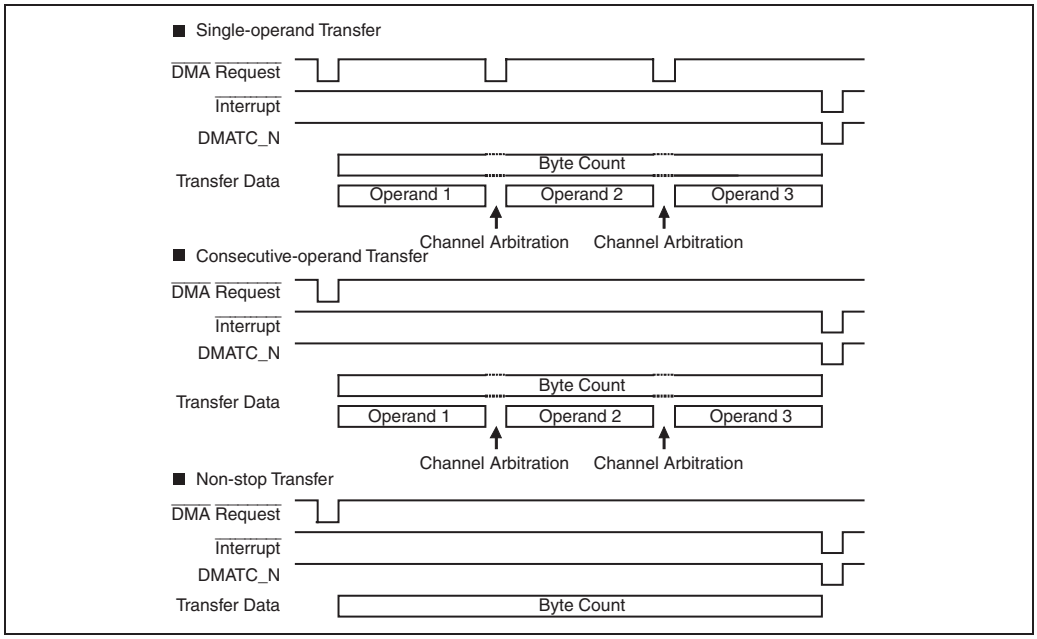


Figure 46.18 DMA Transfers

Table 46.16 shows the combinations of DMA transfer mode and DMA transfer condition.

Table 46.16 Combinations of DMA Transfer Mode and DMA Transfer Condition

		DMA Transfer		
		Single-operand transfer (DSEL="00")	**Consecutive-operand transfer (DSEL="01")**	**Non-stop transfer (DSEL="11")**
Transfer Mode	Cycle stealing mode (MDSEL = "00")	Possible	Possible	Possible
	Pipeline mode (MDSEL = "01")	Possible (*2)	Possible (*2)	Impossible
	Fly-by mode (MDSEL = "10")	Partially possible (*1)	Partially possible (*1)	Impossible

Notes: 1. In fly-by mode, single/consecutive-operand transfer between the module and SDRAM only is possible. In this mode, non-stop transfer is impossible.

2. Pipeline-type transfer between the modules or between the SDRAMs is impossible. If the non-stop transfer option is selected, pipeline-type transfer between the module and SDRAM is impossible.

46.4.35 DMA Startup

(1) Initializing the DMAC

Initialize the registers before setting the DMA transfer enable bit (DEN) to 1. Once a DMA transfer starts, the initial settings cannot be changed.

Below is an example procedure for DMAC initialization.

Setup Procedure

Set these registers:
(1) DMA mode register (F1DMAC0/1_DMMODn)
(2) DMA control register A (F1DMAC0/1_DMCNTAn)
(3) DMA control register B (F1DMAC0/1_DMCNTBn)
(4) DMA current source address register (F1DMAC0/1_DMCSADRn)
(5) DMA reload source address register (F1DMAC0/1_DMRSADRn)

When using the reload function, set these registers:
(6) DMA current destination address register (F1DMAC0/1_DMCDADRn)
(7) DMA reload destination address register (F1DMAC0/1_DMRDADRn)

When using the reload function, set these registers:
(8) DMA current byte count register (F1DMAC0/1_DMCBCTn)
(9) DMA reload byte count register (F1DMAC0/1_DMRBCTn)

When using the reload function, set this register:
(10) DMA interrupt control register (F1DMAC0/1_DMICNT)

When using interrupts, set this register:
(11) DMA common interrupt control register (F1DMAC0/1_DMICNTA)

When using interrupts, set these registers:
(12) DMA transfer enable bit (DEN)
(13) DMA start control register (F1DMAC0/1_DMSCNT)

(2) Starting DMA

DMA transfer via a channel is enabled by setting the DMA transfer enable bit (DEN) of DMA control register B (F1DMAC0/1_DMCNTBn) for that channel to 1 and by setting the DMAC module start bit (DMST) of the DMA start control register (F1DMAC0/1_DMSCNT) to 1.

When DMA transfer requests are generated, the priority levels of the channels are checked. A DMA request from the highest-priority channel is accepted and then a DMA transfer starts.

The presence or absence of a DMA request can be determined using the DMA request bit (DREQ) of DMA control register B (F1DMAC0/1_DMCNTBn).

At the start of DMA transfer after a DMA request is accepted, 1 is written to the channel-associated DMA arbitration status bit (DASTS) of DMA arbitration status register (F1DMAC0/1_DMASTS).

46.4.36 DMA Termination and Interrupts

(1) Terminating a DMA Transfer

When the value of the DMA current byte count register (F1DMAC0/1_DMCBCTn) reaches H'000 0000 (which indicates the completion of transferring all data), the DMA transfer end condition is detected. Then, the 1-DMA transfer completes. The following shows operations which are performed after the detection of the DMA transfer end condition.

- **Detecting the End of DMA Transfer:**
  1 is written to the channel-associated DMA transfer end condition detect bit (DEDET) of the DMA transfer end detect register (F1DMAC0/1_DMEDET).

- **Generating an Interrupt Request:**
  An interrupt request is generated to the interrupt controller according to the settings of the DMA interrupt control register (F1DMAC0/1_DMICNT) and DMA common interrupt control register (F1DMAC0/1_DMICNTA).

- **Output of the DMA End Signal:**
  The DMA end (DMATC_N) signal is output according to the settings of the DMA end signal output control bits (DTCM) of the DMA mode register (F1DMAC0/1_DMMODn).

- **Clearing the DMA Transfer Enable Bit (DEN):**
  If the DMA transfer enable clear bit (ECLR) of DMA control register B (F1DMAC0/1_DMCNTBn) is 1, the DEN bit of DMA control register B (F1DMAC0/1_DMCNTBn) is cleared to 0. Then, a DMA transfer is no longer performed via the relevant channel. If the ECLR bit is 0, the DEN bit is not cleared.

- **Reloading the Source Address:**
  If the DMA source address reload function enable bit (SRLOD) of DMA control register A (F1DMAC0/1_DMCNTAn) is 1, the value of the DMA reload source address register (F1DMAC0/1_DMRSADRn) is reloaded into the DMA current source address register (F1DMAC0/1_DMCSADRn).

- **Reloading the Destination Address:**
  If the DMA destination address reload function enable bit (DRLOD) of DMA control register A (F1DMAC0/1_DMCNTAn) is 1, the value of the DMA reload destination address register (F1DMAC0/1_DMRDADRn) is reloaded into the DMA current destination address register (F1DMAC0/1_DMCDADRn).

- **Reloading the Byte Count:**
  If the DMA byte count reload function enable bit (BRLOD) of DMA control register A (F1DMAC0/1_DMCNTAn) is 1, the value of the DMA reload byte count register (F1DMAC0/1_DMRBCTn) is reloaded into the DMA current byte count register (F1DMAC0/1_DMCBCTn).

Note: If reloading does not take place, set ECLR = 1 to clear the DEN bit.

(2) DMA Interrupt Requests

Interrupt request signals to the interrupt controller include the interrupt request signal (DMINT_N) for each channel and the common interrupt request signal (DMINTA_N) shared by the channels.

Figure 46.19 is a block diagram showing how these signals are generated.

If one of the DMA interrupt control bits (DINTM) of the DMA interrupt control register (F1DMAC0/1_DMICNT) is 1 when a DMA transfer ends, an interrupt request is generated via the channel associated with that bit. In addition, if one of the DMA common interrupt request signal control bits (DINTA) of the DMA common interrupt control register (F1DMAC0/1_DMICNTA) is 1, only the signal which is output over the channel associated with that bit serves as the common interrupt request signal. The generated interrupt request can be cleared by writing 1 to the DMA transfer end condition detect bit (DEDET) for the relevant channel.

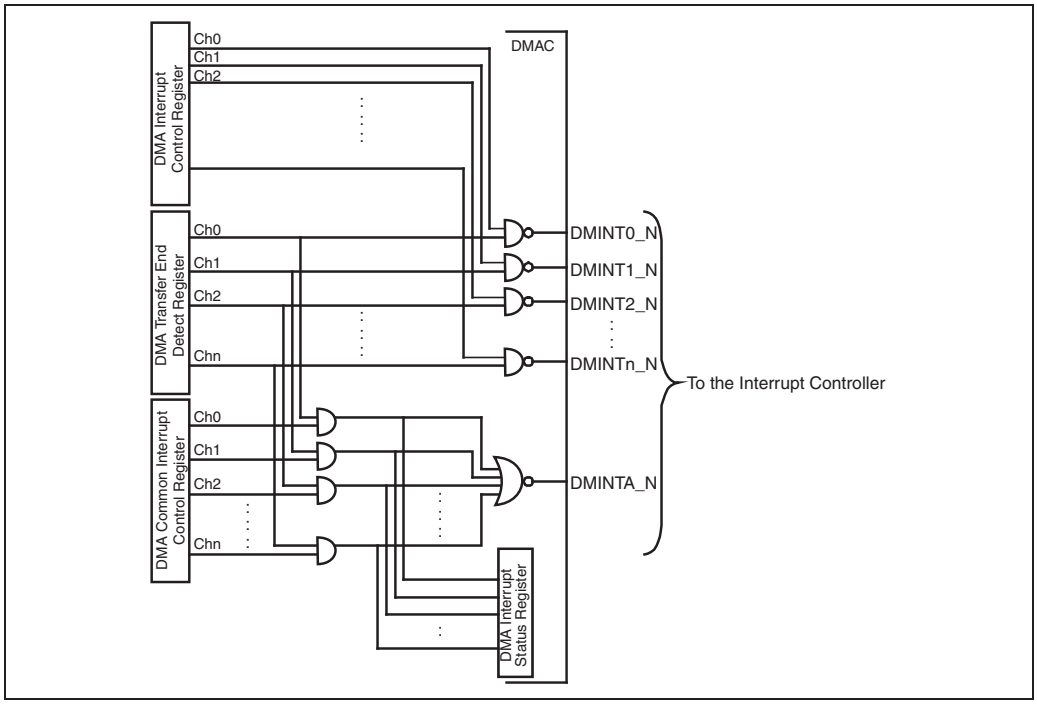


Figure 46.19 Generation of Channel-Associated Interrupt Request Signals and Common Interrupt Request Signal

(3) Output of the DMA End Signal

The DMA end signal (DMATC_N) is output differently depending on the settings of the channel-associated DMA end signal output control bits (DTCM) of the DMA mode register (F1DMAC0/1_DMMODn).

- If DTCM = 00, the DMATC_N signal is fixed at the "H" level and is not output as a valid signal when a DMA transfer ends.
- If DTCM = 01, the DMATC_N signal is output as a valid signal during the read cycle immediately before the end of DMA transfer (i.e., during the read cycle for the last 1-unit transfer).
- If DTCM = 10, the DMATC_N signal is output as a valid signal during the write cycle immediately before the end of DMA transfer (i.e., during the write cycle for the last 1-unit transfer).
- If DTCM = 11, the DMATC_N signal is output as an "L" pulse signal for one clock at the same time a DMA transfer end interrupt occurs.

If a DMA request comes from the on-chip peripheral circuit, the DMATC_N signal is fixed at the "H" level and is not output as a valid signal regardless of the settings of the DTCM bits. This signal should have no effect for fly-by mode. To make it invalid, set DTCM = 00. Figure 46.20 shows the DMA end signal output timing.

Note: For DMA transfer to an external device, the DMATC_N signal might become invalid (H) after the start of the last read or write access to the outside but before the end of access to the external bus.

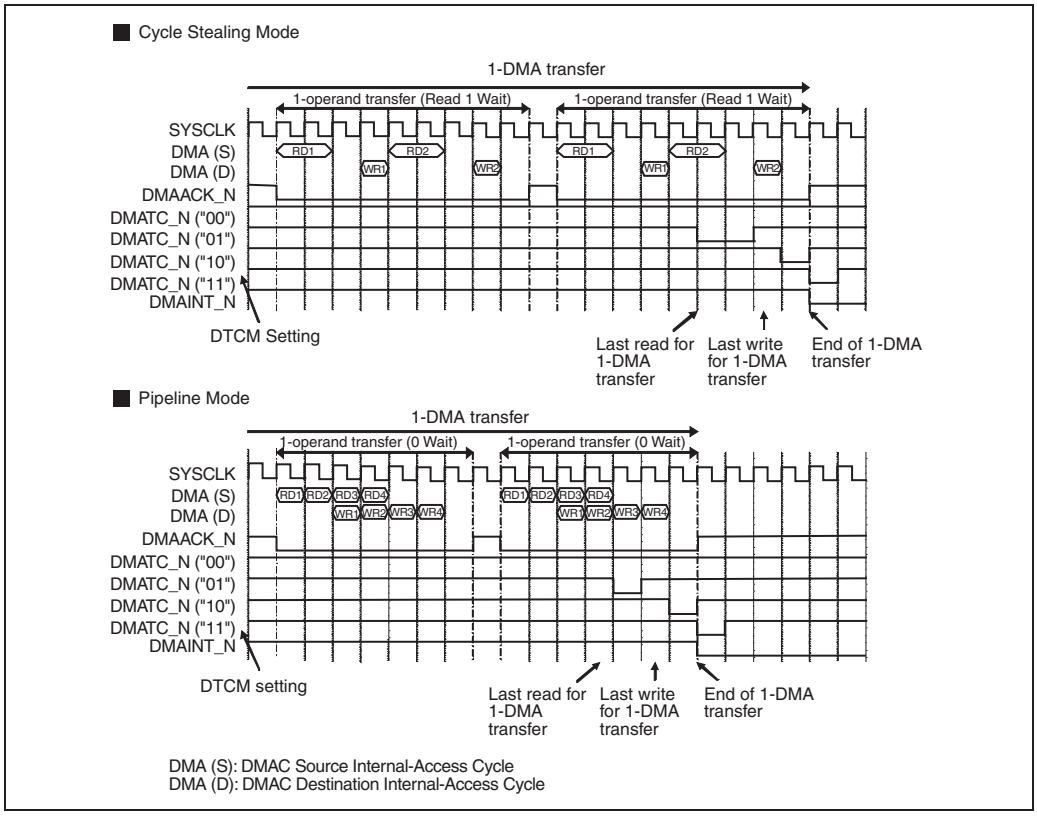


Figure 46.20 DMA End Signal Output Timing

(4) Suspending, Resuming and Aborting a DMA Transfer

(a) Suspending and Resuming a DMA Transfer

The DMAC (all channels) can be temporarily deactivated by clearing the DMAC module start bit (DMST) of the DMA start control register (F1DMAC0/1_DMSCNT) to 0. A channel can also be temporarily deactivated by clearing the DMA transfer enable bit (DEN) of DMA control register B (F1DMAC0/1_DMCNTBn) associated with that channel.

If the DMST or DEN bit is cleared to 0 while one operand is being transferred during single-operand or consecutive-operand transfer, this transfer completes and then no more transfers take place regardless of the transfer mode (cycle stealing, pipeline or fly-by).

If the DMS or DEN bit is cleared to 0 during non-stop transfer, the DMA transfer continues until the byte count reaches 0.

To reactivate the channel, set the DMST and DEN bits to 1. This resumes the DMA transfer operation.

(b) Aborting a DMA Transfer

To abort a channel, write 1 to the DMAC internal status clear bit (DSCLR) of DMA control register B (F1DMAC0/1_DMCNTBn) for that channel while a DMA transfer is temporarily suspended. This initializes the inside of the DMAC and aborts the DMA transfer. In this case, only the transfer status of the DMAC internal circuit is initialized. The registers are not initialized.

46.4.37 DMA Requests

(1) DMA Request Factors

There are a total of eight DMA request factors including the software trigger and DMA request signal inputs. Any one of these factors can be selected with the DMA request factor select bits (DCTG) of channel-associated DMA control register A (F1DMAC0/1_DMCNTAn).

(2) Sense Modes for DMA Requests

If a DMA request signal is selected with the DMA request factor select bits (DCTG = 000001 to 111111), the level sense mode (01/11) or edge sense mode (00/10) can be selected with the input sense mode select bits (STRG) of DMA control register A (F1DMAC0/1_DMCNTAn).*

Note: The level sense mode is only supported in this product.

46.4.38 Determination of DMA Channel Priorities

(1) Channel Priorities

The channels with fixed priorities are shown below. These channels are in descending order of priority from left to right with channel 0 being the highest-priority channel.

Channel 0 > Channel 1 > Channel 2 > … > Channel 6 > Channel 7

(2) Handling Multiplexed DMA Requests

The DMAC determines the channel priorities each time 1-operand transfer completes.

While a lower priority channel performs a data transfer, if a higher priority channel makes a DMA request, the higher priority channel starts a transfer after the end of the transfer involving the lower priority channel.

46.4.39 Reload Function

The reload function is implemented by setting the reload function enable bit of DMA control register A (F1DMAC0/1_DMCNTAn) for each channel and for each transfer parameter (source address, destination address and byte count).

The 2D function is implemented by setting the reload function enable bit (2DRLOD) of DMA control register A (F1DMAC0/1_DMCNTAn) for the six 2D registers (column setup, row setup, block setup, next-row offset, next-block offset and next-line offset registers).

When the DMA transfer end condition is detected, the DMA transfer parameters are reloaded automatically.

(1) Reload Register and Current Register

If not using the reload function, set data in the current register only. If using it, set data in both the reload register and current register.

Do not write to the current register while a 1-operand transfer is underway. If this is done, proper operation is not guaranteed. The reload register can be set during 1-operand transfer. It should be set before the last operand transfer in the DMA transfer process. If it is set during the last operand transfer, reloading might not complete by the end of the DMA transfer.

(2) Consecutive Data Transfer to Dispersed Areas

The reload function is available to enable consecutive data transfer to dispersed areas.

If values are written to the DMA reload source/destination address register (F1DMAC0/1_DMRSADRn F1DMAC0/1_DMRDADRn) or DMA reload byte count register (F1DMAC0/1_DMRBCTn) before the end of transfer, the next transfer parameters can be set without affecting the DMA transfer which is currently executed (via the current register). Therefore, two or more consecutive transfer blocks can be transferred over the same channel even though their destination areas or byte counts are different.

Figure 46.21 shows an example of using the reload function for block transfer to dispersed areas.

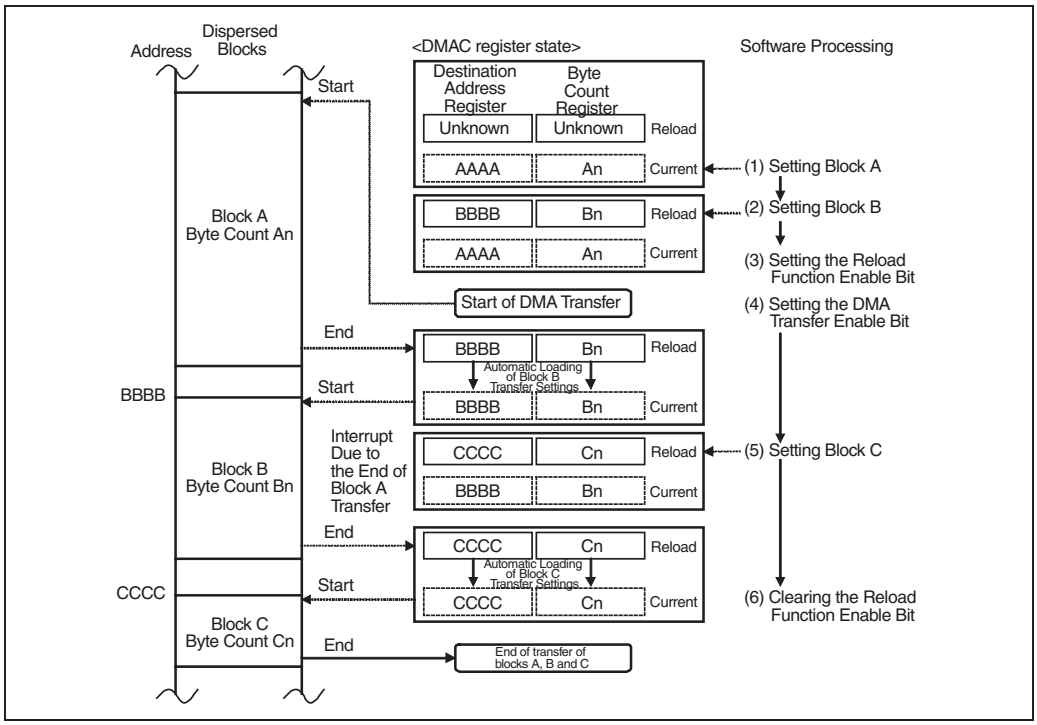


Figure 46.21 Example of Using the Reload Function for Block Transfer to Dispersed Areas

46.4.40 Rotate Function

If the rotate option is selected for addressing mode, the address is incremented. It can be selected for the work source address register or work destination address register. After 1-operand transfer, the address register for which this option has been selected contains the same value as the DMA current source address register (F1DMAC0/1_DMCSADRn) or DMA current destination address register (F1DMAC0/1_DMCDADRn) either of which was set at the start of the DMA transfer.

Figure 46.22 shows an example of using the rotate function for transfer (source: rotate, destination: increment).

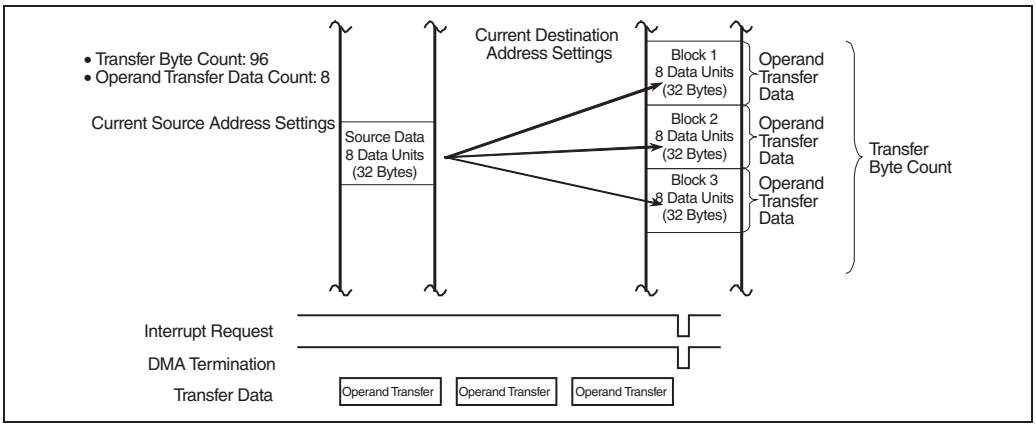


Figure 46.22 Example of Using the Rotate Function for Transfer (Source: Rotate, Destination: Increment)

46.4.41 Precautions in Using DMA

When performing a DMA transfer using the F1DMACs in this processor, observe the following precautions:

- Do not change the data width which is factory fixed at 64 bits (DMMODn.SZSEL = 3).
- Select the fly-by option (DMACNTAn.MDSEL = 2) for DMA transfer mode.
- Select the "H" level sense option (DMACNTAn.MDSEL = 2) for input sense mode.

Section 47 TS Interface (TSIF)

The transport stream interface (TSIF) is a module for receiving the MPEG2 transport stream (TS) used in two-segment broadcasting implemented as part of the digital terrestrial broadcasting services. The TSIF extracts packet data and controls PCR, which are required to decode the system layer of the MPEG2 standard.

47.1 Features

The TSIF has the following features.

- Serial data input
- Support for TS data transfer by DMA auto request
- Acquisition of TS packets
  Filters 67 kinds of PIDs (Packet ID) in total (The PID values of PAT and CAT packets are fixed. For PCR, video, and audio packets, the PID values are predefined.)
  Supports all valid packet receive mode (Null packet is deleted).
  Supports all packet receive mode including Null packet.
  Supports duplicate packet delete mode.
  Capable of specifying the endian type when TS packet data is read
  Supports timestamping TS packet data with timing of obtaining it
- TS data analysis
  Detects random access indicator.
  Detects discontinuity indicator.
  Detects video start code and short header.
- Extraction of PCR information
- Support for system clock generation

[Legend]

MPEG:	Moving picture expert group
TS:	Transport stream
PID:	Packet ID
PAT:	Program association table
CAT:	Conditional access table
PCR:	Program clock reference
ES:	Elementary stream

Figure 47.1 shows a block diagram of the TSIF.

The signals to transfer or control TS data are input as an input signal, and the TS packet data filtered by this module will be output as an output signal.

The serially input TS data is converted into 8-bit parallel data and the header of the TS packet is detected by the TS synchronous detection circuit. The TS filter circuit then determines and filters the PID of the TS packet according to the predefined PID table and stores the TS packet in the buffer for TS packets. Following these processes, only predefined TS packets are stored in the buffer and transferred to memories via a bus interface.

The analysis circuit of a TS header is a block that analyses the header of a TS packet, acquires the header information, and generates a trigger signal sent to other blocks. The ES data search circuit searches the start code and short header of an elementary stream (ES) contained in a TS packet. This result can be used as supplementary data to control the start timing of image decoding through the upper-level software that controls image decoding.

Based on the PCR information extracted from the TS packet, the PCR control unit outputs information needed for system clock control.

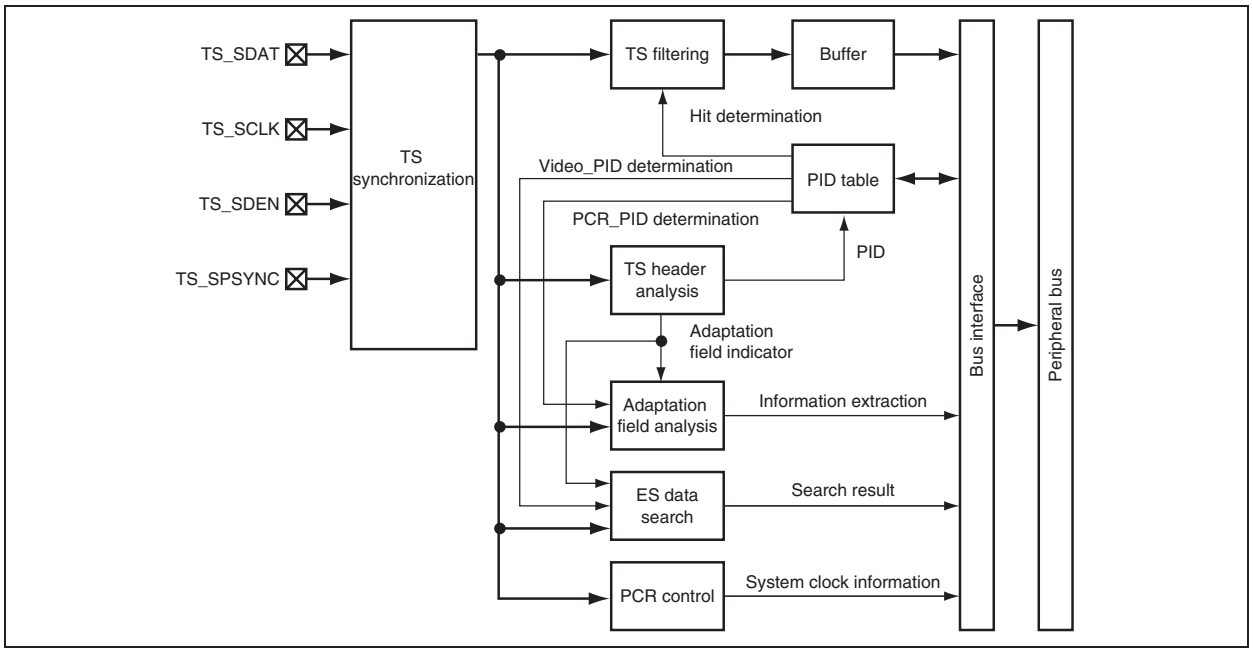


Figure 47.1 TSIF Block Diagram

47.2 Input/Output Pins

Table 47.1 shows the pin configuration.

Table 47.1 Pin Configuration

Pin Name	Function	I/O	Description
TS_SDAT	TS serial data	Input	Serial Input Pin of TS Packet Data
TS_SDAT2			Polarity inversion is enabled by register setting.
TS_SCK	TS serial clock	Input	Serial Input Clock Pin
TS_SCK2			Polarity inversion is enabled by register setting. The initial value is synchronized with the rising edge.
TS_SDEN	TS data enable	Input	Serial Input Enable Signal Pin
TS_SDEN2			Polarity inversion and On/Off setting are enabled by register setting. The initial value is On and enabled after the TS_SDEN signal is driven high.
TS_SPSYNC	TS data synchronization	Input	Byte Boundary Signal Pin
TS_SPSYNC2			Polarity inversion is enabled by register setting. The initial value is set on a byte boundary at the rising edge. If an LSI that does not have the TS_SPSYNC signal is connected, follow the method of handling synchronization signals in the LSI. Signals that have the same waveform of the TS_SDEN signal described in this chapter can be connected to this pin (see figure , Timing of Serial Data Input in , TSIF Module Signal Timing).

47.3 Register Descriptions

Table 47.2 shows the TSIF register configuration. Table 47.3 shows the register states in each operating mode.

Table 47.2 Register Configuration

Register Name	Abbreviation	R/W	Address	Access Size
TSIF0 control register	TS0CTLR	R/W	H'FFE8 0000	32
TSIF0 PID data register	TS0PIDR	R/W	H'FFE8 0004	32
TSIF0 command register	TS0CMDR	R/W	H'FFE8 0008	32
TSIF0 interrupt status register	TS0STR	R/W	H'FFE8 000C	32
TSIF0 TS data register	TS0TSDR	R	H'FFE8 0010	32
TSIF0 buffer clear register	TS0BUFCLRR	R/W	H'FFE8 0014	32
TSIF0 interrupt enable register	TS0INTER	R/W	H'FFE8 0018	32
TSIF0 PSCALE register	TS0PSCALER	R/W	H'FFE8 0020	32
TSIF0 PSCALE_R register	TS0PSCALERR	R/W	H'FFE8 0024	32
TSIF0 PCRADCMODE register	TS0PCRADCMDR	R/W	H'FFE8 0028	32
TSIF0 PCRADC register	TS0PCRADCR	R	H'FFE8 002C	32
TSIF0 TR_PCRADC register	TS0TRPCRADCR	R	H'FFE8 0030	32
TSIF0 D_PCRADC register	TS0DPCRADCR	R	H'FFE8 0034	32
TSIF0 free run counter L	TS0FRCL	R/W	H'FFE8 0040	32
TSIF0 free run counter H	TS0FRCH	R/W	H'FFE8 0044	32
TSIF0 FSCALE register	TS0FSCALER	R/W	H'FFE8 0048	32
TSIF0 FSCALE R register	TS0FSCALERR	R/W	H'FFE8 004C	32
TSIF0 compare match ctrl register	TS0CMCTLR	R/W	H'FFE8 0050	32
TSIF0 compare match counter 0	TS0CMCNT0	R/W	H'FFE8 0054	32
TSIF0 compare match counter 1	TS0CMCNT1	R/W	H'FFE8 005C	32
TSIF0 compare match constant reg 0	TS0CMCOR0	R/W	H'FFE8 0064	32
TSIF0 compare match constant reg 1	TS0CMCOR1	R/W	H'FFE8 006C	32
TSIF0 packet counter	TS0PCNT	R/W	H'FFE8 0074	32
TSIF0 packet counter keep register	TS0PCNTKP	R/W	H'FFE8 0078	32
TSIF0 packet counter push register	TS0PCNTPSH	R/W	H'FFE8 007C	32
TSIF1 control register	TS1CTLR	R/W	H'FFE9 0000	32
TSIF1 PID data register	TS1PIDR	R/W	H'FFE9 0004	32
TSIF1 command register	TS1CMDR	R/W	H'FFE9 0008	32
TSIF1 interrupt status register	TS1STR	R/W	H'FFE9 000C	32
TSIF1 TS data register	TS1TSDR	R	H'FFE9 0010	32
TSIF1 buffer clear register	TS1BUFCLRR	R/W	H'FFE9 0014	32
TSIF1 interrupt enable register	TS1INTER	R/W	H'FFE9 0018	32
TSIF1 PSCALE register	TS1PSCALER	R/W	H'FFE9 0020	32
TSIF1 PSCALE_R register	TS1PSCALERR	R/W	H'FFE9 0024	32
TSIF1 PCRADCMODE register	TS1PCRADCMDR	R/W	H'FFE9 0028	32
TSIF1 PCRADC register	TS1PCRADCR	R	H'FFE9 002C	32
TSIF1 TR_PCRADC register	TS1TRPCRADCR	R	H'FFE9 0030	32

TSIF1 D_PCRADC register	TS1DPCRADCR	R	H'FFE9 0034	32
TSIF1 free run counter L	TS1FRCL	R/W	H'FFE9 0040	32
TSIF1 free run counter H	TS1FRCH	R/W	H'FFE9 0044	32
TSIF1 FSCALE register	TS1FSCALER	R/W	H'FFE9 0048	32
TSIF1 FSCALE R register	TS1FSCALERR	R/W	H'FFE9 004C	32
TSIF1 compare match ctrl register	TS1CMCTLR	R/W	H'FFE9 0050	32
TSIF1 compare match counter 0	TS1CMCNT0	R/W	H'FFE9 0054	32
TSIF1 compare match counter 1	TS1CMCNT1	R/W	H'FFE9 005C	32
TSIF1 compare match constant reg 0	TS1CMCOR0	R/W	H'FFE9 0064	32
TSIF1 compare match constant reg 1	TS1CMCOR1	R/W	H'FFE9 006C	32
TSIF1 packet counter	TS1PCNT	R/W	H'FFE9 0074	32
TSIF1 packet counter keep register	TS1PCNTKP	R/W	H'FFE9 0078	32
TSIF1 packet counter push register	TS1PCNTPSH	R/W	H'FFE9 007C	32

Table 47.3 Register States in Each Operating Mode

Register Abbreviation	Reset*	Module Standby
TSCTLR	Initialized	Retained
TSPIDR	Initialized	Retained
TSCMDR	Initialized	Retained
TSSTR	Initialized	Retained
TSTSDR	Initialized	Retained
TSBUFCLRR	Initialized	Retained
TSINTER	Initialized	Retained
TSPSCALER	Initialized	Retained
TSPSCALERR	Initialized	Retained
TSPCRADCMDR	Initialized	Retained
TSPCRADCR	Initialized	Retained
TSTRPCRADCR	Initialized	Retained
TSDPCRADCR	Initialized	Retained
TSFRCL	Initialized	Retained
TSFRCH	Initialized	Retained
TSFSCALER	Initialized	Retained
TSFSCALERR	Initialized	Retained
TSCMCTLR	Initialized	Retained
TSCMCNT0	Initialized	Retained
TSCMCNT1	Initialized	Retained
TSCMCOR0	Initialized	Retained
TSCMCOR1	Initialized	Retained
TSPCNT	Initialized	Retained
TSPCNTKP	Initialized	Retained
TSPCNTPSH	Initialized	Retained

Note: * Refer the contents of “1-D.2 Range of Reset” of LSI information.

47.3.1 TSIF Control Register (TSCTLR)

TSCTLR is a register for controlling the TSIF.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	PLNGTH	TSDATP	TSCLKP	TSVLDP	–	PSYCP	–	–	SDENE	–	–	BUF4	TFA	DPDMD	DREQMD
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R/W	R	R/W	R	R	R/W	R	R	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EN	PCRMD	FRCMD	FRCSEL	FRCLATCH	FRCADD[1:0]		FRCSTR	FRCPSC[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
30	PLNGTH	0	R/W	Byte Configuration Set of TS Packet Data 0: TS packet is 204-byte configuration. 1: TS packet is 188-byte configuration.
29	TSDATP	0	R/W	Input Polarity Set of TS Packet Data 0: TS data input is positive polarity. 1: TS data input is negative polarity (used after polarity inversion).
28	TSCLKP	0	R/W	Input Polarity Set of TS Clock 0: TS data clock input is positive polarity. (TS data is received at the rising edge.) 1: TS data clock input is negative polarity. (TS data is received at the falling edge.)
27	TSVLDP	0	R/W	Input Polarity Set of TS Packet Data Enable Signal 0: The TS_SDEN signal from the TS decoder is positive polarity (enabled at high). 1: The TS_SDEN signal from the TS decoder is negative polarity (enabled at low).
26	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
25	PSYCP	0	R/W	Input Polarity Set of TS Packet Data Sync Signal 0: TS packet sync signal TS_SPSYNC is positive polarity (sync byte at high). 1: TS packet sync signal TS_SPSYNC is negative polarity (sync byte at low).
24, 23	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
22	SDENE	0	R/W	TS Packet Data Enable Signal Enabled/Disabled 0: The TS_SDEN signal from the TS decoder is enabled. 1: The TS_SDEN signal from the TS decoder is disabled.
21 to 19	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
18	TFA	0	R/W	Software Reset Signal in the TSIF This bit automatically enters the reset state on startup. Release the reset by writing 1. The TSIF internal registers are not initialized with this bit. When a reset is issued, confirm 0 first by reading this bit and release the reset. Note: Set this bit to 1 after TS_SCK of eight cycles or more is input. 0: The TSIF is reset internally (except internal registers). 1: Reset is released.
17	DPDMD	0	R/W	Duplicate Data of Consecutive TS Packets (Duplicate Packets) Delete When the PID of the previous consecutive packet matches continuity_counter, the data is deleted. However, when adaptation_field_control = ×0 (x: don't care), the data is not deleted. 0: Duplicate data valid mode Even when the PID of the consecutive packet and continuity_counter match, the data is not deleted. 1: Duplicate data delete mode When the PID of the previous consecutive packet and continuity_counter match, the data is deleted. Note that this is valid only when adaptation_field_control = ×1 (x: don't care).
16	DREQMD	0	R/W	After TS data transfer of one packet (188 or 192 bytes) by DMAC, selects whether the PEC bit in TSBUFCLRR is set to 1 automatically. 0: DMA interrupt transfer mode After TS data transfer of one packet (188 or 192 bytes), the PEC bit is not set to 1. 1: DMA auto-transfer mode After TS data transfer of one packet (188 or 192 bytes), the PEC bit is set to 1 and the internal buffer is cleared.
15	EN	0	R/W	Specifies the endian type for reading TS packet data from TSTSDR. 0: Big endian 1: Little endian
14	PCRMD	0	R/W	Specifies settings for displaying time indicated by TSPCRADC and TSTRPCRADC 0: Displays the time in 90 kHz units 1: Displays the time in 45 kHz units

Bit	Bit Name	Initial Value	R/W	Description
13	FRCMD	0	R/W	Clock setting of TSFRC 0: Displays the time in 90 kHz units 1: Displays the time in 45 kHz units It is necessary to make it FRCSEL=1 to validate this setting. It is invalid in the case of FRCSEL=0.
12	FRCSEL	0	R/W	The setting of the base clock of TSFRC 0: The divider clock set in FRCPSC is used. 1:The internal pre-scaler(FSCALER) is used.
11	FRCLATCH	0	R/W	Snapshot setting of the internal free-run counter It keeps a snapshot of the internal free-run counter by this setting. The kept value is readable in TSFRCL or TSFRCH. The snapshot is updated by overwriting in FRCLATCH=1. The internal free-run counter keeping is controlled by FRCSTR 0: The snapshot setting of TSFRCL/TSFRCH is off. 1: The snapshot setting of TSFRCL/TSFRCH is on. (The snapshot is updated when It overwrite in “1”).
10-9	FRCADD[1:0]	H’0	R/W	Determines whether to add a TSFRC value (timestamp) with timing of a PID match. 0x0: Does not add a TSFRC value to TSTSDR (TSTSDR reads 188-byte TS packet data) 0x1: Adds a TSFRC value to the 189th to 192nd bytes of TSTSDR (TSTSDR reads 188-byte TS packet data plus the 4-byte TSFRC value) 0x2: Reserved 0x3: Adds a 64bit of TSFRC value to the 189th to 196th bytes of TSTSDR (TSTSDR reads 188-byte TS packet data plus the 8-byte TSFRC value)
8	FRCSTR	0	R/W	Specifies the settings for the TSFRC operation 0: Stops the TSFRC counting operation 1: Performs the TSFRC counting-up operation
7 to 0	FRCPSC7 to FRCPSC0	H'00	R/W	Sets a division clock for TSFRC To set the clock to Bφ divided by n, set FRCPSC to n – 1. Example: To set the clock to 1 MHz (divided by 50) while Bφ is 50 MHz, set FRCPSC[7:0] to 49 (H'31). FRCSEL=0 is necessary to validate this setting. It is invalid in FRCSEL=1.

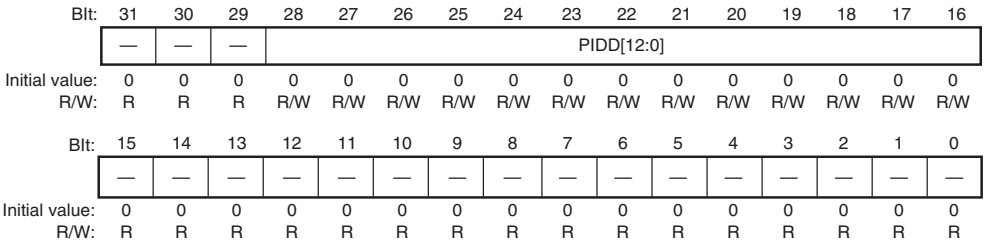
The table below shows the conditions where the TFA bit is reflected in the TSIF.

The TFA bit is reflected in the TSIF depending on the condition of the DREQMD bit with the following timing.

DREQMD Bit	TFA Bit	Reflection Timing
0	0 → 1	Reflected accordingly by register setting
	1 → 0	Reflected accordingly by register setting
1	0 → 1	Reflected accordingly by register setting
	1 → 0	Timing when the PEC bit is automatically set to 1

47.3.2 TSIF PID Data Register (TSPIDR)

TSPIDR is a register used to set the PID value that sets the section table of the PID filter. The settings to PIDD can be reflected by writing to TSCMDR after this register is written to.



Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 16	PIDD12 to PIDD0	H'0000	R/W	Byte Configuration Set of TS Packet Data These bits set the PID value that sets the section table of the PID filter. The setting of this register can be reflected by writing to TSCMDR after setting PIDD.
15 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

47.3.3 TSIF Command Register (TSCMDR)

TSCMDR is a register that sets the value set by TSPIDR to the PID table.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	PT[5]	—	—	ALLPIDMD	PIDMD	TFE	—	PPS	PT[4:0]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28	PT[5]	0	R/W	Selecting a section for setting the PID table (see table 47.4) These bits are valid only when the PIDMD bit and the TFE bit are 0.
27, 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25	ALLPIDMD	0	R/W	PID Filter Mode Set ALLPIDMD PIDMD 0 0: A value set in the PID table is valid (PID filter mode). 0 1: All PIDs other than Null packet (PID = H'1FFF) are valid (all valid packet receive mode). 1 *: All PIDs including Null packet (PID = H'1FFF) are valid (all packet receive mode).
24	PIDMD	0	R/W	
23	TFE	0	R/W	Content of the PID Table Cleared 0: — 1: The content of the PID table is cleared.
22	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
21	PPS	0	R/W	Selecting a section for setting the PID table (see table 43.4) These bits are valid only when the PIDMD bit and the TFE bit are 0.
20 to 16	PT4 to PT0	00000	R/W	
15 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Write a value to be set in the section table of the PID filter for TSPIDR while the PIDMD bit is 0. Then, writing one of the following values in table 43.4 sets a PID value in the specified select section.

In addition to the PID value set above, PIDs for PAT (fixed to H'0000) and CAT (fixed to H'0001) are set.

Table 47.4 Relation among PPS, PT Setting, and PID Values

PPS	PT 5 and PT 0	Select Section
1	xxxxxx	PCR_PID
0	000000	Video
0	000001	Audio
0	000010	PID_1
0	000011	PID_2
0	000100	PID_3
0	000101	PID_4
0	000110	PID_5
0	000111	PID_6
0	001000	PID_7
0	001001	PID_8
0	001010	PID_9
0	001011	PID_10
0	001100	PID_11
0	001101	PID_12
0	001110	PID_13
0	001111	PID_14
0	010000	PID_15
0	010001	PID_16
0	010010	PID_17
0	010011	PID_18
0	010100	PID_19
0	010101	PID_20
0	010110	PID_21
0	010111	PID_22
0	011000	PID_23
0	011001	PID_24
0	011010	PID_25
0	011011	PID_26
0	011100	PID_27
0	011101	PID_28
0	011110	PID_29
0	011111	PID_30
0	100000	PID_31
0	100001	PID_32
0	100010	PID_33
0	100011	PID_34
0	100100	PID_35
0	100101	PID_36
0	100110	PID_37

PPS	PT 5 and PT 0	Select Section
0	100111	PID_38
0	101000	PID_39
0	101001	PID_40
0	101010	PID_41
0	101011	PID_42
0	101100	PID_43
0	101101	PID_44
0	101110	PID_45
0	101111	PID_46
0	110000	PID_47
0	110001	PID_48
0	110010	PID_49
0	110011	PID_50
0	110100	PID_51
0	110101	PID_52
0	110110	PID_53
0	110111	PID_54
0	111000	PID_55
0	111001	PID_56
0	111010	PID_57
0	111011	PID_58
0	111100	PID_59
0	111101	PID_60
0	111110	PID_61
0	111111	PID_62

Note: X: Don't care

47.3.4 TSIF Interrupt Status Register (TSSTR)

TSSTR is a register that indicates the internal status of the TSIF. Each bit in TSSTR can be cleared by writing 0. Bits other than the SYNCF bit are set when a packet is received. Each bit in TSSTR (except for the SYNCF bit) is initialized by the TFA bit in TSCTLR.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	PID[12:0]												
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	CM1MF	CM0MF	–	ADCF	PIDF	STOF	RANDF	DISCF	SYNCF	OFEF	–	VSCF	VSHF	TSIFITF
Initial value:	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 16	PID12 to PID0	H'0000	R/W	These bits indicate the PID of the TS packet input immediately before.
15 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13	CM1MF	0	R/W	COMPARE MATCH1 matching flag The flag to show that “COMPARE MATCH COUNTER” counts down from a value set in TSCMCOR1 and became 0 It can’t write “1” by software 0:The value of TSCMCNT1 doesn’t become h’0000 0000. 1:The value of TSCMCNT1 became h’0000 0000 [A clear condition] It is written 0 to CM1MF
12	CM0MF	0	R/W	COMPARE MATCH0 matching flag The flag to show that “COMPARE MATCH COUNTER” counts down from a value set in TSCMCOR0 and became 0 It can’t write “1” by software 0:The value of TSCMCNT0 doesn’t become h’0000 0000. 1:The value of TSCMCNT0 became h’0000 0000 [A clear condition] It is written 0 to CM0MF
11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10	ADCF	0	R/W	0: — 1: Indicates that PCRADC was updated (the PCR packet was input).
9	PIDF	0	R/W	0: — 1: Indicates that the set PID packet was received in the PID filter mode (ALLPIDMD = 0 and PIDMD = 0).
8	STOF	0	R/W	0: — 1: Indicates that the status of bits was updated (except this bit) by the completion of the next packet reception with the interrupt generated.
7	RANDF	0	R/W	0: — 1: Indicates that random_access_indicator of the TS packet input immediately before is 1.

Bit	Bit Name	Initial Value	R/W	Description
6	DISCF	0	R/W	0: — 1: Indicates that discontinuity_indicator of the PCR packet input immediately before shows the PCR discontinuous state.
5	SYNCF	1	R	Internal Synchronous/Asynchronous Mode State caused by Detection of the TS Packet Sync Signal When the sync signal (H'47) is detected three times consecutively in asynchronous mode, the TSIF enters the synchronous mode. When the sync signal is not detected four times consecutively in synchronous mode, it enters the asynchronous mode. The write value should always be 0. 0: Indicates that the TSIF is in synchronous mode (the TS packet is synchronized). 1: Indicates that the TSIF is in asynchronous mode (the TS packet is not synchronized).
4	OFEF	0	R/W	TSIF Internal Buffer Overflow 0: — 1: Indicates that an overflow error occurred in the internal buffer.
3	—	Undefined	R	Reserved The write value should always be 0.
2	VSCF	0	R/W	Video Packet Start Code Detection Flag 0: — 1: Indicates that the TS packet input immediately before is a video packet and its payload contains a start code (B'0000 0000 0000 0000 0000 0001 xxxx xxxx).
1	VSHF	0	R/W	Video Packet Short Header Detection Flag 0: — 1: Indicates that the TS packet input immediately before is a video packet and its payload contains a short header (B'0000 0000 0000 0000 1000 00xx xxxx xxxx).
0	TSIFINTF	0	R/W	TSIF Transfer Request Flag Indicates that the internal buffer contains one packet (188 bytes) of TS data. 0: — 1: Indicates that the internal buffer contains one packet of TS data.

47.3.5 TSIF TS Data Register (TSTSDR)

TSTSDR is a register to read TS packet data extracted by the set PID. Setting the EN bit in TSCTLR specifies the endian type.

When FRCADD[1:0] in TSCTLR is 2’b01, the TSFRC value (timestamp), which is recorded with the timing of a PID match, is stored in the 189th to 192nd bytes. This value can be used as packet management data.

It is stored in the 189th to 196th bytes at the time of FRCADD[1:0]=2'b11 setting.

After reading one packet (188 bytes) of TS data from this register, the PEC bit in TSBUFCLRR should be set to 1 (unless it is in DMA auto-transfer mode).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TSD[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TSD[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	TSD31 to TSD0	H'0000 0000	R	FRCADD in TSCTLR = 00: • 1 to 188 bytes: TS Packet Data Extracted by the Set PID FRCADD in TSCTLR = 01: • 1 to 188 bytes: TS Packet Data Extracted by the Set PID • 189 to 192 bytes: TSFRC value recorded with timing of a PID match FRCADD in TSCTLR = 11: • 1 to 188 bytes: TS Packet Data Extracted by the Set PID • 189 to 196 bytes: TSFRC(H/L) value recorded with timing of a PID match

- TS packet data format

  [Big endian] EN bit in TSCTLR = 0:

Bit:	31	24	23	16	15	8	7	0
	TSDn[7:0]		TSDn + 1[7:0]		TSDn + 2[7:0]		TSDn + 3[7:0]	

(n = 0, 4, 8, ..., 180, 184)

  [Little endian] EN bit in TSCTLR = 1:

Bit:	31	24	23	16	15	8	7	0
	TSDn + 3[7:0]		TSDn + 2[7:0]		TSDn + 1[7:0]		TSDn[7:0]	

(n = 0, 4, 8, ..., 180, 184)

Note * Since the TSFRC(H/L) value, which is recorded with timing of a PID match and is in the 189th to 192nd(196th) bytes, is a 32-bit counter value, it is always read as longword data.

Bit:	31	0
	TSFRC[31:0] at PID matching	

47.3.6 TSIF Buffer Clear Register (TSBUFCLRR)

TSBUFCLRR is a register that clears the internal buffer of the TSIF after TS packet data is read.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PEC
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	PEC	0	R/W	Internal Buffer Clear This bit should be set to 1 immediately after TS packet data is read. When one packet of TS data is discarded because of a transfer error or such, this bit should be set to 1. This bit is automatically cleared to 0 after it has been set to 1. Do not access this register, while the DREQMD bit in TSCTLR is set to 1, or after TS packet data is read. 0: — 1: Clears the internal buffer after the TS packet is transferred (automatically returns to 0 after 1 is set). When one packet of data transferred is discarded because of a transfer error or such, 1 should always be set.

47.3.7 TSIF Interrupt Enable Register (TSINTER)

TSINTER is a register that controls an interrupt request from the TSIF.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	CM1ME	CM0ME	–	ADCE	PIDE	STOE	RANDE	DISCE	SYNCE	ODEE	–	VSCE	VSHE	TSIFINTE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13	CM1ME	0	R/W	0:- 1: Generates an interrupt when TSCMCNT1 counted down, and a value became h'0000 0000
12	CM0ME	0	R/W	0:- 1: Generates an interrupt when TSCMCNT0 counted down, and a value became h'0000 0000
11	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
10	ADCE	0	R/W	0: — 1: Generates an interrupt when PCRADC is updated (PCR packet is input).
9	PIDE	0	R/W	0: — 1: Generates an interrupt when the set PID packet is received in PID filter mode.
8	STOE	0	R/W	0: — 1: Generates an interrupt when the status is updated (interrupt time is over) by the completion of the next packet reception with the interrupt generated.
7	RANDE	0	R/W	0: — 1: Generates an interrupt when random_access_indicator of the TS packet input immediately before is 1.
6	DISCE	0	R/W	0: — 1: Generates an interrupt when discontinuity_indicator of the PCR packet input immediately before indicates PCR discontinuity.
5	SYNCE	0	R/W	0: — 1: Generates an interrupt when the TSIF is in asynchronous mode.

Bit	Bit Name	Initial Value	R/W	Description
4	OFEE	0	R/W	0: — 1: Generates an interrupt when an overflow error occurs in the internal buffer.
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2	VSCE	0	R/W	0: — 1: Generates an interrupt when the start code of a video packet is detected in the TS packet input immediately before.
1	VSHE	0	R/W	0: — 1: Generates an interrupt when the short header of a video packet is detected in the TS packet input immediately before.
0	TSIFINTE	0	R/W	0: — 1: Generates an interrupt when the internal buffer contains one packet (188 bytes) of TS data.

47.3.8 TSIF PSCALE Register (TSPSCALER)

TSPSCALER is a register that sets counter values 1 and 2 of the internal prescaler. When EXT_MODE = B'0, set the value of the PSCALE2 bit so that the value is equivalent to the value of the PSCALE1 bit plus 1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	PSCALE2[9:0]									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	PSCALE1[9:0]									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25 to 16	PSCALE2 9 to PSCALE2 0	H'000	R/W	These bits set counter value 2 of the internal prescaler.
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 0	PSCALE1 9 to PSCALE1 0	H'000	R/W	These bits set counter value 1 of the internal prescaler.

47.3.9 TSIF PSCALE_R Register (TSPSCALERR)

TSPSCALERR is a register that sets the ratio of counter values 1 and 2 of the internal prescaler.

When EXT_MODE = B'0, set the values of the PSCALE_R1 bit and the PSCALE_R2 bit so that the sum of these two bits is 9.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	PSCALE_R2[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	PSCALE_R1[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 20	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
19 to 16	PSCALE_R2 3 to PSCALE_R2 0	H'0	R/W	These bits set the ratio of counter value 2 of the internal prescaler.
15 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	PSCALE_R1 3 to PSCALE_R1 0	H'0	R/W	These bits set the ratio of counter value 1 of the internal prescaler.

After setting TSPSCALERR while TSPSCALER is H'0000 0000, set TSPSCALER.

When EXT_MODE = B'0, set TSPSCALER and TSPSCALERR so that the following equation is satisfied.

$$\left(\frac{PSCALE_R1 + PSCALE_R2}{PSCALE1 \times PSCALE_R1 + PSCALE2 \times PSCALE_R2}\right) \times B\phi = 90\ kHz$$

$$PSCALE_R1 + PSCALE_R2 = 9$$
$$PSCALE2 = PSCALE1 + 1$$

The examples below show register settings of TSPSCALER and TSPSCALERR corresponding to each operating frequency of the TSIF. When EXT_MODE = B'1, operating frequencies listed in table 47.5 are only supported.

Table 47.5 Setting Example of TSPSCALER and TSPSCALERR Corresponding to Each Operating Frequency

- EXT_MODE = B'0

Operating Frequency [MHz]	PSCALE2	PSCALE1	PSCALE_R2	PSCALE_R1
10.0	H’38	H’37	H’5	H’4
12.0	H’43	H’42	H’3	H’6
12.6	H’46	H’45	H’9	H’0
12.8	H’48	H’47	H’1	H’8
14.4	H’51	H’50	H’0	H’9
16.0	H’59	H’58	H’8	H’1
19.2	H’6B	H’6A	H’6	H’3
20.0	H’70	H’6F	H’1	H’8
27.0	H’97	H’96	H’0	H’9
33.0	H’B8	H’B7	H’3	H’6
48.0	H’10B	H’10A	H’6	H’3
50.0	H’116	H’115	H'7	H’2
54.0	H’12D	H’12C	H’0	H’9
66	H’16F	H’16E	H’6	H’3
83.4	H’1D0	H’1CF	H’3	H’6
100	H’22C	H’22B	H’5	H’4

- EXT_MODE = B'1

Operating Frequency [MHz]	PSCALE2	PSCALE1	PSCALE_R2	PSCALE_R1
13.5	H'000	H'001	H'0	H'1
27.0	H'000	H'002	H'0	H'1
40.5	H'000	H'003	H'0	H'1
54.0	H'000	H'004	H'0	H'1

Note: The operating frequency is a bus clock.

47.3.10 TSIF PCRADC Mode Register (TSPCRADCMDR)

TSPCRADCMDR is a register that sets the PCRADC mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	EXT_MODE	TR_SEL[4:0]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	EXT_MODE	0	R/W	Sets whether PCR_extension is included in the calculation of D_PCRADC. The EXT_MODE bit can be set to 1 only when this block operates at (13.5 × n) MHz (n = 1, 2, 3, 4). 0: PCR_extension is not included in the D_PCRADC calculation. 1: PCR_extension is included in the D_PCRADC calculation.
4	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
3 to 0	TR_SEL3 to TR_SEL0	H'00	R/W	These bits select a trigger signal for PCRADC to be input to the TSIF. Do not set two or more bits to 1. 0000: A trigger signal is not selected. 1000: An interrupt signal from DMAC channel 3 is selected as a trigger. 0100: An interrupt signal from DMAC channel 2 is selected as a trigger. 0010: An interrupt signal from DMAC channel 1 is selected as a trigger. 0001: An interrupt signal from DMAC channel 0 is selected as a trigger. Other than above: Setting prohibited

47.3.11 TSIF PCRADC Register (TSPCRADCR)

TSPCRADCR is a register that indicates the PCR value incremented by the internal clock (indicates time in a unit of 90 kHz).

After a reset is released, inputting a PCR packet starts count-up operation. Then, the counter value is corrected by using the PCR value in the stream each time a PCR packet is input.

This register is also updated in the packet asynchronous state.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	D_PCRADC[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	D_CRADC[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PCRADC31 to PCRADC0	H'0000 0000	R	These bits indicate the PCR value incremented by the internal clock. PCRMD in TSCTLR = 0: these bits indicate time in 90-kHz units PCRMD in TSCTLR = 1: these bits indicate time in 45-kHz units

47.3.12 TSIF TR_PCRADC Register (TSTRPCRADCR)

TSTRPCRADCR indicates the value of PCRADC read by a trigger signal for PCRADC selected by the TR_SEL bit (indicates time in a unit of 90 kHz).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TR_PCRADC[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TR_PCRADC[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	TR_PCRADC31 to TR_PCRADC0	H'0000 0000	R	These bits indicate the PCRADC value read by a trigger signal for PCRADC selected by the TR_SEL bit. PCRMD in TSCTLR = 0: these bits indicate time in 90-kHz units PCRMD in TSCTLR = 1: these bits indicate time in 45-kHz units

47.3.13 TSIF D_PCRADC Register (TSDPCRADCR)

TSDPCRADCR indicates the value of the stream PCR minus PCRADC. After a reset is released and a second packet is input, the value of this register is valid.

When the value of the stream PCR minus PCRADC is greater than 32767 or smaller than –32768, the bits D_PCRADC[31:16] indicate H'8000. (The setting of PCRMD in TSCTLR does not affect D_PCRADC. D_PCRADC[31:16] and D_PCRADC[15:0] indicate a clock difference in a unit of 90 kHz and 27 MHz, respectively.)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	D_PCRADC[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	D_PCRADC[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	D_PCRADC31 to D_PCRADC0	H'0000 0000	R	These bits indicate the value of the stream PCR minus PCRADC.

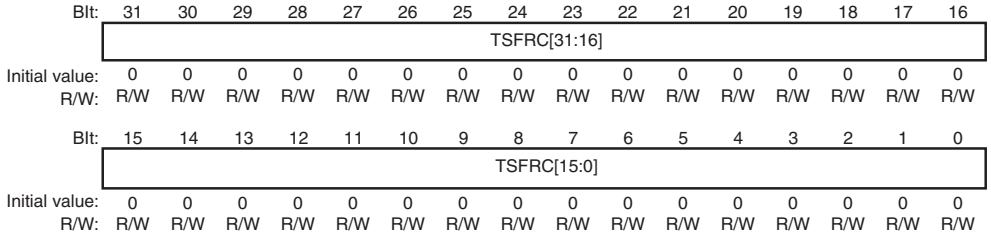
47.3.14 TSIF Free Run Counter (TSFRCL)

TSFRCL is a 32-bit free run counter that counts up with a clock divided by setting FRCPSC[7:0] in TSCTLR or internal pre-scaler.

This counter starts counting up after choose clock in FRCSEL and FRCPSC in TSCTLR is set to 1.

TSFRCL is initialized to H'00000000 by a power-on reset, manual reset, R-standby or U-standby. Setting TFA in TSCTLR to 0 does not initialize this counter.

Setting FRCADD in TSCTLR to 01 stores the TSFRCL value (timestamp), which is recorded with timing of a PID match, in the 189th to 192nd bytes of TSTDR.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	TSFRC31 to TSFRC0	H'0000 0000	R/W	Indicate the value of the free run counter.(lower)

47.3.15 TSIF Free Run Counter (TSFRCH)

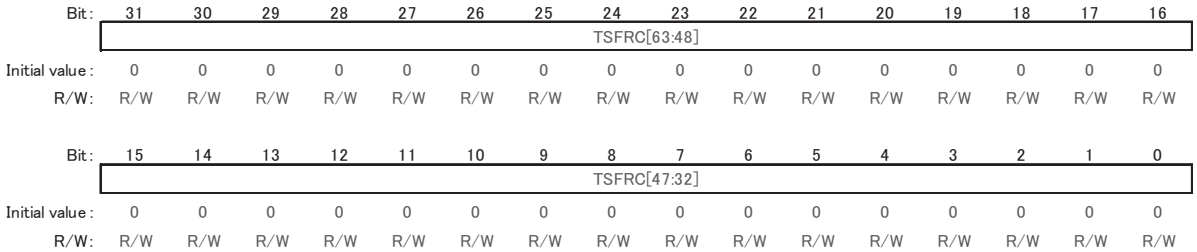
TSFRCH links TSFRCL in free run counter of 32-bit and functions as it of 64-bit.

It is necessary to set 11 of FRCADD in TSCTLR to let it function as free run counter of 64-bit.

This counter starts counting up after choose clock in FRCSEL and FRCPSC in TSCTLR is set to 1.

TSFRCH is initialized to H'00000000 by a power-on reset, manual reset, R-standby or U-standby. Setting TFA in TSCTLR to 0 does not initialize this counter.

Setting FRCADD in TSCTLR to 11 stores the TSFRC(H/L) value (timestamp), which is recorded with timing of a PID match, in the 189th to 196th bytes of TSTDR.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	TSFRC64 to TSFRC32	H'0000 0000	R/W	Indicate the value of the free run counter.(upper)

47.3.16 TSIF FSCALE Register (TSFSCALER)

TSFSCALER is a register that sets counter values 1 and 2 of the internal prescaler used in TSFRC. Set the value of the FSCALE2 bit so that the value is equivalent to the value of the FSCALE1 bit plus 1.

The specifications of the setting follow TSFSCALER.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	FSCALE2[9:0]									
Initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	FSCALE1[9:0]									
Initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25 to16	FSCALE2 9 to FSCALE2 0	H'000	R/W	These bits set counter value 2 of the internal prescaler used in TSFRC.
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 0	FSCALE1 9 to FSCALE1 0	H'000	R/W	These bits set counter value 1 of the internal prescaler used in TSFRC.

47.3.17 TSIF FSCALE_R Register (TSFSCALERR)

TSFSCALERR is a register that sets the ratio of counter values 1 and 2 of the internal prescaler used in TSFRC.

Set the values of the FSCALE_R1 bit and the FSCALE_R2 bit so that the sum of these two bits is 9.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	FSCALE_R2[3:0]			
Initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	FSCALE_R1[3:0]			
Initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 20	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
19 to 16	FSCALE_R2 3 to FSCALE_R2 0	H'0	R/W	These bits set the ratio of counter value 2 of the internal prescaler used TSFRC.
15 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	FSCALE_R1 3 to FSCALE_R1 0	H'0	R/W	These bits set the ratio of counter value 1 of the internal prescaler used TSFRC.

47.3.18 TSIF COMPARE MATCH Control Register (TSCMCTLR)

TSCMCTLR chooses Run/Stop of COMPARE MATCH COUNTER0 and COMPARE MATCH COUNTER1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PIDEX	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	CM1GO	–	–	–	CM0GO
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	PIDEX	0	R/W	This bit choose Use/Not_Use from choice section PID_34 to PID_64. 0: NOT use 1: use
30 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	CM1GO	H'0	R/W	This bit choose Run/Stop COMPARE MATCH COUNTER1(TSCMCNT1). 0: TSCMCNT1 stops a count. 1: TSCMCNT1 starts counting.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	CM0GO	H'0	R/W	This bit choose Run/Stop COMPARE MATCH COUNTER0(TSCMCNT0). 0: TSCMCNT0 stops a count. 1: TSCMCNT0 starts counting.

47.3.19 TSIF COMPARE MATCH COUNTER0 (TSCMCNT0)

TSCMCNT0 is free run counter of 32-bit counting down in clock set in TSCTLR.FRCPSC[7:0] or internal prescaler used in TSFRC.

Countdown is started after setting of CM0GO=1 in TSCMCTLR.

As for TSCMCNT0, it is counted down by a value set by TSCMCOR0, and it is counted down by a value set again by TSCMCOR0 when it became H'0000_0000 if it is CM0GO=1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CMCNT0[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMCNT0[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	CMCNT0 31 to CMCNT0 0	H'0000 0000	R/W	There bits show a value of the COMPARE MATCH COUNTER0.

47.3.20 TSIF COMPARE MATCH COUNTER1 (TSCMCNT1)

TSCMCNT0 is one shot counter of 32-bit counting down in clock set in TSCTLR.FRCPSC[7:0] or internal prescaler used in TSFRC.

Countdown is started after setting of CM1GO=1 in TSCMCTLR.

TSCMCNT1 stops after having become H'0000_0000 by countdown.

It write 0 in CM1GO to run it again, and it is necessary to write 1 afterwards.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CMCNT1[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMCNT1[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	CMCNT1 31 to CMCNT1 0	H'0000 0000	R/W	There bits show a value of the COMPARE MATCH COUNTER1.

47.3.21 TSIF COMPARE MATCH CONSTANT Register0 (TSCMCOR0)

TSCMCOR0 sets a value at the time of a count down start of COMPARE MATCH COUNTER0 (TSCMCNT0).

It loads a value of TSCMCOR0 in TSCMCNT0 after setting of CM0GO=1 in TSCMCTLR.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TSCOR0[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TSCOR0[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	TSCOR0 31 to TSCOR0 0	H'0000 0000	R/W	These bits set a value at the time of the countdown start of the COMPARE MATCH COUNTER0.

47.3.22 TSIF COMPARE MATCH CONSTANT Register1 (TSCMCOR1)

TSCMCOR1 sets a value at the time of a count down start of COMPARE MATCH COUNTER1 (TSCMCNT1).

It loads a value of TSCMCOR1 in TSCMCNT1 after setting of CM1GO=1 in TSCMCTLR.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TSCOR1[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TSCOR1[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	TSCOR1 31 to TSCOR1 0	H'0000 0000	R/W	These bits set a value at the time of the countdown start of the COMPARE MATCH COUNTER1.

47.3.23 TSIF TS PACKET COUNT Register (TSPCNT)

TSPCNT is 32-bit register showing the number of the TS packets begin to read in DMA from TSTSDR.

When it wrote 1 in TSPCNTPSH.PCTPH, TSPCNT is initialized to H'0000_0000.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PCNT[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PCNT[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PCNT 31 to PCNT 0	H'0000 0000	R/W	These bits show a TS packet number read in DMA from TSTSDR. It stop count up with a value of H'FFFF_FFFF.

47.3.24 TSIF TS PACKET COUNT KEEP Register (TSPCNTKP)

TSPCNTKP is 32-bit register.

TSPCNTKP keeps the number of the TS packets which TSPCNT shows when It was written 1 in TSPCNTPSH.PCTPH.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PCNTKP[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PCNTKP[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PCNTKP 31 to PCNTKP 0	H'0000 0000	R/W	When It wrote 1 in TSPCNTPSH.PCTPH, It show a TS packet number read in DMA from TSTSDR.

47.3.25 TSIF TS PACKET COUNT PUSH Register (TSPCNTPSH)

TSPCNTPSH is 32-bit register.

It copy a value of TSPCNT at that time in TSPCNTKP when It write 1 in PCTPH.

When you want to copy it again, clear of the PCTPH is necessary.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	PCTPH
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	PCTPH	0	R/W	

47.4 Operation

47.4.1 TS Data Protocol

The TS packet supported by this LSI consists of 188-byte execution data including the sync byte and 16-byte Reed-Solomon code (parity data) for an error correction, with configuration of 204 bytes in total (figure 47.2). The TSIF supports TS data formats of both 188 bytes (without parity) and 204 bytes (with parity).

The data input pins consist of the following.

- Serial data (TS_SDAT) input
- Serial data clock (TS_SCK) input
- Synchronous (TS_SPSYNC) input
- Enable (TS_SDEN) input

Depending on the specifications of the LSI to be connected, the polarity of these pins can be switched by software (figure 47.3).

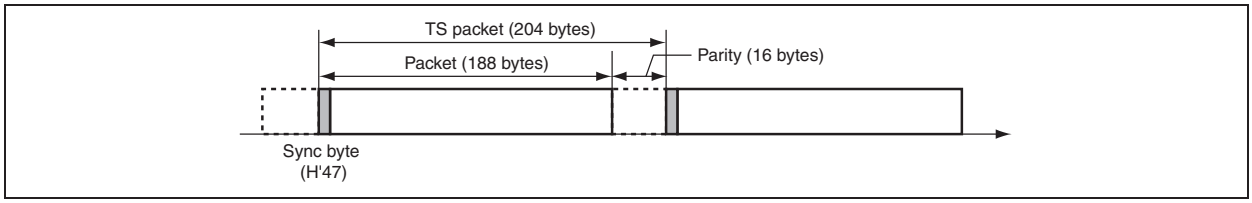


Figure 47.2 MPEG2-TS Packet Configuration

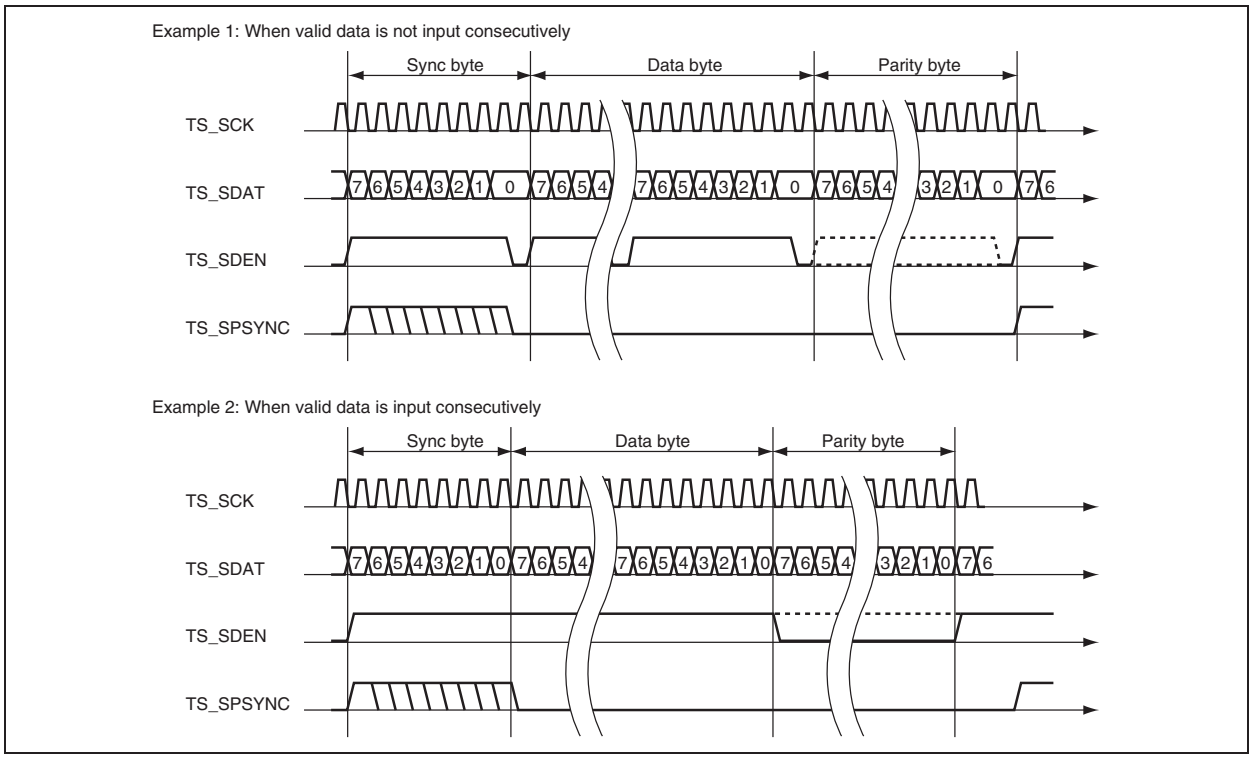


Figure 47.3 Timing of TS Data Serial Input

47.4.2 Synchronous Processing Unit

The function of synchronous processing is to synchronize packets for carrying out the subsequent PID filtering and such.

The TS packet data is constantly sent from a terrestrial station. The receiving terminal starts receiving the data regardless of the timing of the sender. This causes the receiving terminal to receive an incomplete packet. The synchronous processing is essential to identifying the start of TS packet data that are not played from the start and accurately process various data in the packet.

Moreover, as the signal quality of input data may deteriorate according to the transmission status, the TS packet data received via a tuner, OFDM demodulator, and the like may contain errors. The synchronous processing includes protection against such errors.

When the receiving terminal is started up, it searches for the sync byte (H'47). If the sync byte is detected, the receiving terminal checks whether or not the sync byte will appear again after one packet cycle (188 bytes or 204 bytes). If the sync byte appears twice consecutively, synchronization is confirmed. Once synchronized, even when the sync byte does not appear at a fixed position, an error is not generated immediately and the regular processing is continued.

When the sync byte has not appeared 4 times consecutively, the receiving terminal determines that synchronization is lost. Once synchronization is lost, the process for synchronization starts in the same way as when the receiving terminal is started up.

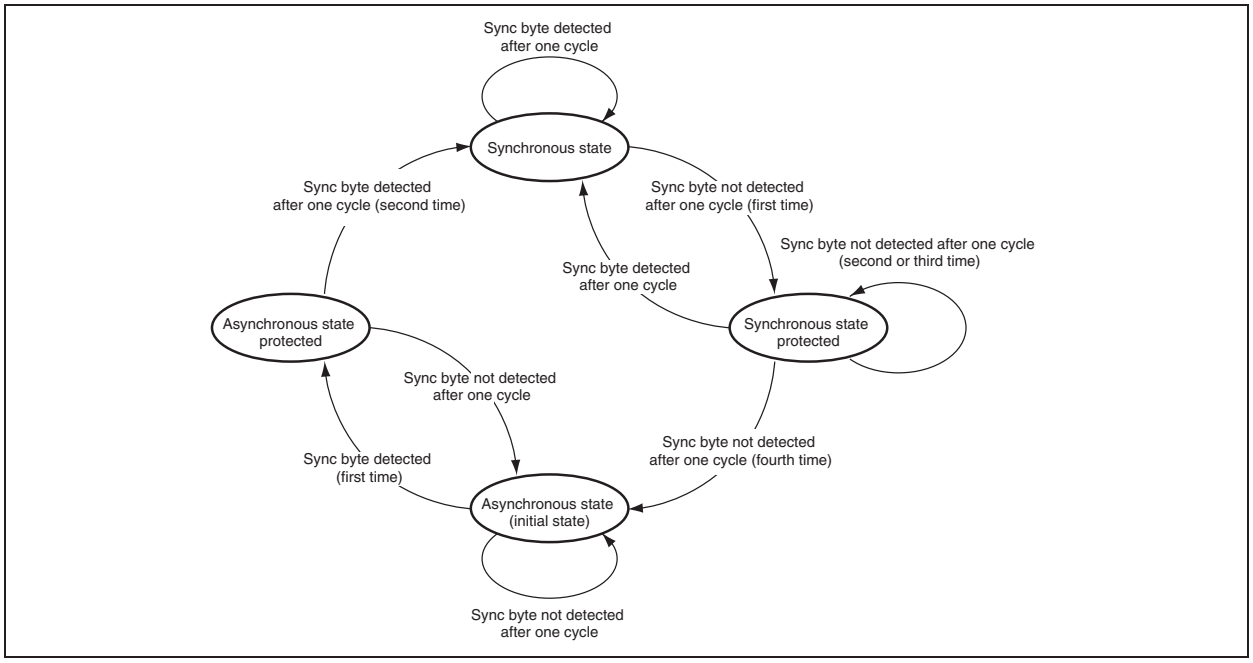


Figure 47.4 Detection State Configuration of Sync Byte

47.4.3 PID Filter Unit

PID filtering checks the PIDs of TS packets and if they match the predefined PID table values, the packets are stored in the buffer.

A total of 67 values can be registered as PID values. However, the values for PAT (H'0000) and CAT (H'0001) are fixed and not changeable. Even though the PID values for the PCR packet, video packet, and audio packet should be specified in the dedicated sections, respectively, another 62 PID values can be specified in any of the sections.

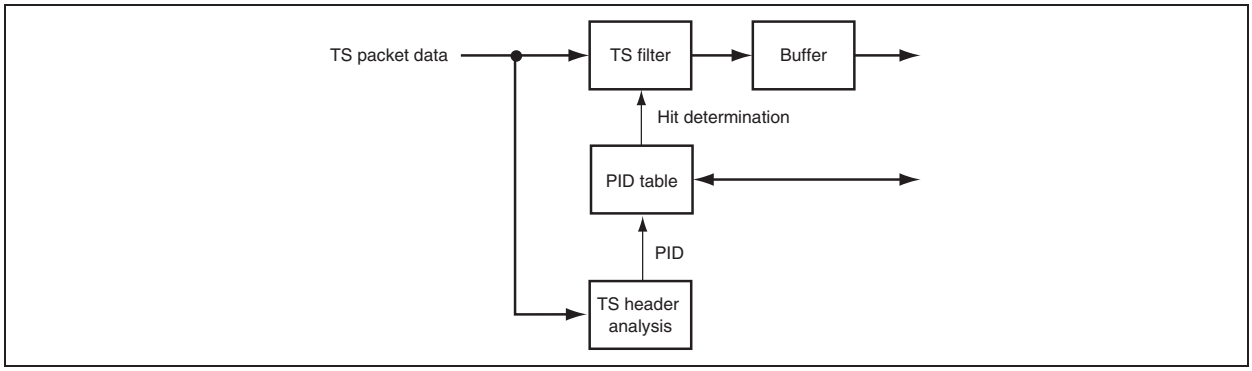


Figure 47.5 Block Diagram of PID Filtering

Table 47.6 PID Table

No.	Section	PID Value (12 Bits)	Description
1	Video	Any setting	Dedicated for video packet
2	Audio	Any setting	Dedicated for audio packet
3	PID1	Any setting	For any packet
4	PID2	Any setting	For any packet
5	PID3	Any setting	For any packet
6	PID4	Any setting	For any packet
7	PID5	Any setting	For any packet
8	PID6	Any setting	For any packet
9	PID7	Any setting	For any packet
10	PID8	Any setting	For any packet
11	PID9	Any setting	For any packet
12	PID10	Any setting	For any packet
13	PID11	Any setting	For any packet
14	PID12	Any setting	For any packet
15	PID13	Any setting	For any packet
16	PID14	Any setting	For any packet
17	PID15	Any setting	For any packet
18	PID16	Any setting	For any packet
19	PID17	Any setting	For any packet
20	PID18	Any setting	For any packet
21	PID19	Any setting	For any packet
22	PID20	Any setting	For any packet
23	PID21	Any setting	For any packet
24	PID22	Any setting	For any packet
25	PID23	Any setting	For any packet
26	PID24	Any setting	For any packet
27	PID25	Any setting	For any packet
28	PID26	Any setting	For any packet
29	PID27	Any setting	For any packet
30	PID28	Any setting	For any packet
31	PID29	Any setting	For any packet
32	PID30	Any setting	For any packet
33	PID31	Any setting	For any packet
34	PID32	Any setting	For any packet
35	PID33	Any setting	For any packet
36	PID34	Any setting	For any packet
37	PID35	Any setting	For any packet
38	PID36	Any setting	For any packet
39	PID37	Any setting	For any packet
40	PID38	Any setting	For any packet
41	PID39	Any setting	For any packet

No.	Section	PID Value (12 Bits)	Description
42	PID40	Any setting	For any packet
43	PID41	Any setting	For any packet
44	PID42	Any setting	For any packet
45	PID43	Any setting	For any packet
46	PID44	Any setting	For any packet
47	PID45	Any setting	For any packet
48	PID46	Any setting	For any packet
49	PID47	Any setting	For any packet
50	PID48	Any setting	For any packet
51	PID49	Any setting	For any packet
52	PID50	Any setting	For any packet
53	PID51	Any setting	For any packet
54	PID52	Any setting	For any packet
55	PID53	Any setting	For any packet
56	PID54	Any setting	For any packet
57	PID55	Any setting	For any packet
58	PID56	Any setting	For any packet
59	PID57	Any setting	For any packet
60	PID58	Any setting	For any packet
61	PID59	Any setting	For any packet
62	PID60	Any setting	For any packet
63	PID61	Any setting	For any packet
64	PID62	Any setting	For any packet
65	PAT	Fixed to H'0000	Dedicated for PAT packet
66	CAT	Fixed to H'0001	Dedicated for CAT packet
67	PCR	Any setting	Dedicated for PCR packet

47.4.4 Bitstream Search Unit

The function of the bitstream search unit is to check the contents of the PCR and video packets to reduce the load of software. The functions listed below are available.

1. PCR discontinuity check

   PCR discontinuity (Discontinuity-indicator) is automatically detected and reflected in the status register. This is to reduce the delay in software processing if a PCR packet is input. PCR is a reference clock sent from a base station (broadcasting station) and may be switched to another PCR because of program changes and so on.
2. PCR_flag detection

   The PCR_flag is detected from the adaptation_field of the TS packet and reflected in the status register.
3. random_access_indicator detection

   The random_access_indicator is detected from the adaptation_field of the TS packet and reflected in the status register.
4. Duplicate packet delete

   The PID and continuity_counter are checked from consecutive TS packets to prevent duplicate TS data from being stored in the buffer.

5. Start code check

   When a start code (H'0000 01xx) is contained in a video stream, it is reflected in the status register. The start code marks the boundary in image data of the MPEG standard and is applied at the start of a sequence, image, and such.

6. Short header check

   When a short header (B'0000 0000 0000 0000 1000 00xx xxxx xxxx) is contained in a video stream, it is reflected in the status register.

These processes are performed in the adaptation field analysis unit and the ES data search unit.

At the time of TS header analysis for PID filtering, the presence of an adaptation field is analyzed. When hit information of a PCR packet or video packet in the PID table is input, the necessary process at each block is initiated.

Each result is reflected in the status register.

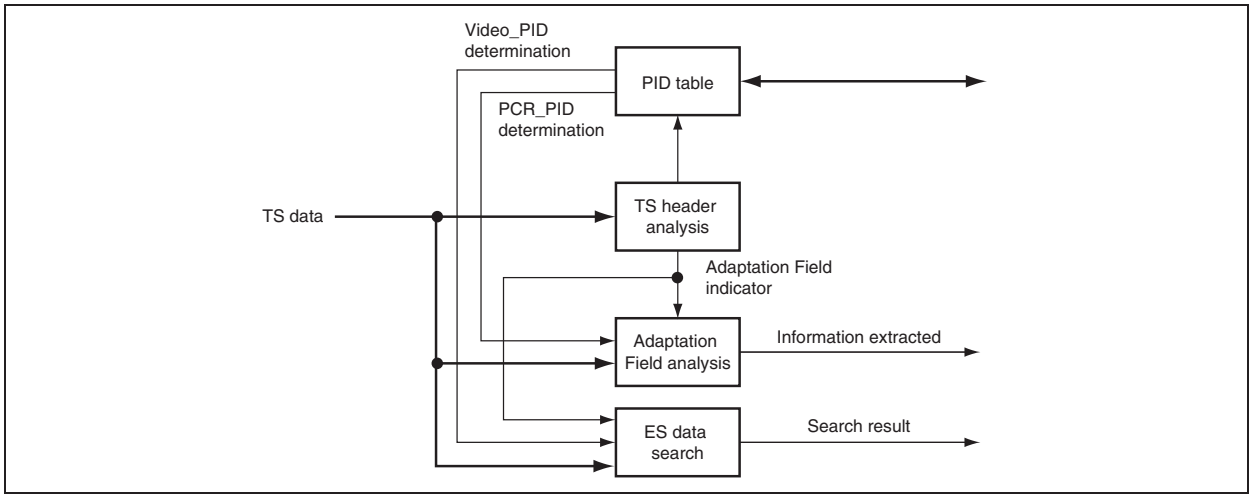


Figure 47.6 Block Diagram of Stream Search Unit

47.4.5 Process Flow

Figure 43.7 shows an outline of the process flow in the TSIF module.

Since the TSIF is in the reset state at power-on, it does not generate any signals until the initialization is completed. A TS packet ID (PID) to be extracted by the TSIF is set in the PID table. After other necessary settings have been completed, software reset is released and the TSIF is started up while a desired interrupt is allowed at the same time. After this, the TSIF waits until the necessary TS packet is extracted.

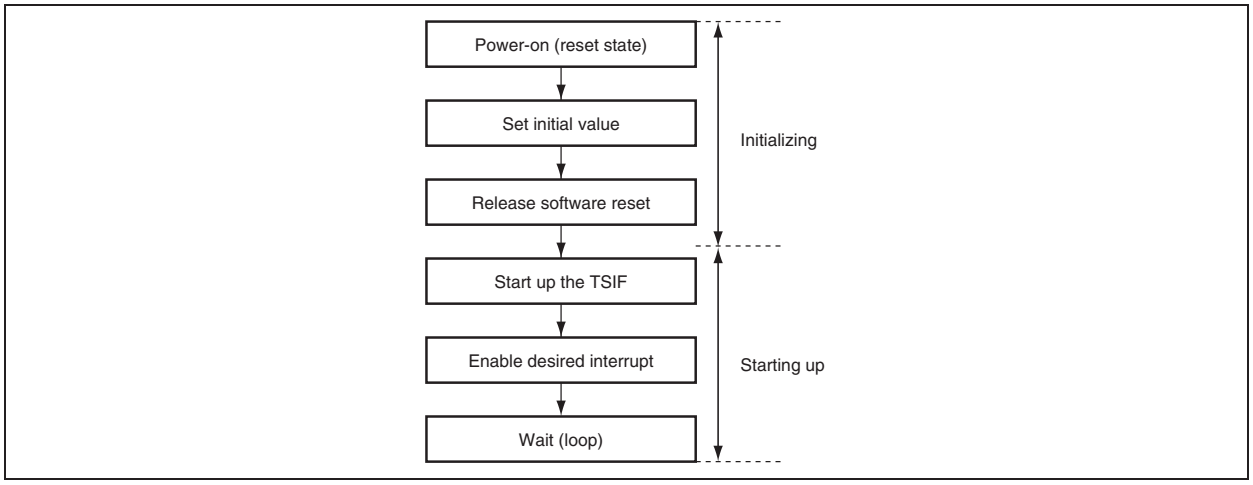


Figure 47.7 TSIF Process Flow

Two types of TS packet transfer are available as described below.

(1) DMA Interrupt Transfer Mode (figure 43.8)

The interrupt routine transfers the packet data stored in the buffer to a queue created in memory. Multiple queues must be created depending on the values of PIDs (e.g., video or audio). When an interrupt is generated, the TSSTR register is read first. If a status error is detected during reading, and the packet data is going to be discarded, the PEC bit in the TSBUFCLRR register should be set. The value of the PID bit in the TSSTR register should then be checked.

For example, if the packet is a video packet, it will be transferred to a video packet queue by DMA and so on. After 188-byte data is transferred or TS data plus TSFRC (192 bytes or 196bytes) is transferred, the PEC bit must be set to clear the internal buffer.

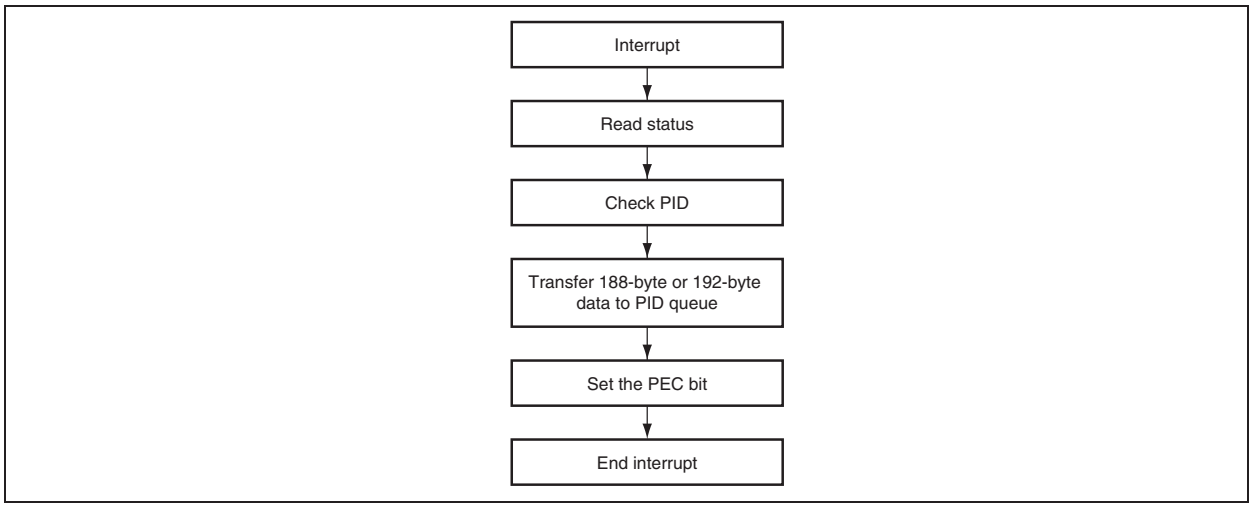


Figure 47.8 TSIF Interrupt Process Flow

(2) DMA Auto-Transfer Mode

To use this mode, the necessary setting should be made in the DMAC block before starting up the TSIF. When a single TS packet (188 bytes) is input or a single TS packet plus TSFRC (192 bytes or 196bytes) is input, the TSIF automatically issues a transfer request signal to the DMA and starts DMA transfer. Using this mode reduces the frequency of interrupts.

Section 48 High-Definition Multimedia Interface (HDMI)

This LSI has HDMI transmitter IP which is compliant with HDMI 1.3a specification.

48.1 Features

- HDMI version 1.3a, HDCP version 1.2 and DVI version 1.0 compliant transmitter
- Internal NV memory for HDCP Key
- Supports DTV from 480i to 1080i/60fps(or 1080p/30fps) HD resolution
- Programmable 2-way color space converter
- Compliant with EIA/CEA-861D
- Gamut metadata transmission
- Supports RGB, YCbCr digital video input (24bit RGB 888 / 24bit YCbCr 4:2:2) from LCDC(*1)
- Supports standard SPDIF input from FSI2(*2) for stereo or compressed audio up to 192KHz
- Programmable PLL characteristics, channel delay and transmitter pre-emphasis rate

Note: *1 : Please refer to section 40 “LCDC”.
*2 : Please refer to section 51 “FSI2/FMSI”.

48.2 Block Diagram

Figure 48.1 shows a block diagram of the HDMI transmitter.

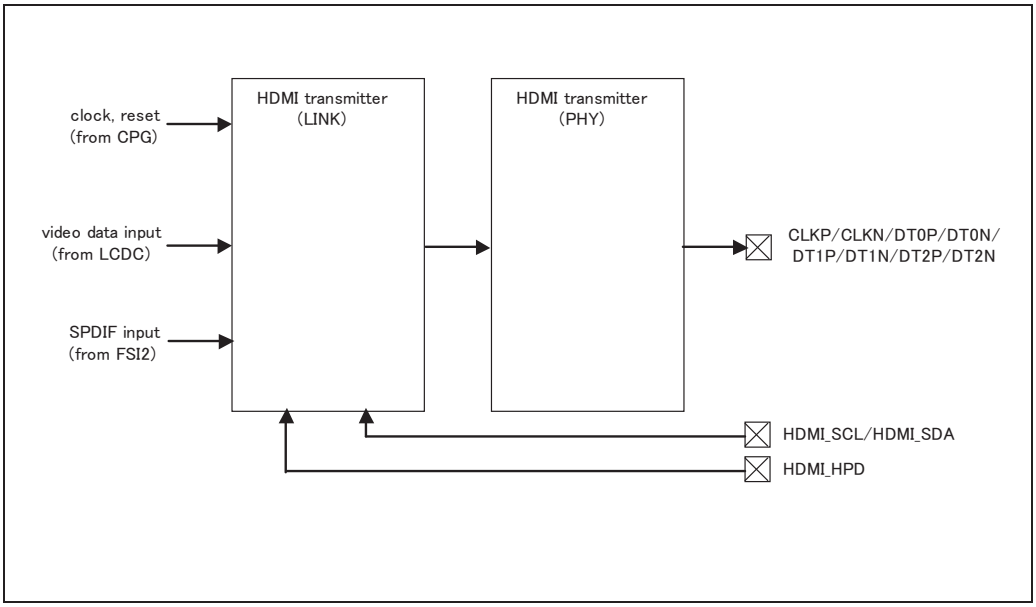


Figure 48.1 Block Diagram

48.3 Pin Configuration

Table 48.1 lists the pins of the HDMI transmitter.

Table 48.1 Pin List

Pin Name	Function	I/O	Description
TMDS_CLKP	Differential pin (plus) for Clock	Output	Differential pixel clock (plus) for HDMI cable interface signal TMDS_CLKP
TMDS_CLKN	Differential pin (minus) for Clock	Output	Differential pixel clock (minus) for HDMI cable interface signal TMDS_CLKN
TMDS_DT0P	Differential pin (plus) for Data0	Output	Differential serial data (plus) for HDMI cable interface signal TMDS_DT0P
TMDS_DT0N	Differential pin (minus) for Data0	Output	Differential serial data (minus) for HDMI cable interface signal TMDS_DT0N
TMDS_DT1P	Differential pin (plus) for Data1	Output	Differential serial data (plus) for HDMI cable interface signal TMDS_DT1P
TMDS_DT1N	Differential pin (minus) for Data1	Output	Differential serial data (minus) for HDMI cable interface signal TMDS_DT1N
TMDS_DT2P	Differential pin (plus) for Data2	Output	Differential serial data (plus) for HDMI cable interface signal TMDS_DT2P
TMDS_DT2N	Differential pin (minus) for Data2	Output	Differential serial data (minus) for HDMI cable interface signal TMDS_DT2N
TMDS_REXT	External Register	—	External Register (470 ohms to 2.5V)
HDMI_SCL	DDC signal	Inout	SCL signal for DDC line
HDMI_SDA	DDC signal	Inout	SDA signal for DDC line
HDMI_HPD	Hot Plug Detect	Input	Hot Plug Detect Input

Section 49 Consumer Electronics Control (CEC) Function

This LSI has control circuit for CEC signal which is specified by HDMI specification.

49.1 Features

- Clock source : RCLK(32.768KHz) is used for basic behavior clock.
- Data format
  - start bit : 1bit
  - data bit : 8bit
  - EOM bit : 1bit
  - ACK bit : 1bit
- Interrupt

  Transmission interrupt
  - 8 bit data transmission completion
  - 10 bit data transmission completion

  Transmission error interrupt
  - Arbitration Lost Detection
  - NACK reception (ACK reception for Broadcast transfer)

  Reception interrupt
  - 8 bit data reception completion
  - 10 bit data reception completion

  Reception error interrupt
  - Unacceptable signal reception
- Error detection

  Arbitration lost : During transmission, in either status bellow, arbitration lost is detected
  - At the changing CEC pins “Hi-Z” to “L” output, CEC pins is already “L” level.
  - At the changing CEC pins “L” output to “Hi-Z”, CEC pins is “L” level over acceptable range.

  Transmission error : CCBTA bit of CCBT2 register is matched with CTNACK bit of CECC2 register

  Reception acceptable range error : “L” or “H” period of reception data is out of acceptable range

- Function
  Digital filter : enable / disable can be selected
  Transmission stop condition: ACK / NACK can be selected
  Arbitration lost detection condition : either of following condition can be selected
    - During sending start bit and initiator address
    - During sending start bit and all of the data bit
- Transmission rising edge timing : can be selected from 8 phase
- Transmission falling edge timing : can be selected from 4 phase
- Receive data timing : detection timing can be selected from either of following
    - Detect only falling edge
    - Detect both rising and falling edge
- ACK output as reception : either of following can be selected
    - Program insertion : assigned by CCRBAO bit of CCRB2 register
    - Hardware insertion : output ACK in the case destination address is matched,
      output NACK in the case destination address is unmatched
- Acceptable range of start bit : +/-200us or +/-300us
- Acceptable range of data bit : either of following can be selected
    - From falling edge to rising edge +/-200us, from rising edge to falling edge +/- 350us
    - From falling edge to rising edge +/-300us, from rising edge to falling edge +/- 500us
- “L” pulse output, as reception error occurrence: output “L” pulse or not can be selected
- Waiting control of error “L” pulse output : either of following can be selected
    - In the case input CEC level is low as error occurrence, output “L” pulse synchronized with input CEC rising.
    - Output “L” pulse , regardless of input CEC level.

49.2 Block Diagram

Figure 49-1 shows a block diagram of CEC function.

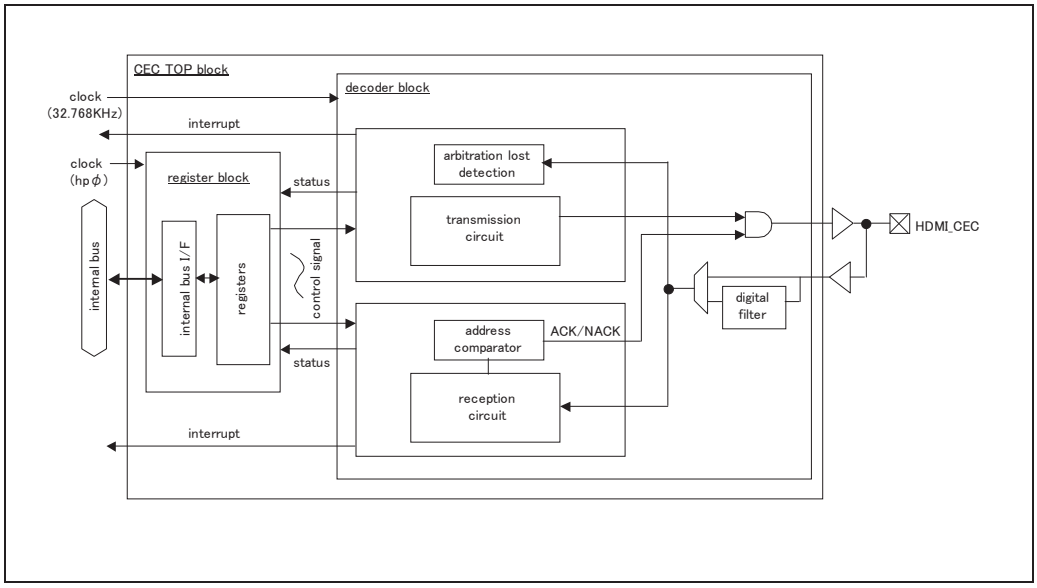


Figure 49-1 Block Diagram

49.3 Pin Configuration

Table 49.1 lists the pins of the CEC function.

Table 49-1 Pin List

Pin Name	Function	I/O	Description
HDMI_CEC	CEC	Inout	CEC control signal

49.4 Register Descriptions

Table 49-2 shows the CEC register configuration. Table 49-3 shows the register states in each operation mode.

Table 49-2 Register Configuration

Register	Abbreviation	R/W	Address	Access Size
CEC function control register 1	CECC1	R/W	H'E6BF 0000	8
CEC function control register 2	CECC2	R/W	H'E6BF 0001	8
CEC function control register 3	CECC3	R/W	H'E6BF 0002	8
CEC function control register 4	CECC4	R/W	H'E6BF 0003	8
CEC flag register	CECFLG	R/W	H'E6BF 0004	8
CEC interrupt factor select register	CISEL	R/W	H'E6BF 0005	8
CEC transmission buffer register 1	CCTB1	R/W	H'E6BF 0006	8
CEC transmission buffer register 2	CCTB2	R/W	H'E6BF 0007	8
CEC reception buffer register 1	CCRB1	R/W	H'E6BF 0008	8
CEC reception buffer register 2	CCRB2	R/W	H'E6BF 0009	8
CEC reception follower address register 1	CRADR1	R/W	H'E6BF 000A	8
CEC reception follower address register 2	CRADR2	R/W	H'E6BF 000B	8
CEC interrupt flag register	CINTR	R/W	H'E6BF 001C	8
CEC interrupt flag clear register	CINTCLR	R/W	H'E6BF 001D	8
CEC interrupt mode select register	CINTSEL	R/W	H'E6BF 001E	8

Table 49-3 Register States in Each Operation Mode

Register Abbreviation	Power-On Reset	System Reset	A3SP Area Power Cutoff
CECC1	Initialized	Initialized	Initialized
CECC2	Initialized	Initialized	Initialized
CECC3	Initialized	Initialized	Initialized
CECC4	Initialized	Initialized	Initialized
CECFLG	Initialized	Initialized	Initialized
CISEL	Initialized	Initialized	Initialized
CCTB1	Initialized	Initialized	Initialized
CCTB2	Initialized	Initialized	Initialized
CCRB1	Initialized	Initialized	Initialized
CCRB2	Initialized	Initialized	Initialized
CRADR1	Initialized	Initialized	Initialized
CRADR2	Initialized	Initialized	Initialized
CINTR	Initialized	Initialized	Initialized
CINTCLR	Initialized	Initialized	Initialized
CINTSEL	Initialized	Initialized	Initialized

49.4.1 CEC function control register 1 (CECC1)

CECC1

bit:	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	CECEN
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 1	–	All 0	R	Reserved This bit is always read as 0. The write value should always be 0.
0	CECEN	0	R/W	CEC function enable bit 0: CEC function disable 1: CEC function enable The CEC circuit is reset by setting CECEN "0".

49.4.2 CEC function control register 2 (CECC2)

CECC2

bit:	7	6	5	4	3	2	1	0
	CDATRNG	CSTRRNG	CFIL	CTABTS	CRACK	CTACKEN	CTNACK	CRRNG
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	CDATRNG	0	R/W	Data bit acceptable range specification bit 0: The period from falling edge to rising edge is +/- 200us The period from rising edge to falling edge is +/- 350us 1: The period from falling edge to rising edge is +/- 300us The period from rising edge to falling edge is +/- 500us
6	CSTRRNG	0	R/W	Start bit acceptable range specification bit 0: +/- 200us 1: +/- 300us

Bit	Bit Name	Initial Value	R/W	Description
5	CFIL	0	R/W	Digital filter enable bit 0: Digital filter disable 1: Digital filter enable
4	CTABTS	0	R/W	Arbitration lost detect condition select bit 0: During transmission of start bit and initiator address 1: During transmission of start bit and all of the data bit This bit selects the range of the arbitration lost detection at CEC rising edge. Except for CEC rising edge, the arbitration lost is detected regardless of this bit.
3	CRACK	0	R/W	Reception ACK output mode select bit 0: Program insertion 1: Hardware insertion When this bit is set to “0”, Output CCRBAO bit level in CCRB2 register as the reception ACK data. When this bit is set to “1”, if the received destination address is matched with the address selected by CRADR1 and CRADR2 registers, then output the ACK. And if the received destination address is not matched with the address selected by CRADR1 and CRADR2 registers, then output the NACK.
2	CTACKEN	0	R/W	Transmission NACK(ACK) stop control bit 0: Continue transmission regardless of NACK/ACK 1: Stop transmission by NACK/ACK reception When this bit is set to “1”, please select the stop condition by CTNACK bit.
1	CTNACK	0	R/W	Transmission NACK(ACK) stop condition select bit 0: Stop by ACK 1: Stop by NACK This bit is valid when CTACKEN bit is set to 1.
0	CRRNG	0	R/W	Reception edge detection select bit 0: Detect only falling edge 1: Detect rising and falling edge

49.4.3 CEC function control register 3 (CECC3)

CECC3

bit:	7	6	5	4	3	2	1	0
	–	–	–	–	CEOMI	CREGCLR	CRXDEN	CTXDEN
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	–	All 0	R	Reserved This bit is always read as 0. The write value should always be 0.
3	CEOMI	0	R/W	Disable EOM bit 0: EOM enable 1: EOM disable This bit select that stop or continue the transmission/reception when the EOM is “1”. Table 49-4 shows the behavior in the case EOM is “1”.
2	CREGCLR	0	R/W	CREGFLG clear bit When this bit is set to “1”, CREGFLG bit of CECC4 register is cleared to “0”. Before setting this bit to “1” next time, set this bit “0”.
1	CRXDEN	0	R/W	Enable reception register 0: reception stopped 1: reception permitted After 1 RCLK cycle of setting this bit, the reception is stopped or permitted.
0	CTXDEN	0	R/W	Enable transmission register 0: transmission stopped 1: transmission permitted After 1 RCLK cycle of setting this bit, the transmission is stopped or permitted.

Table 49-4 Behavior in the case EOM is "1"

CEOMI bit	Behavior in the case EOM is "1"	
	Reception	Transmission
0	Neglect the received data after the receiving EOM "1". (Wait for START bit)	Stop to transmit data after the transmitting EOM "1".
1	Reply ACK or NACK to the received data even after receiving EOM "1".	Transmit data even after the transmitting EOM "1".

When the CEOMI bit is "1", to stop the transmission, please set CTXDEN bit of CECC3 register.

49.4.4 CEC function control register 4 (CECC4)

CECC4

bit:	7	6	5	4	3	2	1	0
	CABTWEN	CREGFLG	CFALL[1:0]		CABTEN	CRISE[2:0]		
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	CABTWEN	0	R/W	Error "L" pulse output wait control bit 0: Output "L" pulse regardless of the CEC signal 1: Output "L" pulse at rising edge of the CEC signal This bit is valid when CABTEN bit is set to "1". In the case this bit is "1", when a reception error is detected during CEC input level is "L", error "L" pulse is output from next CEC rising edge. But when CEC rising edge is not detected within 3.6ms after an error occurrence, regarding the other devices output the error "L" pulse, this device doesn't output the error "L" pulse.
6	CREGFLG	0	R	CEC reception edge detection flag 0: The CEC "L" is not detected 1: The CEC "L" is detected When the CEC "L" is detected, this bit is set to "1". When CREGCLR bit of CECC3 register is set to "1", this bit is cleared to "0".
5, 4	CFALL[1:0]	00	R/W	CEC fall timing select bit Please refer Table 49-5.

Bit	Bit Name	Initial Value	R/W	Description
3	CABTEN	0	R/W	Error “L” pulse output enable bit 0: disable 1: enable When this bit is set to “1”, the received data bit is over the acceptable reception range, output 3.6ms “L” pulse. The “L” pulse output timing is selectable by CABTWEN bit.
2 to 0	CRISE[2:0]	000	R/W	CEC rise timing select bit Please refer Table 49-6.

Table 49-5 CEC fall timing in transmission

CFALL[1:0] bit	CEC fall timing	
	Start bit	Data bit
00b	The standard value (*1)	The standard value (*2)
01b	The standard value – 2 RCLK cycles	The standard value – 7 RCLK cycles
10b	The standard value – 3 RCLK cycles	The standard value – 9 RCLK cycles
11b	The standard value – 5 RCLK cycles	The standard value – 11 RCLK cycles

*1 : 4.5ms from the falling edge of start bit
*2 : 2.4ms from the bit start event

Table 49-6 CEC rising timing in transmission

CRISE[2:0] bit	CEC rise timing (common to start bit and data bit)
000b	The standard value (*)
001b	The standard value – 1 RCLK cycle
010b	The standard value – 2 RCLK cycles
011b	The standard value – 3 RCLK cycles
100b	The standard value – 4 RCLK cycles
101b	The standard value – 5 RCLK cycles
110b	The standard value – 6 RCLK cycles
111b	The standard value + 1 RCLK cycle

* : Start bit : 3.7ms from the falling edge of start bit
Data bit (logical 0) : 1.5ms from the bit start event
Data bit (logical 1) : 0.6ms from the bit start event

49.4.5 CEC flag register (CECFLG)

CECFLG

bit:	7	6	5	4	3	2	1	0
	CRSTFLG	CTD8FLG	CRD8FLG	CTNACKFLG	CTABTFLG	CRERRFLG	CTFLG	CRFLG
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
7	CRSTFLG	0	R	Start bit detect flag 0: The start bit is not detected or 8th bit is received 1: The start bit is detected
6	CTD8FLG	0	R	8th data transmit flag 0: The 8th bit is not transmitted or the 10th bit is transmitted 1: The 8th bit is transmitted
5	CRD8FLG	0	R	8th data receive flag 0: The 8th bit is not received or the 10th bit is received 1: The 8th bit is received
4	CTNACKFLG	0	R	Transmission NACK detect flag 0: NACK or ACK are not detected 1: NACK is detected (in the case Directly address transmission) ACK is detected (in the case Broadcast transmission) When CTXDEN bit of CECC3 register (stop the transmission), this bit is cleared to “0”.
3	CTABTFLG	0	R	Arbitration lost detect flag 0: Not detected 1: Detected When CTXDEN bit of CECC3 register (stop the transmission), this bit is cleared to “0”.
2	CRERRFLG	0	R	Reception error detect flag 0: Not detected 1: Reception error (out of the acceptable range) is detected When CRXDEN bit of CECC3 register (stop the reception), this bit is cleared to “0”.
1	CTFLG	0	R	Transmission state flag 0: Waiting 1: During transmission

Bit	Bit Name	Initial Value	R/W	Description
0	CRFLG	0	R	Reception state flag 0: Waiting 1: During reception When CABTEN bit of CECC4 register is set to “1” (error “L” output is permitted) and the error “L” pulse is output, this bit is also set to “1”.

49.4.6 CEC interrupt factor select register (CISEL)

CISEL

bit:	7	6	5	4	3	2	1	0
	CRISELS	CTISEL2	CTISEL1	CTISEL0	CRISELM	CRISEL2	CRISEL1	CRISEL0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	CRISELS	0	R/W	Reception start bit interrupt enable 0: disable 1: enable
6	CTISEL2	0	R/W	Transmission error interrupt enable 0: disable 1: enable
5	CTISEL1	0	R/W	Transmission 10th bit interrupt enable 0: disable 1: enable
4	CTISEL0	0	R/W	Transmission 8th bit interrupt enable 0: disable 1: enable
3	CRISELM	0	R/W	Reception interrupt mode select bit 0: The reception 8th/10th bit interrupt occurs regardless of destination address 1: Only in the case that the destination address is matched or the broadcast address, the reception 8th/10th bit interrupt occurs.

Bit	Bit Name	Initial Value	R/W	Description
2	CRISEL2	0	R/W	Reception error interrupt enable 0: disable 1: enable
1	CRISEL1	0	R/W	Reception 10th bit interrupt enable 0: disable 1: enable
0	CRISEL0	0	R/W	Reception 8th bit interrupt enable 0: disable 1: enable

Please set CISEL register when CECEN bit of CECC1 register is “0”.

49.4.7 CEC transmission buffer register 1 (CCTB1)

CCTB1

bit:	7	6	5	4	3	2	1	0
	CCTB1[7:0]							
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	CCTB1[7:0]	All 0	R/W	Please set transmission data

Please set CCTB1 register either of the following terms.

- When CTXDEN bit of CECC3 register is “0” (stop transmission)
- When CTXDEN bit of CECC3 register is “1” and CTD8FLG bit of CECFLG register is “1” (during the transmission EOM or ACK bit)

Please don’t set CCTB1 register when CTXDEN is “1” and CTD8FLG is “0”(during the transmission from 1st to 8th bit).

49.4.8 CEC transmission buffer register 2 (CCTB2)

CCTB2

bit:	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	CCTBA	CCTBE
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 2	—	All 0	R	Reserved This bit is always read as 0. The write value should always be 0.
1	CCTBA	0	R	Transmission ACK/NACK input bit 0: ACK is detected 1: NACK is detected Please read this bit after 10th bit (ACK bit) transmission (after CTD8FLG bit of CECFLG register is changed form "1" to "0").
0	CCTBE	0	R/W	Transmission EOM bit 0: The data block is continued 1: The data block is finished

Please set CCTBE bit either of the following terms.

- When CTXDEN bit of CECC3 register is "0" (stop transmission)
- When CTXDEN bit of CECC3 register is "1" and CTD8FLG bit of CECFLG register is "1" (during the transmission EOM or ACK bit)

Please don't set CCTBE bit when CTXDEN is "1" and CTD8FLG is "0"(during the transmission from 1st to 8th bit).

CCRB1

bit:	7	6	5	4	3	2	1	0
	CCRB1[7:0]							
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

49.4.9 CEC reception buffer register 1 (CCRB1)

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	CCRB1[7:0]	All 0	R	Received data is set

Please read CCRB1 register after receiving the 8th bit data.
(After CRD8FLG bit of CECFLG register is changed from "0" to "1")

49.4.10 CEC reception buffer register 2 (CCRB2)

CCRB2

bit:	7	6	5	4	3	2	1	0
	–	–	–	–	–	CCRBAI	CCRBAO	CCRBE
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R

Bit	Bit Name	Initial Value	R/W	Description
7 to 3	–	All 0	R	Reserved This bit is always read as 0. The write value should always be 0.
2	CCRBAI	0	R	Reception ACK input bit 0: ACK is detected 1: NACK is detected Please read this bit after 10th bit (ACK bit) reception (after CRD8FLG bit of CECFLG register is changed form “1” to “0”).
1	CCRBAO	0	R/W	Reception ACK output bit 0: Output ACK 1: Output NACK This bit is valid when CRACK bit of CECC2 register is “1” (program insertion).
0	CCRBE	0	R	Reception EOM bit 0: The data block is continued 1: The data block is finished Please read this bit after 10th bit (ACK bit) reception (after CRD8FLG bit of CECFLG register is changed form “1” to “0”).

Please set CCRBAO bit either of the following terms.

- When CRXDEN bit of CECC3 register is “0” (stop transmission)
- When CRXDEN bit of CECC3 register is “1” and receiving from the start bit to EOM bit

Please don’t set CCRBAO bit during receiving ACK bit.

49.4.11 CEC reception follower address register 1 (CRADR1)

CRADR1

bit:	7	6	5	4	3	2	1	0
	CRADRI17	CRADRI16	CRADRI15	CRADRI14	CRADRI13	CRADRI12	CRADRI11	CRADRI10
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description	
7	CRADRI17	0	R/W	Address 0111b select bit	0: not selected
6	CRADRI16	0	R/W	Address 0110b select bit	1: selected
5	CRADRI15	0	R/W	Address 0101b select bit	
4	CRADRI14	0	R/W	Address 0100b select bit	
3	CRADRI13	0	R/W	Address 0011b select bit	
2	CRADRI12	0	R/W	Address 0010b select bit	
1	CRADRI11	0	R/W	Address 0001b select bit	
0	CRADRI10	0	R/W	Address 0000b select bit	

Please select reception follower address of this device.
Please set CRADR1 register when CECEN bit of CECC1 register is “0”.

49.4.12 CEC reception follower address register 2 (CRADR2)

CRADR2

bit:	7	6	5	4	3	2	1	0
	CRADRI27	CRADRI26	CRADRI25	CRADRI24	CRADRI23	CRADRI22	CRADRI21	CRADRI20
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description	
7	CRADRI27	0	R/W	Address 1111b select bit	0: not selected
6	CRADRI26	0	R/W	Address 1110b select bit	1: selected
5	CRADRI25	0	R/W	Address 1101b select bit	
4	CRADRI24	0	R/W	Address 1100b select bit	
3	CRADRI23	0	R/W	Address 1011b select bit	
2	CRADRI22	0	R/W	Address 1010b select bit	
1	CRADRI21	0	R/W	Address 1001b select bit	
0	CRADRI20	0	R/W	Address 1000b select bit	

Please select reception follower address of this device.
Please set CRADR2 register when CECEN bit of CECC1 register is “0”.

In the case that CRADRI27 bit is set to “1”, when the follower address is “1111b”(broadcast) and CRACK bit of CECC2 register is “1” (the hardware insertion of ACK output in the reception), ACK is replied.

In this section, it may be represented as “destination address is matched” that received destination address is matched to the address selected by CRADR1 or CRADR2 registers.

49.4.13 CEC interrupt factor register (CINTR)

CINTR

bit:	7	6	5	4	3	2	1	0
	CINT7	CINT6	CINT5	CINT4	CINT3	CINT2	CINT1	CINT0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
7	CINT7	0	R	Interrupt factor 7 0: Reception 8th bit interrupt is not detected 1: Reception 8th bit interrupt is detected This bit is cleared to “0” by writing “1” to CINTCLR7 bit of CINTCLR register.
6	CINT6	0	R	Interrupt factor 6 0: Reception 10th bit interrupt is not detected 1: Reception 10th bit interrupt is detected This bit is cleared to “0” by writing “1” to CINTCLR6 bit of CINTCLR register.
5	CINT5	0	R	Interrupt factor 5 0: Reception error interrupt is not detected 1: Reception error interrupt is detected This bit is cleared to “0” by writing “1” to CINTCLR5 bit of CINTCLR register.
4	CINT4	0	R	Interrupt factor 4 0: Reception start bit interrupt is not detected 1: Reception start bit interrupt is detected This bit is cleared to “0” by writing “1” to CINTCLR4 bit of CINTCLR register.

Bit	Bit Name	Initial Value	R/W	Description
3	CINT3	0	R	Interrupt factor 3 0: Transmission 8th bit interrupt is not detected 1: Transmission 8th bit interrupt is detected This bit is cleared to “0” by writing “1” to CINTCLR3 bit of CINTCLR register.
2	CINT2	0	R	Interrupt factor 2 0: Transmission 10th bit interrupt is not detected 1: Transmission 10th bit interrupt is detected This bit is cleared to “0” by writing “1” to CINTCLR2 bit of CINTCLR register.
1	CINT1	0	R	Interrupt factor 1 0: Transmission NACK interrupt is not detected 1: Transmission NACK interrupt is detected This bit is cleared to “0” by writing “1” to CINTCLR1 bit of CINTCLR register.
0	CINT0	0	R	Interrupt factor 0 0: Arbitration lost interrupt is not detected 1: Arbitration lost interrupt is detected This bit is cleared to “0” by writing “1” to CINTCLR0 bit of CINTCLR register.

49.4.14 CEC interrupt factor clear register (CINTCLR)

CINTCLR

bit:	7	6	5	4	3	2	1	0
	CINTCLR7	CINTCLR6	CINTCLR5	CINTCLR4	CINTCLR3	CINTCLR2	CINTCLR1	CINTCLR0
Initial value:	0	0	0	0	0	0	0	0
R/W:	W	W	W	W	W	W	W	W

Bit	Bit Name	Initial Value	R/W	Description
7	CINTCLR7	—	W	CEC interrupt factor clear bit 7 0 : no operation 1: Clear CINT7 bit and the interrupt factor indicated by CINT7
6	CINTCLR6	—	W	CEC interrupt factor clear bit 6 0 : no operation 1: Clear CINT6 bit and the interrupt factor indicated by CINT6

Bit	Bit Name	Initial Value	R/W	Description
5	CINTCLR5	–	W	CEC interrupt factor clear bit 5 0 : no operation 1: Clear CINT5 bit and the interrupt factor indicated by CINT5
4	CINTCLR4	–	W	CEC interrupt factor clear bit 4 0 : no operation 1: Clear CINT4 bit and the interrupt factor indicated by CINT4
3	CINTCLR3	–	W	CEC interrupt factor clear bit 3 0 : no operation 1: Clear CINT3 bit and the interrupt factor indicated by CINT3
2	CINTCLR2	–	W	CEC interrupt factor clear bit 2 0 : no operation 1: Clear CINT2 bit and the interrupt factor indicated by CINT2
1	CINTCLR1	–	W	CEC interrupt factor clear bit 1 0 : no operation 1: Clear CINT1 bit and the interrupt factor indicated by CINT1
0	CINTCLR0	–	W	CEC interrupt factor clear bit 0 0 : no operation 1: Clear CINT0 bit and the interrupt factor indicated by CINT0

49.4.15 CEC interrupt mode select register (CINTSEL)

CINTSEL

bit:	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	CINTSEL
Initial value:	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 1	–	All 0	R	Reserved This bit is always read as 0. The write value should always be 0.
0	CINTSEL	1	R/W	CEC interrupt mode select bit 0: Output the interrupt signals until the interrupt factors are cleared by CINTCLR register 1: Output the interrupt signals for 1 RCLK cycle

49.5 Operation

49.5.1 CEC input/output timing and the specification value

RCLK(32.768KHz) clock is used for source clock of CEC operations for transmission and reception.

Therefore, in the case of the transmission, an output signal is changed at the timing which is created by source clock and which is the nearest as CEC specification value. Also in the case of the reception, an input signal is sampled at the timing which is created by source clock.

An acceptable reception range or an output timing may be expressed by the values in some sections. The nearest timing which is created by source clock is also used for these values.

49.5.2 Digital filter

CEC input signals are transmitted to the internal circuit synchronized with the source clock RCLK. In the case that CFIL bit of CECC2 register is “1”, if the input CEC level is matched two RCLK cycles, the input level is transmitted to the internal circuit.

Figure 49-2 shows the timing diagram of digital filter.

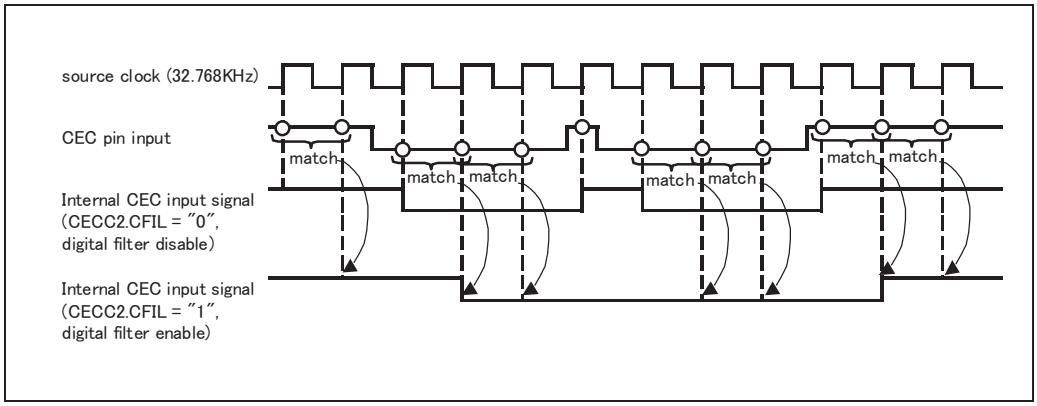


Figure 49-2 Digital filter

49.5.3 Data reception

49.5.3.1 Start bit decision

The decision timing of start and data bit can be selected by CRRNG bit of CECC2 register. The acceptable range of start bit can be selected by CSTRRNG bit of CECC2 register. Figure 49-3 shows the acceptable range of start bit.

When acceptable start bit is detected, CRSTFLG bit of CECFLG register is set to “1” (detect start bit).

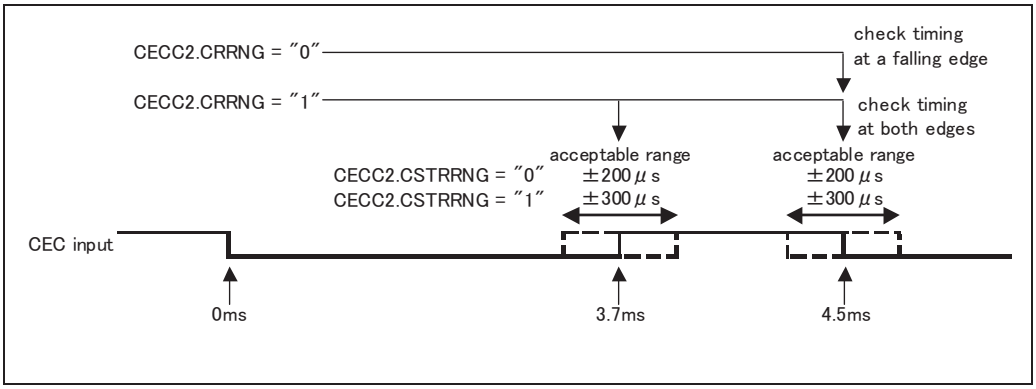


Figure 49-3 Acceptable range of start bit

49.5.3.2 Data bit decision

The decision timing of start and data bit can be selected by CRRNG bit of CECC2 register. The acceptable range of data bit can be selected by CDATRNG bit of CECC2 register. Figure 49-4 and Figure 49-5 shows the acceptable range of data bit.

When CRRNG bit of CECC2 register is “0”, if the CEC rising edge is before 1.05ms, the received data is judged as “1”, and if the CEC rising edge is after 1.05ms, the received data is judged as “0”.

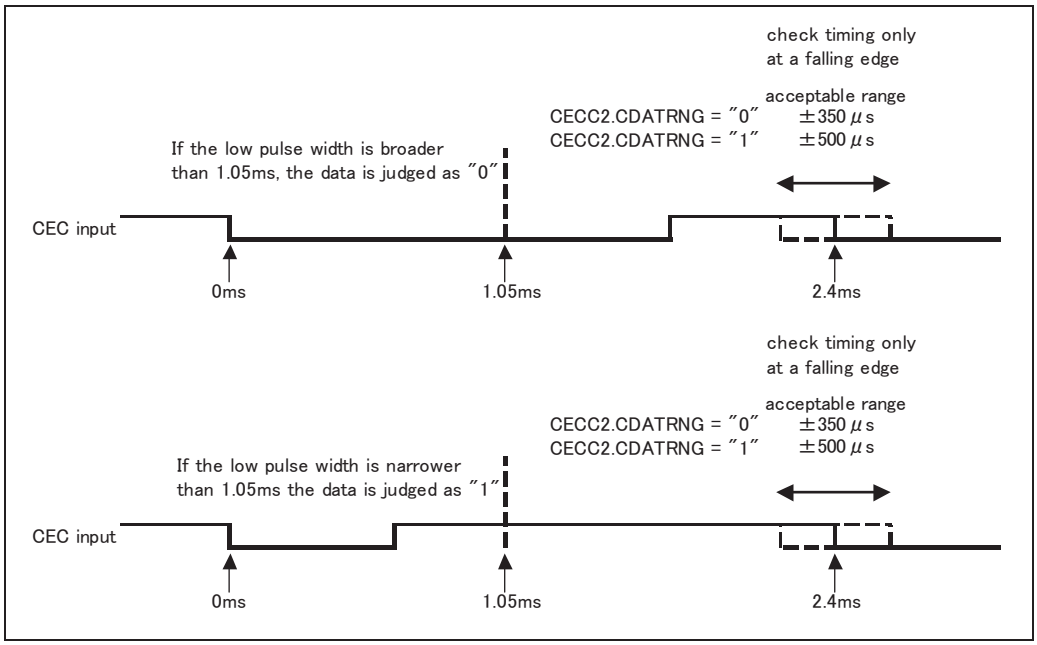


Figure 49-4 Acceptable range of data bit (CECC2.CRRNG = “0”)

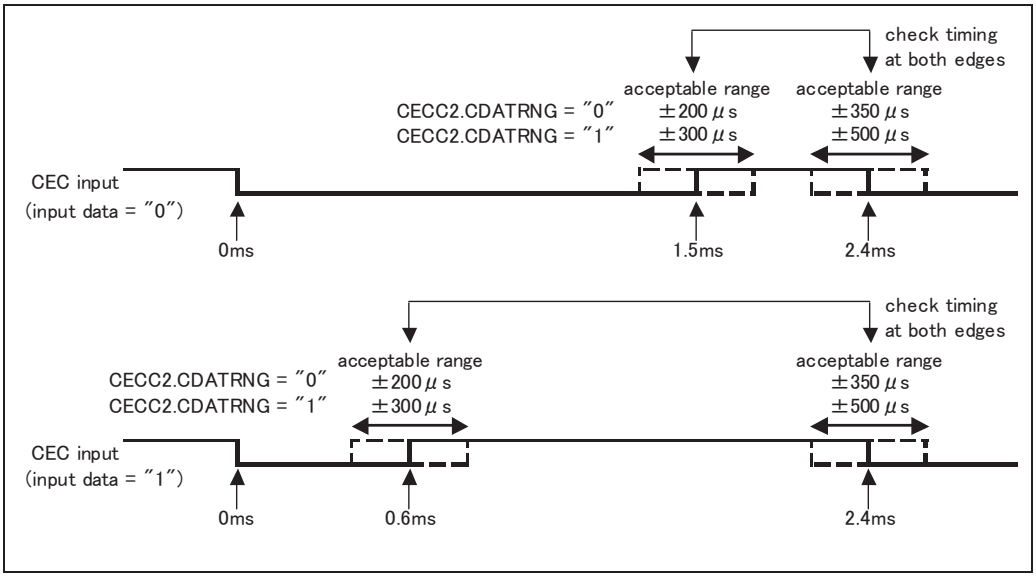


Figure 49-5 Acceptable range of data bit (CECC2.CRRNG = "1")

If the data reception timing is out of the acceptable range, reception error occurs. And it causes following operation.

- CRERRFLG bit of CECFLG register is set to "1"(reception error).
- In the case that CABTEN bit of CECC4 register is "1", 3.6ms "L" pulse is transmitted.

When CABTEN bit of CECC4 register is "1", output timing of error "L" pulse can be selected by CABTWEN bit of CECC4 register. Figure 49-6 shows output timing of error "L" pulse.

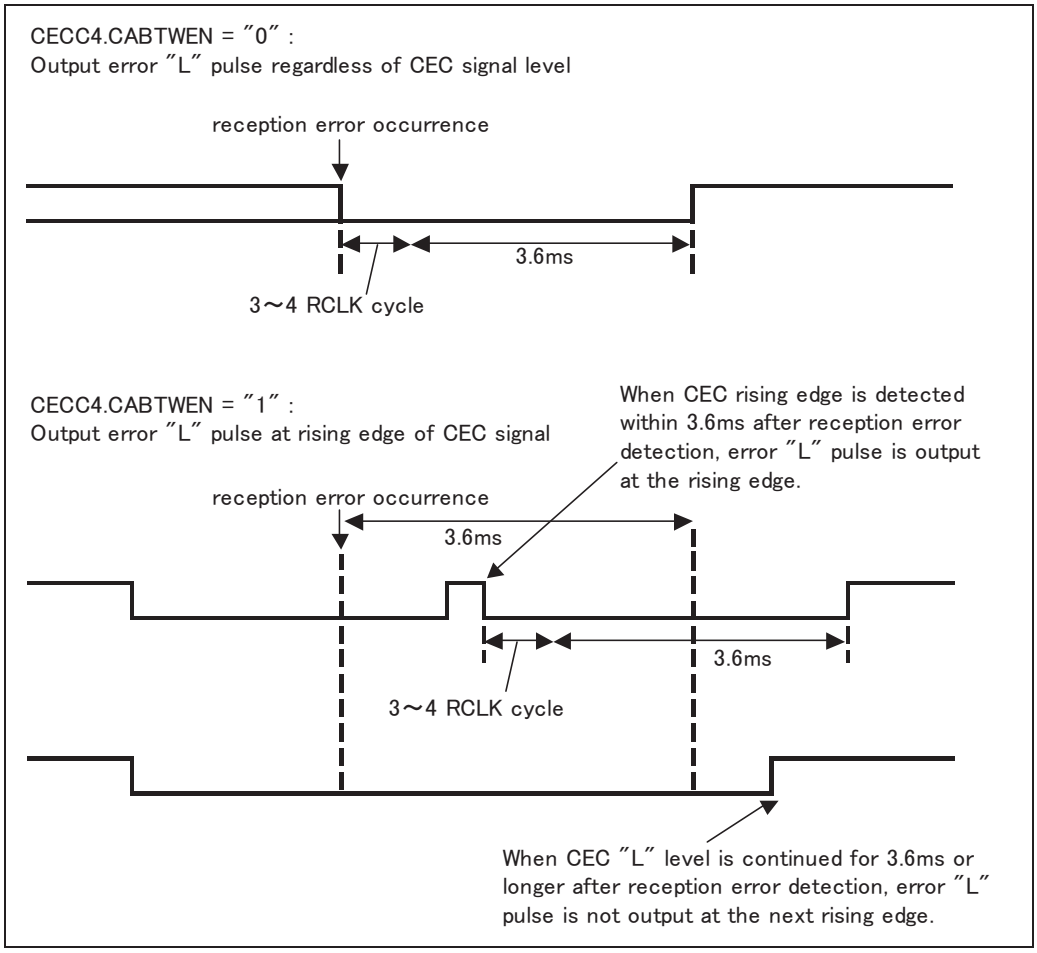


Figure 49-6 Error "L" pulse at reception error (CECC4.CABTEN = "1")

49.5.3.3 ACK bit output

ACK bit value which is transmitted at 10th bit can be selected.

In the case that CRACK bit of CECC2 register is "0" (program insertion), the value which is set to CCRBAO bit of CCRB2 register is output as ACK data.

In the case that CRACK bit is “1” (hardware insertion), the ACK or NACK output is decided by the relation between a received Destination address and the address selected by CRADR1 or CRADR2 registers.

Table 49-7 shows ACK or NACK output conditions.

Table 49-7 ACK output

CRACK bit	CCRBAO bit	Destination Address		ACK output
		Received Destination Address	The own address selected by CRADR1 or CRADR2 registers	
0	0	-	-	ACK
	1	-	-	NACK
1	-	Directly address (0000b～1110b)	Match with received address	ACK
			Not match with received address	NACK
		Broadcast address (1111b)	1111b(match with received address)	ACK
			0000b～1110b	NACK

49.5.3.4 Example of reception sequence

Figure 49-7 shows an example of reception sequence. Figure 49-8 shows an example of reception sequence (error occasion case, changing from “error L pulse disable” to “enable”).

When a reception error is detected, CRERRFLG bit of CECFLG register is set to “1”. When a reception is stopped by a reception error, please set “0” to CRXDEN bit of CECC3 register (reception stop), then CRERRFLG is set to “0”. For restarting reception, please wait for more than 1 RCLK cycle after setting CRXDEN bit “0”, and then set CRXDEN bit “1”(reception permit).

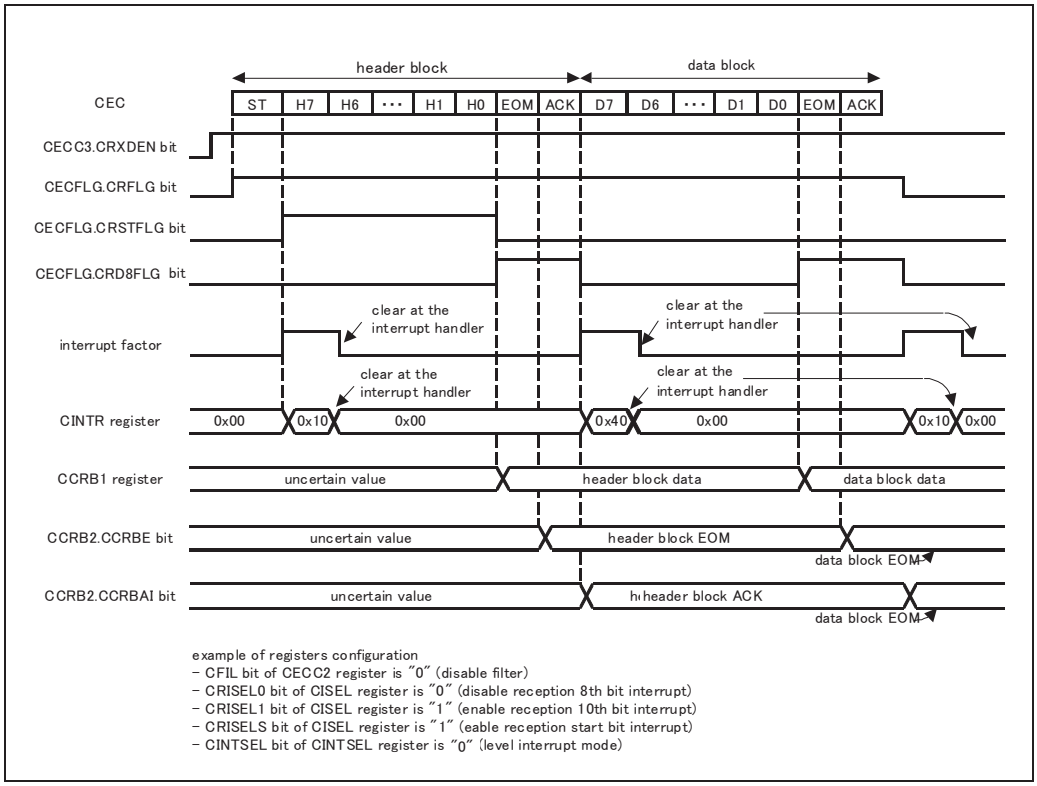


Figure 49-7 Example of reception sequence

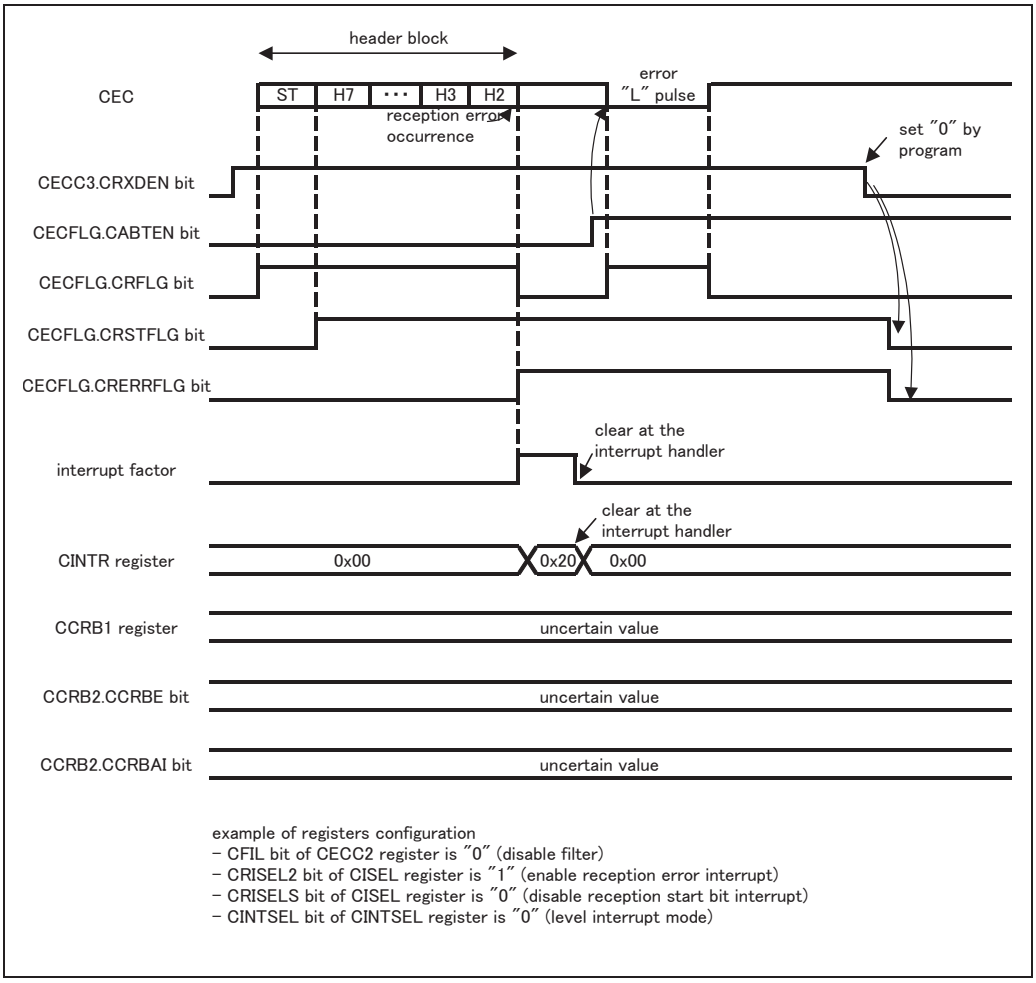


Figure 49-8 Example of reception sequence
(In the case that reception error occurs, and error "L" pulse is changed from disable to enable)

49.5.4 Data transmission

49.5.4.1 Transmission timing select

The rise timing or fall timing of transmission signal can be selected.

The rise timing of transmission signal can be selected by CRISE[2:0] bit of CECC4 register.

Figure 49-9 shows rise timing of transmission signal.

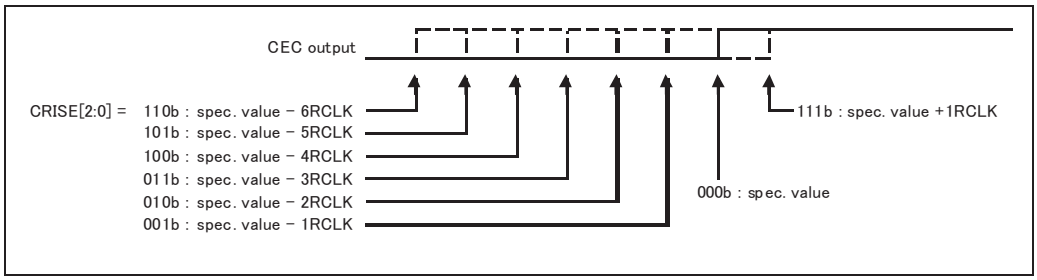


Figure 49-9 Rise timing of transmission signal

The fall timing of transmission signal can be selected by CFALL[1:0] bit of CECC4 register.

Figure 49-10 shows fall timing of transmission signal.

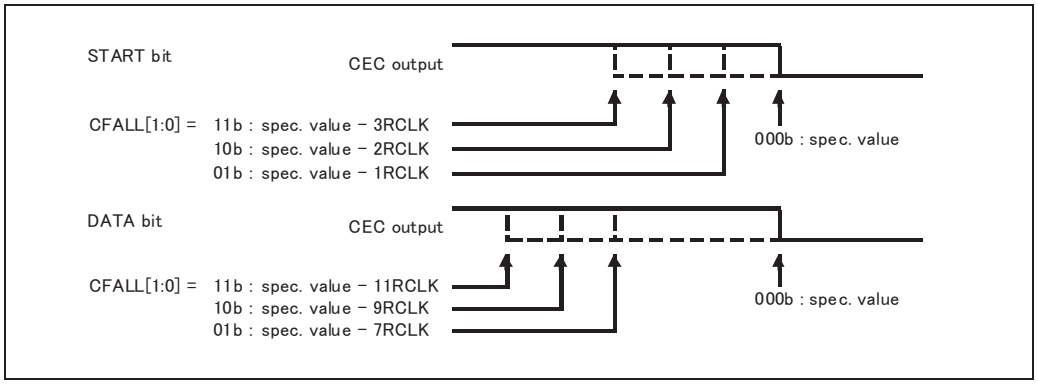


Figure 49-10 Fall timing of transmission signal

49.5.4.2 Arbitration lost detection

During a data transmission, an arbitration lost is detected in the following case

- When this LSI make CEC signal Hi-Z, CEC signal becomes “L” by an external factor.

The range that arbitration lost can be detected at CEC rising edge can be selected by CTABTS bit of CECC2 register. Figure 49-11 shows the range of the arbitration lost detection.

When an arbitration lost is detected, CTABTFLG bit of CECFLG register is set to “1” (arbitration lost detected).

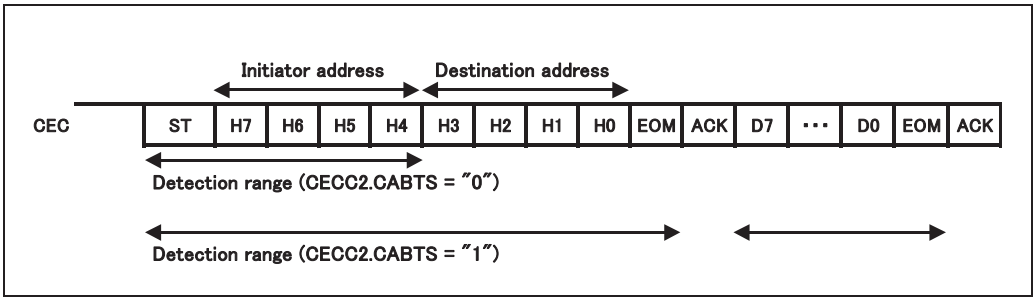


Figure 49-11 The range of arbitration lost detection

49.5.4.3 Example of transmission sequence

Figure 49-12 shows an example of transmission sequence. Figure 49-13 shows an example of transmission sequence (in the case of receiving NACK). And Figure 49-14 shows an example of transmission sequence (in the case of arbitration lost detection).

After transmission completion, please set “0” to CTXDEN bit of CECC3 register (transmission stop). Even in the case continuous transmission, after 1 frame (a header and some data blocks) transmission, please set “0” to CTXDEN. And then, after waiting for more than 1 RCLK cycle, please set CTXDEN bit “1”(transmission permit) again.

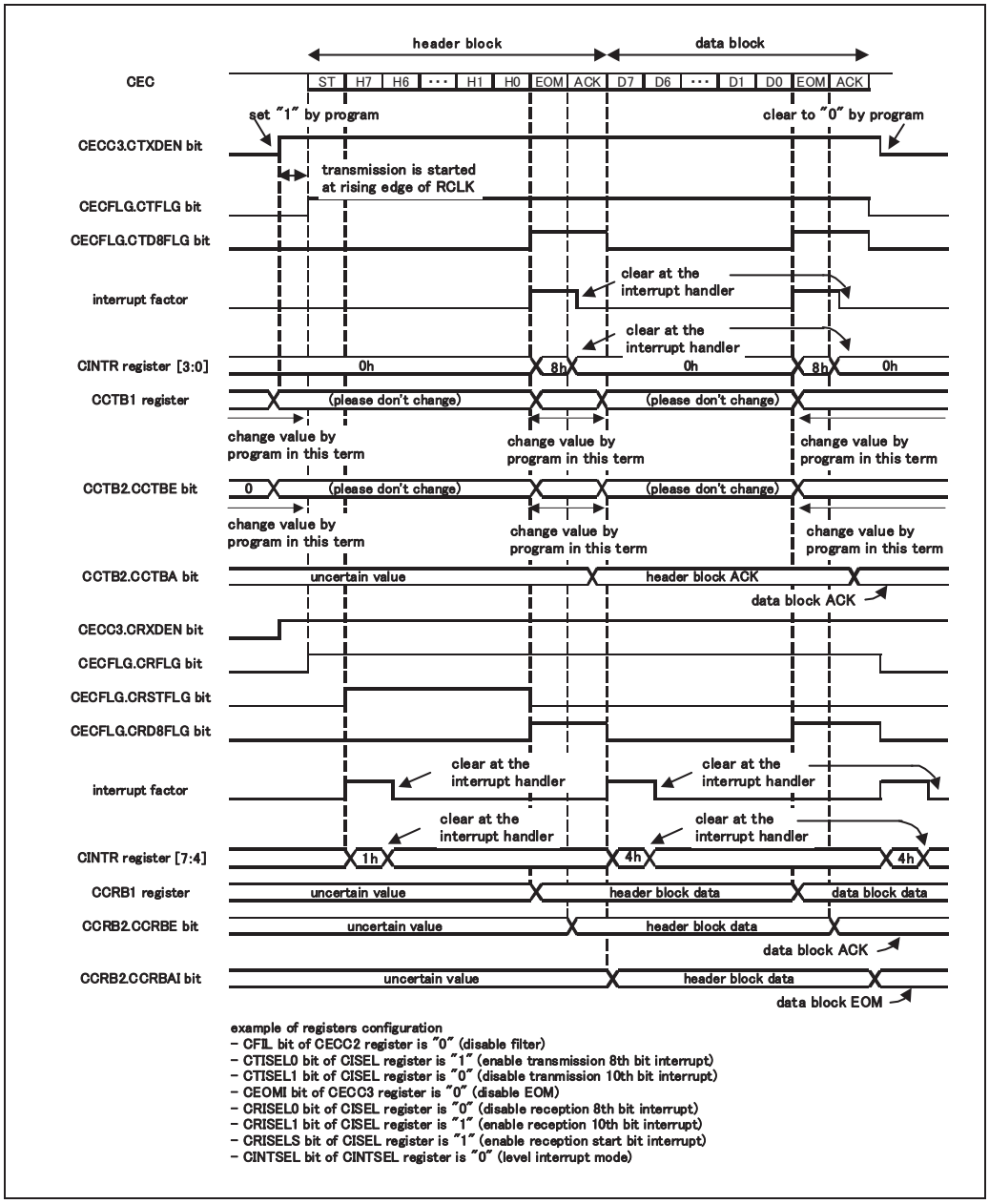


Figure 49-12 Example of transmission sequence

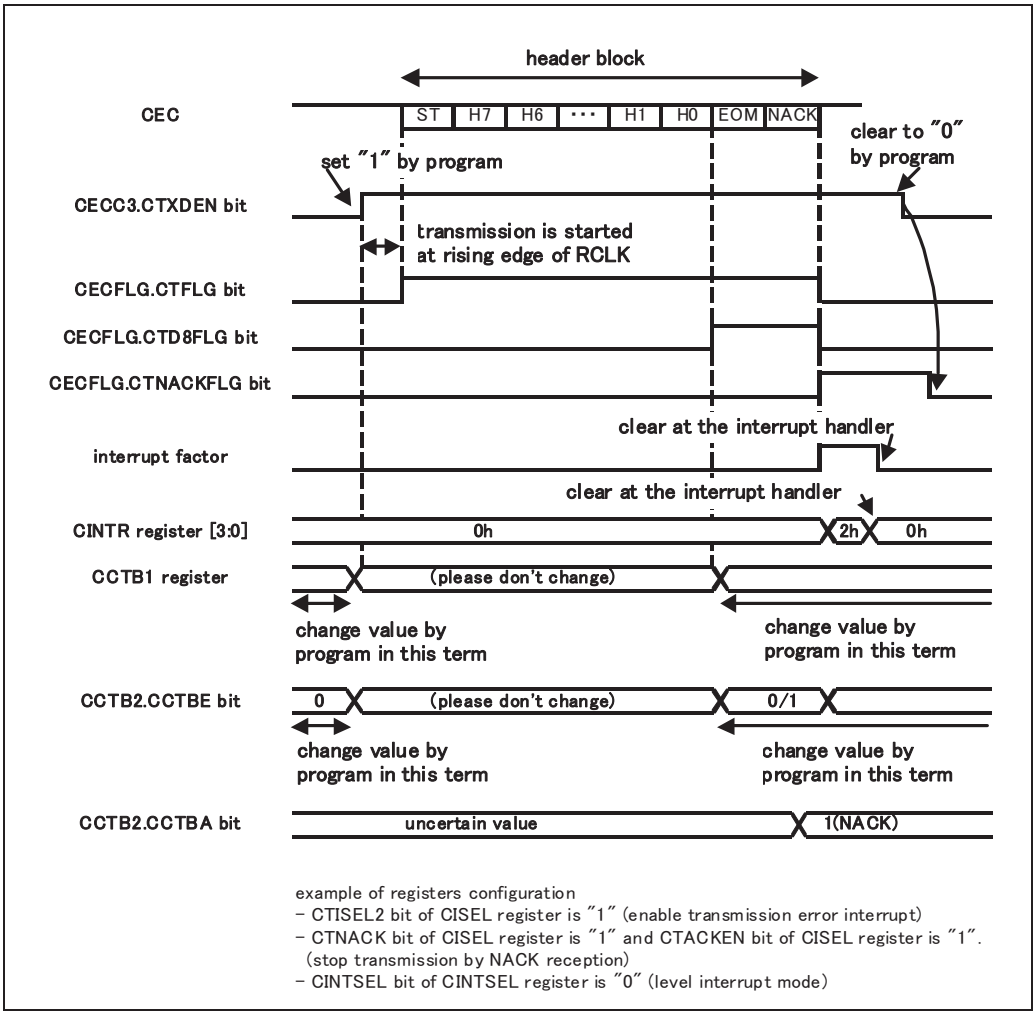


Figure 49-13 Example of transmission sequence (receive NACK)

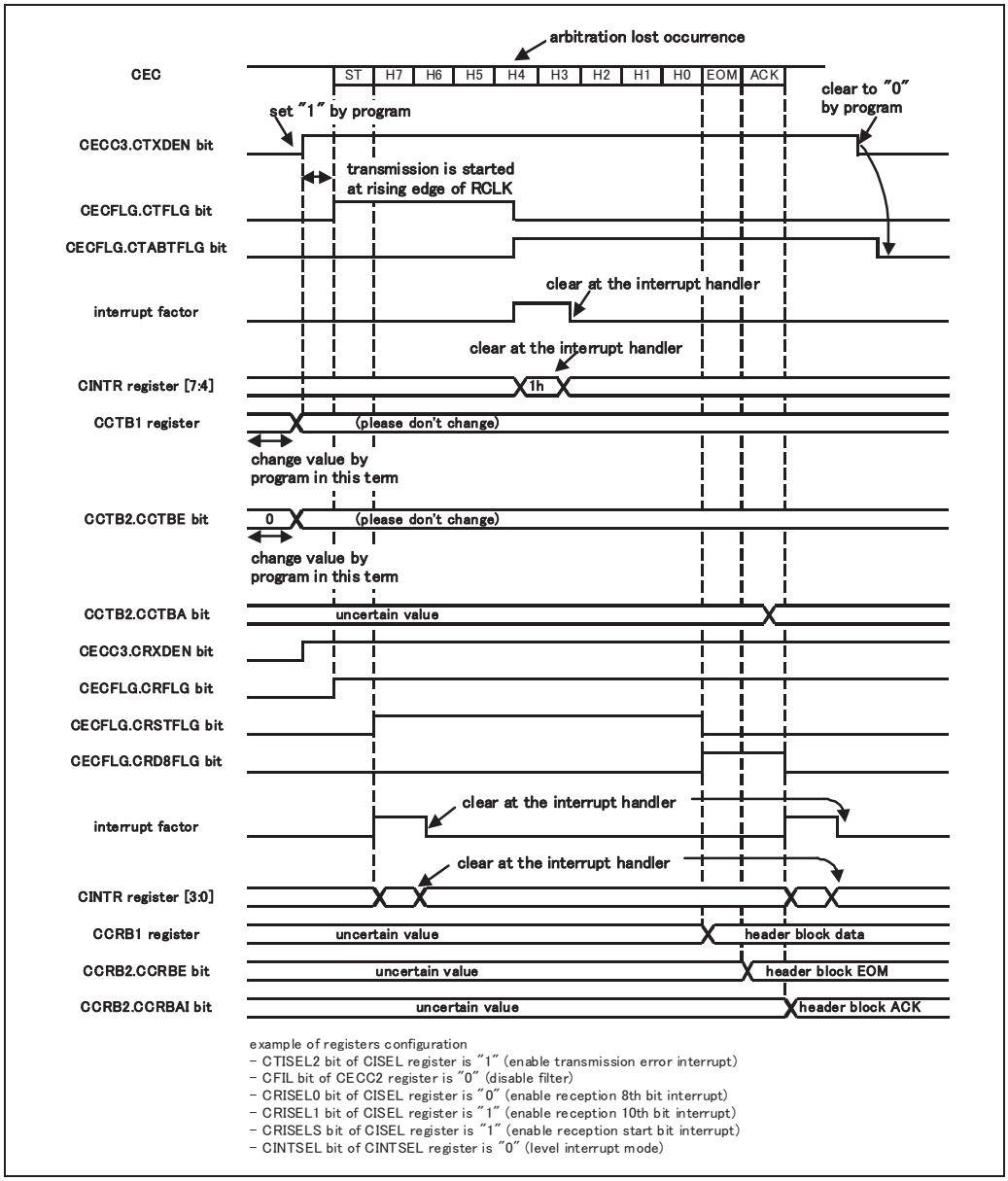


Figure 49-14 Example of transmission sequence (arbitration lost detection)

49.6 Interrupt

CEC function has CEC1 interrupt and CEC2 interrupt.

Table 49-8 and Table 49-9 show the interrupt factor of CEC function. CEC1 interrupt request and CEC2 interrupt request occurs by these interrupt factors. In the case that CRISELM bit of CISEL register is “1”, reception 8th/10th bit interrupt occurs only following cases.

- Destination address matches with the address selected by CRADRI1 register or CRADRI2 register.
- Destination address is Broadcast address (1111b)

Table 49-8 CEC1 interrupt factor

Interrupt type	Interrupt factor	Interrupt request timing	Enable bit
Transmission interrupt	Transmission 8th bit	CECFLG.CTD8FLG bit changes “0” to 1”	CTISEL0
	Transmission 10th bit	CECFLG.CTD8FLG bit changes “1” to “0”	CTISEL1
Transmission error interrupt	Arbitration lost	CECFLG.CTABTFLG bit changes “0” to “1”	CTISEL2
	NACK reception (Directly address) ACK reception (Broadcast address)	CECFLGCTNACKFLG bit changes “0” to “1”	

Table 49-9 CEC2 interrupt factor

Interrupt type	Interrupt factor	Interrupt request timing	Enable bit
Reception interrupt	Reception 8th bit	CECFLG.CRD8FLG bit changes “0” to 1”	CRISEL0
	Reception 10th bit	CECFLG.CRD8FLG bit changes “1” to “0”	CRISEL1
	Start bit detection	CECFLG.CRSTFLG bit changes “0” to “1”	CRISELS
Reception error interrupt	Out of acceptable range	CECFLGCRERRFLG bit changes “0” to “1”	CRISEL2

Figure 49-15 shows block diagram of CEC function interrupt. In the case that CINTSEL bit is "1", interrupt request is maintained until CINT[7:0] bits of CINTR register are cleared by CINTCLR register.

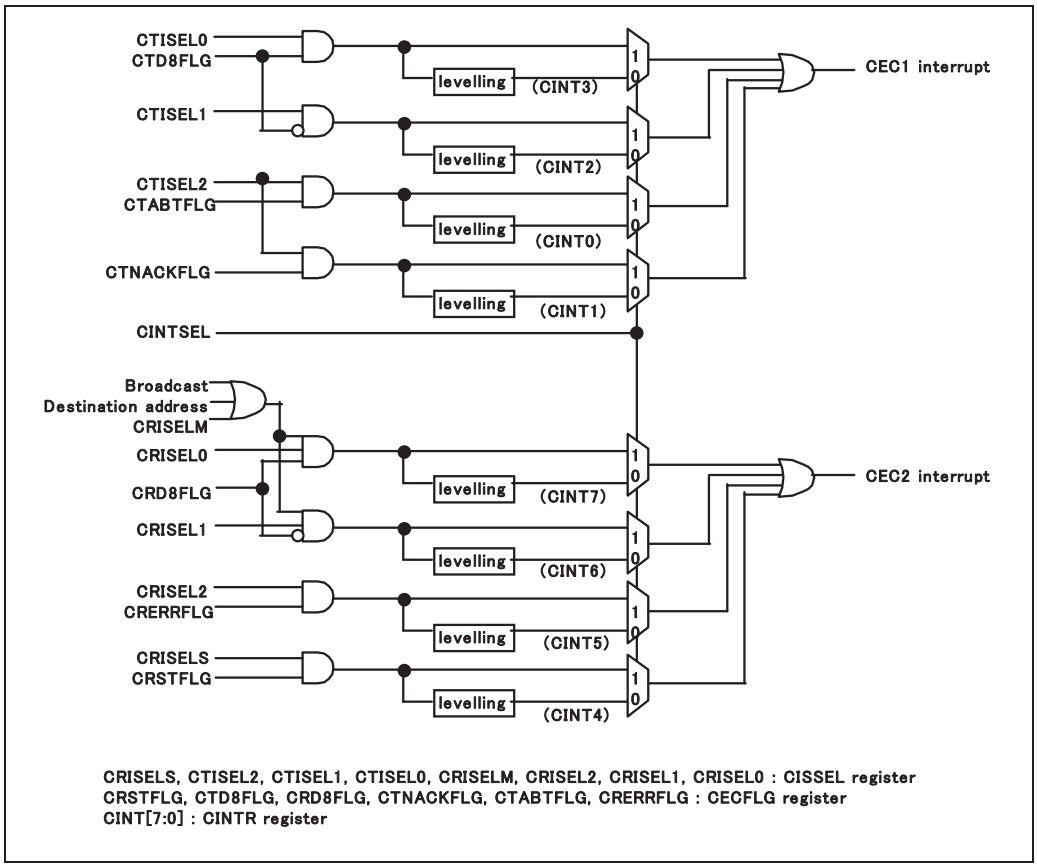


Figure 49-15 Interrupt of CEC function

49.7 Notes for using CEC function

49.7.4.1 Operation of register bits

CEC register bits are operated synchronously with RCLK. When register bit is written by program, the value is changed immediately. But internal circuit acts at RCLK clock timing. Therefore, in the case continuously writing same bit or reading bits which is influenced other bits, please wait for more than 1 RCLK cycle.

Example 1 : In the case continuously writing same bit

(1) Set a bit “0”

(2) Wait 1 RCLK cycle

(3) Change the bit to “1”

Example 2 : In the case reading bits which is influenced other bits

In the case, after stopping reception, reading CRERRFLG bit of CECFLG register “0” (error not detected)

(1) Set CRXDEN bit of CECC3 register “0”(reception stop)

(2) Wait 1 RCLK cycle

(3) Read CRERRFLG bit of CECFLG register

Section 50 Sound Processing Unit 2 (SPU2)

The sound processing unit 2 (SPU2) is a dedicated unit for sound and audio processing, which consists of two DSPs that are specially designed to process audio CODECs such as AAC or MP3 and to perform pre- and post-sound processing and two bus bridges (SPU–DMAC) each of which has a DMAC that can be started by the DSP and system CPU.

The SPU2 is enhanced to support direct access from the system CPU to DSP I/O peripheral modules and access from the DSP to SPU2 external spaces in order to perform pre- and post-processing as well as audio CODEC processing by the DSP.

50.1 Features

Table 50.1 shows the SPU2 functions and features.

Table 50.1 MAC Functions and Features

Component	Item	Description
DMAC	Number of channels	• 3 channels
	Transfer data length	• SHwy: 1 longword (4 bytes), 8 longwords (32 bytes) • DSP-P RAM: 32 bits/32 bits × 8 bursts • DSP-X/Y RAM: 24 bits 16 bits × 16/24 bits × 8 bursts (aligned mode) 24 bits × 10/11 bursts (seamless mode)
	Max. transfer count	• 65,535 (16 bits)
	Address mode	• Dual address mode
	Addressing	• Upper 9 bits fixed (base address) • Fixed/23-bit (8-MByte) increment
	Transfer request	• Auto request
	Priority order	• Fixed (Ch0>Ch1>Ch2)
	Interrupt request	• Interrupt requests can be generated to the SH and DSP at the end of data transfer. Both of interrupt sources and interrupt requests can be masked.
	Data swap	• DMA transfer data can be swapped. (Byte swap, word swap, byte-word swap)
	• A DMAC that supports all the above functions is integrated with a DSP. • The SPU2 has two sets of DSPs and DMACs. • With more than one DSP, transfers between the DSP-X/Y and memory are complete within the SPU without using the SHwy.	

Component	Item	Description
Bus bridge	DSP interface	• Supports DMA transfers between the external memory and the DSP. • Provides direct access to the DSP memory from the CPU in target through mode. • Provides access to the external space (such as the CPU registers) of the SPU2 from the DSP in bus-through mode. • Provides access to the SPU2 registers from the DSP.
Bus bridge	IO interface	• Arbitrates access to the SPU2 registers and external peripheral modules from the DSP and the CPU. • Can be connected with peripheral modules.

Figure 50.1 shows a block diagram of the SPU2.

As shown in the figure, the SPU2 has two DSPs.

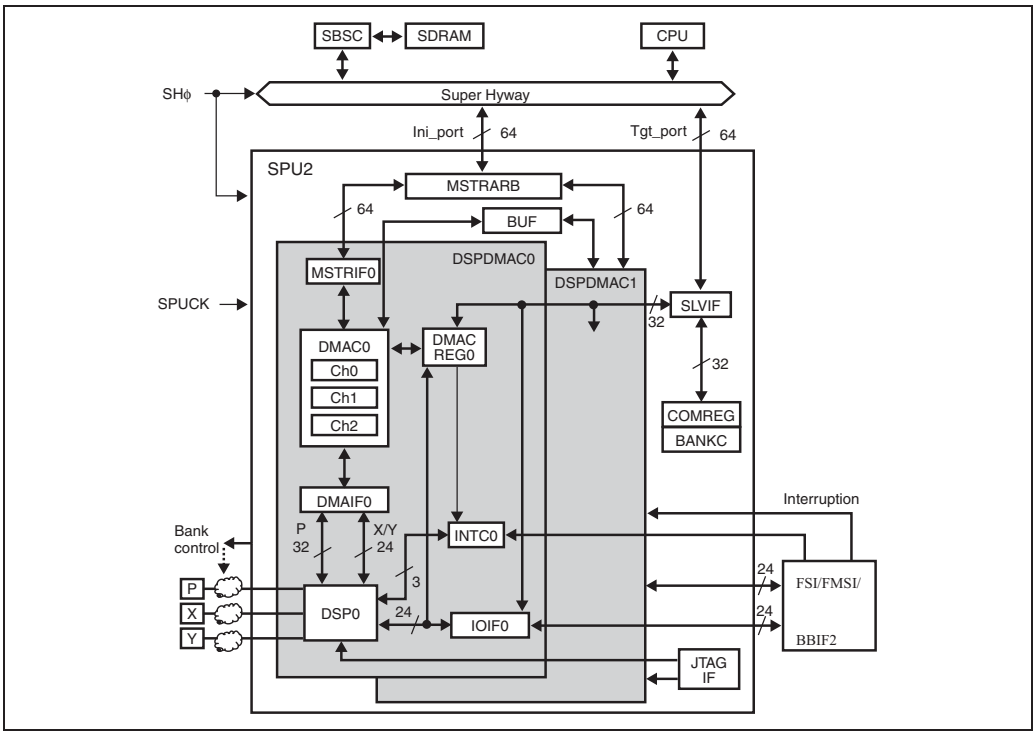


Figure 50.1 SPU2 Block Diagram

Table 50.2 gives a brief description of each block in the SPU2.

Table 50.2 Overview of SPU2 Sub Modules

Module Abbreviation		Overview
SLVIF		• SHwy target interface • One port regardless of the number of DSPs
COMREG		• Global registers shared between the CPU and all integrated DSPs
BANKC		• Memory bank controller used to control memory shared among the DSPs
JTAGIF		• JTAG debug interface supporting multi-core systems
MSTRARB		• SHwy initiator interface • Arbiter that grants SHwy bus mastership to one port when more than one DSP is equipped
BUF		• DMA data buffer used for DMA data communication between the DSPs
DSPDMAC		• One DSPDMAC module integrated (including the following sub modules) when one DSP is equipped.
	DMACREG	• Register used mainly to start a DMAC
	INTC	• DSP interrupt controller • Controls the one-hot condition of the SPU2 internal interrupt sources and two SPU2 external sources.
	IOIF	• DSP-IO interface • Arbitrates access to the DSP-IO space from the DSP and CPU.
	MSTRIF	• Bus master interface that supports SHwy initiator ports • Issues bus commands when a DMAC is started. • Issues bus commands in bus-through mode.
	DMAC	• 3-channel DMA controller
	DMAIF	• DSP's DMA interface
	DSP	• 24-bit DSP dedicated for audio processing

50.2 Register Descriptions

The table below shows the SPU2 register configuration.

Table 50.3 Register Configuration

Register Name	Abbreviation	R/W		Access Size (Bit)		Physical Address	DSP Address
		CPU	DSP	CPU	DSP		
PRAM bank control register 0	PBANKC0	R/W	R	32	24	H'FE2F FC00	H'FF00
PRAM bank control register 1	PBANKC1	R/W	R	32	24	H'FE2F FC04	H'FF01
XRAM bank control register 0	XBANKC0	R/W	R/W	32	24	H'FE2F FC10	H'FF04
XRAM bank control register 1	XBANKC1	R/W	R/W	32	24	H'FE2F FC14	H'FF05
SPU software reset register	SPUSRST	R/W	R	32	24	H'FE2F FC24	H'FF09
SPU address register	SPUADR	R	R	32	24	H'FE2F FC28	H'FF0A
SHwy endian register	ENDIAN	R	R	32	24	H'FE2F FC2C	H'FF0B
Global common register 0	GCOM0	R/W	R/W	32	24	H'FE2F FC40	H'FF10
Global common register 1	GCOM1	R/W	R/W	32	24	H'FE2F FC44	H'FF11
Global common register 2	GCOM2	R/W	R/W	32	24	H'FE2F FC48	H'FF12
Global common register 3	GCOM3	R/W	R/W	32	24	H'FE2F FC4C	H'FF13
Global common register 4	GCOM4	R/W	R/W	32	24	H'FE2F FC50	H'FF14
Global common register 5	GCOM5	R/W	R/W	32	24	H'FE2F FC54	H'FF15
Global common register 6	GCOM6	R/W	R/W	32	24	H'FE2F FC58	H'FF16
Global common register 7	GCOM7	R/W	R/W	32	24	H'FE2F FC5C	H'FF17
Inter-DSP communication buffer register 0	DMABUF0	R	R	32	24	H'FE2F FC80	H'FF20
Inter-DSP communication buffer register 1	DMABUF1	R	R	32	24	H'FE2F FC84	H'FF21
Inter-DSP communication buffer register 2	DMABUF2	R	R	32	24	H'FE2F FC88	H'FF22
Inter-DSP communication buffer register 3	DMABUF3	R	R	32	24	H'FE2F FC8C	H'FF23
DSP0 registers							
DSP full reset register	DSPRST	R/W	R	32	24	H'FE2F FD00	H'FF40
DSP core reset register	DSPCORERST	R/W	R	32	24	H'FE2F FD04	H'FF41

Register Name	Abbreviation	R/W		Access Size (Bit)		Physical Address	DSP Address
		CPU	DSP	CPU	DSP		
DSP hold register	DSPHOLD	R	R	32	24	H'FE2F FD08	H'FF42
DSP restart register	DSPRESTART	R/W	R	32	24	H'FE2F FD0C	H'FF43
CPU interrupt source mask register	IEMASKC	R/W	—	32	24	H'FE2F FD18	H'FF46
CPU interrupt signal mask register	IMASKC	R/W	—	32	24	H'FE2F FD1C	H'FF47
CPU interrupt source register	IEVENTC	R/W	—	32	24	H'FE2F FD20	H'FF48
DSP interrupt source mask register	IEMASKD	—	R/W	32	24	H'FE2F FD24	H'FF49
DSP interrupt signal mask register	IMASKD	—	R/W	32	24	H'FE2F FD28	H'FF4A
DSP interrupt set register	IESETD	R/W	R/W	32	24	H'FE2F FD2C	H'FF4B
DSP interrupt clear register	IECLRD	—	R/W	32	24	H'FE2F FD30	H'FF4C
DMAC operation register	OR	R/W	R/W	32	24	H'FE2F FD34	H'FF4D
CPU-DSP communication register 0	COM0	R/W	R/W	32	24	H'FE2F FD38	H'FF4E
CPU-DSP communication register 1	COM1	R/W	R/W	32	24	H'FE2F FD3C	H'FF4F
CPU-DSP communication register 2	COM2	R/W	R/W	32	24	H'FE2F FD40	H'FF50
CPU-DSP communication register 3	COM3	R/W	R/W	32	24	H'FE2F FD44	H'FF51
CPU-DSP communication register 4	COM4	R/W	R/W	32	24	H'FE2F FD48	H'FF52
CPU-DSP communication register 5	COM5	R/W	R/W	32	24	H'FE2F FD4C	H'FF53
CPU-DSP communication register 6	COM6	R/W	R/W	32	24	H'FE2F FD50	H'FF54
CPU-DSP communication register 7	COM7	R/W	R/W	32	24	H'FE2F FD54	H'FF55
Bus-through address high register	BTADRU	R/W	R/W	32	24	H'FE2F FD58	H'FF56
Bus-through address low register	BTADRL	R/W	R/W	32	24	H'FE2F FD5C	H'FF57
Bus-through write data high register	WDATU	R/W	R/W	32	24	H'FE2F FD60	H'FF58
Bus-through write data low register	WDATL	R/W	R/W	32	24	H'FE2F FD64	H'FF59
Bus-through read data high register	RDATU	R	R	32	24	H'FE2F FD68	H'FF5A
Bus-through read data low register	RDATL	R	R	32	24	H'FE2F FD6C	H'FF5B
Bus-through mode control register	BTCTRL	R	R/W	32	24	H'FE2F FD70	H'FF5C
SPU status register	SPUSTS	R	R	32	24	H'FE2F FD74	H'FF5D
Source base address register 0	SBAR0	R/W	R/W	32	24	H'FE2F FE00	H'FF80
Source address register 0	SAR0	R/W	R/W	32	24	H'FE2F FE04	H'FF81
Destination base address register 0	DBAR0	R/W	R/W	32	24	H'FE2F FE08	H'FF82
Destination address register 0	DAR0	R/W	R/W	32	24	H'FE2F FE0C	H'FF83

Register Name	Abbreviation	R/W		Access Size (Bit)		Physical Address	DSP Address
		CPU	DSP	CPU	DSP		
Transfer count register 0	TCR0	R/W	R/W	32	24	H'FE2F FE10	H'FF84
SHwy priority register 0	SHPRI0	R/W	R/W	32	24	H'FE2F FE14	H'FF85
Channel control register 0	CHCR0	R/W	R/W	32	24	H'FE2F FE18	H'FF86
Source base address register 1	SBAR1	R/W	R/W	32	24	H'FE2F FE20	H'FF88
Source address register 1	SAR1	R/W	R/W	32	24		H'FF89
Destination base address register 1	DBAR1	R/W	R/W	32	24	H'FE2F FE28	H'FF8A
Destination address register 1	DAR1	R/W	R/W	32	24	H'FE2F FE2C	H'FF8B
Transfer count register 1	TCR1	R/W	R/W	32	24	H'FE2F FE30	H'FF8C
SHwy priority register 1	SHPRI1	R/W	R/W	32	24	H'FE2F FE34	H'FF8D
Channel control register 1	CHCR1	R/W	R/W	32	24	H'FE2F FE38	H'FF8E
Source base address register 2	SBAR2	R/W	R/W	32	24	H'FE2F FE40	H'FF90
Source address register 2	SAR2	R/W	R/W	32	24	H'FE2F FE44	H'FF91
Destination base address register 2	DBAR2	R/W	R/W	32	24	H'FE2F FE48	H'FF92
Destination address register 2	DAR2	R/W	R/W	32	24	H'FE2F FE4C	H'FF93
Transfer count register 2	TCR2	R/W	R/W	32	24	H'FE2F FE50	H'FF94
SHwy priority register 2	SHPRI2	R/W	R/W	32	24	H'FE2F FE54	H'FF95
Channel control register 2	CHCR2	R/W	R/W	32	24	H'FE2F FE58	H'FF96
Loop start address register 0	LSA0	R/W	R/W	32	24	H'FE2F FE80	H'FFA0
Loop end address register 0	LEA0	R/W	R/W	32	24	H'FE2F FE84	H'FFA1
Loop start address register 1	LSA1	R/W	R/W	32	24	H'FE2F FE90	H'FFA4
Loop end address register 1	LEA1	R/W	R/W	32	24	H'FE2F FE94	H'FFA5
Loop start address register 2	LSA2	R/W	R/W	32	24	H'FE2F FEA0	H'FFA8
Loop end address register 2	LEA2	R/W	R/W	32	24	H'FE2F FEA4	H'FFA9
DSP1 registers							
DSP full reset register	DSPRST	R/W	R	32	24	H'FE3F FD00	H'FF40
DSP core reset register	DSPCORERST	R/W	R	32	24	H'FE3F FD04	H'FF41
DSP hold register	DSPHOLD	R	R	32	24	H'FE3F FD08	H'FF42
DSP restart register	DSPRESTART	R/W	R	32	24	H'FE3F FD0C	H'FF43
CPU interrupt source mask register	IEMASKC	R/W	—	32	24	H'FE3F FD18	H'FF46
CPU interrupt signal mask register	IMASKC	R/W	—	32	24	H'FE3F FD1C	H'FF47

Register Name	Abbreviation	R/W		Access Size (Bit)		Physical Address	DSP Address
		CPU	DSP	CPU	DSP		
CPU interrupt source register	IEVENTC	R/W	—	32	24	H'FE3F FD20	H'FF48
DSP interrupt source mask register	IEMASKD	—	R/W	32	24	H'FE3F FD24	H'FF49
DSP interrupt signal mask register	IMASKD	—	R/W	32	24	H'FE3F FD28	H'FF4A
DSP interrupt set register	IESETD	R/W	R/W	32	24	H'FE3F FD2C	H'FF4B
DSP interrupt clear register	IECLRD	—	R/W	32	24	H'FE3F FD30	H'FF4C
DMAC operation register	OR	R/W	R/W	32	24	H'FE3F FD34	H'FF4D
CPU-DSP communication register 0	COM0	R/W	R/W	32	24	H'FE3F FD38	H'FF4E
CPU-DSP communication register 1	COM1	R/W	R/W	32	24	H'FE3F FD3C	H'FF4F
CPU-DSP communication register 2	COM2	R/W	R/W	32	24	H'FE3F FD40	H'FF50
CPU-DSP communication register 3	COM3	R/W	R/W	32	24	H'FE3F FD44	H'FF51
CPU-DSP communication register 4	COM4	R/W	R/W	32	24	H'FE3F FD48	H'FF52
CPU-DSP communication register 5	COM5	R/W	R/W	32	24	H'FE3F FD4C	H'FF53
CPU-DSP communication register 6	COM6	R/W	R/W	32	24	H'FE3F FD50	H'FF54
CPU-DSP communication register 7	COM7	R/W	R/W	32	24	H'FE3F FD54	H'FF55
Bus-through address high register	BTADRU	R/W	R/W	32	24	H'FE3F FD58	H'FF56
Bus-through address low register	BTADRL	R/W	R/W	32	24	H'FE3F FD5C	H'FF57
Bus-through write data high register	WDATU	R/W	R/W	32	24	H'FE3F FD60	H'FF58
Bus-through write data low register	WDATL	R/W	R/W	32	24	H'FE3F FD64	H'FF59
Bus-through read data high register	RDATU	R	R	32	24	H'FE3F FD68	H'FF5A
Bus-through read data low register	RDATL	R	R	32	24	H'FE3F FD6C	H'FF5B
Bus-through mode control register	BTCTRL	R	R/W	32	24	H'FE3F FD70	H'FF5C
SPU status register	SPUSTS	R	R	32	24	H'FE3F FD74	H'FF5D
Source base address register 0	SBAR0	R/W	R/W	32	24	H'FE3F FE00	H'FF80
Source address register 0	SAR0	R/W	R/W	32	24	H'FE3F FE04	H'FF81
Destination base address register 0	DBAR0	R/W	R/W	32	24	H'FE3F FE08	H'FF82
Destination address register 0	DAR0	R/W	R/W	32	24	H'FE3F FE0C	H'FF83
Transfer count register 0	TCR0	R/W	R/W	32	24	H'FE3F FE10	H'FF84
SHwy priority register 0	SHPRI0	R/W	R/W	32	24	H'FE3F FE14	H'FF85
Channel control register 0	CHCR0	R/W	R/W	32	24	H'FE3F FE18	H'FF86
Source base address register 1	SBAR1	R/W	R/W	32	24	H'FE3F FE20	H'FF88

Register Name	Abbreviation	R/W		Access Size (Bit)		Register Name	Abbreviation
		CPU	DSP	CPU	DSP		
Source address register 1	SAR1	R/W	R/W	32	24	H'FE3F FE24	H'FF89
Destination base address register 1	DBAR1	R/W	R/W	32	24	H'FE3F FE28	H'FF8A
Destination address register 1	DAR1	R/W	R/W	32	24	H'FE3F FE2C	H'FF8B
Transfer count register 1	TCR1	R/W	R/W	32	24	H'FE3F FE30	H'FF8C
SHwy priority register 1	SHPRI1	R/W	R/W	32	24	H'FE3F FE34	H'FF8D
Channel control register 1	CHCR1	R/W	R/W	32	24	H'FE3F FE38	H'FF8E
Source base address register 2	SBAR2	R/W	R/W	32	24	H'FE3F FE40	H'FF90
Source address register 2	SAR2	R/W	R/W	32	24	H'FE3F FE44	H'FF91
Destination base address register 2	DBAR2	R/W	R/W	32	24	H'FE3F FE48	H'FF92
Destination address register 2	DAR2	R/W	R/W	32	24	H'FE3F FE4C	H'FF93
Transfer count register 2	TCR2	R/W	R/W	32	24	H'FE3F FE50	H'FF94
SHwy priority register 2	SHPRI2	R/W	R/W	32	24	H'FE3F FE54	H'FF95
Channel control register 2	CHCR2	R/W	R/W	32	24	H'FE3F FE58	H'FF96
Loop start address register 0	LSA0	R/W	R/W	32	24	H'FE3F FE80	H'FFA0
Loop end address register 0	LEA0	R/W	R/W	32	24	H'FE3F FE84	H'FFA1
Loop start address register 1	LSA1	R/W	R/W	32	24	H'FE3F FE90	H'FFA4
Loop end address register 1	LEA1	R/W	R/W	32	24	H'FE3F FE94	H'FFA5
Loop start address register 2	LSA2	R/W	R/W	32	24	H'FE3F FEA0	H'FFA8
Loop end address register 2	LEA2	R/W	R/W	32	24	H'FE3F FEA4	H'FFA9

Table 50.4 Register States in Each Operating Mode

Register Abbreviation	Reset *	Module Standby
PBANKC0, 1	Initialized	Retained
XBANKC0, 1	Initialized	Retained
SPUSRST	Initialized	Retained
SPUADR	Initialized	Retained
ENDIAN	Initialized	Retained
GCOM0 to 7	Initialized	Retained
DMABUF0 to 3	Initialized	Retained
DSPRST	Initialized	Retained
DSPCORERST	Initialized	Retained
DSPHOLD*	Initialized	Retained
DSPRESTART	Initialized	Retained
IEMASKC	Initialized	Retained
IMASKC	Initialized	Retained
IEVENTC	Initialized	Retained
IEMASKD	Initialized	Retained
IMASKD	Initialized	Retained
IESETD	Initialized	Retained
IECLRD	Initialized	Retained
OR	Initialized	Retained
COM0 to 7	Initialized	Retained
BTADRU	Initialized	Retained
BTADRL	Initialized	Retained
WDATU	Initialized	Retained
WDATL	Initialized	Retained
RDATU	Initialized	Retained
RDATL	Initialized	Retained
BTCTRL	Initialized	Retained
SPUSTS	Initialized	Retained
SBAR0 to 2	Initialized	Retained

Register Abbreviation	Reset *	Module Standby
SAR0 to 2	Initialized	Retained
DBAR0 to 2	Initialized	Retained
DAR0 to 2	Initialized	Retained
TCR0 to 2*	Initialized	Retained
SHPRI0 to 2*	Initialized	Retained
CHCR0 to 2*	Initialized	Retained
LSA0 to 2*	Initialized	Retained
LEA0 to 2*	Initialized	Retained

Note: * Indicates the states of both DSP0/DSP1 registers.

Note: * For details, refer to section 1-D Overview reset.

50.2.1 PRAM Bank Control Register 0 (PBANKC0)

PBANKC0 is a 32-bit readable/writable register that controls which bank in the program memory (DSP0-PRAM) for one of the SPU2's on-chip DSPs (DSP0) is used. PBANKC0 can be written only by the CPU.

Each of this register indicates the availability of a bank that consists of 32 bits x 8 Kwords. If 1 is set in bit N, then it means DSP0 uses bank N. This product has 40 Kwords of program memory that can be used by DSP0 and DSP1. In the initial state, DSP0 is set to use all of the 40-Kword memory.

Do not set 1 in the same bit position of PBANKC0[4:0] and PBANKC1[4:0].

The register value should be changed after the CPU resets the DSP and before it clears the reset state.

For details, see section 50.3.3, DSP Memory Allocation.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	PBANKC0[4:0]				
Initial value:	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 5	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.
4 to 0	PBANKC0 [4:0]	H'1F	R/(W)*	PRAM Bank Control bits for DSP0 0: DSP0 does not use bank N. 1: DSP0 uses bank N.

Note: * Writable only by the CPU.

50.2.2 PRAM Bank Control Register 1 (PBANKC1)

PBANKC1 is a 32-bit readable/writable register that controls which bank in the program memory (DSP1-PRAM) for one of the SPU2's on-chip DSPs (DSP1) is used. PBANKC1 can be written only by the CPU.

Each of this register indicates the availability of a bank that consists of 32 bits × 8 Kwords. If 1 is set in bit N, then it means DSP1 uses bank N. This product has 40 Kwords of program memory that can be used by DSP0 and DSP1. In the initial state, DSP0 is set not to use any of the 40-Kword memory. Refer to the description of the PBANKC0 register to specify the bank to be used by DSP1.

The register value should be changed after the CPU resets the DSP and before it clears the reset state.

For details, see section 50.3.3, DSP Memory Allocation.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	PBANKC1[4:0]				
Initial value:	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 8	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4 to 0	PBANKC1 [4:0]	H'00	R/(W)*	PRAM Bank Control bits for DSP1 0: DSP1 does not use bank N. 1: DSP1 uses bank N.

Note: * Writable only by the CPU.

50.2.3 XRAM Bank Control Register 0 (XBANKC0)

XBANKC0 is a 32-bit readable/writable register that controls which bank in the X memory (DSP0-XRAM) for one of the SPU2's on-chip DSPs (DSP0) is used.

Each of this register indicates the availability of a bank that consists of 24 bits × 8 Kwords. If 1 is set in bit N, then it means DSP0 uses bank N. This product has 56 Kwords of memory that can be used by DSP0 and DSP1. In the initial state, DSP0 is set to use all of the 56-Kword memory.

Before the CPU changes the register value, it has to make sure that all of the SPU2's on-chip DSPs are ready for switching banks.

For details, refer to section 50.3.3, DSP Memory Allocation.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	XBANKC0[6:0]						
Initial value:	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
6 to 0	XBANKC0 [6:0]	H'7F	R/W	XRAM Bank Control bits for DSP0 0: DSP0 does not use bank N. 1: DSP0 uses bank N.

50.2.4 XRAM Bank Control Register 1 (XBANKC1)

XBANKC1 is a 32-bit readable/writable register that controls which bank in the X memory (DSP1-XRAM) for one of the SPU2's on-chip DSPs (DSP1) is used.

Each bit in this register indicates the availability of a bank that consists of 24 bits × 8 Kwords. If 1 is set in bit N, then it means DSP1 uses bank N. In the initial state, DSP1 is set not to use any bank. Refer to the description of the XBANKC0 register to specify the bank to be used by DSP1.

Before the CPU changes the register value, it has to make sure that all of the SPU2's on-chip DSPs are ready for switching banks.

For details, see section 50.3.3, DSP Memory Allocation.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	XBANKC1[6:0]						
Initial value:	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 8	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6 to 0	XBANKC1 [6:0]	H'00	R/W	XRAM Bank Control bits for DSP1 0: DSP1 does not use bank N. 1: DSP1 uses bank N.

50.2.5 SPU Software Reset Register (SPUSRST)

SPUSRST is a 32-bit readable/writable register that controls operation of the registers (SPU software reset) in the SPU.

When the SPUSRST bit is set to 0, the registers in the SPU2 are initialized. As these registers include the DSPRST and DSPCORERST registers, the DSP are also initialized.

When issuing a software reset by writing 0 to any bit in this register, read this register after the write to make sure the bit is written to 0, and then clear the reset by writing 1 to the bit.

When accessing a DSP as a SHwy target, set 1 to make the SPU2 operational. However, host access to SPU2 registers, such as to set the SPUSRST bit to 1 to clear the reset, is always guaranteed.

The BUF3SRST to BUF0SRST bits are software reset registers used to clear buffers for inter-DSP communication and are numbered according to the buffer number. For example, the BUF3SRST bit initializes the DMABUF3 register to 0.

When clearing buffers, reset after the DMA transfer on the channel that is used in an inter-DSP communication is stopped by interrupting the transfer or when it is complete.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	BUF3 SRST	BUF2 SRST	BUF1 SRST	BUF0 SRST	—	—	—	SPU SRST
Initial value:	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R/(W)*

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	BUF3SRST	1	R/W	DMABUF3 Software Reset bit 0: DMABUF3 is reset. 1: DMABUF3 operates normally.
6	BUF2SRST	1	R/W	DMABUF2 Software Reset bit 0: DMABUF2 is reset. 1: DMABUF2 operates normally.
5	BUF1SRST	1	R/W	DMABUF1 Software Reset bit 0: DMABUF1 is reset. 1: DMABUF1 operates normally.
4	BUF0SRST	1	R/W	DMABUF0 Software Reset bit 0: DMABUF0 is reset. 1: DMABUF0 operates normally.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	SPUSRST	1	R/(W)*	SPU2 Software Reset bit 0: SPU2 is reset. 1: SPU2 operates normally.

Note: * Writable only by the CPU.

50.2.6 SPU Address Register (SPUADR)

SPUADR is a 32-bit read-only register that indicates the upper 12 bits (bits 32 to 20) of the physical address of the SPU2.

The DSP can start the DMAC involving the DSP memory by setting the value read from this register in the SBAR or DBAR register (see the description later), even if the SPU2 mapping address varies depending on products. This allows the program more portable.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SPUADR[31:20]												—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 20	SPUADR [31:20]	—	R	SPU2 Mapping Address bits These bits indicate the upper 12 bits of the SPU2 mapping address.
19 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

50.2.7 SHwy Endian Register (ENDIAN)

ENDIAN is a 32-bit read-only register that indicates the endian of the SHwy. Reading this register returns the value specified by the MD5 pin in bit 0. This register is useful in cases such as if you want to change data swap methods for the SPU2's on-chip DMAC depending on the endian of the SHwy, allowing the program more portable.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ENDIAN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	ENDIAN	—	R	SHwy Endian bit This bit indicates the endian of the SHwy, which is specified by the MD5 pin. 0: The SHwy operates in big endian mode. 1: The SHwy operates in little endian mode.

50.2.8 Global Common Registers 0 to 7 (GCOM0 to 7)

GCOM0 to 7 are 32-bit readable/writable registers that can be controlled by the CPU and all of the SPU2's on-chip DSPs. These registers are mainly used as communication registers for inter-DSP communication.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	GCOMn[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GCOMn[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	GCOMn[23:0]	H'00 0000	R/W	Global Common bits (n=0 to 7) The CPU and all of the SPU2's on-chip DSP can control these bits to use mainly as communication registers for inter-DSP communication.

50.2.9 Internal Transfer Buffer Registers 0 to 3 (DMABUF0 to 3)

DMABUF0 to 3 are read-only registers that are used as temporary buffers for DMA transfers (inter-DSP transfers) within the SPU2 without using the SHwy.

When an inter-DSP transfer is performed by setting the IM1 bit in the CHCR register to 1, the address of this register should be specified as the source or destination address. The CHCR.DAM or CHCR.SAM bit should also be set to 1 to fix the address.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	BUFn[23:8]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BUFn[7:0]								—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 8*	BUFn[23:0]	H'00 0000	R	Buffer for intra-SPU2 DMA transfer (n=0 to 3) When a DMA transfer is performed within the SPU2 without using the SHwy by setting the CHCRn.IM bit to 1, the address of this register should be specified as the source or destination address.
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Note: * DSP: 23 to 0

Two DMA channels should be used for inter-DSP transfers. For example, if inter-DSP communication is to be performed from DSP0-XRAM to DSP1-XRAM as shown in figure 50.2, both DMAC0 and DMAC1 should be started. The source and destination addresses should be set as shown in table 50.5.

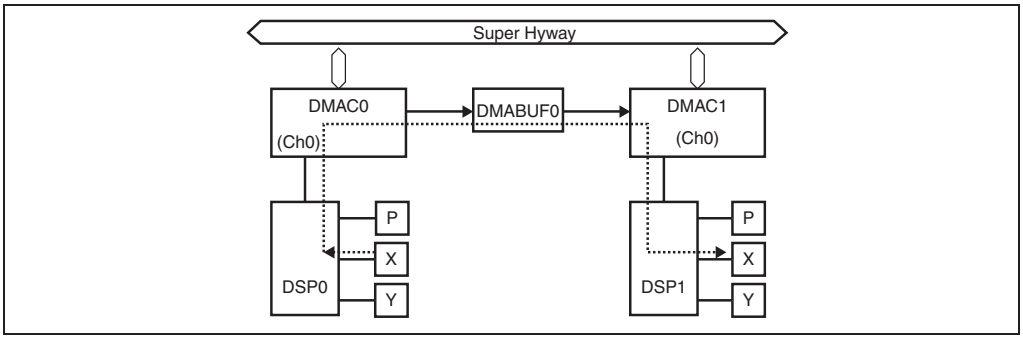


Figure 50.2 Example of Inter-DSP Transfer

Table 50.5 Example of Inter-DSP Communication Setting

Example of Setting for Transfer from DSP0-XRAM to DSP1-XRAM (SHwy Bypassed)	Source Address (SBAR00, SAR00)	Destination Address (DBAR01, DAR01)
DMAC0 CH0	DSP0-XRAM	DMABUF0/1/2/3 (fixed)
DMAC1 CH0	DMABUF0/1/2/3 (fixed)	DSP1-XRAM

50.2.10 DSP Full Reset Register (DSPRST)

DSPRST is a 32-bit readable/writable register. Only the CPU can write to this register.

The SPU2's on-chip DSP has two reset control bits, the DSPRST bit in this register and the DSPCORERST bit in the DSPCORERST register, that can be used to control DSP full reset and DSP core reset respectively.

The SPU2's on-chip DSP can be divided into DSP core, DSP memory shell, and DSP debug module. While the DSPRST bit in this register is 1, all FFs in them except the DSP debug module are initialized.

While this bit is 1, the DSP memory shell is also initialized and the DSP-P/X/YRAM cannot be accessed. Therefore, when downloading a DSP program, set this bit to 0 to clear the DSP initialized state. When doing it, however, do not write 0 to the DSPCORERST register described below.

Note that setting this register to 1 does not initialize the DMAC control registers such as SAR or CHCR and the SPU2 registers such as DSP-CPU communication registers (e.g. COM0). These registers must be initialized individually.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DSP RST
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/(W)*

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	DSPRST	1	R/(W)*	DSPn Reset bit 0: Activates the DSP (i.e., clears the DSP reset). 1: Resets the DSP.

Note: * Writable only by the CPU.

50.2.11 DSP Core Reset Register (DSPCORERST)

DSPCORERST is a 32-bit readable/writable register. Only the CPU can write to this register.

The SPU2's on-chip DSP can be divided into DSP core, DSP memory shell, and DSP debug module. While the DSPCORERST bit is 1, only the DSP core is initialized.

While this bit is 1, the DSP memory shell is not initialized and DSP memory access such as to download DSP programs is still available. To reset when downloading them, follow the steps below.

1. Initial sate (after a power-on reset)
   DSPRST = 1 (DSP full reset)
   DSPCORERST = 1
2. DSP reset control 1
   DSPRST = 0 (clear the DSP full reset.)
   DSPCORERST = 1 (initial value: initializes the DSP core only.)
   Download the desired data to the DSP-P/X/Y.
3. DSP reset control 2
   DSPRST = 0 (clear the DSP full reset.)
   DSPCORERST = 0 (clear the DSP core reset, start a program fetch.)

Note that similarly to the DSPRST register, setting the DSPCORERST register to 1 does not initialize the DMAC control registers such as SAR or CHCR and the SPU2 registers such as DSP-CPU communication registers (e.g. COM0). These registers must be initialized individually.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DSPCORERST
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/(W)*

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	DSPCORERST	1	R/(W)*	DSP Core Reset bit 0: Activates the DSP core (i.e., clears the DSP core reset). 1: Resets the DSP core.

Note: * Writable only by the CPU.

50.2.12 DSP Hold Register (DSPHOLD)

DSPHOLD is a 32-bit read-only register. The STOP_ACK bit indicates the DSP core status.

The HOLD_ACK bit is the acknowledge status of the hold request when the DSP makes access with wait state to I/O peripheral modules. When this bit is 1, the DSP is in hold state.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	STOP_ACK	—	—	—	HOLD ACK	—	—	—	—
Initial value:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	STOP_ACK	1	R	STOP Acknowledge bit This bit is set when the DSP core is reset. 0: The DSP core is normal. 1: The DSP core is reset.
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	HOLD_ACK	0	R	DSP Hold Acknowledge bit 0: The DSP core is active. 1: The DSP core is in hold state.
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

50.2.13 DSP Restart Register (DSPRESTART)

DSPRESTART is a 32-bit readable/writable register. Only the CPU can write to this register.

The HALT_ACK bit is set to 1 when the DSP is in halt state. To clear this halt state, set the RESTART bit to 1. When the DSP detects the restart signal and the halt signal from the DSP is negated, the RESTART bit is automatically updated to 0.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	RE START	—	—	—	HALT _ACK
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/(W)*	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	RESTART	0	R/(W)*	DSP Restart bit This bit can be used to clear the DSP halt state. 0: Does not restart the DSP. 1: Restarts the DSP.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	HALT_ACK	0	R	DSP Halt Acknowledge bit 0: The DSP is active. 1: The DSP is in halt state.

Note: * Writable only by the CPU.

50.2.14 CPU Interrupt Source Mask Register (IEMASKC)

IEMASKC is a 32-bit readable/writable register that masks various interrupt sources to the CPU individually. If this register masks an interrupt source, the interrupt source is not enabled even if the corresponding interrupt is unmasked by the IMASKC register described later. Thus, the interrupt does not occur.

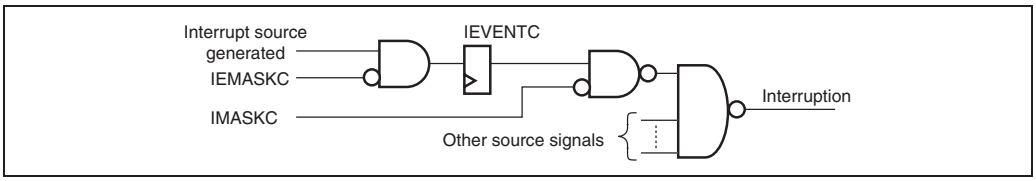


Figure 50.3 CPU Interrupt Source Mask

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	DSPIE MASKC	—	—	—	CH2IE MASKC	—	—	—	CH1IE MASKC	—	—	—	CH0IE MASKC
Initial value:	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
R/W:	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	DSPIEMASKC	1	R/W	Mask bit for the source of the DSP register setting interrupt to the CPU Set this bit to 0 when the DSPIEVENTC bit in the IEVENTC register should be set. 0: Does not mask the interrupt source (i.e., enables the interrupt source). 1: Masks the interrupt source (i/e., disables the interrupt source).

Bit	Bit Name	Initial Value	R/W	Description
11 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	CH2IEMASKC	1	R/W	Mask for the source of the CH2 transfer end interrupt related to CPU interrupt Set this bit to 0 when the interrupt source should be generated after CH2 DMA transfer is complete. 0: Does not mask the interrupt source (i.e., enables the interrupt source). 1: Masks the interrupt source (i.e., disables the interrupt source).
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	CH1IEMASKC	1	R/W	Mask for the source of the CH1 transfer end interrupt related to CPU interrupt Set this bit to 0 when the interrupt source should be generated after CH1 DMA transfer is complete. 0: Does not mask the interrupt source (i.e., enables the interrupt source). 1: Masks the interrupt source (i.e., disables the interrupt source).
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	CH0IEMASKC	1	R/W	Mask for the source of the CH0 transfer end interrupt related to CPU interrupt Set this bit to 0 when the interrupt source should be generated after CH0 DMA transfer is complete. 0: Does not mask the interrupt source (i.e., enables the interrupt source). 1: Masks the interrupt source (i.e., disables the interrupt source).

50.2.15 CPU Interrupt Signal Mask Register (IMASKC)

IMASKC is a 32-bit readable/writable register that masks various interrupts to the CPU individually.

To generate an interrupt request signal for an interrupt source, set the related bit in this register to 0 and also set the related mask bit in the IEMASKC register above to 0. If the IEMASKC register masks an interrupt source, the interrupt request signal does not occur even if the IMASKC register unmasks the interrupt signal.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	DSPI MASKC	—	—	—	CH2I MASKC	—	—	—	CH1I MASKC	—	—	—	CH0I MASKC
Initial value:	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
R/W:	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	DSPIMASKC	1	R/W	Mask bit for the DSP register setting interrupt to the CPU If the DSP set the DSPEVENTC bit in the IEVNTC register to 1 and also sets this mask bit to 0, then the interrupt request is generated to the CPU. 0: Does not mask the interrupt (i.e., enables the interrupt request signal). 1: Masks the interrupt (i.e., disables the interrupt request signal).
11 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	CH2IMASKC	1	R/W	Mask bit for the CH2 transfer end interrupt 0: Does not mask the interrupt (i.e., enables the interrupt request signal). 1: Masks the interrupt (i.e., disables the interrupt request signal).

Bit	Bit Name	Initial Value	R/W	Description
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	CH1IMASKC	1	R/W	Mask bit for the CH1 transfer end interrupt 0: Does not mask the interrupt (i.e., enables the interrupt request signal). 1: Masks the interrupt (i.e., disables the interrupt request signal).
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	CH0IMASKC	1	R/W	Mask bit for the CH0 transfer end interrupt 0: Does not mask the interrupt (i.e., enables the interrupt request signal). 1: Masks the interrupt (i.e., disables the interrupt request signal).

50.2.16 CPU Interrupt Source Register (IEVENTC)

IEVENTC is a 32-bit readable/writable register that indicates the source of an interrupt to the CPU. The CPU can only clear the register to 0. Even it attempts to write 1 to the register, the register remains unchanged. When using the interrupt handler to clear the interrupt source related to one CHIEVENTC bit, set the other CHIEVENTC bits to 1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	DSPIEVENTC	—	—	—	CH2IEVENTC	—	—	—	CH1IEVENTC	—	—	—	CH0IEVENTC
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	DSPIEVENTC	0	R/W*1	Source of the DSP register setting interrupt to the CPU Only the DSP can write to this bit. If the IEMASKC and IMASKC registers cancel the mask and the DSP sets this bit to 1, the interrupt request is generated to the CPU. The CPU can write nothing but 0. 0: The DSP register setting interrupt is not generated. 1: The DSP register setting interrupt is generated.
11 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	CH2IEVENTC	0	R/W*2	Source of the CH2 transfer end interrupt 0: The CH2 transfer end interrupt is not generated. 1: The CH2 transfer end interrupt is generated.
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
4	CH1IEVENTC	0	R/W*2	Source of the CH1 transfer end interrupt 0: The CH1 transfer end interrupt is not generated. 1: The CH1 transfer end interrupt is generated.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	CH0IEVENTC	0	R/W*2	Source of the CH0 transfer end interrupt 0: The CH0 transfer end interrupt is not generated. 1: The CH0 transfer end interrupt is generated.

Note: *1 Only the DSP can write 1 to the DSPIEVENTC bit. The CPU can only clear it to 0.
*2 The CPU can only clear the CHIEVENTC bits to 0. Even if it attempts to write 1 to these bits, they remain unchanged.

50.2.17 DSP Interrupt Source Mask Register (IEMASKD)

IEMASKD is a 32-bit readable/writable register that masks various interrupt sources to the DSP individually. If this register masks an interrupt source, the interrupt source is not enabled even if the IMASKD register described later unmasks the interrupt. Thus, that interrupt does not occur.

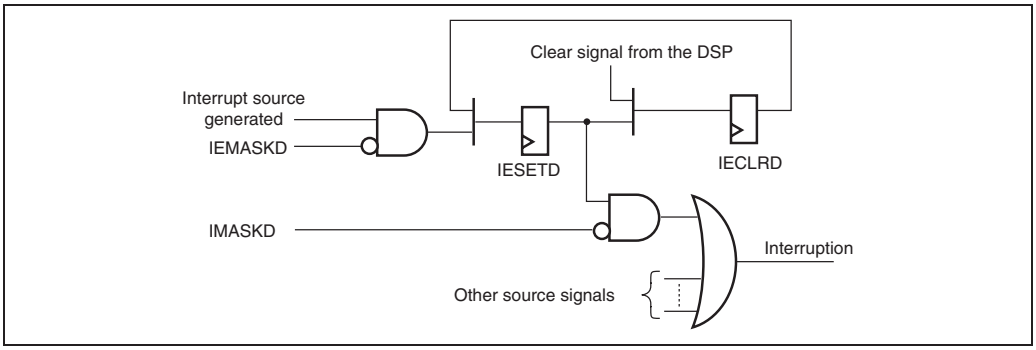


Figure 50.4 DSP Interrupt Source Mask

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	DSP1IE MASKD	DSP0IE MASKD	—	—	—	CPUIE MASKD
Initial value:	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	BTIE MASKD	—	—	—	CH2IE MASKD	—	—	—	CH1IE MASKD	—	—	—	CH0IE MASKD
Initial value:	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
R/W:	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23, 22	—	11	R	Reserved These bits are always read as 1. The write value should always be 1.

Bit	Bit Name	Initial Value	R/W	Description
21	DSP1IE MASKD	1	R/W	Mask bit for the source of the CPU register setting interrupt from DSP1 0: Does not mask the interrupt source (i.e., enables the interrupt source). 1: Masks the interrupt source (i.e., disables the interrupt source).
20	DSP0IE MASKD	1	R/W	Mask bit for the source of the CPU register setting interrupt from DSP0 0: Does not mask the interrupt source (i.e., enables the interrupt source). 1: Masks the interrupt source (i.e., disables the interrupt source).
19 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	CPUIE MASKD	1	R/W	Mask bit for the source of the register setting interrupt related to DSP interrupt To set the CPUIEVENTD bit in the IEVENTD register, set this mask bit to 0. 0: Does not mask the interrupt source (i.e., enables the interrupt source). 1: Masks the interrupt source (i.e., disables the interrupt source).
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	BTIE MASKD	1	R/W	Mask bit for the source of the bus-through access end interrupt related to DSP To generate the interrupt source after the completion of bus-through access, set this mask bit to 0. 0: Does not mask the interrupt source (i.e., enables the interrupt source). 1: Masks the interrupt source (i.e., disables the interrupt source).
11 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
8	CH2IE MASKD	1	R/W	Mask bit for the source of the CH2 transfer end interrupt related to DSP interrupt To generate the interrupt source after the completion of CH2 DMA transfer, set this mask bit to 0. 0: Does not mask the interrupt source (i.e., enables the interrupt source). 1: Masks the interrupt source (i.e., disables the interrupt source).
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	CH1IE MASKD	1	R/W	Mask bit for the source of the CH1 transfer end interrupt related to DSP interrupt To generate the interrupt source after the completion of CH1 DMA transfer, set this mask bit to 0. 0: Does not mask the interrupt source (i.e., enables the interrupt source). 1: Masks the interrupt source (i.e., disables the interrupt source).
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	CH0IE MASKD	1	R/W	Mask bit for the source of the CH1 transfer end interrupt related to DSP interrupt To generate the interrupt source after the completion of CH0 DMA transfer, set this mask bit to 0. 0: Does not mask the interrupt source (i.e., enables the interrupt source). 1: Masks the interrupt source (i.e., disables the interrupt source).

50.2.18 DSP Interrupt Mask Register (IMASKD)

IMASKD is a 32-bit readable/writable register that masks various interrupts to the DSP individually.

To generate an interrupt request signal for an interrupt source, set the related source bit in this register to 0 and also set the related source mask bit in the IEMASKD register above to 0. If the IEMASKD register masks an interrupt source, the interrupt request signal does not occur even if the IMASKD register clears the interrupt mask.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	DSP1IMASKD	DSP0IMASKD	—	—	—	CPUIMASKD
Initial value:	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	BTIMASKD	—	—	—	CH2IMASKD	—	—	—	CH1IMASKD	—	—	—	CH0IMASKD
Initial value:	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
R/W:	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23, 22	—	11	R	Reserved These bits are always read as 1. The write value should always be 1.
21	DSP1IMASKD	1	R/W	Mask bit for the register setting interrupt signal to the DSP from DSP1 0: Does not mask the interrupt source (i.e., enables the interrupt source). 1: Masks the interrupt source (i.e., disables the interrupt source).
20	DSP0IMASKD	1	R/W	Mask bit for the register setting interrupt signal to the DSP from DSP0 0: Does not mask the interrupt source (i.e., enables the interrupt source). 1: Masks the interrupt source (i.e., disables the interrupt source).

Bit	Bit Name	Initial Value	R/W	Description
19 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	CPUIMASKD	1	R/W	Mask bit for the CPU register setting interrupt to the DSP If the DSP sets the CPUEVENTD bit in the IEVENTD register to 1 and also sets this mask bit to 0, then the interrupt request is generated to the CPU. 0: Does not mask the interrupt (i.e., enables the interrupt request signal). 1: Masks the interrupt (i.e., disables the interrupt request signal).
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	BTIMASKD	1	R/W	Mask bit for the bus-through access end interrupt related to DSP interrupt 0: Does not mask the interrupt (i.e., enables the interrupt request signal). 1: Masks the interrupt (i.e., disables the interrupt request signal).
11 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	CH2IMASKD	1	R/W	Mask bit for the CH2 transfer end interrupt 0: Does not mask the interrupt (i.e., enables the interrupt request signal). 1: Masks the interrupt (i.e., disables the interrupt request signal).
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
4	CH1IMASKD	1	R/W	Mask bit for the CH1 transfer end interrupt 0: Does not mask the interrupt (i.e., enables the interrupt request signal). 1: Masks the interrupt (i.e., disables the interrupt request signal).
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	CH0IMASKD	1	R/W	Mask bit for the CH0 transfer end interrupt 0: Does not mask the interrupt (i.e., enables the interrupt request signal). 1: Masks the interrupt (i.e., disables the interrupt request signal).

50.2.19 DSP Interrupt Set Register (IESETD)

IESETD is a 32-bit readable/writable register that indicates the source of an interrupt to the DSP. When using the interrupt handler to clear an interrupt source, this register is updated by writing 0 to each bit of the IECLRD register.

When an interrupt whose source can be identified by this register occurs, int[2] of the interrupt signal int[2:0] to the DSP is asserted. If int[2] is asserted and the DSP accepts it, the DSP program counter jumps to the interrupt vector irq3 to handle the interrupt.

Similarly to int[2], interrupts to the DSP from SPU2 peripheral modules are assigned to int[1:0] and these interrupts are handled by jumping to irq2 with int[1] and to irq1 with int[0].

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	DSP1IE SETD	DSP0IE SETD	—	—	—	CPUIE SETD
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/(W)*	R/(W)*	R	R	R	R/(W)*

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	BTIE SETD	—	—	—	CH2IE SETD	—	—	—	CH1IE SETD	—	—	—	CH0IE SETD
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
21	DSP1IESETD	0	R/(W)*	Source bit of the register setting interrupt from DSP1 0: The register setting interrupt to the DSP is not generated by DSP1. 1: The register setting interrupt to the DSP is generated by DSP1.
20	DSP0IESETD	0	R/(W)*	Source bit of the register setting interrupt from DSP0 0: The register setting interrupt to the DSP is not generated by DSP0. 1: The register setting interrupt to the DSP is generated by DSP0.
19 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	CPUIESETD	0	R/(W)*	Source of the CPU register setting interrupt to the DSP Only the CPU can write to this bit. When the IEMASKD and IMASKD registers clear the masks and the CPU sets this bit to 1, the interrupt request is generated to the DSP. 0: The CPU register setting interrupt is not generated. 1: The CPU register setting interrupt is generated.
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	BTIESETD	0	R/W	Source of the bus-through access end interrupt 0: The bus-through access end interrupt is not generated. 1: The bus-through access end interrupt is generated.

Bit	Bit Name	Initial Value	R/W	Description
11 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	CH2IESETD	0	R/W	Source of the CH2 transfer end interrupt 0: The CH2 transfer end interrupt is not generated. 1: The CH2 transfer end interrupt is generated.
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	CH1IESETD	0	R/W	Source of the CH1 transfer end interrupt 0: The CH1 transfer end interrupt is not generated. 1: The CH1 transfer end interrupt is generated.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	CH0IESETD	0	R/W	Source of the CH0 transfer end interrupt 0: The CH0 transfer end interrupt is not generated. 1: The CH0 transfer end interrupt is generated.

Note: * Each DSP can write 1 to the DSPnIESETD bit only. It should write 1 to the DSPnIESETD bit corresponding the number of the DSP to which an interrupt request should be sent. Even if it writes 0 to the bit, the bit value remains unchanged (0 is no written). Only the CPU can write 1 to the CPUIESETD bit. Even if it writes 0 to the bit, the bit value remains unchanged (0 is no written).

50.2.20 DSP Interrupt Clear Register (IECLRD)

IECLRD is a 32-bit readable/writable register that is used to clear the source of an interrupt to the DSP. To clear an interrupt source with the interrupt handler, write 0 to the bit related to that source and also write 1 to the other bits. If you write 0 to a bit not related to that source, an inappropriate interrupt source might be cleared.

Only one source can be cleared at a time. Even if interrupts by more than one interrupt source are detected by reading this register, clear only one source, perform the processing related to the source, and then return to the main routine. In this case, another interrupt should be detected immediately after returning to the main routine. If you clear more than one source at a time, more interrupts are to be generated than expected and interrupts without interrupt sources may be detected.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	DSP1IECLRD	DSP0IECLRD	—	—	—	CPUIECLRD
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/(W)*	R/(W)*	R	R	R	R/(W)*

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	BTIECLRD	—	—	—	CH2IECLRD	—	—	—	CH1IECLRD	—	—	—	CH0IECLRD
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/(W)*	R	R	R	R/(W)*	R	R	R	R/(W)*	R	R	R	R/(W)*

Bit	Bit Name	Initial Value	R/W	Description
31 to 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
21	DSP1IECLRD	0	R/(W)*	Bit for clearing the source of the register setting interrupt to the DSP from DSP1 0: The register setting interrupt to the DSP from DSP1 is absent (cleared). 1: The register setting interrupt to the DSP from DSP1 is present.
20	DSP0IECLRD	0	R/(W)*	Bit for clearing the source of the register setting interrupt to the DSP from DSP0 0: The register setting interrupt to the DSP from DSP0 is absent (cleared). 1: The register setting interrupt to the DSP from DSP0 is present.

Bit	Bit Name	Initial Value	R/W	Description
19 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	CPUIECLRD	0	R/(W)*	Bit for clearing the source of the CPU register setting interrupt to the DSP 0: The CPU register setting interrupt is absent (cleared). 1: The CPU register setting interrupt is present.
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	BTIECLRD	0	R/(W)*	Bit for clearing the source of the bus-through access end interrupt 0: The bus-through access end interrupt is absent (cleared). 1: The bus-through access end interrupt is present.
11 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	CH2IECLRD	0	R/(W)*	Bit for clearing the source of the CH2 transfer end interrupt destined to the DSP. 0: The CH2 transfer end interrupt is absent (cleared). 1: The CH2 transfer end interrupt is present.
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	CH1IECLRD	0	R/(W)*	Bit for clearing the source of the CH1 transfer end interrupt destined to the DSP. 0: The CH1 transfer end interrupt is absent (cleared). 1: The CH1 transfer end interrupt is present.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
0	CH0IECLRD	0	R/(W)*	Bit for clearing the source of the CH0 transfer end interrupt destined to the DSP. 0: The CH0 transfer end interrupt is absent (cleared). 1: The CH0 transfer end interrupt is present.

Note: * Only writing 0 is reflected on each DSP. Write 0 to the bit related to the source to be cleared and write 1 to the other bits. Only one source can be cleared at a time.

50.2.21 DMAC Operation Register (OR)

OR is a 32-bit readable/writable register that includes the master enable bit to control all transfer channels apart from the CHCR.DE bit that enables or disables one channel at a time.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DME
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	DME	0	R/W	DMA Master Enable This bit enables or disables all transfer channels. 0: Disables all transfer channels. 1: Enables all transfer channels.

50.2.22 CPU-DSP Communication Registers 0 to 7 (COM0 to 7)

COM0 to COM7 are 32-bit readable/writable registers that are used for communication between the CPU and the DSP. Both of them can write to these registers. These registers contain 192 bits (24 bits x 8) whose usages are defined according to system-specific needs. These register values do not affect to the SPU2 operation at all.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	COMn[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	COMn[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	COMn[23:0]	H'00 0000	R/W	Bits for communication between the CPU and the DSP (n = 0 to 7) These bits can be defined for communication between the CPU and the DSP.

50.2.23 Bus-Through Address High Register (BTADRU)

BTADRU is a 32-bit readable/writable register that specifies the upper address when the DSP accesses SPU2 external registers or SDRAM. This upper address is concatenated with the lower address specified in the BTADRL register below to access the SPU2 external space.

For details, see 50.2.29, Bus-Through Mode Control Register (BTCTRL).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BTADR[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 0	BTADR[31:16]	H'0000	R/W	Upper bits of the bus-through address These bits specify the upper address (16 bits) when the DSP accesses the SPU2 external space in bus-through mode.

50.2.24 Bus-Through Address Low Register (BTADRL)

BTADRL is a 32-bit readable/writable register that specifies the lower address when the DSP accesses SPU2 external registers or SDRAM. This lower address is concatenated with the upper address specified in the BTADRU register above to access the SPU2 external space.

For details, see section, 50.2.29 Bus-Through Mode Control Register (BTCTRL).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BTADR[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 0	BTADR[15:0]	H'0000	R/W	Lower bits of the bus-through address These bits specify the lower address (16 bits) when the DSP accesses the SPU2 external space in bus-through mode.

50.2.25 Bus-Through Write Data High Register (WDATU)

WDATU is a 32-bit readable/writable register that specifies the upper bits of write data when the DSP makes write access to SPU2 external registers or SDRAM.. These upper bits of data are concatenated with the lower bits of data specified in the WDATL register below to make write access to the SPU2 external space.

For details, see section 50.2.29, Bus-Through Mode Control Register (BTCTRL).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WDAT[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 0	WDAT[31:16]	H'0000	R/W	Upper bits of write data in bus-through write mode These bits specify the upper 16 bits of write data when the DSP makes 32-bit write access to the SPU2 external space in bus-through mode.

50.2.26 Bus-Through Write Data Low Register (WDATL)

WDATL is a 32-bit readable/writable register that specifies the lower bits of write data when the DSP makes write access to SPU2 external registers or SDRAM.. These lower bits of write data are concatenated with the upper bits of write data specified in the WDATU register above to make write access to the SPU2 external space.

For details, see section 50.2.29, Bus-Through Mode Control Register (BTCTRL).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WDAT[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 0	WDAT[15:0]	H'0000	R/W	Lower bits of write data in bus-through write mode These bits specify the lower 16 bits of write data when the DSP makes 32-bit write access to the SPU2 external space in bus-through mode. For 32-bit access: Specify the lower 16 bits of 32-bit data. For 16-bit access: Specify 16 bits. For 8-bit access: Specify 8 bits in bits[7:0].

50.2.27 Bus-Through Read Data High Register (RDATU)

RDATU is a 32-bit read-only register that contains the upper bits of read data when the DSP makes 32-bit read access to the SPU2 external registers or SDRAM.

For details, see section 50.2.29, Bus-Through Mode Control Register (BTCTRL).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RDAT[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 0	RDAT{31:16}	H'0000	R	Upper bits of read data in bus-through read mode These bits contain the upper 16 bits of read data when the DSP makes 32-bit read access to the SPU2 external space in bus-through mode.

50.2.28 Bus-Through Read Data Low Register (RDATL)

RDATL is a 32-bit read-only register that contains the lower bits of read data when the DSP makes 32-bit read access to the SPU2 external registers or SDRAM and the whole read data bits when it makes 16-/8-bit read access.

For details, see section 50.2.29, Bus-Through Mode Control Register (BTCTRL).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RDAT[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 0	RDAT[15:0]	H'0000	R	Lower bits of read data in bus-through read mode These bits contain the lower 16 bits of read data when the DSP makes 32-bit read access to the SPU2 external space and contain the whole read data bits when it makes 16-/8-bit access in bus-through mode. In 8-bit read access, bit 8 out of bits[15:8] is updated to 0 and read data are contained in bits[7:0].

50.2.29 Bus-Through Mode Control Register (BTCTRL)

BTCTRL is a register that can be read and written only by the DSP, which controls bus-through mode. The CPU can only read it. Bus-through mode refers to the way in which the DSP accesses the SPU2 external registers or SDRAM.

This register controls the type (read/write) and size of access in bus-through mode.

Write 1 to either of the BTR or BTW bit at a time. When the desired access is complete after writing 1 to the bit, it returns to 0 automatically.

In read access, the BTR bit returns to 0 automatically when the RDATU/RDATL register stores the read data.

In write access, the BTW bit returns to 0 automatically when the response packet to the store access to the Super Hyway is received. Therefore, you should read the data at the same address as the target write access in order to make sure if the write data is written completely.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	BTS[1:0]		—	—	—	—	—	—	—	BTW	—	—	—	BTR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/(W)*	R/(W)*	R	R	R	R	R	R	R	R/(W)*	R	R	R	R/(W)*

Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13, 12	BTS[1:0]	00	R/(W)*	These bits specify the access size in bus-through mode. 00: 32 bits (LOAD4/STORE4) 01: 16 bits (LOAD2/STORE2) 10: 8 bits (LOAD1/STORE1) 11: Setting prohibited
11 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
4	BTW	0	R/(W)*	Control bit for write access in bus-through mode Do not set this bit and the BTR bit to 1 at a time. Also, do not set this bit to 1 when the BTR bit is 1. 0: No write access is in progress or the write access is complete. 1: Starts a write access or the write access is in progress.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	BTR	0	R/(W)*	Control bit for read access in bus-through mode Do not set this bit and the BTW bit to 1 at a time. Also, do not set this bit to 1 when the BTW bit is 1. 0: No read access is in progress or the read access is complete. 1: Starts a read access or the read access is in progress.

Note: * Writable only by the DSP.

Figure 50.5 shows a flow chart of a memory access in bus-through mode. If you do not need to make sure if the data is written completely in write access, you can perform other processing after writing 1 to the BTW bit in the BTCTL register.

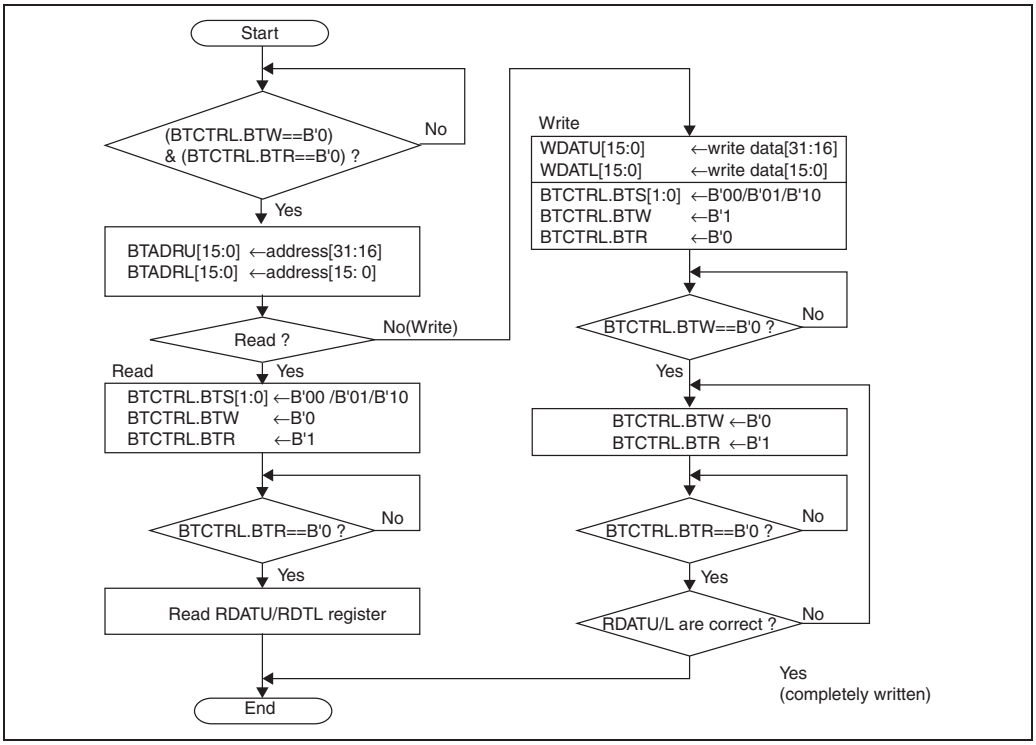


Figure 50.5 Flow Chart of Accessing SPU2 External Space in Bus-Through Mode (Example of Polling Register)

50.2.30 SPU Status Register (SPUSTS)

SPUSTS is a 32-bit read-only register. By reading this register, you can check the DMA transfer status and determine if there is any ongoing bus-through access at the time when it is read.

The DMA_ON bit is 1 while there is ongoing DMA transfer or bus-through access from the DSP to the SPU2 external space. To check if DMA transfer is stopped after setting the DME bit in the OR register or the DE bit in the CHCR register (that corresponds to the channel to stop) to 0, confirm that the DMA_ON bit is set to 0. To check that for a specific channel, confirm also that the CH_SEL bit is set to B'11.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	DMA_ON	CH_SEL[1:0]		BT_ON	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 23	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
22	DMA_ON	0	R	DMA Enable 0: No DMA transfer. 1: DMA/BT transfer is present (DMA transfer or bus-through access in progress).
21, 20	CH_SEL[1:0]	00	R	DMA Channel 00: CH0 DMA transfer in progress 01: CH1 DMA transfer in progress 10: CH2 DMA transfer in progress 11: No DMA transfer, or bus-through access in progress
19	BT_ON	0	R	DMA Enable 0: No bus-through access. 1: Bus-through access is present (bus-through in progress).

Bit	Bit Name	Initial Value	R/W	Description
18 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

50.2.31 Source Base Address Register 0 to 2 (SBAR0 to 2)

SBARn is a 32-bit readable/writable register that consists of the source base address bits SBARn[8:0] that specify the upper9 bits of the source address for DMA transfer.

DSPn reads from/writes to the upper 24 bits in this register. Do not specify addresses in the P2 space. Specifying H'Axxx xxxx is considered an error by the SHwy packet router and the transfer fails (specify H'0xxx xxxx instead).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SBARn[8:0]									—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 23[*1]	SBARn[8:0]	H'000	R/W	Source base address bits for specifying the upper 9 bits of the source address. Note that transfer of data which is continuous across an 8-Mbyte boundary in memory space is impossible. A write is prohibited during DMA transfer.
22 to 0[*2]	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Note: *1 DSP: 23 to 15
*2 DSP: 14 to 0

50.2.32 Source Address Registers 0 to 2 (SAR0 to 2)

SARn is a 32-bit readable/writable register that consists of the source address bits SARn[22:2] that specify the bits [22:2] of the source address for DMA transfer. It supported only data transfer that are performed in 4- or 32-byte units.

Note that transfer of data which is continuous across an 8-Mbyte boundary in memory space is impossible.

To use the source as a ring buffer, set the address within the ring buffer in this register.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	SARn[22:16]						
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SARn[15:2]														—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 23	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
22 to 2	SARn[22:2]	H'00 0000	R/W	Source base address bits for specifying the bits [22:2] of the source address. Note that transfer of data which is continuous across an 8-Mbyte boundary in memory space is impossible. A write is prohibited during DMA transfer.
1, 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

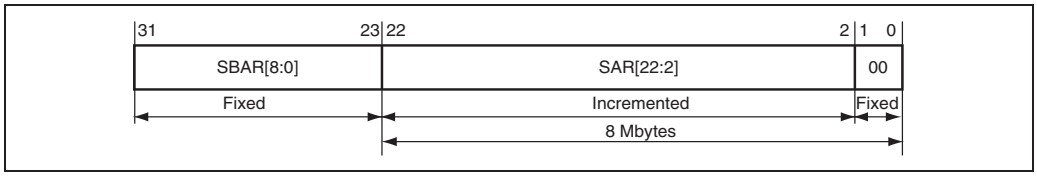


Figure 50.6 Source Address Configuration

50.2.33 Destination Base Address Registers 0 to 2 (DBAR0 to 2)

DBARn is 32-bit readable/writable registers that consists of the destination base address bits DBARn[8:0] that specify the upper 9 bits of the destination address for DMA transfer.

DSPn reads from/writes to the upper 24 bits in this register.

Do not specify addresses in the P2 space. Specifying H'Axxx xxxx is considered an error by the SHwy packet router and the transfer fails (specify H'0xxx xxxx instead).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DBARn[8:0]									—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 23*1	DBARn[8:0]	H'000	R/W	Destination Base Address bits for specifying the upper 9 bits of the destination address. Note that transfer of data which is continuous across an 8-Mbyte boundary in memory space is impossible. A write is prohibited during DMA transfer.
22 to 0*2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Note: *1 DSP: 23 to 15
*2 DSP: 14 to 0

50.2.34 Destination Address Registers 0 to 2 (DAR0 to 2)

DARn is a 32-bit readable/writable register that consists of the destination address bits DARn[22:2] that specify the bits [22:2] of the destination address for DMA transfer. It supported only data transfer that are performed in 32-bit or 32-byte units.

Note that transfer of data which is continuous across an 8-Mbyte boundary in memory space is impossible.

To use the destination as a ring buffer, set the address within the ring buffer in this register.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	DARn[22:16]						
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DARn[15:2]														—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 23	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
22 to 2	DARn[22:0]	H'00 0000	R/W	Destination Base Address bits for specifying the bits [22:2] of the destination address. Note that transfer of data which is continuous across an 8-Mbyte boundary in memory space is impossible. A write is prohibited during DMA transfer.
1, 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

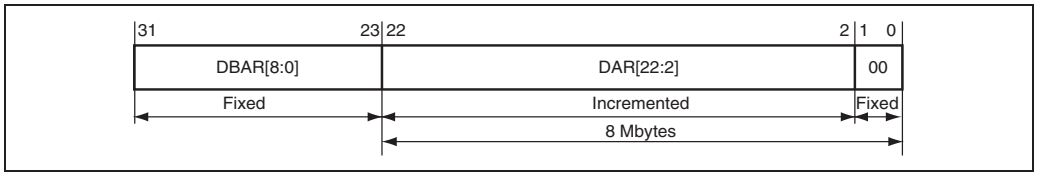


Figure 50.7 Destination Address Configuration

50.2.35 Transfer Count Registers 0 to 2 (TCR0 to 2)

TCRn is a 32-bit readable/writable register that specifies the amount of DMA transfer.

TCR is set to 1 for 4-byte transfer. Specifying H'FFFF for 4-byte transfer permits 4-byte transfer to take place a maximum of 65,535 times.

TCR is also set to 1 for 24-bit transfer which does not involve the SuperHyway. An example of this is DMA transfer from the DSP-XRAM to the DSP-YRAM.

If the transfer size for the SuperHyway is specified as 32 bytes with the TS bit in CHCRn, then the TCRn is decremented by 8. In this case, specify a multiple of 8 in the TCRn.

If the TS bit of the CHCRn is set to B'111 and seamless transfer mode is selected, then specify a multiple of 24 (H'18) in the TCR.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TCRn[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 0	TCRn[15:0]	H'0000	R/W	This bit specifies the amount of transfer. TCR = 1 means 4-byte transfer. The remaining amount of transfer is indicated during transfer. A write is prohibited during transfer.

50.2.36 SHwy Priority Registers 0 to 2 (SHPRI0 to 2)

SHPRIn is a 32-bit readable/writable register whose 4 bits are used to set the SHwy process priority when the transfer destination or source address is specified as an address in memory space under management by the CPU.

The greater the set value, the higher the SHwy process priority (H'F: highest priority, H'0: lowest priority). The priority can be specified for each DMA channel.

If both the transfer source and destination addresses are specified as addresses in the SPU memory space, the SHwy is not accessed and thus the priority value for the channel is ignored.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	SHPRIn[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	SHPRIn[3:0]	H'E	R/W	These bits specify the SHwy process priority.

50.2.37 Channel Control Registers 0 to 2 (CHCR0 to 2)

CHCRn is a 32-bit readable/writable register that controls the address mode, transfer size, etc.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	SWAP[1:0]		DAM	SAM	—	—	IM[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	TS[2:0]			—	—	RINGC[1:0]		—	—	—	TE	—	—	—	DE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R	R/W	R/W	R	R	R	R/(W)*	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23, 22	SWAP[1:0]	00	R/W	Swap bits These bits specify how to swap DMA transfer data. 00: No swap 01: Byte swap 10: Word swap 11: Byte-word swap
21	DAM	0	R/W	Destination Address Mode This bit specifies whether to increment or fix the transfer destination address. 0: Increments the address. 1: Fixes the address.
20	SAM	0	R/W	Source Address Mode This bit specifies whether to increment or fix the transfer source address. 0: Increments the address. 1: Fixes the address.
19, 18	—	00	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
17, 16	IM[1:0]	00	R/W	Intra-SPU2 Transfer Mode (inter-DSP transfer) Set this bit to transfer data within the SPU2 space without using the SHwy. When this bit is set to B'10 or B'11, set the TS bit to B'000. 00: Normal transfer mode 01: Normal transfer mode 10: Intra-SPU2 transfer mode (the source is used as a buffer) 11: Intra-SPU2 transfer mode (the destination is used as a buffer)
15	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
14 to 12	TS[2:0]	All 0	R/W	Transfer Size These bits specify the unit of transfer. 000: Single transfer mode 1 (specify B'000 for iner-DSP transfer) 001: Single transfer mode 2 010: Single transfer mode 3 011: Single transfer mode 4 100: Burst alignment transfer mode 1 101: Burst alignment transfer mode 2 110: Burst alignment transfer mode 3 111: Burst seamless transfer mode
11, 10	—	00	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
9, 8	RINGC[1:0]	00	R/W	Ring Buffer Control These bits enables/disables ring buffer. For details, refer to section 50.6 Modulo Addressing. 00: Off (LSA/LEA disabled) 01: Setting prohibited 10: Enabled (the ring buffer is the source) Specify an address within the ring buffer in SAR. 11: Enabled (the ring buffer is the destination) Specify an address within the ring buffer in DAR.
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	TE	0	R/(W)*	Transfer End Flag This bit is set to 1 when TCR reaches 0 and transfer ends. 0: Transfer is in progress or interrupted (this bit is retained as 0 even if you try to write 1 to it). 1: Transfer is complete (write 0 to the bit to clear it).
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	DE	0	R/W	DMA Transfer Enable This bit specifies enables or disables DMA transfer over the channel. Both this bit and the DME bit in the OR register to start the transfer. 0: Disables the transfer. 1: Enables the transfer.

Note: * Only 0 can be written to clear the flag.

Table 50.6 shows the TS encoding and transfer targets.

Table 50.6 TS Bit Encoding and Transfer Targets

	Transfer Source (Read)			Transfer Destination (Write)		
		DSP memory			DSP memory	
CHCRn.TS	SHwy	P	X/Y	SHwy	P	X/Y
000	32 bits (LOAD4)	32 bits	32 bits of data which includes 24 bits of read data and H’00 concatenated to the least significant bit	32 bits (STORE4)	32 bits	Upper 24 bits of transfer source data
001	32 bits (LOAD4)	32 bits	32 bits of data which includes 24 bits of read data and H’00 concatenated to the most significant bit	32 bits (STORE4)	32 bits	Lower 24 bits of transfer source data
010	32 bits (LOAD4)	32 bits	32 bits of data which includes 24 bits of read data and H’00 concatenated to the least significant bit	32 bits (STORE4)	32 bits	24 bits of data which includes upper 16 bits of transfer source data and H’00 concatenated to the least significant bit ({16 bits, H'00})
011	32 bits (LOAD4)	32 bits	32 bits of data which includes 24 bits of read data and H’00 concatenated to the most significant bit	32 bits (STORE4)	32 bits	24 bits of data which includes lower 16 bits of transfer source data and H’00 concatenated to the most significant bit ({H'00, 16 bits})
100	64 bits×4 (LOAD32)	32 bits×8	{24 bits,H'00}×8	64 bits×4 (STORE32)	32 bits×8	Upper 24 bits of transfer source data × 8

	Transfer Source (Read)			Transfer Destination (Write)		
		DSP memory			DSP memory	
CHCRn.TS	SHwy	P	X/Y	SHwy	P	X/Y
101	64 bits×4 (LOAD32)	32 bits×8	{H'00,24 bits}×8	64 bits×4 (STORE32)	32 bits×8	Lower 24 bits of transfer source data x 8
110	64 bits×4 (LOAD32)	—*1	{24 bits,H'00}×16	64 bits×4 (STORE32) If the transfer source is X/Y, upper 16 bits x 16 is changed to 64 bits x 4.	—*1	{16 bits,H'00}×16
111	64 bits×4 (LOAD32)	—*1	{24 bits,H'00}×N (10or11) (Transfer destination is SHwy only)*2	64 bits×4 (STORE32)	—*1	24 bits×n (10or11) (Transfer source is SHwy only)*2

Note: *1 Do not specify the PRAM. If you specify, transfer data is undetermined.

*2 If TS = B'111, specify the source and destination of transfer as SHwy→SHwy, SHwy→DSP-X/Y, or DSP-X/Y→SHwy.

Intra-SPU2 transfer mode (inter-DSP transfer) is a mode in which data transfer, for example from the DSP0-XRAM to DSP1-XRAM, is complete within the SPU2 without using the SHwy. Since transfer in this mode is performed via the dedicated buffers (BUF0 to 3) in the SPU2, two DMACs, one for each of the data transmitting side and the data receiving side should be started. The DSP memory is the source and BUF0 to 3 are the destination during data transmission while the DSP memory is the destination and BUF0 to 3 are the source during data reception. Thus, set the IM bit in the CHCR register to B'11 on the data transmitting side and to B'10 on the data receiving side.

When the TS bit in the CHCR register to H'4 to 6, set a multiple of 8 in the TCR register. When the TS bit in the CHCR register to H'7, set a multiple of 24 (H'18) in the TCR register.

The SWAP[1:0] bits specify the method of swapping DMA transfer data. SHwy bus data is swapped by the specified method.

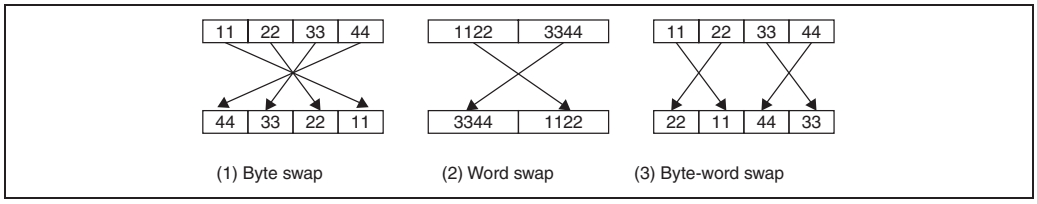


Figure 50.8 Data Swapping Methods

50.2.38 Loop Start Address Registers 0 to 2 (LSA0 to 2)

LSA0 to 2 are 32-bit readable/writable registers. Each of these registers specifies the loop start address by its word address when the source or destination is used as a ring buffer during DMA transfer on DMA channels 0 to 2.

The ring buffer is used only for the DSP data X/Y memory (XRAM/YRAM) and either the source or destination can be used as a ring buffer for one transfer. The maximum size of ring buffer is 48 Kbytes (24 bits x 16 Kwords) and the space for it is from the address specified by this register to the end address specified by the registers LEA0 to 2 below.

The value set in this register is valid only if the RINGC[1:0] bits in the CHCR register are set to B'10 or B'11.

For details, see section 50.6, Modulo Addressing.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LSAn[15:2]														—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 2	LSAn[15:2]	H'0000	R/W	Loop Start Address bits of ring buffer Specify the address by its word address (physical address[15:2]).
1, 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

50.2.39 Loop End Address Registers 0 to 2 (LEA0 to 2)

LEA0 to 2 are 32-bit readable/writable registers. Each of these registers specifies the loop end address by its word address when the source or destination is used as a ring buffer during DMA transfer on DMA channels 0 to 2.

The ring buffer is used only for the DSP data X/Y memory (XRAM/YRAM) and either the source or destination can be used as a ring buffer for one transfer. The maximum size of ring buffer is 48 Kbytes (24 bits x 16 Kwords) and the space for it is from the address specified by the registers LSA0 to 2 above to the end address specified by this register.

The value set in this register is valid only if the RINGC[1:0] bits in the CHCR register are set to B'10 or B'11.

For details, see section 50.6, Modulo Addressing.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LEAn[15:2]														—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 2	LEAn[15:2]	H'0000	R/W	Loop End Address bits of ring buffer Specify the address by its word address (physical address[15:2]).
1, 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

50.3 Memory Description

The SPU2 memory configuration is shown in figure 50.9. In this figure, the SPU2 is allocated to the physical space from H'00 0000 to H'1F FFFF (21 bits: 2 Mbytes).

Each DSP's instruction RAM (PRAM), data RAM (X/YRAM), and DSP-IO peripheral module space and the SPU register (SPUREG) are mapped to this space.

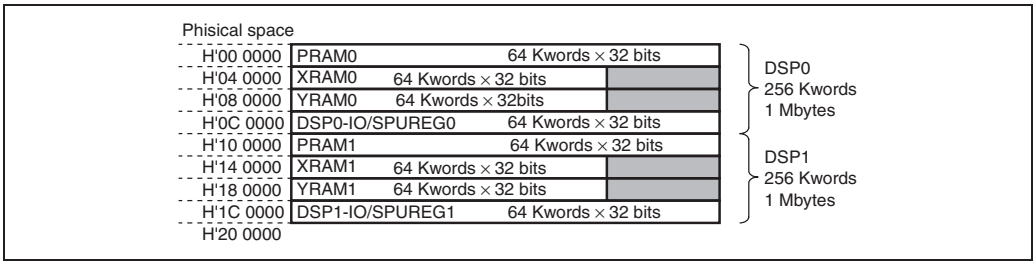


Figure 50.9 SPU2 Memory Configuration (Basic Two-DSP Configuration)

50.3.1 DSP Instruction RAM Areas

The DSP instruction RAM (PRAM) configuration is shown in figure 50.10. The PRAM is mapped to a 256-Kbyte space (64 Kwords × 32 bits).

This product has 160-Kbyte (40 Kwords × 32 bits) of instruction RAM.

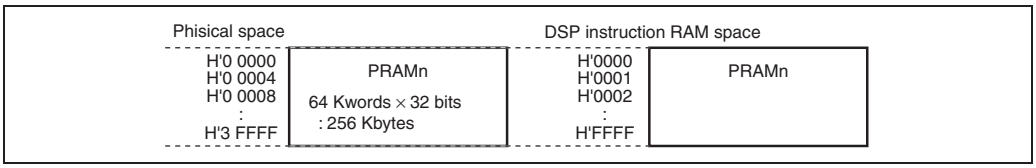


Figure 50.10 DSP Instruction RAM (PRAM) Configuration

50.3.2 DSP Data RAM Areas

The DSP data RAM (XRAM and YRAM) configurations are shown in figure 50.11. Both the XRAM and YRAM consist of 192-Kbyte (64 Kwords × 24 bits) of space.

This product has 168-Kbyte (56 Kwords × 24 bits) of data RAM.

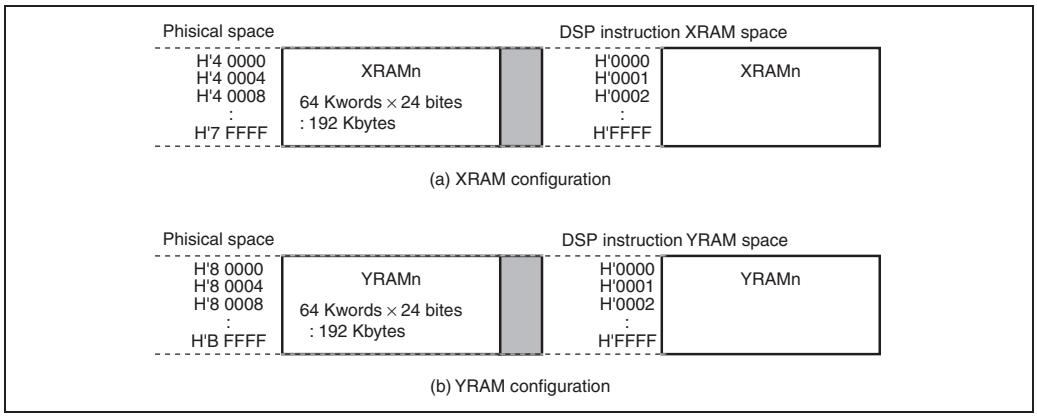


Figure 50.11 DSP Data RAM (XRAM/YRAM) Configurations

50.3.3 DSP Memory Allocation

The SPU2 can change memory allocation for DSP0 and DSP1 by switching memory banks. The PRAM and XRAM are allocated in this way.

DSP0 and DSP1 can map 32 bits×40 Kwords (= 160 Kbytes) of PRAM and 24 bits×56 Kwords (= 168 Kbytes) of XRAM.

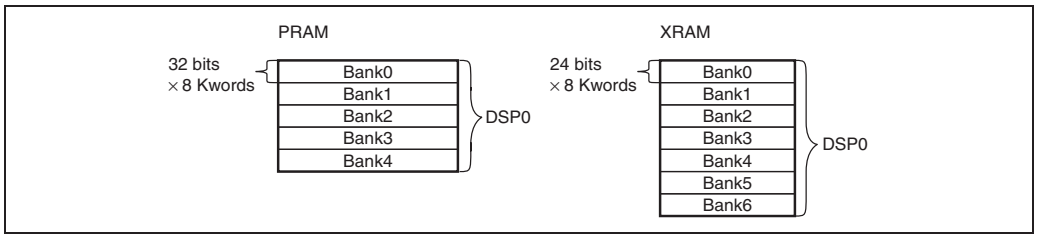


Figure 50.12 Initial Memory Allocation

In the initial state, DSP0 is set to use all of the PRAM (40 Kwords) and XRAM (56 Kwords), DSP1 is set to use no banks in the PRAM and XRAM.

Specify the banks to be used by DSP0 and DSP1.

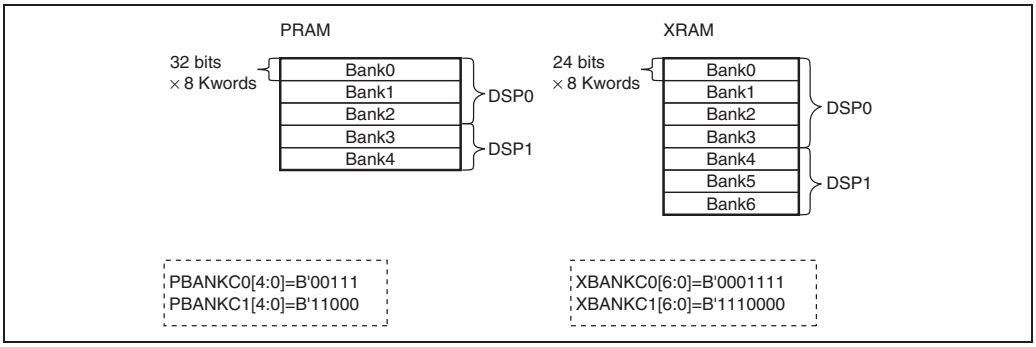


Figure 50.13 Example of Memory Allocation

(1) Example of Switching PRAM Banks

Figure 50.14 shows an example of switching PRAM banks. Figure 50.15 and 50.16 show examples of PRAM memory allocation.

In this example, application A is switched to application C for DSP0 and application B is switched to application D for DSP1. Reset the DSP core before switching application.

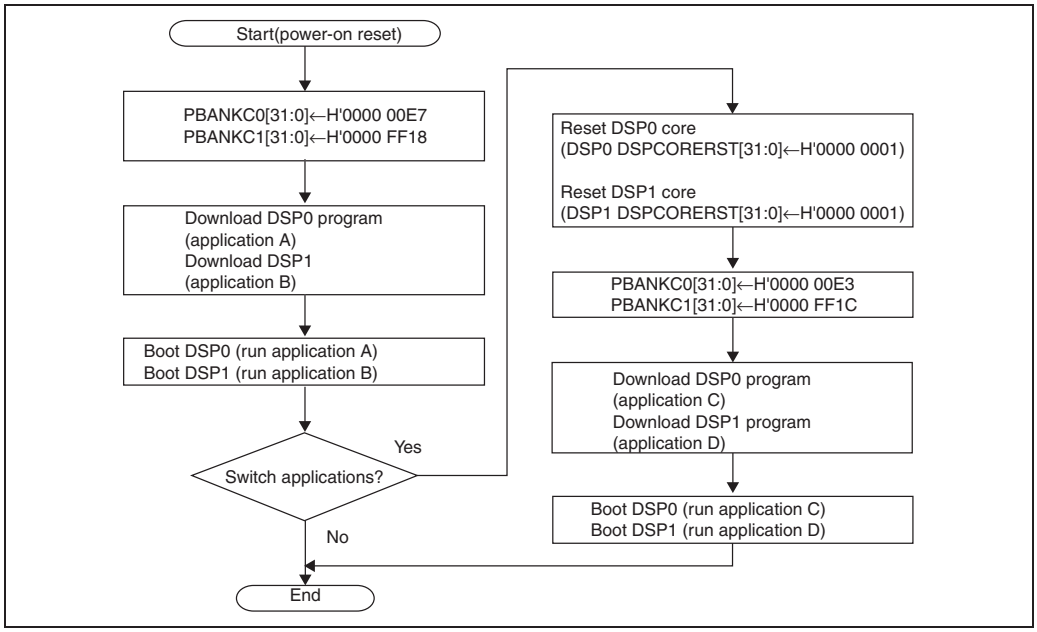


Figure 50.14 Example of Procedure for Switching PRAM Banks

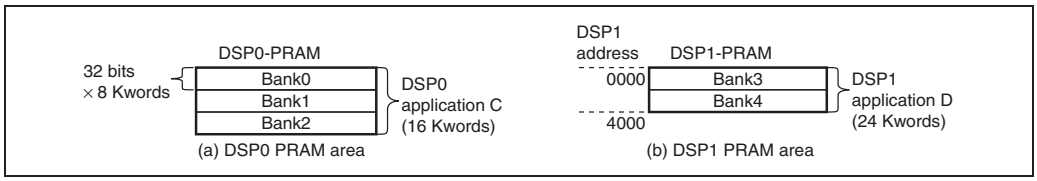


Figure 50.15 Program Areas for Application A and B (Initial Memory Allocation)

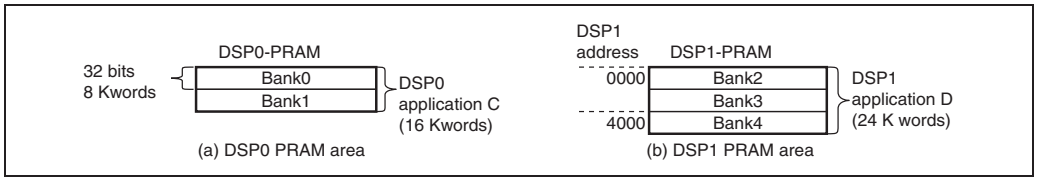


Figure 50.16 Program Areas for Application C and D (Modified Memory Allocation)

(2) Example of Switching XRAM Banks

The XRAM, similarly to the PROM, can be allocated between DSP0 and DSP1. This product has 56 Kwords (8 Kwords×7 banks) of XRAM. Adjust XRAM allocation depending on applications by controlling the XBANKC0 and XVANKC1 registers.

50.3.4 DSP I/O Area

The DSP I/O space configuration is shown in figure 50.17. 64 Kwords are mapped to this space like the XRAM and YRAM and the addressing unit for the YRAM is used for addressing this space.

The SPU registers are mapped to the I/O space, which can be accessed by both the CPU and the DSP.

However, the peripheral area can be accessed only by the DSP.

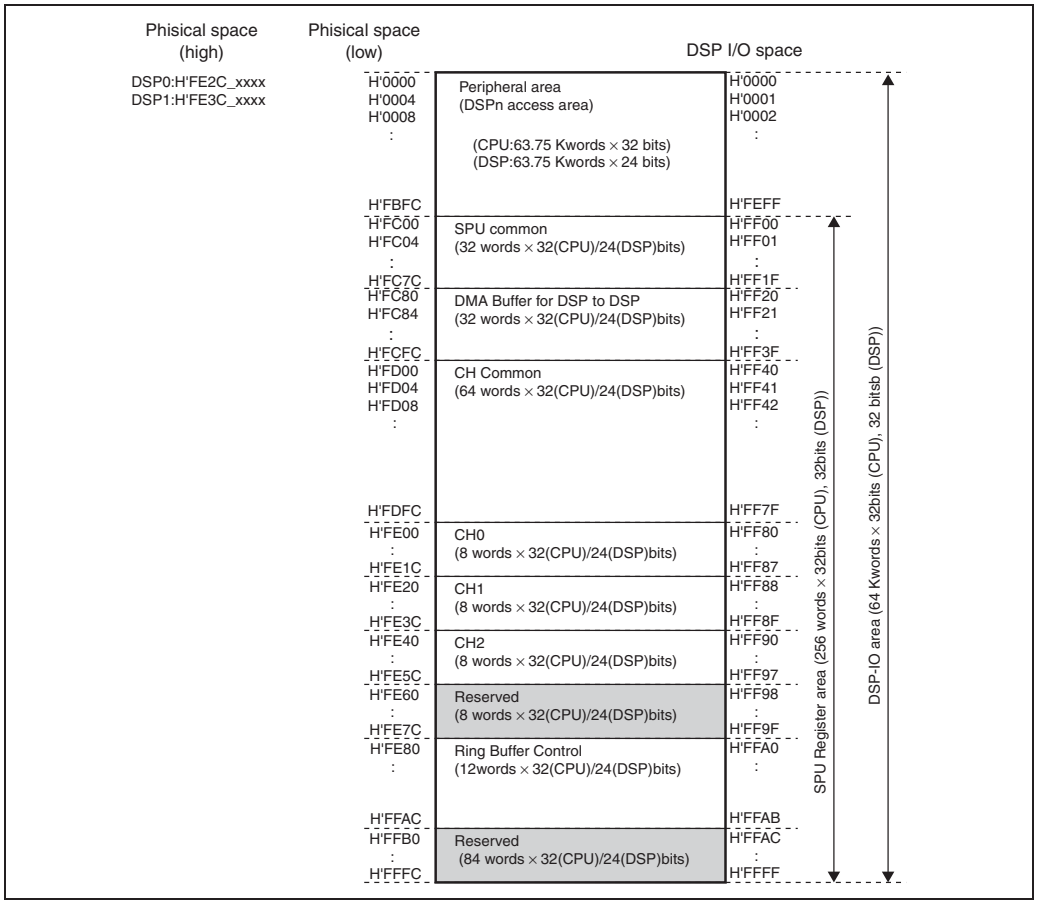


Figure 50.17 DSP I/O Space Configuration

The FSI is mapped from H'0000 to H'00FF in the DSP I/O space.

50.3.5 Interrupt Interface Specifications

The SPU2 outputs the same number of interrupt request signals to the CPU as that of the on-chip DSPs. These signals should be cleared at the beginning of the interrupt handler after the event occurs. The masks for the interrupt request signals to the CPU are controlled by the IMASKC register. The interrupt sources are controlled by the IEMASKC and IEVENTC registers.

When clearing an interrupt source, write 0 to the bit corresponding to the source to be cleared and 1 to the other bits.

Each DSP has three interrupt signals to the DSP in the SPU2. One of them is assigned to the source in the SPU2 and the other two have input pins for the SPU2 external peripheral modules.

When the DSP accepts an interrupt, it asserts the acknowledge signal for 1 cycle. To assert spui_int_dsp0[1] by the SPU2 external peripheral modules, spui_int_dsp0[1] should be negated by assertion of spuo_int_ack_dsp0[1]. Similarly, spui_int_dsp0[0] should also be negated by assertion of spuo_int_ack_dsp0[0].

To reassert them, they should be negated for at least 1 cycle.

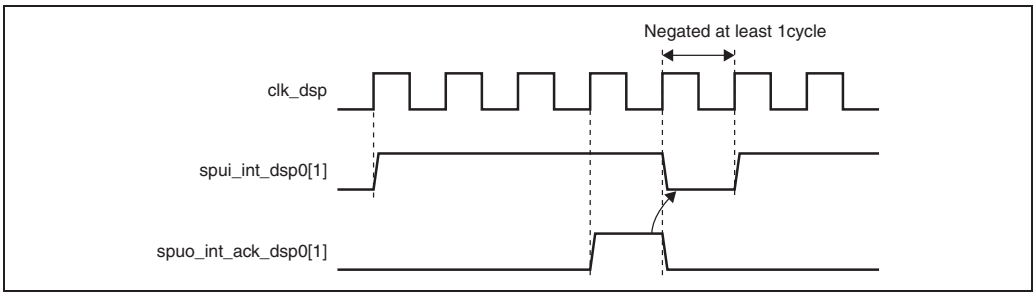


Figure 50.18 Interrupt Signal Timing

When the DSP is interrupted, one bit of the interrupt signals to the DSP (int[2:0]) is asserted.

If the interrupt is generated by the SPU2 internal source, int[2] is asserted. When int[2] is accepted by the DSP, the program counter of the DSP jumps to the interrupt vector irq3 to execute interrupt handling.

Interrupts from the SPU2 peripheral modules are assigned to int[1:0] and they are handle by jumping to irq2 with int[1] or to irq1 with int[0].

50.4 Start Procedures

50.4.1 Procedure for Starting the DSP

The procedure for starting the DSP is shown in figure 50.19. To start the DSP after a hardware reset, follow the flow chart below to download a DSP program. The procedure for starting the DSP is common to both of the DSPs in this product and there is no restriction on the order of starting them.

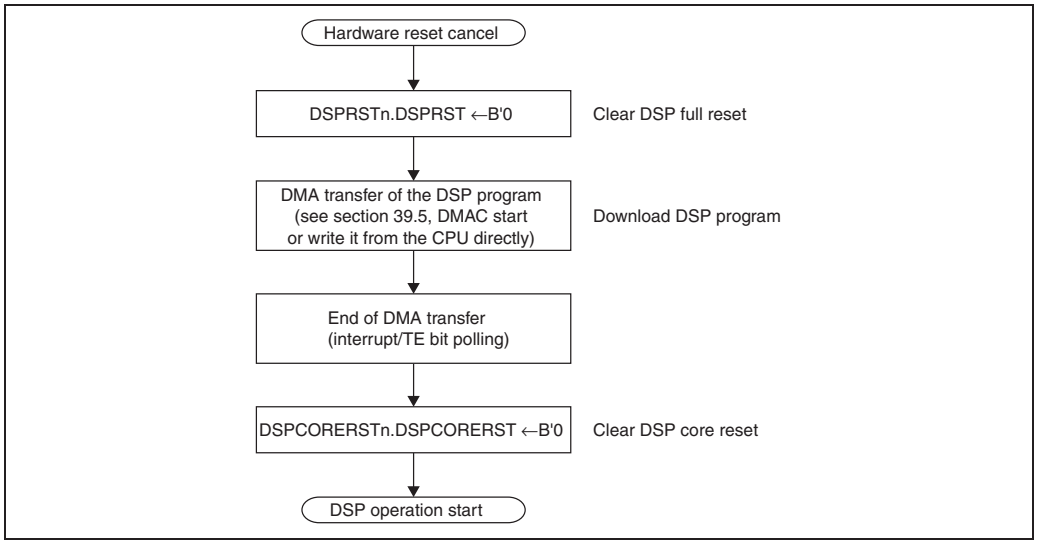


Figure 50.19 Procedure for Starting the DSP

50.5 DMAC Start

An example procedure for setting the registers for starting the DMAC is shown in figure 50.20.

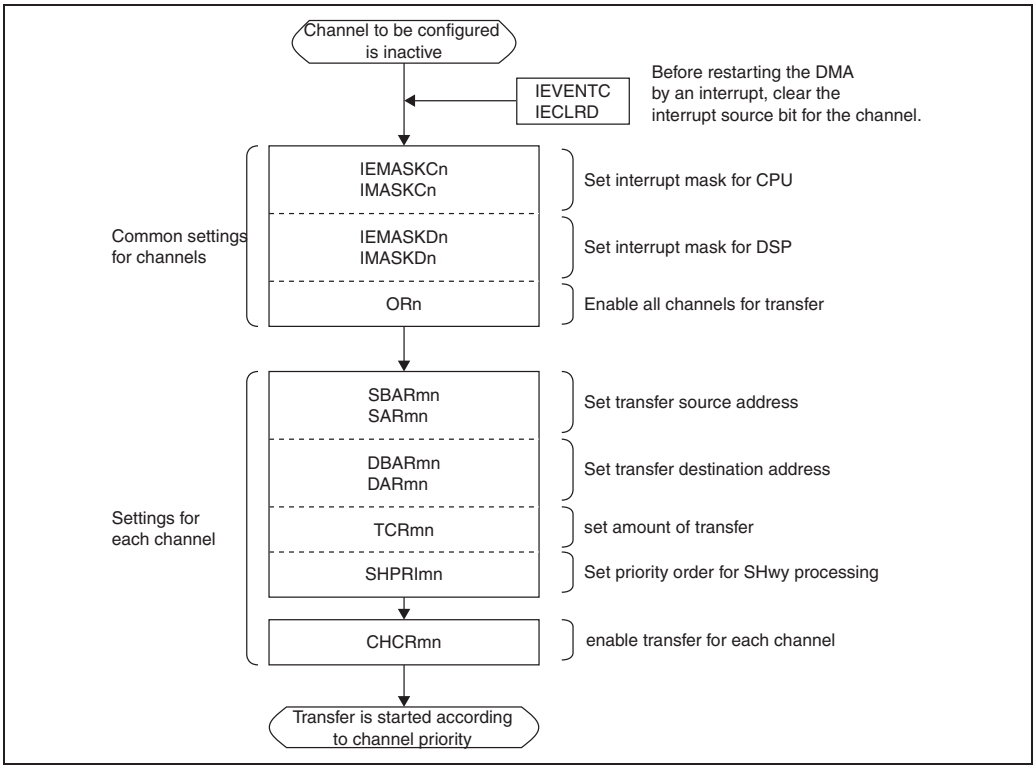


Figure 50.20 Recommended Procedure for Starting the DMAC

50.6 Modulo Addressing

Table 50.7 shows the SPU2-DMAC modulo addressing specifications.

Table 50.7 SPU2-DMAC Modulo Addressing Specifications

Item	Description
Target memory	• DSP-XRAM or DSP-YRAM
Target range	• 96 bytes to 48 Kbytes (24 bits×16 Kwords)
	• The ring buffer size should be determined by the LEA−LSA in 32-word (96-byte) units.
DMA channel	• Supported on all channels (CH0, CH1, CH2)
Source/destination selection	• Modulo addressing supported for source or destination only (DMA transfer between ring buffers is unsupported.)
Ring end address	• When the DMA source is used as a ring buffer, the data in the address specified by LEA0 to 2 are not transferred.
	• When the DMA destination is used as a ring buffer, data are not stored in the address specified by LEA0 to 2.
Address for starting DMA (source/destination)	• When using the DMA source as a ring buffer, specify an address in the ring buffer as the source address for starting DMA transfer (LSA can be specified , but not LEA).
	• When using the DMA destination as a ring buffer, specify an address in the ring buffer as the destination address for starting DMA transfer (LSA can be specified, but not LEA).

Figure 50.21 shows an example of modulo addressing. When using the DSP-XRAM for the DMA source as a ring buffer, specify an address in the ring buffer area for starting DMA transfer.

When the data one word before LEA are transferred in the Nth DMA transfer, the next transfer starts from the address specified by LSA.

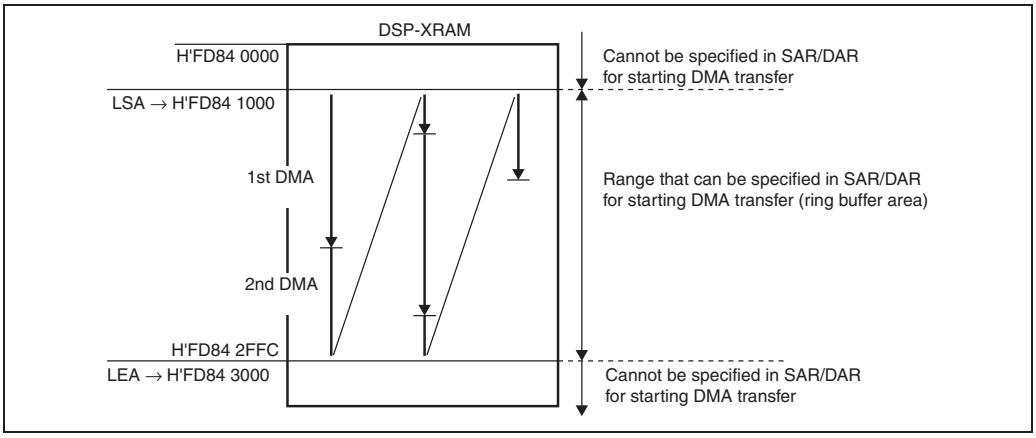


Figure 50.21 Example of Modulo Addressing

50.7 Restrictions

Table 50.8 shows the restrictions on the use of the SPU2.

Table 50.8 SPU2 Usage Restrictions

	Restrictions	
No.	**Item**	**Description**
1	Unit of access	Only 32-bit access to the SPU registers from the CPU is guaranteed.
2	Register setting	If the CHCR.DE and OR.DME bits are set to 1 and DMA transfer via a DMA channel is enabled, a write to the SPU registers via that DMA channel should not be performed. However, the CHCR.TE bit can be cleared to 0. Also, the CHCR.DE bit can be negated to interrupt the DMA transfer.
3	DMA transfer area	The SARn and DARn registers should be specified so that data starting at address H'0000 0000 can be transferred in 8-Mbyte units or less. Data transfer across an 8-Mbyte boundary in which the 24th bit produces a carry is not guaranteed.
4	Intra-SPU2 transfer (inter-DSP transfer)	Two DMA channels should be used if a transfer is performed in the SPU2 without using the SHwy. Also, the CHCR.TS bit should be set to 0.
5	LD32/ST32 transfer	If CHCR.TS = B’100/B’101/B’110 is specified, TCRn should be a multiple of 8 (H’0018).
6	Seamless transfer	If CHCR.TS = B’111 is specified, TCRn should be a multiple of 24 (H’0018).
7	Bus through mode	When the DSP accesses the SPU2 external space in bus-through mode, the SPU2 external address should be specified in the BTADRU register.
8	Initiator source	When more than one DSP is included and the SHwy initiator port is implemented with one port, initiator source 0 and 1 should have the same value.

Section 51 FIFO-Buffered Serial Interface 2 (FSI2/FMSI)

The FIFO-buffered serial interface 2 (FSI2) and the FIFO-incorporating melody and serial interface (FMSI) are sound I/O interfaces that support both analog and digital connections. It has an output function that outputs 24-bit data output from the audio processing circuit with 3 lines: LR clock, bit clock, and serial clock lines, and an input function that converts input 3-line data to 24-bit data. It supports continuous I/O operation by managing FIFO states and generating interrupts. FSI2 supports an SPDIF interface.

These modules act as peripheral circuits of the SPU2 (Sound Processing Unit 2) audio processing circuit.

51.1 Features

The functions and features are listed in table 51.1.

Table 51.1 List of FSI2 Functions

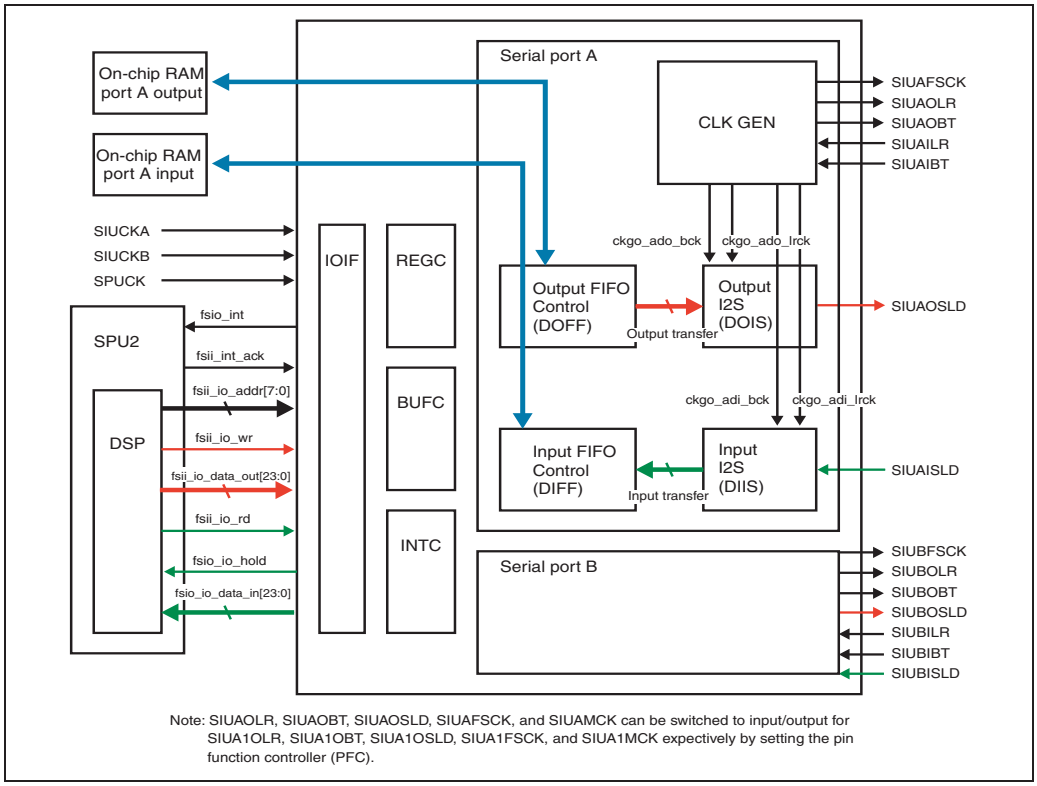
Classification	Item	Details
Operating frequency	Sampling frequency (fs)	8kHz to 96kHz (max.) SPDIF up to 192kHz[stream]
	Audio clock	Clock signal (at 32 f_S, 64 f_S, 128 f_S, 256 f_S, or 512 f_S) used to generate the LR clock and bit clock 512 kHz to 49.15 MHz (max.) (64 × 8 kHz to 512 × 96kHz)
	DSP clock	FSI2 operating frequency: 120MHz(max)
DSP/IO	Data bus width	24 bits
Supported I/O format	Monaural (1 channel)	MONO, MONO Delay
	Stereo (2 channels)	I2S, PCM
	Multi-channel (1 to 8 channels)	TDM, TDM Delay

Classification	Item	Details
Output interface	3-line serial output (× 2: ports A and B)	Master operation (generates the LR and bit clocks from the audio clocks: 64 fs, 128 fs, 256 fs, 512 fs)
		LR clock (fs): 8 kHz to 9 6kHz
		Bit clock:
		32 bits/fs, 64 bits/fs, 128 bits/fs, 256 bis/fs, 512 bits/fs (monaural)
		64 bits/fs, 128 bits/fs, 256 bits/fs, 512 bits/fs (stereo)
		256 bits/fs, 512 bits/fs (multi-channel)
		Slave operation (can operate with the external LR and bit clocks)
		LR clock (fs): 8 kHz to 96 kHz
		Bit clock:
		32 bits/fs, 64 bits/fs, 128 bits/fs, 256 bits/fs, 512 bits/fs (monaural)
		64 bits/fs, 128 bits/fs, 256 bits/fs, 512 bits/fs (stereo)
		256 bits/fs, 512 bits/fs (multi-channel)
Input interface	3-line serial input (× 1: ports A)	Master operation
		Supports the same LR and bit clocks as the output interface.
		Slave operation
		Supports the same LR and bit clocks as the output interface.
FIFO	FIFO status	State, number of stored sample data, overflow, underflow
	FIFO clear	Clears the address pointer.
	Interrupt source condition select	Output operation:
		(1) Empty.
		(2) More than half of data areas are free.
		(3) Data areas for more than 1 sample are free.
		Input operation:
		(1) Full.
		(2) More than half of data areas are occupied.
		(3) Data areas for more than 1 sample are occupied.

Classification	Item	Details
Interrupt	Interrupt control	Can generate interrupt requests externally. Supports masks for interrupt sources and interrupt signals.
Muting	Mute mode	Normal muting and muting at zero crossing

Figure 51.1 shows a block diagram of the FSI2.

Serial port B has the same structure and interface as serial port A.



Note: SIUAOLR, SIUAOBT, SIUAOSLD, SIUAFSCK, and SIUAMCK can be switched to input/output for SIUA1OLR, SIUA1OBT, SIUA1OSLD, SIUA1FSCK, and SIUA1MCK expectively by setting the pin function controller (PFC).

Figure 51.1 Block Diagram

The followings are the brief descriptions of each block.

(1) Serial Port A

Serial port A is a module that consists of 5 modules: CLK GEN, data output FIFO control, data input FIFO control, data output I2S, and data input I2S, and performs I/O operations for audio data

(a) CLK GEN

CLK GEN selects the master clock generated internally or the slave clock supplied external and outputs it to the internal modules (DOIS, DIIS).

(b) Data Output FIFO Control (DOFF)

A FIFO to which data from the DSP is written is called output FIFO. The DOFF controls access to the DP-RAM. The FIFO states are reflected on the FIFO status register (A_DOFF_ST).

The output FIFO control register (A_DOFF_CTL) can be used to select the condition for generating the FIFO interrupt source (A_DOFF_CTL.IHC).

The FIFO clear (A_DOFF_CTL.CLR) initializes the access pointer to the on-chip RAM and the error history.

(c) Data Output I2S (DOIS)

The DOIS controls a counter based on the rising and falling edges of the LR clock generated from the CLK GEN to request data to the DOFF.

It also determines the channel number associated with data and stores data into the corresponding channel buffer. It reads data at the next LR clock and shifts it to the left to output serial data.

(d) Data Input FIFO Control (DIFF)

A FIFO to which external data is written is called input FIFO. The DIFF controls access to the DP-RAM. The FIFO states are reflected on the FIFO status register (A_DIFF_ST).

The input FIFO control register (A_DIFF_CTL) can be used to select the condition for generating the FIFO interrupt source (A_DIFF_CTL.IHC).

The FIFO clear (A_DIFF_CTL.CLR) initializes the access pointer to the on-chip RAM and the error history.

(e) Data Input I2S (DIIS)

The DIIS controls a counter based on the rising and falling edges of the LR clock generated from the CLK GEN to store the parallel converted signal to each channel buffer. The stored data are concatenated the channel number and written to input FIFOs.

(f) BP-IF (Biphase mark Interface)

The BP-IF outputs the Biphase mark format after modulating the SPDIF format (IEC60958) from 64 bit/fs to 128bit/fs.

(g) SPTR (SPDIF Transfer Return)

IF FSI2 treats SPDIF format, the SPTR makes the user's data, the state of channel and so on including in the audio data, and outputs to the BP-IF and the DOIS.

(2) Serial Port B

Serial port B has the same structure and interface as serial port A and operates independently.

(3) Other Management Modules

These modules control registers for major functions.

(a) INTC

This module controls interrupt signals. It aggregates 4 interrupt sources generated internally and outputs as one interrupt signal externally. Interrupt events are triggered based on the FIFO capacity. The condition can be changed.

Interrupt source and interrupt signal masks can be used to control how to handle those triggered events.

(b) BUFC

The BUFC block controls data reads/writes between the DSP and FIFOs. To read input data continuously, data are prefetched from FIFOs. Data are output with 4 waits on the initial read, but the following reads can be performed continuously with one wait by controlling the buffer pointer and reading data stored in buffers.

(c) REGC

This module manages registers that are not used by INTC and BUFC. It is used to manage format, clock, and MUTE settings.

(d) IOIF

This module selects read data of INTC, BUFC, and REGC.

Table 51.2 summarizes the number of wait cycles for the registers accessible from the DSP-IO.

Table 51.2 Wait Cycles for FSI2 Register Read/Write

Register	Read	Write
A_DIDT	Initial read (4 waits)	Prohibited
B_DIDT	2nd and following reads (1 wait)	
Other registers	1 wait	No wait

51.2 Input/Output Pins

Table 51.3 shows the FSI2 pin configurations.

Table 51.3 Pin Configurations

FSI2 Block	Pin Name	Function	Input/Output	Description
Port A	FSIACK	Port A master clock input	Input	Master clock input pin for port A
	FSIAILR	Port A sound input L/R clock	Input	Sound input L/R clock pin (slave)
	FSIAIBT	Port A sound input bit clock	Input	Sound input bit clock pin (slave)
	FSIAISLD	Port A sound input serial data	Input	Sound input serial data pin
	FSIAOMC	Port A master clock output	Output	Master clock output pin for port A
	FSIAOLR	Port A sound output L/R clock	Output	Sound output L/R clock pin (master)
	FSIAOBT	Port A sound output bit clock	Output	Sound output bit clock pin (master)
	FSIAOSLD	Port A sound output serial data	Output	Sound output serial data pin
	FSIASPDIF	Port A sound output SPDIF data	Output	Sound output SPDIF pin
Port B	FSIBCK	Port B master clock input	Input	Master clock input pin for port B
	FSIBSPDIF	Port A sound output SPDIF data	Output	Connect to the HDMI

51.3 Register Descriptions

Table 51.4 shows the FSI2 register configuration.

Table 51.4 Register Configuration

Type	Register Name	Abbreviation	R/W (Common to CPU/DSP)	Access Size		Physical Address	DSP Address
				CPU	DSP		
Port A	Port A output serial format register	A_DO_FMT	R/W	32	24	H'FE3C0000	H'0000
	Port A output FIFO control register	A_DOFF_CTL	R/W	32	24	H'FE3C0004	H'0001
	Port A output FIFO status register	A_DOFF_ST	R/W	32	24	H'FE3C0008	H'0002
	Port A input serial format register	A_DI_FMT	R/W	32	24	H'FE3C000C	H'0003
	Port A input FIFO control register	A_DIFF_CTL	R/W	32	24	H'FE3C0010	H'0004
	Port A input FIFO status register	A_DIFF_ST	R/W	32	24	H'FE3C0014	H'0005
	Port A Audio clock control register	A_ACK_MD	R/W	32	24	H'FE3C0018	H'0006
	Port A clock invert control register	A_ACK_RV	R/W	32	24	H'FE3C001C	H'0007
	Port A read data register	A_DIDT	R	32	24	H'FE3C0020	H'0008
	Port A write data register	A_DODT	W	32	24	H'FE3C0024	H'0009
	Port A MUTE state register	A_MUTE_ST	R	32	24	H'FE3C0028	H'000A
	Port A DMA control register(Output)	A_OUT_DMAC	R/W	32	24	H'FE3C002C	H'000B
	Port A output control register	A_OUT_SEL	R/W	32	24	H'FE3C0030	H'000C
	Port A output SPDIF state register	A_OUT_SPST	R/W	32	24	H'FE3C0034	H'000D
	Port A DMA control register(Input)	A_IN_DMAC	R/W	32	24	H'FE3C0038	H'000E
	Port A input control register	A_IN_SEL	R/W	32	24	H'FE3C003C	H'000F
Port B	Port B output serial format register	B_DO_FMT	R/W	32	24	H'FE3C0040	H'0010
	Port B output FIFO control register	B_DOFF_CTL	R/W	32	24	H'FE3C0044	H'0011
	Port B output FIFO status register	B_DOFF_ST	R/W	32	24	H'FE3C0048	H'0012
	Port B Audio clock control register	B_ACK_MD	R/W	32	24	H'FE3C0058	H'0016
	Port B clock invert control register	B_ACK_RV	R/W	32	24	H'FE3C005C	H'0017
	Port B write data register	B_DODT	W	32	24	H'FE3C0064	H'0019
	Port B MUTE state register	B_MUTE_ST	R	32	24	H'FE3C0068	H'001A
	Port B DMA control register(Output)	B_OUT_DMAC	R/W	32	24	H'FE3C006C	H'001B
	Port B output control register	B_OUT_SEL	R/W	32	24	H'FE3C0070	H'001C
	Port B output SPDIF state register	B_OUT_SPST	R/W	32	24	H'FE3C0074	H'001D
Port A/B	Port A master clock control register	A_MST_CTLR	R/W	32	24	H'FE3C0180	H'0060

Type	Register Name	Abbreviation	R/W (Common to CPU/DSP)	Access Size		Physical Address	DSP Address
				CPU	DSP		
Port A/B	Port B master clock control register	B_MST_CTLR	R/W	32	24	H'FE3C01A0	H'0068
Timer	Timer set register	TMR_CTL	R/W	32	24	H'FE3C01D8	H'0076
	Timer clear register	TMR_CLR	R/W	32	24	H'FE3C01DC	H'0077
Interrupt	Interrupt clear register	INT_CLR	R/W	32	24	H'FE3C01F0	H'007C
	CPU interrupt state register	CPU_INT_ST	R/W	32	24	H'FE3C01F4	H'007D
	CPU interrupt source mask register	CPU_IEMSK	R/W	32	24	H'FE3C01F8	H'007E
	CPU interrupt signal mask register	CPU_IMSK	R/W	32	24	H'FE3C01FC	H'007F
	DSP interrupt state register	DSP_INT_ST	R/W	32	24	H'FE3C0200	H'0080
	DSP interrupt source mask register	DSP_IEMSK	R/W	32	24	H'FE3C0204	H'0081
	DSP interrupt signal mask register	DSP_IMSK	R/W	32	24	H'FE3C0208	H'0082
MUTE	MUTE set register	MUTE	R/W	32	24	H'FE3C020C	H'0083

Type	Register Name	Abbreviation	R/W (Common to CPU/DSP)	Access Size CPU	Access Size DSP	Physical Address	DSP Address
Reset	Clock reset register	ACK_RST	R/W	32	24	H'FE3C0210	H'0084
	Software reset register	SOFT_RST	R/W	32	24	H'FE3C0214	H'0085
FIFO	FIFO size register	FIFO_SZ	R	32	24	H'FE3C0218	H'0086
Peripheral	Clock select register	CLK_SEL	R/W	32	-	H'FE3C0220	-
Bus	SWAP select register	SWAP_SEL	R/W	32	-	H'FE3C0228	-
	HPB software reset register	HPB_SRST	R/W	32	-	H'FE3C022C	-
Port A	SPDIF(60958)	A_SP_CHST00	R/W	32	24	H'FE3C0240	H'0090
Param	Port A channel state register	A_SP_CHST01				H'FE3C0244	H'0091
	SPDIF(60958)	A_SP_USDT00				H'FE3C02A0	H'00A8
	Port A user data register	…	R/W	32	24	…	…
		A_SP_USDT23				H'FE3C02FC	H'00BF
	SPDIF(61937) Port A preamble pa register	A_SP_PA	R/W	32	24	H'FE3C0300	H'00C0
	SPDIF(61937) Port A preamble pb register	A_SP_PB	R/W	32	24	H'FE3C0304	H'00C1
	SPDIF(61937) Port A preamble pc register	A_SP_PC	R/W	32	24	H'FE3C0308	H'00C2
	SPDIF(61937) Port A preamble pd register	A_SP_PD	R/W	32	24	H'FE3C030C	H'00C3
	Port A Pause cycle register	A_SP_PS	R/W	32	24	H'FE3C0314	H'00C5
	Port A Pause length register	A_SP_PL	R/W	32	24	H'FE3C0318	H'00C6
	Port A Frame size register	A_SP_FS	R/W	32	24	H'FE3C031C	H'00C7
Port B	SPDIF(60958)	B_SP_CHST00	R/W	32	24	H'FE3C0320	H'00C8
Param	Port B channel state register	B_SP_CHST01				H'FE3C0324	H'00C9
	SPDIF(60958)	B_SP_USDT00				H'FE3C0380	H'00E0
	Port B user data register	…	R/W	32	24	…	…
		B_SP_USDT23				H'FE3C03DC	H'00F7
	SPDIF(61937) Port B preamble pa register	B_SP_PA	R/W	32	24	H'FE3C03E0	H'00F8

Type	Register Name	Abbreviation	R/W (Common to CPU/DSP)	Access Size		Physical Address	DSP Address
				CPU	DSP		
Port B Param	SPDIF(61937) Port B preamble pb register	B_SP_PB	R/W	32	24	H'FE3C03E4	H'00F9
	SPDIF(61937) Port B preamble pc register	B_SP_PC	R/W	32	24	H'FE3C03E8	H'00FA
	SPDIF(61937) Port B preamble pd register	B_SP_PD	R/W	32	24	H'FE3C03EC	H'00FB
	Port B Pause cycle register	B_SP_PS	R/W	32	24	H'FE3C03F4	H'00FD
	Port B Pause length register	B_SP_PL	R/W	32	24	H'FE3C03F8	H'00FE
	Port B Frame size register	B_SP_FS	R/W	32	24	H'FE3C03FC	H'00FF
common	Interrupt SEL register	INT_SEL	R/W	32	24	H'FE3FF808	H'FE02

Note: The port A and port B registers have the same functions and settings.

51.3.1 Port A/B Output Serial Format Register (A_DO_FMT/B_DO_FMT)

A_DO_FMT/B_DO_FMT is a 32-bit readable/writable register. It selects the format from MONO, MONO_Delay, PCM, I2S, TDM, and TDM_Delay that is used in output operations on serial ports A/B.

When TDM and TDM_Delay modes are selected, it also specifies the number of channels (1 to 8 channels).

Bit:	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	FMT[2:0]			—	NCH[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6 to 4	FMT[2:0]	011	R/W	Format Select 000: MONO (1 channel) 001: MONO Delay (1 channel) 010: PCM (2 channels) 011: I2S (2 channels) 100: TDM (1 to 8 channels) 101: TDM Delay (1 to 8 channels) 110: Setting prohibited 111: Setting prohibited
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
2 to 0	NCH[2:0]	000	R/W	These bits specify the number of channels in TDM and TDM_Delay modes. When selecting the modes other than TDM and TDM_Delay, specify B'000. 000: 1 channel 001: 2 channels 010: 3 channels 011: 4 channels 100: 5 channels 101: 6 channels 110: 7 channels 111: 8 channels

51.3.2 Port A/B Output FIFO Control Register (A_DOFF_CTL/B_DOFFCTL)

A_DOFF_CTL/B_DOFF_CTL is a 32-bit readable/writable register that selects the conditions for generating interrupt sources of serial ports A/B. The FIFO clear initializes the access pointer to the on-chip RAM and the history of overflow and underflow errors.

Bit:	23	22	21	20	19	18	17	16
	—	—	IHC[1:0]		—	—	—	—
Initial value:	0	0	0	1	0	0	0	0
R/W:	R	R	R/W	R/W	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/(W)*

Bit	Bit Name	Initial Value	R/W	Description
31, 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
21, 20	IHC[1:0]	01	R/W	Interrupt Source Condition Select 00: Empty. 01: More than half of data areas are free. 10: Data areas for more than 1 sample are free. 11: Setting prohibited (Full state)
19 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	CLR	0	R/(W)*	FIFO Clear This bit initializes the access pointer and the error history. This bit is always read as 0. 0: When only the interrupt source condition is changed, the write value should be 0. 1: Clears FIFOs.

Note: * f 1 is written to the CLR bit, it is asserted for 1 pulse and cleared to 0.

51.3.3 Port A/B Output FIFO Status Register (A_DOFF_ST/B_DOFF_ST)

A_DOFF_ST/B_DOFF_ST is a 32-bit readable/writable register. It can be used to read the output FIFO states for serial ports A/B, the number of stored sample data, and the history of overflow and underflow errors.

The OF and UF bits clear the history when they are written to 0.

Bit:	23	22	21	20	19	18	17	16
	—	—	ST[1:0]		—	—	—	SZ[8]
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SZ[7:0]								—	—	—	OF	—	—	—	UF
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/(W)*	R	R	R	R/(W)*

Bit	Bit Name	Initial Value	R/W	Description
31, 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
21, 20	ST[1:0]	00	R	FIFO State 00: Empty state. 01: Less than half of data areas are occupied. 10: More than half of data areas are occupied. 11: Full state.
19 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
16 to 8	SZ[8:0]	H'000	R	Number of Sample Data These bits indicate the number of sample data stored in FIFOs. The maximum value varies depending on the number of channels selected for the format. The maximum number of sample data for each channel is shown below (if 256 words of DP-RAM is connected). If more data than the maximum number in the parenthesis are written, an overflow occurs. FIFOs are used in 4-channel units in 3-channel mode and in 8-channel units in 5- to 7-channel mode, meaning that more FIFOs than the required size of DP-RAM are used. The DSP should take into account the maximum number of writes for these extra FIFOs. 1 channel: 256 (256 × 1 = 256) 2 channels: 128 (128 × 2 = 256) 3 channels: 64 (64 × 3 = 192) 4 channels: 64 (64 × 4 = 256) 5 channels: 32 (32 × 5 = 160) 6 channels: 32 (32 × 6 = 192) 7 channels: 32 (32 × 7 = 224) 8 channels: 32 (32 × 8 = 256)
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	OF	0	R/(W)*	FIFO Error History 0: No error has occurred. 1: Overflow has occurred.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	UF	0	R/(W)*	FIFO Error History 0: No error has occurred. 1: Underflow has occurred.

Note: * The FIFO error history is cleared by writing 0 to this bit and retained by writing 1 to it.

51.3.4 Port A Input Serial Format Register (A_DI_FMT)

A_DI_FMT is a 32-bit readable/writable register that selects the format used in I/O operations of serial ports A from MONO, MONO_Delay, PCM, I2S, TDM, and TDM_Delay.

When TDM and TDM_Delay are selected, the number of channels should be specified.

Bit:	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	FMT[2:0]			—	NCH[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6 to 4	FMT[2:0]	011	R/W	Format Select 000: MONO (1 channels 001: MONO Delay (1 channel) 010: PCM (2 channels) 011: I2S (2 channels) 100: TDM (1 to 8 channels) 101: TDM Delay (1 to 8 channels) 110: Setting prohibited 111: Setting prohibited
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
2 to 0	NCH[2:0]	000	R/W	These bits specify the number of channels for the TDM and TDM_Delay formats. When selecting the modes other than TDM and TDM_Delay, specify B'000. 000: 1 channel 001: 2 channels 010: 3 channels 011: 4 channels 100: 5 channels 101: 6 channels 110: 7 channels 111: 8 channels

51.3.5 Port A Input FIFO Control Register (A_DIFF_CTL)

A_DIFF_CTL is a 32-bit readable/writable register that sets the condition for generating interrupt sources of serial port A input FIFOs. The FIFO clear initializes the access pointer to the on-chip RAM.

It also deletes the history of overflow and underflow errors.

Bit:	23	22	21	20	19	18	17	16
	—	—	IHC[1:0]		—	—	—	—
Initial value:	0	0	0	1	0	0	0	0
R/W:	R	R	R/W	R/W	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/(W)*

Bit	Bit Name	Initial Value	R/W	Description
31, 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
21, 20	IHC[1:0]	01	R/W	Condition for generating interrupt source 00: Full state 01: Number of data is over half the FIFO capacity. 10: More than 1 sample of data is in FIFOs. 11: Setting prohibited (empty state)
19 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	CLR	0	R/(W)*	FIFO Clear This bit initializes the access pointer and the error history. This bit is always read as 0. 0: When only the interrupt source condition is changed, the write value should be 0. 1: Clears FIFOs.

Note: * If 1 is written to the CLR bit, it is asserted for 1 pulse and cleared to B'0.

51.3.6 Port A Input FIFO Status Register (A_DIFF_ST)

A_DIFF_ST is a 32-bit readable/writable register. It can be used to read the input FIFO states for serial ports A, the number of stored sample data, and the history of overflow and underflow errors.

The OF and UF bits clear the history when they are written to 0.

Bit:	23	22	21	20	19	18	17	16
	—	—	ST[1:0]		—	—	—	SZ[8]
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SZ[7:0]								—	—	—	OF	—	—	—	UF
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31, 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
21, 20	ST[1:0]	00	R	FIFO State 00: Empty state. 01: Less than half of data areas are occupied. 10: More than half of data areas are occupied. 11: Full state.
19 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
16 to 8	SZ[8:0]	H'000	R	Number of Sample Data These bits indicate the number of sample data stored in FIFOs. The maximum value varies depending on the number of channels selected for the format. The maximum number of sample data for each channel is shown below (if 256 words of DP-RAM is connected). If more data than the maximum number in the parenthesis are read, an underflow occurs. FIFOs are used in 4-channel units in 3-channel mode and in 8-channel units in 5- to 7-channel mode, meaning that more FIFOs than the required size of DP-RAM are used. The DSP should take into account the maximum number of writes for these extra FIFOs. 1 channel: 256 (256 × 1 = 256) 2 channels: 128 (128 × 2 = 256) 3 channels: 64 (64 × 3 = 192) 4 channels: 64 (64 × 4 = 256) 5 channels: 32 (32 × 5 = 160) 6 channels: 32 (32 × 6 = 192) 7 channels: 32 (32 × 7 = 224) 8 channels: 32 (32 × 8 = 256)
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	OF	0	R/(W)*	FIFO Error History 0: No error has occurred. 1: Overflow has occurred.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	UF	0	R/(W)*	FIFO Error History 0: No error has occurred. 1: Underflow has occurred.

Note: * The FIFO error history is cleared by writing 0 to this bit and retained by writing 1 to it.

51.3.7 Port A/B Clock Set Register (A_ACK_MD/B_ACK_MD)

A_ACK_MD/B_ACK_MD is a 32-bit readable/writable register. It generates the master clock used by serial ports A/B and selects master/slave operation of the LR and bit clocks used internally.

The master clock is generated from the external audio clock. The block diagram is shown in figure 51.2.

Bit	Bit Name	Initial Value	R/W	Description
31 to 15	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
14 to 12	ACKMD[1:0]	000	R/W	These bits specify the audio clock to generate the master LR clock. Select the audio clock (fs) to be input for the sampling frequency (fs). 000: 512 fs 001: 256 fs 010: 128 fs 011: 64 fs 100: 32 fs Note: When selecting SPDIF(PCM or stream), select 512 fs/256 fs/128 fs.
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10 to 8	BPFMD[1:0]	001	R/W	These bits set the division ratio of the master bit clock. Some settings are unavailable depending or the format and the input audio clock. Refer to table 51.5. 000: 32bit/fs 001: 64bit/fs 010: 128bit/fs 011: 256bit/fs 100: 512bit/fs 101: Reserve 110: Reserve 111: 16bit/fs

Bit	Bit Name	Initial Value	R/W	Description
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	DIMD	0	R/W	DIIS Module Master/Slave Select 0: Slave operation 1: Master operation
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	DOMD	0	R/W	DOIS Module Master/Slave Select 0: Slave operation 1: Master operation

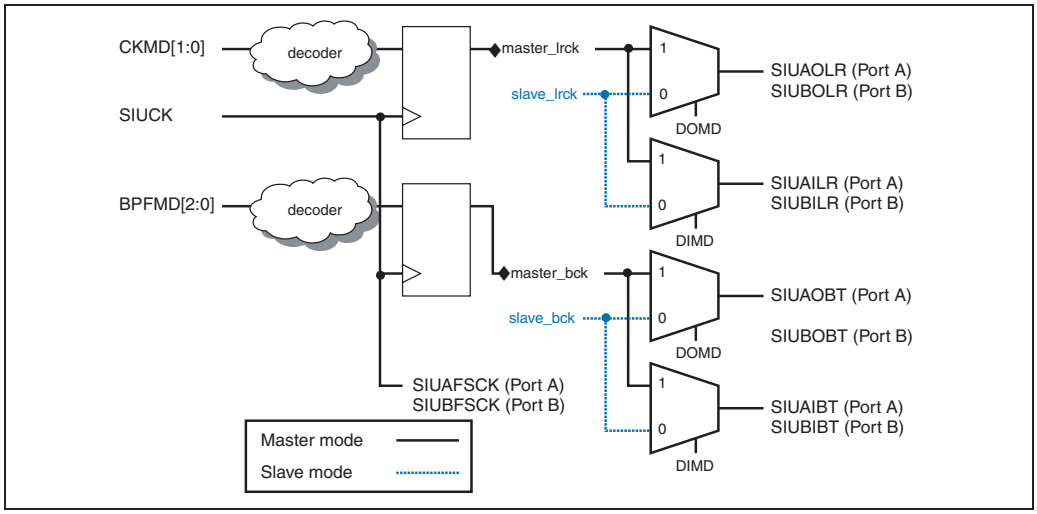


Figure 51.2 Master Clock Generation, I/O Operations, Master/Slave Selection

Table 51.5 List of Supported Formats

	MONO, MONO Delay	I2S, PCM	TDM, TDM Delay
Operating Clock	**BPFMD**	**BPFMD**	**BPFMD**
Master	64 bit/fs	64 bit/fs	(*)
ACKMD: 64 fs	32 bit/fs		
Master	128 bit/fs	128 bit/fs	(*)
ACKMD: 128 fs	64 bit/fs	64 bit/fs	
	32 bit/fs		
Master	256 bit/fs	256 bit/fs	256 bit/fs
ACKMD: 256 fs	128 bit/fs	128 bit/fs	
	64 bit/fs	64 bit/fs	
	32 bit/fs		
Master	512 bit/fs	512 bit/fs	512 bit/fs
ACKMD: 512 fs	256 bit/fs	256 bit/fs	256 bit/fs
	128 bit/fs	128 bit/fs	
	64 bit/fs	64 bit/fs	
	32 bit/fs		
Slave	512 bit/fs	512 bit/fs	512 bit/fs
	256 bit/fs	256 bit/fs	256 bit/fs
	128 bit/fs	128 bit/fs	
	64 bit/fs	64 bit/fs	
	32 bit/fs		

Note: * In TDM/TDM Delay modes, select 256 fs and 512 fs.

51.3.8 Port A/B Clock Invert control register (A_ACK_RV/B_ACK_RV)

A_ACK_RV/B_ACK_RV is a 32-bit readable/writable register that selects inversion of the master and slave clocks for serial ports A/B. They can be inverted according to the external interface specifications.

Bit:	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	LRM	—	—	—	BRM	—	—	—	LRS	—	—	—	BRS
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	LRM	0	R/W	Master LR Clock Inversion 0: Clock not inverted 1: Clock inverted
11 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	BRM	0	R/W	Master Bit Clock Inversion 0: Clock not inverted 1: Clock inverted
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	LRS	0	R/W	Slave LR Clock Inversion 0: Clock not inverted 1: Clock inverted
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
0	BRS	0	R/W	Slave Bit Clock Inversion 0: Clock not inverted 1: Clock inverted

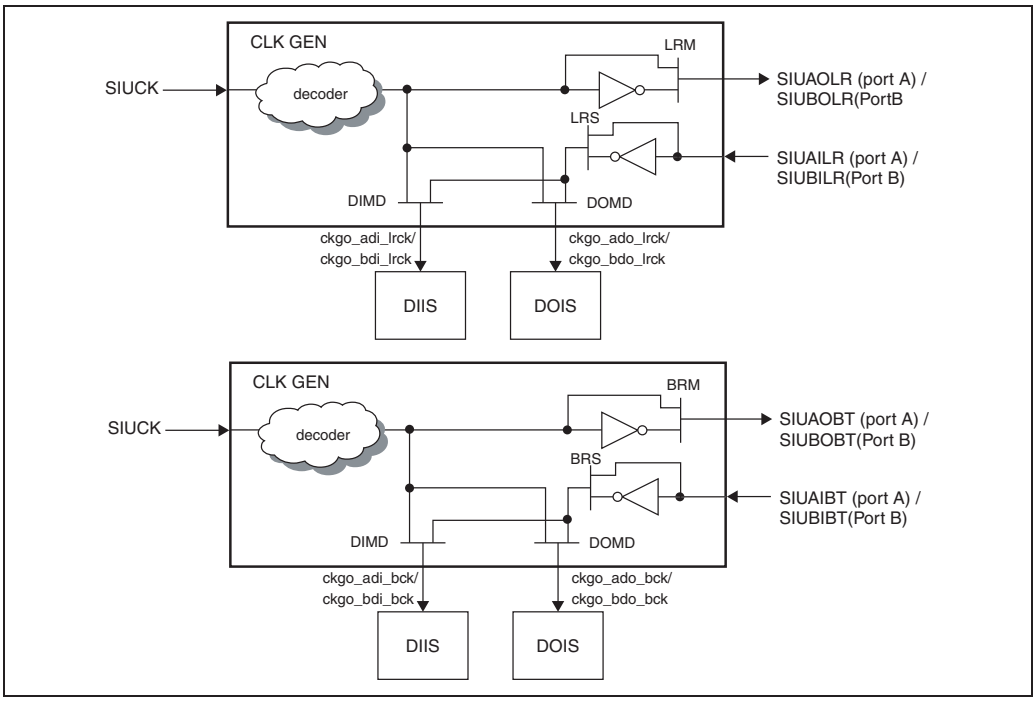


Figure 51.3 Master/Slave Clock Inversion Selector

Only one clock system (master output, bit and LR clocks for slave input pins) can be generated for one serial port. Thus, master-master and slave-slave operations with different formats and different bit and LR clocks cannot be performed on the same serial port.

To perform simultaneous input and output operations with different formats, bit clocks, and LR clocks, configure those operations for port A and port B separately.

51.3.9 Port A Read Data Register (A_DIDT)

A_DIDT is a 32-bit read-only register that can be used to read data stored in serial ports A input FIFOs. If FIFOs are empty, a read causes an underflow error.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
									DIDT[23:16]							
Initial value:									0	0	0	0	0	0	0	0
R/W:									R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DIDT[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DIDT[31:0]	H'00 0000	R	These bits contain data from input FIFOs. This register is read-only.

51.3.10 Port A/B Write Data Register (A_DODT/B_DODT)

A_DODT/B_DODT is a 32-bit write-only register that can be used to write data to serial ports A/B output FIFOs. If FIFOs are full, a write causes an overflow error.

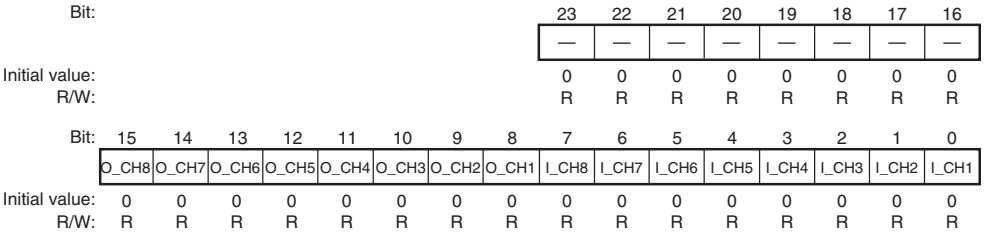
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
									DODT[23:16]							
Initial value:									0	0	0	0	0	0	0	0
R/W:									W	W	W	W	W	W	W	W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DODT[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DODT[31:0]	H'00 0000	W	These bits contain data to output FIFOs. This register is write-only.

51.3.11 Port A/B MUTE State (A_MUTE_ST/B_MUTE_ST)

A_MUTE_ST/B_MUTE_ST is a 32-bit read-only register that indicates the MUTE state for each channel in I/O operations on ports A/B.



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	O_CH8	0	R	Port A Output MUTE State 0: Channel 8 MUTE disabled 1: Channel 8 MUTE on
14	O_CH7	0	R	Port A Output MUTE State 0: Channel 7 MUTE off 1: Channel 7 MUTE on
13	O_CH6	0	R	Port A Output MUTE State 0: Channel 6 MUTE off 1: Channel 6 MUTE on
12	O_CH5	0	R	Port A Output MUTE State 0: Channel 5 MUTE off 1: Channel 5 MUTE on
11	O_CH4	0	R	Port A Output MUTE State 0: Channel 4 MUTE off 1: Channel 4 MUTE on
10	O_CH3	0	R	Port A Output MUTE State 0: Channel 3 MUTE off 1: Channel 3 MUTE on

Bit	Bit Name	Initial Value	R/W	Description
9	O_CH2	0	R	Port A Output MUTE State 0: Channel 2 MUTE off 1: Channel 2 MUTE on
8	O_CH1	0	R	Port A Output MUTE State 0: Channel 1 MUTE off 1: Channel 1 MUTE on
7	I_CH8	0	R	Port A Input MUTE State 0: Channel 8 MUTE off 1: Channel 8 MUTE on *Port B is reserve bit
6	I_CH7	0	R	Port A Input MUTE State 0: Channel 7 MUTE off 1: Channel 7 MUTE on *Port B is reserve bit
5	I_CH6	0	R	Port A Input MUTE State 0: Channel 6 MUTE off 1: Channel 6 MUTE on *Port B is reserve bit
4	I_CH5	0	R	Port A Input MUTE State 0: Channel 5 MUTE off 1: Channel 5 MUTE on *Port B is reserve bit
3	I_CH4	0	R	Port A Input MUTE State 0: Channel 4 MUTE off 1: Channel 4 MUTE on *Port B is reserve bit
2	I_CH3	0	R	Port A Input MUTE State 0: Channel 3 MUTE off 1: Channel 3 MUTE on *Port B is reserve bit
1	I_CH2	0	R	Port A Input MUTE State 0: Channel 2 MUTE off 1: Channel 2 MUTE on

Bit	Bit Name	Initial Value	R/W	Description
				*Port B is reserve bit
0	I_CH1	0	R	Port A Input MUTE State 0: Channel 1 MUTE off 1: Channel 1 MUTE on *Port B is reserve bit

51.3.12 Port A/B DMA control register [Output] (A_OUT_DMA/B_OUT_DMAC)

A_OUT_DMAC/B_OUT_DMAC is a 32-bit readable/writable register that can be accessed by CPU.

Bit	Bit Name	Initial Value	R/W	Description
31 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5 to 4	VDMD	00	R/W	Setting valid data 00: Package in front 01: Package in the back 10: Stream mode(16bit * 2) 11: Reserve When using PCM format or SPDIF (IEC60958) format, set “10”. When using SPDIF (IEC61937) format, set “10”
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	DMA_ON	0	R/W	DMA active bit 0: DMA Off 1: DMA On

1) Package in front

Byte address	31	0
0–3	dat0[23:0]	don't care
4–7	dat1[23:0]	don't care
8–C	dat2[23:0]	don't care

2) Package in the back

Byte address	31	0
0–3	don't care	dat0[23:0]
4–7	don't care	dat1[23:0]
8–C	don't care	dat2[23:0]

3) Stream mode (16bit * 2)

Byte address	31	0
0–3	dat0[15:0]	dat1[15:0]
4–7	dat2[15:0]	dat3[15:0]
8–C	dat4[15:0]	dat5[15:0]

51.3.13 Port A/B output control register (A_OUT_SEL/B_OUT_SEL)

A_OUT_SEL/B_OUT_SEL is a 32-bit readable/writable register that control serial output. When using SPDIF (IEC60958) format, set “00” to SO_MD bits.

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	FCLR	0	R/W	Clear frame number of SPDIF 0: Keep value 1: Initialize value.
19 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	DMMD	0	R/W	Select SPDIF output timing when output data 1/2 full of FIFO. 0: Output Biphase only 1: Output Biphase and serial data
3 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1 to 0	SO_MD	01	R/(W)*	Port A Output FIFO Interrupt 00: serial output (OFF) Biphase output (OFF) 01: serial output (ON) Biphase output (OFF) 10: serial output (OFF) Biphase output (ON) 11: serial output (ON) Biphase output (ON)

51.3.14 Port A/B output SPDIF state register (A_OUT_SPST/B_OUT_SPST)

A_OUT_SPST/B_OUT_SPST is a 32-bit readable/writable register. This register change state information of channel and value of interrupt.

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 8	FSIZE	00000000	R	Count value of sample of SPDIF (IEC:60958) 00000000: ready 00000001: first frame … 11000000: last frame (192)
7 to 0	ESIZE	01100000	R/W	Set value of interrupt frame of SPDIF (IEC:60958) 00000000: ready 00000001: first frame … 11000000: last frame (192)

51.3.15 Port A DMA control register [Input] (A_IN_DMAC)

A_OUT_DMAC is a 32-bit readable/writable register that can be accessed by CPU.

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	VDMD	0	R/W	Setting valid data 0: Package in front 1: Package in the back
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	DMA_ON	0	R/W	DMA active bit 0: DMA Off 1: DMA On

51.3.16 Port A input control register (A_IN_SEL)

A_IN_SEL is a 32-bit readable/writable register that control serial input.

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	SI_MD	1	R/W	Select serial input mode 0: SI-IF (Off) 1: SI-IF (On)

51.3.17 Port A/B master clock control register (A_MST_CTLR/B_MST_CTLR)

A_MST_CTLR/B_MST_CTLR is a 32-bit readable/writable register that fix signal in SPDIF mode.

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	BP	0	R/W	Fix the signal of Biphase output 0: Fix Low (On) 1: Fix Low (Off)
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	SE	0	R/W	Fix the master clock 0: Fix Low (On) 1: Fix Low (Off)

51.3.18 Timer set register (TMR_CTL)

TMR_CTL is a 32-bit readable/writable register that counts value of sample, Output of port A, port A and Input of port A. If value of counter is overflow, FSI2 interrupt occur.

Bit	Bit Name	Initial Value	R/W	Description
31 to 20	AI	1101	R/W	Sampling frequency of Port A input 0000: 1 0001: 2 0010: 4 0011: 8 0100: 16 0101: 32 0110: 64 0111: 128 1000: 256 1001: 512 1010: 1024 1011: 2048 1100: 4096 1101: 8192 1110: 16384 1111: 32768
19 to 16	AO	1101	R/W	Sampling frequency of Port A output same function (bit 31 to 20)
15 to 12	—	1101	R	Reserved These bits are always read as 1101. The write value should always be 1101.
11 to 8	BO	1101	R/W	Sampling frequency of Port B output same function (bit 31 to 20)
0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

51.3.19 Timer clear register (TMR_CLR)

TMR_CLR is a 32-bit readable/writable register that clear the value of counter.

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	AI_CLR	0	R/W	Clear the value of counter for Port A input. 0: keep 1: clear
19 to 17	—	All 0	R	Reserved These bits are always read as 1101. The write value should always be 1101.
16	AO_CLR	0	R/W	Clear the value of counter for Port A output. 0: keep 1: clear
15 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	BO_CLR	0	R/W	Clear the value of counter for Port B output. 0: keep 1: clear
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

51.3.20 Interrupt clear register (INT_CLR)

INT_CLR is a 32-bit readable/writable register that clear interrupts to CPU.

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	CPIC	0	R/W	Clear the interrupt to CPU. 0: keep 1: clear
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

51.3.21 CPU Interrupt State Register (CPU_INT_ST)

CPU_INT_ST is a 32-bit readable/writable register that retains 4 interrupt sources separately. Only writing 0 to clear is accepted. Writing 1 does not change the bit value. To clear a specific interrupt source, write 0 to the corresponding bit and 1 to the other bits.

The interrupt state register is set if the specified interrupt condition matches the FIFO state while the corresponding interrupt mask is cleared. If an interrupt source is cleared at the same time as the interrupt source occurs, the interrupt condition takes precedence.

Bit:	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	IIB	—	—	—	IOB	—	—	—	IIA	—	—	—	IOA
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/(W)*	R	R	R	R/(W)*	R	R	R	R/(W)*	R	R	R	R/(W)*

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	IESTTAI	0	R/W	Factor of timer interrupt for port A input 0: Clear 1: Keep
19	IESTOEBO	0	R/W	Factor of end interrupt for port B output 0: Clear 1: Keep
18	IESTOEAO	0	R/W	Factor of end interrupt for port A output 0: Clear 1: Keep
17	IESTTBO	0	R/W	Factor of timer interrupt for port B 0: Clear 1: Keep
16	IESTTAO	0	R/W	Factor of timer interrupt for port A 0: Clear 1: Keep

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11	IESTSEBO	0	R/W	Factor of next SPDIF stream interrupt for port B 0: Clear 1: Keep
10	IESTBEBO	0	R/W	Factor of interrupt that update information of SPDIF parameter for port B 0: Clear 1: Keep
9	IESTEBO	0	R/W	Factor of FIFO Error interrupt for port B output 0: Clear 1: Keep
8	IESTBO	0	R/W	Factor of FIFO state interrupt for port B output 0: Clear 1: Keep
7 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	IESTEAI	0	R/W	Factor of FIFO Error interrupt for port A input 0: Clear 1: Keep
4	IESTAI	0	R/W	Factor of FIFO state interrupt for port A input 0: Clear 1: Keep
3	IESTSEAO	0	R/W	Factor of next SPDIF stream interrupt for port A 0: Clear 1: Keep
2	IESTBEAO	0	R/W	Factor of interrupt that update information of SPDIF parameter for port B 0: Clear 1: Keep
1	IESTEAO	0	R/W	Factor of FIFO Error interrupt for port A output 0: Clear

Bit	Bit Name	Initial Value	R/W	Description
				1: Keep should always be 0.
0	IESTAO	0	R/W	Factor of FIFO state interrupt for port B output 0: Clear 1: Keep

Note: * Writing 0 to this bit clears the interrupt source. Writing 1 does not change the bit value.

51.3.22 CPU Interrupt Source Mask Set Register (CPU_IEMSK)

IEMASK is a 32-bit readable/writable register that masks the interrupt source for each FIFO. If this register masks an interrupt source, the interrupt source is not enabled even if the IMASK register below unmasks the interrupt signal. Thus, the interrupt does not occur.

Bit:	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	MIRB	—	—	—	MORB	—	—	—	MIRA	—	—	—	MORA
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	IEMSKTBI	0	R/W	Port A Input Timer Interrupt Request Mask 0: Disabled(Mask) 1: Enabled
19	IEMSKOEBO	0	R/W	Port B output End Interrupt Request Mask 0: Disabled(Mask) 1: Enabled
18	IEMSKOEAO	0	R/W	Port A output End Interrupt Request Mask 0: Disabled(Mask) 1: Enabled
17	IEMSKTBO	0	R/W	Port B Output Timer Interrupt Request Mask 0: Disabled(Mask) 1: Enabled
16	IEMSKTAO	0	R/W	Port A Output Timer Interrupt Request Mask 0: Disabled(Mask) 1: Enabled
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value

Bit	Bit Name	Initial Value	R/W	Description
				should always be 0.
11	IEMSKSEBO	0	R/W	Port B output next SPDIF stream Request Mask 0: Disabled(Mask) 1: Enabled
10	IEMSKBEBO	0	R/W	Port B Output update information of SPDIF Request Mask 0: Disabled(Mask) 1: Enabled
9	IEMSKEBO	0	R/W	Port B output FIFO Error Request Mask 0: Disabled(Mask) 1: Enabled
8	IEMSKBO	0	R/W	Port B output FIFO status Request Mask 0: Disabled(Mask) 1: Enabled
7 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	IEMSKEAI	0	R/W	Port A input FIFO Error Request Mask 0: Disabled(Mask) 1: Enabled
4	IEMSKAI	0	R/W	Port A input FIFO status Request Mask 0: Disabled(Mask) 1: Enable
3	IEMSKSEAO	0	R/W	Port A output next SPDIF stream Request Mask 0: Disabled(Mask) 1: Enabled
2	IEMSKBEAO	0	R/W	Port A Output update information of SPDIF Request Mask 0: Disabled(Mask) 1: Enabled
1	IEMSKEAO	0	R/W	Port A output FIFO Error Request Mask 0: Disabled(Mask) 1: Enabled

Bit	Bit Name	Initial Value	R/W	Description
0	IEMSKAO	0	R/W	Port A output FIFO status Request Mask 0: Disabled(Mask) 1: Enabled

51.3.23 CPU Interrupt Signal Mask Set Register (CPU_IMSK)

CPU_IMASK is a 32-bit readable/writable register that masks the interrupt signal for each FIFO to the DSP. If an interrupt source for a FIFO whose interrupt signal is unmasked, the interrupt request signal occurs.

Bit:	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	MIB	—	—	—	MOB	—	—	—	MIA	—	—	—	MOA
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	IMSKTAI	0	R/W	Port A Input Timer Interrupt Signal Mask 0: Disabled(Mask) 1: Enabled
19	IMSKOEBO	0	R/W	Port B output End Interrupt Request Mask 0: Disabled(Mask) 1: Enabled.
18	IMSKOEAO	0	R/W	Port A output End Interrupt Request Mask 0: Disabled(Mask) 1: Enabled.
17	IMSKTBO	0	R/W	Port B Output Timer Interrupt Request Mask 0: Disabled(Mask) 1: Enabled

Bit	Bit Name	Initial Value	R/W	Description
16	IMSKTAO	0	R/W	Port A Output Timer Interrupt Request Mask 0: Disabled(Mask) 1: Enabled
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11	IMSKSEBO	0	R/W	Port B output next SPDIF stream Request Mask 0: Disabled(Mask) 1: Enabled
10	IMSKBEBO	0	R/W	Port B Output update information of SPDIF Request Mask 0: Disabled(Mask) 1: Enabled
9	IMSKEBO	0	R/W	Port B output FIFO Error Request Mask 0: Disabled(Mask) 1: Enabled
8	IMSKBO	0	R/W	Port B output FIFO status Request Mask 0: Disabled(Mask) 1: Enabled
7 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	IMSKEAI	0	R/W	Port A input FIFO Error Request Mask 0: Disabled(Mask) 1: Enabled
4	IMSKAI	0	R/W	Port A input FIFO status Request Mask 0: Disabled(Mask) 1: Enable
3	IMSKSEAO	0	R/W	Port A output next SPDIF stream Request Mask 0: Disabled(Mask) 1: Enabled
2	IMSKBEAO	0	R/W	Port A Output update information of SPDIF Request Mask 0: Disabled(Mask)

Bit	Bit Name	Initial Value	R/W	Description
				1: Enabled
1	IMSKEAO	0	R/W	Port A output FIFO Error Request Mask 0: Disabled(Mask) 1: Enabled
0	IMSKAO	0	R/W	Port A output FIFO status Request Mask 0: Disabled(Mask) 1: Enabled

51.3.24 DSP Interrupt State Register (DSP_INT_ST)

DSP_INT_ST is a 32-bit readable/writable register that retains 4 interrupt sources separately. Only writing 0 to clear is accepted. Writing 1 does not change the bit value. To clear a specific interrupt source, write 0 to the corresponding bit and 1 to the other bits.

The interrupt state register is set if the specified interrupt condition matches the FIFO state while the corresponding interrupt mask is cleared. If an interrupt source is cleared at the same time as the interrupt source occurs, the interrupt condition takes precedence.

Bit:	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	IIB	—	—	—	IOB	—	—	—	IIA	—	—	—	IOA
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/(W)*	R	R	R	R/(W)*	R	R	R	R/(W)*	R	R	R	R/(W)*

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	IESTTAI	0	R/W	Factor of timer interrupt for port A input 0: Clear 1: Keep
19	IESTOEBO	0	R/W	Factor of end interrupt for port B output 0: Clear 1: Keep
18	IESTOEAO	0	R/W	Factor of end interrupt for port A output 0: Clear 1: Keep
17	IESTTBO	0	R/W	Factor of timer interrupt for port B 0: Clear 1: Keep
16	IESTTAO	0	R/W	Factor of timer interrupt for port A 0: Clear 1: Keep

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11	IESTSEBO	0	R/W	Factor of next SPDIF stream interrupt for port B 0: Clear 1: Keep
10	IESTBEBO	0	R/W	Factor of interrupt that update information of SPDIF parameter for port B 0: Clear 1: Keep
9	IESTEBO	0	R/W	Factor of FIFO Error interrupt for port B output 0: Clear 1: Keep
8	IESTBO	0	R/W	Factor of FIFO state interrupt for port B output 0: Clear 1: Keep
7 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	IESTEAI	0	R/W	Factor of FIFO Error interrupt for port A input 0: Clear 1: Keep
4	IESTAI	0	R/W	Factor of FIFO state interrupt for port A input 0: Clear 1: Keep
3	IESTSEAO	0	R/W	Factor of next SPDIF stream interrupt for port A 0: Clear 1: Keep
2	IESTBEAO	0	R/W	Factor of interrupt that update information of SPDIF parameter for port B 0: Clear 1: Keep
1	IESTEAO	0	R/W	Factor of FIFO Error interrupt for port A output 0: Clear

Bit	Bit Name	Initial Value	R/W	Description
				1: Keep should always be 0.
0	IESTAO	0	R/W	Factor of FIFO state interrupt for port B output 0: Clear 1: Keep

Note: * Writing 0 to this bit clears the interrupt source. Writing 1 does not change the bit value.

51.3.25 DSP Interrupt Source Mask Set Register (DSP_IEMSK)

DSP_IEMASK is a 32-bit readable/writable register that masks the interrupt source for each FIFO. If this register masks an interrupt source, the interrupt source is not enabled even if the DSP_IMASK register below unmasks the interrupt signal. Thus, the interrupt does not occur.

Bit:	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	MIRB	—	—	—	MORB	—	—	—	MIRA	—	—	—	MORA
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	IEMSKTBI	0	R/W	Port A Input Timer Interrupt Request Mask 0: Disabled(Mask) 1: Enabled
19	IEMSKOEBO	0	R/W	Port B output End Interrupt Request Mask 0: Disabled(Mask) 1: Enabled
18	IEMSKOEAO	0	R/W	Port A output End Interrupt Request Mask 0: Disabled(Mask) 1: Enabled
17	IEMSKTBO	0	R/W	Port B Output Timer Interrupt Request Mask 0: Disabled(Mask) 1: Enabled
16	IEMSKTAO	0	R/W	Port A Output Timer Interrupt Request Mask 0: Disabled(Mask) 1: Enabled
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value

Bit	Bit Name	Initial Value	R/W	Description
				should always be 0.
11	IEMSKSEBO	0	R/W	Port B output next SPDIF stream Request Mask 0: Disabled(Mask) 1: Enabled
10	IEMSKBEBO	0	R/W	Port B Output update information of SPDIF Request Mask 0: Disabled(Mask) 1: Enabled
9	IEMSKEBO	0	R/W	Port B output FIFO Error Request Mask 0: Disabled(Mask) 1: Enabled
8	IEMSKBO	0	R/W	Port B output FIFO status Request Mask 0: Disabled(Mask) 1: Enabled
7 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	IEMSKEAI	0	R/W	Port A input FIFO Error Request Mask 0: Disabled(Mask) 1: Enabled
4	IEMSKAI	0	R/W	Port A input FIFO status Request Mask 0: Disabled(Mask) 1: Enable
3	IEMSKSEAO	0	R/W	Port A output next SPDIF stream Request Mask 0: Disabled(Mask) 1: Enabled
2	IEMSKBEAO	0	R/W	Port A Output update information of SPDIF Request Mask 0: Disabled(Mask) 1: Enabled
1	IEMSKEAO	0	R/W	Port A output FIFO Error Request Mask 0: Disabled(Mask) 1: Enabled

Bit	Bit Name	Initial Value	R/W	Description
0	IEMSKAO	0	R/W	Port A output FIFO status Request Mask 0: Disabled(Mask) 1: Enabled

51.3.26 DSP Interrupt Signal Mask Set Register (DSP_IMSK)

DSP_IMASK is a 32-bit readable/writable register that masks the interrupt signal for each FIFO to the DSP. If an interrupt source for a FIFO whose interrupt signal is unmasked, the interrupt request signal occurs.

Bit:	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	MIB	—	—	—	MOB	—	—	—	MIA	—	—	—	MOA
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	IMSKTAI	0	R/W	Port A Input Timer Interrupt Signal Mask 0: Disabled(Mask) 1: Enabled
19	IMSKOEBO	0	R/W	Port B output End Interrupt Request Mask 0: Disabled(Mask) 1: Enabled.
18	IMSKOEAO	0	R/W	Port A output End Interrupt Request Mask 0: Disabled(Mask) 1: Enabled.
17	IMSKTBO	0	R/W	Port B Output Timer Interrupt Request Mask 0: Disabled(Mask) 1: Enabled

Bit	Bit Name	Initial Value	R/W	Description
16	IMSKTAO	0	R/W	Port A Output Timer Interrupt Request Mask 0: Disabled(Mask) 1: Enabled
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11	IMSKSEBO	0	R/W	Port B output next SPDIF stream Request Mask 0: Disabled(Mask) 1: Enabled
10	IMSKBEBO	0	R/W	Port B Output update information of SPDIF Request Mask 0: Disabled(Mask) 1: Enabled
9	IMSKEBO	0	R/W	Port B output FIFO Error Request Mask 0: Disabled(Mask) 1: Enabled
8	IMSKBO	0	R/W	Port B output FIFO status Request Mask 0: Disabled(Mask) 1: Enabled
7 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	IMSKEAI	0	R/W	Port A input FIFO Error Request Mask 0: Disabled(Mask) 1: Enabled
4	IMSKAI	0	R/W	Port A input FIFO status Request Mask 0: Disabled(Mask) 1: Enable
3	IMSKSEAO	0	R/W	Port A output next SPDIF stream Request Mask 0: Disabled(Mask) 1: Enabled
2	IMSKBEAO	0	R/W	Port A Output update information of SPDIF Request Mask 0: Disabled(Mask)

Bit	Bit Name	Initial Value	R/W	Description
				1: Enabled
1	IMSKEAO	0	R/W	Port A output FIFO Error Request Mask 0: Disabled(Mask) 1: Enabled
0	IMSKAO	0	R/W	Port A output FIFO status Request Mask 0: Disabled(Mask) 1: Enabled

51.3.27 MUTE Set Register (MUTE)

MUTE is a 32-bit readable/writable register that enables the MUTE function of the inputs/outputs for ports A/B. Set MUTE on/off after selecting MUTE mode. For the mute timing specifications, refer to section 51.5, MUTE Specifications.

Bit:	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	TSIB	TYIB	—	—	TSOB	TYOB	—	—	TSIA	TYIA	—	—	TSOA	TYOA
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	TSOB	0	R/W	Port B Output MUTE 0: MUTE off 1: MUTE on
8	TYOB	0	R/W	Port B Output MUTE Mode Set 0: Normal MUTE 1: Zero cross MUTE
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	TSIA	0	R/W	Port A Input MUTE 0: MUTE off 1: MUTE on
4	TYIA	0	R/W	Port A Input MUTE Mode Set 0: Normal MUTE 1: Zero cross MUTE
3, 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
1	TSOA	0	R/W	Port A Output MUTE 0: MUTE off 1: MUTE on
0	TYOA	0	R/W	Port A Output MUTE Mode Set 0: Normal MUTE 1: Zero cross MUTE

51.3.28 Clock Reset Set Register (ACK_RST)

ACK_RST is a 32-bit readable/writable register. During reset, it masks the LR and bit clocks that are output from the clock-generating block. Clear the reset after setting formats and clocks by follow the operation flow.

Bit:	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	CRB	—	—	—	CRA
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	PBCR	0	R/W	Port B Clock Reset 0: Issues a reset. 1: Clear the reset.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	PACR	0	R/W	Port A Clock Reset 0: Issues a reset. 1: Clears the reset.

Note: * This bit should be asserted for longer than the audio clock period so that the counter synchronized with it is reset.

51.3.29 Software Reset Set Register (SOFT_RST)

SOFT_RST is a 32-bit readable/writable register that initializes the internal registers.

Bit:	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	SRB	—	—	—	SRA	—	—	—	IR	—	—	—	SR
Initial value:	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
R/W:	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	PBSR	1	R/W	Port B Software Reset This bit performs a port B FIFO clear. 0: Issues a reset. 1: Clears the reset.
11 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	PASR	1	R/W	Port A Software Reset This bit performs a port A FIFO clear. 0: Issues a reset. 1: Clears the reset.
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	IR	1	R/W	Interrupt Reset This bit negates the interrupt signal without receiving an acknowledge. 0: Issues a reset. 1: Clears the reset.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value

Bit	Bit Name	Initial Value	R/W	Description
				should always be 0.
0	FSISR	1	R/W	Software Reset This bit initializes all registers. 0: Issues a reset. 1: Clears the reset.

51.3.30 FIFO Size Register (FIFO_SZ)

FIFO_SZ is a 32-bit read-only register that indicates the on-chip RAM capacity.

Bit:	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	BI[2:0]			—	BO[2:0]			—	AI[2:0]			—	AO[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 8	BO[2:0]	000	R	Port B Output FIFO Capacity These bits indicate the on-chip RAM capacity. 000: 256 words 001: 512 words 010: 1024 words 011: 2048 words 111: Out-of-spec capacity is set (error) Note: No value other than listed above is output.

Bit	Bit Name	Initial Value	R/W	Description
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6 to 4	AI[2:0]	000	R	Port A Input FIFO Capacity These bits indicate the on-chip RAM capacity. 000: 256 words 001: 512 words 010: 1024 words 011: 2048 words 111: Out-of-spec capacity is set (error) Note: No value other than listed above is output.
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2 to 0	AO[2:0]	000	R	Port A Output FIFO Capacity These bits indicate the on-chip RAM capacity. 000: 256 words 001: 512 words 010: 1024 words 011: 2048 words 111: Out-of-spec capacity is set (error) Note: No value other than listed above is output.

51.3.31 Clock select register (CLK_SEL)

CLK_SEL is a 32-bit readable/writable register that select clock for FSI2.This register access from CPU only by HPB bus only.

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	DSPS	0	R/W	Select FSI2 clock. 0: Bus clock(HP clock) 1: DSP clock(SPU clock)

Note: Not change this register value while FSI2 transfer data.

51.3.32 Swap select register (SWAP_SEL)

SWAP_SEL is a 32-bit readable/writable register that select clock for FSI2.This register access from CPU only by HPB bus only.

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1 to 0	BW	0	R/W	Select SWAP mode. 00: normal 01: Byte swap 10: Word swap 11: Byte word swap

Note: Not change this register value while FSI2 transfer data.

51.3.33 HPB software reset register (HPB_SRST)

SWAP_SEL is a 32-bit readable/writable register that select clock for FSI2.This register access from CPU only by HPB bus only.

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	HPBSR	1	R/W	HPB reset 0: Reset to HPB block 1: normal
19 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
16	DSPSR	0	R/W	DSP reset 0: Reset to DSP block 1: normal
15 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Note: Not change this register value while FSI2 transfer data.

51.3.34 SPDIF (60958) Port A/B channel state register (A_SP_CHST00, A_SP_CH01/ B_SP_CHST00, B_SP_CH01)

A_SP_CHST00, A_SP_CHST01, B_SP_CHST00 and B_SP_CHST01 are 32-bit readable/writable registers that set value of channel state by 1block.

Bit	Bit Name	Initial Value	R/W	Description
31 to 15	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
14	ST	0	R/W	Audio identification 0: Audio 1: except for audio Note: Set value “1”, when using stream mode.
13	ST	0	R/W	Copyright protection 0: protection 1: non-protection
12 to 10	ST	000	R/W	Select emphasis 000: non-emphasis 001: emphasis (50/15 micro sec) 010: reserve 011: reserve
9 to 8	—	00	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	ST	0	R/W	Category code 00000000: 2 channel general format 10000000: 2 channel CD 01000000: 2 channel PCM encoder/decoder 11000000: 2 channel DAT

51.3.35 SPDIF (60958) Port A/B user data register (A_SP_USD00 - A_SP_USD23/ B_SP_USD00 - B_SP_USD23)

A_SP_USD00 - A_SP_USD23, B_SP_USD00 - B_SP_USD22 and B_SP_USD23 are 32-bit readable/writable registers that set value of channel state by 1block.

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 0	US	All 0	R/W	User data

51.3.36 SPDIF (61937) Port A/B preamble pa register (A_SP_PA/ B_SP_PA)

A_SP_PA and B_SP_PA are 32-bit readable/writable registers that set value of preamble data.

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 0	PA	All 0	R/W	Preamble pa paremeter (IEC61937)

51.3.37 SPDIF (61937) Port A/B preamble pb register (A_SP_PB/ B_SP_PB)

A_SP_PB and B_SP_PB are 32-bit readable/writable registers that set value of preamble data.

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 0	PB	All 0	R/W	Preamble pb paremeter (IEC61937)

51.3.38 SPDIF (61937) Port A/B preamble pc register (A_SP_PC/ B_SP_PC)

A_SP_PC and B_SP_PC are 32-bit readable/writable registers that set value of preamble data.

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 0	PC	All 0	R/W	Preamble pc paremeter (IEC61937)

51.3.39 SPDIF (61937) Port A/B preamble pd register (A_SP_PD/ B_SP_PD)

A_SP_PD and B_SP_PD are 32-bit readable/writable registers that set value of preamble data.

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 0	PD	All 0	R/W	Preamble pd paremeter (IEC61937)

51.3.40 Port A/B Pause cycle register (A_SP_PS/ B_SP_PS)

A_SP_PS and B_SP_PS are 32-bit readable/writable registers that set value of pause cycle (IEC60958).

Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 0	PS	All 0	R/W	Set value of pause frame.

Do not set it excluding the following value.

Stream format	Value of 1 frame for pause
AC-3 data	3 frame(Recommend)
MPEG-1 layer 1 data	32 frame(Must)
MPEG-1 layer 2 or 3 data	
MPEG-2 without extension	
MPEG-2 data with extension	
MPEG-2 layer 1 low sampling frequency	64 frame(Must)
MPEG-2 layer 2 or 3 low sampling frequency	
MPEG-2 AAC	32 frame(Recommend)
MPEG-2 AAC and half-rate low sampling frequency	64 frame(Recommend)
MPEG-2 AAC and quarter-rate low sampling frequency	128 frame(Recommend)
MPEG-4 AAC	32 frame(Recommend)
MPEG-4 AAC and half-rate low sampling frequency	64 frame(Recommend)
MPEG-4 AAC and quarter-rate low sampling frequency	128 frame(Recommend)
MPEG-4 AAC double-rate high sampling frequency	16 frame(Recommend)

51.3.41 Port A/B Pause length register (A_SP_PL/ B_SP_PL)

A_SP_PL and B_SP_PL are 32-bit readable/writable registers that set value of pause all frame (IEC60958).

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 0	PL	All 0	R/W	Set value of pause frame.

Do not set it excluding the following value.

Stream format	Value of 1 frame for pause
AC-3 data	3 frame(1 frame) x N*
MPEG-1 layer 1 data	32 frame(1 frame) x N*
MPEG-1 layer 2 or 3 data	
MPEG-2 without extension	
MPEG-2 data with extension	
MPEG-2 layer 1 low sampling frequency	64 frame(1 frame) x N*
MPEG-2 layer 2 or 3 low sampling frequency	
MPEG-2 AAC	32 frame(1 frame) x N*
MPEG-2 AAC and half-rate low sampling frequency	64 frame(1 frame) x N*
MPEG-2 AAC and quarter-rate low sampling frequency	128 frame(1 frame) x N*
MPEG-4 AAC	32 frame(1 frame) x N*
MPEG-4 AAC and half-rate low sampling frequency	64 frame(1 frame) x N*
MPEG-4 AAC and quarter-rate low sampling frequency	128 frame(1 frame) x N*
MPEG-4 AAC double-rate high sampling frequency	16 frame(1 frame) x N*

Note: N = 1,2,3,… Set value of all of frame is 65535 frame or less.

51.3.42 Port A/B Frame size register (A_SP_FS/ B_SP_FS)

A_SP_FS and B_SP_FS are 32-bit readable/writable registers that set value of frame (IEC60958), when using SPDIF stream data.

Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 0	PL	All 0	R/W	Set value of frame while 1 frame.

Do not set it excluding the following value.

Stream format	Value of 1 frame
Null-data	3frame to 4096frame(Recommend)
AC3 data	1536 frame
Pause	-
MPEG-1 layer 1 data	384 frame
MPEG-1 layer 2 or 3 data, or MPEG-2 without extension	1152 frame
MPEG-2 data with extension	1152 frame
MPEG-2 AAC ADTS	1024 frame
MPEG-2 layer 1 low sampling frequency	768 frame
MPEG-2 layer 2 or 3 low sampling frequency	2304 frame
MPEG-2 AAC ADTS low sampling frequency	2048/4096 frame
MPEG-4 AAC	1024/2048/4096/512 frame

51.3.43 Interrupt select register (INT_SEL)

INT_SEL is 32-bit readable/writable registers that select redirection which DSP of SPU2 or INTC.

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 2	FMSI_SEL	00	R/W	Select redirection for FMSI 01: DSP of SPU2 only 10: INTC only
1 to 0	FSI_SEL	00	R/W	Select redirection for FSI2 01: DSP of SPU2 only 10: INTC only

51.4 Interface Specifications

51.4.1 FSI2 and SPU2 Connection Interface Specifications

The FSI2 uses an 8-bit address space (H'00 to H'FF). The FSI2 registers can be read and written via the SPU2 DSP/IO bus.

(1) BUFC Specifications

Figure 51.5 shows the data flow from read requests to the A_DIDT and B_DIDT registers to the data output.

To read data stored in input FIFOs continuously, the fsio_io_hold signal is maintained when the A_DIDT or B_DIDT register is read. When a read request is sent to the FSI2, the hold signal is not driven low and the read request is kept asserted until data are stored in buffers in the control block. Thus, data requests are generated continuously and the next data to be read are stored in the control block buffers.

Data can be read continuously with one wait like other registers by prefetching data in the control block buffers.

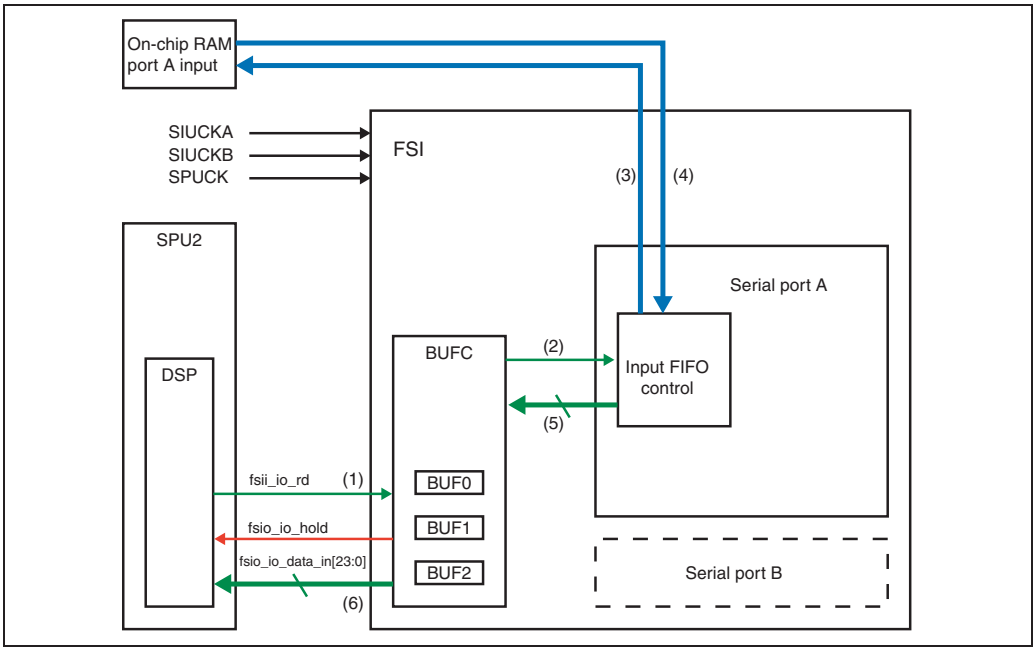


Figure 51.5 Block Diagram of Input FIFO Read Request

51.4.2 Clock Interface Specifications

A block diagram of clock signals is shown in figure 51.6.

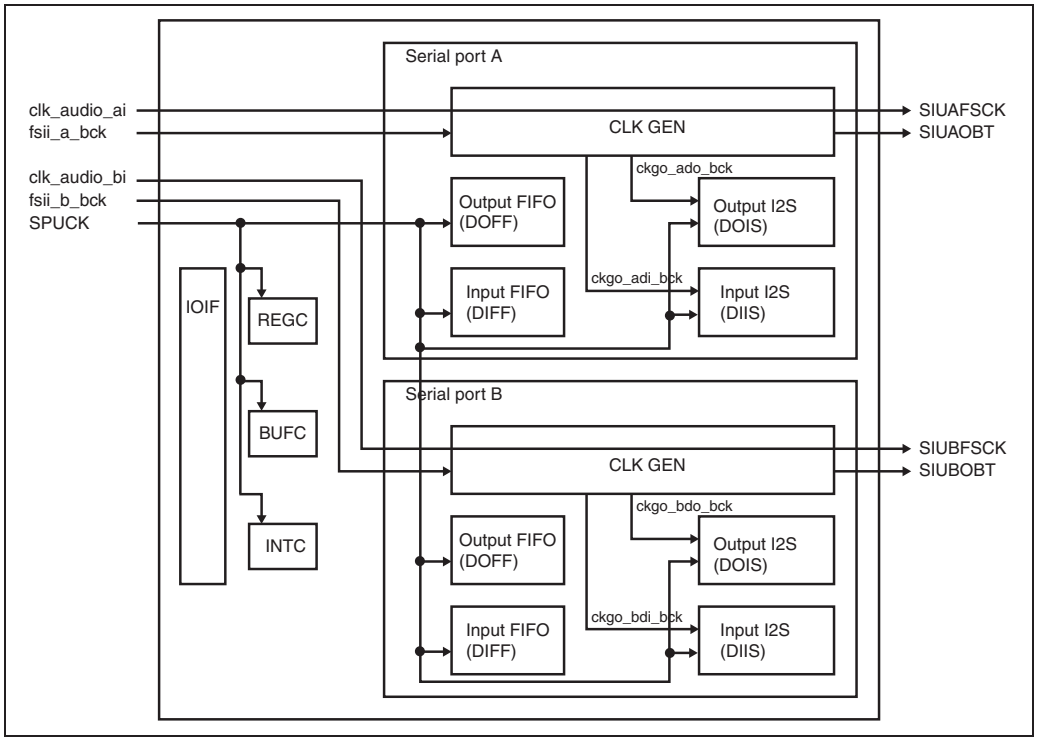


Figure 51.6 Block Diagram of FSI2 Clock Inputs

51.4.3 Reset Interface Specifications

Table 51.6 lists the FSI2 resets.

Table 51.6 FSI2 Rest Type, Initialization Register and Block

			Initializing Module							
Reset Name	**Register**	**Initialization Register**	**INTC**	**BUFC**	**REGC**	**CLK GEN**	**Output FIFO**	**Input FIFO**	**Output I2S**	**Input I2S**
Hardware reset	—	All registers	√							
Software reset	SOFT_RST.SR	All registers except software reset	√							√ (except FFs synchronized with the Bitclk)
Port A reset	SOFT_RST.SRA	Performs a port A FIFO clear.	—	—	—	—		√ (Port A only)		
Port B reset	SOFT_RST.SRB	Performs a port B FIFO clear.	—	—	—	—		√ (Port B only)		
Clock reset A	CLK_RST.CRA	—	—	—	—	√ (Port A)	—	—	—	—
Clock reset B	CLK_RST.CRB	—	—	—	—	√ (Port B)	—	—	—	—
Interrupt reset	SOFT_RST.IR	—	√ (fsio_int negated)	—	—	—	—	—	—	—
Port A output FIFO clear	A_DOFF_CTL.CLR	—	—	—	—	—	√ (Port A)	—	—	—
Port A input FIFO clear	A_DIFF_CTL.CLR	—	—	√ (Port A)	—	—	—	√ (Port A)	—	—
Port B output FIFO clear	B_DOFF_CTL.CLR	—	—	—	—	—	√ (Port B)	—	—	—
Port B input FIFO clear	B_DIFF_CTL.CLR	—	—	√ (Port B)	—	—	—	√ (Port B)	—	—

[Legend] √: Reset, —: Register retained

(1) Hardware Reset

Initializes all registers and modules.

(2) Software Reset

Initializes all registers except the software reset register (SOFT_RST.SR) and all modules. In master operation, the bit clock that is used for asynchronous passing may be fixed due to a clock reset, perform a software reset after resetting ports A/B (see (8) Procedures for Initializing the FSI2).

(3) Port A/B Reset

These are the reset signals to initialize the FFs that are synchronized with the bit clock.

Since the bit clock is used for asynchronous passing, this reset requires to wait for longer than 1 bit clock cycle after a register write to perform it.

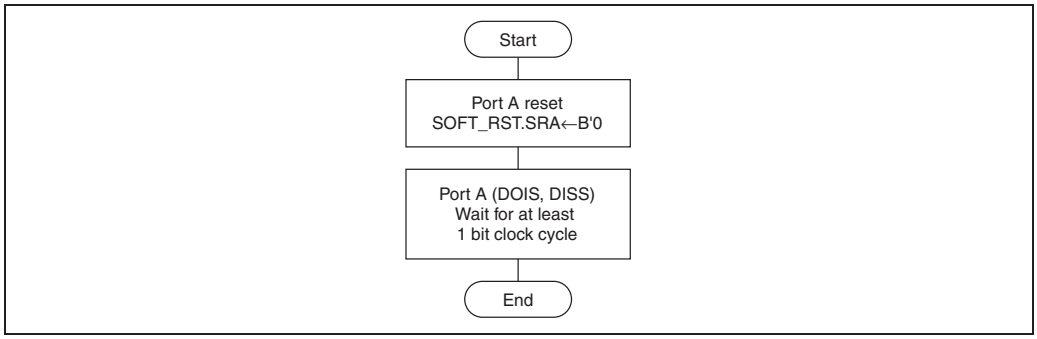


Figure 51.7 Flow of Port A Reset

(4) Clock Reset A/B

These are the reset signals to initialize the FFs that are synchronized with the audio clock.

Since the audio clock is used for asynchronous passing, this reset requires to wait for longer than 1 audio clock cycle after a register write to perform it.

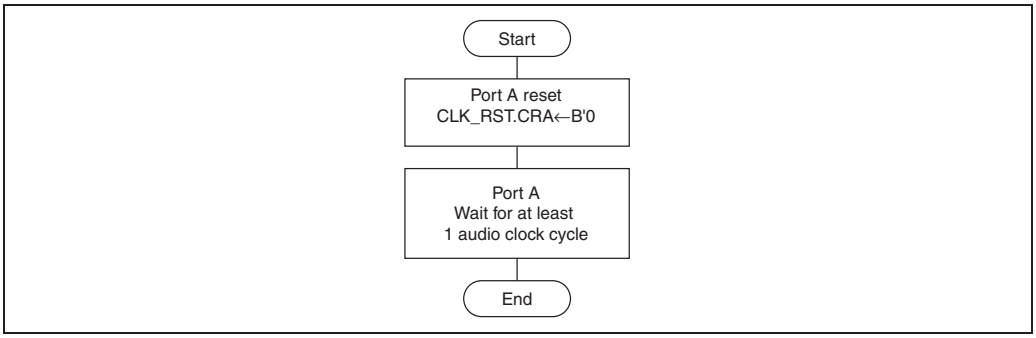


Figure 51.8 Flow of Clock Reset A

(5) Interrupt Reset

Negates the interrupt signal (fsio_int) when the corresponding register is written.

(6) Port A/B Output FIFO Clear

Clears the address pointer of the FIFO control block and the error history.

(7) Port A/B Input FIFO Clear

Clears the address pointer of the FIFO control block, the error history, and buffers for continuous 1-wait reads.

(8) Procedures for Initializing the FSI2

The procedures for initializing the FSI2 are shown in figure 51.9. There are two types of procedures: one by using a hardware reset and another by using a software reset. To achieve the same effect as a hardware reset, perform a software reset after port A/B reset (initializing the FFs that are synchronized with the bit clock).

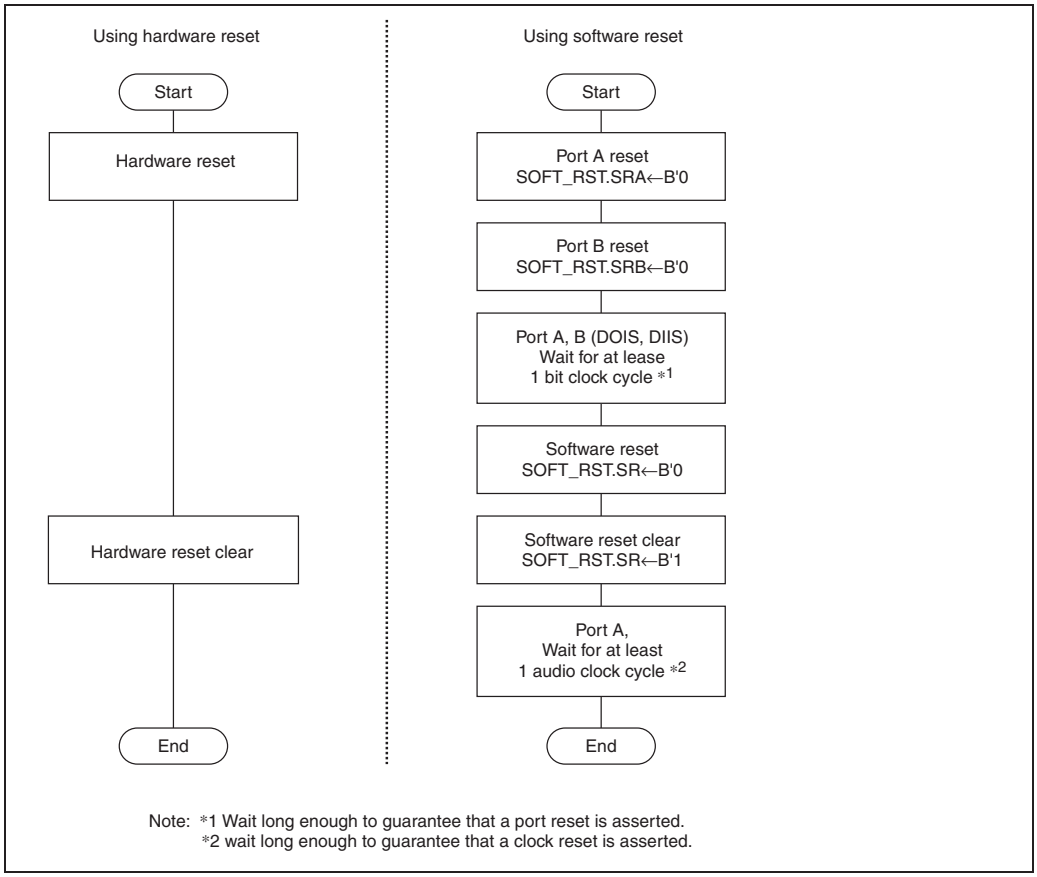


Figure 51.9 Operation Flow of FSI2 Initial States

51.4.4 Interrupt Interface Specifications

The FSI2 has an interrupt signal line for external modules. The positive interrupt signal is connected to SPU2 and the negative interrupt signal is connected to the CPU (INTC).

In normal operation, SPU2 handles interrupts and the CPU interrupt signal is not used.

The CPU interrupt signal is used for debugging where DSP programs of SPU2 are not started.

Table 51.7 shows the pin configurations in normal operation.

Table51.7 Interrupt Pin Configurations

Pin Name	Input/Output	Function	Polarity
fsio_int	Output	Interrupt requests to SPU2	High
fsii_int_ack	Input	In response to a request, SPU2 returns a 1-pulse acknowledge and the FSI2 drives fsio_int low.	High

In normal operation, the external interrupt signal (fsio_int) is asserted by any of four interrupt sources. Once the interrupt signal is asserted after it is negated by fsii_int_ack, it is never asserted again until at least one interrupt source is cleared (int_set=0).

Figure 51.10 shows a timing chart of the interrupt signal.

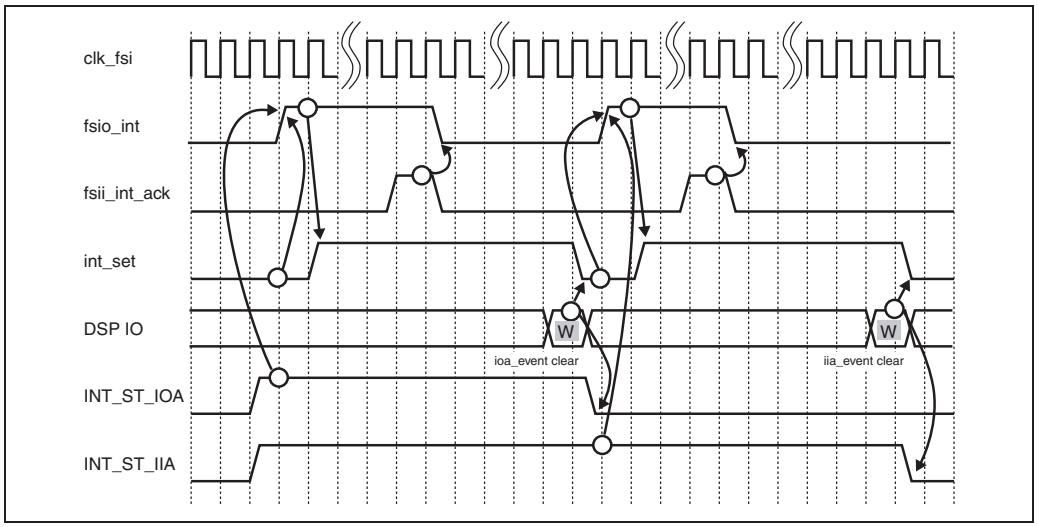


Figure 51.10 Timing Chart of Interrupt Signal

If all masks for interrupt sources and signals are cleared, the interrupt status registers (INT_ST.IOA, INT_ST.IIA) function as the interrupt request signals (int_ioa, int_iia).

SPU2 clears the source (int_st_ioa) at the end of interrupt handling. By this clearing, the interrupt control signal (int_set) is B'0 and is asserted again when another source occurs.

51.5 MUTE Specifications

The FSI2 has normal MUTE and zero cross MUTE functions for input/output operations. The MUTE circuits are implemented for output FIFOs and input FIFOs.

(1) Normal MUTE

The normal MUTE mutes on a per sample data basis. It is turned on (outputs 0) for channel 1 first 2 samples after it is enabled. Similarly, it is turned off for channel 1 first 2 samples after it is disabled.

Figure 51.11 shows the 2-channel audio output and the MUTE signal.

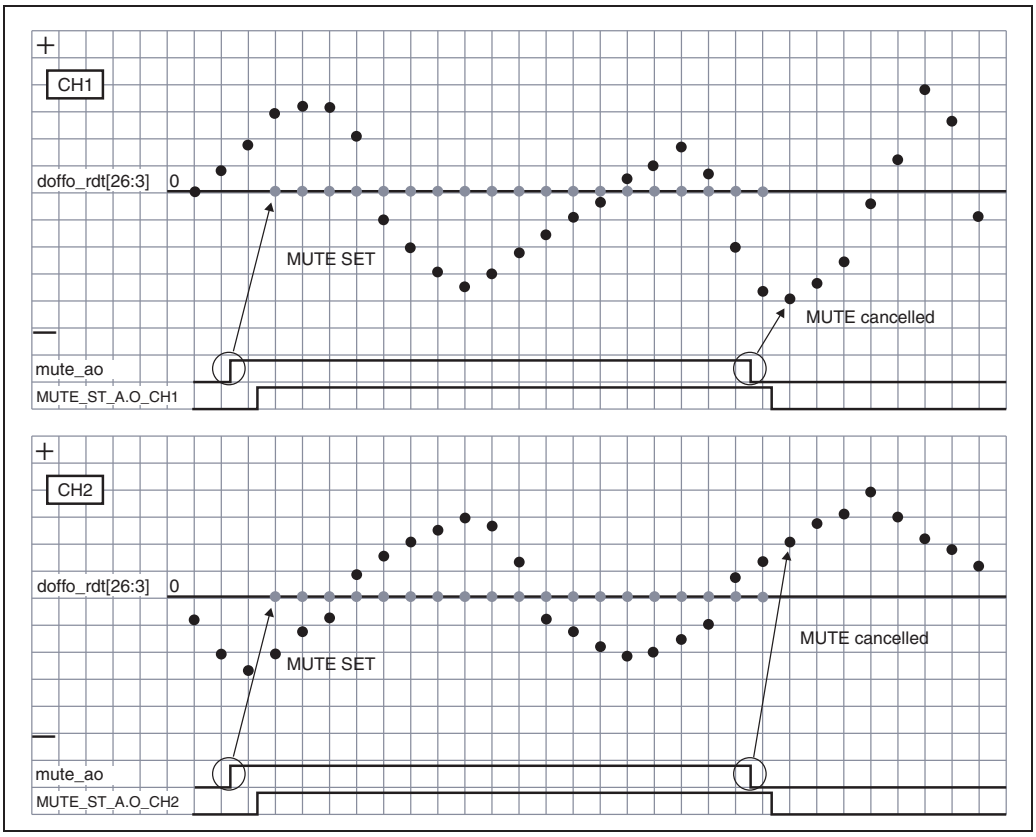


Figure 51.11 Normal MUTE Specification (Output Operation)

When the MUTE signal is asserted in input operation, the conversion module (input I2S) takes data written to input FIFOs and writes 0 to the on-chip RAM.

(2) Zero Cross MUTE

If the zero cross MUTE function is enabled, it compares current data to the previous one on each channel independently.

The conditions for turning on the mute are (1) the previous data is 0, (2) current data is 0, and (3) the sign of current data does not match the one of the previous data.

If any of these conditions ((1) to (3)) is satisfied, the mute is turned on (0 is output) until the zero cross MUTE function is disabled.

The mute (outputting 0) is turned off, just like it is turned on, if any of the conditions ((1) to (3)) is satisfied when current data is compared to the previous one on each channel independently.

Figure 51.12 shows the 2-channel audio output and zero cross MUTE signal.

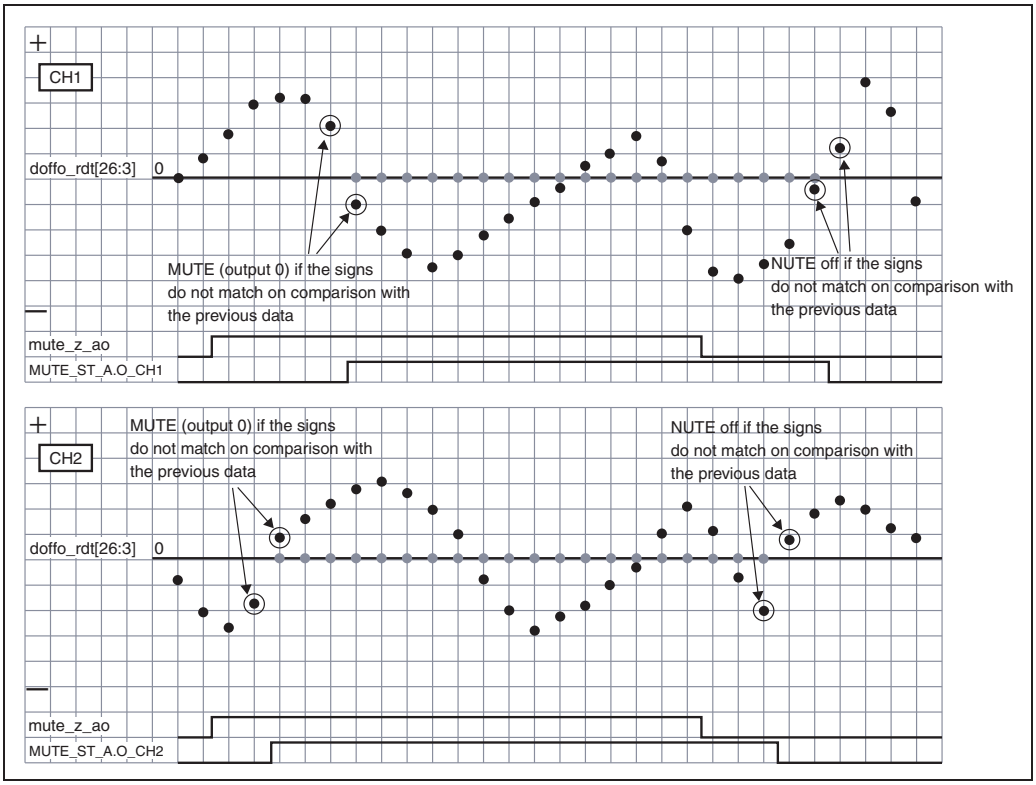


Figure 51.12 Zero Cross MUTE Specification (Output Operation)

Even if the zero cross MUTE function is enabled, the mute (outputting 0) is not turned on unless any of the conditions (1) to (3) is met.

Even if any of the conditions (1) to (3) is met, the mute (outputting 0) is not turned off unless the zero cross MUTE function is disabled.

After the zero cross MUTE function is enabled, it can be switched to the normal MUTE function to turn on/off the mute forcibly.

When the MUTE signal is asserted in input operation, the conversion module (input I2S) compares data written to input FIFOs to determine if the conditions (1) to (3) are met and writes 0 to the on-chip RAM.

51.6 FIFO Overflow/Underflow Specifications

When an underflow or overflow error occurs, the FIFO contains the error related information in a register. This section describes underflows and overflows in the output FIFOs and input FIFOs.

An output FIFO underflow occurs when the output I2S requests data (req) while the FIFO is empty. When it occurs, the output FIFO outputs H'00 0000 and the channel number [2:0]. An overflow occurs when the DSP tries to write more data than the FIFO capacity. Such write operations are ignored. No overflow occurs under management by the DSP.

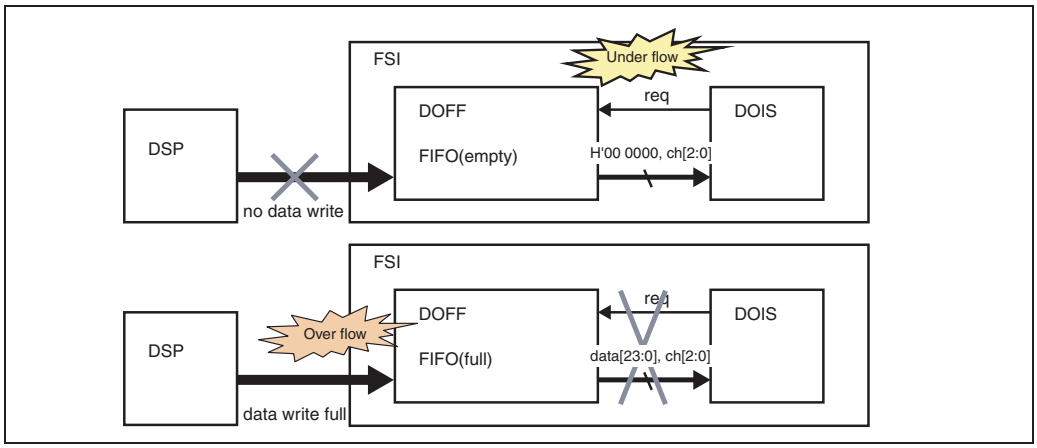


Figure 51.13 Output FIFO Underflow/Overflow

An input FIFO overflow occurs if 3-line serial data is input to the FIFO externally when it is full. The write to the input FIFO that caused an overflow is ignored. An underflow occurs when a read request is issued by the DSP while the input FIFO is empty. When it occurs, the read request returns 0. No underflow occurs under management by the DSP.

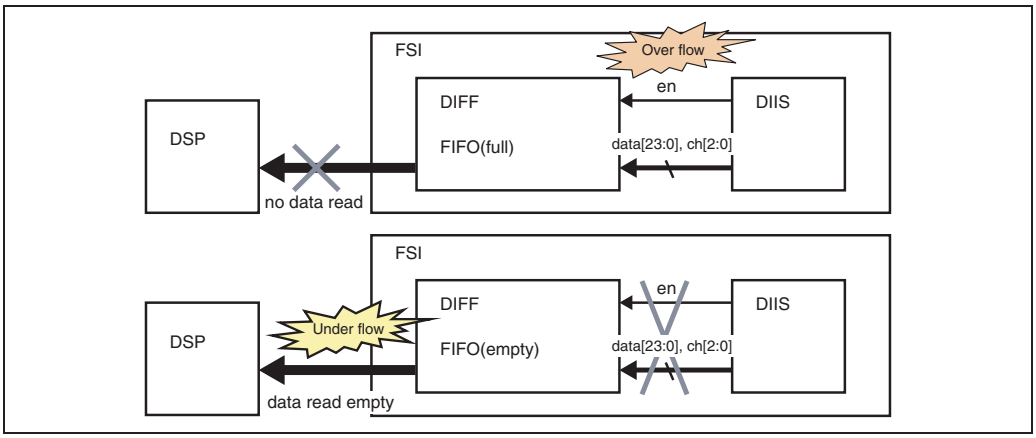


Figure 51.14 Input FIFO Overflow/Underflow

51.7 FIFO Clear

The FSI2 has a FIFO clear function for input and output separately. This function does the following:

(1) Clearing the UF/OF error history

Clears the FIFO status to 0.

(2) Clearing the address pointer of the FIFO control

Initializes the counter that controls the on-chip RAM access. When a FIFO clear is performed, the address pointer returns to the start address and data prior to the clear is overwritten.

(3) Clearing data prefetched by the BUFC block and the buffer pointer

Clears data prefetched by the BUFC block for continuous reads and the buffer pointer.

(4) Masking the FIFO control block

Can be enabled for the request (CH0) corresponding to the second sample after a FIFO clear. This is because the state of the mask is determined by the request (output) and enable (input) after the format and clock settings is fixed.

51.8 Serial Data Formats

All formats for 3-line serial data are shown below. The internal modules (DOIS, DIIS) operate based on the falling edge of the LR clock (CH0) that is inverted on the rising edge of the bit clock. Although the master clock is generated according to the specification in master operation, the inversion register needs to be set properly if the external LR and bit clocks are input directly in slave operation. Along with serial data formats, the inversion settings for slave operation are shown below for reference.

The MONO and MONO_Delay serial data formats are shown below.

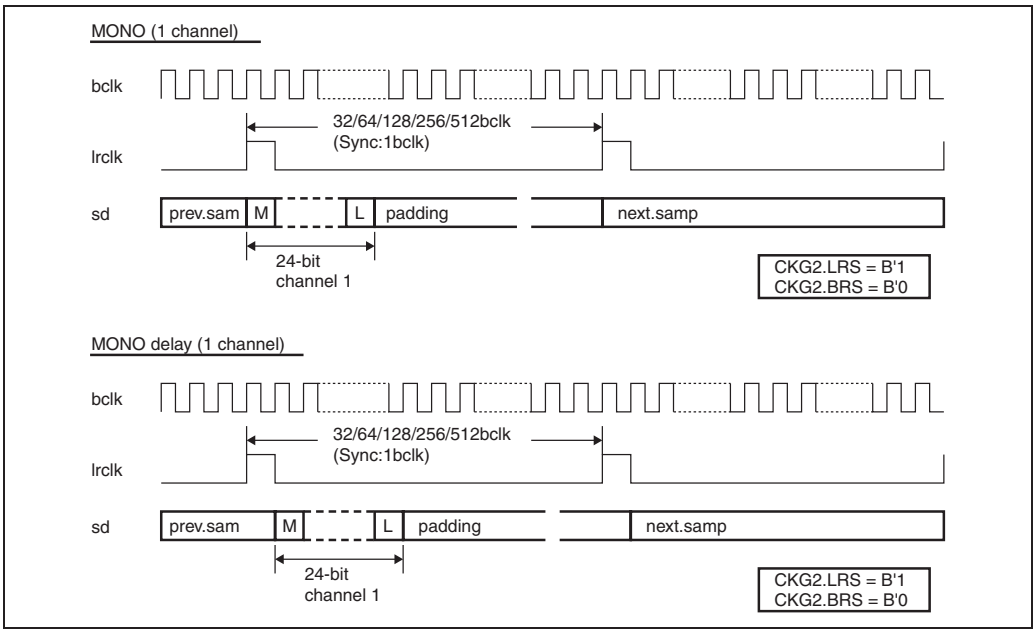


Figure 51.15 MONO and MONO_Delay Formats

The PCM and I2S serial data formats are shown below.

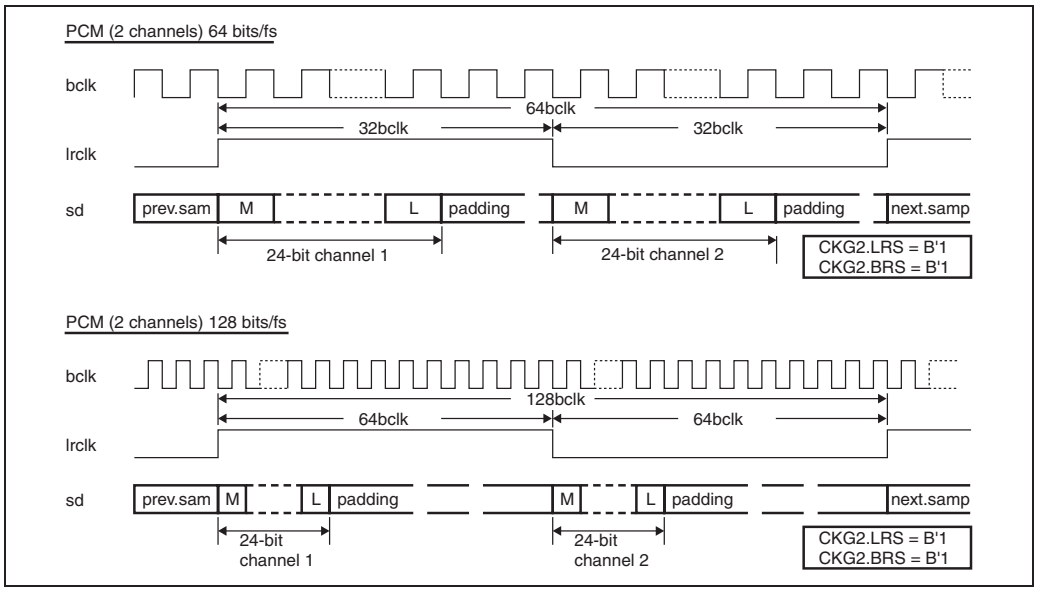


Figure 51.16 PCM Formats

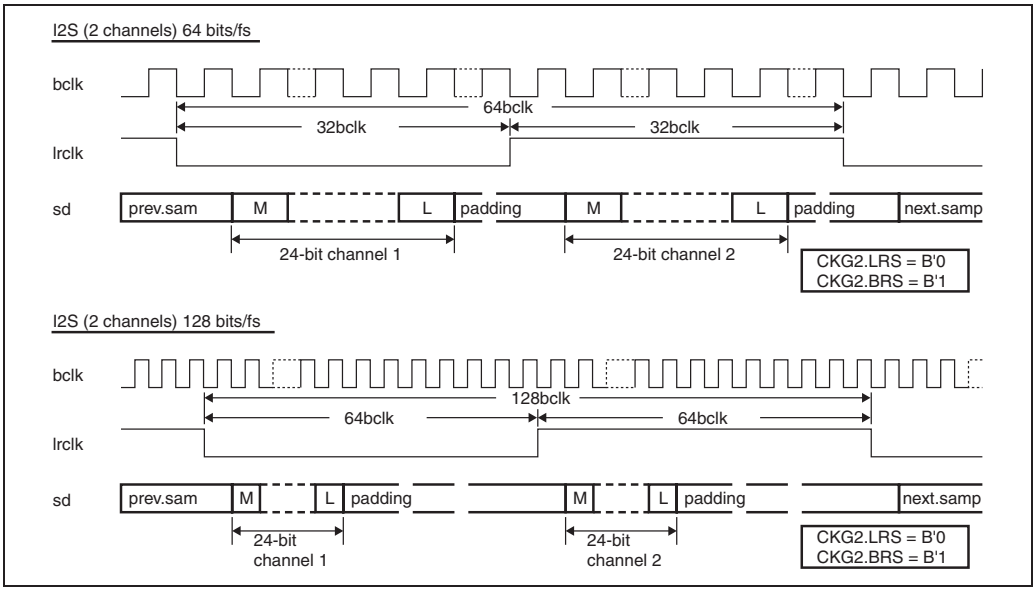


Figure 51.17 I2S Formats

The TDM and TDM_Delay serial data formats are shown below.

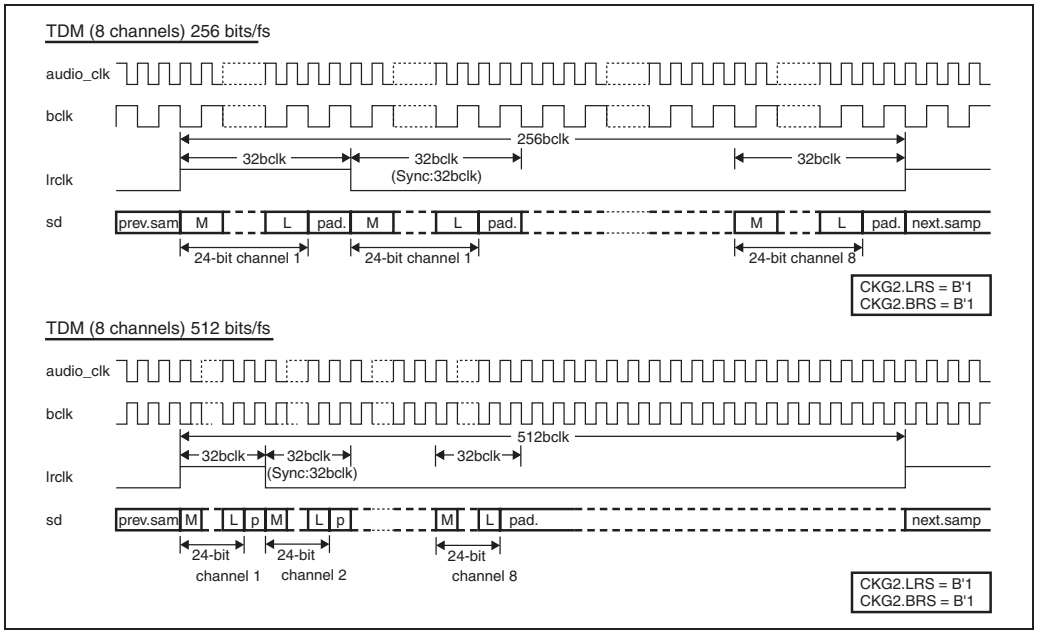


Figure 51.18 TDM Formats

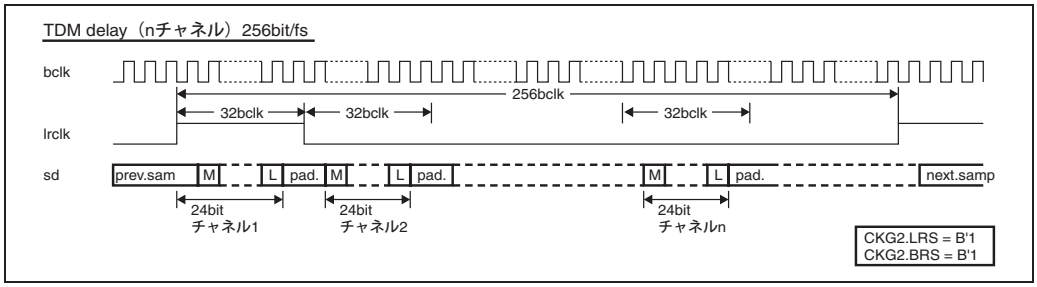


Figure 51.19 TDM Delay Formats

51.9 Operation Flows

51.9.1 Procedure for Starting the FSI2

A flow chart for starting the FSI2 for serial port A is shown in figure 51.20. This flow chart is applicable for serial port B.

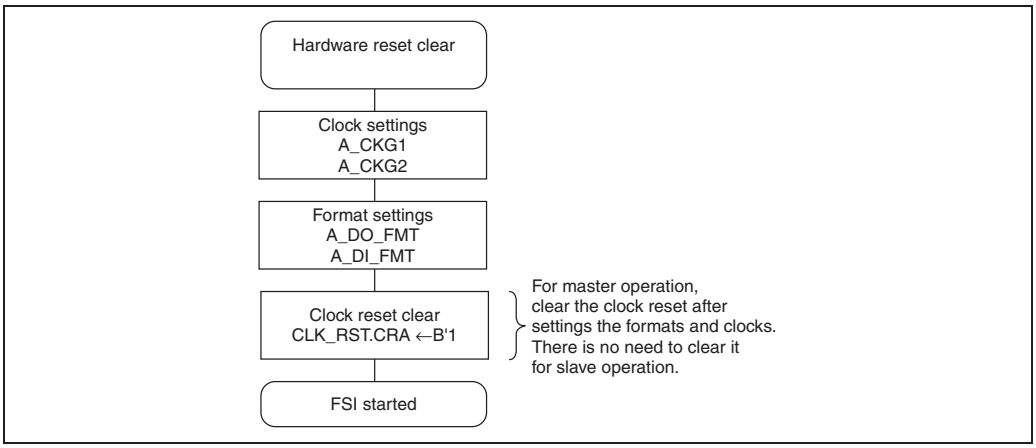


Figure 51.20 Flow for Starting FSI2 (Port A)

Use the steps above to start the FSI2. The configured bit and LR clocks are input to the conversion block (DOIS and DIIS modules), and data requests generated and data writes are started in the FIFO control block (DOFF and DIFF modules).

51.9.2 Procedure for Restarting the FSI2

A flow chart for restarting the FSI2 for serial port A is shown below. This flow chart is applicable for serial port B. To reconfigure transfer format and clock setting, follow the steps in this flow.

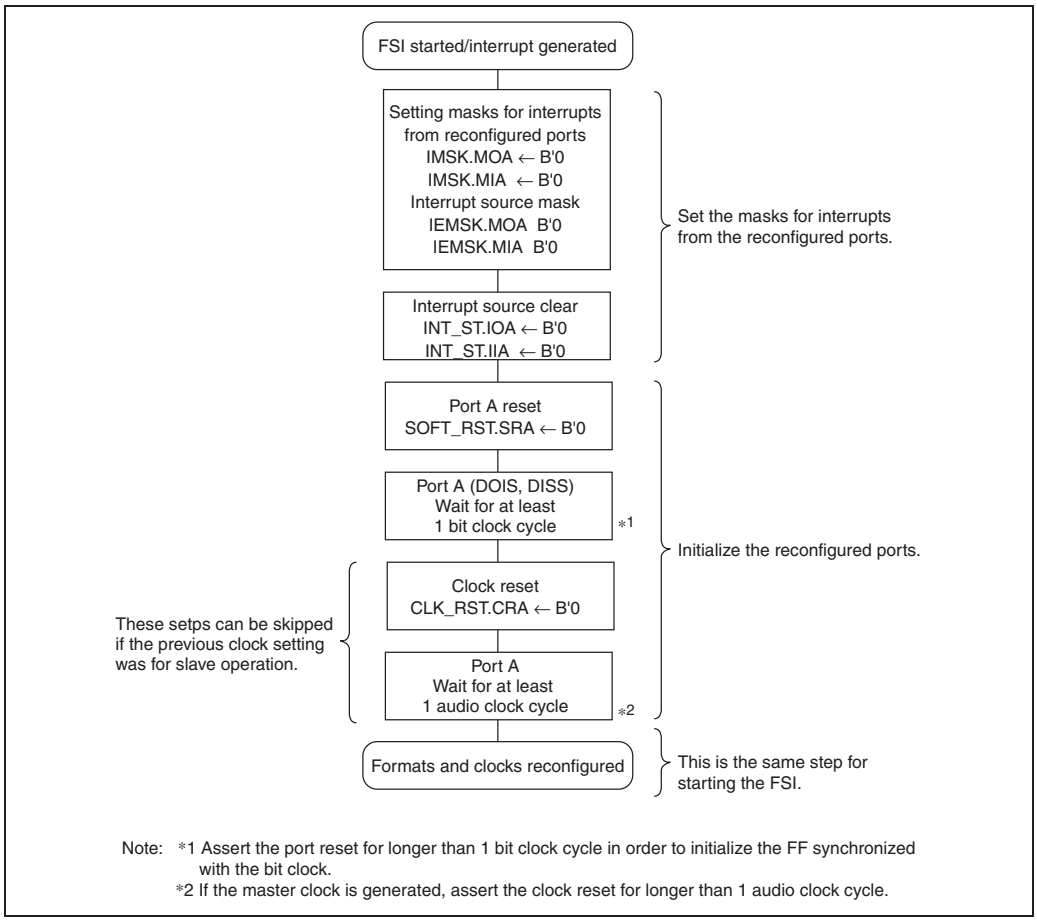


Figure 51.21 Flow for Restarting FSI2 (Port A)

Perform a port reset to initialize the port after setting the masks for the reconfigured port.

After initializing the port, return to the steps in section 51.9.1, Procedure for Starting the FSI2 to reconfigure the format and clock settings.

51.9.3 Procedure for Configuring Initial Interrupt Setting

A flow for configuring the initial interrupt setting after the FSI2 is started is shown in figure 51.22.

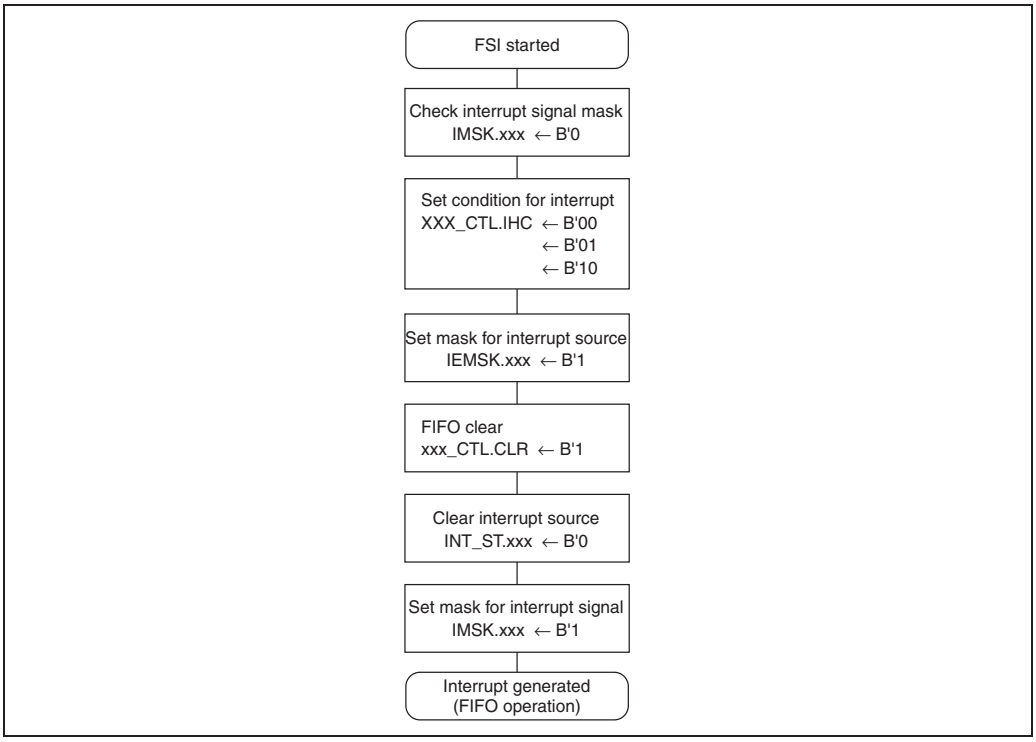


Figure 51.22ow for Configuring Initial Interrupt Setting

Interrupt settings can be configured for ports A/B and input/output (4 modes) independently. "xxx" in the figure indicates any signal to be transferred.

After checking if the mask for the signal to be transferred is set, select the interrupt condition and set the interrupt source mask, then perform a FIFO clear. Clear the interrupt source that may be generated and retained before the FIFO clear, clear the signal mask.

An interrupt signal occurs based on the FIFO capacity after a FIFO clear. Use this flow to configure interrupts if audio data are used for input and output operation initially.

51.9.4 Example of DSP Operation Flow

Figure 51.23 shows an example of the operation flow that the DSP follows to transfer audio data continuously after it accepts an interrupt.

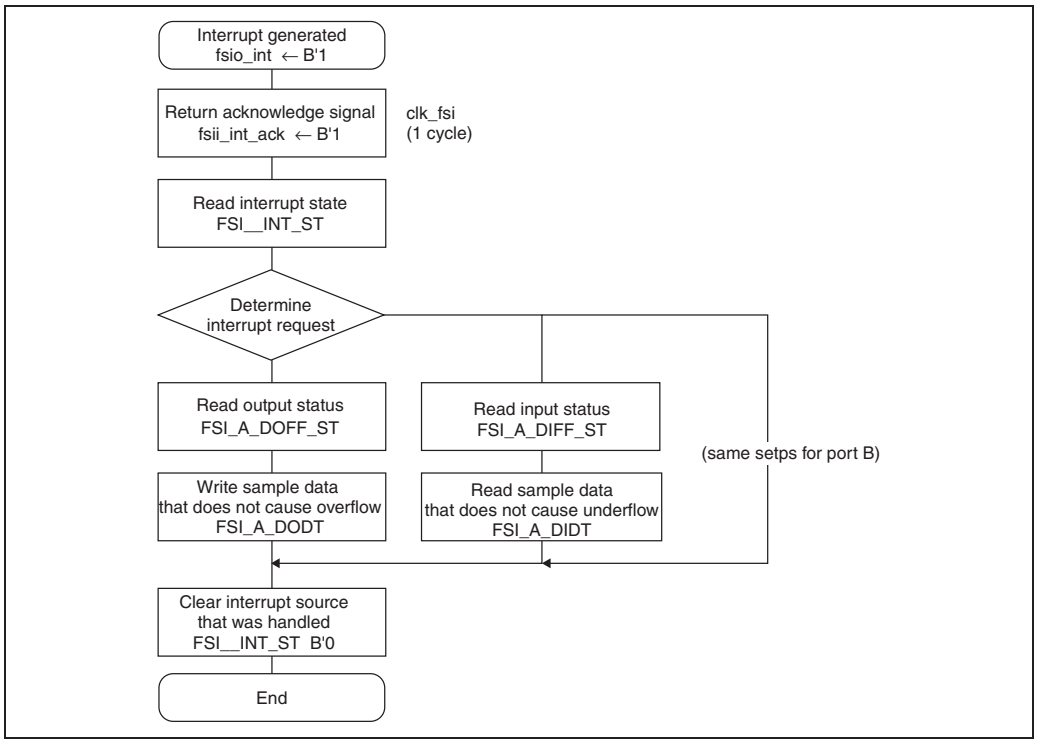


Figure 51.23ample of DSP Operation Flow

The DSP that accepts the interrupt signal returns an acknowledge signal for one cycle to the FSI2. Then, it reads the interrupt state to determine which FIFO caused the interrupt and handles the interrupt adequately. When it is handled, the DSP clears the interrupt source and exits the flow. Clearing the interrupt source allows the FSI2 to assert a new interrupt signal.

51.10 Restrictions

Table 51.8 shows the restrictions that apply to the use of the FSI2.

Table 51.8 Usage Restrictions

	Restrictions	
No.	**Item**	**Description**
1	Clock setting for master operation	In TDM and TDM Delay modes, the LR clock cannot be generated from 64 fs and 128 fs of audio clock, so they should not be set.
2		The bit clock setting (BPFMD register) is restricted by the input audio clock and format (any bit clock faster than the audio clock cannot be generated).
3	Timing for generating interrupt signal	An interrupt signal is generated 2 cycles (clk_fsi) after the FIFO status matches the interrupt source condition (match event) while all masks are cleared.
4	Worst case overflow/underflow	In the worst case such as system clock: 4MHz, fs: 96kHz (bit_clk = 50MHz), TDM (8 channels), overflow and underflow errors occur about 10 system clock cycles after the output interrupt (FIFO empty) and input interrupt (FIFO full) signals are generated. To enable continuous operation in such a worst case, select the half of the FIFO capacity as the level for generating interrupt. Additionally, the system clock should be nearly equal to the bit clock for stable continuous operation. In this case, the number of cycles from the FIFO full state to generating an overflow is extended from 10 cycles to about 100 cycles by using the system clock that is ten times faster (40MHz) and to about 700 cycles by selecting the half of the FIFO capacity as the level for generating interrupt. Consequently, it takes about 70000 cycles (product of the two cycle counts) until an overflow occurs by doing the both.
5	FIFO status read	Since the FIFO status is read with 1 wait, the result indicates the status that is 1 cycle (clk_fsi) old.
6	Simultaneous input and output operations	Simultaneous operation such as master-master or slave-slave operation is not allowed on the same serial port with different formats and LR/bit clocks (one serial port has only one I/O system)
7	Port reset	When performing an internal reset of the DOIS and DIIS modules due to the change in formats or clocks, the reset should be asserted longer than the input bit clock.
8	Clock reset	Since the counter for generating the master clock is synchronized with the audio clock, a reset should be asserted longer than the audio clock to reset the counter for reconfiguration.

51.11 FMSI (FIFO-incorporating Melody and Serial Interface)

The FMSI is an audio interface that incorporates a FIFO controller sporting both serial and parallel interfaces. A parallel port has been added as an expansion circuit for the FSI module. As well as incorporating existing FSI functionality, interrupt functionality has been strengthened, and 16-bit transmission formats are handled.

This module acts as a peripheral circuit of the SPU2 (Sound Processing Unit 2) audio processing circuit.

51.11.1 Characteristics of the FMSI Module

Characteristics and functions of the FMSI are described in table 51.9.

Table 51.9 List of FMSI Characteristics and Functions

Classification	Item	Details
Operating frequencies	Sampling frequency (f_S)	8 kHz to 96 kHz (max.)
	Audio clock	Clock signal (at 32 f_S, 64 f_S, 128 f_S, 256 f_S, or 512 f_S) used to generate the LR clock and bit clock
		256 kHz to 49.15 MHz (32 × 8 kHz to 512 × 96 kHz)
	IO bus clock	Operating frequency of the FMSI (100 MHz, max.)
	Sync. clock for the parallel interface	Operating frequency of the HPB (100 MHz, max.)
DSP/IO	Width of the IO bus	24 bits
Clock control	Control of the audio clock input to the interface section	Master operation (operation is to generate the LR and bit clocks from the audio clock)
		Slave operation (operation is to generate the LR and bit clocks from an external audio clock)
Output interface	Three-line serial output	Data width: 16 or 24 bits
		Formats Monaural (1 channel): Mono or mono with delay Stereo (2 channels): PCM or I2S Multi-channel (1 to 8 channels): TDM or TDM with delay
	Parallel output (MSU)	Data width: 16 bits
		Number of channels: 1

Classification	Item	Details
Input interface	Three-line serial input	Handles data in the same formats as the three-line serial output.
	Parallel input (SCUV)	Data width: 16 or 24 bits Number of channels: 2
FIFO	Capacity	Connected to external DP-RAM 24 bits × 256 words
	FIFO state information	Indicates the FIFO state (sampling data, underflow, or overflow)
	FIFO clearing	Initializes the FIFO state
	Interrupt source condition select	Controlled by the number of samples Output operation: Space equivalent to more than xxx samples is empty. Input operation: Data is equivalent to xxx or more samples.
Timer	Timer control	Interrupt generation is based on the counting of sampling periods.
Interrupts	Interrupt control	Single output for interrupt signals from all sources Control of source masking and signal masking
Direct transfer	Control of direct transfer	Continuous operation by DSP IO without reading and writing of registers 1. Parallel input (SCUV) to serial output 2. Serial input to parallel output (MSU) Note: This is with equal sampling frequencies.
Muting	Mute mode	Normal muting and muting at zero crossing

51.12 FMSI Block Diagram

Figure 51.24 shows a block diagram of the FMSI.

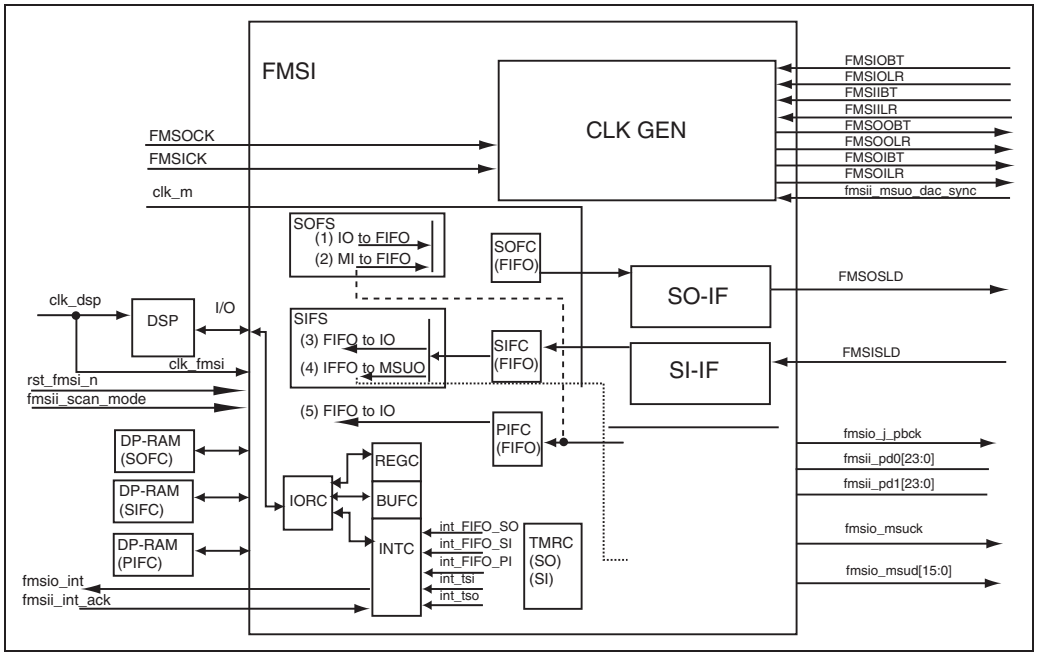


Figure 51.24 FMSI Block Diagram

The following provides an overview of modules comprising the FMSI.

51.12.1 CLK GEN (Clock Generation)

The CLK GEN generates the audio clock (for the LR clock and bit clock) used for the interface block (SO-IF, SI-IF, MI-IF, and MSUO-IF). The CLK GEN includes the following two systems for serial output (parallel input) and serial input (parallel output).

- SO system: For SO-IF (operating clock: clk_fmsi, FMSOCK or FMSIOBT)
- SI system: For SI-IF (operating clock: clk_fmsi, FMSICK or FMSIIBT)

51.12.2 SO-IF (Serial Output Interface)

The SO-IF issues a read request to the FIFO (SOFC) and performs serial conversion of read data with the operating clocks, clk_fmsi and ckgo_sdo_bck. A read request synchronized with clk_fmsi and serial conversion synchronized with ckgo_sdo_bck are performed asynchronously by switching the clocks.

51.12.3 SI-IF (Serial Input Interface)

The SI-IF performs parallel conversion of serial data and writes data to the FIFO (SIFC) with the operating clocks, clk_fmsi and ckgo_sdi_bck. Parallel conversion synchronized with ckgo_sdi_bck and data write synchronized with clk_fmsi are performed asynchronously by switching the clocks.

51.12.4 SOFC (Serial Output FIFO Control)

The SOFC is a serial output FIFO controller that controls accesses to a DP-RAM connected externally. The SOFC monitors the DP-RAM usage size (number of samples) and error history. A MUTE circuit is included. The operating clock is clk_fmsi.

51.12.5 SOFS (Serial Output FIFO Select)

The SOFS selects the DSP-IO bus or direct transfer MI-IF via which serial output data is to be written. The operating clock is clk_fmsi.

51.12.6 SIFC (Serial Input FIFO Control)

The SIFC is a serial input FIFO controller that controls accesses to a DP-RAM connected externally. The SIFC monitors the DP-RAM usage size (number of samples) and error history. A MUTE circuit is included. The operating clock is clk_fmsi.

51.12.7 SIFS (Serial Input FIFO Select)

The SOFS selects the DSP-IO bus or direct transfer MSUO-IF for serial input data. The operating clock is clk_fmsi.

51.12.8 PIFC (Parallel Input FIFO Control)

The PIFC is a parallel input FIFO controller that controls accesses to a DP-RAM connected externally. The PIFC monitors the DP-RAM usage size (number of samples) and error history. A MUTE circuit is included. The operating clock clk_fmsi.

51.12.9 TMRC (Timer Control)

The TMRC counts the sampling frequency cycles for the SO (MI) and SI (MSUO) systems. If the counter value exceeds the value specified by the register, an interrupt source is generated.

51.12.10 INTC (Interrupt Control)

This module controls interrupt signals. Interrupt sources generated internally are collected into one interrupt signal to be output externally. Interrupt sources can be masked individually.

51.12.11 BUFC (Buffer Control)

The BUFC block controls data reads/writes between the DSP and FIFOs. To read input data continuously, data are prefetched from FIFOs. Data are output with 4 waits on the initial read, but the following reads can be performed continuously with one wait by controlling the buffer pointer and reading data stored in buffers.

51.12.12 REGC (Register Control)

This module manages registers that are not used by INTC and BUFC. It is used to manage format, clock, and MUTE settings.

51.12.13 IORC (Input Output Register Control)

This module selects read data of INTC, BUFC, and REGC.

51.13 Input/Output Pins

Table 51.10 shows the FMSI pin configuration.

Table 51.10 FMSI Pin Configuration

Pin Name	I/O	Function
FMSOCK	Input	Audio clock input pin for SO-IF and MI-IF
FMSICK	Input	Audio clock input pin for SI-IF
FMSOOLR	Output	Output LR clock pin (master)
FMSOOBT	Output	Output bit clock pin (master)
FMSOILR	Output	Input LR clock pin (master)
FMSOIBT	Output	Input bit clock pin (master)
FMSIOLR	Input	Output LR clock pin (slave)
FMSIOBT	Input	Output bit clock pin (slave)
FMSIILR	Input	Input LR clock pin (slave)
FMSIIBT	Input	Input bit clock pin (slave)
FMSOSLD	Output	Output serial data pin
FMSISLD	Input	Input serial data pin

51.14 Register Descriptions

Figure 51.25 shows a schematic of FMSI address mapping. Table 51.11 shows the FMSI register configuration. The FMSI is mapped in the SPU2 (DSP1-IO) peripheral module area, which can be accessed by the CPU and DSP.

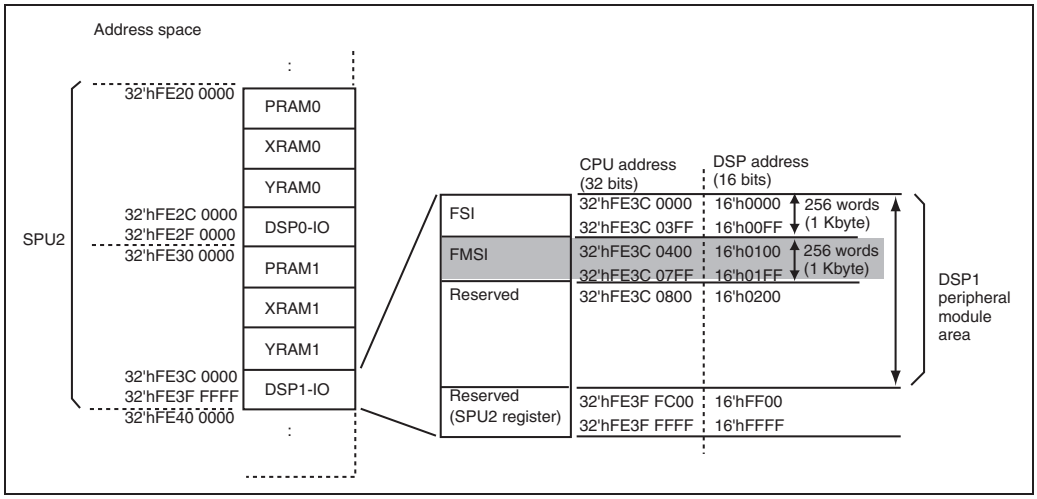


Figure 51.25 FMSI Address Space

The FMSI has 256 words (1 Kbyte) of address space.

Table 51.11 FMSI Register Configuration

Register Name	Abbrev.	R/W	Physical Address	DSP Address	Access Size		Dynamic/ Static
					CPU	DSP	
Serial output format register	S_DO_FMT	R/W	H'FE3C 0400	H'0100	32	24	S
Serial output FIFO control register	S_DOFF_CTL	R/W	H'FE3C 0404	H'0101	32	24	S/D*
Serial output FIFO status register	S_DOFF_ST	R/W	H'FE3C 0408	H'0102	32	24	D
Serial input format register	S_DI_FMT	R/W	H'FE3C 040C	H'0103	32	24	S
Serial input FIFO control register	S_DIFF_CTL	R/W	H'FE3C 0410	H'0104	32	24	S/D*
Serial input FIFO status register	S_DIFF_ST	R/W	H'FE3C 0414	H'0105	32	24	D
Serial input FIFO read register	S_DIDT	R	H'FE3C 0420	H'0108	32	24	D
Serial output FIFO write register	S_DODT	W	H'FE3C 0424	H'0109	32	24	D
Serial MUTE state register	S_MUTE_ST	R	H'FE3C 0428	H'010A	32	24	D
Parallel input format register	P_DI_FMT	R/W	H'FE3C 044C	H'0113	32	24	S
Parallel input FIFO control register	P_DIFF_CTL	R/W	H'FE3C 0450	H'0114	32	24	S/D*
Parallel input FIFO status register	P_DIFF_ST	R/W	H'FE3C 0454	H'0115	32	24	D
Parallel input FIFO read register	P_DIDT	R	H'FE3C 0460	H'0118	32	24	D
Parallel MUTE state register	P_MUTE_ST	R	H'FE3C 0468	H'011A	32	24	D
SO-IF and MI-IF operating clock set register	SOMI_CKG_ MD	R/W	H'FE3C 05C0	H'0170	32	24	S

Register Name	Abbrev.	R/W	Physical Address	DSP Address	Access Size		Dynamic/ Static
					CPU	DSP	
SO-IF and MI-IF operating clock invert register	SOMI_CKG_RV	R/W	H'FE3C 05C4	H'0171	32	24	S
SI-IF and MSUO-IF operating clock set register	SIMO_CKG_MD	R/W	H'FE3C 05C8	H'0172	32	24	S
SI-IF and MSUO-IF operating clock invert register	SIMO_CKG_RV	R/W	H'FE3C 05CC	H'0173	32	24	S
Clock system set register	CKG_SMD	R/W	H'FE3C 05D0	H'0174	32	24	S
Timer count set register	TMR_CTL	R/W	H'FE3C 05D8	H'0176	32	24	D
Timer count clear register	TMR_CLR	R/W	H'FE3C 05DC	H'0177	32	24	D
Direct serial transfer set register	DRCT_SRL	R/W	H'FE3C 05E0	H'0178	32	24	S
Interrupt state register	INT_ST	R/W	H'FE3C 0600	H'0180	32	24	D
Interrupt source mask register	IEMSK	R/W	H'FE3C 0605	H'0181	32	24	D
Interrupt signal mask register	IMSK	R/W	H'FE3C 0608	H'0182	32	24	D
MUTE set register	MUTE	R/W	H'FE3C 060C	H'0183	32	24	D
Clock reset register	CLK_RST	R/W	H'FE3C 0610	H'0184	32	24	S
Software reset register	SOFT_RST	R/W	H'FE3C 0614	H'0185	32	24	S
FIFO size register	FIFO_SZ	R	H'FE3C 0618	H'0186	32	24	S

Note: The (FIFO) CLR bit (bit 0) is a static bit; however, all the other bits in the register, that is, interrupt monitoring condition setting bits can be modified dynamically.

There are two types of registers, dynamic and static. Static registers should not be modified when the FSI is in operation (during continuous operation).

The CPU can write/read data to/from the lower bits (23 to 0) in registers. The upper bits are read as 0 and cannot be modified.

For setting the FMSI operation, also see a description of the register for selecting the FSI/FMSI interrupt acknowledge destination in section 51.3.43.

51.14.1 Serial Output Format Register (S_DO_FMT)

S_DO_FMT is a 24-bit readable/writable register that sets the bus width and selects the format to be used from MONO, MONO_Delay, PCM, I2S, TDM, and TDM_Delay.

When TDM and TDM_Delay modes are selected, this register specifies the number of channels (1 to 8 channels).

Bit:	23	22	21	20	19	18	17	16
	—	—	—	BWS	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	FMT[2:0]			—	NCH[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
23 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	BWS	0	R/W	Bus Width Select Selects the bus width for serial transfer. 0: 24 bits 1: 16 bits
19 to 7	—	All 0	R	Reserved
6 to 4	FMT	011	R/W	Format Selects the serial output format. 000: MONO (1 channel) 001: MONO Delay (1 channel) 010: PCM (2 channels) 011: I2S (2 channels) 100: TDM (1 to 8 channels) 101: TDM Delay (1 to 8 channels) 110: Setting prohibited 111: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Description
3	—	0	R	Reserved
2 to 0	NCH	000	R/W	Number of Channels Specifies the number of channels in TDM and TDM_Delay modes. 000: 1 channel 001: 2 channels 010: 3 channels 011: 4 channels 100: 5 channels 101: 6 channels 110: 7 channels 111: 8 channels When selecting the modes other than TDM and TDM_Delay, specify 000.

51.14.2 Serial Output FIFO Control Register (S_DOFF_CTL)

S_DOFF_CTL is a 24-bit readable/writable register that specifies the conditions for generating interrupt sources and initializes the FIFO (SOFC). Interrupt control can be selected from rough control that is conventionally used for FSI-IP and control using the number of samples.

Bit:	23	22	21	20	19	18	17	16
	—	—	IHC[1:0]		—	—	—	ISC[8]
Initial value:	0	0	0	1	0	0	0	0
R/W:	R	R	R/W	R/W	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ISC[7:0]								—	—	—	IMS	—	—	—	CLR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R	R	R	R/(W)*

Bit	Bit Name	Initial Value	R/W	Description
23, 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
21, 20	IHC	01	R/W	Interrupt Happening Condition Selects an interrupt source generation condition (rough control). 00: Empty state 01: More than half of the FIFO is free. 10: Has storage capacity for one or more samples. 11: Setting prohibited (Full state) (Data storage amount when more than half of the FIFO is free) 1 channel: 127 samples (127 words) or less 2 channels: 63 samples (126 words) or less 3 or 4 channels: 31 samples (3 channels: 93 words, 4 channels: 124 words) or less 5 to 8 channels: 15 samples (5 channels: 75 words, 6 channels: 90 words, 7 channels: 105 words, 8 channels: 120 words) or less
19 to 17	—	All 0	R	Reserved

Bit	Bit Name	Initial Value	R/W	Description
16 to 8	ISC	h'000	R/W	Interrupt Sample Condition Specifies an interrupt source generation condition by the number of samples that can be stored in free areas (control by the number of samples). (Example: format: ch1) h'100: Empty state h'080: Has storage capacity for 80 or more samples. h'001: Has storage capacity for one or more samples. h'000: Setting prohibited (Full state) The set value must not exceed the upper limit for the number of channels. (Settable values) 1 channel: 0 to 256 samples (h'0 to h'100) 2 channels: 0 to 128 samples (h'0 to h'80) 3 or 4 channels: 0 to 64 samples (h'0 to h'40) 5 to 8 channels: 0 to 32 samples (h'0 to h'20)
7 to 5	—	All 0	R	Reserved
4	IMS	0	R/W	Interrupt Mode Select Selects interrupt control mode. 0: Rough control (IHC) 1: Control by the number of samples (ISC)
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0*	CLR	0	W	Clear Clears the FIFO. Initializes the access pointer and the error history. 0: When only the interrupt source generation condition is changed, the write value should be 0. 1: Clears the FIFO. This bit is always read as 0.

Note: If 1 is written to the CLR bit, the bit is asserted for one pulse and then cleared to 0.

51.14.3 Serial Output FIFO Status Register (S_DOFF_ST)

S_DOFF_ST is a 24-bit read-only register (the OF and UF bits can be written to). It can be used to read the serial output FIFO states, the number of stored sample data, and the history of overflow and underflow errors. For procedure for clearing the OF and UF bits, refer to section 51.18.2, Error Flag Clear.

Bit:	23	22	21	20	19	18	17	16
	—	—	ST[1:0]		—	—	—	SZ[8]
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SZ[7:0]								—	—	—	OF	—	—	—	UF
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/(W)*	R	R	R	R/(W)*

Bit	Bit Name	Initial Value	R/W	Description
23, 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
21, 20	ST	00	R	Status Indicates the FIFO status. 00: Empty state 01: Less than half of the FIFO is used. 10: Half or more of the FIFO is used. 11: Full state
19 to 17	—	All 0	R	Reserved

Bit	Bit Name	Initial Value	R/W	Description
16 to 8	SZ	h'000	R	Size Number of sample data Indicates the number of sample data stored in the FIFO. The maximum value depends on the number of channels selected for the format. The maximum number of sample data for each number of channels is shown below. If more samples than the maximum number of samples in the parentheses are written, an overflow occurs. 1 channel: 256 (256 × 1 = 256 words) 2 channels: 128 (128 × 2 = 256 words) 3 channels: 64 (64 × 3 = 192 words) 4 channels: 64 (64 × 4 = 256 words) 5 channels: 32 (32 × 5 = 160 words) 6 channels: 32 (32 × 6 = 192 words) 7 channels: 32 (32 × 7 = 224 words) 8 channels: 32 (32 × 8 = 256 words) FIFOs are used in 4-channel units in 3-channel mode and in 8-channel units in 5- to 7-channel mode, meaning that more FIFOs than the required size of DP-RAM are used. For the DSP, the maximum number of writes must be taken into account.
7 to 5	—	All 0	R	Reserved
4*	OF	0	R/W	Overflow Indicates the FIFO error history. 0: No error has occurred. 1: Overflow has occurred.
3 to 1	—	All 0	R	Reserved
0*	UF	0	R/W	Underflow Indicates the FIFO error history. 0: No error has occurred. 1: Underflow has occurred.

Note: The FIFO error history is cleared by writing 0 to this bit and retained by writing 1 to it.

51.14.4 Serial Input Format Register (S_DI_FMT)

S_DI_FMT is a 24-bit readable/writable register that sets the bus width and selects the format to be used from MONO, MONO_Delay, PCM, I2S, TDM, and TDM_Delay.

When TDM and TDM_Delay modes are selected, this register specifies the number of channels (1 to 8 channels).

Bit:	23	22	21	20	19	18	17	16
	—	—	—	BWS	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	FMT[2:0]			—	NCH[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
23 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	BMS	0	R/W	Bus Width Select Selects the bus width for serial transfer. 0: 24 bits 1: 16 bits
19 to 7	—	All 0	R	Reserved
6 to 4	FMT	011	R/W	Format Selects the serial input format. 000: MONO (1 channel) 001: MONO Delay (1 channel) 010: PCM (2 channels) 011: I2S (2 channels) 100: TDM (1 to 8 channels) 101: TDM Delay (1 to 8 channels) 110: Setting prohibited 111: Setting prohibited.

Bit	Bit Name	Initial Value	R/W	Description
3	—	0	R	Reserved
2 to 0	NCH	000	R/W	Number of Channels Specifies the number of channels in TDM and TDM_Delay modes. 000: 1 channel 001: 2 channels 010: 3 channels 011: 4 channels 100: 5 channels 101: 6 channels 110: 7 channels 111: 8 channels When selecting the modes other than TDM and TDM_Delay, specify 000.

51.14.5 Serial Input FIFO Control Register (S_DIFF_CTL)

S_DIFF_CTL is a 24-bit readable/writable register that specifies the conditions for generating interrupt sources and initializes the FIFO (SIFC). Interrupt control can be selected from rough control that is conventionally used for FSI-IP and control using the number of samples.

Bit:	23	22	21	20	19	18	17	16
	—	—	IHC[1:0]		—	—	—	ISC[8]
Initial value:	0	0	0	1	0	0	0	0
R/W:	R	R	R/W	R/W	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ISC[7:0]								—	—	—	IMS	—	—	—	CLR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R	R	R	R/(W)*

Bit	Bit Name	Initial Value	R/W	Description
23, 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
21, 20	IHC	01	R/W	Interrupt Happening Condition Interrupt source generation condition (rough control) 00: Full state 01: Amount of data in the FIFO equals or exceeds half the FIFO capacity. 10: One or more sample data is in the FIFO. 11: Setting prohibited (empty state) (Data storage amount when half or more of the FIFO space is free) 1 channel: 128 samples (128 words) or more 2 channels: 64 samples (128 words) or more 3 or 4 channels: 32 samples (3 channels: 96 words, 4 channels: 128 words) or more 5 to 8 channels: 16 samples (5 channels: 80 words, 6 channels: 96 words, 7 channels: 112 words, 8 channels: 128 words) or more
19 to 17	—	All 0	R	Reserved

Bit	Bit Name	Initial Value	R/W	Description
16 to 8	ISC	h'000	R/W	Interrupt Sample Condition Specifies an interrupt source generation condition by data size (control by the number of samples). h'xxx: xxx or more sample data are in the FIFO. h'001: One or more sample data is in the FIFO. h'000: No data (Empty state) The set value must not exceed the upper limit for the number of channels specified for the pertinent format. (Settable values) 1 channel: 0 to 256 samples (h'0 to h'100) 2 channels: 0 to 128 samples (h'0 to h'80) 3 or 4 channels: 0 to 64 samples (h'0 to h'40) 5 to 8 channels: 0 to 32 samples (h'0 to h'20)
7 to 5	—	0	R	Reserved
4	IMS	0	R/W	Interrupt Mode Select Selects interrupt control mode. 0: Rough control (IHC) 1: Control by the number of samples (ISC)
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0*	CLR	0	W	Clear Clears the FIFO. Initializes the access pointer and the error history. 0: When only the interrupt source generation condition is changed, the write value should be 0. 1: Clears the FIFO. This bit is always read as 0.

Note: If 1 is written to the CLR bit, the bit is asserted for one pulse and then cleared to 0.

51.14.6 Serial Input FIFO Status Register (S_DIFF_ST)

S_DIFF_ST is a 24-bit read-only register (the OF and UF bits can be written to). It can be used to read the serial input FIFO states, the number of stored sample data, and the history of overflow and underflow errors. For procedure for clearing the OF and UF bits, refer to section 51.18.2, Error Flag Clear.

Bit:	23	22	21	20	19	18	17	16
	—	—	ST[1:0]		—	—	—	SZ[8]
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SZ[7:0]								—	—	—	OF	—	—	—	UF
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/(W)*	R	R	R	R/(W)*

Bit	Bit Name	Initial Value	R/W	Description
23, 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
21, 20	ST	00	R	Status Indicates the FIFO status. 00: Empty state 01: Less than half of the FIFO is used. 10: Half or more of the FIFO is used. 11: Full state
19 to 17	—	All 0	R	Reserved

Bit	Bit Name	Initial Value	R/W	Description
16 to 8	SZ	h'000	R	Size Number of sample data Indicates the number of sample data stored in FIFOs. The maximum value depends on the number of channels selected for the format. The maximum number of sample data for each number of channels is shown below. If more samples than the maximum number of samples in the parentheses are read, an underflow occurs. 1 channel: 256 (256 × 1 = 256 words) 2 channels: 128 (128 × 2 = 256 words) 3 channels: 64 (64 × 3 = 192 words) 4 channels: 64 (64 × 4 = 256 words) 5 channels: 32 (32 × 5 = 160 words) 6 channels: 32 (32 × 6 = 192 words) 7 channels: 32 (32 × 7 = 224 words) 8 channels: 32 (32 × 8 = 256 words) FIFOs are used in 4-channel units in 3-channel mode and in 8-channel units in 5- to 7-channel mode, meaning that more FIFOs than the required size of DP-RAM are used. For the DSP, the maximum number of reads must be taken into account.
7 to 5	—	All 0	R	Reserved
4*	OF	0	R/W	Overflow Indicates the FIFO error history. 0: No error has occurred. 1: Overflow has occurred.
3 to 1	—	All 0	R	Reserved
0*	UF	0	R/W	Underflow Indicates the FIFO error history. 0: No error has occurred. 1: Underflow has occurred.

Note: The FIFO error history is cleared by writing 0 to this bit and retained by writing 1 to it.

51.14.7 Serial Input FIFO Read Register (S_DIDT)

S_DIDT is a 24-bit read-only register that can be used to read data stored in the serial input FIFO. If the FIFO is empty, a read causes an underflow error.

Bit:	23	22	21	20	19	18	17	16
	DIDT[23:16]							
Initial value:	0	0	0	0	0	0	0	0
R/W:	R*	R*	R*	R*	R*	R*	R*	R*

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DIDT[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R*	R*	R*	R*	R*	R*	R*	R*	R	R	R	R	R	R	R	R

* In 16-bit transfer mode, valid data is output to bits 23 to 8.

Bit	Bit Name	Initial Value	R/W	Description
23 to 0	DIDT	h'00 0000	R	Read-only register used to read data stored in the serial input FIFO.

51.14.8 Serial Output FIFO Write Register (S_DODT)

S_DODT is a 24-bit write-only register that can be used to write data to the serial output FIFO. If the FIFO is full, a write causes an overflow error.

Bit:	23	22	21	20	19	18	17	16
	DODT[23:16]							
Initial value:	0	0	0	0	0	0	0	0
R/W:	W*	W*	W*	W*	W*	W*	W*	W*

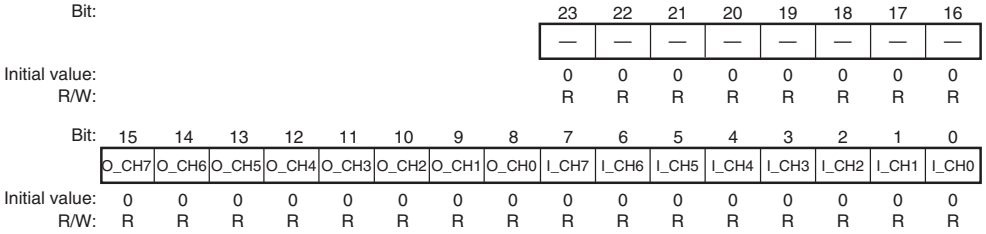
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DODT[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W*	W*	W*	W*	W*	W*	W*	W*	W	W	W	W	W	W	W	W

* In 16-bit transfer mode, write valid data in bits 23 to 8.

Bit	Bit Name	Initial Value	R/W	Description
23 to 0	DODT	h'00 0000	W	Write-only register used to write data to the serial output FIFO.

51.14.9 Serial MUTE State Register (S_MUTE_ST)

S_MUTE_ST is a 24-bit read-only register that indicates the MUTE state for each channel in serial I/O operation.



Bit:	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	O_CH7	O_CH6	O_CH5	O_CH4	O_CH3	O_CH2	O_CH1	O_CH0	I_CH7	I_CH6	I_CH5	I_CH4	I_CH3	I_CH2	I_CH1	I_CH0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
23 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	O_CH7	0	R	Serial Output MUTE State (Same name for bits 14 to 8) 0: Channel 8 MUTE off 1: Channel 8 MUTE on
14	O_CH6	0	R	0: Channel 7 MUTE off 1: Channel 7 MUTE on
13	O_CH5	0	R	0: Channel 6 MUTE off 1: Channel 6 MUTE on
12	O_CH4	0	R	0: Channel 5 MUTE off 1: Channel 5 MUTE on
11	O_CH3	0	R	0: Channel 4 MUTE off 1: Channel 4 MUTE on
10	O_CH2	0	R	0: Channel 3 MUTE off 1: Channel 3 MUTE on
9	O_CH1	0	R	0: Channel 2 MUTE off 1: Channel 2 MUTE on
8	O_CH0	0	R	0: Channel 1 MUTE off 1: Channel 1 MUTE on

Bit	Bit Name	Initial Value	R/W	Description
7	I_CH7	0	R	Serial Input MUTE State (Same name for bits 6 to 0) 0: Channel 8 MUTE off 1: Channel 8 MUTE on
6	I_CH6	0	R	0: Channel 7 MUTE off 1: Channel 7 MUTE on
5	I_CH5	0	R	0: Channel 6 MUTE off 1: Channel 6 MUTE on
4	I_CH4	0	R	0: Channel 5 MUTE off 1: Channel 5 MUTE on
3	I_CH3	0	R	0: Channel 4 MUTE off 1: Channel 4 MUTE on
2	I_CH2	0	R	0: Channel 3 MUTE off 1: Channel 3 MUTE on
1	I_CH1	0	R	0: Channel 2 MUTE off 1: Channel 2 MUTE on
0	I_CH0	0	R	0: Channel 1 MUTE off 1: Channel 1 MUTE on

51.14.10 Parallel Input Format Register (P_DI_FMT)

P_DI_FMT is a 24-bit readable/writable register that specifies the bus width and the number of channels for data transfer.

Bit:	23	22	21	20	19	18	17	16
	—	—	—	BWS	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	NCH
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
23 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	BWS	0	R/W	Bus Width Select Selects the bus width of the MI-IF module. 0: 24 bits 1: 16 bits (the lower 8 bits are invalid.)
19 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	NCH	1	R/W	Number of Channel Selects the number of channels of the MI-IF module. 0: 1 channel 1: 2 channels

51.14.11 Parallel Input FIFO Control Register (P_DIFF_CTL)

P_DIFF_CTL is a 24-bit readable/writable register that sets the condition for generating interrupt sources and initializes the FIFO (PIFC). Interrupt control can be selected from rough control that is conventionally used for FSI-IP and control using the number of samples.

Bit:	23	22	21	20	19	18	17	16
	—	—	IHC[1:0]		—	—	—	ISC[8]
Initial value:	0	0	0	1	0	0	0	0
R/W:	R	R	R/W	R/W	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ISC[7:0]								—	—	—	IMS	—	—	—	CLR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R	R	R	R/(W)*

Bit	Bit Name	Initial Value	R/W	Description
23, 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
21, 20	IHC	01	R/W	Interrupt Happening Condition Interrupt source generation condition (rough control) 00: Full state 01: Amount of data in the FIFO equals or exceeds half the FIFO capacity. 10: One or more sample data is in the FIFO. 11: Setting prohibited (empty state) (Data storage amount when half or more of the FIFO space is used) 1 channel: 128 samples (128 words) or more 2 channels: 64 samples (128 words) or more 3 or 4 channels: 32 samples (3 channels: 96 words, 4 channels: 128 words) or more 5 to 8 channels: 16 samples (5 channels: 80 words, 6 channels: 96 words, 7 channels: 112 words, 8 channels: 128 words) or more
19 to 17	—	All 0	R	Reserved

Bit	Bit Name	Initial Value	R/W	Description
16 to 8	ISC	h'000	R/W	Interrupt Sample Condition Interrupt source generation condition (control by the number of samples) Specifies the interrupt source generation condition by data size. h'xxx: xxx or more sample data are in the FIFO. h'001: One or more sample data is in the FIFO. h'000: No data (Empty state) The set value must not exceed the upper limit for the number of channels specified for the pertinent format. Settable values: 1 channel: 0 to 256 samples (h'0 to h'100) 2 channels: 0 to 128 samples (h'0 to h'80) 3 or 4 channels: 0 to 64 samples (h'0 to h'40) 5 to 8 channels: 0 to 32 samples (h'0 to h'20)
7 to 5	—	All 0	R	Reserved
4	IMS	0	R/W	Interrupt Mode Select Selects interrupt control. 0: Rough control (IHC) 1: Control by the number of samples (ISC)
3 to 1	—	All 0	R	Reserved
0*	CLR	0	W	Clear Clears the FIFO. Initializes the access pointer and the error history. 0: When only the interrupt source generation condition is changed, the write value should be 0. 1: Clears the FIFO. This bit is always read as 0.

Note: If 1 is written to the CLR bit, the bit is asserted for one pulse and then cleared to 0.

51.14.12 Parallel Input FIFO Status Register (P_DIFF_ST)

P_DIFF_ST is a 24-bit read-only register (the OF and UF bits can be written to). It can be used to read the parallel input FIFO states, the number of stored sample data, and the history of overflow and underflow errors. For procedure for clearing the OF and UF bits, refer to section 51.18.2, Error Flag Clear.

Bit:	23	22	21	20	19	18	17	16
	—	—	ST[1:0]		—	—	—	SZ[8]
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SZ[7:0]								—	—	—	OF	—	—	—	UF
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/(W)*	R	R	R	R/(W)*

Bit	Bit Name	Initial Value	R/W	Description
23, 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
21, 20	ST	00	R	Status Indicates the FIFO status. 00: Empty state 01: Less than half of the FIFO is used. 10: Half or more of the FIFO is used. 11: Full state
19 to 17	—	All 0	R	Reserved
16 to 8	SZ	h'000	R	Size Number of sample data Indicates the number of sample data stored in the FIFO. The maximum number of sample data 1 channel: 256 (256 × 1 = 256 words) 2 channels: 128 (128 × 2 = 256 words)
7 to 5	—	All 0	R	Reserved

Bit	Bit Name	Initial Value	R/W	Description
4*	OF	0	R/W	Overflow Indicates the FIFO error history. 0: No error has occurred. 1: Overflow has occurred.
3 to 1	—	All 0	R	Reserved
0*	UF	0	R/W	Underflow Indicates the FIFO error history. 0: No error has occurred. 1: Underflow has occurred.

Note: The FIFO error history is cleared by writing 0 to this bit and retained by writing 1 to it.

51.14.13 Parallel Input FIFO Read Register (P_DIDT)

P_DIDT is a 24-bit read-only register that can be used to read data stored in the parallel input FIFO. If the FIFO is empty, a read causes an underflow error.

Bit:	23	22	21	20	19	18	17	16
	DIDT[23:16]							
Initial value:	0	0	0	0	0	0	0	0
R/W:	R*	R*	R*	R*	R*	R*	R*	R*

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DIDT[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R*	R*	R*	R*	R*	R*	R*	R*	R	R	R	R	R	R	R	R

Note: * In 16-bit transfer mode, valid data is output to bits 23 to 8.

Bit	Bit Name	Initial Value	R/W	Description
23 to 0	DIDT	h'00 0000	R	Read-only register used to read data stored in the parallel input FIFO.

51.14.14 Parallel MUTE State Register (P_MUTE_ST)

P_MUTE_ST is a 24-bit read-only register that indicates the MUTE state for each channel in parallel input operation.

Bit:	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	I_CH1	I_CH0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

* In 16-bit transfer mode, write valid data in bits 23 to 8.

Bit	Bit Name	Initial Value	R/W	Description
23 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	I_CH1	0	R	Parallel Input MUTE State (Same name for bit 0) 0: Channel 2 MUTE off 1: Channel 2 MUTE on
0	I_CH0	0	R	0: Channel 1 MUTE off 1: Channel 1 MUTE on

51.14.15 SO-IF and MI-IF Operating Clock Set Register (SOMI_CKG_MD)

SOMI_CKG_MD is a 24-bit readable/writable register. It generates the master clock and selects audio clock used in the SO-IF and MI-IF modules.

Bit:	23	22	21	20	19	18	17	16
	—	—	—	MSUSYNCS	—	—	—	—
Initial value:	0	0	0	1	0	0	0	0
R/W:	R	R	R	R/(W)*2	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	ACKMD[2:0]			—	BPFMD[2:0]			—	—	—	DIPMD	—	—	—	DOSMD
Initial value:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
R/W:	R	R/(W)*1	R/(W)*1	R/(W)*1	R	R/(W)*1	R/(W)*1	R/(W)*1	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
23 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20*2	MSUSYNCS	1	R/W	MSU SYNC Select Selects the synchronization clock for generating the reference clock for the MI-IF module. 1: Generates the reference clock using serial LR clock. 0: Generates the reference clock using the MSU sync signal.
19 to 15	—	All 0	R	Reserved

Bit	Bit Name	Initial Value	R/W	Description
14 to 12*[1]	ACKMD	000	R/W	Audio Clock Mode Specifies the audio clock used for generating the master LR clock. Select the audio clock (fs) to be input in terms of a multiple of the sampling frequency (fs). 000: 512 fs 001: 256 fs 010: 128 fs 011: 64 fs 100: 32 fs Setting these bits is not necessary for slave operation.
11	—	0	R	Reserved
10 to 8*[1]	BPFMD	001	R/W	Bit/Fs Mode Sets the division ratio of the master bit clock. 111: 16 bit/fs 000: 32 bit/fs 001: 64 bit/fs 010: 128 bit/fs 011: 256 bit/fs 100: 512 bit/fs 101: Setting prohibited 110: Setting prohibited Setting these bits is not necessary for slave operation.
7 to 5	—	All 0	R	Reserved
4	DIPMD	0	R/W	Data Input Parallel Mode Selects master or slave operation for the MI-IF module. 0: Slave operation 1: Master operation
3 to 1	—	All 0	R	Reserved

Bit	Bit Name	Initial Value	R/W	Description
0	DOSMD	0	R/W	Data Output Serial Mode Selects master or slave operation for the SO-IF module. 0: Slave operation 1: Master operation

Notes: 1. Some values cannot be set depending on the format and transfer bus width. For the formats and the ACKMD and BPFMD bit settings, refer to section 51.19.
2. For the clock to the MI-IF module, the settings of the MSUSYNCS bit take precedence. (When MSUSYNCS is 1, the set value of DIPMD is ignored.)

51.14.16 SO-IF and MI-IF Operating Clock Invert Register (SOMI_CKG_RV)

SOMI_CKG_RV is a 24-bit readable/writable register that specifies whether to invert bit clocks and LR clocks. In master mode, set the bits according to the formats of the external ADC and the DAC. In slave operation, set the bits so that the external clock is input to the circuit at the falling edge of the LR clock and the rising edge of the bit clock. Figure 51.3 shows the relation among clock inversion, the master/slave selector, and the clock setting registers in terms of the LR clock.

Bit:	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	LRM	—	—	—	BRM	—	—	—	LRS	—	—	—	BRS
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
23 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	LRM	0	R/W	LR Clock Reverse Master Specifies whether to invert the master LR clock. 0: Clock not inverted 1: Clock inverted
11 to 9	—	All 0	R	Reserved
8	BRM	0	R/W	Bit Clock Reverse Master Specifies whether to invert the master bit clock. 0: Clock not inverted 1: Clock inverted
7 to 5	—	All 0	R	Reserved
4	LRS	0	R/W	LR Clock Reverse Slave Specifies whether to invert the slave LR clock. 0: Clock not inverted 1: Clock inverted

Bit	Bit Name	Initial Value	R/W	Description
3 to 1	—	All 0	R	Reserved
0	BRS	0	R/W	Bit Clock Reverse Slave Specifies whether to invert the slave bit clock. 0: Clock not inverted 1: Clock inverted

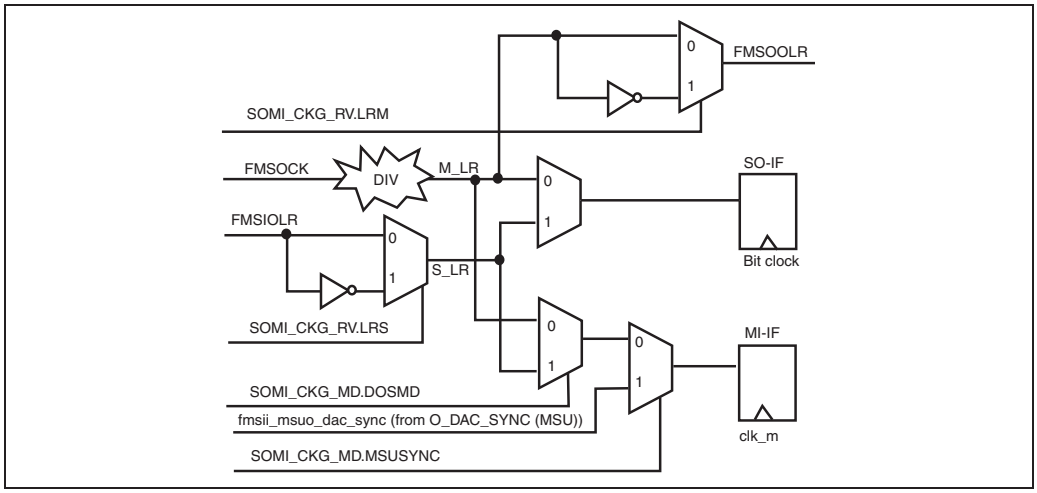


Figure 51.26 LR Clock Selector for SO-IF and MI-IF Modules (Inversion, Master/Slave)

51.14.17 SI-IF and MSUO-IF Operating Clock Set Register (SIMO_CKG_MD)

SIMO_CKG_MD is a 24-bit readable/writable register. It generates the master clock and selects audio clock used in the SI-IF module.

Bit:	23	22	21	20	19	18	17	16
	—	—	—	MSUOG	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	ACKMD[2:0]			—	BPFMD[2:0]			—	—	—	DOPMD	—	—	—	DISMD
Initial value:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
R/W:	R	R/(W)*1	R/(W)*1	R/(W)*1	R	R/(W)*1	R/(W)*1	R/(W)*1	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
23 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	MSUOG	0	R/W	Controls the timing signal to be output to the MSU. 0: Gated (fixed to low) until SI-IF ® MSUO-IF is selected. 1: Output regardless of the mode.
19 to 15	—	All 0	R	Reserved
14 to 12	ACKMD*	000	R/W	Audio Clock Mode Specifies the audio clock used to generate the master LR clock. Select the audio clock (fs) to be input in terms of a multiple of the sampling frequency (fs). 000: 512 fs 001: 256 fs 010: 128 fs 011: 64 fs 100: 32 fs Setting these bits is not necessary for slave operation.
11	—	0	R	Reserved

Bit	Bit Name	Initial Value	R/W	Description
10 to 8	BPFMD*	001	R/W	Bit/Fs Mode Sets the division ratio of the master bit clock. 111: 16 bit/fs 000: 32 bit/fs 001: 64 bit/fs 010: 128 bit/fs 011: 256 bit/fs 100: 512 bit/fs 101: Setting prohibited 110: Setting prohibited Setting these bits is not necessary for slave operation.
7 to 5	—	All 0	R	Reserved
4	DOPMD	0	R/W	Data Output Parallel Mode Selects master or slave operation for the MSUO-IF module. 0: Slave operation 1: Master operation
3 to 1	—	All 0	R	Reserved
0	DISMD	0	R/W	Data Input Serial Mode Selects master or slave operation for the SI-IF module. 0: Slave operation 1: Master operation

Note: Some values cannot be set depending on the format and transfer bus width. For the formats and the ACKMD and BPFMD bit settings, refer to section 51.19.

51.14.18 SI-IF and MSUO-IF Operating Clock Invert Register (SIMO_CKG_RV)

SIMO_CKG_RV is a 24-bit readable/writable register that specifies whether to invert bit clocks and LR clocks. In master mode, set the bits according to the formats of the external ADC and DAC. In slave operation, set the bits so that the external clock is input to the circuit at the falling edge of the LR clock and the rising edge of the bit clock. Figure 51.4 shows the relation among clock inversion, the master/slave selector, and the clock setting registers in terms of the LR clock.

Bit:	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	LRM	—	—	—	BRM	—	—	—	LRS	—	—	—	BRS
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
23 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	LRM	0	R/W	LR Clock Reverse Master Specifies whether to invert the master LR clock. 0: Clock not inverted 1: Clock inverted
11 to 9	—	All 0	R	Reserved
8	BRM	0	R/W	Bit Clock Reverse Master Specifies whether to invert the master bit clock. 0: Clock not inverted 1: Clock inverted
7 to 5	—	All 0	R	Reserved
4	LRS	0	R/W	LR Clock Reverse Slave Specifies whether to invert the slave LR clock. 0: Clock not inverted 1: Clock inverted

Bit	Bit Name	Initial Value	R/W	Description
3 to 1	—	All 0	R	Reserved
0	BRS	0	R/W	Bit Clock Reverse Slave Specifies whether to invert the slave bit clock. 0: Clock not inverted 1: Clock inverted

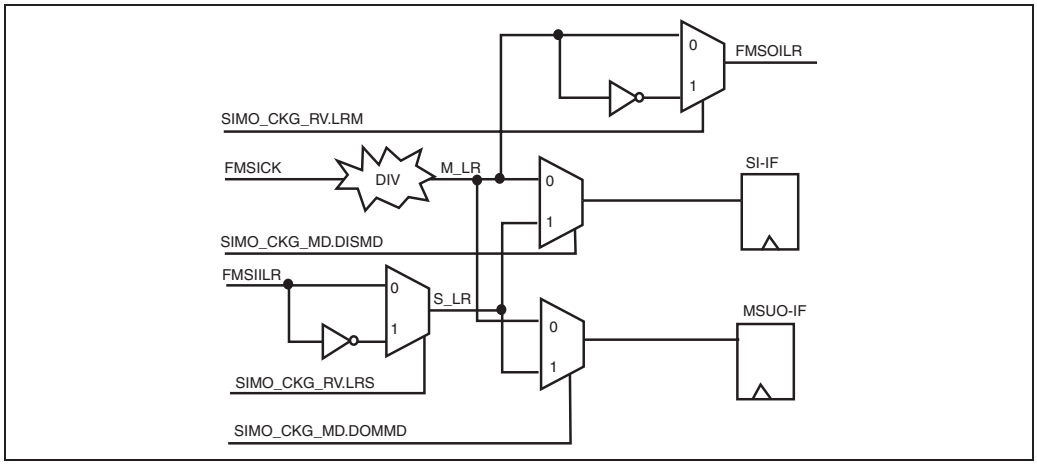


Figure 51.27 LR Clock Selector for SI-IF and MSUO-IF Modules (Inversion, Master/Slave)

51.14.19 Clock System Set Register (CKG_SMD)

CKG_SMD is a 24-bit readable/writable register. The FMSI has two clock systems. Set this register to operate the FMSI with only one clock system.

Bit:	23	22	21	20	19	18	17	16
	—	—	—	MSMD	—	—	—	SSMD
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
23 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	MSMD	0	R/W	Master Synchronism Mode Master mode 0: Two clock systems 1: One clock system
19 to 17	—	All 0	R	Reserved
16	SSMD	0	R/W	Slave Synchronism Mode Slave mode 0: Two clock systems 1: One clock system
15 to 0	—	All 0	R	Reserved

Figure 51.28 shows the external audio clock pins of the FMSI. In master mode operation with one clock system, FMSOCK is valid and the signals that have the same phases as (FMSOOBT, FMSOOLR) and (FMSOIBT, FMSOILR) are output as the master output clocks. In slave mode operation with one clock system, FMSIOBT and FMSIOLR are valid.

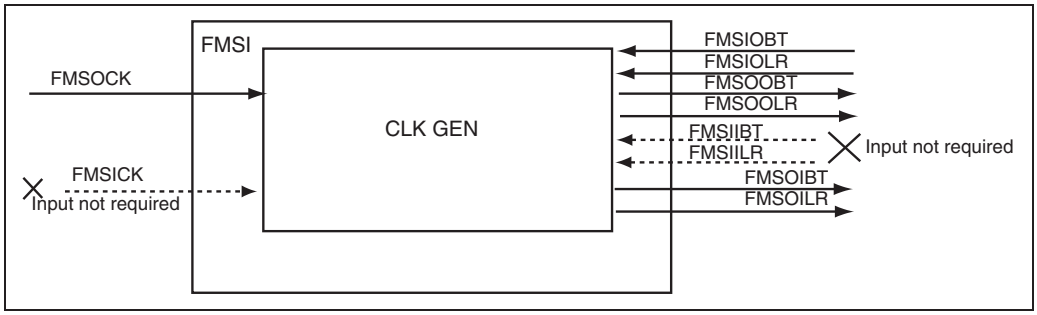


Figure 51.28 FMSI Audio Clock Pins

In operation with one clock system, the master clock is generated using the SOMI_CKG_MD register. The operation clock invert registers SOMI_CKG_RV and SIMO_CKG_RV can be set. Note that, however, the same value must be set for these two registers because the outputs have the same phase.

In operation with one clock system, SOMI_CKG_RV is used to set slave clock inversion.

51.14.20 Timer Count Set Register (TMR_CTL)

TMR_CTL is a 24-bit readable/writable register that controls timer operation. The counter counts the number of samples transferred in master/slave operation of the SO and SI systems. When the counter value reaches the set value, an interrupt source is generated.

Bit:	23	22	21	20	19	18	17	16
	SI[3:0]				SO[3:0]			
Initial value:	1	0	1	1	1	0	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SOM
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
23 to 20	SI	1011	R/W	Sampling Frequency for the SI System Sets the value of the counter at which an interrupt source is to be generated. 0000: 1 0001: 2 0010: 4 0011: 8 0100: 16 0101: 32 0110: 64 0111: 128 1000: 256 1001: 512 1010: 1024 1011: 2048 1100: 4096 1101: 8192 1110: 16384 1111: 32768

Bit	Bit Name	Initial Value	R/W	Description
19 to 16	SO	1011	R/W	Sampling Frequency for the SO System Sets the value of the counter at which an interrupt source is to be generated. (The settings are the same as for bits 23 to 20.)
15 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	SOM	0	R/W	Sampling Frequency Setting for Counting for the SO System 0: SO-IF 1: MI-IF

51.14.21 Timer Count Clear Register (TMR_CLR)

TMR_CLR is a 24-bit readable/writable register that clears the counter and the interrupt source that is asserted on a counter overflow.

Bit:	23	22	21	20	19	18	17	16
	—	—	—	SI_CLR	—	—	—	SO_CLR
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
23 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	SI_CLR	0	R/W	Clears the counter for the SI system. 0: Retains a count value. 1: Clears the counter and the interrupt source.
19 to 17	—	All 0	R	Reserved
16	SO_CLR	0	R/W	Clears the counter for the SO system. 0: Retains a count value. 1: Clears the counter and the interrupt source.
15 to 0	—	All 0	R	Reserved

Figure 51.29 shows a block diagram of the timer control circuit.

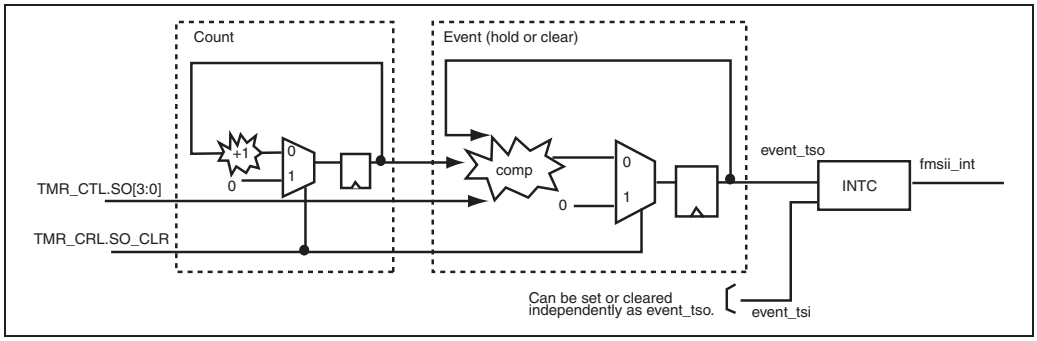


Figure 51.29 Block Diagram of the Timer Control Circuit

The interrupt source for the interrupt control block (INTC) is asserted when the counter overflows and held asserted until cleared. In the interrupt handling routine, clear the counter before clearing the interrupt source.

51.14.22 Direct Serial Transfer Set Register (DRCT_SRL)

DRCT_SRL is a 24-bit readable/writable register that sets direct transfer of parallel and serial data at the same sampling frequency without reading and writing registers (I/O).

Bit:	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	SIMD[1:0]		—	—	—	SOMD
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
23 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5, 4	SIMD	00	R/W	Serial Input Mode Select 00: IO (3) Serial input → DSP-IO 10: MSUO-IF (4) Serial input → parallel (MSU) output Other than those above: Reserved. (Setting prohibited.)
3 to 1	—	All 0	R	Reserved
0	SOMD	0	R/W	Serial Output Mode Select 0: IO (1) DSP-IO → serial output 1: MI-IF (2) Parallel (SCUV) input → serial output

51.14.23 Interrupt State Register (INT_ST)

INT_ST is a 24-bit readable/writable register that retains 6 sources of the FIFO and timer interrupts separately. Only writing 0 to clear is accepted. Writing 1 does not change the bit value. To clear a specific interrupt source, write 0 to the corresponding bit and 1 to the other bits.

The interrupt state register is set if the specified interrupt condition matches the FIFO and timer status while the corresponding interrupt mask is cleared. If an interrupt source is cleared at the same time as the interrupt source occurs, the interrupt condition takes precedence.

Bit:	23	22	21	20	19	18	17	16
	—	—	—	IESTATSI	—	—	—	IESTATSO
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/(W)*	R	R	R	R/(W)*

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	IESTAEPI	IESTAPI	—	—	IESTAESI	IESTASI	—	—	IESTAESO	IESTASO
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/(W)*	R/(W)*	R	R	R/(W)*	R/(W)*	R	R	R/(W)*	R/(W)*

Bit	Bit Name	Initial Value	R/W	Description
23 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20*	IESTATSI	0	R/W	SI System Timer Interrupt Event Status 1: Clears the interrupt source. 0: Retains the interrupt source.
19 to 17	—	All 0	R	Reserved
16*	IESTATSO	0	R/W	SO System Timer Interrupt Event Status 1: Clears the interrupt source. 0: Retains the interrupt source.
15 to 10	—	All 0	R	Reserved
9*	IESTAEPI	0	R/W	Parallel Input FIFO Error Status 1: Clears the interrupt source. 0: Retains the interrupt source.
8*	IESTAPI	0	R/W	Parallel Input FIFO Interrupt Event Status 1: Clears the interrupt source. 0: Retains the interrupt source.

Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	All 0	R	Reserved
5*	IESTAESI	0	R/W	Serial Input FIFO Error Status 1: Clears the interrupt source. 0: Retains the interrupt source.
4*	IESTASI	0	R/W	Serial Input FIFO Interrupt Event Status 1: Clears the interrupt source. 0: Retains the interrupt source.
3, 2	—	All 0	R	Reserved
1*	IESTAESO	0	R/W	Serial Output FIFO Error Status 1: Clears the interrupt source. 0: Retains the interrupt source.
0*	IESTASO	0	R/W	Serial Output FIFO Interrupt Event Status 1: Clears the interrupt source. 0: Retains the interrupt source.

Note: Writing 0 to this bit clears the interrupt source. Writing 1 does not change the bit value.

51.14.24 Interrupt Source Mask Register (IEMSK)

IEMSK is a 24-bit readable/writable register that masks the interrupt source for each FIFO. If this register masks an interrupt source, the interrupt source is not enabled even if the IMSK register described below unmasks the interrupt signal. Thus, the interrupt does not occur.

Bit:	23	22	21	20	19	18	17	16
	—	—	—	IEMSKTSI	—	—	—	IEMSKTSO
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	IEMSKEPI	IEMSKPI	—	—	IEMSKESI	IEMSKSI	—	—	IEMSKESO	IEMSKSO
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
23 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	IEMSKTSI	0	R/W	SI System Timer Interrupt Source Mask 0: Interrupt source masked 1: Interrupt source enabled
19 to 17	—	All 0	R	Reserved
16	IEMSKTSO	0	R/W	SO System Timer Interrupt Source Mask 0: Interrupt source masked 1: Interrupt source enabled
15 to 10	—	All 0	R	Reserved
9	IEMSKEPI	0	R/W	Parallel Input FIFO Error Interrupt Source Mask 0: Interrupt source masked 1: Interrupt source enabled
8	IEMSKPI	0	R/W	Parallel Input FIFO Interrupt Source Mask 0: Interrupt source masked 1: Interrupt source enabled
7, 6	—	All 0	R	Reserved

Bit	Bit Name	Initial Value	R/W	Description
5	IEMSKESI	0	R/W	Serial Input FIFO Error Interrupt Source Mask 0: Interrupt source masked 1: Interrupt source enabled
4	IEMSKSI	0	R/W	Serial Input FIFO Interrupt Source Mask 0: Interrupt source masked 1: Interrupt source enabled
3, 2	—	All 0	R	Reserved
1	IEMSKESO	0	R/W	Serial Output FIFO Error Interrupt Source Mask 0: Interrupt source masked 1: Interrupt source enabled
0	IEMSKSO	0	R/W	Serial Output FIFO Interrupt Source Mask 0: Interrupt source masked 1: Interrupt source enabled

51.14.25 Interrupt Signal Mask Register (IMSK)

IMSK is a 24-bit readable/writable register that masks each interrupt signal. For the relationship among interrupt status, interrupt source mask, and interrupt signal mask, refer to section 51.15.4, Interrupt Interface Specifications.

Bit:	23	22	21	20	19	18	17	16
	—	—	—	IMSKTSI	—	—	—	IMSKTSO
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	IMSKEPI	IMSKPI	—	—	IMSKESI	IMSKSI	—	—	IMSKESO	IMSKSO
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
23 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	IMSKTSI	0	R/W	SI System Timer Interrupt Signal Mask 0: Interrupt signal masked 1: Interrupt signal enabled
19 to 17	—	All 0	R	Reserved
16	IMSKTSO	0	R/W	SO System Timer Interrupt Signal Mask (Same as bit 20) 0: Interrupt signal masked 1: Interrupt signal enabled
15 to 10	—	All 0	R	Reserved
9	IMSKEPI	0	R/W	Parallel Input FIFO Error Interrupt Signal Mask (Same as bit 20) 0: Interrupt signal masked 1: Interrupt signal enabled
8	IMSKPI	0	R/W	Parallel Input FIFO Interrupt Signal Mask (Same as bit 20) 0: Interrupt signal masked 1: Interrupt signal enabled

Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	All 0	R	Reserved
5	IMSKESI	0	R/W	Serial Input FIFO Error Interrupt Signal Mask (Same as bit 20) 0: Interrupt signal masked 1: Interrupt signal enabled
4	IMSKSI	0	R/W	Serial Input FIFO Interrupt Signal Mask (Same as bit 20) 0: Interrupt signal masked 1: Interrupt signal enabled
3, 2	—	All 0	R	Reserved
1	IMSKESO	0	R/W	Serial Output FIFO Error Interrupt Signal Mask (Same as bit 20) 0: Interrupt signal masked 1: Interrupt signal enabled
0	IMSKSO	0	R/W	Serial Output FIFO Interrupt Signal Mask (Same as bit 20) 0: Interrupt signal masked 1: Interrupt signal enabled

51.14.26 MUTE Set Register (MUTE)

MUTE is a 24-bit readable/writable register that enables the MUTE function. Set MUTE on/off after selecting MUTE mode.

Bit:	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	MUTEPI	MUTETPI	—	—	MUTESI	MUTETSI	—	—	MUTESO	MUTETSO
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
23 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	MUTEPI	0	R/W	Mute Parallel Input Enables parallel input MUTE. 0: MUTE off 1: MUTE on
9	MUTETPI	0	R/W	Mute Type Parallel Input Selects parallel input MUTE mode. 0: Normal MUTE 1: Zero cross MUTE
7, 6	—	All 0	R	Reserved
5	MUTESI	0	R/W	Mute Serial Input Enables serial input MUTE. 0: MUTE off 1: MUTE on
4	MUTETSI	0	R/W	Mute Type Serial Input Selects serial input MUTE mode. 0: Normal MUTE 1: Zero cross MUTE
3, 2	—	All 0	R	Reserved

Bit	Bit Name	Initial Value	R/W	Description
1	MUTESO	0	R/W	Mute Serial Output Enables serial output MUTE. 0: MUTE off 1: MUTE on
0	MUTETSO	0	R/W	Mute Type Serial Output Selects serial output MUTE mode. 0: Normal MUTE 1: Zero cross MUTE

51.14.27 Clock Reset Register (CLK_RST)

CLK_RST is a 24-bit readable/writable register that resets the counter for generating the master clock. To operate the FMSI in master mode, set the formats and clocks before releasing the reset. During reset, the LR and bit clocks are not output to the external and internal IF blocks. However, when the frequency division ratio of the bit clock frequency to fs is 1:1, the bit clock pulses continue to be applied.

Bit:	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	SICR	—	—	—	SOCR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/(W)*	R	R	R	R/(W)*

Bit	Bit Name	Initial Value	R/W	Description
23 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4*	SICR	0	R/W	SI-IF Clock Reset Resets the counter for generating master clock for the SI system. 0: Resets the counter. 1: Releases a reset.
3 to 1	—	All 0	R	Reserved
0*	SOCR	0	R/W	SO-IF Clock Reset Resets the counter for generating master clock for the SO system. 0: Resets the counter. 1: Releases a reset.

Note: This bit should be asserted longer than the audio clock period so that the counter synchronized with it is reset.

51.14.28 Software Reset Register (SOFT_RST)

SOFT__RST is a 24-bit readable/writable register that resets the internal buffers, registers and interrupt signal.

Bit:	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	SISR	—	—	—	SOSR	—	—	—	IR	—	—	—	SR
Initial value:	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
R/W:	R	R	R	R/(W)*	R	R	R	R/(W)*	R	R	R	R/W	R	R	R	R/W

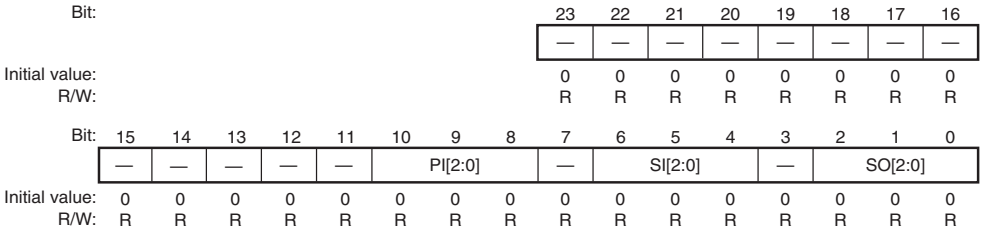
Bit	Bit Name	Initial Value	R/W	Description
23 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12*	SISR	1	R/W	Serial Input Soft Reset Resets the SI-IF module. Initializes the FFs synchronized with the bit clock in the SI-IF module. 0: Issues a reset. 1: Releases a reset.
11 to 9	—	All 0	R	Reserved
8*	SOSR	1	R/W	Serial Output Soft Reset Resets the SO-IF module. Initializes the FFs synchronized with the bit clock in the SO-IF module. 0: Issues a reset. 1: Releases a reset.
7 to 5	—	All 0	R	Reserved

Bit	Bit Name	Initial Value	R/W	Description
4	IR	1	R/W	Interrupt Reset Negates the interrupt signal (fmsio_int) even when the acknowledge signal (fmsii_int_ack) is not returned. 0: Issues a reset. 1: Releases a reset.
3 to 1	—	All 0	R	Reserved
0	SR	1	R/W	Software Reset Initializes all the registers. 0: Issues a reset. 1: Releases a reset.

Note: The SISR and SOSR bits should be asserted longer than the period of the bit clock applied to the SI-IF and SO-IF modules.

51.14.29 FIFO Size Register (FIFO_SZ)

FIFO_SZ is a 24-bit read-only register that indicates the capacity of the externally-connected DP-RAM.



Bit	Bit Name	Initial Value	R/W	Description
23 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 8	PI	000	R	Parallel Input Parallel input FIFO capacity Indicates the capacity of the connected DP-RAM. 000: 256 words These bits are always read as 000.
7	—	0	R	Reserved
6 to 4	SI	000	R	Serial Input Serial input FIFO capacity (The settings are the same as for bits 10 to 8.) These bits are always read as 000.
3	—	0	R	Reserved
2 to 0	SO	000	R	Serial Output Serial output FIFO capacity (The settings are the same as for bits 10 to 8.) These bits are always read as 000.

51.15 Interface Specifications

51.15.1 FMSI Access Specifications

(1) FMSI and DSP-IO Connection

The FMSI uses an 8-bit address space (8'h00 to 8'hFF). The FMSI registers can be read and written via the SPU2 DSP/IO bus. Figure 51.30 shows I/O space mapping viewed from the DSP side. 16-bit space from 0000 to FEFF is provided as a peripheral area. When connecting the FMSI to the DSP-IO, use an address decoder that asserts the write enable (fmsii_io_wr) and read enable (fmsii_io_rd) only for the specified upper 8-bit address. Figure 51.31 shows connection between the FMSI and DSP-IO.

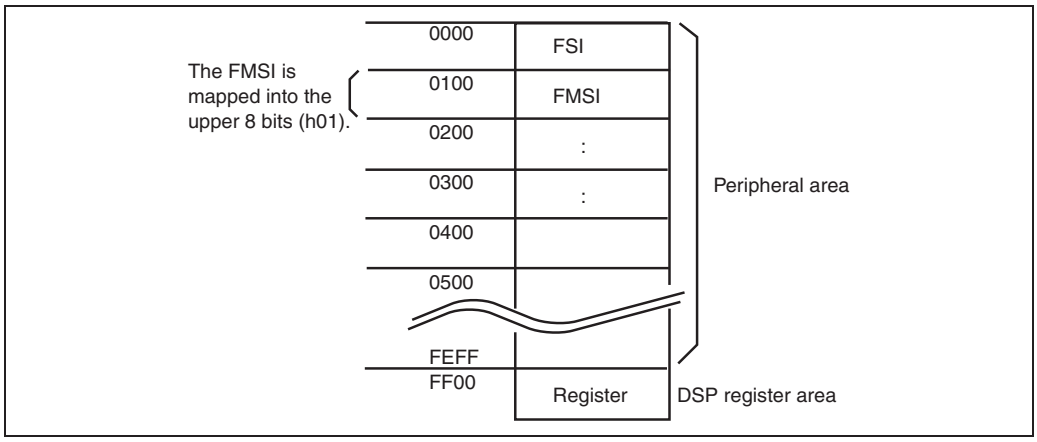


Figure 51.30 Example of DSP-IO Space Mapping

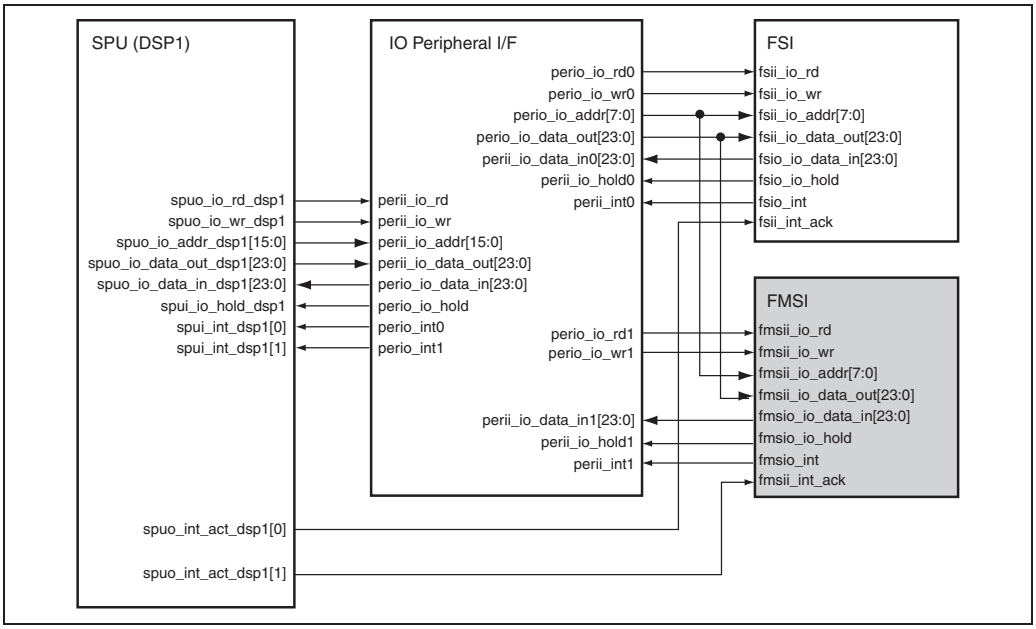


Figure 51.31 Example of Address Decoder for FMSI and DSP-IO Connection

(2) FMSI Access Timing

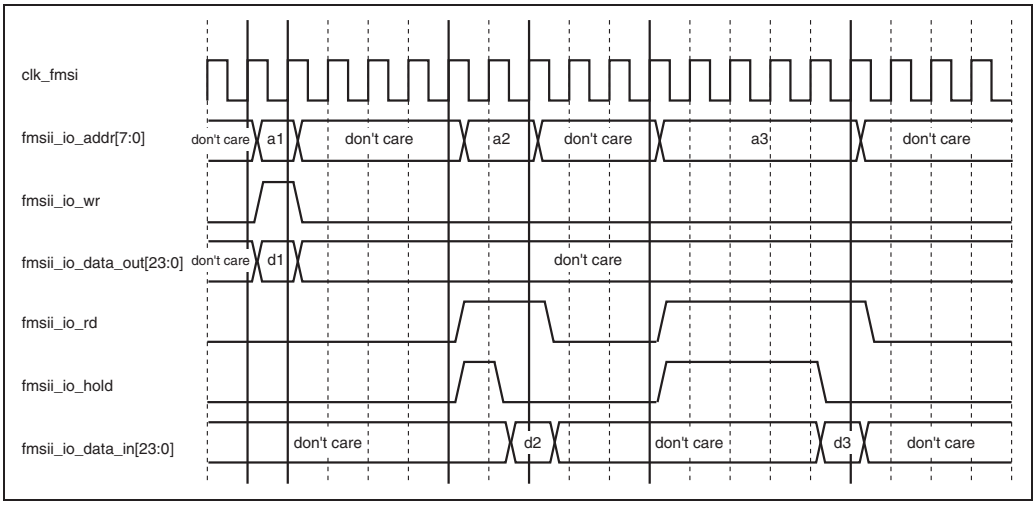


Figure 51.32 FMSI and DSP-IO Connection

Figure 51.32 shows the FMSI access timing. Write accesses are performed with no wait cycles. In read accesses, the hold signal fmsio_io_hold is asserted after the read enable signal fmsii_io_rd is output.

The number of wait cycles differs depending on the address. For the FIFO read address (S_DIDT, P_DIDT), the hold signal is kept asserted for one to four wait cycles. The other registers output an effective value, fmsio_io_data_in[23:0], after one wait cycle.

Table 51.12 summarizes the number of wait cycles for the accessible registers.

Table 51.12 Wait Cycles for FMSI Register Read/Write

Register	Read	Write
S_DIDT, P_DIDT	Initial read: 4 waits 2nd and following reads: 1 wait	Prohibited
Other registers	1 wait	No wait

51.15.2 Clock Interface Specifications

Figure 51.33 shows a block diagram of clock signals. Table 51.13 lists the FMSI clocks.

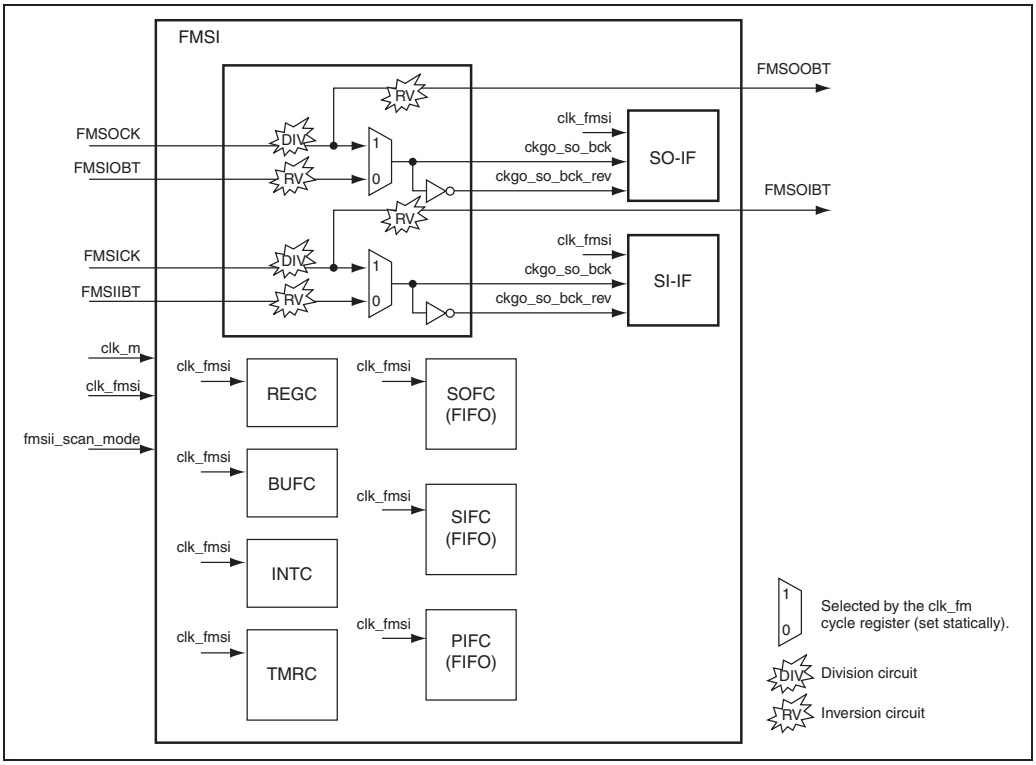


Figure 51.33 Block Diagram of FMSI Clock Inputs

The modules in the thick-line frames in figure 51.33 provide asynchronous processing.

Table 51.13 FMSI Clock Pins

Clock Name	Category	Type	Description	Synchronization (clk_fmsi basis)
clk_fmsi	Common	G4 internal	DSP operating clock	—
clk_m	Common	G4 internal	HPB bus clock	Asynchronous
FMSOCK	SO	Input	SO audio clock	Asynchronous
FMSICK	SI	Input	SI audio clock	Asynchronous
FMSIOBT	SO	Input	SO slave bit clock	Asynchronous
FMSIIBT	SI	Input	SI slave bit clock	Asynchronous
ckgo_so_bck	SO	FMSI internal	SO DOIS bit clock	Asynchronous
ckgo_so_bck_rev	SO	FMSI internal	Inverted clock of ckgo_so_bck	Asynchronous
ckgo_si_bck	SI	FMSI internal	SI DIIS bit clock	Asynchronous
ckgo_si_bck_rev	SI	FMSI internal	Inverted clock of ckgo_si_bck	Asynchronous
FMSOOBT	SO	Output	SO master bit clock	Asynchronous
FMSOIBT	SI	Output	SI master bit clock	Asynchronous

51.15.3 FIFO Access Specifications

(1) FMSI and DSP-RAM Connection

Figure 51.34 shows an example of connection between the FIFO control and DP-RAM.

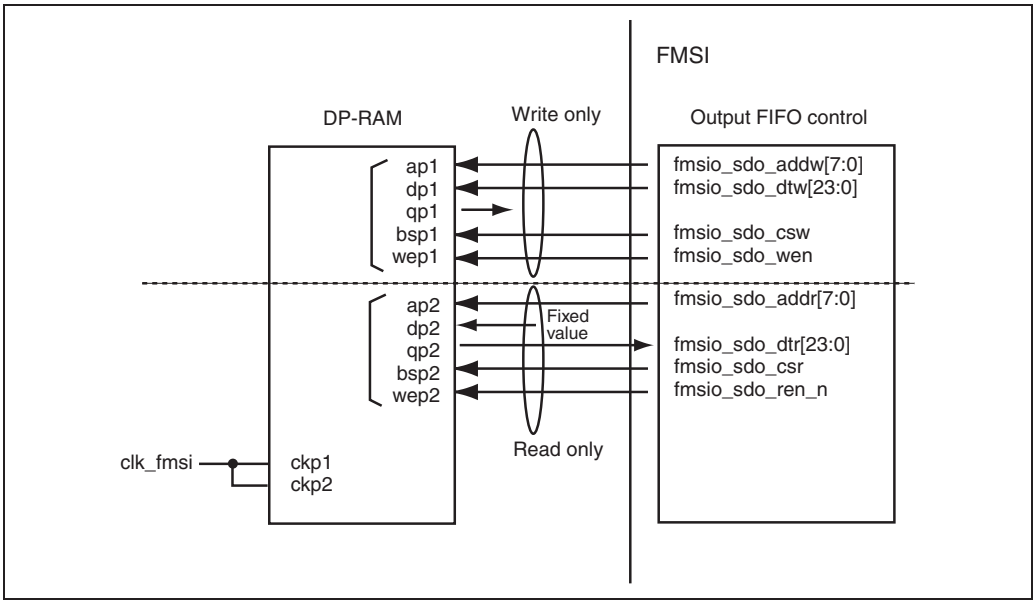


Figure 51.34 Sample Connection between Output FIFO and DP-RAM

(2) DP-RAM Access Timing

Figure 51.35 shows a timing chart of the access to the DP-RAM.

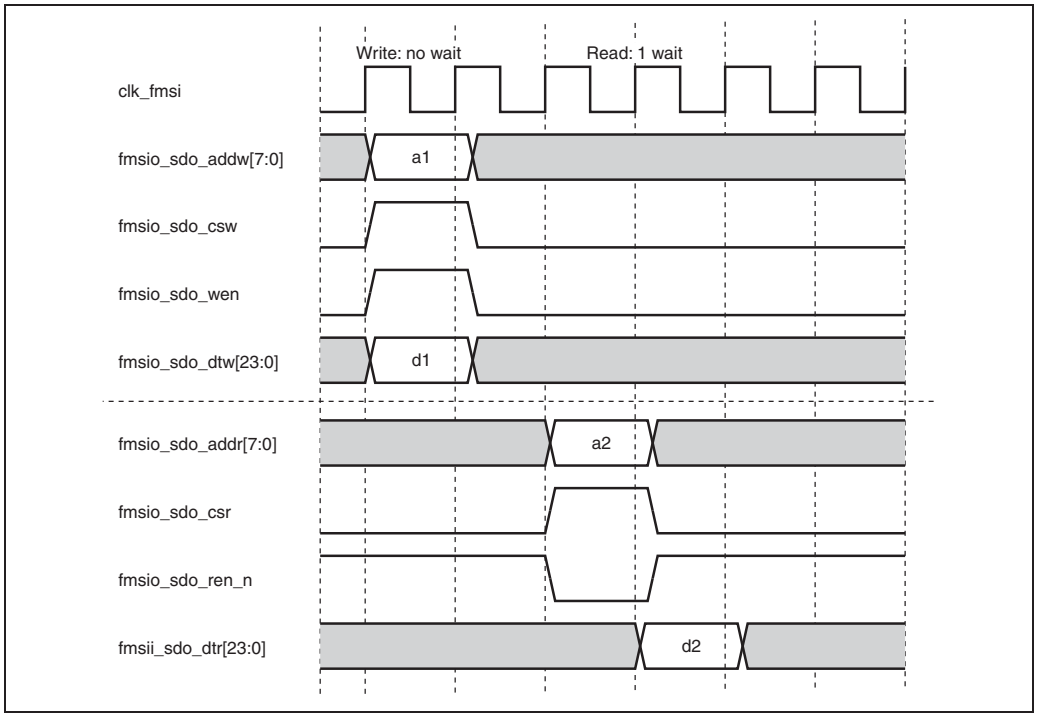


Figure 51.35 DP-RAM Access Timing

Connect a DP-RAM that can be read from or written to with the above timing. During the DP-RAM accesses, port 1 is used for write accesses only and port 2 for read accesses only. The FMSI outputs the fmsi_sdo_csw and fmsio_sdo_wen as the same signals and fmsio_sdo_csr and fmsio_sdo_ren_n as signals inverted to each other.

51.15.4 Interrupt Interface Specifications

The FMSI has one interrupt signal line. Table 51.14 shows the interrupt pin configuration.

Table51.14 Interrupt Pin Configuration

Pin Name	Input/Output	Function	Polarity
fmsio_int	Output	Interrupt requests to external modules	High
fmsii_int_ack	Input	Response to an interrupt request; the FMSI negates fmsio_int in response to fmsii_int_ack.	High

Figure 51.36 shows a register controller block for interrupt signals. Although only the int_so (serial output) is shown representatively in this figure, eight interrupt sources individually support the interrupt state and source masks and signal masks can be set independently for the sources.

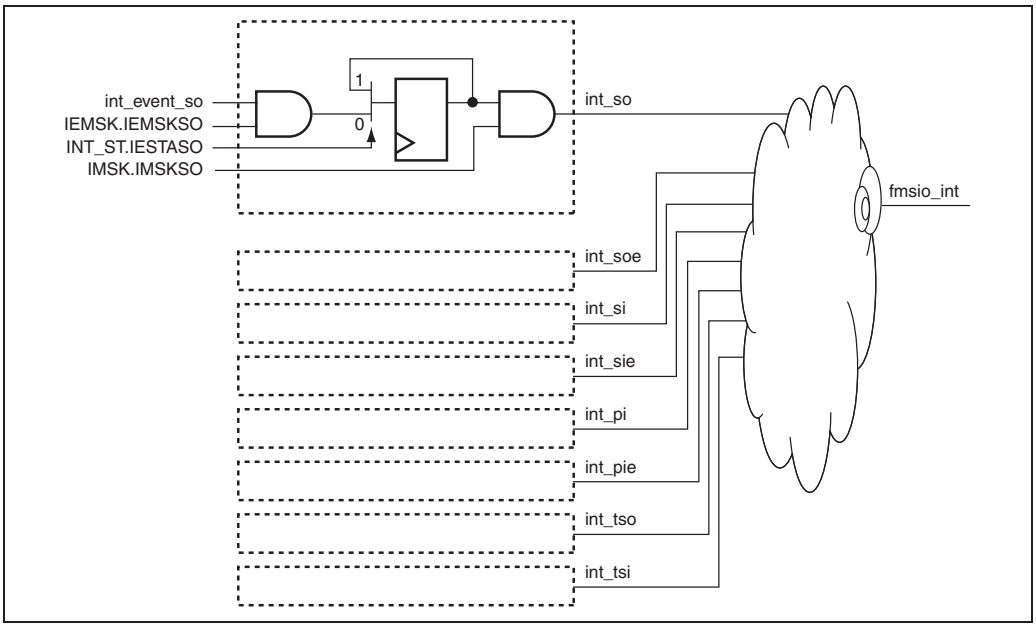


Figure 51.36 Interrupt Signals (Register Controller)

Figure 51.37 shows a timing chart of the interrupt signal. The external interrupt signal (fmsio_int) is asserted by any of eight interrupt sources. Once the interrupt signal is asserted after it is negated by fmsii_int_ack, it is never asserted again until at least one interrupt source is cleared in the status register.

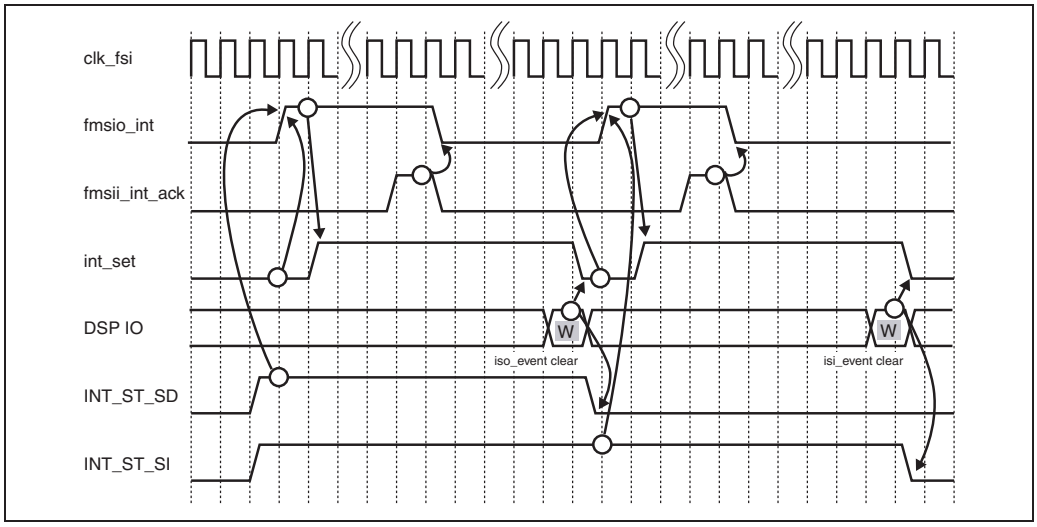


Figure 51.37 Timing Chart of Interrupt Signal

For debugging, fmsio_int can be negated without returning fmsii_int_ack by writing to the IR bit in SOFT_RST.

51.16 Reset Specifications

Table 51.15 lists the FMSI resets.

Table 51.15 FMSI Resets and Initializing Modules

Reset Name	REGC	BUFC	INTC	TMRC	CLK GEN	SOFC	SIFC	PIFC	SOIF	SIIF
Hardware reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset
Software reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset* 1	Reset* 1
SO-IF reset	—	—	—	—	—	—	—	—	Reset	—
SI-IF reset	—	—	—	—	—	—	—	—	—	Reset
Clock reset SOM	—	—	—	—	Reset	—	—	—	—	—
Clock reset SIMC	—	—	—	—	Reset	—	—	—	—	—
Interrupt reset	—	—	Reset* 2	—	—	—	—	—	—	—
Serial output FIFO clear	—	—	—	—	—	Reset	—	—	—	—
Serial input FIFO clear	—	Reset* 3	—	—	—	—	Reset	—	—	—
Parallel input FIFO clear	—	Reset* 3	—	—	—	—	—	Reset	—	—

—: Register retained.

Notes: 1. Except FFs synchronized with the bit clock
2. The interrupt signal is negated.
3. The buffer used for prefetching read data is initialized.

Details of the resets (initialized modules, initialized registers, and setting flows) are shown below.

1. Hardware Reset (rst_fmsi_n)
   Initializes all registers and modules by the active-low reset signal.
2. Software Reset (SOFT_RST.SR)
   Initializes all registers except the software reset register (SOFT_RST.SR) and all modules. In master operation, the bit clock that is used for asynchronous passing may be fixed due to a clock reset, perform a software reset after resetting SI-IF and SO-IF (see (9) Procedures for Initializing the FMSI).
3. SO-IF Reset, SI-IF Reset (SOFT_RST.SRSO, SOFT_RST.SRSI)

These are the reset signals to initialize the FFs that are synchronized with the bit clock.

Since the bit clock is used for asynchronous passing, this reset requires to wait for longer than 1 bit clock cycle after a register write to perform it.

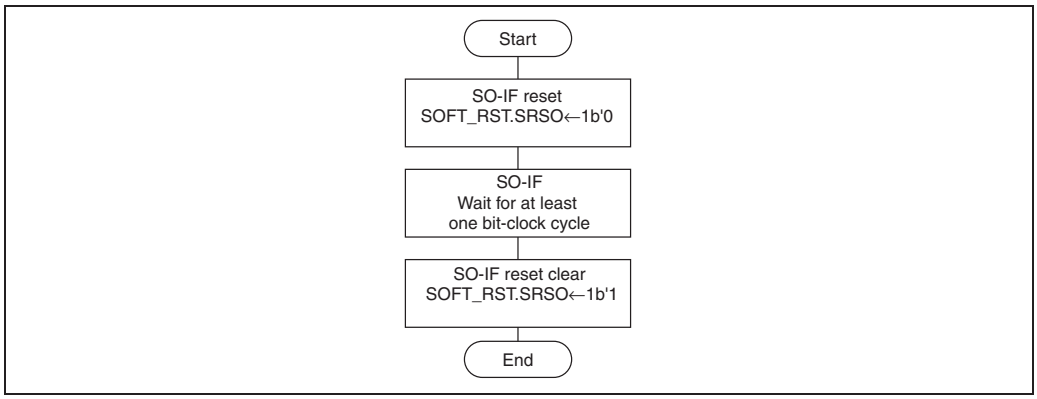


Figure 51.38 Flow of SO-IF Reset (Same for SI-IF Reset)

4. Clock Resets SOMI and SIMO (CLK_RST.CRSOMI, CLK_RST.CRSIMO)

   These are the reset signals to initialize the counters that are synchronized with the audio clock for generating the master clock.

   Since the audio clock is used for asynchronous passing, this reset requires to wait for longer than 1 audio clock cycle after a register write to perform it.

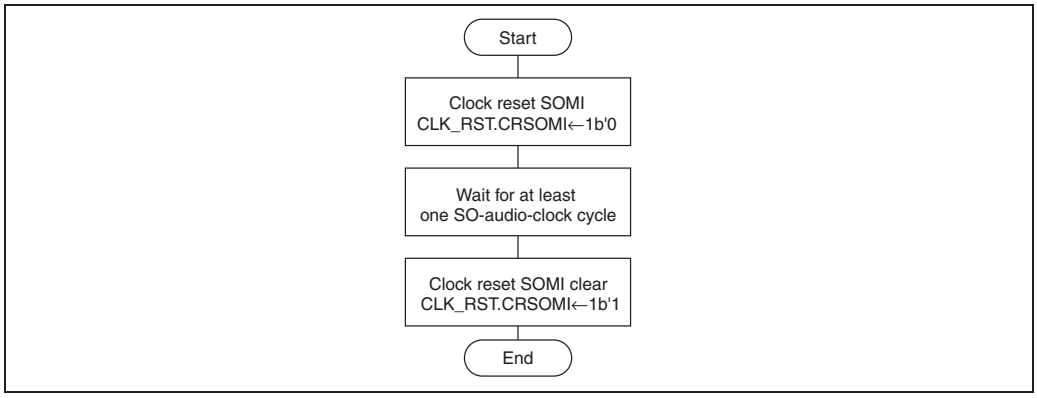


Figure 51.39 Flow of Clock Reset SOMI (Same for Clock Reset SIMO)

5. Interrupt Reset (SOFT_RST.IR)

Negates the interrupt signal (fmsio_int) when the corresponding register is written. The reset should be released after the negation.

6. Serial Output FIFO Clear (S_DOFF_CTL.CLR)

   Clears the address pointer of the serial FIFO control block (SOFC) and the error history.

7. Serial Input FIFO Clear (S_DIFF_CTL.CLR)

   Clears the address pointer of the serial FIFO control block (SIFC), the error history, and buffers for continuous 1-wait reads.

8. Parallel Input FIFO Clear (P_DIFF_CTL.CLR)

   Clears the address pointer of the parallel FIFO control block (PIFC), the error history, and buffers for continuous 1-wait reads.

9. Procedures for Initializing the FMSI

   The procedures for initializing the FMSI are shown in figure 51.40. There are two types of procedures: one by using a hardware reset and another by using a software reset. To achieve the same effect as a hardware reset, perform a software reset after SO-IF reset or SI-IF reset (initializing the FFs that are synchronized with the bit clock).

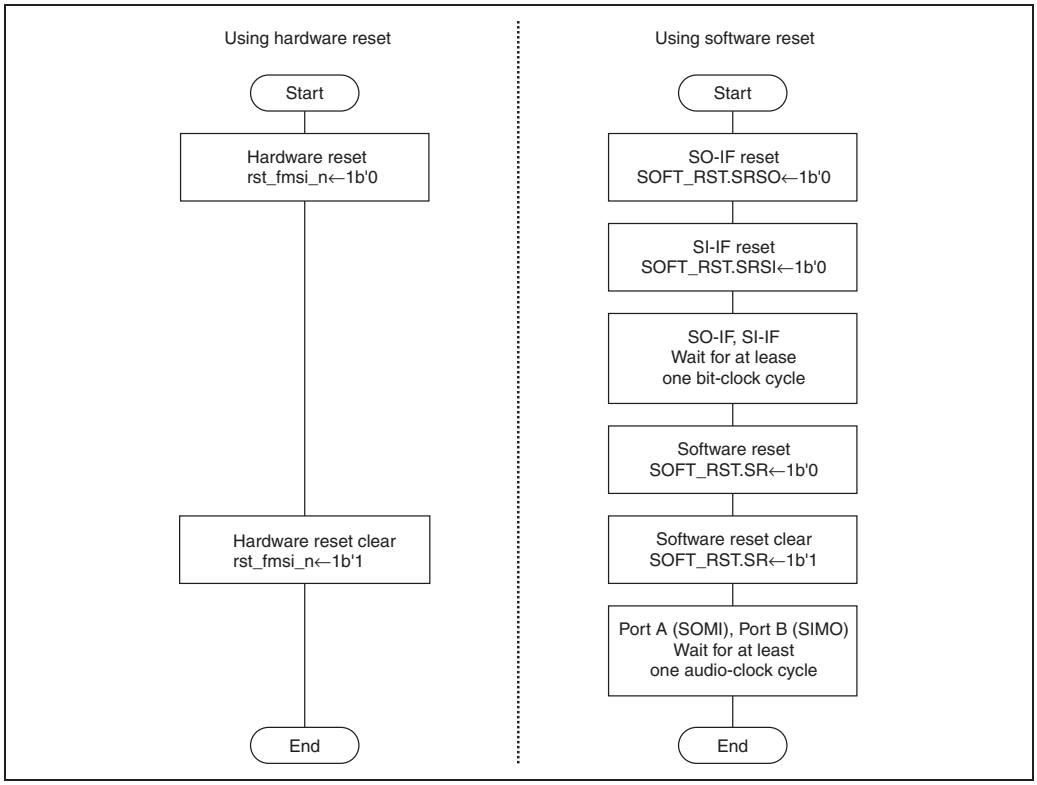


Figure 51.40 Flow of FMSI Initialization Operation

51.17 MUTE Specifications

The FMSI has normal MUTE and zero cross MUTE functions for input/output operations. The MUTE circuits are implemented for output FIFO control block (SOFC) and input FIFO control block (SIFC and PIFC).

51.17.1 Normal MUTE

The normal MUTE mutes on a per sample data basis. It is turned on (outputs 0) for channel 1 first 2 samples after it is enabled. Similarly, it is turned off for channel 1 first 2 samples after it is disabled.

Figure 51.41 shows the 2-channel audio output and the MUTE signal.

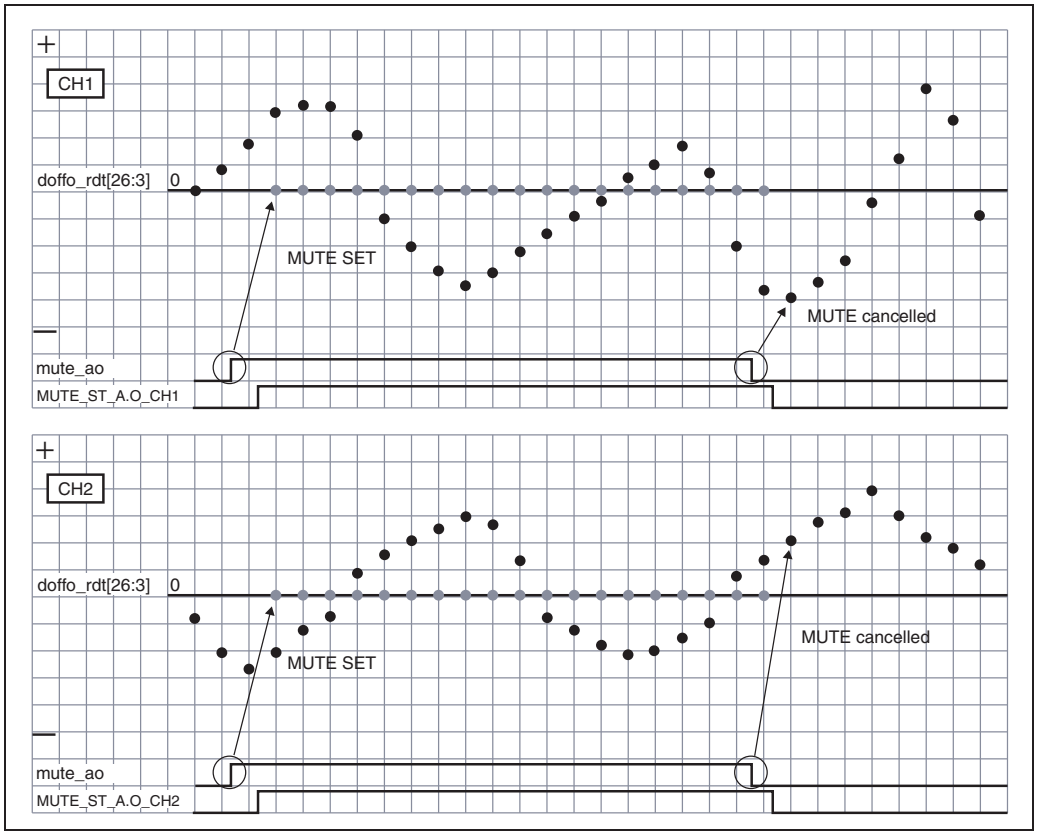


Figure 51.41 Normal MUTE Specification (Output Operation)

When the MUTE signal is asserted in input operation, the conversion module (input I2S) takes data written to input FIFOs and writes 0 to the DP-RAM.

51.17.2 Zero Cross MUTE

If the zero cross MUTE function is enabled, it compares current data to the previous one on each channel independently.

The conditions for turning on the mute are (1) the previous data is 0, (2) current data is 0, and (3) the sign of current data does not match the one of the previous data.

If any of these conditions ((1) to (3)) is satisfied, the mute is turned on (0 is output) until the zero cross MUTE function is disabled.

The mute (outputting 0) is turned off, just like it is turned on, if any of the conditions ((1) to (3)) is satisfied when current data is compared to the previous one on each channel independently.

Figure 51.42 shows the 2-channel audio output and zero cross MUTE signal.

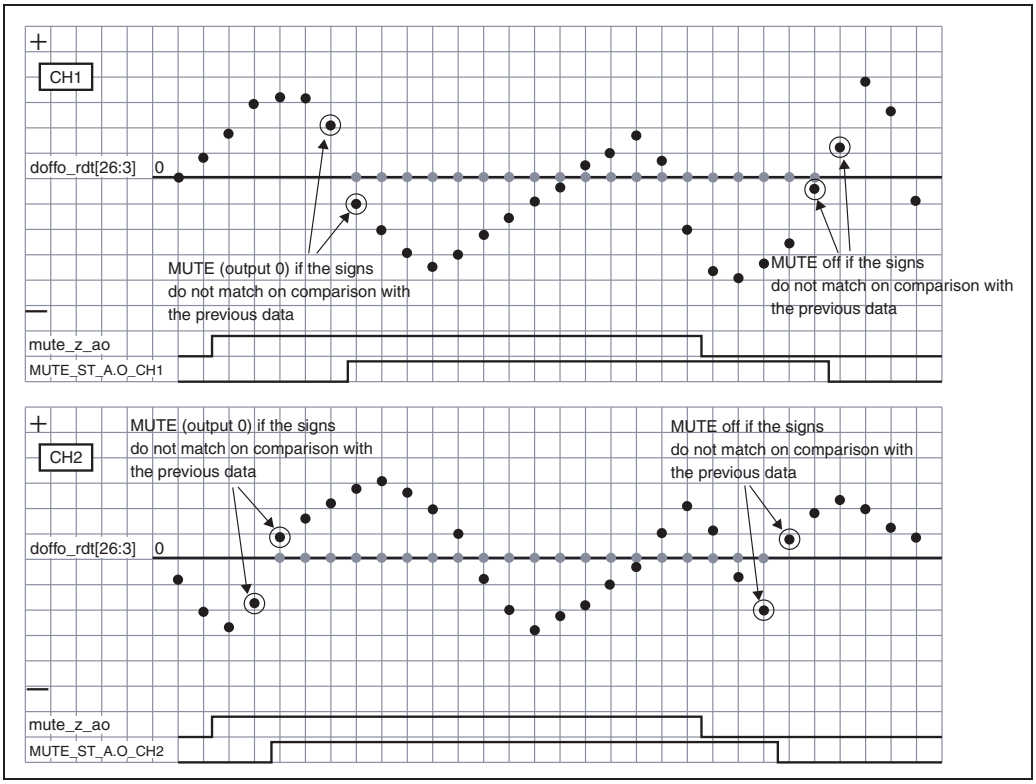


Figure 51.42 Zero Cross MUTE Specification (Output Operation)

Even if the zero cross MUTE function is enabled, the mute (outputting 0) is not turned on unless any of the conditions (1) to (3) is met.

Even if any of the conditions (1) to (3) is met, the mute (outputting 0) is not turned off unless the zero cross MUTE function is disabled.

After the zero cross MUTE function is enabled, it can be switched to the normal MUTE function to turn on/off the mute forcibly.

When the MUTE signal is asserted in input operation, the conversion module (input I2S) compares data written to input FIFOs to determine if the conditions (1) to (3) are met and writes 0 to the DP-RAM.

51.18 FIFO Overflow/Underflow

51.18.1 Specifications

When an underflow or overflow error occurs, the FIFO contains the error related information in a register. This section describes underflows and overflows in the output FIFOs and input FIFOs.

An output FIFO underflow occurs when the SO-IF requests data (req) while the FIFO is empty. When it occurs, the output FIFO outputs 24'h0 and the channel number [2:0]. An overflow occurs when the DSP tries to write more data than the FIFO capacity. Such write operations are ignored. No overflow occurs under management by the DSP.

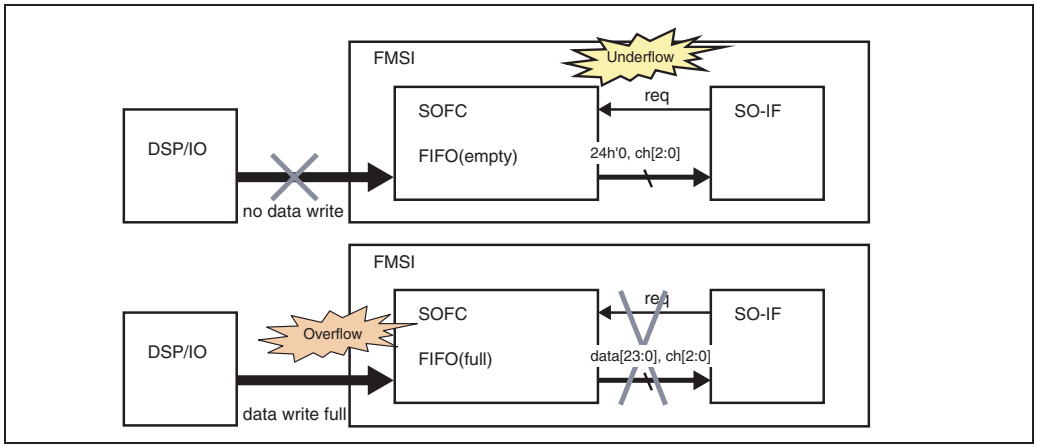


Figure 51.43 Output FIFO Underflow/Overflow

An input FIFO overflow occurs if 3-line serial data is input to the FIFO externally when it is full. The write to the input FIFO that caused an overflow is ignored. An underflow occurs when a read request is issued by the DSP while the input FIFO is empty. When it occurs, the read request returns 0. No underflow occurs under management by the DSP.

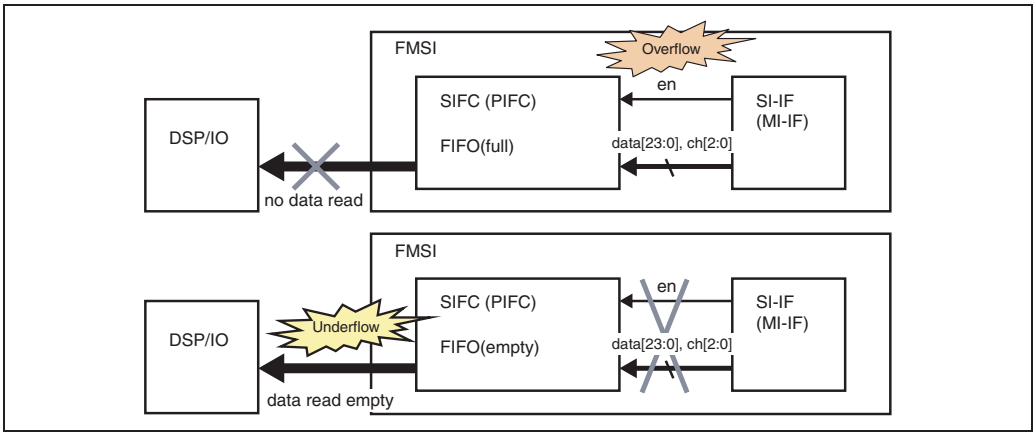


Figure 51.44 Input FIFO Overflow/Underflow

51.18.2 Error Flag Clear

Table 51.16 lists the FMSI error flags. The FMSI uses six error flags. Figures 51.45 and 51.46 show error flag clear flows for serial output and serial input, respectively.

Table 51.16 List of Error Flags

Register Name	Description	
S_DOFF_ST.OF	Serial output	Overflow error
S_DOFF_ST.UF		Underflow error
S_DIFF_ST.OF	Serial input	Overflow error
S_DIFF_ST.UF		Underflow error
P_DIFF_ST.OF	Parallel input	Overflow error
O_DIFF_ST.UF		Underflow error

(1) Clearing Serial Output Overflow Error

If an overflow occurs during serial output operation and the flag is detected, perform the processing specific to the application and clear the flag.

(2) Clearing Serial Output Underflow Error

If an underflow occurs during serial output operation and the flag is detected, perform the processing specific to the application, write the output data to S_DODT, and clear the flag.

(3) Clearing Serial Input Overflow Error

If an overflow occurs during serial input operation and the flag is detected, perform the processing specific to the application, read the input data from S_DIDT, and clear the flag.

(4) Clearing Serial Input Underflow Error

If an underflow occurs during serial input operation and the flag is detected, perform the processing specific to the application and clear the flag.

(5) Clearing Parallel Input Overflow Error

Same as (3) above.

(6) Clearing Parallel Input Underflow Error

Same as (4) above.

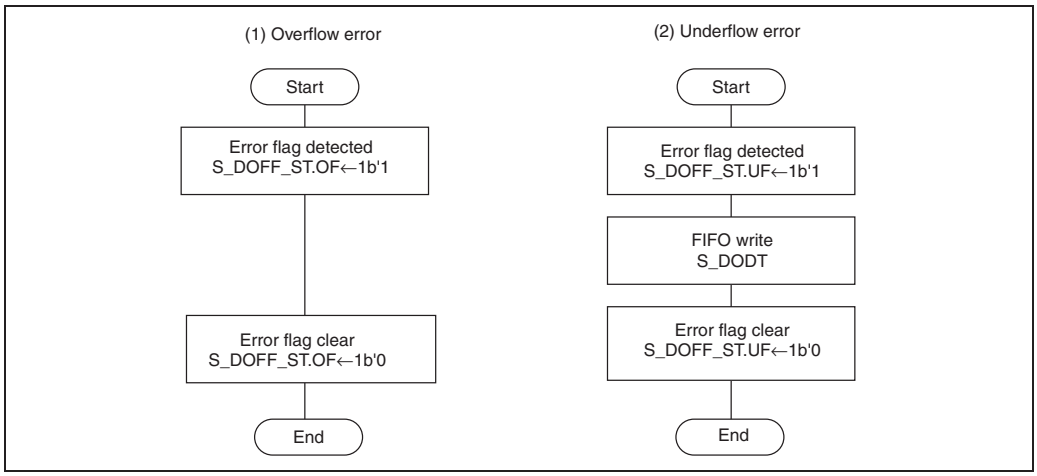


Figure 51.45 Flow for Clearing Serial Output Error Flag

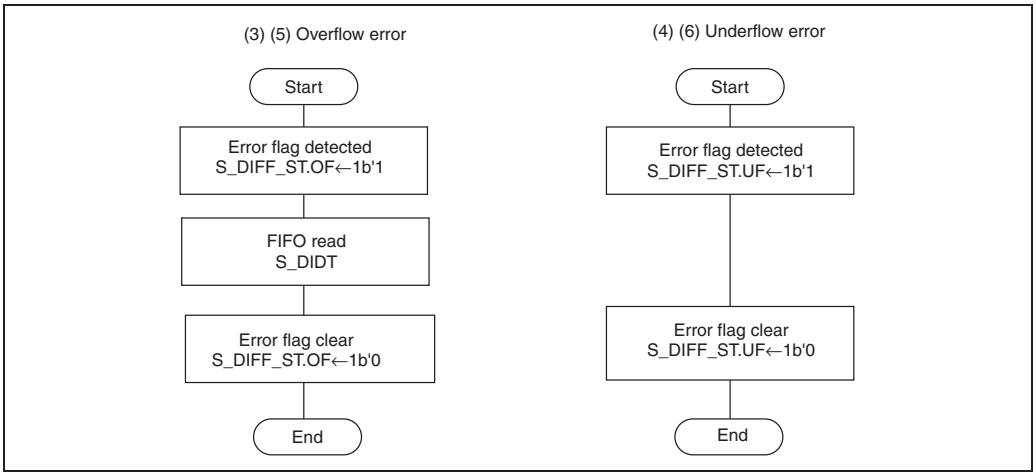


Figure 51.46 Flow for Clearing Serial Input Error Flag

51.19 FIFO Clear

Each FIFO controller has a FIFO clear function. This function performs the following:

1. Clearing the UF/OF error history
   Clears the FIFO status to 0.
2. Clearing the address pointer of the FIFO control
   Initializes the counter that controls the DP-RAM access. When a FIFO clear is performed, the address pointer returns to the start address and data prior to the clear is overwritten.
3. Clearing data prefetched by the BUFC block and the buffer pointer
   Clears data prefetched by the BUFC block for continuous reads and the buffer pointer.
4. Masking the FIFO control block
   Can be enabled for the request (CH1) corresponding to the second sample after a FIFO clear. This is because the state of the mask is determined by the request (output) and enable (input) after the format and clock settings is fixed.

51.20 Direct Transfer

The FMSI supports the following two types of direct transfers to perform serial input/output without using the DSP.

1. MI-IF → SO-IF (DRCT_SRL.SOMD = 1'b1)
2. SI-IF → MSUO-IF (DRCT_SRL.SIMD = 2'b10)

Table 51.17 shows formats and clock settings for the direct transfer.

Table 51.17 Formats and Clock Settings for Direct Transfer

Type	Input-Side Format	Output-Side Format	Bus Width
1	1 channel	MONO, MONO_Delay	24 or 16 bits only
	2 channels	PCM, I2S	↑
2	MONO, MONO_Delay	1 channel	16 bits only

In type 2 transfer above, the MSUO-IF supports only the 16-bit 1-channel transfer. Thus, there is no register to select the transfer format. Select an appropriate serial transfer format in the input-side.

51.21 Audio Format

51.21.1 Serial Format

Tables 51.18 and 51.19 show serial formats in which operation is guaranteed for the FMSI. The audio clock and format can be set independently for input and output.

Table 51.18 List of Supported Serial Formats (24-Bit Transfer)

	MONO, MONO Delay	I2S, PCM	TDM, TDM Delay
Operating Clock	**BPFMD**	**BPFMD**	**BPFMD**
Master ACKMD: 32 fs	32 bits/fs	Setting prohibited	Setting prohibited
Master ACKMD: 64 fs	64 bits/fs 32 bits/fs	64 bits/fs	Setting prohibited
Master ACKMD: 128 fs	128 bits/fs 64 bits/fs 32 bits/fs	128 bits/fs 64 bits/fs	128 bits/fs
Master ACKMD: 256 fs	256 bits/fs 128 bits/fs 64 bits/fs 32 bits/fs	256 bits/fs 128 bits/fs 64 bits/fs	256 bits/fs 128 bits/fs
Master ACKMD: 512 fs	512 bits/fs 256 bits/fs 128 bits/fs 64 bits/fs 32 bits/fs	512 bits/fs 256 bits/fs 128 bits/fs 64 bits/fs	512 bits/fs 256 bits/fs 128 bits/fs
Slave	32 bits/fs or more	64 bits/fs or more	128 bits/fs or more (4 channels) 256 bits/fs or more (8 channels)

Table 51.19 List of Supported Serial Formats (16-Bit Transfer)

	MONO, MONO Delay	I2S, PCM	TDM, TDM Delay
Operating Clock	**BPFMD**	**BPFMD**	**BPFMD**
Master	32 bits/fs	32 bits/fs	Setting prohibited
ACKMD: 32 fs	16 bits/fs		
Master	64 bits/fs	64 bits/fs	64 bits/fs
ACKMD: 64 fs	32 bits/fs	32 bits/fs	
	16 bits/fs		
Master	128 bits/fs	128 bits/fs	128 bits/fs
ACKMD: 128 fs	64 bits/fs	64 bits/fs	64 bits/fs
	32 bits/fs	32 bits/fs	
	16 bits/fs		
Master	256 bits/fs	256 bits/fs	256 bits/fs
ACKMD: 256 fs	128 bits/fs	128 bits/fs	128 bits/fs
	64 bits/fs	64 bits/fs	64 bits/fs
	32 bits/fs	32 bits/fs	
	16 bits/fs		
Master	512 bits/fs	512 bits/fs	512 bits/fs
ACKMD: 512 fs	256 bits/fs	256 bits/fs	256 bits/fs
	128 bits/fs	128 bits/fs	128 bits/fs
	64 bits/fs	64 bits/fs	64 bits/fs
	32 bits/fs	32 bits/fs	
	16 bits/fs		
Slave	16 bits/fs or more	32 bits/fs or more	64 bits/fs or more (4 channels)
			128 bits/fs or more (8 channels)

The serial conversion section (SO-IF, SI-IF) operates based on the falling edge of the LR clock that is inverted on the rising edge of the bit clock. Although the master clock is generated according to the specification in master operation, the inversion register needs to be set properly if the external LR and bit clocks are input directly in slave operation. Along with serial data formats, the inversion settings for slave operation are shown below for reference. The LR clock and bit clock, which are output during master operation, can be inverted according to the DAC and ADC

specifications. In the MONO and MONO_Delay formats shown in figures 51.47 and 51.48, these clocks are not inverted. In the other formats, the bit clock is inverted to be output.

Register settings during master operation (address xxx indicates a serial output):

- MONO and MONO_Delay formats in figures 51.47 and 51.48:
  xxx_CKG_RV.LRM =
- PCM, I2S, TDM, and TDM_Delay formats in figures 51.49 to 51.56:
  xxx_CKG_RV.LRM =

The main formats for 3-line serial data are shown below.

In delay mode (I2S), MSB data is output one bit-clock cycle behind the LR clock.

The MONO and MONO_Delay serial data formats are shown below.

(1) MONO (1 channel), 24-bit and 16-bit

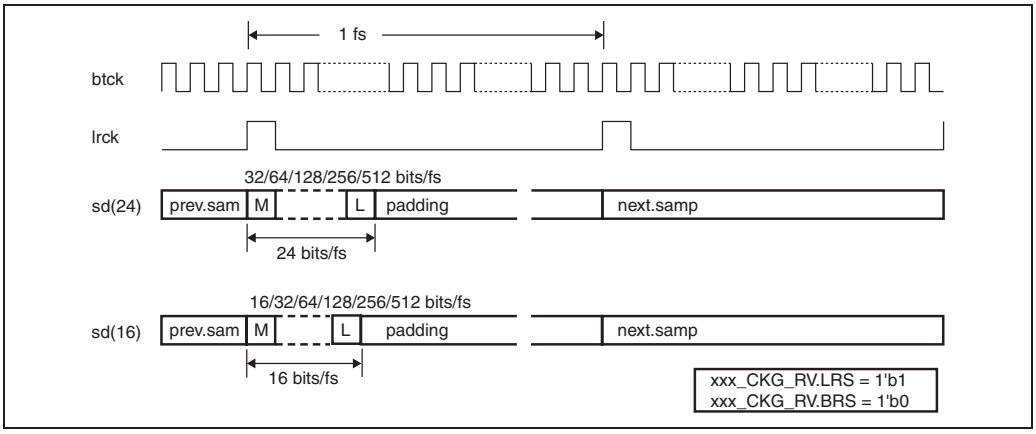


Figure 51.47 MONO Format

(2) MONO_Delay (1 channel), 24-bit and 16-bit

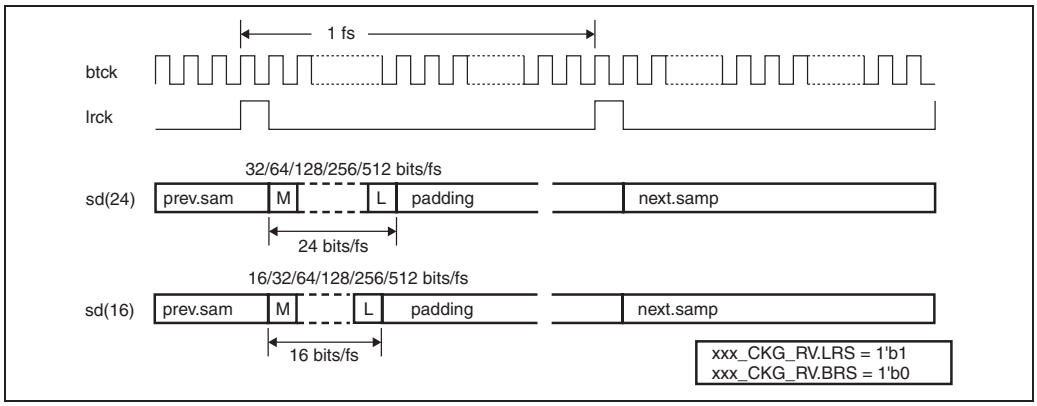


Figure 51.48 MONO_Delay Format

The PCM serial data formats are shown below.

(3) PCM (2 channels) 64 bits/fs, 24-bit and 16-bit

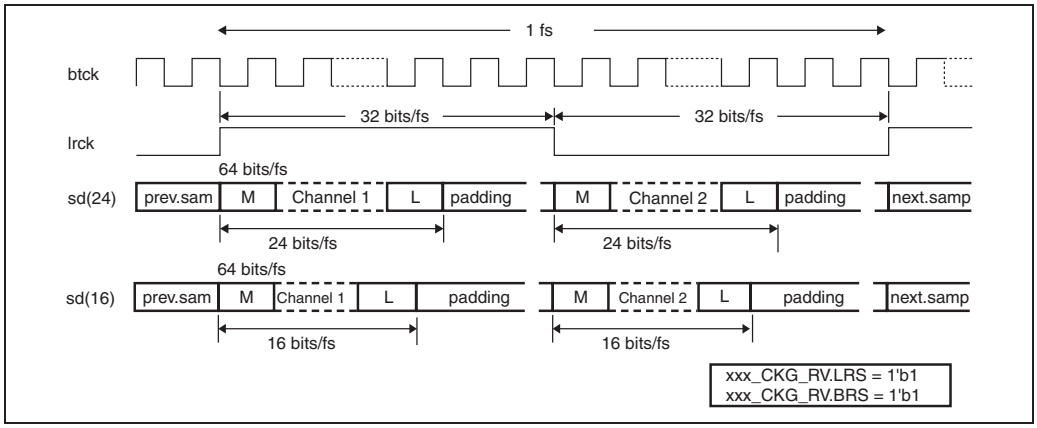


Figure 51.49 PCM Format (64 bits/fs)

(4) PCM (2 channels) 128 bits/fs, 24-bit and 16-bit

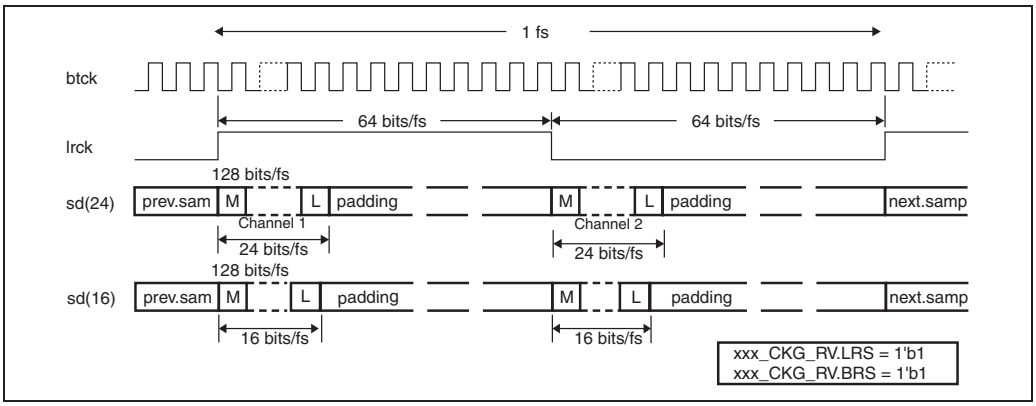


Figure 51.50 PCM Format (128 bits/fs)

The I2S serial data formats are shown below.

(5) I2S (2 channels) 64 bits/fs, 24-bit and 16-bit

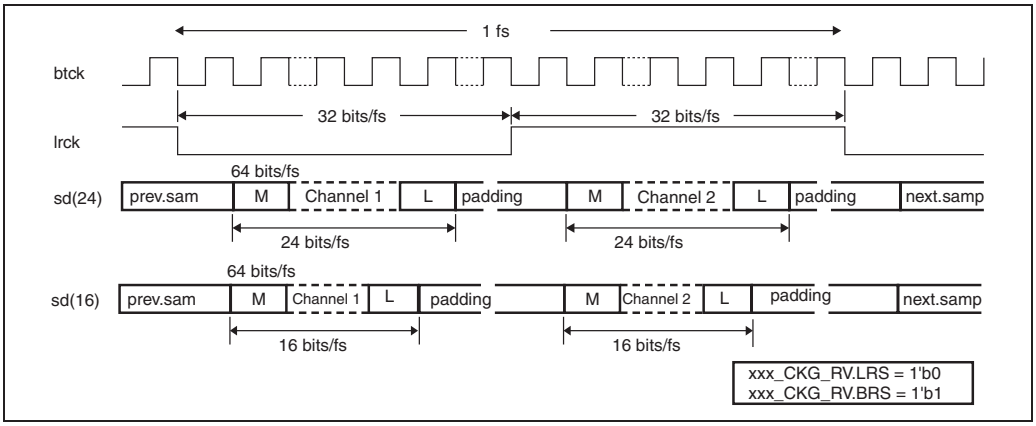


Figure 51.51 I2S Format (64 bits/fs)

(6) I2S (2 channels) 128 bits/fs, 24-bit and 16-bit

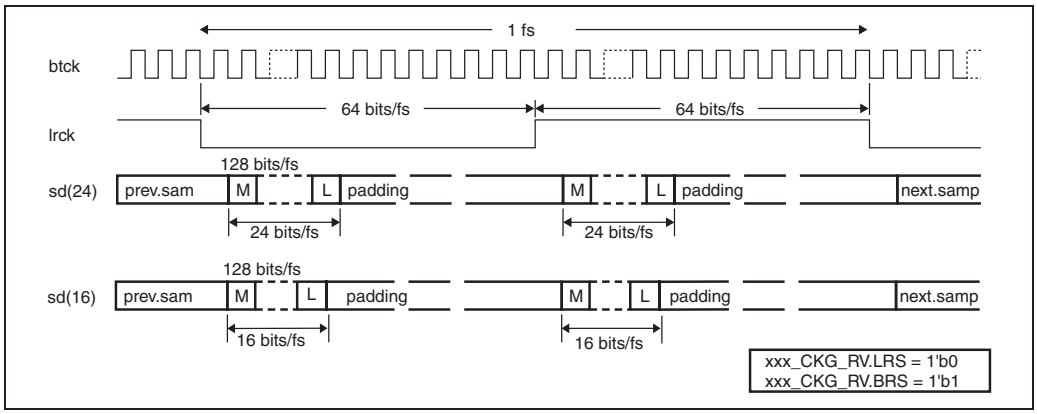


Figure 51.52 I2S Format (128 bits/fs)

The TDM and TDM_Delay serial data formats are shown below.

(7) TDM (8 channels) 256 bits/fs, 24-bit

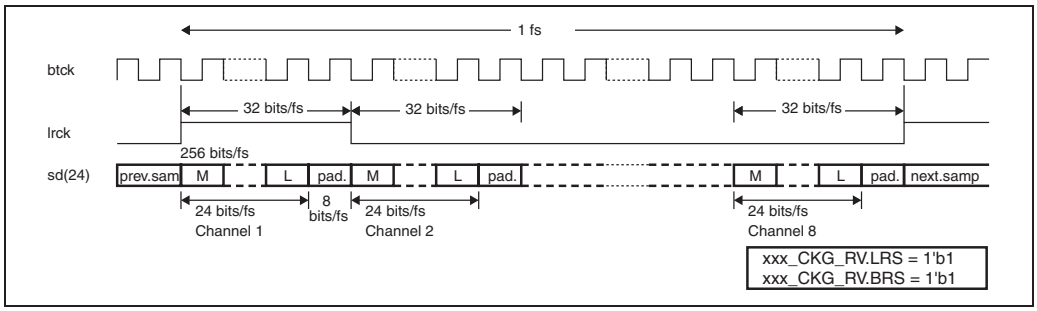


Figure 51.53 TDM Format (256 bits/fs, 24-bit)

(8) TDM (8 channels) 512 bits/fs, 24-bit

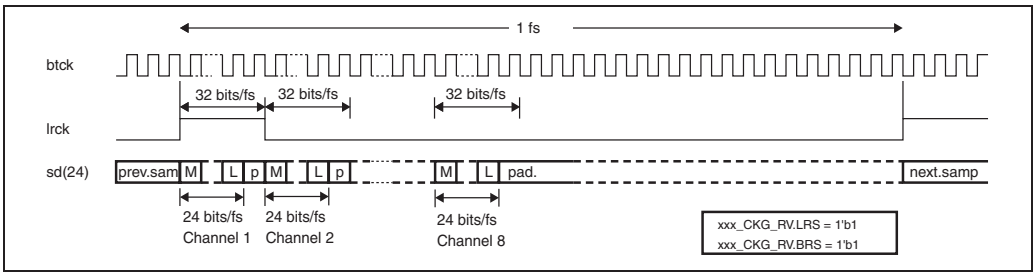


Figure 51.54 TDM Format (512 bits/fs, 24-bit)

(9) TDM_Delay (8 channels) 512 bits/fs, 24-bit

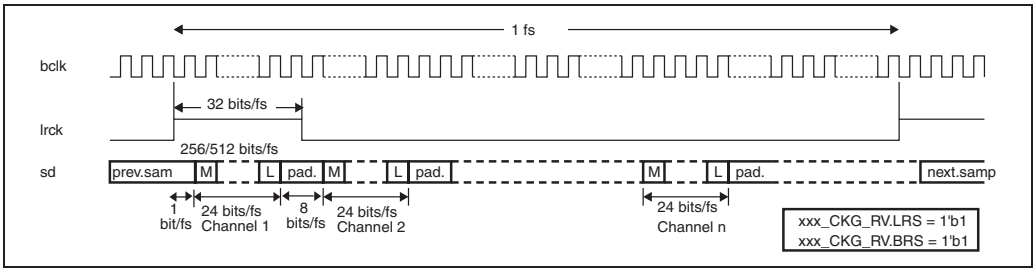


Figure 51.55 TDM_Delay Format (512 bits/fs, 24-bit)

(10) TDM (8 channels) 128 bits/fs, 16-bit

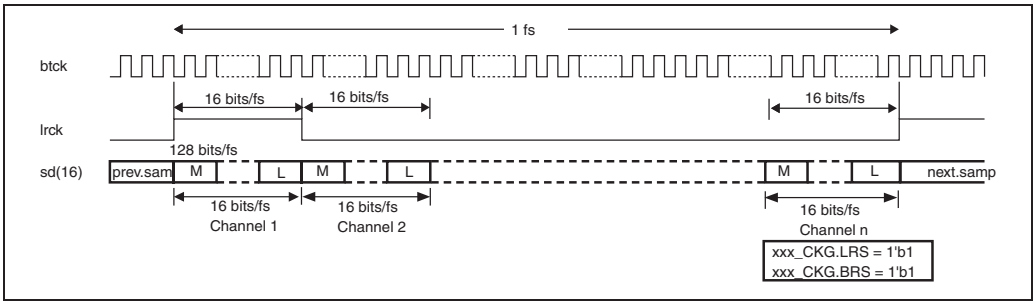


Figure 51.56 TDM Format (128 bits/fs, 16-bit)

51.21.2 Parallel Format

The FMSI supports the following parallel transfer formats.

Table 51.20 Parallel Transfer Formats (Common to 24-bit and 16-bit transfers)

Port SIMO	Port SOMI
MSUO-IF (1CH)	**MI-IF (1CH or 2CH)**
Master, ACKMD: 32 fs	Master, ACKMD: 32 fs
Master, ACKMD: 64 fs	Master, ACKMD: 64 fs
Master, ACKMD: 128 fs	Master, ACKMD: 128 fs
Master, ACKMD: 256 fs	Master, ACKMD: 256 fs
Master, ACKMD: 512 fs	Master, ACKMD: 512 fs
Slave	Slave

Figure 51.57 shows the MI-IF timing chart.

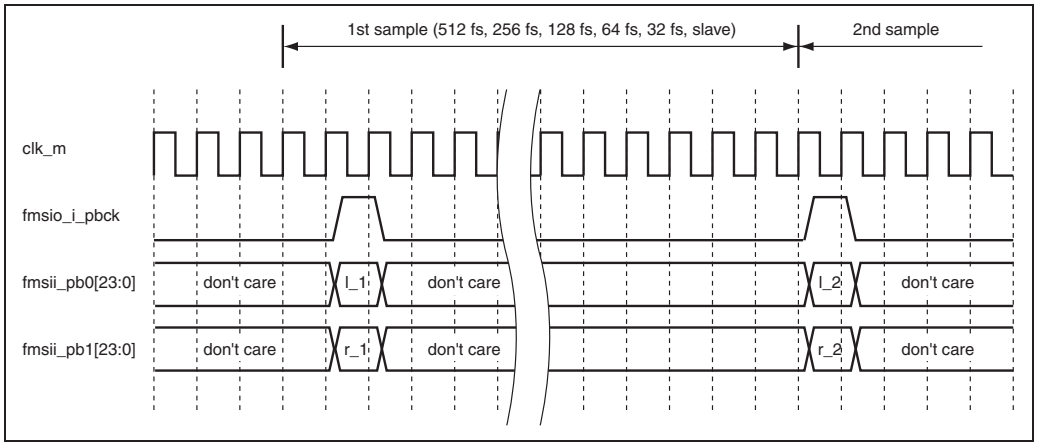


Figure 51.57 MI-IF Timing Chart

Figure 51.58 shows the MSUO-IF timing chart.

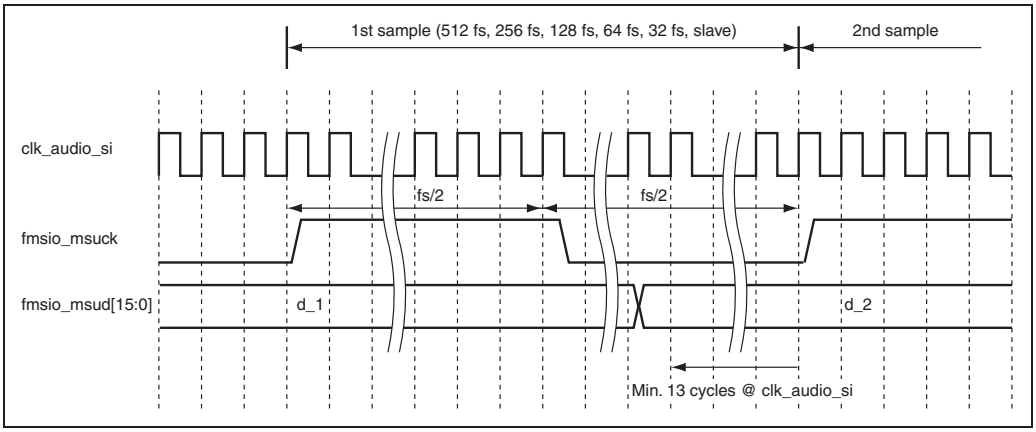


Figure 51.58 MSUO-IF Timing Chart

fmsio_msud[15:0] are received at the falling edge of fmsio_msuck and are asynchronized with clk_fmsi before being output. The output value is settled at least 13 cycles before the rising edge of fmsio_msuck.

51.22 Operation Flows

The FMSI operation flows are shown below. The FMSI can be accessed from the SPU2 DSP and CPU (via the SPU2). Before an access to the FMSI from the CPU, the clock should be supplied to the SPU2 and the SPUSRST bit in SPUSRST should be set to 1 to release the SPU2 software reset.

Figure 51.59 shows the relation between the entire FMSI operation and individual processing flows.

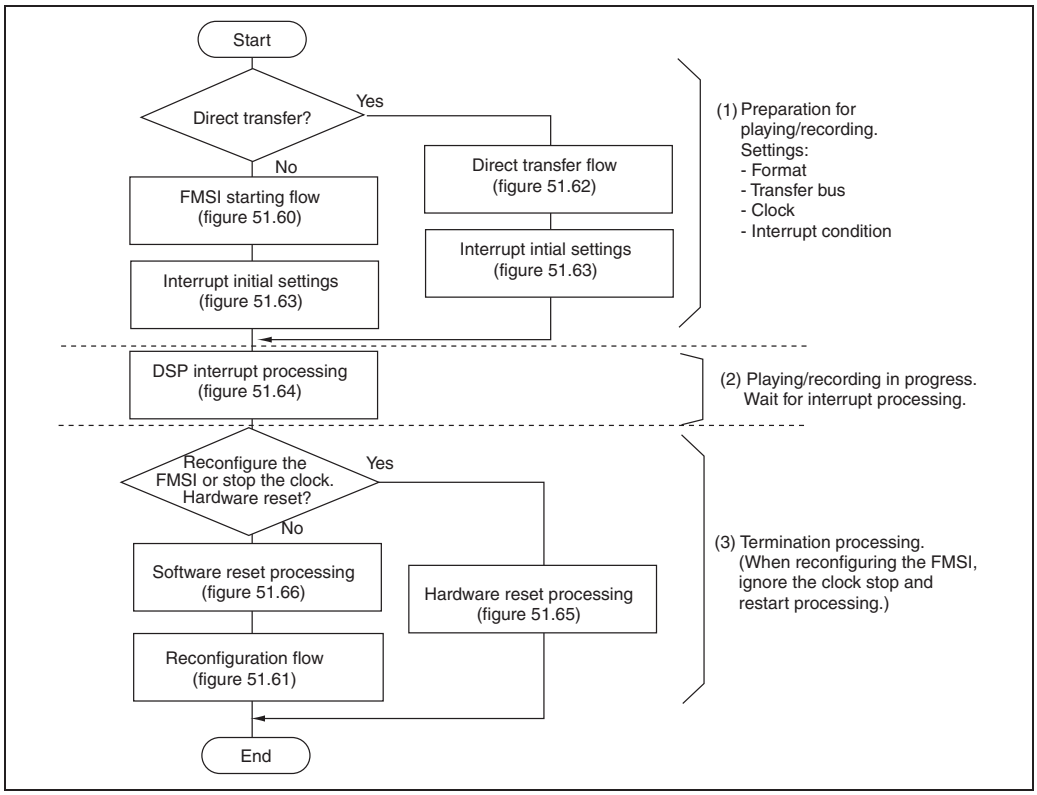


Figure 51.59 Entire FMSI Operation and Individual Processing Flows

51.22.1 Procedure for Starting the FMSI

The FMSI starting procedure is shown below. In the initial settings during FMSI starting operation, the transfer path and format and operating clock are set. When modifying the transfer format after the initial settings, perform the procedure described in section 51.22.2, Procedure for Restarting the FMSI, before modifying the format. When stopping the clocks, perform the procedure described in section 51.22.6, Procedure for Stopping and Restarting Clocks, before stopping the clocks.

A flow chart for starting the FMSI is shown in figure 51.60.

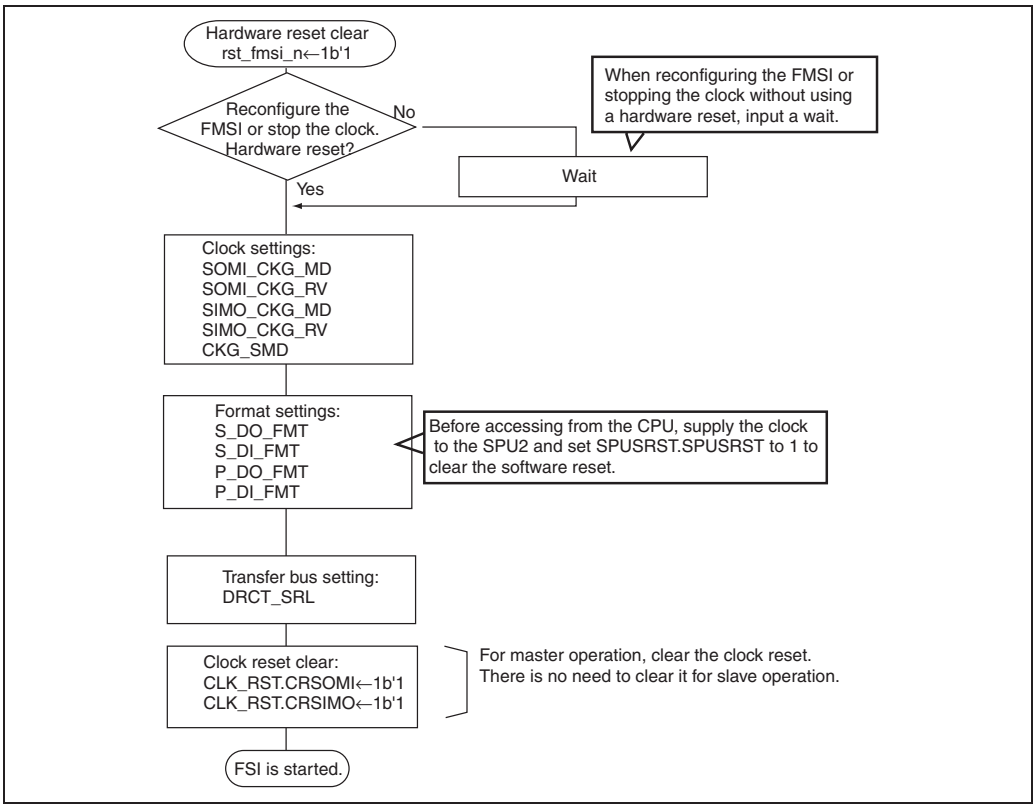
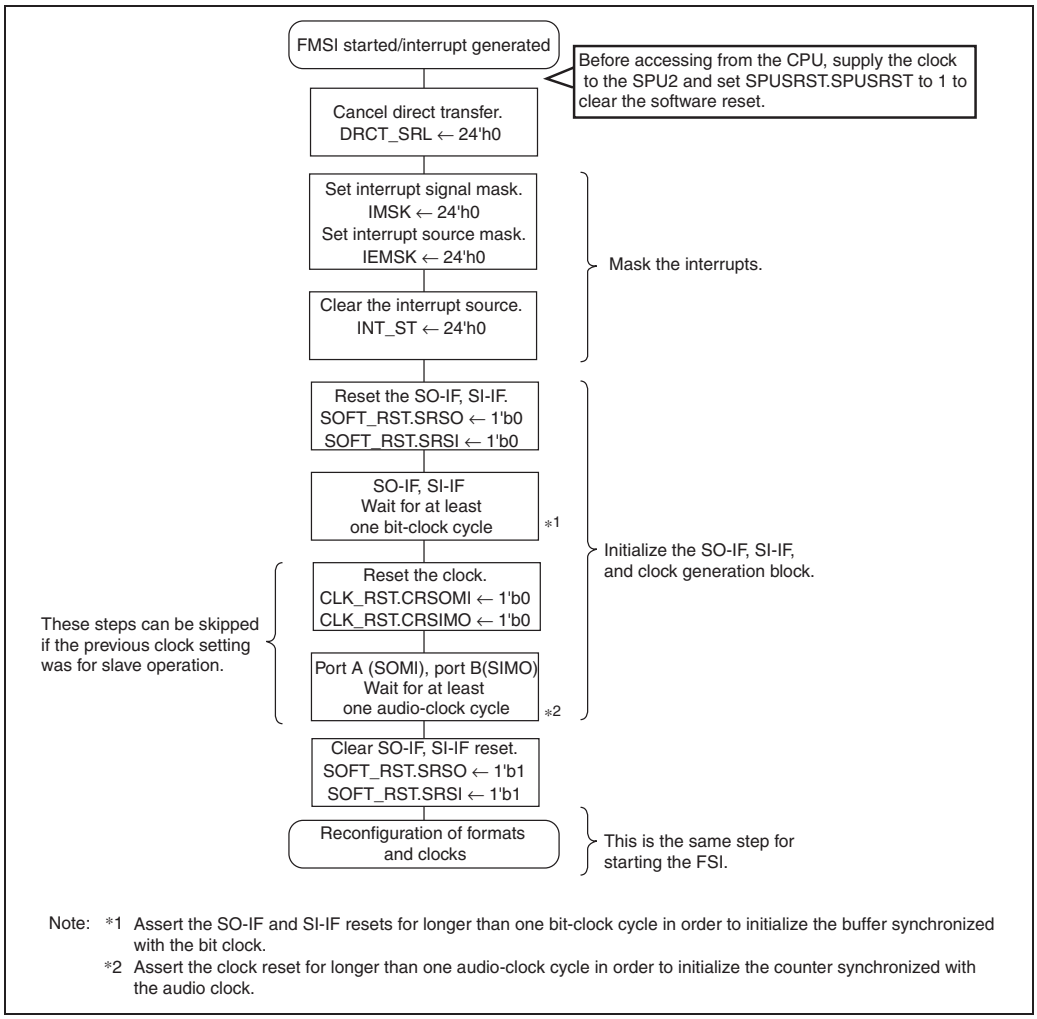


Figure 51.60 Flow for Starting FMSI

Use the steps above to start the FMSI. Paths not used for transfer should be set to the initial values. The specified audio clock is input to the serial conversion block (SO-IF, SI-IF, MI-IF, MSUO-IF).

51.22.2 Procedure for Restarting the FMSI

A flow chart for restarting the FMSI is shown below. To reconfigure transfer paths, formats, and clock setting, follow the steps in this flow. To reconfigure them using a hardware reset, this flow is not necessary. After the reset, return to the steps in section 51.22.1, Procedure for Starting the FMSI.



Note: *1 Assert the SO-IF and SI-IF resets for longer than one bit-clock cycle in order to initialize the buffer synchronized with the bit clock.
*2 Assert the clock reset for longer than one audio-clock cycle in order to initialize the counter synchronized with the audio clock.

Figure 51.61 Flow for Restarting FMSI

51.22.3 Direct Transfer Operation Flow

Figure 51.62 shows a flow for FMSI direct transfer. To prevent an underflow or overflow error from occurring in the first transfer, perform the settings in this flow.

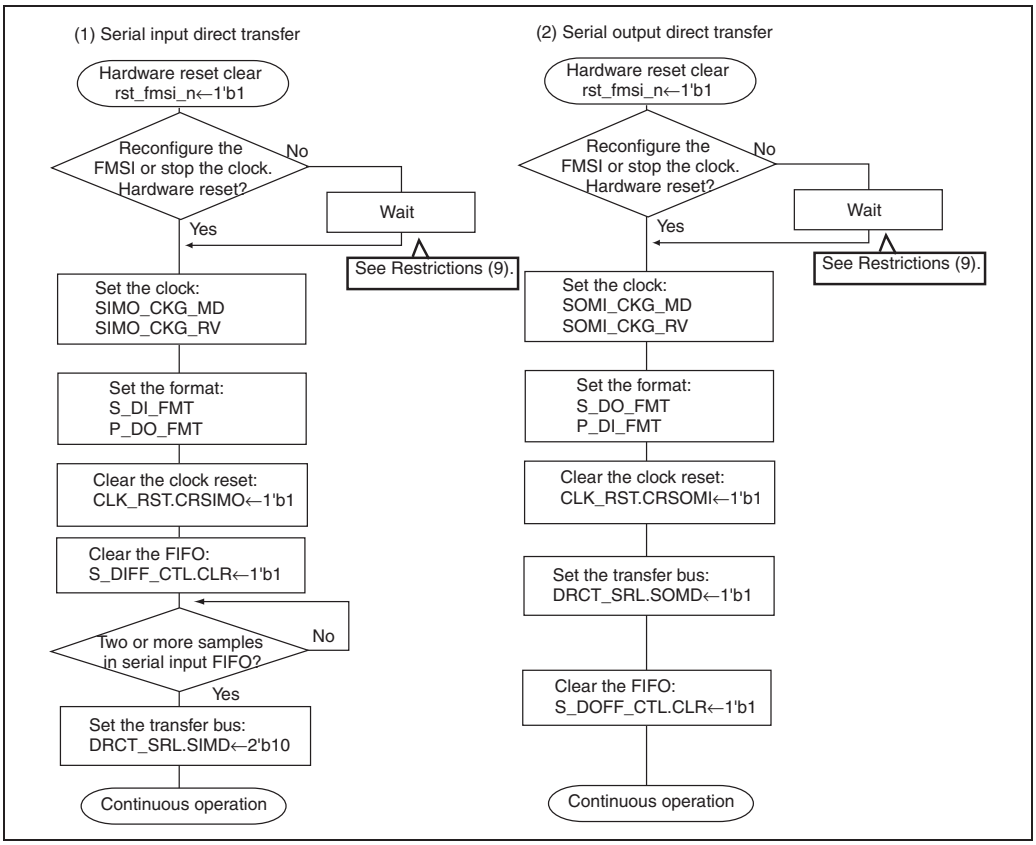


Figure 51.62 Flow for Direct Transfer

Descriptions for interrupt settings are omitted here. Add the procedure shown in section 51.22.4 before or after the FIFO clear steps. If an underflow or overflow error occurs after continuous operation, a transfer error due to unmatched sampling frequency is caused.

51.22.4 Procedure for Configuring Initial Interrupt Setting

A flow for configuring the initial interrupt setting after the FMSI starting is shown in figure 51.63.

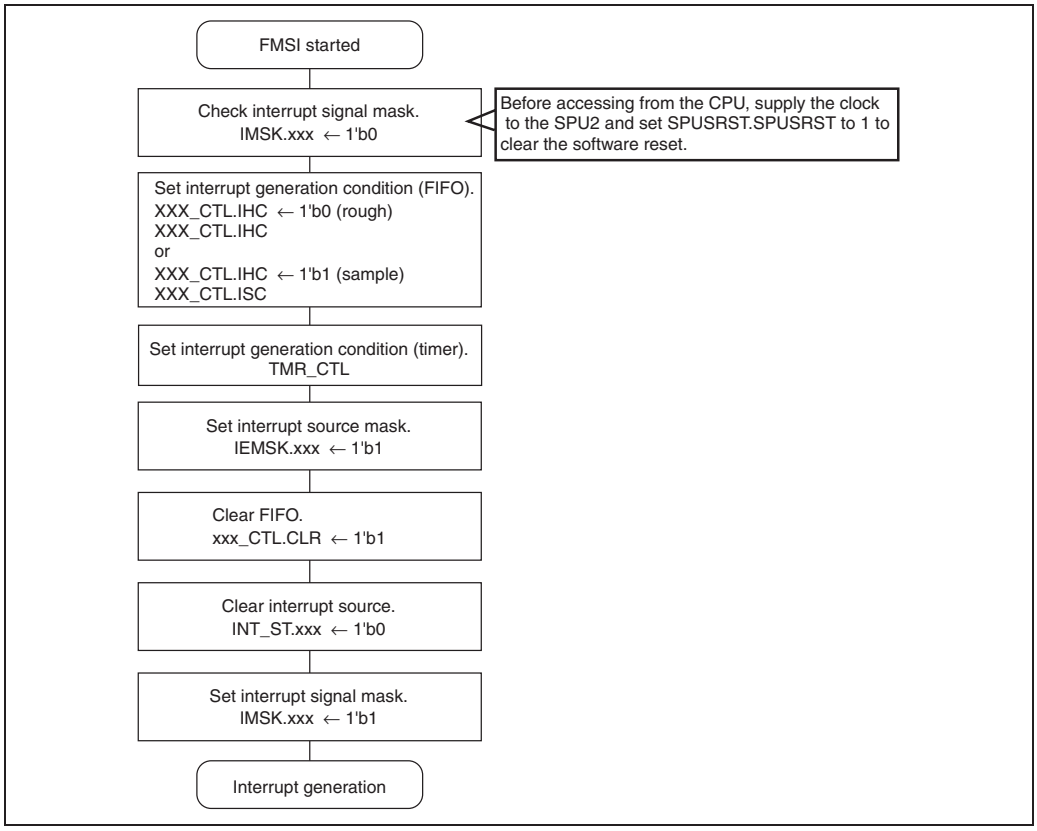


Figure 51.63 Flow for Configuring Initial Interrupt Setting

Eight interrupt conditions can be set associated with the FIFO capacity (SOFC, SIFC, and PIFC), FIFO error (SOFC, SIFC, and PIFC), and timer (TSO and TSI). "xxx" in the figure indicates any signal to be transferred.

After checking if the mask for the signal to be transferred is set, select the interrupt condition and set the interrupt source mask, then perform a FIFO clear. Clear the interrupt source that may be generated and retained before the FIFO clear, clear the signal mask.

An interrupt signal occurs based on the FIFO capacity and timer count after a FIFO clear.

51.22.5 Example of DSP Operation Flow

Figure 51.64 shows an example of the operation flow that the DSP follows to transfer audio data continuously after it accepts an interrupt.

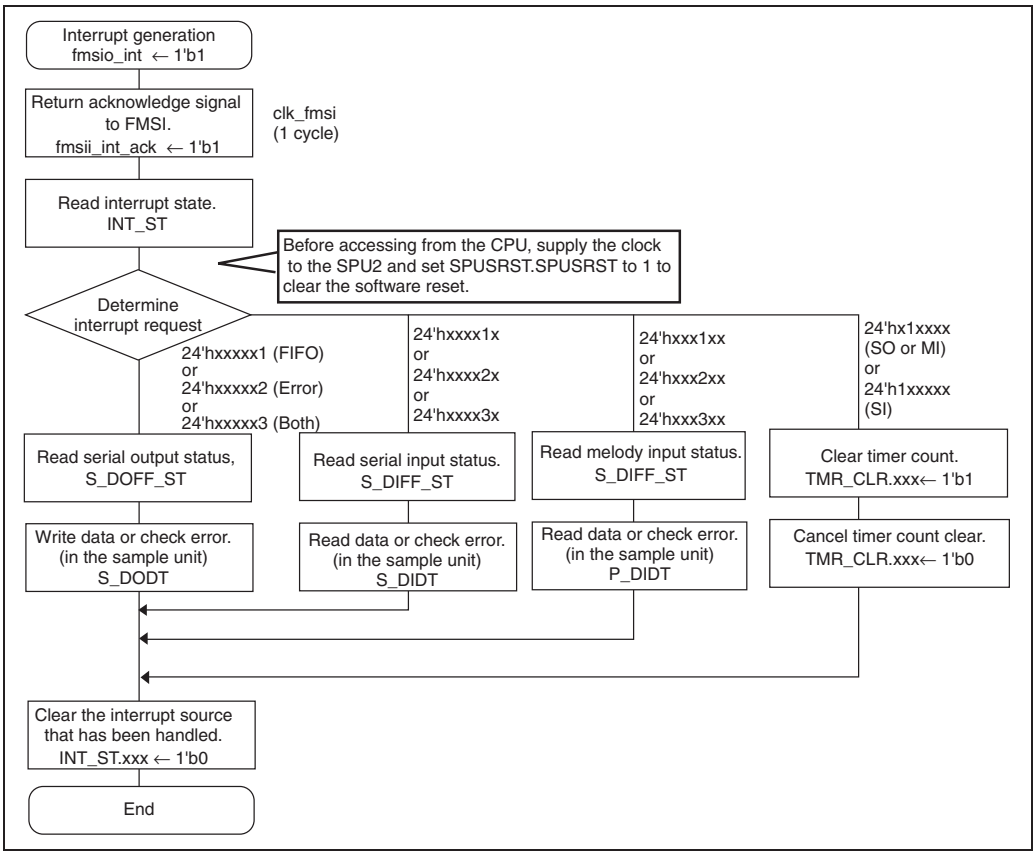


Figure 51.64 Example of DSP Operation Flow

The DSP that accepts the interrupt signal returns an acknowledge signal (fmsii_int_ack) for one cycle to the FMSI. Then, it reads the interrupt state (INT_ST) to determine which FIFO caused the interrupt and handles the interrupt adequately. When it is handled, the DSP clears the interrupt source and exits the flow. Clearing the interrupt source allows the FMSI to assert a new interrupt signal.

To handle multiple interrupt sources continuously by one interrupt, clear all the sources simultaneously at the end. After clearing the source, be sure to exit the interrupt routine and wait for fmsio_int to be set to 1.

51.22.6 Procedure for Stopping and Restarting Clocks

Figures 51.65 and 51.66 show flows for stopping and restarting clocks.

Before stopping all the FMSI clocks, input a hardware reset. After restarting the clocks, set the starting steps shown in figures 51.65 and 51.66.

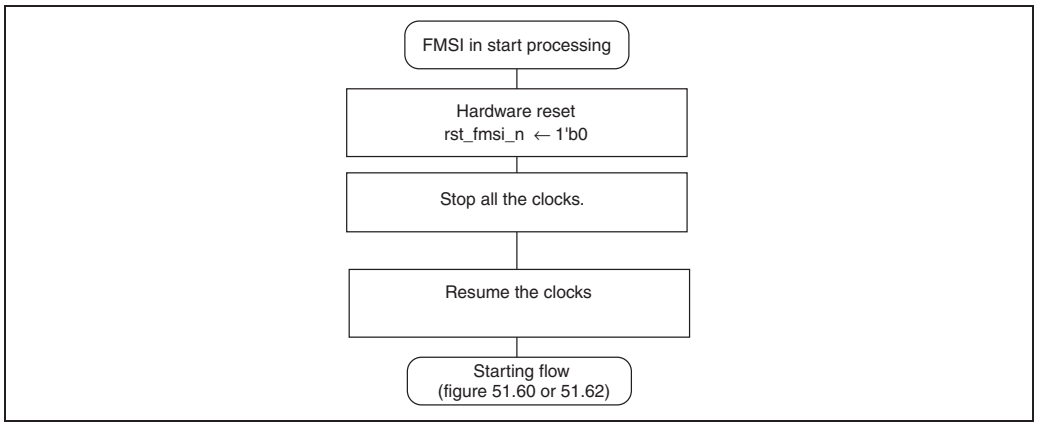


Figure 51.65 Flow for Stopping and Restarting All Clocks (Hardware Reset)

To stop specific clocks with multiple transfers in progress, perform a reset for the target transfers in the reconfiguration flow in figure 51.66 and then stop the clocks. To restart the transfer, first restart the stopped clocks and then set only the stopped transfer using the procedure in figure 51.65 or 51.66.

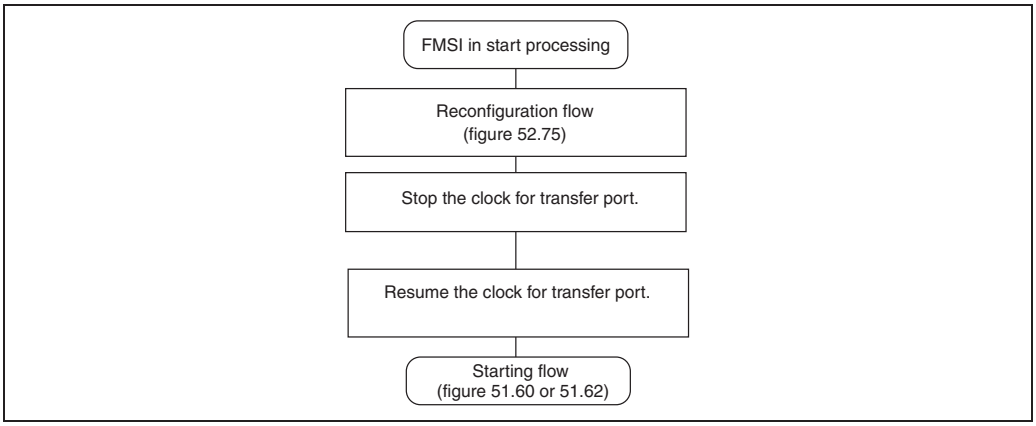


Figure 51.66 Flow for Stopping and Restarting Specific Clocks (Software Reset Only)

To stop all the clocks without using a hardware reset, perform a reset for all the ports as shown in figure 51.65.

51.23 Restrictions

Table 51.21 shows the restrictions that apply to the use of the FMSI.

Table 51.21 FMSI Usage Restrictions

	Restrictions	
No.	**Item**	**Description**
1	Direct path mode	Continuous operation can be guaranteed when the same sampling frequency is used. The same number of channels and bit width should be used between the input side and output side.
2	Port reset	When performing an internal reset of the SO-IF and SI-IF modules due to the change in formats, the reset should be longer than one cycle of the input bit-clock.
3	Clock reset	When reconfiguring the master clock, the reset should be longer than one audio-clock cycle.
4	Timer interrupt	Since one timer system is shared by the SO-IF and MI-IF, different sampling frequency operations cannot be counted at the same time.
5	Parallel IF audio clock (MI-IF)	To operate the MI-IF with an externally input audio clock (LR or MSUOsync signal for the slave), input a timing signal that has a high or low period longer than one clk_m cycle.
6	Parallel IF audio clock (MSUO-IF)	To operate the MSUO-IF with an externally input audio clock (LR signal for the slave), input a timing signal that has a high or low period longer than one clk_fmsi cycle.
7	Software reset	If FIFO is read during the entire software reset (SOFT_RST.SR) is asserted, the bus freezes. Do not perform a FIFO read (S_DIDT, P_DIDT) during a software reset.
8	Note for FMSI reconfiguration and clock stop	If the FMSI is reconfigured and clocks are stopped without using a hardware reset, the previous transfer data may be left in the MI-IF buffer. Insert a wait for 2 μs or more before performing the starting flow shown in figure 51.60.

Section 52 FSI Private Divider (FSIDIV)

The FSI Private Divider is a module that is used for generating audio clock.

52.1 Features

The functions and features are listed in table 52.1.

Table 52.1 List of FSIDIV Functions

Item	Contents	Details
Operating frequency	Source clock for master audio clock for port A	Up to 200MHz
	Source clock for master audio clock for port B	Up to 200MHz
	BUS clock	Up to 100MHz
Coverage of valid setting for divider	Frequency dividing for port A	1/2 to 1/65535
	Frequency dividing for port B	1/2 to 1/65535

Figure 52.1 shows a block diagram of the FSIDIV.

Divider for port B has the same structure and interface as divider for port A.

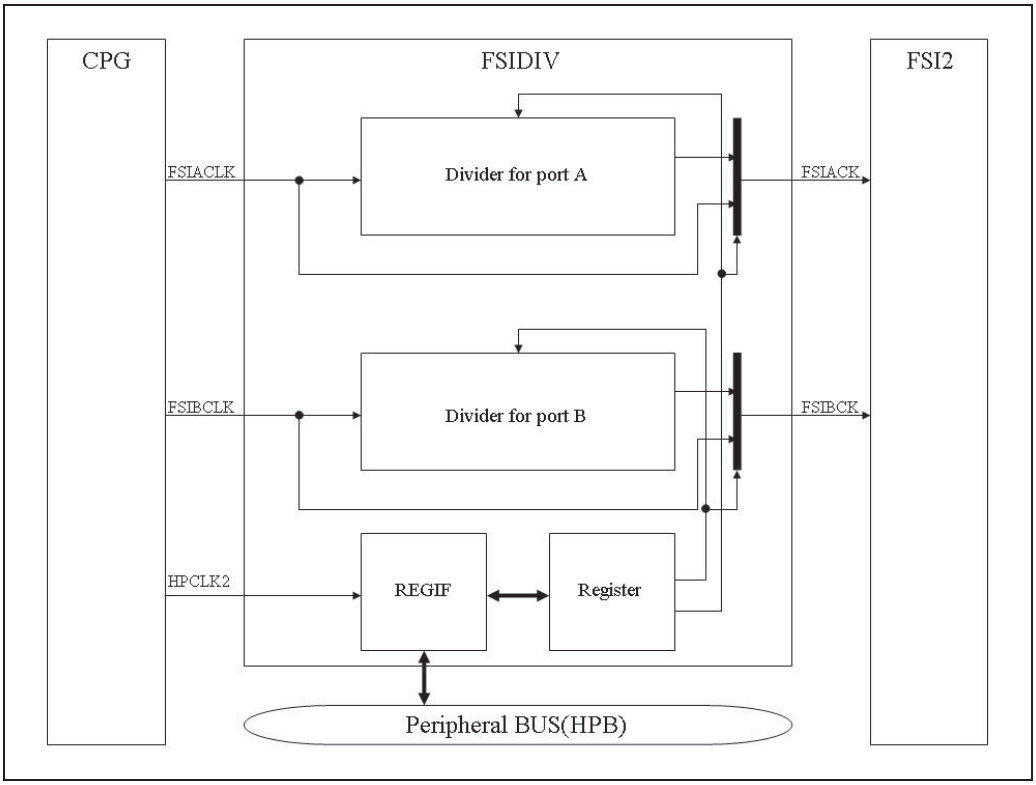


Figure 52.1 Block Diagram

52.2 Register Descriptions

Table 52.2 shows the FSIDIV register configuration.

Table 52.2 Register Configuration

Register Name	Abbreviation	R/W	initial value	Access Size	Physical Address
Port A Divider control register	FSIDIVA	R/W	H'00000000	32	H'FE1F8000
Port B Divider control register	FSIDIVB	R/W	H'00000000	32	H'FE1F8008

52.2.1 Port A Divider control register (FSIDIVA)

FSIDIVA is a 32-bit readable/writable register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PARAM_A[15:0]															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	EN	-	-	-	-	-	-	SEL	STA
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	PARAM_A	H'0000	R/W	Setting of dividing frequency 1/[PARA_A] (1/2 to 1/65535)
15 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
8	EN	0	R	Monitor of divider clock enable 0:Setting 1:Enable
7 to 2	—	All 0	R	Reserved This bit is always read as 0. The write value should always be 0.
1	SEL	0	R/W	Clock selection 0:Supply FSIACK directly 1:Supply divider clock
0	STA	0	R/W	Start bit for divider clock 0:Stop divider clock 1:Start divider clock

52.2.2 Port B Divider control register (FSIDIVB)

FSIDIVB is a 32-bit readable/writable register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PARAM_B[15:0]															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	EN	-	-	-	-	-	-	SEL	STA
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	PARAM_B	H'0000	R/W	Setting of dividing frequency 1/[PARA_B] (1/2 to 1/65535)
15 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	EN	0	R	Monitor of divider clock enable 0:Setting 1:Enable
7 to 2	—	All 0	R	Reserved This bit is always read as 0. The write value should always be 0.
1	SEL	0	R/W	Clock selection 0:Supply FSIBCK directly 1:Supply divider clock
0	STA	0	R/W	Start bit for divider clock 0:Stop divider clock 1:Start divider clock

52.3 Operation explanation

Defend the following operation, using the FSIDIV module.

(1) Set “1” to SEL bit of FSIDIVA/FSIDIVB register, using the clock of dividing frequency.

(2) Set value to PARAM_A/PARAM_B bits.

(3) Set “1” to STA bit of FSIDIVA/FSIDIVB register.

(4) Waiting until changing value of EN bit to “1”.

Defend the following operation, changing the value of dividing frequency.

(1) Set “0” to STA bit of FSIDIVA/FSIDIVB register.

(2) Set value to PARAM_A/PARAM_B bits.

(3) Set “1” to STA bit of FSIDIVA/FSIDIVB register.

(4) Waiting until changing value of EN bit to “1”.

Section 53 I²C Bus Interface (IIC)

This LSI has an I²C bus interface of five channels.

Each I²C bus interface uses only one data line (SDA) and one clock line (SCL) to transfer data, saving board and connector space.

53.1 Features

The I²C bus interface has two channels (I²C0 and I²C2) in the realtime domain, three channel (I²C1 and I²C3 and I²C4) in the system domain.

- Start and stop conditions generated automatically
- Selection of acknowledge output levels when receiving
- Automatic loading of acknowledge bit when transmitting
- Data transfer conforming to the I²C format
- Wait function

  A wait can be inserted by driving the SCL pin low after data transfer, excluding acknowledgement.

  The wait can be cleared by clearing the interrupt flag.
- I²C module corresponds to single master bus only.

  This module is always in master mode. Since the slave mode is not incorporated, operation stops with bus open during loss of arbitration in data transfer.
- Four interrupt sources
  - Data transfer enable
  - Wait state
  - Non-acknowledge detection
  - Arbitration lost (operation stops with bus open when bus conflict is detected)
- Data transfer speed
  - Standard mode (100 kHz) and high-speed mode (400 kHz). I²C1 and I²C3 and I²C4 corresponds to HighSpeed (HS) transmission (2MHz or less).
  - SCL clock can be set by clock control register setting
- Clock synchronous processing of SCL line

  A hazard (spike noise) generated in the high-count period by SCL is detected as an arbitration loss.
- DMA transfer

  I²C support transmission and reception using DMA.

Figure 53.1 shows a block diagram of the I²C bus interface.

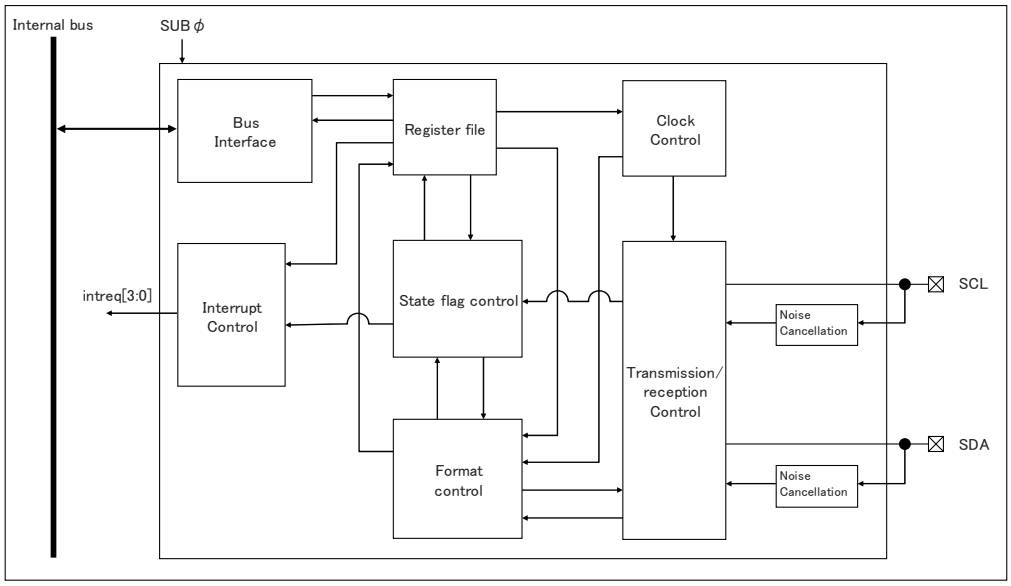


Figure 53.1 Block Diagram of I²C Bus Interface

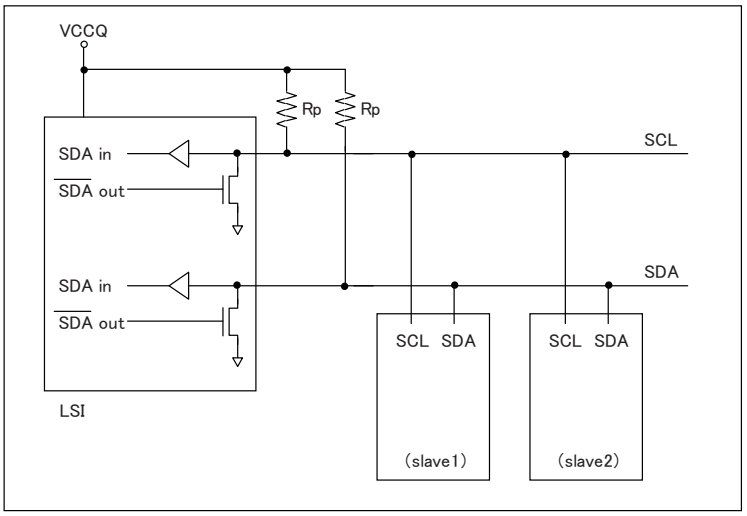


Figure 53.2 I²C Bus Interface Connections

53.2 Input/Output Pins

Table 53.1 summarizes the input/output pins used by the I²C bus interface.

Table 53.1 I²C Bus Interface Pins

Abbreviation	Function	I/O	Description
I²C_SCL0 (O/D)	I²C clock input/ output 0	I/O	I²C0 bus clock input/output pin (channel 0) Incorporates the bus drive function. The output format is the NMOS open-drain. The I/O voltage can be switched between 1.8V and 3.3V. 3.3V tolerant is supported.
I²C_SDA0 (O/D)	I²C data input/ output 0	I/O	I²C0 bus data input/output pin (channel 0) Incorporates the bus drive function. The output format is the NMOS open-drain. The I/O voltage can be switched between 1.8V and 3.3V. 3.3V tolerant is supported.
I²C_SCL1 (O/D)	I²C clock input/ output 1	I/O	I²C1 bus clock input/output pin (channel 1) Incorporates bus drive function. The output format is the NMOS open-drain. The I/O voltage can be switched between 1.8V and 3.3V. 3.3V tolerant is supported.
I²C_SDA1 (O/D)	I²C data input/ output 1	I/O	I²C1 bus data input/output pin (channel 1) Incorporates the bus drive function. The output format is the NMOS open-drain. The I/O voltage can be switched between 1.8V and 3.3V. 3.3V tolerant is supported.
I²C_SCL2 (O/D)	I²C clock input/ output 2	I/O	I²C2 bus clock input/output pin (channel 2) The output format is the NMOS open-drain or CMOS. The I/O voltage can be switched between 1.8V and 3.3V. Tolerant is non-supported.
I²C_SDA2 (O/D)	I²C data input/ output 2	I/O	I²C2 bus data input/output pin (channel 2) The output format is the NMOS open-drain or CMOS. The I/O voltage can be switched between 1.8V and 3.3V. Tolerant is non-supported.
I²C_SCL3 (O/D)	I²C clock input/ output 3	I/O	I²C3 bus clock input/output pin (channel 3) The output format is the NMOS open-drain or CMOS. The I/O voltage can be switched between 1.8V and 3.3V. Tolerant is non-supported.
I²C_SDA3 (O/D)	I²C data input/ output 3	I/O	I²C3 bus data input/output pin (channel 3) The output format is the NMOS open-drain or CMOS. The I/O voltage can be switched between 1.8V and 3.3V. Tolerant is non-supported.
I²C_SCL4 (O/D)	I²C clock input/ output 4	I/O	I²C4 bus clock input/output pin (channel 4) The output format is the NMOS open-drain or CMOS. The I/O voltage can be switched between 1.8V and 3.3V. Tolerant is non-supported.

I²C_SDA4 (O/D)	I²C data input/ output 4	I/O	I²C4 bus data input/output pin (channel 4) The output format is the NMOS open-drain or CMOS. The I/O voltage can be switched between 1.8V and 3.3V. Tolerant is non-supported.

53.3 Register Descriptions

Table 53.2 shows the register configuration of the bus interface. Table 53.3 shows the register state in each processing mode.

Table 53.2 Register Configuration of Bus Interface

Register name	Abbreviated name	R/W	Address	Access size
x is a channel identification character. I²C0:0 I²C1:1 I²C2:2 I²C3:3 I²C4:4	x is a channel identification character. I²C0:0 I²C1:1 I²C2:2 I²C3:3 I²C4:4		High order address I²C0:H'FFF2 I²C1:H'E6C2 I²C2:H'FFF3 I²C3:H'E6D2 I²C4:H'E6D3	
I²C bus data register x	ICDRx	R/W	H'XXXX 0000	8
I²C birth control register x	ICCRx	R/W	H'XXXX 0004	8
I²C bus status register x	ICSRx	R/W	H'XXXX 0008	8
I²C interruption control register x	ICICx	R/W	H'XXXX 000C	8
I²C clock control register low x	ICCLx	R/W	H'XXXX 0010	8
I²C clock control register high x	ICCHx	R/W	H'XXXX 0014	8
I²C transformer register x	ICTRx	R	H'XXXX 0018	8
I²C receipt register x	ICRRx	R	H'XXXX 001C	8
I²C transformer monitor x	ICTAx	R	H'XXXX 0020	8
I²C transformer buffer monitor x	ICTBx	R	H'XXXX 0024	8
I²C transformer control register x	ICTCx	R/W	H'XXXX 0028	8
I²C transformer control status monitor x	ICTDx	R/W	H'XXXX 002C	8
I²C shift register x	ICSFx	R	H'XXXX 0030	8
I²C Hs Clock control register low x*1	ICHLx	R	H'XXXX 0034	8
I²C Hs Clock control register high x*1	ICHHx	R	H'XXXX 0038	8
I²C Hs master code x*1	ICHMCODx	R	H'XXXX 003C	8
I²C Option enabling register x*1	ICVCONx	R	H'XXXX 006C	8
I²C automatic transmission interruption mask register x*1	ICIMSKx	R/W	H'XXXX 0050	8
I²C automatic transmission interruption flag register x*1	ICINTx	R	H'XXXX 0054	8
I²C automatic transmission processing enabling register x*1	ICACEx	R/W	H'XXXX 0058	8
I²C automatic transmission timer control register 1x *1	ICTMC1x	R/W	H'XXXX 0060	8

I²C automatic transmission timer control register 2x *1	ICTMC2x	R/W	H'XXXX 0064	8
I²C automatic transmission wait control register x*1	ICTMCWx	R/W	H'XXXX 0068	8
I²C automatic transmission transformer start register x*1	ICASTARTx	R/W	H'XXXX 0070	8
I²C automatic transmission transformer control register x*1	ICATFRx	R/W	H'XXXX 0080	8
I²C automatic transmission transformer time register 1x *1	ICATSET1x	R/W	H'XXXX 0084	8
I²C automatic transmission transformer time register 2x *1	ICATSET2x	R/W	H'XXXX 0088	8
I²C automatic transmission receipt time register 1x *1	ICARSET1x	R/W	H'XXXX 008C	8
I²C automatic transmission receipt time register 2x *1	ICARSET2x	R/W	H'XXXX 0090	8
I²C automatic transmission transformer data 00x *1	ICATD00x	R/W	H'XXXX 0100	8
I²C automatic transmission transformer data 01x *1	ICATD01x	R/W	H'XXXX 0104	8
I²C automatic transmission transformer data 02x *1	ICATD02x	R/W	H'XXXX 0108	8
I²C automatic transmission transformer data 03x *1	ICATD03x	R/W	H'XXXX 010C	8
I²C automatic transmission transformer data 04x *1	ICATD04x	R/W	H'XXXX 0110	8
I²C automatic transmission transformer data 05x *1	ICATD05x	R/W	H'XXXX 0114	8
I²C automatic transmission transformer data 06x *1	ICATD06x	R/W	H'XXXX 0118	8
I²C automatic transmission transformer data 07x *1	ICATD07x	R/W	H'XXXX 011C	8
I²C automatic transmission transformer data 08x *1	ICATD08x	R/W	H'XXXX 0120	8
I²C automatic transmission transformer data 09x *1	ICATD09x	R/W	H'XXXX 0124	8
I²C automatic transmission transformer data 10x *1	ICATD10x	R/W	H'XXXX 0200	8

I²C automatic transmission transformer data 11x *1	ICATD11x	R/W	H'XXXX 0204	8
I²C automatic transmission transformer data 12x *1	ICATD12x	R/W	H'XXXX 0208	8
I²C automatic transmission transformer data 13x *1	ICATD13x	R/W	H'XXXX 020C	8
I²C automatic transmission transformer data 14x *1	ICATD14x	R/W	H'XXXX 0210	8
I²C automatic transmission transformer data 15x *1	ICATD15x	R/W	H'XXXX 0214	8
I²C automatic transmission transformer data 16x *1	ICATD16x	R/W	H'XXXX 0218	8
I²C automatic transmission transformer data 17x *1	ICATD17x	R/W	H'XXXX 021C	8
I²C automatic transmission transformer data 18x *1	ICATD18x	R/W	H'XXXX 0220	8
I²C automatic transmission transformer data 19x *1	ICATD19x	R/W	H'XXXX 0224	8
I²C automatic transmission receipt data 00x *1	ICARD00x	R	H'XXXX 0300	8
I²C automatic transmission receipt data 01x *1	ICARD01x	R	H'XXXX 0304	8
I²C automatic transmission receipt data 02x *1	ICARD02x	R	H'XXXX 0308	8
I²C automatic transmission receipt data 03x *1	ICARD03x	R	H'XXXX 030C	8
I²C automatic transmission receipt data 04x *1	ICARD04x	R	H'XXXX 0310	8
I²C automatic transmission receipt data 05x *1	ICARD05x	R	H'XXXX 0314	8
I²C automatic transmission receipt data 06x *1	ICARD06x	R	H'XXXX 0318	8
I²C automatic transmission receipt data 07x *1	ICARD07x	R	H'XXXX 031C	8
I²C automatic transmission receipt data 08x *1	ICARD08x	R	H'XXXX 0320	8
I²C automatic transmission receipt data 09x *1	ICARD09x	R	H'XXXX 0324	8

I²C automatic transmission receipt data 10x *1	ICARD10x	R	H'XXXX 0400	8
I²C automatic transmission receipt data 11x *1	ICARD11x	R	H'XXXX 0404	8
I²C automatic transmission receipt data 12x *1	ICARD12x	R	H'XXXX 0408	8
I²C automatic transmission receipt data 13x *1	ICARD13x	R	H'XXXX 040C	8
I²C automatic transmission receipt data 14x *1	ICARD14x	R	H'XXXX 0410	8
I²C automatic transmission receipt data 15x *1	ICARD15x	R	H'XXXX 0414	8
I²C automatic transmission receipt data 16x *1	ICARD16x	R	H'XXXX 0418	8
I²C automatic transmission receipt data 17x *1	ICARD17x	R	H'XXXX 041C	8
I²C automatic transmission receipt data 18x *1	ICARD18x	R	H'XXXX 0420	8
I²C automatic transmission receipt data 19x *1	ICARD19x	R	H'XXXX 0424	8

*1 Only I²C2 and I²C3 and I²C4 are effective. Please do not access in I²C0 and I²C1.

The automatic transmission assumes the end of communication by interruption, and error detection, please do not perform principle polling during automatic transmission.

Table 53.3 Register State in Each Processing Mode

Register abbreviated name	Reset	Module Standby
ICDRx	Initialization	Maintenance
ICCRx	Initialization	Maintenance
ICSRx	Initialization	Maintenance
ICICx	Initialization	Maintenance
ICCLx	Initialization	Maintenance
ICCHx	Initialization	Maintenance
ICTRx	Initialization	Maintenance
ICRRx	Initialization	Maintenance
ICTAx	Initialization	Maintenance
ICTBx	Initialization	Maintenance
ICTCx	Initialization	Maintenance
ICTDx	Initialization	Maintenance
ICSFx	Initialization	Maintenance
ICHLx	Initialization	Maintenance
ICHHx	Initialization	Maintenance
ICHMCODx	Initialization	Maintenance
ICVCONx	Initialization	Maintenance
ICIMSKx	Initialization	Maintenance
ICINTx	Initialization	Maintenance
ICACEx	Initialization	Maintenance
ICTMC1x	Initialization	Maintenance
ICTMC2x	Initialization	Maintenance
ICTMCWx	Initialization	Maintenance
ICASTARTx	Initialization	Maintenance
ICATFRx	Initialization	Maintenance
ICATSET1x	Initialization	Maintenance
ICATSET2x	Initialization	Maintenance
ICARSET1x	Initialization	Maintenance
ICARSET2x	Initialization	Maintenance
ICATD00x	Initialization	Maintenance
ICATD01x	Initialization	Maintenance

ICATD02x	Initialization	Maintenance
ICATD03x	Initialization	Maintenance
ICATD04x	Initialization	Maintenance
ICATD05x	Initialization	Maintenance
ICATD06x	Initialization	Maintenance
ICATD07x	Initialization	Maintenance
ICATD08x	Initialization	Maintenance
ICATD09x	Initialization	Maintenance
ICATD10x	Initialization	Maintenance
ICATD11x	Initialization	Maintenance
ICATD12x	Initialization	Maintenance
ICATD13x	Initialization	Maintenance
ICATD14x	Initialization	Maintenance
ICATD15x	Initialization	Maintenance
ICATD16x	Initialization	Maintenance
ICATD17x	Initialization	Maintenance
ICATD18x	Initialization	Maintenance
ICATD19x	Initialization	Maintenance
ICARD00x	Initialization	Maintenance
ICARD01x	Initialization	Maintenance
ICARD02x	Initialization	Maintenance
ICARD03x	Initialization	Maintenance
ICARD04x	Initialization	Maintenance
ICARD05x	Initialization	Maintenance
ICARD06x	Initialization	Maintenance
ICARD07x	Initialization	Maintenance
ICARD08x	Initialization	Maintenance
ICARD09x	Initialization	Maintenance
ICARD10x	Initialization	Maintenance
ICARD11x	Initialization	Maintenance
ICARD12x	Initialization	Maintenance
ICARD13x	Initialization	Maintenance
ICARD14x	Initialization	Maintenance
ICARD15x	Initialization	Maintenance
ICARD16x	Initialization	Maintenance

ICARD17x	Initialization	Maintenance
ICARD18x	Initialization	Maintenance
ICARD19x	Initialization	Maintenance

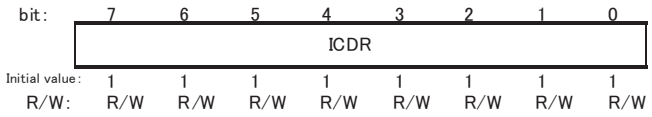
53.3.1 I²C Bus Data Registers (ICDR)

ICDR are 8-bit readable/writable registers that are used as a transmit data register when transmitting, and a receive data register when receiving.

These registers can be written to when the DTE bit in I²C bus status register ICSR is 1 in transmitting.

Receive data of ICDR is valid when the DTE bit in ICSR is 1 in receiving.

The read value of ICDR is H'FF after reset.

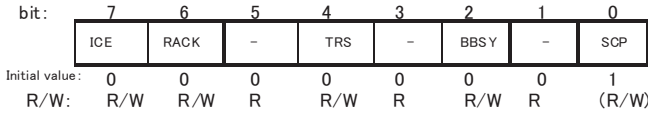


53.3.2 I²C Bus Control Registers (ICCR)

ICCR are 8-bit readable/writable registers that enable or disable the I²C bus interface, and transmission or reception, confirm the I²C bus interface bus status, and issue start/stop conditions.

Table 53.4 ICCR Settings

Issue Condition	When Transmitting	When Receiving
Start condition	H'94	—
Retransmission condition	H'94	H'D4 Changes from reception to transmission
Stop condition	H'90	H'C0
Changes from transmission to reception	H'81	—



bit:	7	6	5	4	3	2	1	0
	ICE	RACK	–	TRS	–	BBSY	–	SCP
Initial value:	0	0	0	0	0	0	0	1
R/W:	R/W	R/W	R	R/W	R	R/W	R	(R/W)

Bit	Bit Name	Initial Value	R/W	Description
7	ICE	0	R/W	I²C Bus Interface Enable Selects whether or not the I²C bus interface is to be used. When ICE is set to 1, transfer operations and access to each register are enabled. When ICE is cleared to 0 during data transmission, ICE releases buses and is forcibly terminated, then all registers in the I²C module are initialized. (See section 53.5, Usage Notes.) When ICE is cleared to 0 after data transmission, all registers in the I²C module are initialized. When the ICCR is updated while this module is being operated, the ICE bit must be set to 1. 0: I²C module disabled and forcibly terminated when 0 is written in data transmission. I²C module internal registers are all initialized. 1: I²C bus interface module enabled for transfer operations
6	RACK	0	R/W	Receive Acknowledge The RACK bit is for storing acknowledge data that is output to the transmission device when the I²C module is receiving data. After data is received from the transmitting device, acknowledge data that has been set to this bit is sent. 0: In receive mode, 0 is output to SDA at acknowledge output timing. 1: In receive mode, 1 is output to SDA at acknowledge output timing.
5	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
4	TRS	0	R/W	Transmit/Receive Select The TRS bit selects whether the I²C bus interface operates in master transmitter or master receiver mode. Although the setting of the TRS bit is modifiable during transfer, the actual change of operating mode is deferred until transfer of the frame containing the acknowledge bit is completed. On completion of this transfer, the changeover is made. 0: Master receive mode Writing of 0 to the bit (if this is done during data transfer, the operating mode is only changed after one frame has been transferred) 1: Master transmit mode Writing of 1 (at the time of a retransmission/stop condition; at this time, the operating mode is changed after a retransmission or stop condition has been generated subsequent to data transfer.)
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
2	BBSY	0	R/W	Bus Busy The BBSY flag is used to issue start and stop conditions. To issue a start condition, write 1 in BBSY and 0 in SCP. A retransmit start condition is issued in the same way. To issue a stop condition, write 0 in BBSY and 0 in SCP. Since this module is always in master mode, a bus state is not detected by the BBSY bit. When a start condition is issued from other masters, it is detected that arbitration is lost and operation is stopped. 0: A stop condition is issued (the SCP bit is also used). 1: Start and retransmit conditions are issued (the SCP bit is also used).
1	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
0	SCP	1	(R/W)*	Start Condition/Stop Condition Prohibit Controls the issuing of start and stop conditions. To issue a start condition, write 1 in BBSY and 0 in SCP. A retransmit start condition is issued in the same way. To issue a stop condition, write 0 in BBSY and 0 in SCP. This bit is always read as 1. If 1 is written, the data is not stored. 0: Writing 0 issues a start or stop condition, in combination with the BBSY flag 1: Reading always returns a value of 1. Writing is ignored.

Note: * For the SCP bit, only writing 0 is valid. Always read as 1.

53.3.3 I²C Bus Status Registers (ICSR)

ICSR are 8-bit readable/writable registers that perform interrupt request.

bit:	7	6	5	4	3	2	1	0
	SCLM	SDAM	–	BUSY	AL	TACK	WAIT	DTE
Initial value:	1	1	0	0	0	0	0	0
R/W:	R	R	R	R	R/(W)*	R/(W)*	R/(W)*	R

Bit	Bit Name	Initial Value	R/W	Description
7	SCLM	1	R	SCL Monitor Stores data in which the SCL state is sampled at SUBϕ. 0: Indicates SCL is 0. 1: Indicates SCL is 1.
6	SDAM	1	R	SDA Monitor Stores data in which the SDA state is sampled at SUBϕ. 0: Indicates SDA is 0. 1: Indicates SDA is 1.
5	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
4	BUSY	0	R	I²C Transmit State Bit Indicates the I²C state. After the start condition is generated, I²C is in the transmit state and this bit is set to 1. After the stop condition is generated, I²C is in the non-transmit state and this bit is cleared to 0. When arbitration is lost, the SDA line is open. The SCL clock line outputs clocks until the acknowledge end of the frame and releases buses. The BUSY flag is set to 1 until acknowledge end, and is cleared to 0 at acknowledge end. 0: • In I²C non-transmit state after stop condition is generated. • At acknowledge end after arbitration is lost 1: In I²C transmit state after start condition is generated

Bit	Bit Name	Initial Value	R/W	Description
3	AL	0	R/(W)*	Arbitration Lost This flag indicates that arbitration was lost. The I²C bus interface monitors the SDA. If the I²C bus interface detects data differing from the data it sent, it sets AL to 1 to indicate that the bus has been conflicted. AL is reset by writing 0 to this bit, write access to ICDR in transmit mode, or read access to ICDR in receive mode when DTE is 1. When arbitration lost is detected in data transfer, the SDA line is open. The SCL clock line outputs clocks until the acknowledge end of the frame and releases buses. The AL bit does not depend on the ALE bit in ICIC, and is always updated. When the ALE bit in ICIC is 0, an arbitration lost interrupt request is not issued to the interrupt controller. When other masters issue the start condition, arbitration lost is detected and operation is stopped. 0: Bus arbitration won • When ICDR data is written (transmit mode) or read (receive mode) • When 0 is written in AL after reading AL = 1 1: Arbitration lost • If receive data changes when SCL clocks count at a high level in master receive mode • If the SCL line is in a low level when SCL clocks count at a high level • If a start condition is detected before this module issues a start condition • If the monitored external SDA and data output from this module disagree

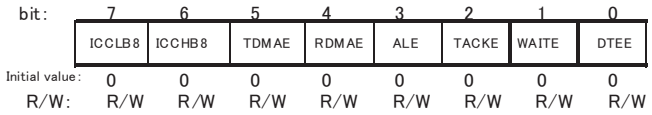
Bit	Bit Name	Initial Value	R/W	Description
2	TACK	0	R/(W)*	Transmit Acknowledge Bit Stores acknowledge data issued from the receiving device in transmit mode. The non-acknowledge interrupt state can be cleared by clearing the TACK bit to 0. In transmit mode, after the receiving device receives data, it returns acknowledge data, and this data is loaded into TACK. This bit is always 0 when the TACKE bit in ICIC is 0. 0: • Transmit mode: Indicates that the receiving device has acknowledged the data (signal is 0) • When 0 is written, indicates that the receiving device has acknowledged the data (signal is 0) 1: Transmit mode: Indicates that the receiving device has not acknowledged the data (signal is 1)
1	WAIT	0	R/(W)*	Wait Indicates that a wait state follows the transmission of data other than the acknowledge bit. When the value of the WAITE bit in ICIC is 1, a data transfer that is not followed by the acknowledge bit leads to SCL being driven to the low level and the initiation of a state of waiting. At this time, the WAIT bit is automatically set to 1 and a WAIT interrupt is generated. Release from the state of waiting is accomplished by clearing the WAIT bit (to 0). WAIT is always 0 when WAITE in ICIC is 0. 0: Normal state 1: At wait

Bit	Bit Name	Initial Value	R/W	Description
0	DTE	0	R	Data Transmit Enable Indicates the transmit state between ICDR and internal transmit/receive buffer. This bit is read only, and automatically set or cleared. 0: • When reset • When data is written to ICDR in transmit mode (TRS = 1) • When data is read from ICDR in receive mode (TRS = 0) • When the TRS bit is changed • When the retransmit/stop conditions are written to the BBSY and SCP bits in ICCR 1: • When the start/retransmit conditions are generated • When transmit data is sent to the transmit buffer from ICDR in transmit mode (TRS = 1) • When receive data is sent to ICDR in receive mode (TRS = 0)

Note: * Only 0 can be written, for flag clearing.

53.3.4 I²C Interrupt Control Registers (ICIC)

ICIC are 8-bit registers that enable/disable an interrupt request.



bit:	7	6	5	4	3	2	1	0
	ICCLB8	ICCHB8	TDMAE	RDMAE	ALE	TACKE	WAITE	DTEE
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

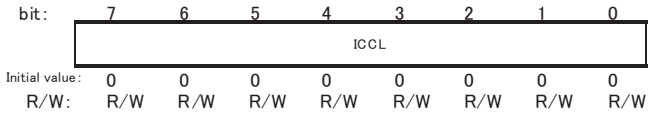
Bit	Bit Name	Initial Value	R/W	Description
7	ICCLB8	0	R/W	I²C Clock Control Low Bit 8 Sets low-level time of SCL, when the period of ICCL is set to H'100 to H'1FF in SUBϕ. Table 53.5 shows transfer rate settings.
6	ICCHB8	0	R/W	I²C Clock Control High Bit 8 Sets high-level time of SCL, when the period of ICCH is set to H'100 to H'1FF in SUBϕ. Table 53.5 shows transfer rate settings.
5	TDMAE	0	R/W1	Transmit Data DMA Transfer Request Enable1 When DTEE is 1, the TDMAE decides whether an interrupt at data transmission (TRS = 1) is used for CPU or as a DMA transfer request. When using DMA by automatic transmission, a setup of this bit is unnecessary. 0: Uses TDMAE as a CPU interrupt. 1: Uses TDMAE as a DMA transfer request to DMAC.
4	RDMAE	0	R/W1	Receive Data DMA Transfer Request Enable1 When DTEE is 1, the RDMAE decides whether an interrupt at data transmission (TRS = 0) is used for CPU or as a DMA transfer request. When using DMA by automatic transmission, a setup of this bit is unnecessary. 0: Uses RDMAE as a CPU interrupt. 1: Uses RDMAE as a DMA transfer request to DMAC

Bit	Bit Name	Initial Value	R/W	Description
3	ALE	0	R/W	Arbitration Lost Interrupt Enables/disables an arbitration lost interrupt request. An arbitration lost interrupt occurs if arbitration lost occurs when ALE is 1. At this time, the AL bit in ICSR is set to 1. With AL set to 1, do not clear ALE to 0. 0: Interrupt disabled 1: Arbitration lost interrupt
2	TACKE	0	R/W	Non-acknowledge Detection Interrupt Enables/disables a non-acknowledge detection interrupt request. A non-acknowledge interrupt occurs if non-acknowledge is received when TACKE is 1. At this time, the TACK bit in ICSR is set to 1. With TACK set to 1, do not clear TACKE to 0. 0: Interrupt disabled 1: Non-acknowledge detection interrupt
1	WAITE	0	R/W	Wait Interrupt Enables/disables a wait interrupt request. Indicates that a wait state follows the transmission of data other than the acknowledge bit by driving SCL to the low level when WAITE is 1. At this time, a WAIT interrupt occurs, and the WAIT bit in ICSR is set to 1. With WAIT in ICSR set to 1, do not clear WAITE to 0. 0: Interrupt disabled 1: Wait interrupt
0	DTEE	0	R/W	Data Transmit Enable Interrupt Enables/disables a data transmit enable interrupt request. An interrupt request is issued if the DTE bit in ICSR is set to 1 when DTEE is 1. 0: Interrupt disabled 1: Data transmit enable interrupt

53.3.5 I²C Clock Control Registers Low (ICCL)

ICCL are 8-bit readable/writable registers that can set low-level time of SCL.

ICCL is initialized to H'00 by a reset.

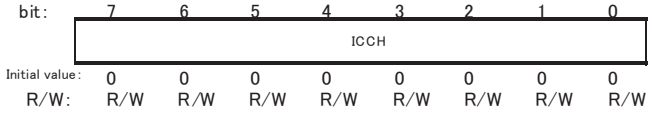


Note: Settings of H'01 to H'09 are prohibited.
No SCL clock is generated for ICIC[7]=B'0 and ICCL= H'00 and H'FF or ICCH = H'00 and H'FF.

53.3.6 I²C Clock Control Registers High (ICCH)

ICCH are 8-bit readable/writable registers that can set high-level-time of SCL.

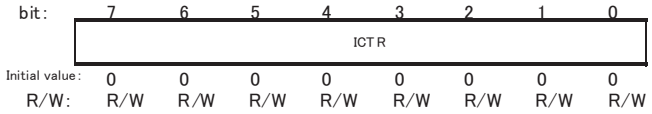
ICCH is initialized to H'00 by a reset.



Note: Settings of H'01 to H'09 are prohibited.
No SCL clock is generated for ICIC[7]=B'0 and ICCL= H'00 and H'FF or ICCH = H'00 and H'FF.

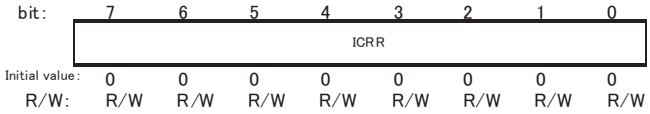
53.3.7 I²C Transmit Registers (ICTR)

ICTR are 8-bit registers that monitor transmit data of the I²C bus interface.



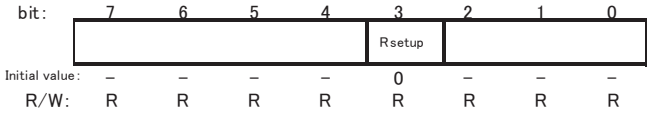
53.3.8 I²C Receive Registers (ICRR)

ICRR are 8-bit registers that monitor receive data for the I²C bus interface.



53.3.9 I²C Transmit Monitor Registers (ICTA)

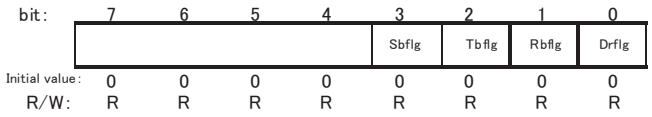
ICTA are 8-bit registers that monitor the retransmission condition setting status of the I²C bus interface.



Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	—	R	Reserved Writing to this bit is prohibited.
3	Rsetup	0	R	Retransmission Condition Setup Monitor The value of 1 remains to be set in this bit for the period from the setting of a retransmission condition (ICCR = H'94) during communication until the generation of the retransmission condition.
2 to 0	—	—	R	Reserved Writing to this bit is prohibited.

53.3.10 I²CTransmit Buffer Monitor Registers (ICTB)

ICTB are 8-bit registers that monitor the communication status of the I²C bus interface.



Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	—	R	Reserved
3	Sbflg	0	R	ICSF Buffer Flag 0: ICSF has no transmit data. 1: ICSF has transmit data.
2	Tbflg	0	R	ICTR Buffer Flag 0: ICTR has no transmit data. 1: ICTR has transmit data.
1	Rbflg	0	R	ICRR Buffer Flag 0: ICRR has no transmit data. 1: ICRR has transmit data.
0	Drflg	0	R	ICDR Buffer Flag 0: ICDR has no transmit data. 1: ICDR has transmit data.

53.3.11 I²C Transmit Control Registers (ICTC)

ICTC are 8-bit registers that select pins to be used for I²C communication with the functions of SDA delay adjustment, SCL synchronization, and pin selection.

ICTC is initialized to H'00 by a reset.

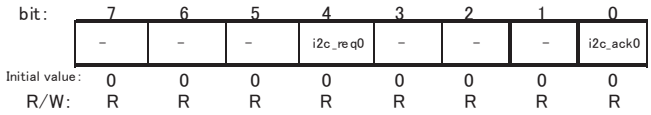
bit:	7	6	5	4	3	2	1	0
	sda_dly4	sda_dly3	sda_dly2	sda_dly1	sda_dly0	sync_en	–	–
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
7 to 3	sda_dly[4:0]	00000	R/W	SDA Data Delay Select These bits set the SDA data output delay from the SCL. 00000: No SDA data delay (recommended) 00001: SDA data is delayed by one SUBϕ cycle. 00010: SDA data is delayed by two SUBϕ cycles. . . . . 11110: SDA data is delayed by 30 SUBϕ cycles. 11111: SDA data is delayed by 31 SUBϕ cycles. When the SDA data output is delayed, the AC specifications of the I²C bus interface may not be satisfied. Therefore, setting these bits to 00000 is recommended.
2	sync_en	0	R/W	SCL Synchronization Select Sets whether the SCL line synchronizing function is provided or not. 0: SCL line synchronization is provided (recommended). 1: SCL line synchronization is not provided. When this bit is set to 1, the AC specifications of the I²C bus interface may not be satisfied. Therefore, setting this bit to 0 is recommended.

Bit	Bit Name	Initial Value	R/W	Description
1 to 0	—	—	R	Reserved

53.3.12 I²C Transmit Control Status Monitor Registers (ICTD)

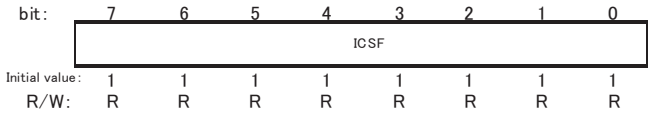
ICTD are 8-bit registers that monitor communication status of the I²C bus interface.



Bit	Bit Name	Initial Value	R/W	Description
7 to 5	—	0	R	Reserved
• 4	• I²C_req0	• 0	R/W	I²C Communication Request 0 • Communication request to channel-0 pins in ICTD0 • Communication request to channel-1 pins in ICTD1 0: No communication request 1: Communication request underway
3 to 1	—	0	R	Reserved
0	I²C_ack0	0	R/W	I²C Communication Status 0 Communication acknowledge to channel-0 pins in ICTD0 Communication acknowledge to channel-1 pins in ICTD1 0: No communication 1: Communication acknowledge underway

53.3.13 I²C Shift Registers (ICSF)

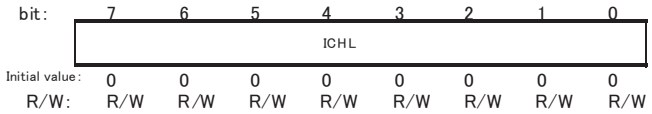
ICSF are 8-bit registers that monitor data being transmitted for the I²C bus interface.



53.3.14 I²C HighSpeed SCL register low (ICHL)

ICHL are 8-bit readable/writable registers that can set low-level time of SCL at the time of HS transmission.

ICHL is initialized by H'00 at the time of reset.

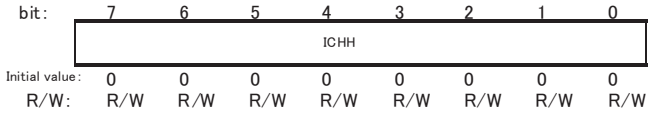


[Note] A setup of H'01 to H'03 is prohibition.

53.3.15 I²C HighSpeed SCL register high (ICHH)

ICHH is an 8-bit register and can set up the high-level time of SCL at the time of HS transmission.

ICHH is initialized by H'00 at the time of reset.

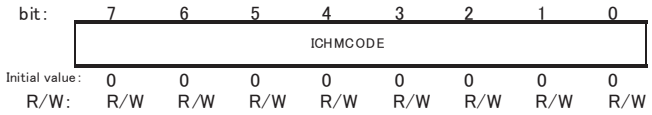


[Note] A setup of H'01 to H'02 is prohibition.

53.3.16 I²C HighSpeed Master code register (ICHMCODE)

ICHMCODE is an 8-bit register and is a register which stores a master code required at the time of HS transmission.

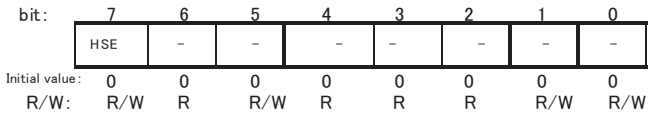
ICHMCODE is initialized by H'00 at the time of reset.



53.3.17 I²C option enabling register (ICVCON)

ICVCON sets up ON/OFF of the optional feature of I²C by an 8-bit register.

Not change this register value during I²C communication.



Bit	Bit Name	Initial Value	R/W	Description
7	HSE*1	0	R/W	Hs enable bit *1 In order to use HS transmission, a setup of automatic transmission is also required. 0: HS transmission is not used. 1: HS transmission is used.
6:0	-	0	R	Reserve bit Always give the value to write in as 0.

*1 Only I²C2 and I²C3 and I²C4 are effective. Please do not access in I²C0 and I²C1.
.The automatic transmission assumes the end of communication by interruption, and error detection, please do not perform
principle polling during automatic transmission.

53.3.18 I²C automatic transmission interruption mask register (ICIMSK)

ICIMSK is an 8-bit register and chooses prohibition/permission of the interrupt request output of automatic transmission.

Interruption is outputted to AL interruption event code. Generated interruption can be checked by ICINT.

bit:	7	6	5	4	3	2	1	0
	AENDM	TMC2M	TMC1M	TMOUTM	ALM	TACKM	-	-
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	AENDM	0	R/W	End interruption mask bit of I²C automatic transmission 0: Interruption is not outputted to INTC at the time of the end of automatic transmission. 1: Interruption is outputted to INTC at the time of the end of automatic transmission.
6	TMC2M	0	R/W	End interruption mask bit of I²C automatic transmission timer count 2 0: Interruption is not outputted to INTC at the time of the end of timer count 2. 1: Interruption is outputted to INTC at the time of the end of timer count 2.
5	TMC1M	0	R/W	End interruption mask bit of I²C automatic transmission timer count 1 0: Interruption is not outputted to INTC at the time of the end of timer count 1. 1: Interruption is outputted to INTC at the time of the end of timer count 1.
4	TMOUTM	0	R/W	I²C automatic transmission timeout error interruption mask bit 0: Interruption is not outputted to INTC at the time of a timeout error. 1: Interruption is outputted to INTC at the time of a timeout error.
3	ALM	0	R/W	I²C automatic transmission AL interruption mask bit 0: Interruption is not outputted to INTC at the time of the automatic transmission AL. 1: Interruption is outputted to INTC at the time of the automatic transmission AL.
2	TACKM	0	R/W	I²C automatic transmission TACK interruption mask bit 0: Interruption is not outputted to INTC at the time of the automatic transmission TACK. 1: Interruption is outputted to INTC at the time of the automatic transmission TACK.
1	-	0	R/W	Reserve bit Always give the value to write in as 0.
0	-	0	R/W	Reserve bit Always give the value to write in as 0.

53.3.19 I²C automatic transmission interruption flag register (ICINT1, ICINT2)

ICINT is an 8-bit register and displays the interruption state at the time of automatic transmission.

The interrupt bit can be cleared with ICASTART[7]=1 at beginning automatic operation ,or ICCR[7]=0.

bit:	7	6	5	4	3	2	1	0
	AEND	TMC2	TMC1	TMOUT	AAL	ATACK	AWAIT	ADTE
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
7	AEND	0	R	End flag bit of I²C automatic transmission 0: Under Automatic Transmission 1: End of Automatic Transmission
6	TMC2	0	R	End flag bit of I²C automatic transmission timer count 2 0: Timer Count 2 Un-Ending. 1: Timer Count 2 End
5	TMC1	0	R	End flag bit of I²C automatic transmission timer count 1 0: Timer Count 1 Un-Ending. 1: Timer Count 1 End
4	TMOUT	0	R	I²C automatic transmission timeout error flag bit 0: With No Timeout Error 1: Timeout Error Generating
3	AAL	0	R	I²C automatic transmission AL flag bit 0: With No AL 1: AL Generating
2	ATACK	0	R	I²C automatic transmission TACK flag bit 0: With No TACK 1: TACK Generating
1	AWAIT	0	R	I²C automatic transmission WAIT flag bit 0: With No WAIT 1: WAIT Generating
0	ADTE	0	R	I²C automatic transmission DTE flag bit 0: With No DTE 1: DTE Generating

53.3.20 I²C automatic transmission processing enabling register (ICACE1, ICACE2)

ICACE is an 8-bit register and chooses the use existence of each function under automatic transmission.

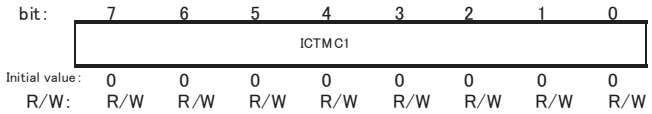
bit:	7	6	5	4	3	2	1	0
	AENDE	TMC2E	TMC1E	TMOUTE	ALE	TACKE	WAITE	–
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	AENDE	0	R/W	End detection enabling bit of automatic transmission 0: End of Automatic Transmission is not Detected. 1: Detect End of Automatic Transmission and it Outputs to ICINT.
6	TMC2E	0	R/W	A timer 1, a timer 2 enabling bit It is chosen whether end interruption of automatic transmission and timeout error detection timing are outputted after the setup time of TMC1 or TMC2. Refer to Fig. 53.3 for the wait timing of TMC1 and TMC2. ICACE[6:5] = 00:TMC1 and TMC2 are not used. It outputs after ICACE[6:5] = 01:TMC1. It outputs after ICACE[6:5] = 11:TMC1+TMC2. ICACE[6:5] = 10: Prohibition of a setup
5	TMC1E	0	R/W	
4	TMOUTE	0	R/W	Timeout error enabling bit After condition precedent generation can be detected as a timeout error to the timing set up by TMC1/TMC2, when the Low drive of SCL and the SDA continues being carried out. 0: Timeout Error is not Detected. 1: Detect Timeout Error and it Outputs to ICINT.
3	ALE	0	R/W	I²C transmission automatic AL error-handling enabling bit It is chosen whether processing to AL error generated during automatic transmission (a retry or stop processing) is performed. 0: With No Automatic AL Processing (AL is not Detected) 1: Those with automatic AL processing (opening and SCL are outputted for a SDA bus by 1 byte +ACK, and retry or stop processing is performed.)
2	TACKE	0	R/W	I²C transmission automatic ACK error-handling enabling bit It is chosen whether processing to the ACK error generated during automatic transmission (a retry or stop processing) is performed. 0: With no automatic ACK error handling. 1: Those with automatic ACK error handling. (Retry or stop processing is performed.)

1	WAITE	0	R/W	I²C transmission automatic WAIT processing enabling bit Only the time set up by ICTMCW during automatic transmission chooses whether automatic WAIT processing is performed. 0: With no automatic WAIT processing. 1: Those with automatic WAIT processing. (it set up by the ICTMCW register -- period WAIT is carried out)
0	-	0	R/W	Reserve bit Always give the value to write in as 0.

53.3.21 I²C automatic transmission timer control register 1 (ICTMC1)

ICTMC1 sets up the delay time of the detection timing of the end of automatic transmission, and a timeout error by an 8-bit register.

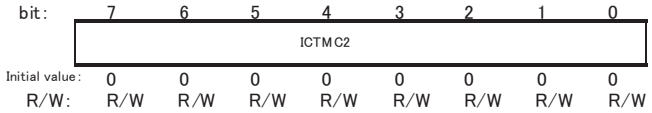


The delay time which can be set up by ICTMC1 becomes below. Delay time $= {}_{10}$(ICTMC1) x100xt_{SUBCK} which can be set up by ICTMC1

(the case of SUBCK=48MHz, it can set up from min 0us to max 530us by 2us unit.)

53.3.22 I²C automatic transmission timer control register 2 (ICTMC2)

ICTMC2 sets up the delay time of the detection timing of the end of automatic transmission, and a timeout error by an 8-bit register.



The delay time which can be set up by ICTMC2 becomes below. Delay time $= {}_{10}$(ICTMC2) x100xt_{SUBCK} which can be set up by ICTMC2

(SUBCK = in the case of 48MHz, it can set up from min 0us to max 530us by 2us unit.)

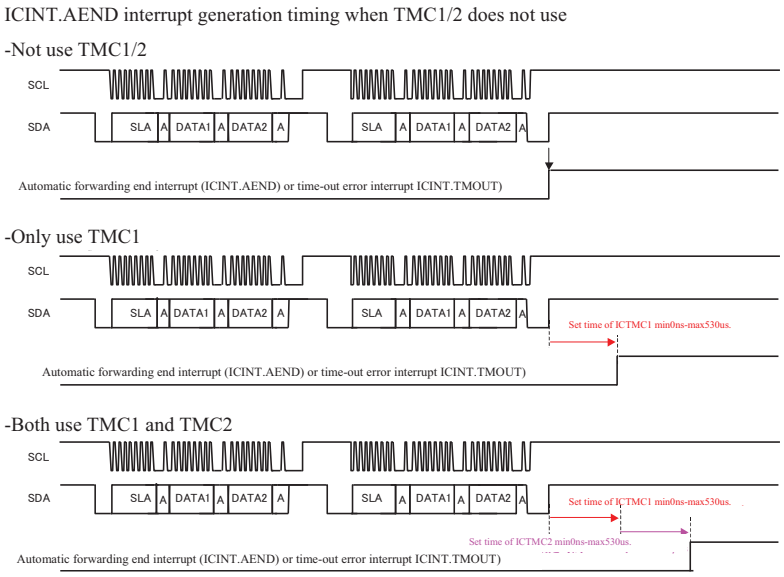
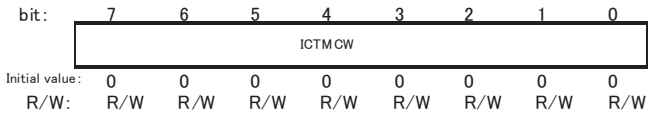


Fig. 53.3 Wait timing chart of TMC1, TMC2

53.3.23 I²C automatic transmission wait control register (ICTMCW1, ICTMCW2)

ICTMCW sets up the wait time under automatic transmission by an 8-bit register. When you carry out one set of ICACE(s) [1] and you use a wait function, please be sure to change into a set point (values other than H'00).



The wait time which can be set up by ICTMCW becomes below.

Delay time $= {}_{10}(\text{ICTMCW}) \times 10 \times t_{SUBCK}$ by ICTMCW

(SUBCK = in the case of 48MHz, it can set up by min 0ns and max53microsecond 0.2us unit.)

Although wait time can be set up this register, it is delayed by a SCL cycle unit.
For this reason , a SCL bus may not wait even if it changes this register.

Moreover, it wait for 1 SCL cycle before ACK even if it is not concerned with a setup of a wait control register during automatic transmission.

53.3.24 I²C automatic transmission transformer start register (ICSTART)

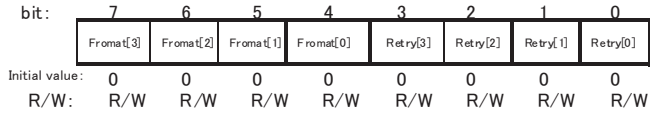
ICSTART is an 8-bit register and sets up end processing in the middle of the start of automatic transmission, and reset.

bit:	7	6	5	4	3	2	1	0
	AutoStart	AutoTrans Reset	AutoStop	–	–	–	ATDMA	ARDMA
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	AutoStart	0	R/W	I²C automatic transmission start bit When you start automatic transmission of I²C, carry out one set of these bits. Don't clear this bit zero during automatic transmission.
6	AutoTransReset	0	R/W	I²C automatic transmission processing reset bit When you reset the internal processing about automatic transmission, set this bit to 1. When you perform automatic transmission processing again, clear zero. In addition, a register is not initialized in reset by this bit. Use ICE reset, when you initialize a register.
5	AutoStop	0	R/W	It is a stop bit in the middle of I²C automatic transmission. A condition precedent is generated for under automatic transmission per 1 byte +ACK bit by carrying out one set of these bits, and communication is ended. following the communication format which will have been set up if this function is used -- an end -- things may not be made. 0: Normal Operation 1: Publish a condition precedent in the middle of automatic transmission, and communication is ended.
4:2	-	0	R/W	Reserve bit Always give the value to write in as 0.
1	AutoTDMAenable	0	R/W	At the time of automatic transmission DMA transmitting specification bit 0: DMA is not Used. 1: All Transmission is Performed by DMA.
0	AutoRDMAenable	0	R/W	At the time of automatic transmission DMA reception specification bit 0: DMA is not Used. 1: All Reception is Performed by DMA.

53.3.25 I²C automatic transmission transformer control register (ICATFR)

ICATFR is an 8-bit register and sets the number of times of a retry to an automatic transmission format.



Bit	Bit Name	Initial Value	R/W	Description
7:4	Transformat [3:0]	0000	R/W	I²C automatic transmission format selection The format of automatic transmission is specified. Refer to Fig. 53.7 for a communication format. S= start conditions, Sr= resending conditions, P= condition precedent 0000: S-> Transmitting 1->P 0001: S-> Transmitting 1 -> Receiving 1->P 0010: S-> Transmitting 1 ->Sr-> Transmitting 2->P 0011: S-> Transmitting 1 ->Sr-> Transmitting 2 -> Receiving 1->P 0100: S-> Transmitting 1 -> Receiving 1 ->Sr-> Transmitting 2->P 0101: S-> Transmitting 1 -> Receiving 1 ->Sr-> Transmitting 2 -> Receiving 2->P Others: Prohibition of a setup
3:0	ReTry[3:0]	0000	R/W	Number-of-times selection of I²C automatic transmission retry * The number of times which communicates again automatically during automatic transmission at the time of AL error or non-ACK error generating is specified. If one of the number of times of a retry turns into the number of times set as this bit, interruption of AL and non-ACK will be outputted. ReTry [3:0] =H'0: With no retry It retries to ReTry[3:0] =H'1:1 time. - It retries to ReTry[3:0] =H'E:14 time. ReTry[3:0] =H'F: Prohibition of a setup

[Note] Retry processing cannot be performed when using * DMA transfer.

53.3.26 I²C automatic transmission transformer time register 1 (ICATSET1)

ICATSET1 is an 8-bit register and it specifies the number of data of the transmission 1 of the format set up by ICATFR [7:4].

When using registers ICATD00-ICATD09, in [256 bytes of] a maximum of 10 bytes and DMA transmission, it can transmit.
A slave address is also contained in transmitting data.

ICATD00-ICATD09 are used. :
1 byte (ICATSET1 [7:0] =8'h00) - 10 bytes (ICATSET1[7:0] = 8'h09)
DMA is used. :
256 bytes (ICATSET1[7:0] =8'hFF) of MAX

bit:	7	6	5	4	3	2	1	0
	ICATSET1							
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

53.3.27 I²C automatic transmission transformer time register 2 (ICATSET2)

ICATSET2 is an 8-bit register and it specifies the number of data of the transmission 2 of the format set up by ICATFR [7:3].

When using registers ICATD10-ICATD19, in [256 bytes of] a maximum of 10 bytes and DMA transmission, it can transmit. Slave address data is also contained in transmitting data.

ICATD10-ICATD19 are used. :
1 byte (ICATSET2 [7:0] =8'h00) - 10 bytes (ICATSET2 [7:0] =8'h09)
DMA is used. :
256 bytes (ICATSET2[7:0] =8'hFF) of MAX

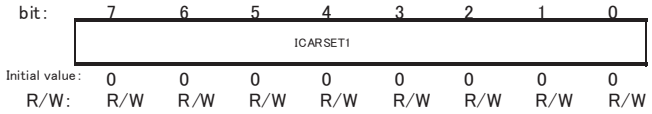
bit:	7	6	5	4	3	2	1	0
	ICATSET2							
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

53.3.28 I²C automatic transmission receipt time register 1 (ICARSET1)

ICARSET1 is an 8-bit register and it specifies the number of data of the reception 1 of the format set up by ICATFR [7:3].

When using registers ICARD00-ICARD09, in [256 bytes of] a maximum of 10 bytes and DMA reception, it can receive.

ICARD00-ICARD09 are used. :
1 byte (ICARSET1 [7:0] =8'h00) - 10 bytes (ICARSET1 [7:0] =8'h09)
DMA is used. :
256 bytes (ICARSET1[7:0] =8'hFF) of MAX

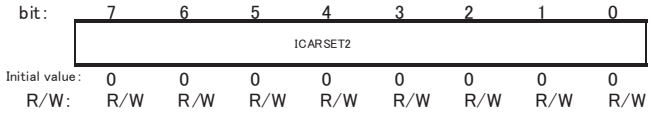


53.3.29 I²C automatic transmission receipt time register 2 (ICARSET2)

ICARSET2 is an 8-bit register and it specifies the number of data of the reception 2 of the format set up by ICATFR [7:3].

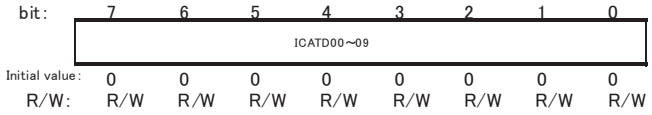
When using registers ICARD10-ICARTD19, in [256 bytes of] a maximum of 10 bytes and DMA reception, it can receive.

ICARD10-ICARD19 are used. :
1 byte (ICARSET2 [7:0] =8'h00) - 10 bytes (ICARSET2[7:0] = 8'h09)
DMA is used. :
256 bytes (ICARSET2[7:0] =8'hFF) of MAX



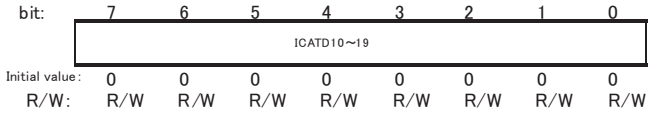
53.3.30 I²C automatic transmission transformer data 00-09 (ICATD00-ICATD09)

ICATD 00-09 is an 8-bit register, and stores the data of transmission 1.



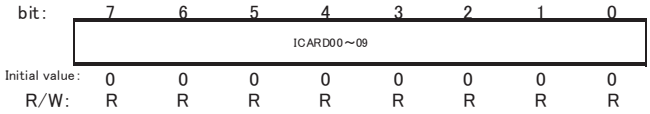
53.3.31 I²C automatic transmission transformer data 10-19 (ICATD10-ICATD19)

ICATD 10-19 is an 8-bit register, and stores the data of transmission 2.



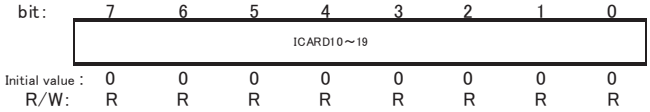
53.3.32 I²C automatic transmission receipt data 00-09 (ICARD00-ICARD09)

ICARD 00-09 is an 8-bit register, and stores the receiving data of reception 1.



53.3.33 I²C automatic transmission receipt data 10-19 (ICARD10-ICARD19)

ICARD 10-19 is an 8-bit register, and stores the receiving data of reception 2.



53.3.14 Transfer Rate

An I²C transfer rate can be set by ICCL, ICCH, ICIC7 and ICIC6, and SUBϕ. Table 53.5 lists transfer rate settings, and Figure 53.4 shows SCL waveforms.

Table 53.5 Transfer Rate Settings

	SUBϕ	ICIC[7] + ICCL	ICIC[6] + ICCH	Transfer Rate*2
Standard	12 MHz	H'042	H'036	100 kHz
	13.5 MHz	H'04A	H'03D	100 kHz
	24 MHz	H'082	H'06E	100 kHz
	27 MHz	H'096	H'078	100 kHz
	33 MHz	H'0AF	H'09B	100 kHz
	48 MHz	H'10B	H'0D5	100 kHz
Fast Speed*1	12 MHz	H'012	H'00C	400 kHz
	13.5 MHz	H'016	H'00C	397.1 kHz
	24 MHz	H'026	H'016	400 kHz
	27 MHz	H'02C	H'018	397.1 kHz
	33 MHz	H'033	H'020	397.6 kHz
	48 MHz	H'043	H'035	400 kHz
High Speed*3	48MHz	H'0F	H'08	2MHz

Notes: 1. When the set value of ICCL/ICCH is H'00A (minimum), 8 MHz is required for SUBϕ if a transfer rate is 400 kHz. If SUBϕ is less than 8 MHz, a transfer rate of 400 kHz is not ensured.

2. The transfer rates in above settings are theoretical values. The actual transfer rates are generally smaller than those theoretical values due to the pull-up resistor (Rp) and the capacitance (Cp). However, there is no harm in communication because the actual transfer rates satisfy the I²C bus specifications. (Smaller ICCL and ICCH can increase the actual transfer rates. In this case, though, set ICCL and ICCH to ensure that t_{LOW} and t_{HIGH} are within the specifications.)

3. In three actual measurements, a transmission rate may become low with the pull-up resistor (Rp) of a board, and electrostatic capacity (Cp). In order to improve transmission performance, please change the value of ICHL and ICHH in the range which SCL becomes in I^2C-bus standard.

(1) Notes on the transfer rate

The transfer rates in above settings are theoretical values. The actual transfer rates are generally smaller than the theoretical values due to the pull-up resistor (Rp) and the capacitance (Cp). However, there is no harm in communication because the actual transfer rates satisfy the I²C bus

specifications. (Smaller ICCL and ICCH can increase the actual transfer rates. In this case, though, set ICCL and ICCH to ensure that t_{LOW} and t_{HIGH} are within the specifications.)

A calculation example of ICCL and ICCH:*[1]

- Conditions
  - SUBϕ: 48 MHz
  - I²C transfer rate: 100 kHz
  - L/H ratio in SCL*[2]: L/H = 5/4
- Result
  - ICIC[7] + ICCL = (SUBϕ ÷ I²C transfer rate) × (L ÷ (L + H))
  - = $((48 \times 10^6) \div (100 \times 10^3)) \times (5 \div (5 + 4) = 267 = (10B)_{16}$
  - ICIC[6] + ICCH = (SUBϕ ÷ I²C transfer rate) × (H ÷ (L + H))
  - = $((48 \times 10^6) \div (100 \times 10^3)) \times (4 \div (5 + 4) = 213 = (0D5)_{16}$

Notes: 1. If the result is indivisible, some modifications are introduced to make the total count number closer to the desirable transfer rate.
2. SCL L/H ratio is arbitrary as long as it satisfies t_{LOW} and t_{HIGH}. In above case, L/H is set as 5/4.

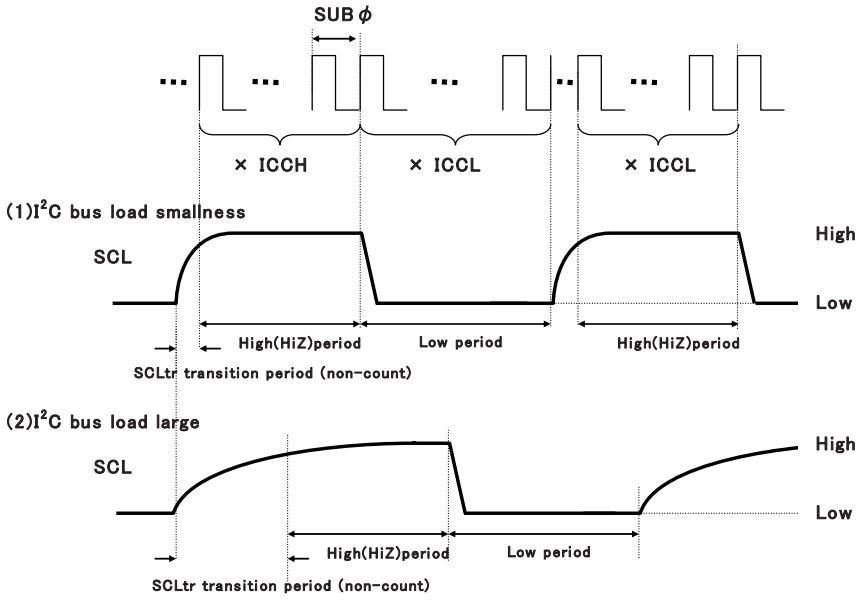


Figure 53.4 SCL Waveforms

53.4 Operation

53.4.1 I²C Bus Data Format

The I²C bus formats are addressing formats with an acknowledge bit. These are shown in figures 53.5 and 53.6. The first frame following a start condition always consists of 8 bits. the format at the time of HS mode which can be used is shown in Fig. 53.7

The symbols used in figures 53.5 and 53.6 are explained in Table 53.6.

Table 53.6 I²C Bus Data Format Symbols

Symbol	Description
S	Start condition. The master device drives SDA from high to low while SCL is high.
Sr	Retransmit condition. The master device drives SDA from high to low while SCL is high.
SLA	Slave address, by which the master device selects a slave device.
R/W	Indicates the direction of data transfer: from the slave device to the master device when R/W is 1, or from the master device to the slave device when R/W is 0.
A	Acknowledge. The receiving device (the receiving device in master transmit mode, or the master in master receive mode) drives SDA low to acknowledge a transfer.
DATA	Transmitted or received data. The bit length is 8 bits.
P	Stop condition. The master device drives SDA from low to high while SCL is high.

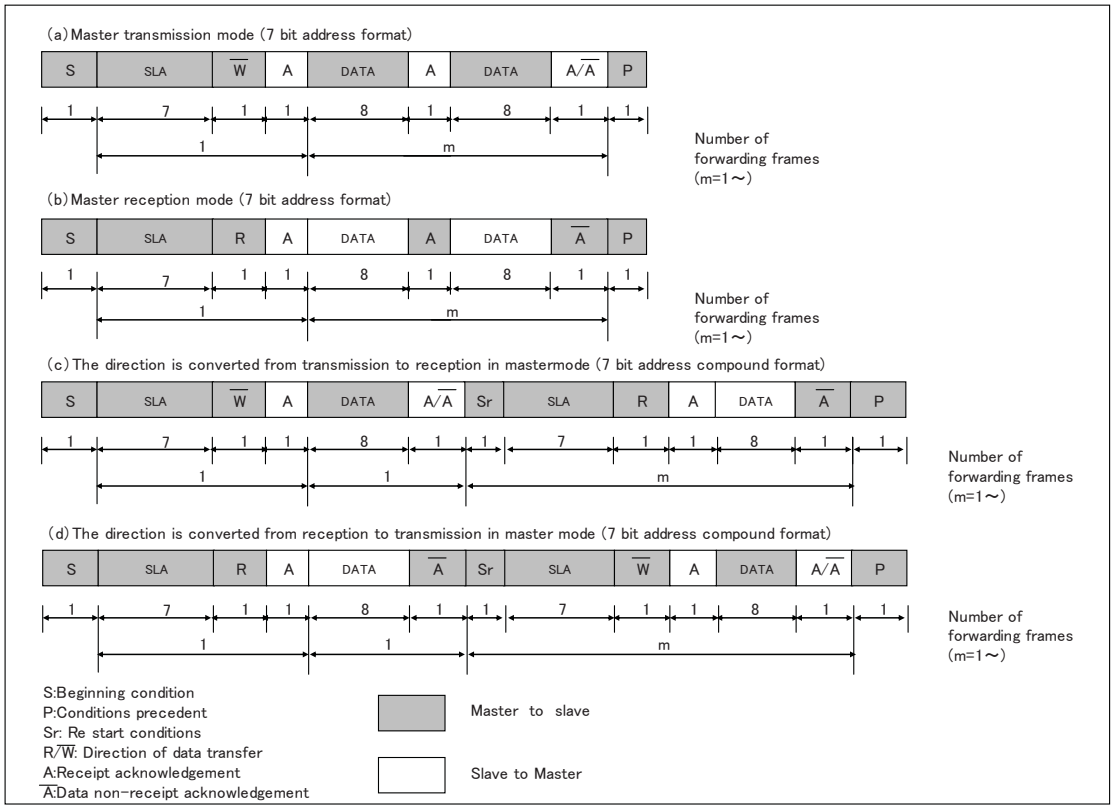


Figure 53.5 I²C Bus Data Formats (7-Bit Address Format)

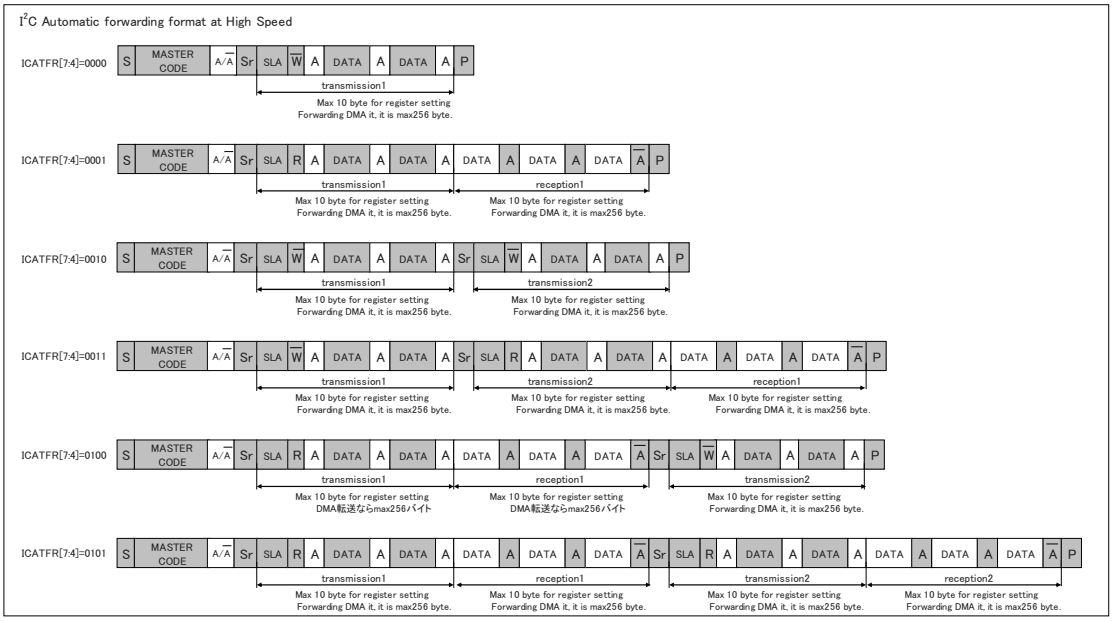


Figure 53.7. The bus data format which can be I²C HS automatic transmission used

53.4.2 Master Transmit Operation

In master transmit mode, the master device outputs the transmit clock and transmit data, and after the receiving device receives data, it returns an acknowledge signal. The transmission procedure and operations are described below.

1. Set bits in ICCL, ICCH, and ICIC according to the operating mode.
2. Write H'94 in ICCR to issue the start condition. The DTE bit in ICSR is then set to 1.
3. To transmit data, write data to ICDR. The DTE bit is then automatically cleared.
   Data transmission starts when data is sent to the internal transmit buffer. The DTE bit in ICSR is then set to 1 again.
4. To issue and generate the stop condition, write the final data to ICDR, then write H'90 to ICCR.
   DTE is not set to 1 from issuing the stop condition to generating the stop condition. After the final data is transmitted, the stop condition is generated and operation is stopped.
5. To issue and generate the retransmit condition, write the final data to ICDR, then write H'94 to ICCR.
   DTE is not set to 1 from issuing the retransmit condition to generating the retransmit condition. After the final data is transmitted, the retransmit condition is generated.
6. To change from transmission to reception, write the final data to ICDR, then write H'81 to ICCR. After transmitting the final data, transmission is automatically changed to reception and receiving operation is started.

By repeating step 3, data can be consequently transmitted. A non-acknowledge interrupt occurs if the received acknowledge bit is 1 (TACK = 1) when non-acknowledge is detected. To continuously transmit data without detecting non-acknowledge, set the TACKE bit in ICIC to 0, and perform steps 3 and 4 to 6. At this time, since non-acknowledge is not detected, data can be continuously transmitted.

To change transmission to reception, write H'81 to ICCR until the completion of transmission of the final data. At this time, if writing to ICCR is delayed, use a WAIT interrupt to write to ICCR until the completion of transmission of the final data.

To generate a retransmit condition during transmission, the final data is written to ICDR and H'94 is written to ICCR. If, due to a delay in ICDR or ICCR writing, processing is performed continuously before and after generating the ACK bit, a DTE interrupt is generated before the retransmit condition is generated, which disables the software control for normal communication. For this reason, modify ICDR and ICCR before generating the ACK bit.

ICDR and ICCR can be written before the ACK bit is generated by modifying them from the occurrence of a WAIT interrupt until the WAIT interrupt source is cleared.

To generate a stop condition during transmission, the final data is written to ICDR and H'90 is written to ICCR. If, due to a delay in ICDR or ICCR writing, processing is performed continuously before and after generating the ACK bit, a DTE interrupt is generated before the stop condition is generated. For this reason, modify ICDR and ICCR before generating the ACK bit.

ICDR and ICCR can be written before the ACK bit is generated by modifying them from the occurrence of a WAIT interrupt until the WAIT interrupt source is cleared.

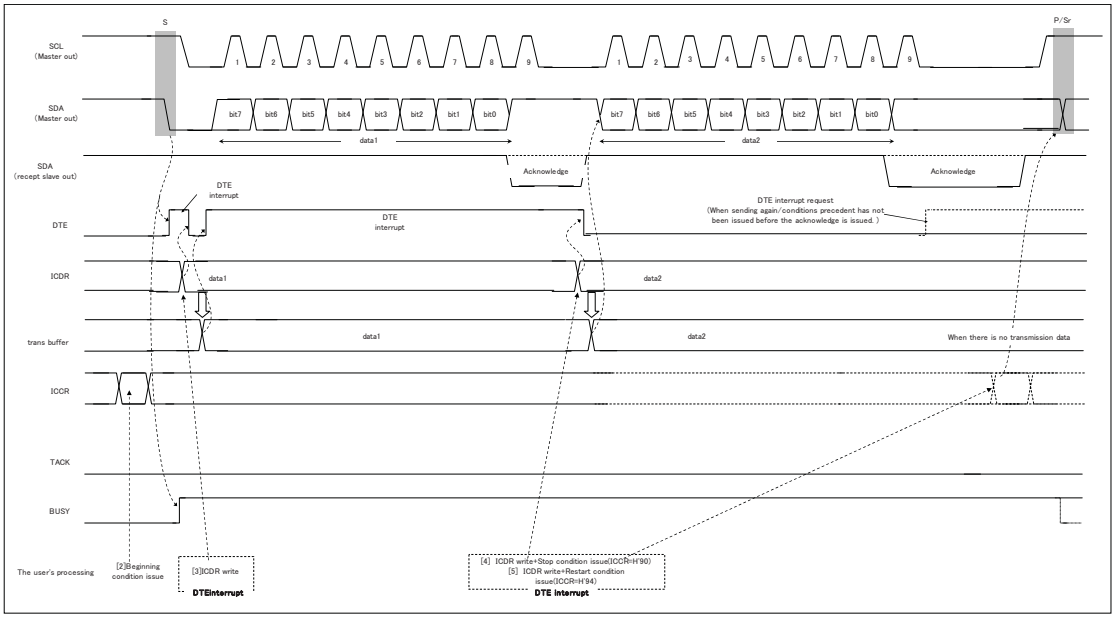


Figure 53.8 Example of Master Transmit Mode Operation Timing (WAIT = 0)

53.4.3 Master Receive Operation

In master receive mode, the master device outputs the receive clock, and returns an acknowledge signal after the transmit device transmits data. The reception procedure and operations in master receive mode are described below.

(1) When Two or More Bytes of Data are Received Continuously

1. Switch from transmit mode to receive mode automatically to start reception.
2. After data is received to the receive buffer, data is transmitted to ICDR and the DTE bit is set to 1. At this time, the next data reception starts.
3. To continuously receive data, read data from ICDR. When data is read from ICDR, the DTE bit is automatically cleared.
4. To issue/generate the stop condition, read data from ICDR, then write H'C0 to ICCR. After the stop condition is issued, the final data is received. After data is read from ICDR, the stop condition is generated to stop the operation.
5. To issue/generate the retransmit condition, read data from ICDR, then write H'D4 to ICCR. After the retransmit condition is issued, the final data is received. After data is read from ICDR, the retransmit condition is generated. Then, reception is automatically switched to transmission, and transmission starts.

Two or more bytes of data can be received continuously by repeating steps 2 and 3.

The following problem can arise if the stop or retransmission condition is to be issued during the continuous reception of two or more bytes of data. If the byte immediately before the final byte is read from ICDR and H'D4 or H'C0 (to generate the retransmission or stop condition) is written to ICCR, but writing to ICCR is delayed and processing to overwrite this register cannot be completed by the time the NACK bit should be generated on reception of the last byte (reading of ICDR), an ACK bit will be generated on reception of the last byte. This operation is not in accord with the I²C communications protocol.

Accordingly, ensure that the change to the ICCR setting is complete in time for the NACK bit to be generated in response to reading of ICDR for reception of the final byte.

Furthermore, after generation of the WAIT interrupt, reading of ICDR for the last byte but one and writing to ICCR by the time the WAIT interrupt source has been cleared ensures that the NACK bit will be generated when the last byte is received.

(2) When Only One Byte of Data is Received

When only one byte data is received, use a WAIT interrupt to issue the stop/retransmit condition to ICCR.

1. Switch from transmit mode to receive mode automatically to start reception.
2. The WAIT bit is set to 1. At this time, write H'C0 to ICCR to issue/generate the stop condition. Write H'D4 to ICCR to issue/generate the retransmit condition.
3. The WAIT bit is cleared to 0.
4. After data is received to the receive buffer, data is transmitted to ICDR and the DTE bit is set to 1.
5. When the stop condition has been issued to ICCR, the stop condition is generated to stop the operation after data is read from ICDR. When the retransmit condition has been issued to ICCR, the retransmit condition is generated, reception is then automatically switched to transmission, and transmission starts.

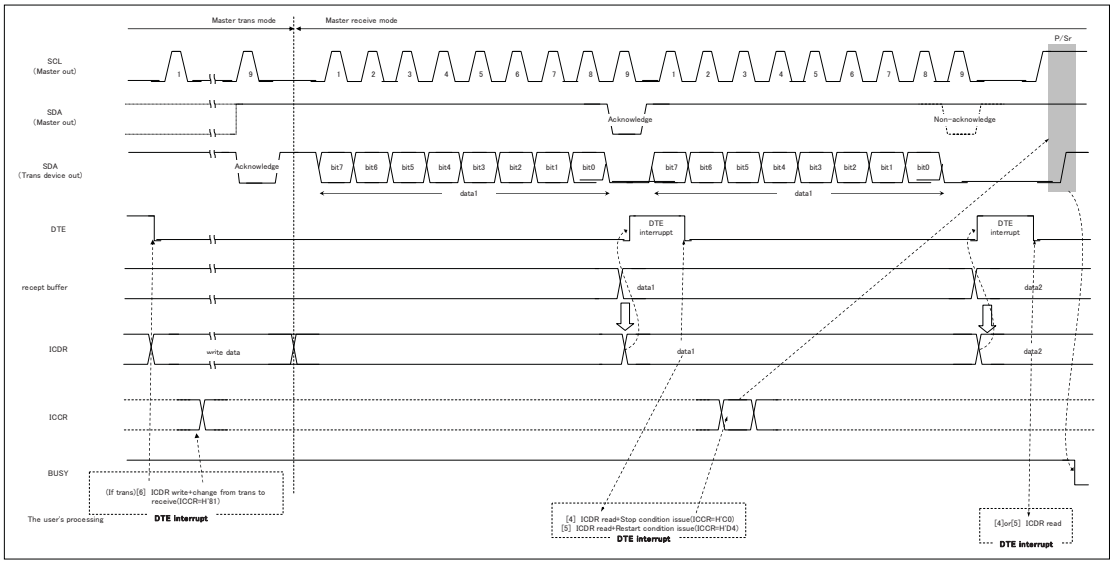


Figure 53.9 Example of Master Receive Mode Operation Timing (WAIT = 0)

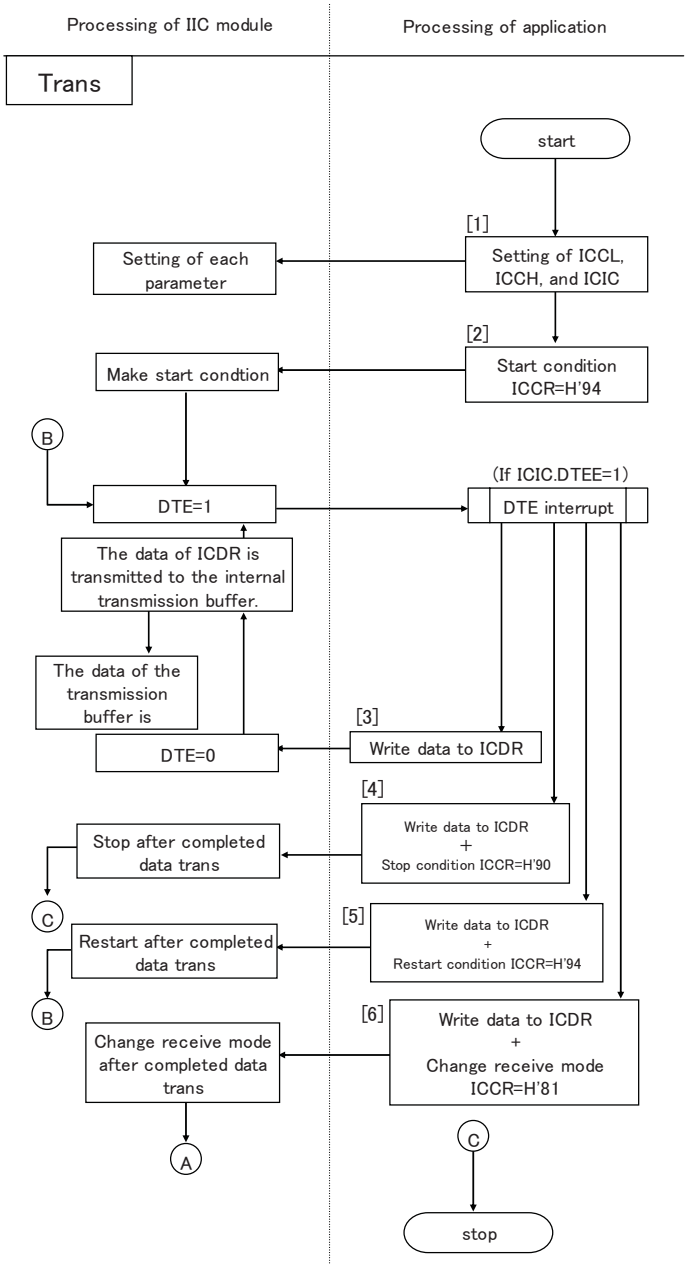


Figure 53.10 I²C Transmission Sequence (in Transmit Mode)

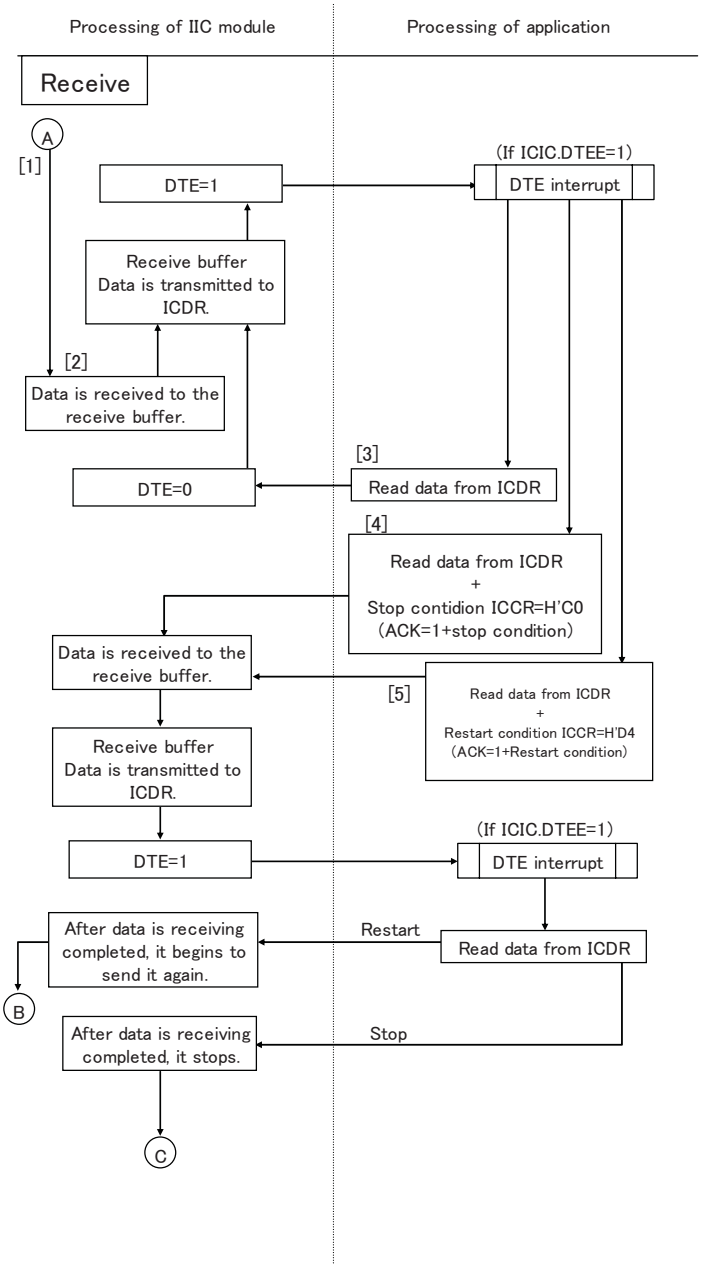


Figure 53.11 I²C Transmission Sequence (in Receive Mode of Two or More Bytes of Data)

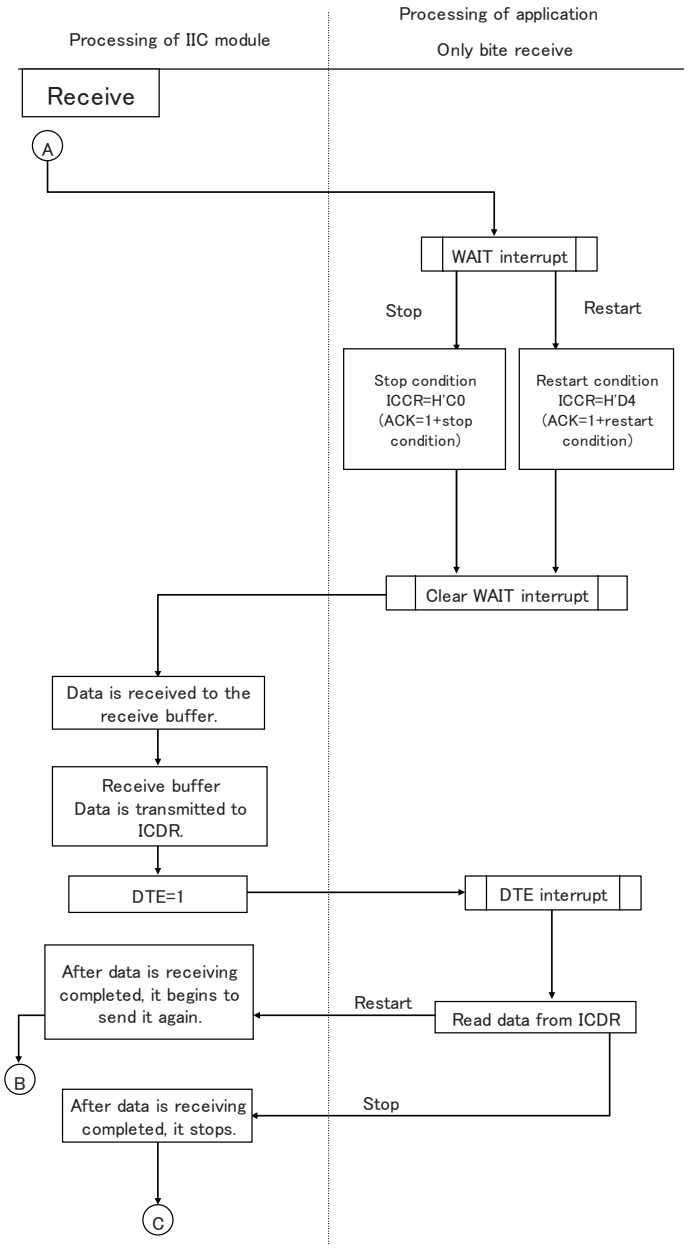


Figure 53.12 I²C Transmission Sequence (in Receive Mode of One Byte of Data)

53.4.4 I²C Continuous Transmission by DMA

In DMA transmit mode, the master device outputs a DMA request to the DMAC. The received DMAC returns ICDR data writing and DMARACK to the master device. The transmission procedure and operations are described below.

1. Set bits in ICCL, ICCH, and ICIC according to the operating mode. Set the TDMAE and WAITE bits in ICIC to 1. Then, set the DMAC. For the setting methods of the DMAC, refer to section 8, Direct Memory Access Controller (DMAC).
2. Write H'94 to ICCR to set the start condition. A DMA request is then output.
3. When the DMAC receives a DMA request, data is written to ICDR. Transmission is then started. When transmission is performed the number of times specified by DMAC, a DEI interrupt in DMAC is set.
4. To set or generate the stop condition, clear the RDMAE bit of ICIC to 0 and set the DTEE bit to 1. After setting of ICIC, the DTE bit is set to 1. At this time, when H'90 is written to ICCR, the stop condition is generated, and operation is stopped.

By repeating step 3, data can be consequently transmitted. A non-acknowledge interrupt occurs when non-acknowledge is detected. To continuously transmit data without detecting non-acknowledge, set the TACKE bit in ICIC to 0, and perform steps 3 and 4. At this time, since non-acknowledge is not detected, data can be continuously transmitted.

53.4.5 I²C Continuous Receive by DMA

In DMA receive mode, the master device outputs a DMA request to the DMAC. The DMAC that received the request returns ICDR data reading and DMARACK to the master device. When I²C continuous receive is performed by DMA, receive data of 4 bytes or more is needed. The reception procedure and operations are described below.

1. For transmission, set bits in ICCL, ICCH, and ICIC according to operating mode. Set the RDMAE and WAITE bits in ICIC to 1. Then, set the DMAC. For the setting methods of the DMAC, refer to section 8, Direct Memory Access Controller (DMAC).
2. Switch from transmit mode to receive mode automatically to start reception.
3. After data is received at the receive buffer, a DMA request is output. At this time, the next data reception starts.
4. To continuously receive data, read data from ICDR in each DMA request. When reception is performed the number of times specified by DMAC, a DEI interrupt in DMAC is set.
5. To set or generate the stop condition, clear the RDMAE bit of ICIC to 0 and set the DTEE bit to 1. After setting of ICIC, the DTE bit is set to 1. At this time, when H'D4 is written to ICCR, data is read from ICDR.
6. Write H'D4 to ICCR and read data from ICDR. The DTE bit is then cleared automatically. The DTE bit is set to 1 again, and the stop condition is generated, and operation is stopped after data has been read from ICDR.

By repeating step 3, data of 4 bytes or more can be continuously received.

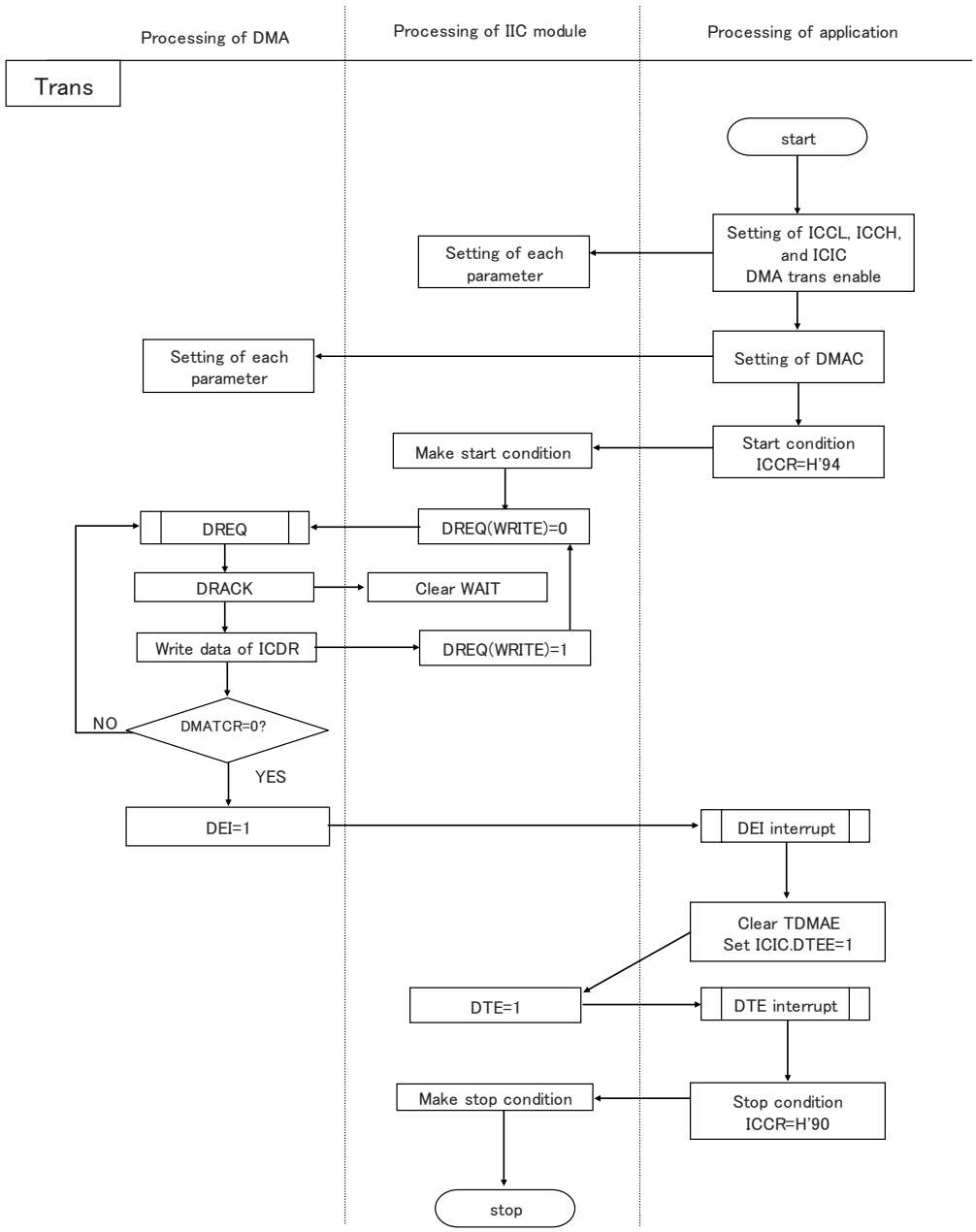


Figure 53.13 I²C Continuous Transmission Sequence by DMA

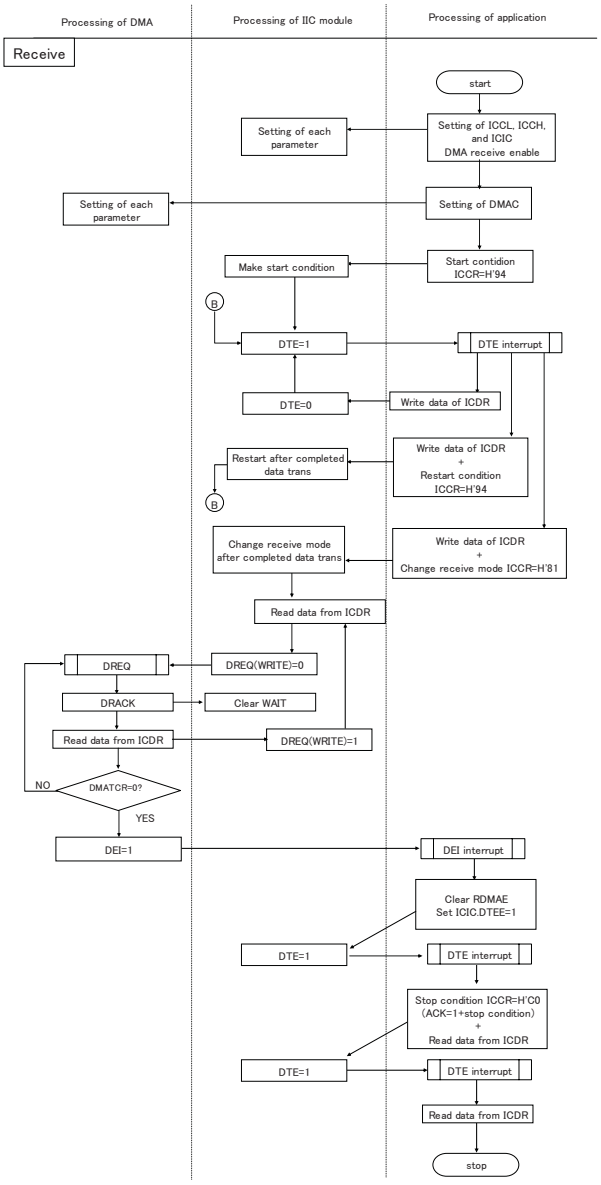


Figure 53.14 I²C Continuous Receive Sequence by DMA

53.4.6 Synchronizing SCL Line

When the SCL line state is changed from high to low, related devices start counting in the low period. When the clock of a device becomes low, the device holds the SCL line low until its clock becomes high (see Figure 53.15). However, even if the clock of the device is changed from low to high, the SCL line state does not change when clocks of other devices are in the low period. Therefore, the low period of the SCL line is determined by the device with the longest low period. At this time, a device with the short low period waits in the high state.

When all devices complete the low period, the clock line is open and in the high state. Therefore, the device clock and SCL line are in the same state, and start counting both of pulses in high level period. The SCL line enters the low state again by the device that has first completed the high period.

The low period is determined by the device with the longest low period, and the high period is determined by the device with the shortest high period. The SCL line is then synchronized.

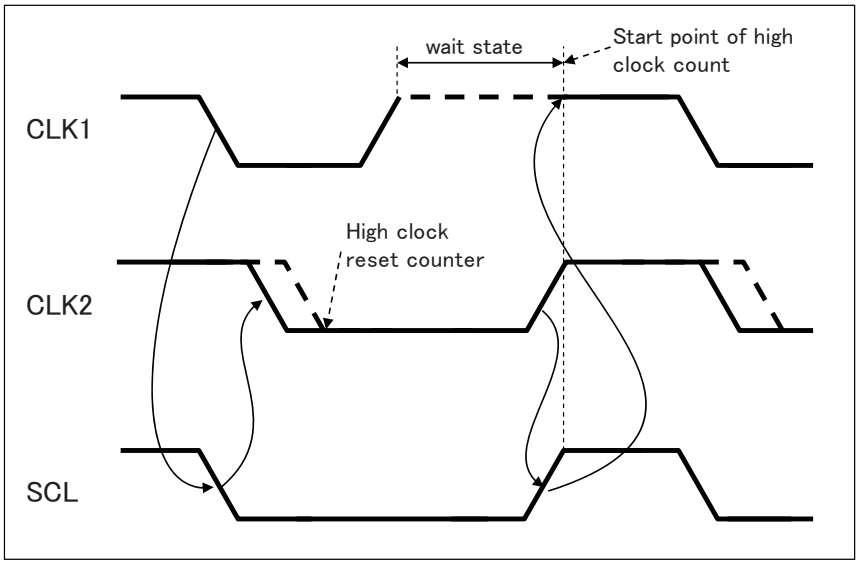


Figure 53.15 Synchronizing SCL Line

53.4.7 Noise Canceler

The logic levels at the SCL and SDA pins are routed through noise cancelers before being latched internally. Figure 53.16 shows a block diagram of the noise canceler circuit.

The noise canceler consists of three cascaded latches and a match detector. The SCL (or SDA) input signal is sampled on SUBϕ, but is not passed forward to the next circuit unless the outputs of both latches agree. If they do not agree, the previous value is held.

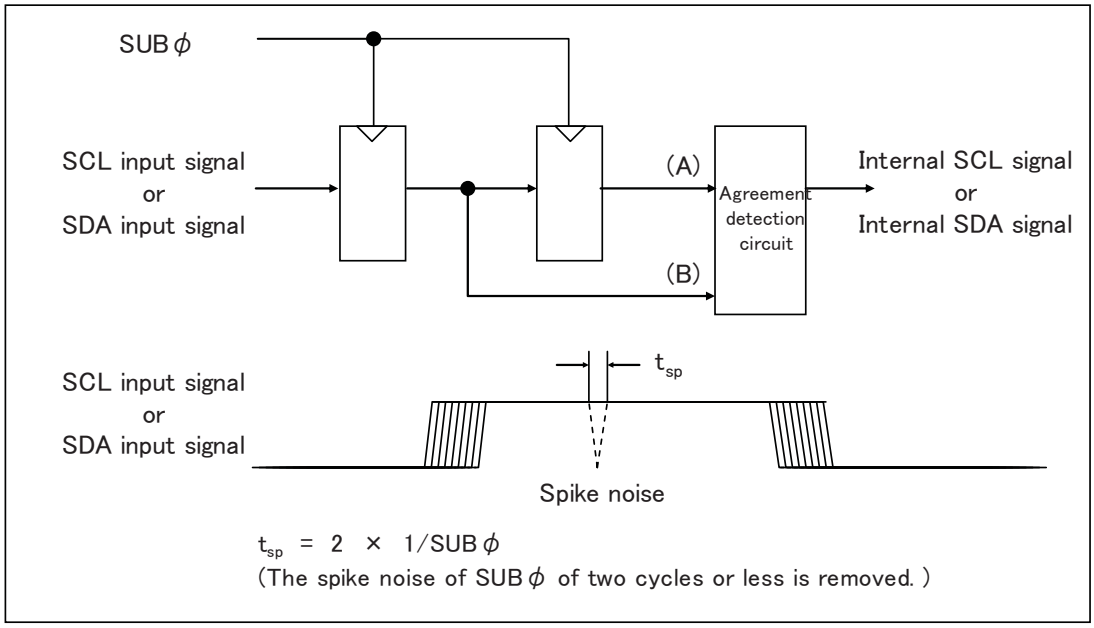


Figure 53.16 Block Diagram of Noise Canceler

53.4.8 Arbitration Lost Operation

This module can issue an arbitration lost interrupt request when bus conflict defeat occurs.

Interrupt occurrence conditions are described below.

- When received data changes while high SCL clocks are counted in master transmit/receive mode.
- When the SCL line becomes low while high SCL clocks are counted.
- When this module detects the start condition before issuing the start condition.
- When the monitored SDA (external) and data output from this module disagree.

Under the above conditions, the AL bit in ICSR is set to 1, and an arbitration lost interrupt occurs.

When arbitration lost is detected in data transmission, the SDA line is open. The SCL clock line outputs clocks until acknowledge end of the frame, then opens buses. Figure 53.17 shows an example of arbitration lost interrupt operation timing.

To cancel an interrupt, clear the AL bit in ICSR to 0. Conditions for clearing to 0 are described below.

- When data is written to ICDR (in transmission), and data is read (in reception), when DTE = 1.
- When 0 is written.

When arbitration is lost by the acknowledge bit, hold SCL and SDA at a low level.

ICE must be reset by the software to release the bus.

With the AL bit set to 1, do not clear the ALE bit to 0. Preferably, the setting of the ALE bit should be performed only before the start of communication.

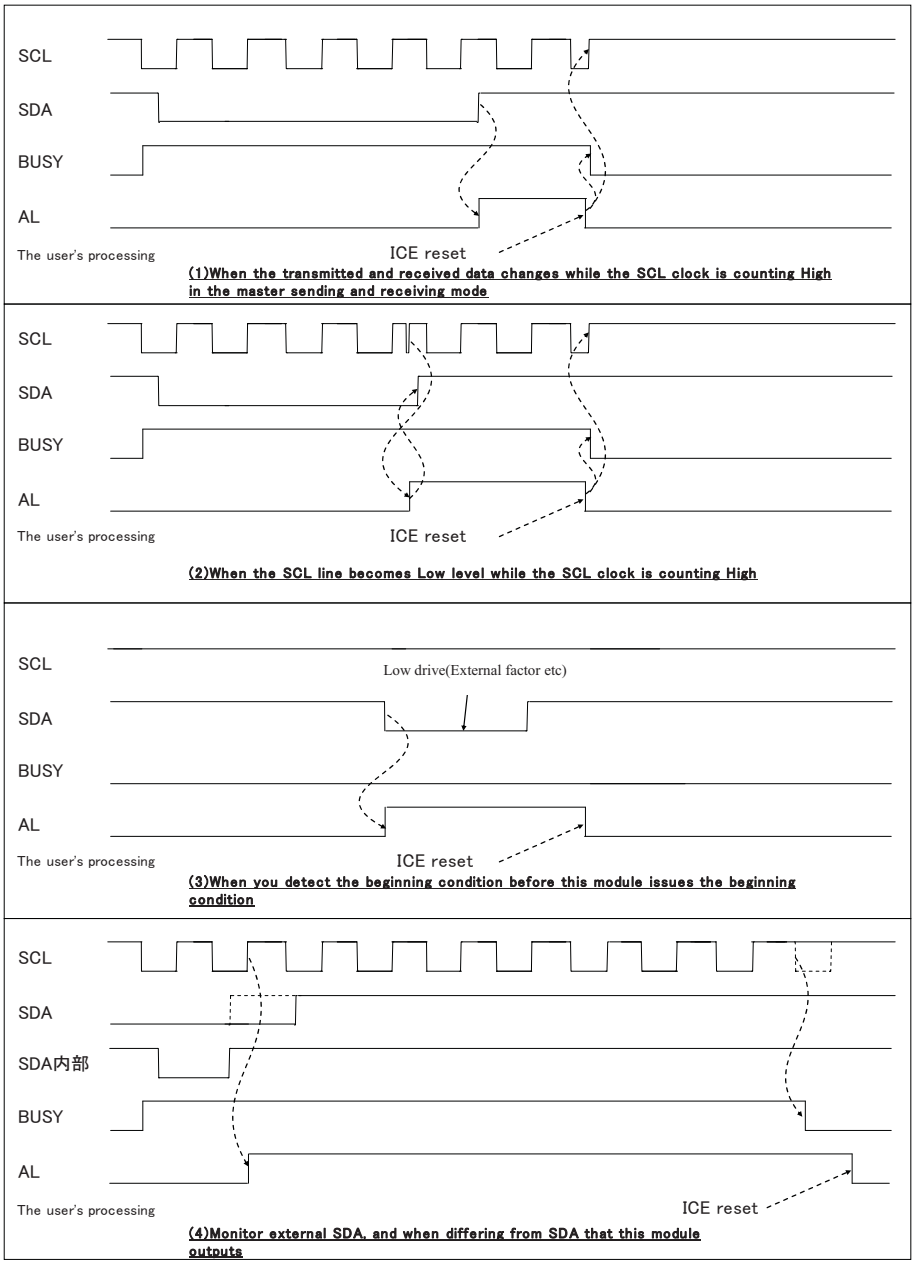


Figure 53.17 Example of Arbitration Lost Interrupt Operation Timing

53.4.9 Non-Acknowledge Operation

This module can issue a non-acknowledge interrupt when there is no acknowledge from the receiving device in transmission.

An acknowledge bit from the receiving device is stored in the TACK bit in ICSR. A non-acknowledge interrupt is issued if the TACK bit is set to 1 when TACKE in ICIC is 1.

To cancel the non-acknowledge interrupt, clear the TACK bit to 0.

With the TACK bit set to 1, do not clear the TACKE bit to 0. Preferably, the setting of the TACKE bit should be performed only before the start of communication.

Figure 53.18 shows an example of non-acknowledge operation timing.

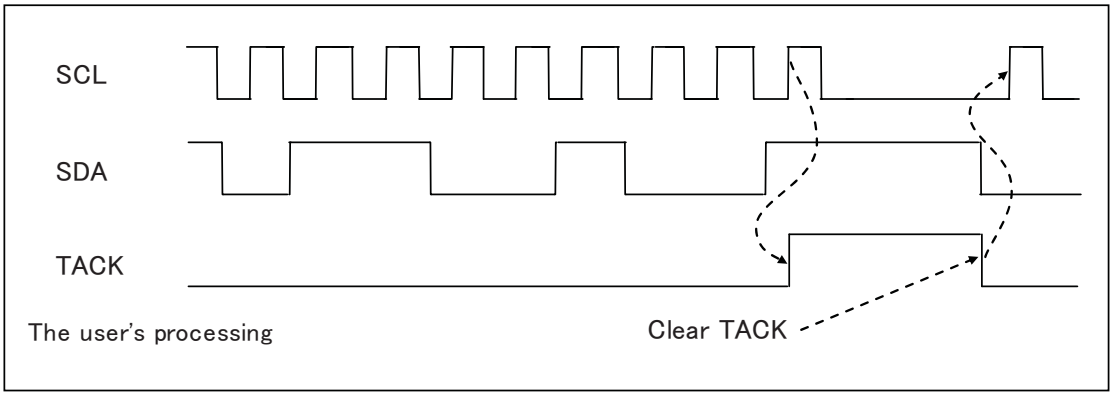


Figure 53.18 Example of Non-Acknowledge Operation Timing

53.4.10 Wait Operation

This module can make operation mode the wait state by the WAIT bit in ICSR. WAIT is set to 1 at a falling edge of the eighth transmit clock for the master device.

After that, the transmit clock is fixed to low until the WAIT bit is cleared to 0.

When the WAIT bit is cleared to 0, the ninth transmit clock is generated, and the state is returned from the wait state.

When performing the I²C communication processing using a WAIT interrupt, the I²C signals stay in the WAIT state from the time when the WAIT state is detected by the hardware until the WAIT interrupt source is cleared by the software. When the module performs communication processing only with a DTE interrupt, the I²C signals do not stay in the WAIT state. Therefore the communication is delayed by the time period where the I²C signals stay in the WAIT state.

Preferably, the setting of the WAITE bit should be performed only before the start of communication

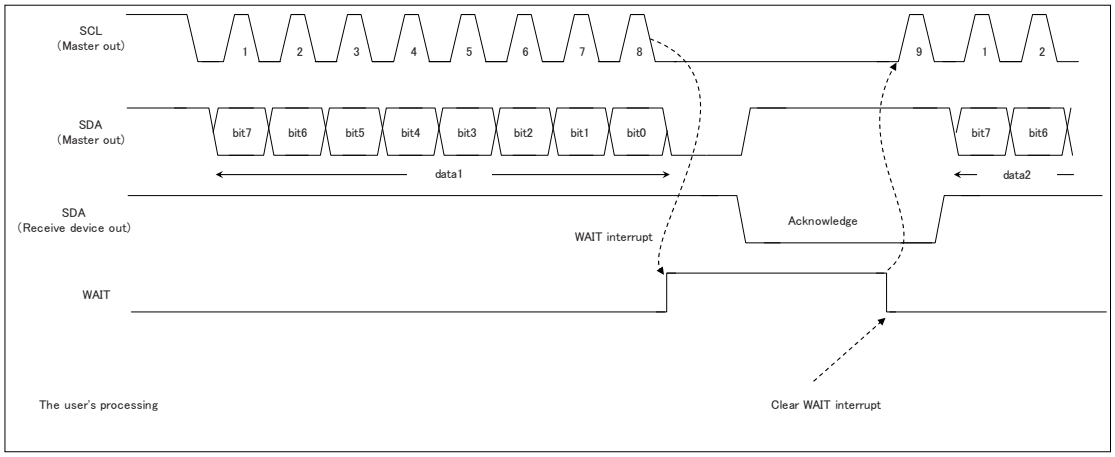


Figure 53.19 Example of Wait Operation Timing

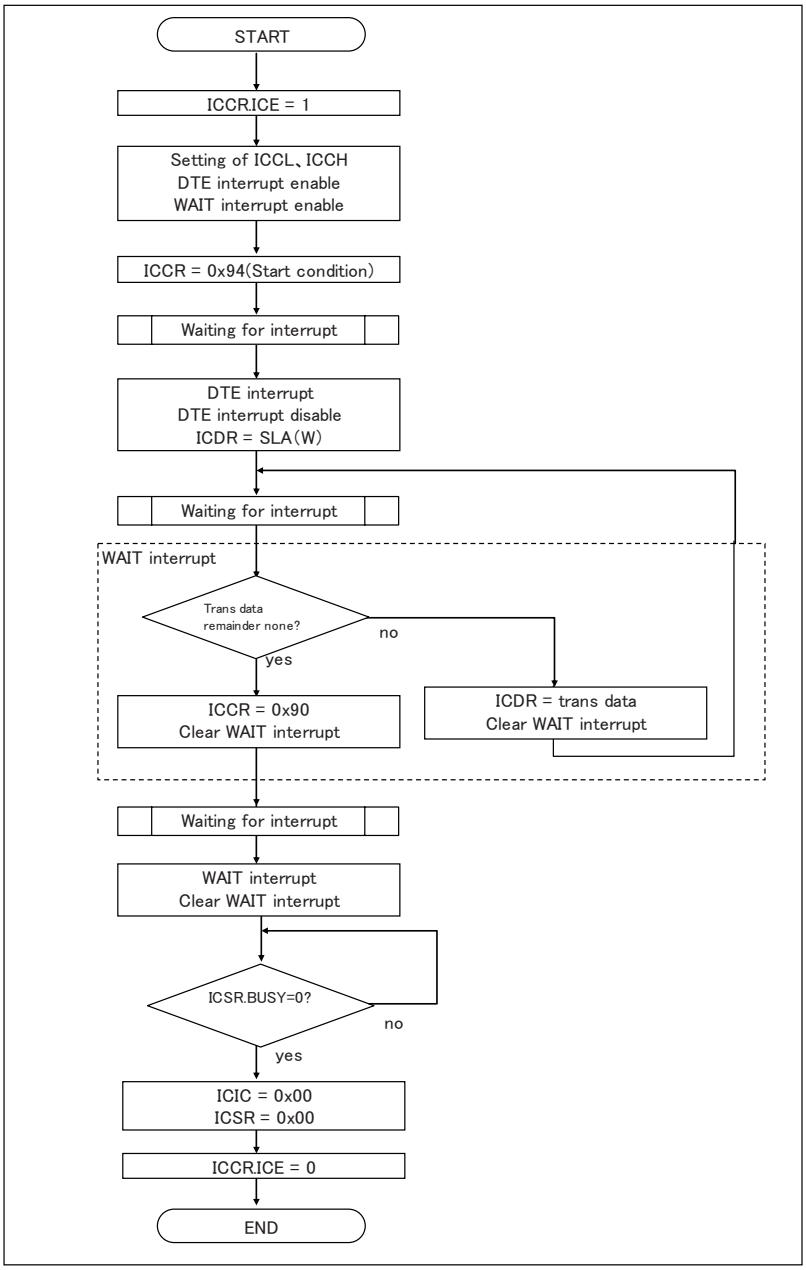


Figure 53.20 An Example of Software Flow for Transmission when Using Waits

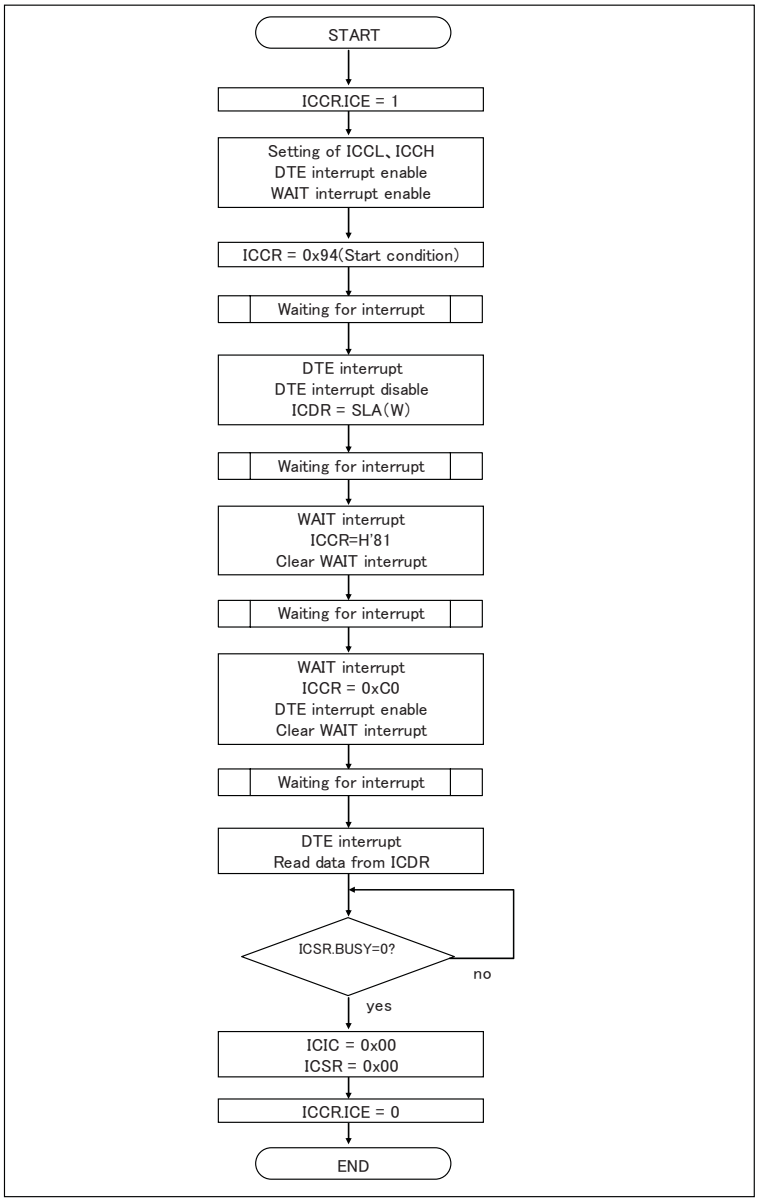


Figure 53.21 An Example of Software Flow for 1-Byte Write/1-Byte Read when Using Waits

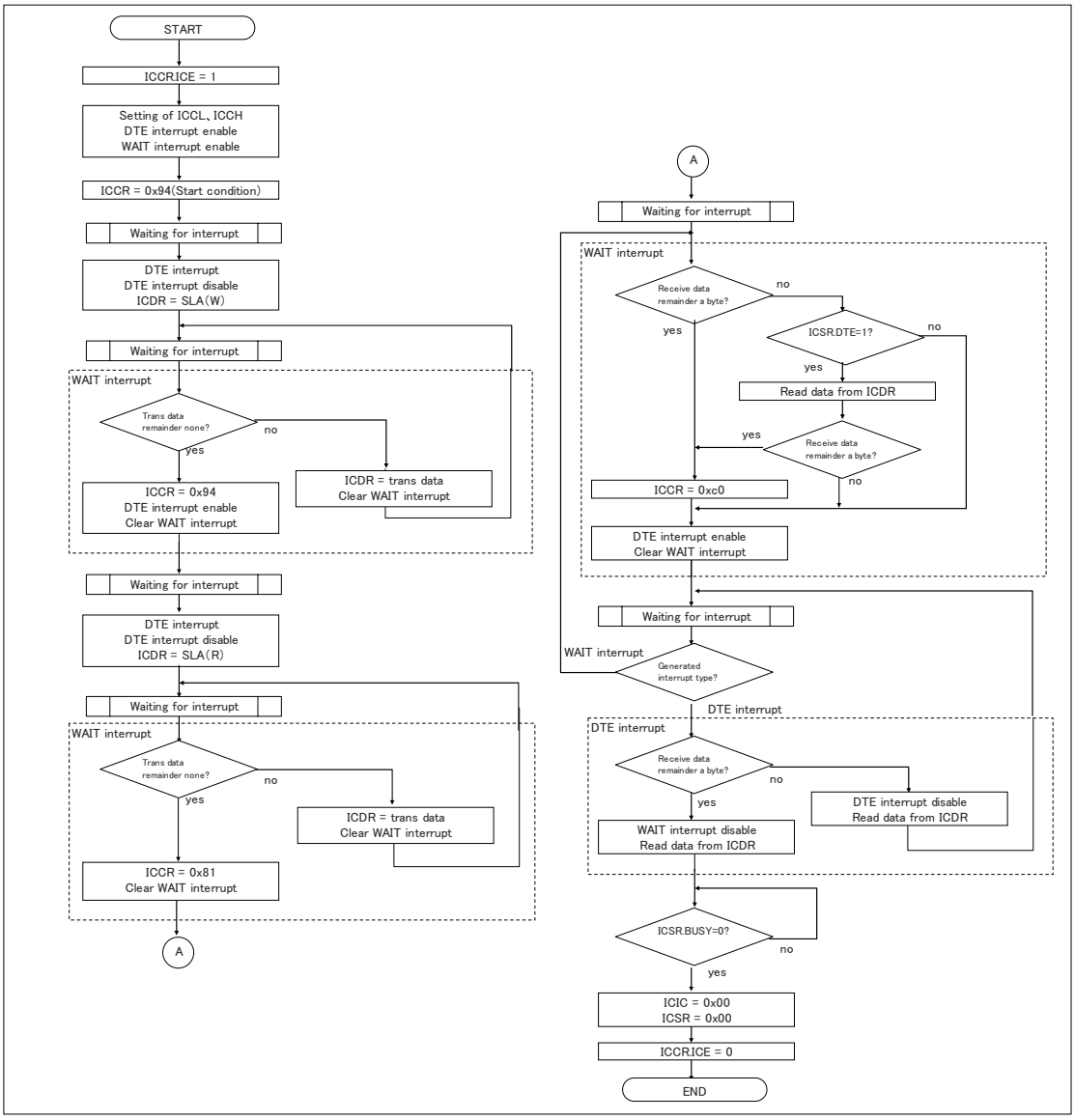


Figure 53.22 An Example of Software Flow for n-Byte Write/n-Byte Read when Using Waits

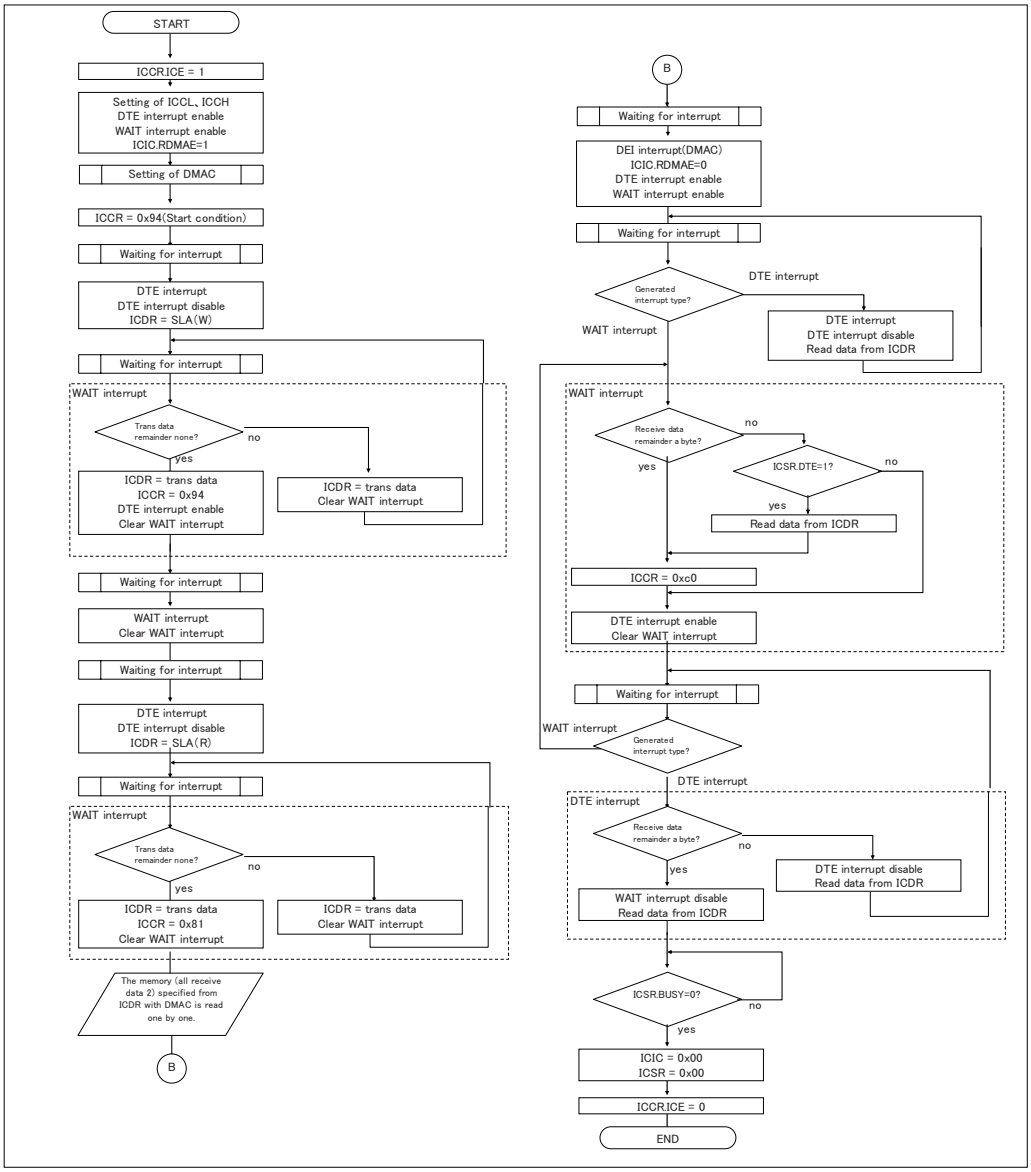


Figure 53.23 An Example of Software Flow for DMA Reception when Using Waits (WAIT = 1)

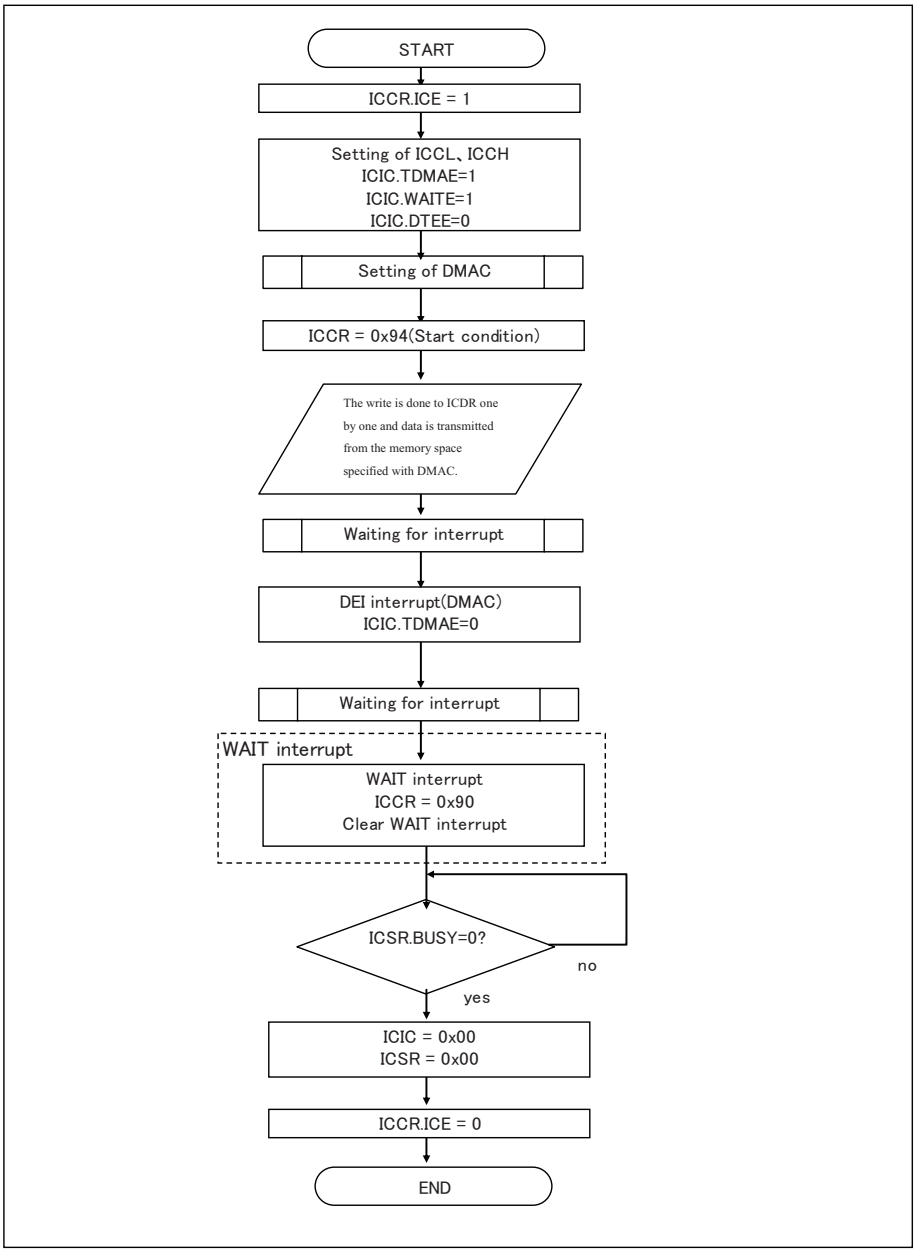


Figure 53.24 An Example of Software Flow for DMA Transmission when Using Waits

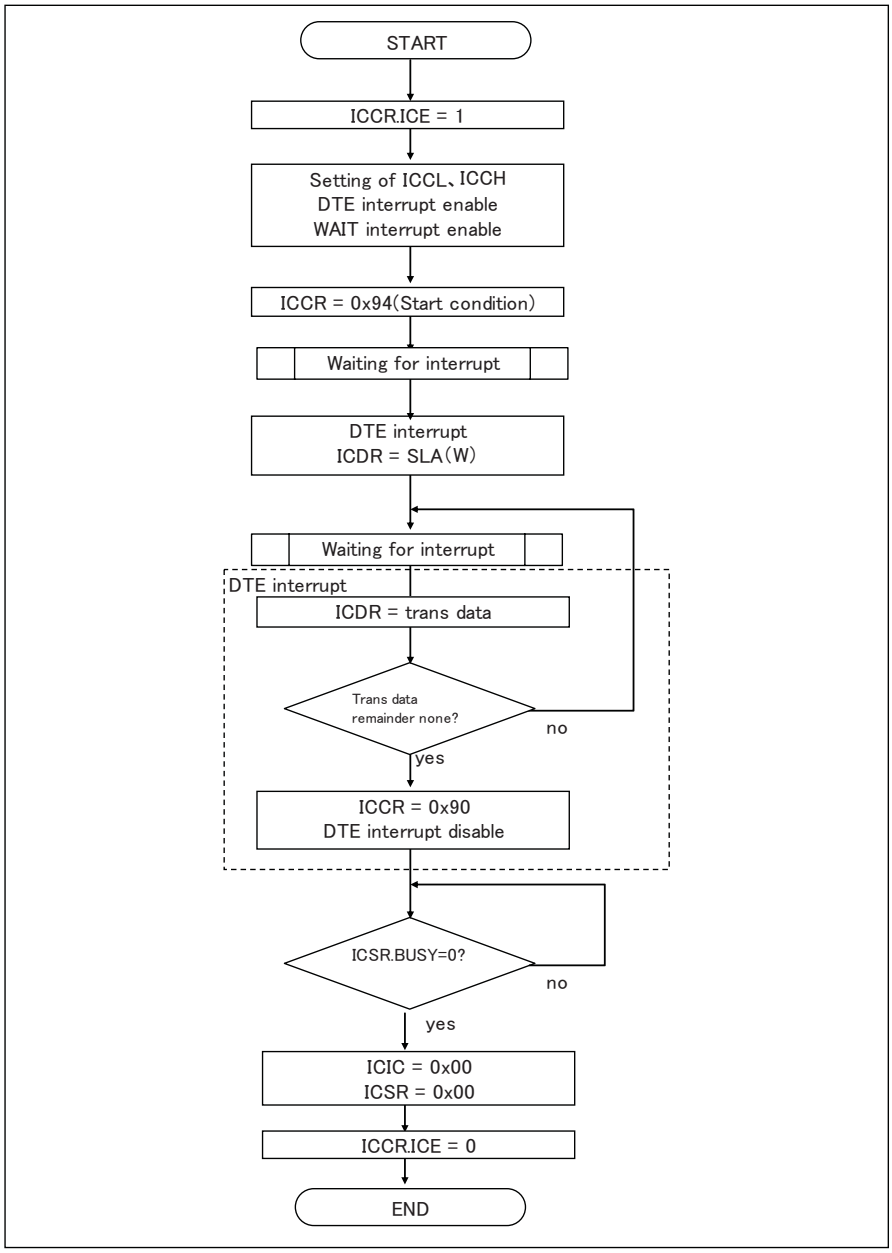


Figure 53.25 An Example of Software Flow for DMA Transmission without Waits

53.4.11 I²C automatic transmission with HS transmission

This I²C is carrying out a register setup of a communication format and several transceiver data minutes beforehand at the time of HS transmission use, transmitting without passing interruption processing until it publishes interruption in the completion of communication, or a communication error henceforth it can do. The communication format and function-settings procedure which are used by automatic transmission are shown in Table 53.7.

The example of a flow of operation at the time of I²C automatic transmission is shown in Fig. 53.26.

Table 53.7 Soft processing at the time of I²C automatic transmission use

I²C use conditions of communication	Use		Hs transmission mode on automatic trans
	Communication format	0	The communication format is selected.
		1	
		2	
		3	Refer to Figure 53.7 for a detailed format.
		4	
		5	
	Interrupt	AEND	○
		TMOUT	○
		AL	○
		TACK	○
	DMA		Select DMA use or not
	Hs transmission mode		○
Register setting procedure before it begins to communicate	ICCR(possible to omit it)	W	0x80
	ICTMC1	W	0x01～0xFF/unnecessary
	ICTMC2	W	0x01～0xFF/unnecessary
	ICTMCW	W	0x01～0xFF/unnecessary
	ICCL	W	0x0A～0xFE
	ICCH	W	0x0A～0xFE
	ICIC	W	0b**001111
	ICHL	W	0x01～0xFE
	ICHH	W	0x01～0xFE
	ICHMCODE	W	Master code

	ICACE	W	0b1**111*0
	ICIMSK	W	0xFC
	ICATFR	W	0x0*～0x5*
	ICVCON	W	0x80
	ICATSET0	W	trans1's trans times
	ICATSET1	W	trans2's trans times/unnecessary
	ICARSET0	W	receive1's receive time/unnecessary
	ICARSET1	W	receive2's receive time/unnecessary
	ICATD00～09	W	SLA and data for trans
	ICATD10～19	W	SLA and data for trans
	ICASTART	W	0x80or81or82or83
Procedure of register setting after communication is completed	ICARD00～09	R	Receive data
	ICARD10～19	R	Receive data
	ICCR	W	0x00

[Note] "*" in front should set up by combining with an operating condition.

"SLA and data" in front, and "receiving data" are applicable registers when performing communication which uses a data register. A write or read is required.

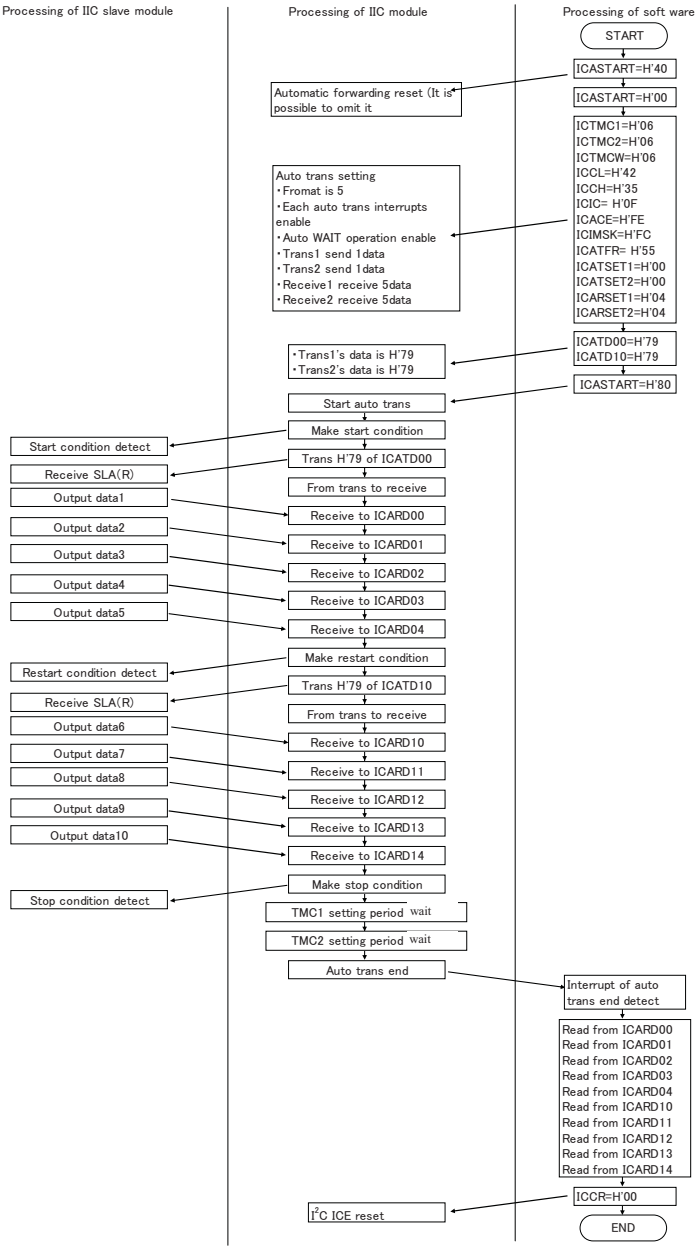


Figure 53.26 Example of an automatic transmission flow at the time of I²C Hs transmission use

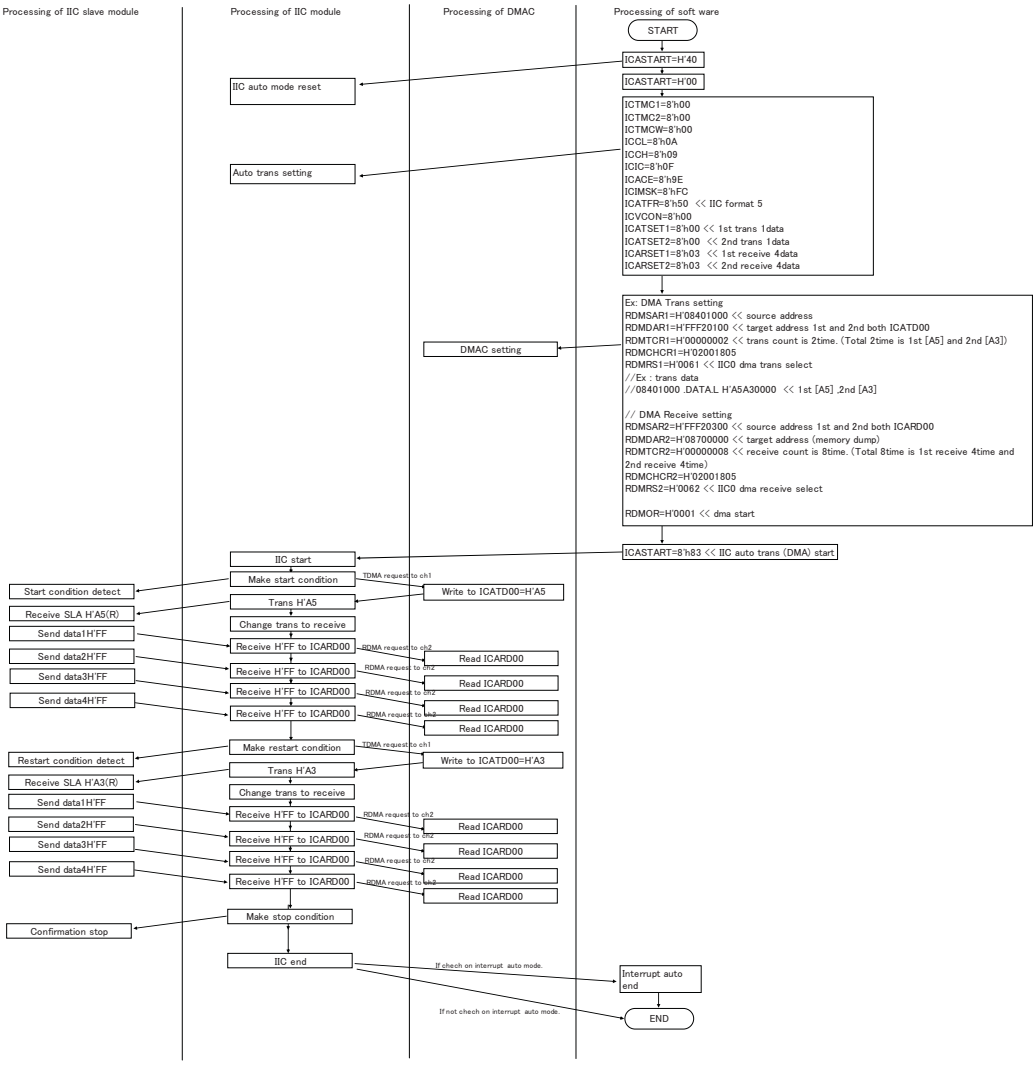


Figure 53. 27 Example of an automatic transmission flow at the time of I²C Hs transmission use (at the time of DMA use)

53.4.12 I²C HighSpeed transmission

I²C corresponds to HS transmission to less than SCL 2MHz in a HighSpeed (HS) format. (It is I^2 C2 and I^2 C3 and I^2 C4)

Automatic transmission is used in order to perform HS transmission.

The communication format which can be used by HS transmission is a figure. 53.7 Soft processing of HS transmission are shown in Table 53.7.

The flow of HS transmission of operation is explained below.

If it sets to HS transmission and an automatic transmission start is carried out, I²C will transmit 1 byte of master code (B'00001XXX) by a standard or high-speed transmission. ICCL and an ICCH register value are respectively reflected the Low period of SCL at this time, and during the High. Although one set of ACK bits after master code transmission are carried out, they do not perform TACK detection.

TACK detection is performed in the ACK bit under HS transmission.

I²C generates resending conditions and starts HS transmission. ICHL and an ICHH register value are respectively reflected the Low period of SCL at this time, and during the High.

I²C communication is performed along with the communication format set as the ICATFR register, and publish stop, end of automatic transmission, or communication error interruption after condition precedent generation henceforth.

AL detection is not performed during HS transmission. Only the period to the standup of communication of SCL of ACK bit falling to the next is possible for SCL synchronous processing. The slave device can carry out the Low drive of the SCL, and can carry out wait of the following processing to this period.

The timing chart of HS transmission and the existence of the function under transmission are shown in Fig. 53.26.

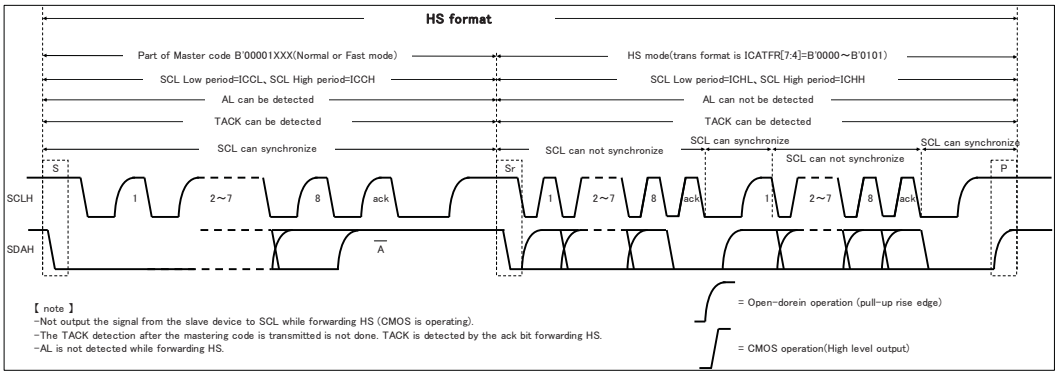


Figure 53.28 The timing chart of I²C HS transmission, and function under transmission

53.5 Usage Notes

(1) Arbitration Lost

A bus may not be released depending on the state of the slave device when arbitration lost is detected.

When resuming the communication after an arbitration lost, the initialization by the ICE bit in ICCR is required to initialize the entire internal data.

(2) ICE Reset

The SCL clock stops immediately after ICE is reset during data transmission. Therefore, a bus may not be released depending on the state of the slave device.

(3) Processing Concerning Stop Condition Generation

When data is transmitted or received after a stop condition has been issued and generated, it may not be possible to generate a stop condition hereafter. Be sure to initialize all registers in the I²C module by clearing the ICE bit in ICCR to 0 after a stop condition has been generated or before making settings to trigger data transmission or reception after a stop condition has been generated.

(4) What to do when the I²C Bus Interface is not Used

Set the ICE bit in ICCR to 0 to disable the unused channels while the I²C bus interface is not used.

(5) It is about an end by the middle about communication of I²C.

It becomes impossible to communicate in an original I²C format by end on the way. When an end is used on the way,

Please check not malfunctioning, even if the end of communication is carried out in the form where the slave side differs from a communication format.

Section 54 Key Scan Interface (KEYSC)

This LSI has a key scan interface (KEYSC) that can set the input or output bit numbers to be programmable.

54.1 Features

- Mounted in the common domain
- On-chip chattering elimination circuit (Chattering elimination time can be set to be programmable)
- Measures to deal with multiple key presses (There is a restriction.)
- Level/edge-selectable internal interrupts
- Auto key scan is controllable
- Input or output bit numbers can be set to be programmable (maximum KEYIN7 to KEYIN0 and KEYOUT7 to KEYOUT0)
- KEYSC can be set as source of power wakeup

Figure 54.1 shows a block diagram of the key scan interface and represents the form of the key pin mode 6 (KEYIN7 to KEYIN0 and KEYOUT7 to KEYOUT0).

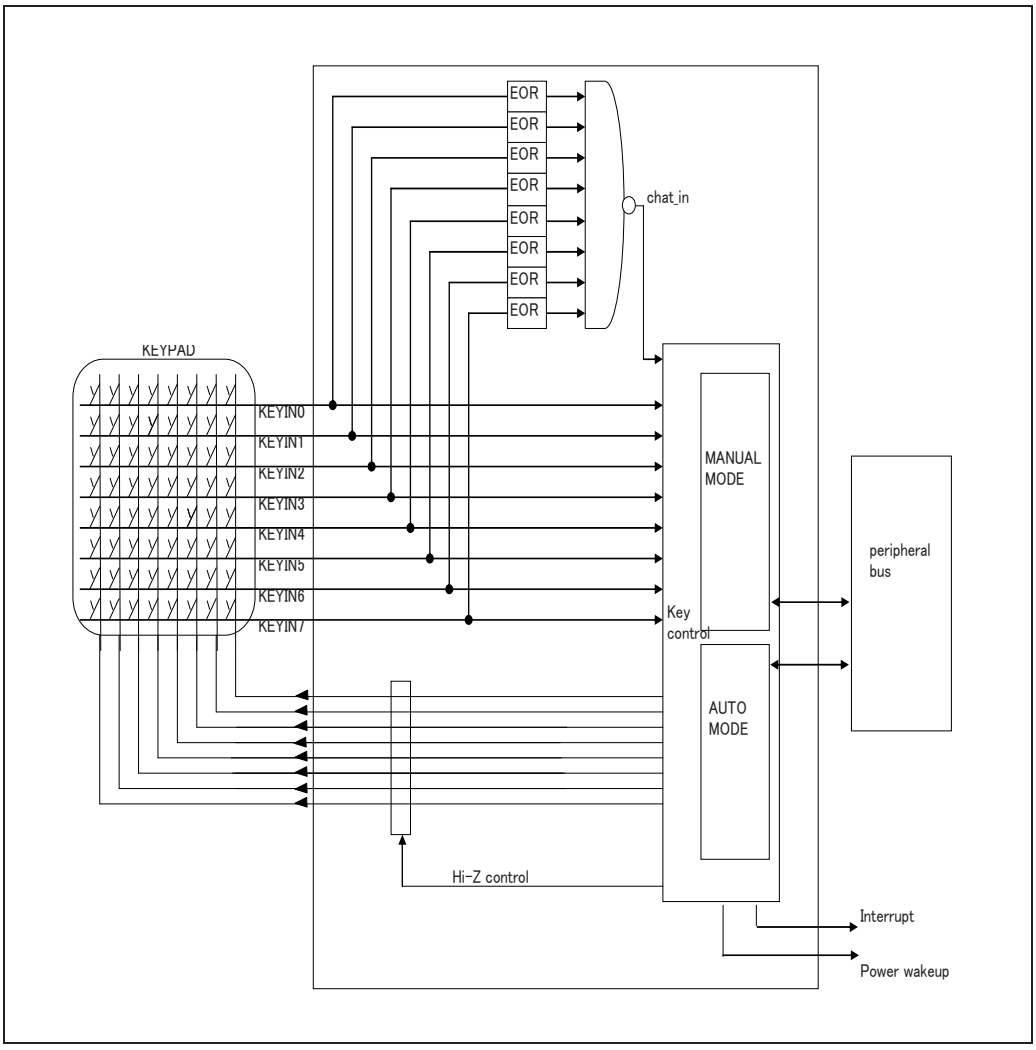


Figure 54.1 Block Diagram of Key Scan Interface (Key Pin Mode 6)

Note: The pull-up is done by GPIO setting.

54.2 Input/Output Pins

The pin configuration of the key scan interface is listed in table 54.1.

Table 54.1 Pin Configuration

Pin Name	Function	I/O	Description
KEYIN7 to KEYIN0	Input key scan interfaces 7 to 0	Input	Key scan interface for input
KEYOUT7 to KEYOUT0	Output key scan interfaces 7 to 0	Output	Key scan interface for output

54.3 Register Descriptions

Table 54.2 shows the KEYSC register configuration. Table 54.3 shows the register states in each operating mode.

Table 54.2 Register Configuration

Register Name	Abbreviation	R/W	Address*	Access Size
Manual key scan control register 1	M_KYCR1	R/W	H'E61B 0000 H'E71B 0000	16
Manual key scan control register 2	M_KYCR2	R/W	H'E61B 0004 H'E71B 0004	16
Manual key scan-in data register	M_KYINDR	R	H'E61B 0008 H'E71B 0008	16
Manual key scan-out data register	M_KYOUTDR	R/W	H'E61B 000C H'E71B 000C	16
Auto key scan control register 1	A_KYCR1	R/W	H’E61B0010 H’E71B0010	16
Auto key scan control register 2	A_KYCR2	R/W	H’E61B0014 H’E71B0014	16
Auto key scan control register 4	A_KYCR4	R/W	H’E61B001C H’E71B001C	16
Auto key scan control register 6	A_KYCR6	R/W	H’E61B0024 H’E71B0024	16
Auto key scan interrupt control register	A_KYIR	R/W	H’E61B0030 H’E71B0030	32
Auto key scan status register	A_KYSR	R/W	H’E61B0034 H’E71B0034	32
Auto key scan-in data register	A_KYINDR	R	H’E61B0038 H’E71B0038	16
Auto key scan-out data register	A_KYOUTDR	R/W	H’E61B003C H’E71B003C	16
Auto key scan data register L	A_KYSCDRL	R	H’E61B0040 H’E71B0040	32
Auto key scan data register H	A_KYSCDRH	R	H’E61B0044 H’E71B0044	32
Auto key scan data-touch register L	A_KYSCDTRL	R	H’E61B0048 H’E61B0048	32
Auto key scan data-touch register H	A_KYSCDTRH	R	H’E61B004C H’E71B004C	32

Auto key scan data-release register L	A_KYSCDRRL	R	H'E61B0050 H'E71B0050	32
Auto key scan data-release register H	A_KYSCDRRH	R	H'E61B0054 H'E71B0054	32
Auto key scan data-count register	A_KYSCDNUM	R/W	H'E61B0060 H'E71B0060	32

Note: * These registers can be accessed from both HPBC area (H'E6xx xxxx) and HPBD area (H'E7xx xxxx).

Table 54.3 Register States in Each Operating Mode

Register Abbreviation	Reset *1	Module Standby
M_KYCR1	Initialized	Retained
M_KYCR2	Initialized*2	Retained
M_KYINDR	Initialized	Retained
M_KYOUTDR	Initialized	Retained
A_KYCR1	Initialized	Retained
A_KYCR2	Initialized	Retained
A_KYCR4	Initialized	Retained
A_KYCR6	Initialized	Retained
A_KYIR	Initialized	Retained
A_KYSR	Initialized	Retained
A_KYINDR	Initialized	Retained
A_KYOUTDR	Initialized	Retained
A_KYSCDRL	Initialized	Retained
A_KYSCDRH	Initialized	Retained
A_KYSCDTRL	Initialized	Retained
A_KYSCDTRH	Initialized	Retained
A_KYSCDRRL	Initialized	Retained
A_KYSCDRRH	Initialized	Retained
A_KYSCDNUM	Initialized	Retained

Note: *1 For details, refer to section 1-D Overview of reset.
*2 The value of bit KEYIF is undefined.

54.3.1 Manual key Scan Control Register 1 (M_KYCR1)

M_KYCR1 is a 16-bit readable/writable register that selects the functions of the key scan interface.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	KYMD[2:0]			KYOUT_IE	—	—	—	—	SCN[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 8	KYMD[2:0]	000	R/W	Key Pin Mode Set the KEYIN/KEYOUT pin to be used. 000: Use key pin mode 1 (KEYIN4 to KEYIN0 and KEYOUT5 to KEYOUT0 are available) 001: Use key pin mode 2 (KEYIN5 to KEYIN0 and KEYOUT4 to KEYOUT0 are available) 010: Use key pin mode 3 (KEYIN6 to KEYIN0 and KEYOUT3 to KEYOUT0 are available) 011: Use key pin mode 4 (KEYIN5 to KEYIN0 and KEYOUT5 to KEYOUT0 are available) 100: Use key pin mode 5 (KEYIN6 to KEYIN0 and KEYOUT5 to KEYOUT0 are available) 101: Use key pin mode 6 (KEYIN7 to KEYIN0 and KEYOUT7 to KEYOUT0 are available) 110: Setting prohibited 111: Setting prohibited
7	KYOUT_IE	0	R/W	Key Scan Standby Mode Cancel Enable When various standby modes are canceled by the key input, this bit should be set to 1. 0: Disables various standby modes to be canceled by the key input. 1: Enables various standby modes to be canceled by the key input.

Bit	Bit Name	Initial Value	R/W	Description
6 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2 to 0	SCN[2:0]	000	R/W	Scan Timing Specify the chattering elimination time for the interrupt detection of the key scan interface. 000: RCLK/16 (0.49 ms) 001: RCLK/32 (0.98 ms) 010: RCLK/64 (1.95 ms) 011: RCLK/128 (3.91 ms) 100: RCLK/256 (7.81 ms) 101: RCLK/512 (15.63 ms) 110: RCLK/1024 (31.25 ms) 111: Chattering elimination circuit is invalid Note: To detect power wakeup operation in edge setting of KEY detect interrupt, It is necessary to do the chattering elimination setting besides 3'b111.

54.3.2 Manual key Scan Control Register 2 (M_KYCR2)

M_KYCR2 is a 16-bit readable/writable register that selects the functions of the key scan interface.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	KYDIR7	KYDIR6	KYDIR5	KYDIR4	KYDIR3	KYDIR2	KYDIR1	KYDIR0	–	–	KYCPU.IE [1:0]		–	–	–	KEYIF
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	–
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	KYDIR7	0	R/W	Key Direction 7 The EOR result of the KEYIN7 pin and this bit is used to detect a KEYIN7 interrupt. Note: Values written at setting key pin modes 1 to 5 are ignored.
14	KYDIR6	0	R/W	Key Direction 6 The EOR result of the KEYIN6 pin and this bit is used to detect a KEYIN6 interrupt. Note: Values written at setting key pin modes 1, 2, and 4 are ignored.

Bit	Bit Name	Initial Value	R/W	Description
13	KYDIR5	0	R/W	Key Direction 5 The EOR result of the KEYIN5 pin and this bit is used to detect a KEYIN5 interrupt. Note: Values written at setting key pin mode 1 are ignored.
12	KYDIR4	0	R/W	Key Direction 4 The EOR result of the KEYIN4 pin and this bit is used to detect a KEYIN4 interrupt.
11	KYDIR3	0	R/W	Key Direction 3 The EOR result of the KEYIN3 pin and this bit is used to detect a KEYIN3 interrupt.
10	KYDIR2	0	R/W	Key Direction 2 The EOR result of the KEYIN2 pin and this bit is used to detect a KEYIN2 interrupt.
9	KYDIR1	0	R/W	Key Direction 1 The EOR result of the KEYIN1 pin and this bit is used to detect a KEYIN1 interrupt.
8	KYDIR0	0	R/W	Key Direction 0 The EOR result of the KEYIN0 pin and this bit is used to detect a KEYIN0 interrupt.
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5, 4	KYCPU_IE [1:0]	00	R/W	Key Internal Interrupt Enable Enable or disable internal interrupt requests to the CPU when there is key input. 00: Key interrupt requests disabled 01: Key interrupt requests enabled (level) 10: Key interrupt requests enabled (rising edge) 11: Key interrupt requests enabled (falling edge) Note: Detect point is chat_in of figure 54.1

Bit	Bit Name	Initial Value	R/W	Description
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	KEYIF	Undefined (value before reset is retained)	R/W	Key Interrupt This flag is set when a key internal interrupt occurs. While this flag is 1, an internal interrupt request is sent to the CPU. (Only when M_KYCR2.KEYCPU_IE is set as rising edge and falling edge, It is held at 1 until overwritten by 0.) 0: No key interrupt occurs 1: A key interrupt occurs*

Note: * Case of level interrupts: When there is even one instance in which the result of the exclusive OR (EOR) of the KEYIN7 to KEYIN0 and the KYDIR7 to KYDIR0, respectively, is 0.

54.3.3 Manual key Scan-In Data Register (M_KYINDR)

M_KYINDR is a 16-bit read-only register that stores the data of pins KEYIN7 to KEYIN0. Bits KYI7DT to KYI0DT correspond respectively to pins KEYIN7to KEYIN0.

In order to use the key scan interface functions, the pin function controller should be used to set the pin function settings to the key scan interface pin side. Pins KEYIN7 to KEYIN0 are pulled-up in the internal LSI.

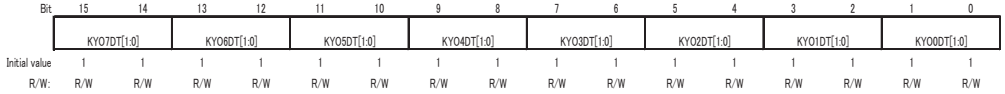
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	KYI7DT	KYI6DT	KYI5DT	KYI4DT	KYI3DT	KYI2DT	KYI1DT	KYI0DT
Initial value	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 8	—	All 0	R	Reserved These bits are always read as 0.
7	KYI7DT	0	R	State of Pin KEYIN7 (1 at high or 0 at low) Note: This bit is always read as 0 in key pin modes 1 to 5.
6	KYI6DT	0	R	State of Pin KEYIN6 (1 at high or 0 at low) Note: This bit is always read as 0 in key pin modes 1, 2, and 4.
5	KYI5DT	0	R	State of Pin KEYIN5 (1 at high or 0 at low) Note: This bit is always read as 0 in key pin mode 1.
4	KYI4DT	1	R	State of Pin KEYIN4 (1 at high or 0 at low)
3	KYI3DT	1	R	State of Pin KEYIN3 (1 at high or 0 at low)
2	KYI2DT	1	R	State of Pin KEYIN2 (1 at high or 0 at low)
1	KYI1DT	1	R	State of Pin KEYIN1 (1 at high or 0 at low)
0	KYI0DT	1	R	State of Pin KEYIN0 (1 at high or 0 at low)

54.3.4 Manual key Scan-Out Data Register (M_KYOUTDR)

M_KYOUTDR is a 16-bit readable/writable register that stores the output data for pins KEYOUT7 to KEYOUT0. Bits KYO7DT to KYO0DT correspond respectively to pins KEYOUT7 to KEYOUT0.

In order to use the key scan interface functions, the pin function controller should be used to set the pin function settings to the key scan interface pin side.



Bit	Bit Name	Initial Value	R/W	Description
15, 14	KYO7DT[1:0]	11	R/W	KYOnDT: Control output data of pin KEYOUTn. (n = 0 to 7) 00: Low-level output 01: High-level output 10: High-impedance state 11: High-impedance state Note: KYO7DT: Values written at setting key pin mode 1 to 5 are ignored. KYO6DT: Values written at setting key pin mode 1 to 5 are ignored. KYO5DT: Values written at setting key pin mode 2 and key pin mode 3 are ignored. KYO4DT: Values written at setting key pin mode 3 are ignored.
13, 12	KYO6DT[1:0]	11	R/W	
11, 10	KYO5DT[1:0]	11	R/W	
9, 8	KYO4DT[1:0]	11	R/W	
7, 6	KYO3DT[1:0]	11	R/W	
5, 4	KYO2DT[1:0]	11	R/W	
3, 2	KYO1DT[1:0]	11	R/W	
1, 0	KYO0DT[1:0]	11	R/W	

54.3.5 Auto key Scan control register 1(A_KYCR1)

A_KYCR1 is a 16-bit readable/writable register that selects the functions of the key scan interface.

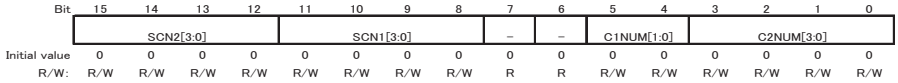
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	KEYEXT	–	–	–	–	KYMD[2:0]			–	–	–	MASK VALUE	–	SCN0[2:0]		
Initial value	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
R/W:	R/W	R	R	R	R	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	KEYEXT	0	R/W	KEY module operation mode can be set 0:MANUAL mode M_register-name can be used 1:AUTO mode A_register-name can be used
14 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 8	KYMD[2:0]	All 0	R/W	KEY pin mode Set the KEYIN/KEYOUT pin to be used. 000: Use key pin mode 1 (KEYIN4 to KEYIN0 and KEYOUT5 to KEYOUT0 are available) 001: Use key pin mode 2 (KEYIN5 to KEYIN0 and KEYOUT4 to KEYOUT0 are available) 010: Use key pin mode 3 (KEYIN6 to KEYIN0 and KEYOUT3 to KEYOUT0 are available) 011: Use key pin mode 4 (KEYIN5 to KEYIN0 and KEYOUT5 to KEYOUT0 are available) 100: Use key pin mode 5 (KEYIN6 to KEYIN0 and KEYOUT5 to KEYOUT0 are available) 101: Use key pin mode 6 (KEYIN7 to KEYIN0 and KEYOUT7 to KEYOUT0 are available)

				110: Setting prohibited 111: Setting prohibited
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	MASK VALUE	1	R/W	This bit value is used to value of Unused key pin.
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2 to 0	SCN0[2:0]	000	R/W	Scan Timing 0 Specify the chattering elimination time for the the key scan interface. 000: RCLK/16 (0.49 ms) 001: RCLK/32 (0.98 ms) 010: RCLK/64 (1.95 ms) 011: RCLK/128 (3.91 ms) 100: RCLK/256 (7.81 ms) 101: RCLK/512 (15.63 ms) 110: RCLK/1024 (31.25 ms) 111: Chattering elimination circuit is invalid Note: To detect power wakeup operation in edge setting of KEY detect interrupt, It is necessary to do the chattering elimination setting besides 3'b111.

54.3.6 Auto key Scan control register 2(A_KYCR2)

A_KYCR2 is a 32-bit readable/writable register that set the each timing.



Bit	Bit Name	Initial Value	R/W	Description
15 to 12	SCN2[3:0]	0000	R/W	Scan timing 2 Specify the wait timing at key scan. 0000: RCLK/16 (0.49ms) 0001: RCLK/32 (0.98ms) 0010: RCLK/64 (1.95ms) 0011: RCLK/128 (3.91ms) 0100: RCLK/256 (7.81ms) 0101: RCLK/512 (15.63ms) 0110: RCLK/1024 (31.25ms) 0111: RCLK/2048 (62.5ms) 1000: RCLK/4096 (125ms) 1001: RCLK/8192 (250ms) 1010: RCLK/16384 (500ms) 1011: RCLK/32768 (1s)
11 to 8	SCN1[3:0]	0000	R/W	Scan timing 1 Specify the measure timing per KEYOUT pin at AUTO KEY SCAN. It is time from setting KEYOUT to reading KEYIN. 0000: RCLK (30.5us) 0001: RCLK/2 (61.0us) ~ 1111: RCLK/16 (488us)

7 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5 to 4	C1NUM[1:0]	All 0	R/W	When key data after AUTO KEY SCAN is same as this bits value times, it is used as temporary valid key data. 00: 1 times 01: 2 times 10: 3 times 11: 4 times
3 to 0	C2NUM[3:0]	All 0	R/W	When temporary valid key data is different from last valid key data and temporary valid key data is same as this bits value times, it is used as valid key data. 0000: setting prohibited 0001: 1 times ~ 1111: 15 times

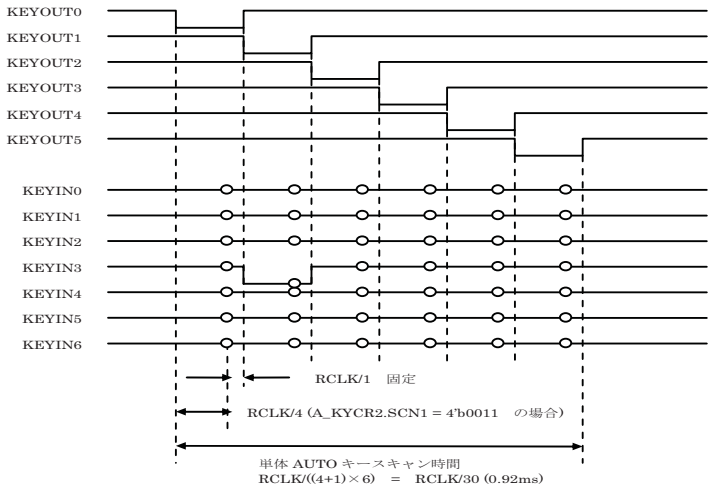


Figure 54.2 example of AUTO KEY SCAN TIMING

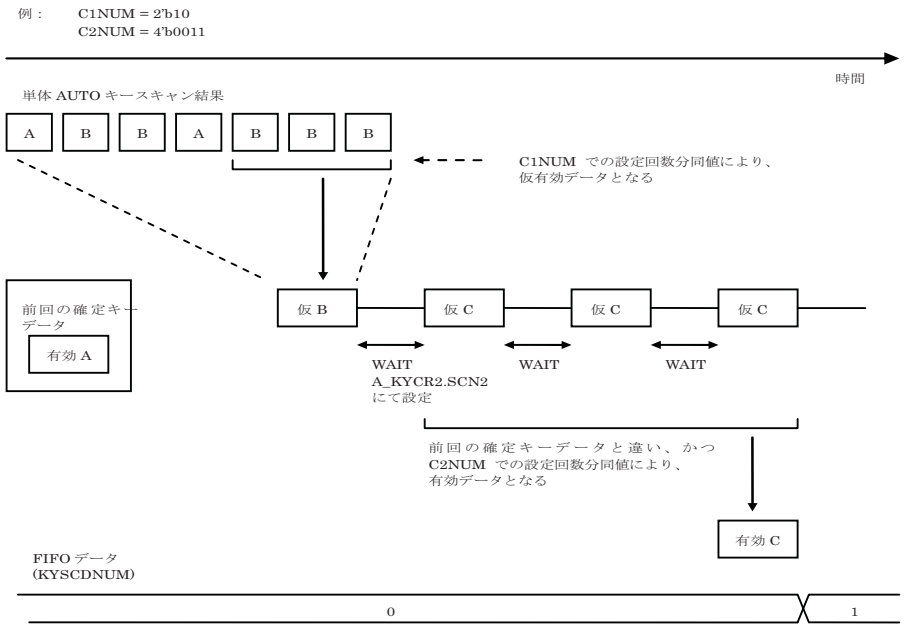


Figure 54.3 Flow until fixing valid data

54.3.7 Auto key Scan control register 4(A_KYCR4)

A_KYCR4 is a 16-bit readable/writable register that selects the functions of the key scan interface.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	NOFIFO	–	AUTO LPSC	–	AUTOKS
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R/W	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 5	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.

4	NOFIFO	0	R/W	Disable FIFO of Key scan data 0:FIFO enable 1:FIFO disable When this bit is 1 and valid data is acquired, A_KYSCFRH/A_KYSCDRL is always updated.
3	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	AUTOLPC	0	R/W	AUTO Key scan loop enable When this bit is written 1, until key is released, valid key data is acquired after key is detected.
1	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
0	AUTOKS	0	R/W	AUTO key scan enable When this bit is written 1, valid key data is acquired only once.

Note: Don't write 1 to both AUTOLPC and AUTOKS at same time.

54.3.8 Auto key Scan control register 6(A_KYCR6)

A_KYCR6 is a 16-bit readable/writable register that selects the functions of the key scan interface.

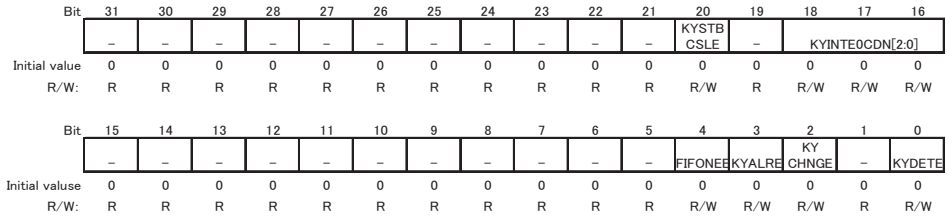
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	KY DIR7	KY DIR6	KY DIR5	KY DIR4	KY DIR3	KY DIR2	KY DIR1	KY DIR0	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description

15	KYDIR7	0	R/W	KEY Direction 7 The EOR result of the KEYIN7 pin and this bit is used to detect a KEYIN7 interrupt. Note: Values written at setting key pin modes 1 to 5 are ignored.
14	KYDIR6	0	R/W	KEY Direction 6 The EOR result of the KEYIN6 pin and this bit is used to detect a KEYIN6 interrupt. Note: Values written at setting key pin modes 1, 2, and 4 are ignored.
13	KYDIR5	0	R/W	KEY Direction 5 The EOR result of the KEYIN5 pin and this bit is used to detect a KEYIN5 interrupt. Note: Values written at setting key pin modes 1 are ignored.
12	KYDIR4	0	R/W	KEY Direction 4 The EOR result of the KEYIN4 pin and this bit is used to detect a KEYIN4 interrupt.
11	KYDIR3	0	R/W	KEY Direction 3 The EOR result of the KEYIN3 pin and this bit is used to detect a KEYIN3 interrupt.
10	KYDIR2	0	R/W	KEY Direction 2 The EOR result of the KEYIN2 pin and this bit is used to detect a KEYIN2 interrupt.
9	KYDIR1	0	R/W	KEY Direction 1 The EOR result of the KEYIN1 pin and this bit is used to detect a KEYIN1 interrupt.
8	KYDIR0	0	R/W	KEY Direction 0 The EOR result of the KEYIN0 pin and this bit is used to detect a KEYIN0 interrupt.

7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

54.3.9 Auto key scan interrupt control register (A_KYIR)



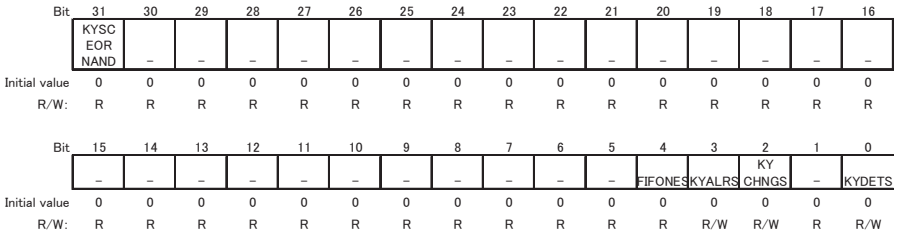
A_KYIR is a 32-bit readable/writable register that selects the functions related to interrupt.

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	KYSTB CSLE	0	R/W	Power wakeup enable When power wakeup is canceled by the key input, this bit should be set to 1. 0: Disables power wakeup to be canceled by the key input. 1: Enables power wakeup to be canceled by the key input.
19	—	0	R	Reserved These bits are always read as 0. The write value

				should always be 0.
18 to 16	KYINTE 0CDN[2: 0]	000	R/W	Condition of KEY detect interrupt Indicate condition of KEY detection 000: Key detect requests disabled 001: Key detect request enabled(level) 010: Key detect request enabled(rising edge) 011:Key detect request enabled(falling edge) 100: Key detect request enabled(both edge) 101 to 111:Reserved
15 to 5	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	FIFONE E	0	R/W	FIFO NotEmpty interrupt enable 0: FIFO interrupt disabled 1: interrupt is enabled
3	KYALR E	0	R/W	KEY all-release interrupt enable 0: key definition interrupt disabled 1: key definition interrupt enabled
2	KYCHN GE	0	R/W	KEY change interrupt 0: KEY change interrupt disabled 1: KEY change interrupt enabled
1	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.

0	KYDETE	0	R/W	KEY detect interrupt 0: KEY detect interrupt disabled 1: KEY detect interrupt enabled

54.3.10 Auto key scan status register (A_KYSR)



A_KYSR is a 32-bit readable/writable register that represents interrupt status.

Bit	Bit Name	Initial Value	R/W	Description
31	KYSCEORNAND	All 0	R	Indicate Key detect result The write data should be always 0.
30 to 5	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	FIFONES	0	R	FIFONotEmpty 0:There is not data in FIFO 1:There is data in FIFO Although this bit can not be written, 1 is not recommended to be written. When A_KYCR4.NOFIFO is 1, this bit Always Display 0.

3	KYALRS	0	R/W	KEY all release 0: No KEY all release has been detected 1: KEY all release has been detected This bit can be cleared by written 0. 1 can not be written.
2	KYCHANGS	0	R/W	KEY change detect interrupt 0: No KEYSCAN change detect interrupt has been detected 1: KEYSCAN change detect interrupt has been detected This bit can be cleared by written 0. 1 can not be written.
1	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
0	KYDETS	0	R/W	KEY detect interrupt 0: No KEY detect interrupt has been detected 1: KEY detect interrupt has been detected This bet should be cleared by software, as long as A_HYIR.KYINTECDN[2:0] is rising edge, falling edge and both edge. This bit can be cleared by written 0. 1 can not be written.

54.3.11 Auto key scan-in data register (A_KYINDR)

A_KYINDR is a 16-bit read-only register that stores the data of pins KEYIN7 to KEYIN0. Bits KYI7DT to KYI0DT correspond respectively to pins KEYIN7 to KEYIN0.

In order to use the key scan interface functions, the pin function controller should be used to set the pin function settings to the key scan interface pin side. Pins KEYIN7 to KEYIN0 are pulled-up in the internal LSI.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	KYI7DT	KYI6DT	KYI5DT	KYI4DT	KYI3DT	KYI2DT	KYI1DT	KYI0DT
Initial value	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 8	—	All 0	R	Reserved These bits are always read as 0.
7	KYI7DT	1	R	State of Pin KEYIN7 (1 at high or 0 at low) Note: This bit is always read as value of A_KYCR1.MASKVALUE in key pin modes 1 to 5.
6	KYI6DT	1	R	State of Pin KEYIN6 (1 at high or 0 at low) Note: This bit is always read as value of A_KYCR1.MASKVALUE in key pin modes 1, 2, and 4.
5	KYI5DT	1	R	State of Pin KEYIN5 (1 at high or 0 at low) Note: This bit is always read as A_KYCR1.MASKVALUE in key pin mode 1.
4	KYI4DT	1	R	State of Pin KEYIN4 (1 at high or 0 at low)
3	KYI3DT	1	R	State of Pin KEYIN3 (1 at high or 0 at low)
2	KYI2DT	1	R	State of Pin KEYIN2 (1 at high or 0 at low)
1	KYI1DT	1	R	State of Pin KEYIN1 (1 at high or 0 at low)
0	KYI0DT	1	R	State of Pin KEYIN0 (1 at high or 0 at low)

54.3.12 Auto key Scan-Out Data Register (A_KYOUTDR)

A_KYOUTDR is a 16-bit readable/writable register that stores the output data for pins KEYOUT7 to KEYOUT0. Bits KYO7DT to KYO0DT correspond respectively to pins KEYOUT7 to KEYOUT0.

In order to use the key scan interface functions, the pin function controller should be used to set the pin function settings to the key scan interface pin side.

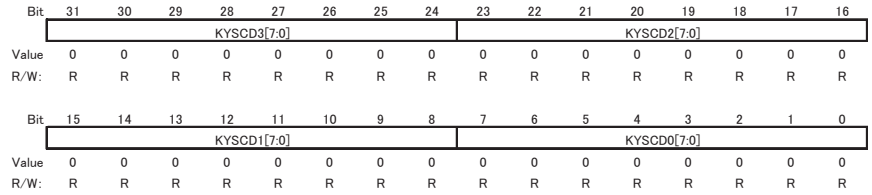
M_KYOUTDR



Bit	Bit Name	Initial Value	R/W	Description
15,14	KYO7DT[1:0]	11	R/W	KYOnDT: Control output data of pin KEYOUTn. (n = 0 to 7) 00: Low-level output 01: High-level output 10: High-impedance state 11: High-impedance state Note: value is reflected by all key mode.
13,12	KYO6DT[1:0]	11	R/W	
11, 10	KYO5DT[1:0]	11	R/W	
9, 8	KYO4DT[1:0]	11	R/W	
7, 6	KYO3DT[1:0]	11	R/W	
5, 4	KYO2DT[1:0]	11	R/W	
3, 2	KYO1DT[1:0]	11	R/W	
1, 0	KYO0DT[1:0]	11	R/W	

54.3.13 Auto key scan data register L (A_KYSCDRL)

A_KYOUTDR is a 32-bit read-only register that stores the scanned data of KEYOUT 3 to 0.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	KYSC3[7:0]	All 0	R	KYOUT3 scan data These bits store Inverted value of KEYIN7 to KEYIN0. Only KEYOUT3 is low level, and other KEYOUT is Hi-Z. Bit corresponding to place where key was pushed becomes 1.
23 to 16	KYSC2[7:0]	All 0	R	KYOUT2 scan data These bits store Inverted value of KEYIN7 to KEYIN0. Only KEYOUT2 is low level, and other KEYOUT is Hi-Z. Bit corresponding to place where key was pushed becomes 1.
15 to 8	KYSC1[7:0]	All 0	R	KYOUT1 scan data These bits store Inverted value of KEYIN7 to KEYIN0. Only KEYOUT1 is low level, and other KEYOUT is Hi-Z. Bit corresponding to place where key was pushed becomes 1.
7 to 0	KYSC1[7:0]	All 0	R	KYOUT0 scan data These bits store Inverted value of KEYIN7 to KEYIN0. Only KEYOUT0 is low level, and other KEYOUT is Hi-Z. Bit corresponding to place where key was pushed becomes 1.

54.3.14 Auto key scan data register H (A_KYSCDRH)

A_KYOUTDR is a 32-bit read-only register that stores the scanned data of KEYOUT 3 to 0.

Number of FIFO (KYSCDNUM) is reduced by reading this register.

Note: Read this register after reading A_KYSCDRL.

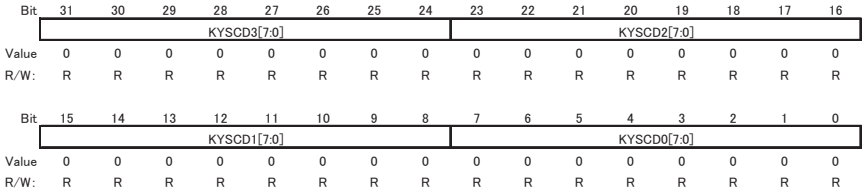
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	KYSCD7[7:0]								KYSCD6[7:0]							
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	KYSCD5[7:0]								KYSCD4[7:0]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	KYSC7[7:0]	All 0	R	KYOUT7 scan data These bits store Inverted value of KEYIN7 to KEYIN0. Only KEYOUT7 is low level, and other KEYOUT is Hi-Z. Bit corresponding to place where key was pushed becomes 1.
23 to 16	KYSC6[7:0]	All 0	R	KYOUT6 scan data These bits store Inverted value of KEYIN7 to KEYIN0. Only KEYOUT6 is low level, and other KEYOUT is Hi-Z. Bit corresponding to place where key was pushed becomes 1.
15 to 8	KYSC5[7:0]	All 0	R	KYOUT5 scan data These bits store Inverted value of KEYIN7 to KEYIN0. Only KEYOUT5 is low level, and other KEYOUT is Hi-Z. Bit corresponding to place where key was pushed becomes 1.
7 to 0	KYSC4[7:0]	All 0	R	KYOUT4 scan data These bits store Inverted value of KEYIN7 to KEYIN0. Only KEYOUT4 is low level, and other KEYOUT is Hi-Z. Bit corresponding to place where key was pushed becomes 1.

54.3.15 Auto key scan data-touch register L (A_KYSCDTRL)

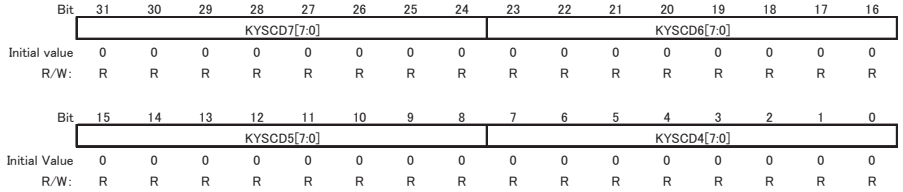
A_KYSCDTRL is a 32-bit read-only register. After data acquisition of KEYSCAN, compared with the last data, the bit corresponding to the key touch stores 1. In case of A_KYCR4.NOFIFO being 1'b0, this register is valid.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	KYSCD3[7:0]	All 0	R	KYOUT3 scan data After data acquisition of KEYOUT3, compared with the last data, the bit corresponding to the key touch stores 1.
23 to 16	KYSCD2[7:0]	All 0	R	KYOUT2 scan data After data acquisition of KEYOUT2, compared with the last data, the bit corresponding to the key touch stores 1.
15 to 8	KYSCD1[7:0]	All 0	R	KYOUT1 scan data After data acquisition of KEYOUT1, compared with the last data, the bit corresponding to the key touch stores 1.
7 to 0	KYSCD0[7:0]	All 0	R	KYOUT0 scan data After data acquisition of KEYOUT0, compared with the last data, the bit corresponding to the key touch stores 1.

54.3.16 Auto key scan data-touch register H (A_KYSCDTRH)

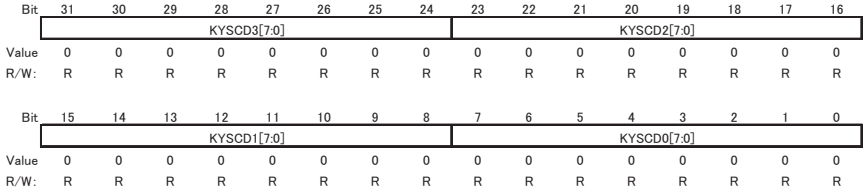
A_KYSCDTRH is a 32-bit read-only register. After data acquisition of KEYSCAN, compared with the last data, the bit corresponding to the key touch stores 1. In case of A_KYCR4.NOFIFO being 1'b0, this register is valid.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	KYSC7[7:0]	All 0	R	KYOUT7 scan data After data acquisition of KEYOUT7, compared with the last data, the bit corresponding to the key touch stores 1.
23 to 16	KYSC6[7:0]	All 0	R	KYOUT6 scan data After data acquisition of KEYOUT6, compared with the last data, the bit corresponding to the key touch stores 1.
15 to 8	KYSC5[7:0]	All 0	R	KYOUT5 scan data After data acquisition of KEYOUT5, compared with the last data, the bit corresponding to the key touch stores 1.
7 to 0	KYSC4[7:0]	All 0	R	KYOUT4 scan data After data acquisition of KEYOUT4, compared with the last data, the bit corresponding to the key touch stores 1.

54.3.17 Auto key scan data-release register L (A_KYSCDRRL)

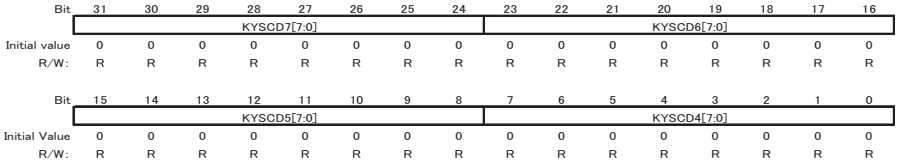
A_KYSCDRRL is a 32-bit read-only register. After data acquisition of KEYSCAN, compared with the last data, the bit corresponding to the key-release stores 1. In case of A_KYCR4.NOFIFO being 1'b0, this register is valid.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	KYSCD3[7:0]	All 0	R	KYOUT3 scan data After data acquisition of KEYOUT3, compared with the last data, the bit corresponding to the key-release stores 1.
23 to 16	KYSCD2[7:0]	All 0	R	KYOUT2 scan data After data acquisition of KEYOUT2, compared with the last data, the bit corresponding to the key-release stores 1.
15 to 8	KYSCD1[7:0]	All 0	R	KYOUT1 scan data After data acquisition of KEYOUT1, compared with the last data, the bit corresponding to the key-release stores 1.
7 to 0	KYSCD0[7:0]	All 0	R	KYOUT0 scan data After data acquisition of KEYOUT0, compared with the last data, the bit corresponding to the key-release stores 1.

54.3.18 Auto key scan data-release register H (A_KYSCDRRH)

A_KYSCDRRH is a 32-bit read-only register. After data acquisition of KEYSCAN, compared with the last data, the bit corresponding to the key-release stores 1. In case of A_KYCR4.NOFIFO being 1'b0, this register is valid.

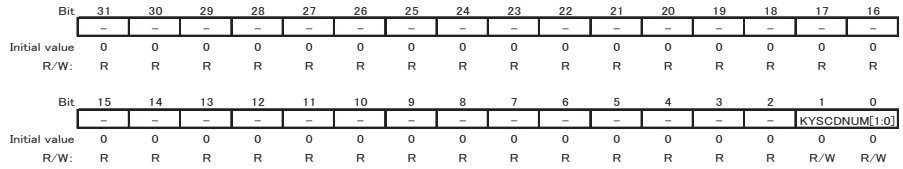


Bit	Bit Name	Initial Value	R/W	Description
31 to 24	KYSCD3[7:0]	All 0	R	KYOUT3 scan data After data acquisition of KEYOUT3, compared with the last data, the bit corresponding to the key-release stores 1.
23 to 16	KYSCD2[7:0]	All 0	R	KYOUT2 scan data After data acquisition of KEYOUT2, compared with the last data, the bit corresponding to the key-release stores 1.
15 to 8	KYSCD1[7:0]	All 0	R	KYOUT1 scan data After data acquisition of KEYOUT1, compared with the last data, the bit corresponding to the key-release stores 1.
7 to 0	KYSCD0[7:0]	All 0	R	KYOUT0 scan data After data acquisition of KEYOUT0, compared with the last data, the bit corresponding to the key-release stores 1.

54.3.19 Auto key scan data-count register (A_KYSCDNUM)

A_KYSCDNUM is a 32-bit readable/writable register that represents the number of data preserved in FIFO. Even if what value is written, FIFO is cleared. In case of A_KYCR4.NOFIFO being 1'b0, this register is valid.

IM



Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
1 to 0	KYSCDNUM[1:0]	All 0	R/W	Scan data number 00: 0 01: 1 11: 2 These bits can be cleared by writing any value.

54.4 Operation

54.4.1 Introduction

This module KEYSC install MANUAL and AUTO mode. These modes are selected by A_KYCR1.KEYEXT.

54.4.2 AUTO MODE operation

(1) AUTO KEY SCAN operation

1. Setting example

Table 54.4 Setting example of AUTO KEY SCAN

Register	Setting value	contents
A_KYCR1	16'h8400	[15] KEYEXT = 1'b1:AUTO mode* [10:8] KYMD[2:0] = 3'b101:KEY pin mode6 [2:0] SCN0[2:0] = 3'b000:key detect chattering elimination RCLK/16(0.49ms)
A_KYCR2	16'h7201	[15:12] SCN2[3:0] = 4'b0111:WAIT per key scan RCLK/2048(62.5ms) [11:8] SCN1[3:0] = 4'b0010:WAIT per KEYOUT setting RCLK/4(122us) [3:0] C2NUM[3:0] = 4'b0001
A_KYCR4	16'h0001	[0] AUTOKS = 1'b1: Excute AUTO KEY SCAN *
A_KYCR6	16'h0000	[14:8] KYDIR[6:0] = 7'b00
A_KYOUTDR	16'h0000	[11:0] KYO<7 to 0>DT[1:0] = H'0000: All output data of KEYOUTn is low level

A_KYIR	32'h00000010	[4] FIFONEE = 1'b1:FIFO interrupt*

Note: * When AUTO MODE, must be set as shown in the above-mentioned.

Others are arbitrary.

Executing AUTO KEY SCAN (AUTOKS = 1'b1) have to be after all register setting is finish.

2. Operation flow by setting example

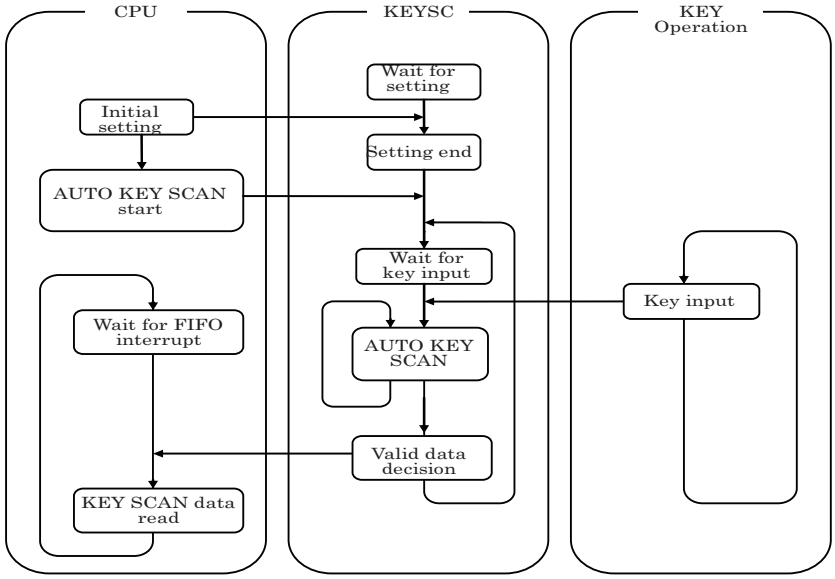


Figure 54.4 AUTO KEY SCAN operation flow

After CPU initializes KEYSC register, CPU starts AUTO KEY SCAN by A_KYCR4.AUTOKS bit and shifts to FIFO INTERRUPT WAIT state of KEY scan-in data. KEYSC module shifts to KEY INPUT WAIT state when AUTO KEY SCAN is started. If KEYSC module in KEY INPUT WAIT state detects KEY input, KEYSC module shifts to AUTO KEY SCAN state and starts KEY SCAN. When valid key data is decided, AUTO KEY SCAN returns to KEY INPUT WAIT state. KEY SCAN is continued repeatedly until all KEY is released. At this time, KEYSC module shifts AUTO KEY SCAN state again if KEY has been pushed. In order to request reading key scan-in data to CPU, KEYSC module generates FIFO interrupt after KEYSC module stores valid key data in FIFO. CPU reads KEY scan-in data until FIFO interrupt is negated. When all KEY is released, KEYSC module returns INPUT WAIT state after valid data is decided.

(2) AUTO KEY SCAN LOOP operation

1. Setting example

Register	Setting value	Contents
A_KYCR1	16'h8400	[15] KEYEXT = 1: AUTO mode* [10:8] KYMD[2:0] = 3'b101: KEY pin mode 6 [2:0] SCN0[2:0] = 3'b000: key detect chattering elimination RCLK/16(0.49ms)
A_KYCR2	16'h7201	[15:12] SCN2[3:0] = 4'b0111: WAIT per key scan [11:8] SCN1[3:0] = 4'b0010: WAIT per KEYOUT setting [3:0] C2NUM[3:0] = 4'b0001
A_KYCR4	16'h0004	[4] AUTOLPSC = 1'b1:Excute loop scan*
A_KYCR6	16'h0000	[14:8] KYDIR[7:0] = 7'h00
A_KYOUTDR	16'h0000	[11:0] KYO<7 to 0>DT[1:0]: All output data of KEYOUTn is low level
A_KYIR	32'h00000010	[4] FIFONEE = 1'b1:FIFO interrupt*

Note: * When Auto mode, must be set as shown in the above-mentioned.

Others are arbitrary.

Executing AUTO KEY SCAN LOOP (AUTOLPSC = 1'b1) have to be after all register setting is finish.

2. Operation flow by setting example

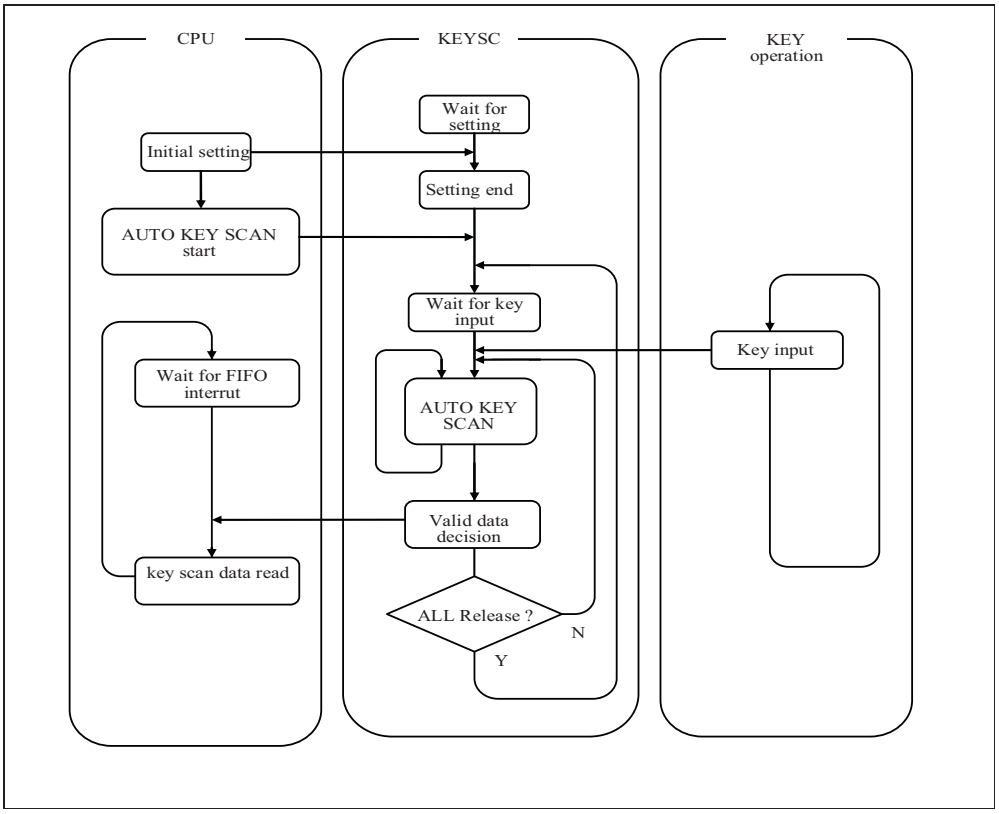


Figure 54.5 AUTO KEY SCAN LOOP operation flow

After CPU initializes KEYSC register, CPU starts AUTO KEY SCAN LOOP by A_KYCR4.AUTOLPSC bit and shifts to FIFO INTERRUPT WAIT. KEYSC module shifts to KEY INPUT WAIT state when AUTO KEY SCAN LOOP is started. If KEYSC module in KEY INPUT WAIT state detects KEY input, KEYSC module shifts to AUTO KEY SCAN LOOP state and starts KEY scan. When valid key data is decided, if its value is all-release, KEYSC module shifts to KEY INPUT WAIT state otherwise KEY SCAN is executed again. In order to request reading key scan-in data to CPU, KEYSC module generates FIFO interrupt after KEYSC module stores valid key data in FIFO. CPU reads KEY scan-in data until FIFO interrupt is negated. When all KEY is released, KEYSC module repeats KEY SCAN after valid data is decided and its value is all-release. KEYSC module returns INPUT WAIT state when valid data is all-release.

54.4.3 Interrupt and Power Wakeup at AUTO mode

Figure 54.6 shows diagrammatic illustration of interrupt and power wakeup at AUTO mode.

There is four interrupts: KEY detect interrupt, KEY change interrupt, KEY all release interrupt and FIFO interrupt.

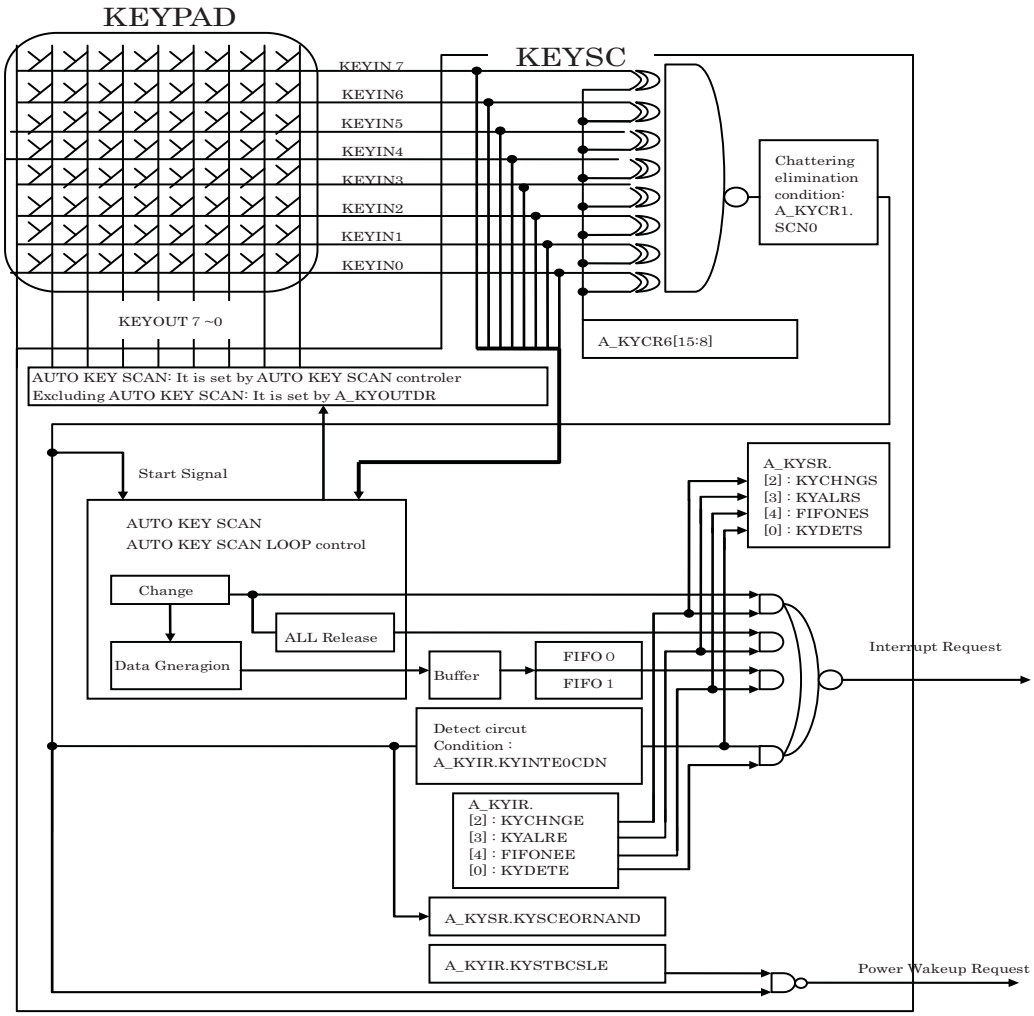


Figure 54.6 diagrammatic illustration of interrupt and power wakeup at AUTO mode

(1) Interrupt

1. KEY detect interrupt

It is used to generate interrupt when the key is pushed without using AUTO KEY SCAN mode and AUTO KEY SCAN LOOP mode. Interrupt can be generated, when key is pushed once or more (setting example: A_KYOUTDR = H'0000, A_KYCR6 = H'0000, A_KYIR = H'00010001). To clear interrupt except for level setting, writing 0 to A_KYSR.KYDETS and reading it repeatedly is needed until 0 is reflected in it.

2. KEY change interrupt

A_KYSR.KYCHNGS stores 1 at AUTO KEY SCAN mode and AUTO KEY SCAN LOOP mode, when AUTO key scan data is different from last one. AUTO key scan data is stored in A_KYSCDRL and A_KYSCDRH. Reading data is needed after WAIT until A_KYSCDNUM store figure excluding 0, because time that data is reflected in that register is slower than time that interrupt is generated. To clear interrupt, writing 0 to A_KYSR.KYCHNGES and reading it repeatedly is needed until 0 is reflected in it.

3. KEY all release interrupt

A_KYSR.KYALRS stores 1 at AUTO KEY SCAN mode and AUTO KEY SCAN LOOP mode, when AUTO key scan data is different from last data and key is all released. AUTO key scan data is stored in A_KYSCDRL and A_KYSCDRH. Reading data is needed after WAIT until A_KYSCDNUM store figure excluding 0, because time that data is reflected in that register is slower than time that interrupt is generated. To clear interrupt, writing 0 to A_KYSR.KYCHNGES and reading it repeatedly is needed until 0 is reflected in it.

4. FIFO interrupt

A_KYSR.FIFONES stores 1 at AUTO KEY SCAN mode and AUTO KEY SCAN LOOP mode, when AUTO key scan data is different from last data. AUTO key scan data is stored in A_KYSCDRL and A_KYSCDRH. Data can be read at once after interrupt has generated. When data is read and the number of data in FIFO becomes 0, A_KYSR.FIFONES becomes 0 automatically. Writing 0 in A_KYSR.FIFONES is not necessary.

(2) Power wakeup

Power wakeup and interrupt can be processed by using KEY detect interrupt. The setting example is shown below.

Register	Setting value	Contents
A_KYSR1	16'h8400	[15] KEYEXT = 1: AUTO mode *1 [10:8] KYMD[2:0] = 3'b100:KEY pin mode 5 [2:0] SCN0[2:0] = 3'b000: key detect chattering elimination RCLK/16(0.49ms) *2
A_KYCR6	16'h0000	[14:8] KYDIR[6:0] = 7'h00
A_KYOUTDR	16'h0000	[11:0]KYO<5 to 0>DT[1:0] = H'0000:all output data low level of KEYOUTn *1
A_KYIR	32'h00120004	[20] KYSTBCSLE = 1'b1:key scan power wakeup enable *1 [18:16] KYINTE0CDN[2:0] = 3'b010:rising edge *1 [0] KYDETE = 1'b1:KEY detect interrupt

*1 These values in this example are just for reference.Only set KYSTBCSLE = 1'b1 is mandatory.

*2 Set SCN0[2:0] = 3'b111 is prohibited.

When key is pushed, power wakeup and interrupt is generated. Writing 0 to A_KYSR.KYDETS and reading it repeatedly is needed until 0 is reflected in it.

54.4.4 Handling of Data at AUTO KEY SCAN MODE and AUTO KEY SCAN LOOP MODE

Detected key data is stored to the buffer once at AUTO KEY SCAN MODE and AUTO KEY SCAN LOOP MODE. The buffer is always a superscription. FIFO controller confirms (1) and (2) and takes data stored in the buffer into FIFO. Figure 54.7 shows flow of data.

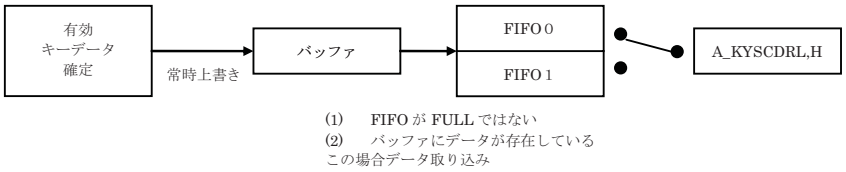


Figure 54.7 flow of data

54.4.5 About output of all key release data at AUTO KEY SCAN and AUTO KEY SCAN LOOP

(1) Data of the first time

Although the sequence is executed at AUTO KEY SCAN and AUTO KEY SCAN LOOP when key is pushed, if key is released while valid data is decided, it is likely to fix it as all data release, though it is data of the first time.

(2) After detecting all key release

Start signal of sequence at AUTO KEY SCAN and AUTO KEY SCAN LOOP is signal (KYSCEORNAND) after all key detect chattering elimination. When chattering elimination setting is done, as for KYSCEORNAND, the timing slows more than the actual key release.

Figure 54.8 shows all key release detect.

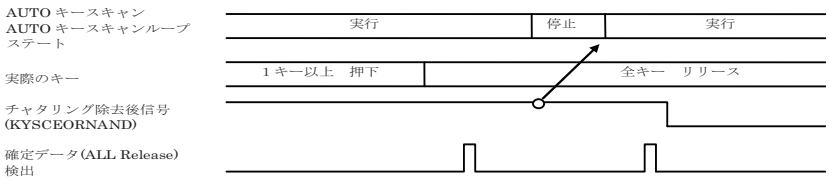


Figure 54.8 all key release detect

54.4.6 When AUTO KEY SCAN and AUTO KEY SCAN LOOP is released

To release AUTO KEY SCAN and AUTO KEY SCAN LOOP MODE, writing 0 in A_KYCR4.AUTOLPSC or A_KYCR4.AUTOKS is needed. However the limiting conditions exist as follow.

(1) Setting prohibition period until the next restarting

Wait (single AUTO KEY SCAN operation time (RCLK/(((A_KYCR2.SCN1 + 1) + 1 * 8)) is needed.

(2) Data annulment after mode is released

After AUTO KEY SCAN MODE and AUTO KEY SCAN LOOP MODE are released, data may be stored in FIFO. Therefore setting of interrupt inhibit is needed. Before restart, FIFO clear is needed by writing to A_KYSCDNUM.

54.4.7 External Pin Control

It is necessary to set the pull-up to KEYIN pins by GPIO setting. However, when the BSCMD pin is 1, KEYIN will automatically becomes pull-up

54.4.8 Chattering Elimination

By setting the M_KYCR1.SCN bit and A_KYCR1.SCN0, chattering elimination in key interrupt detection is possible. Through this chattering elimination, if a key is pressed continuously for longer than a length of time set by the SCN bits, a continuous key press is recognized. Thereafter, when a state in which a key is released continues for longer than a length of time set by the SCN bits, the key is recognized as having been released.

54.4.9 Detection of Multiple Key Presses

While the KYOUTDR setting is used to set the KEYOUT7 to KEYOUT0 pins to the low-level output in order one at a time, and with the other seven pins at high impedance, multiple key presses can be detected by reading KYINDR.

54.4.10 Interrupt generation not anticipated after initial setting of KEYSC

Only once immediately after beginning of KEYSC operation, though the key is not pushed, interrupt might be generated mis-recognizing the key push. To avoid it, by using CPGA software reset register, KEYSC reset is needed before KEYSC initial setting.

54.4.11 Examples of Use of MANUAL MODE

(1) Level Interrupt (KYCPU_IE1 and KYCPU_IE0 = B'01)

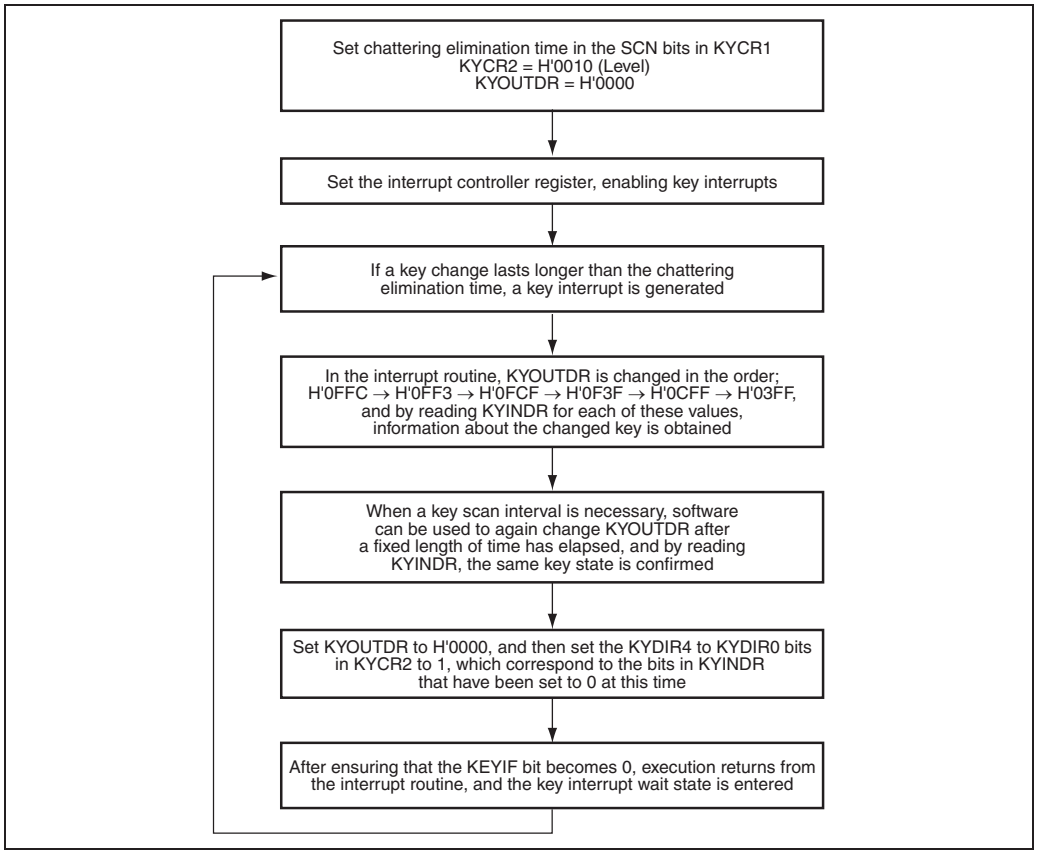


Figure 54.9 Example of Key Scan Using Level Interrupt (Key Pin Mode 1)

(2) Edge Interrupt (KYCPU_IE1 and KYCPU_IE0 = B'1x)

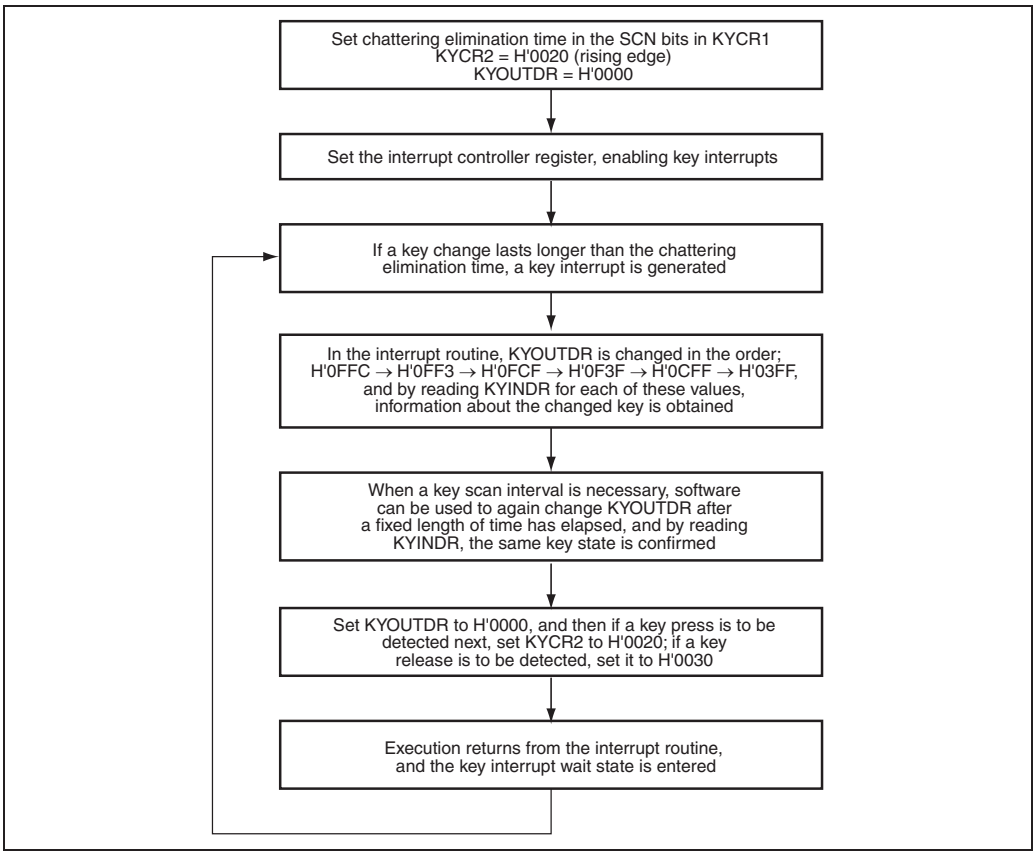


Figure 54.10 Example of Key Scan Using Edge Interrupt (Key Pin Mode 1)

Section 55 IrDA Controller (IrDA)

The IrDA controller (IrDA) controls infrared data communication conforming to IrDA PHY standard 1.1/1.3 in three different speed modes: serial infrared (SIR)-UART (2,400 bits to 115.2 kbits/s) mode, medium infrared (MIR) (0.576 Mbits/s or 1.152 Mbits/s) mode, and fast infrared (FIR) (4.0 Mbits/s) mode.

The IrDA incorporates modules such as an SIR-UART engine, an MIR&FIR engine, a cyclic redundancy check (CRC) engine, a buffer RAM, and an interrupt controller. The SIR-UART engine controls communication in SIR-UART mode and the MIR&FIR engine controls communication in MIR and FIR modes.

The buffer RAM holds one frame of transmit data or up to 16 frames of received data.

In transmission, when one frame of data stored in the buffer RAM has been completely transmitted, transmission is disabled, notifying the end of transmission by issuing an interrupt.

There are two modes for reception; non-FIFO mode where the buffer RAM is treated as a single RAM and FIFO mode where the buffer RAM is treated as a 16-stage FIFO. In the non-FIFO mode, when one frame of data has been completely received and stored in the buffer RAM, reception is disabled, notifying the end of reception by issuing an interrupt. In the FIFO mode, continuous reception of up to 16 frames, DMA auto-request, and interrupt notices are available without software intervention.

In SIR-UART, MIR, and FIR modes, auto-receive mode is available, in which reception is automatically enabled after transmission is completed.

It is possible to set the appropriate SIR transmit pulse width according to the characteristics of the infrared light receiving and emitting module used. The serial interaction pulse (SIP) output and abort output functions are also available. A 48-MHz clock signal is used for communication.

55.1 Features

Table 55.1 IrDA Features

Item	Description
Standard	IrDA PHY1.1/1.3
Communication mode	SIR-UART mode: 2400 bits, 9600 bits, 19.2 kbits, 38.4 kbits, 57.6 kbits, or 115.2 kbits/s MIR mode: 0.576 Mbits/s or 1.152 Mbits/s FIR mode: 4.0 Mbits/s
Data transfer	Transmission: 1 frame unit (The end of transmission is notified by issuing an interrupt.) Reception: Selectable between the frame by frame non-FIFO mode and 16-stage FIFO mode FIFO mode: automatic continuous frame reception, DMA request
Interrupt	• SIR-UART mode Transmission: Frame transmit end Reception: Frame receive end (sources: normal end, transfer area overflow, framing error, and timeout) • MIR mode and FIR mode Transmission: Frame transmit end Reception: Frame receive end (sources: normal end, transfer area overflow, CRC error, and abort detection) • FIFO mode Transmission: None Reception: FIFO interrupts (sources: FIFO write, FIFO area overflow, DMA transfer end)
Pulse modulation/demodulation	SIR-UART mode transmission: Pulse width setting function
Infrared light receiving and emitting module interface	Transmission: IRDA_OUT (SIP output function, abort output function, level inversion function) Reception: IRDA_IN (level inversion function)
Test mode	Internal loop back function for transmit/receive signals

Figure 55.1 shows an internal block diagram of the IrDA.

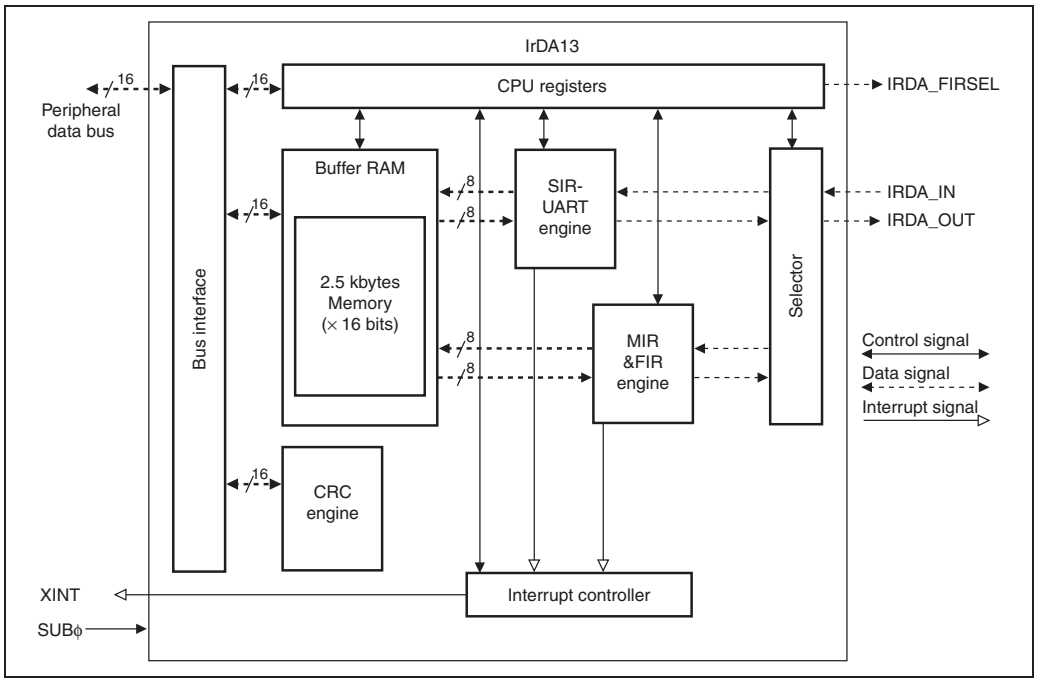


Figure 55.1 Internal Block Diagram of IrDA

55.2 Input/Output Pins

The IrDA has the input/output pins listed in Table 55.2.

Table 55.2 IrDA Pin Configuration

Pin Name	Function	I/O	Description
IRDA_IN	Receive data input	Input	Inputs the received data.
IRDA_OUT	Transmit data output	Output	Outputs the data to be transmitted.
IRDA_FIRSEL	FIR select	Output	Switches between SIR, MIR, and FIR modes.

55.3 Register Descriptions

Table 55.3 shows the IrDA register configuration. Table 55.4 shows the register states in each operating mode.

Table 55.3 IrDA Register Configuration

Register	Abbreviation	R/W	Address	Access Size
Transfer mode register	IRTMR	R/W	H'E6D0 1F00	8/16
Configuration register	IRCFR	R/W	H'E6D0 1F02	8/16
IR control register	IRCTR	R/W	H'E6D0 1F04	8/16
Transmit frame length register	IRTFLR	R/W	H'E6D0 1F20	8/16
Transmit control register	IRTCTR	R/W	H'E6D0 1F22	8/16
Receive frame length register	IRRFLR	R	H'E6D0 1F40	8/16
Receive control register	IRRCTR	R/W	H'E6D0 1F42	8/16
SIR-UART mode interrupt source register	SIRISR	R	H'E6D0 1F60	8/16
SIR-UART mode interrupt mask register	SIRIMR	W	H'E6D0 1F62	8/16
SIR-UART mode interrupt clear register	SIRICR	W	H'E6D0 1F64	8/16
SIR-UART mode baud rate count register	SIRBCR	R/W	H'E6D0 1F68	8/16
MIR/FIR mode interrupt source register	MFIRISR	R	H'E6D0 1F70	8/16
MIR/FIR mode interrupt mask register	MFIRIMR	W	H'E6D0 1F72	8/16
MIR/FIR mode interrupt clear register	MFIRICR	W	H'E6D0 1F74	8/16
CRC engine control register	CRCCTR	R/W	H'E6D0 1F80	8/16
CRC engine input data register	CRCIR	W	H'E6D0 1F86	8/16
CRC engine calculation register	CRCCR	W	H'E6D0 1F8A	16
CRC engine output data register	CRCOR	R	H'E6D0 1F8E	8/16
FIFO current pointer	FIFOCP	R/W	H'E6D0 1FC0	16
FIFO follow pointer	FIFOFP	R/W	H'E6D0 1FC2	16
FIFO receive status mask	FIFORSMSK	R/W	H'E6D0 1FC4	16
FIFO receive status OR	FIFORSOR	R	H'E6D0 1FC6	16

Register	Abbreviation	R/W	Address	Access Size
FIFO select	FIFOSEL	R/W	H'E6D0 1FC8	16
FIFO receive status	FIFORS	R/W	H'E6D0 1FCA	16
FIFO receive frame length	FIFORFL	R/W	H'E6D0 1FCC	16
FIFO RAM current pointer	FIFORAMCP	R/W	H'E6D0 1FCE	16
FIFO RAM follow pointer	FIFORAMFP	R/W	H'E6D0 1FD0	16
BUS interface control	BIFCTL	R/W	H'E6D0 1FD2	16
IrDA buffer RAM	IRDARAM	R/W	H'E6D0 0000 to H'E6D0 1039	8/16/32 (read-only for 32)

Table 55.4 Register States in Each Operating Mode

Register Abbreviation	Reset*	Module Standby
IRTMR	Initialized	Retained
IRCFR	Initialized	Retained
IRCTR	Initialized	Retained
IRTFLR	Initialized	Retained
IRTCTR	Initialized	Retained
IRRFLR	Initialized	Retained
IRRCTR	Initialized	Retained
SIRISR	Initialized	Retained
SIRIMR	Initialized	Retained
SIRICR	Initialized	Retained
SIRBCR	Initialized	Retained
MFIRISR	Initialized	Retained
MFIRIMR	Initialized	Retained
MFIRICR	Initialized	Retained
CRCCTR	Initialized	Retained
CRCIR	Initialized	Retained
CRCCR	Initialized	Retained
CRCOR	Initialized	Retained
FIFOCP	Initialized	Retained

Register Abbreviation	Reset*	Module Standby
FIFOFP	Initialized	Retained
FIFORSMSK	Initialized	Retained
FIFORSOR	Initialized	Retained
FIFOSEL	Initialized	Retained
FIFORS	Initialized	Retained
FIFORFL	Initialized	Retained
FIFORAMCP	Initialized	Retained
FIFORAMFP	Initialized	Retained
BIFCTL	Initialized	Retained
IRDARAM	Undefined	Retained

Note: * For details, refer to section 1-D Overview of reset.

55.3.1 Transfer Mode Register (IRTMR)

IRTMR, shared by SIR-UART, MIR, and FIR modes, is a register that selects a transfer mode and simultaneously masks all the interrupts in each transfer mode.

Before switching the transfer modes or transmit and receive modes through this register, transmission and reception must be disabled.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TMD[1:0]		FIRMD		—	—	—	FIFO RIM	—	—	—	MIM	—	—	—	SIM
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
15, 14	TMD[1:0]	00	R/W	Transfer Mode These bits select the transfer mode. When the mode setting has been completed, either the SIR-UART engine or the MIR&FIR engine corresponding to the selected mode starts operating. 0X: SIR-UART mode 10: FIR mode 11: MIR mode Note: X: Don't care.
13, 12	FIRMD[1:0]	00	R/W	FIR Modulation/Demodulation Pulse Distinction Mode These bits select distinction mode for single pulses or double pulses in the FIR modulation/demodulation pulse reception. In Auto mode, the single-pulse and double-pulse widths are automatically defined based on the interval between STA and PA for distinction. In Manual mode, the single-pulse and double-pulse widths are defined by a register setting for distinction. 0X: Auto mode 10: Manual mode 1 (Single pulse: SUBϕ $\times$ 8 cycles or less, Double pulse: SUBϕ $\times$ 9 cycles or more) 11: Manual mode 2 (Single pulse: SUBϕ $\times$ 9 cycles or less, Double pulse: SUBϕ $\times$ 10 cycles or more) Note: X: Don't care

Bit	Bit Name	Initial Value	R/W	Description
11 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	FIFORIM	0	R/W	FIFO receive interrupt mask This is a mask register that is located above FIFORSMSK. It masks all the interrupt sources of FIFORS. 0: Masks no interrupts. 1: Masks all the interrupts.
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	MIM	0	R/W	MIR/FIR Interrupt Mask Masks all the interrupts generated in MIR and FIR modes. 0: Masks no interrupts. 1: Masks all the interrupts.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	SIM	0	R/W	SIR Interrupt Mask Masks all the interrupts generated in SIR-UART mode. 0: Masks no interrupts. 1: Masks all the interrupts.

55.3.2 Configuration Register (IRCFR)

IRCFR, shared by SIR-UART, MIR, and FIR modes, is a register that controls the receive timeout time and the transmit signals.

Before setting this register, transmission and reception must be disabled.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TPW	—	—	—	—	—	RTO[1:0]		MBR	—	—	STAC	—	—	ABT	SIP
Initial value:	0	—	—	—	—	—	0	0	0	—	—	0	—	—	0	0
R/W:	R/W	R	R	R	R	R	R/W	R/W	R/W	R	R	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	TPW	0	R/W	Transmit Pulse Width (in SIR-UART mode only) Specifies the transmit pulse width in SIR-UART mode. 0: 1.63 μs 1: 3/16T of one-bit duration.
14 to 10	—	Undefined	R	Reserved These bits are always read as 0. The write value should always be 0.
9, 8	RTO[1:0]	00	R/W	Receive Timeout (in SIR-UART mode only) These bits specify the receive timeout time in SIR-UART mode. Setting these bits allows a timeout interrupt to be generated when the interval between the bytes in the same frame exceeds the specified timeout time. The actual interval between the bytes is defined as the interval between the stop bits. 00: A timeout interrupt is not generated. 01: A timeout interrupt is generated when the interval between the bytes exceeds 1 ms. 11: A timeout interrupt is generated when the interval between the bytes exceeds 10 ms. 11: Setting prohibited.

Bit	Bit Name	Initial Value	R/W	Description
7	MBR	0	R/W	MIR Baud Rate Specifies the baud rate in MIR mode. 0: 0.576 Mbits/s 1: 1.152 Mbits/s
6, 5	—	Undefined	R	Reserved These bits are always read as 0. The write value should always be 0.
4	STAC	0	R/W	Start Flag (STA) Count (in MIR and FIR modes only) Specifies the number of STA in a transmit frame in MIR and FIR modes. 0: One STA in FIR mode and two STA in MIR mode. 1: Two STA in FIR mode and three STA in MIR mode.
3, 2	—	Undefined	R	Reserved These bits are always read as 0. The write value should always be 0.
1	ABT	0	R/W	Abort Output (in MIR and FIR modes only) Aborts transmission in MIR and FIR modes. While this bit is 1, the abort state continues to be output from the transmit data output pin. This bit is not used in SIR-UART mode; the abort state is output by writing a character sequence indicating the abort state to the buffer RAM. 0: Normal transmission 1: Abort output
0	SIP	0	R/W	SIP Output (in MIR and FIR modes only) In MIR and FIR modes, SIP is output to notify a device with a communication speed of 115.2 kbits/s or slower that communication is currently being performed in MIR or FIR mode. When this bit is modified to 1, a 1.6-μs-wide SIP pulse is output within 8.7 μs. The 500-ms interval between SIPs should be measured using software. 0: Normal transmission 1: SIP output

55.3.3 IR Control Register (IRCTR)

IRCTR, shared by SIR-UART, MIR, and FIR modes, is a register that controls the infrared light module interface signals.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RSI	—	—	—	—	—	—	IRIN	TSI	—	TSS[1:0]		—	—	—	FIRS
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R/W	R/W	R	R/W	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	RSI	0	R/W	Inverted Receive Signal Input Inverts the received signal before pulse modulation. The logic level of the received signal input is usually negative; however, if the receive signal pin of the infrared light receiving and emitting module used employs the positive logic level, the input signal can be inverted using this bit. 0: Does not invert the received signal. 1: Inverts the received signal.
14 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	IRIN	0	R/W	IRDA_IN Monitor Indicates the status of the IRDA_IN pin. 0: Low level 1: High level
7	TSI	0	R/W	Inverted Transmit Signal Output Inverts the pulse-modulated transmit signal before outputting. 0: Does not invert the transmit signal. 1: Inverts the transmit signal.
6	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
5, 4	TSS[1:0]	00	R/W	Transmit Signal Select Selects the transmit signal output; specifically, selects whether to transmit the signal normally or to control the signal directly through these bits. 00: Normal output 01: Setting prohibited 10: 0 output 11: 1 output
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	FIRS	0	R/W	FIR_SELECT Specifies the FIR_SELECT output for controlling the infrared light receiving and emitting module. 0: 0 output 1: 1 output

55.3.4 Transmit Frame Length Register (IRTFLR)

IRTFLR, shared by SIR-UART, MIR, and FIR modes, is a register that specifies the transmit frame length.

When this register is read, the specified number of data bytes is always read out. If transmission is enabled with this register set to the initial value, no data is transmitted. Here, the TE bit is cleared to 0 and a transmit end interrupt is generated simultaneously, completing transmission.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	TFL[12:0]												
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 0	TFL[12:0]	H'000	R/W	Transmit Frame Length These bits specify the number of data bytes in a frame to be transmitted. In SIR-UART mode, the number of data bytes should include framewrapping. In MIR and FIR modes, the number of data bytes excludes framewrapping; only the IrLAP payload part is considered.

55.3.5 Transmit Control Register (IRTCTR)

IRTCTR, shared by SIR-UART, MIR, and FIR modes, is a register that specifies auto-receive mode and enables/disables transmission.

If transmission is disabled during SIR-UART mode transmission, the SIR-UART engine discards the currently transmitting data byte**,** terminating transmission. In this case, the transmit data is regarded as illegal frame data, and thus does not bring about the reception state even if auto-receive mode is enabled.

If transmission is disabled during MIR or FIR mode transmission, the MIR&FIR engine immediately stops transmission, thus terminating transmission. In this case, the transmit data is regarded as illegal frame data, and thus does not bring about the reception state even if auto-receive mode is enabled.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ARMOD	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	ARMOD	0	R/W	Auto-Receive Mode Specifies auto-receive mode after transmission, in which the end of transmission automatically causes the reception state. 0: No auto-receive mode 1: Auto-receive mode
14 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	TE	0	R/W	Transmit Enable Enables/disables transmission. This bit is automatically cleared to 0 after transmission. 0: Disables transmission. 1: Enables transmission.

55.3.6 Receive Frame Length Register (IRRFLR)

IRRFLR, shared by SIR-UART, MIR, and FIR modes, is a register in which the length of the received frame is stored after reception.

When this register is read during reception, the number of data bytes that have been received so far is read out. This register is initialized if the receive-disabled state is switched to receive-enabled state.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	RFL[12:0]												
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 0	RFL[12:0]	H'000	R	Receive Frame Length These bits indicate the number of data bytes received in the frame. In SIR-UART mode, the indicated number of data bytes includes framewrapping. In MIR and FIR modes, the indicated number of data bytes excludes framewrapping; only the IrLAP payload part is considered.

55.3.7 Receive Control Register (IRRCTR)

IRRCTR, shared by SIR-UART, MIR, and FIR modes, is a register that enables/disables reception.

If reception is disabled during SIR-UART mode reception, the SIR-UART engine discards the currently receiving data byte, thus terminating reception. If reception is disabled during MIR and FIR mode reception, the MIR&FIR engine immediately stops reception**,** terminating reception.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	REPRE	—	—	—	RE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	REPRE	0	R/W	Repeated receive enable Controls whether RE is automatically cleared after reception. REPRE must be set to 1 only when FIFOEN is 1 to prevent the next received data from being overwritten. 0: RE is automatically cleared after reception. 1: RE is not automatically cleared after reception.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	RE	0	R/W	Receive Enable Enables/disables reception. This bit is automatically cleared to 0 after reception. 0: Disables reception. 1: Enables reception.

55.3.8 SIR-UART Mode Interrupt Source Register (SIRISR)

SIRISR, used in SIR-UART mode, is a register that indicates the sources of the interrupts generated in SIR-UART mode. Writing 1 to the bits in SIRICR clears the corresponding bits in this register to 0.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FRE	—	—	—	TROV	—	TOT	FER	FTE	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	FRE	0	R	Frame Receive End Indicates that one frame has been received. 0: One frame has not been received. 1: One frame has been received.
14 to 12	—	All 0	R	Reserved These bits are always read as 0.
11	TROV	0	R	Transfer Area Overflow Indicates that the quantity of the received data bytes has exceeded the buffer RAM area, causing a transfer area overflow. 0: A transfer area overflow has not occurred. 1: A transfer area overflow has occurred.
10	—	0	R	Reserved This bit is always read as 0.
9	TOT	0	R	Timeout Indicates that the interval between the received data bytes in the same frame exceeds the timeout time (1 ms or 10 ms) specified in IRCFR, causing a timeout. 0: A timeout has not occurred. 1: A timeout has occurred.

Bit	Bit Name	Initial Value	R/W	Description
8	FER	0	R	Framing Error Indicates that no stop bit is appended to the received data, causing a framing error. 0: A framing error has not occurred. 1: A framing error has occurred.
7	FTE	0	R	Frame Transmit End Indicates that one frame has been transmitted. 0: One frame has not been transmitted. 1: One frame has been transmitted.
6 to 0	—	All 0	R	Reserved These bits are always read as 0.

55.3.9 SIR-UART Mode Interrupt Mask Register (SIRIMR)

SIRIMR, used in SIR-UART mode, is a register that masks the interrupts generated in SIR-UART mode.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FREIM	—	—	—	TROVIM	—	TOTIM	FERIM	FTEIM	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Bit	Bit Name	Initial Value	R/W	Description
15	FREIM	0	W	Frame Receive End Interrupt Mask Masks the frame receive end interrupt. 0: Does not mask the frame receive end interrupt. 1: Masks the frame receive end interrupt.
14 to 12	—	All 0	W	Reserved The write value should always be 0.
11	TROVIM	0	W	Transfer Area Overflow Interrupt Mask Masks the transfer area overflow interrupt. 0: Does not mask the transfer area overflow. 1: Masks the transfer area overflow.

Bit	Bit Name	Initial Value	R/W	Description
10	—	0	W	Reserved The write value should always be 0.
9	TOTIM	0	W	Timeout Interrupt Mask Masks the timeout interrupt. 0: Does not mask the timeout interrupt. 1: Masks the timeout interrupt.
8	FERIM	0	W	Framing Error Interrupt Mask Masks the framing error interrupt. 0: Does not mask the framing error interrupt. 1: Masks the framing error interrupt.
7	FTEIM	0	W	Frame Transmit End Interrupt Mask Masks the frame transmit end interrupt. 0: Does not mask the frame transmit end interrupt. 1: Masks the frame transmit end interrupt.
6 to 0	—	All 0	W	Reserved The write value should always be 0.

55.3.10 SIR-UART Mode Interrupt Clear Register (SIRICR)

SIRICR, used in SIR-UART mode, is a register that clears the interrupts generated in SIR-UART mode. After 1 is written to the bits in this register thus clearing the corresponding interrupts, the bits automatically return to 0.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FREIC	—	—	—	FROVIC	—	TOTIC	FERIC	FTEIC	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Bit	Bit Name	Initial Value	R/W	Description
15	FREIC	0	W	Frame Receive End Interrupt Clear Clears the frame receive end interrupt. 0: Does not clear the frame receive end interrupt. 1: Clears the frame receive end interrupt.

Bit	Bit Name	Initial Value	R/W	Description
14 to 12	—	All 0	W	Reserved The write value should always be 0.
11	FROVIC	0	W	Transfer Area Overflow Interrupt Clear Clears the transfer area overflow interrupt. 0: Does not clear the transfer area overflow. 1: Clears the transfer area overflow.
10	—	0	W	Reserved The write value should always be 0.
9	TOTIC	0	W	Timeout Interrupt Clear Clears the timeout interrupt. 0: Does not clear the timeout interrupt. 1: Clears the timeout interrupt.
8	FERIC	0	W	Framing Error Interrupt Clear Clears the framing error interrupt. 0: Does not clear the framing error interrupt. 1: Clears the framing error interrupt.
7	FTEIC	0	W	Frame Transmit End Interrupt Clear Clears the frame transmit end interrupt. 0: Does not clear the frame transmit end interrupt. 1: Clears the frame transmit end interrupt.
6 to 0	—	All 0	W	Reserved The write value should always be 0.

55.3.11 SIR-UART Mode Baud Rate Count Register (SIRBCR)

SIRBCR, used in SIR-UART mode, is a register that specifies the baud rate used for both transmission and reception.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	BRC[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 6	—	All 0	R	Reserved The write value should always be 0.
5 to 0	BRC[5:0]	000000	R/W	Baud Rate Count These bits specify the frequency division ratio (baud rate counter value) to produce the desired baud rate from the externally input clock signal. Since the frequency of the externally input 48-MHz clock signal is divided by 26 prior to generating the communication clock signal, the baud rate calculation equation and the baud rate counter values given below are used. The resultant frequency error is +0.16%, which falls within the tolerance prescribed in the IrDA standard. The baud rate counter value must be modified after disabling transmission and reception. Baud rate (bits/s) = 1.8432 MHz/{(baud rate counter value + 1) × 16} Baud rate (bits/s) Baud rate counter value (Hex) 2400 47 (H'2F) 9600 11 (H'B) 19.2 k 5 (H'5) 38.4 k 2 (H'2) 57.6 k 1 (H'1) 115.2 k 0 (H'0)

55.3.12 MIR/FIR Mode Interrupt Source Register (MFIRISR)

MFIRISR, used in MIR and FIR modes, is a register that indicates the sources of the interrupts generated in MIR and FIR modes. Writing 1 to the bits in MFIRICR clears the corresponding bits in this register to 0.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FRE	—	—	—	TROV	—	ABTD	CRC ER	FTE	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	FRE	0	R	Frame Receive End Indicates that one frame has been received. 0: One frame has not been received. 1: One frame has been received.
14 to 12	—	All 0	R	Reserved These bits are always read as 0.
11	TROV	0	R	Transfer Area Overflow Indicates that the quantity of the received data bytes has exceeded the buffer RAM area, causing a transfer area overflow. 0: A transfer area overflow has not occurred. 1: A transfer area overflow has occurred.
10	—	0	R	Reserved This bit is always read as 0.
9	ABTD	0	R	Abort Detection Indicates that an illegal pulse code has been detected in the received data (= abort detection). 0: No illegal pulse codes have been detected. 1: An abort has been detected.

Bit	Bit Name	Initial Value	R/W	Description
8	CRCER	0	R	CRC error Indicates that a CRC error has occurred in the received data. 0: A CRC error has not occurred. 1: A CRC error has occurred.
7	FTE	0	R	Frame Transmit End Indicates that one frame has been transmitted. 0: One frame has not been transmitted. 1: One frame has been transmitted.
6 to 0	—	All 0	R	Reserved These bits are always read as 0.

55.3.13 MIR/FIR Mode Interrupt Mask Register (MFIRIMR)

MFIRIMR, used in MIR and FIR modes, is a register that masks the interrupts generated in MIR and FIR modes.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FREIM	—	—	—	TROVIM	—	ABTDIM	CRCERIM	FTEIM	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Bit	Bit Name	Initial Value	R/W	Description
15	FREIM	0	W	Frame Receive End Interrupt Mask Masks the frame receive end interrupt. 0: Does not mask the frame receive end interrupt. 1: Masks the frame receive end interrupt.
14 to 12	—	All 0	W	Reserved The write value should always be 0.
11	TROVIM	0	W	Transfer Area Overflow Interrupt Mask Masks the transfer area overflow interrupt. 0: Does not mask the transfer area overflow. 1: Masks the transfer area overflow.

Bit	Bit Name	Initial Value	R/W	Description
10	—	0	W	Reserved The write value should always be 0.
9	ABTDIM	0	W	Abort Detection Interrupt Mask Masks the abort detection interrupt. 0: Does not mask the abort detection interrupt. 1: Masks the abort detection interrupt.
8	CRCERIM	0	W	CRC Error Interrupt Mask Masks the CRC error interrupt. 0: Does not mask the CRC error interrupt. 1: Masks the CRC error interrupt.
7	FTEIM	0	W	Frame Transmit End Interrupt Masks the frame transmit end interrupt. 0: Does not mask the frame transmit end interrupt. 1: Masks the frame transmit end interrupt.
6 to 0	—	All 0	W	Reserved The write value should always be 0.

55.3.14 MIR/FIR Mode Interrupt Clear Register (MFIRICR)

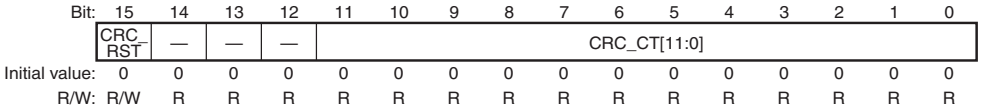
MFIRICR, used in MIR and FIR modes, is a register that clears the interrupts generated in MIR and FIR modes. After 1 is written to the bits in this register thus clearing the corresponding interrupts, the bits automatically return to 0.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FREIC	—	—	—	TEOVIC	—	ABTDIC	CRCERIC	FTEIC	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Bit	Bit Name	Initial Value	R/W	Description
15	FREIC	0	W	Frame Receive End Interrupt Clear Clears the frame receive end interrupt. 0: Does not clear the frame receive end interrupt. 1: Clears the frame receive end interrupt.

Bit	Bit Name	Initial Value	R/W	Description
14 to 12	—	All 0	W	Reserved The write value should always be 0.
11	TEOVIC	0	W	Transfer Area Overflow Interrupt Clear Clears the transfer area overflow interrupt. 0: Does not clear the transfer area overflow. 1: Clears the transfer area overflow.
10	—	0	W	Reserved The write value should always be 0.
9	ABTDIC	0	W	Abort Detection Interrupt Clear Clears the abort detection interrupt. 0: Does not clear the abort detection interrupt. 1: Clears the abort detection interrupt
8	CRCERIC	0	W	CRC Error Interrupt Clear Clears the CRC error interrupt. 0: Does not clear the CRC error interrupt 1: Clears the CRC error interrupt
7	FTEIC	0	W	Frame Transmit End Interrupt Clear Clears the frame transmit end interrupt. 0: Does not clear the frame transmit end interrupt. 1: Clears the frame transmit end interrupt.
6 to 0	—	All 0	W	Reserved The write value should always be 0.

55.3.15 CRC Engine Control Register (CRCCTR)



Bit	Bit Name	Initial Value	R/W	Description
15	CRC_RST	0	R/W	CRC Engine Reset Clears all registers related to CRC calculation. After reset, this bit automatically returns to 0. 0: Normal CRC calculation 1: CRC engine reset
14 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 0	CRC_CT [11:0]	H'000	R	CRC Engine Input Data Count The number of data items that have been input to the CRC engine can be read. After the data count reaches 4096, it will wrap around to H'000.

55.3.16 CRC Engine Input Data Register (CRCIR)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	CRC_IN[11:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

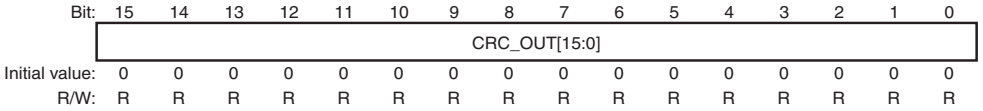
Bit	Bit Name	Initial Value	R/W	Description
15 to 12	—	All 0	W	Reserved These bits are always read as 0. The write value should always be 0.
11 to 0	CRC_IN [11:0]	H'00	W	CRC Engine Input Data The data to be input to the CRC engine should be specified here. The specified data is shifted into the CRC engine calculation register, starting with the LSB (CRC_IN0) of the data into the MSB (CRC_REG15) side of the calculation register.

55.3.17 CRC Engine Calculation Register (CRCCR)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CRC_REG[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

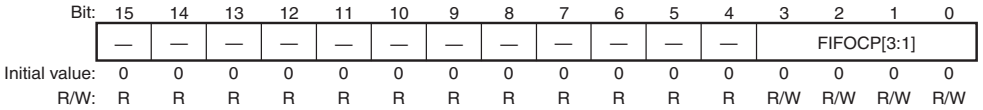
Bit	Bit Name	Initial Value	R/W	Description
15 to 0	CRC_REG [15:0]	H'0000	W	CRC Engine Calculation Data This is a writable register used for diagnosis. Typically, there is no need to access this register.

55.3.18 CRC Engine Output Data Register (CRCOR)



Bit	Bit Name	Initial Value	R/W	Description
15 to 0	CRC_OUT [15:0]	H'0000	R	CRC Engine Output Data The result of calculation in the CRC engine can be read. The result of calculation is shifted into CRC_OUT[15].

55.3.19 FIFO Current Pointer (FIFOCP)



Bit	Bit Name	Initial Value	R/W	Description
15 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	FIFOCP[3:0]	H'0	R/W	These bits indicate the number of a FIFO where received data and status from the serial engine are stored. These are incremented by one after reception and wrap from H'F to H'0. These are valid when FIFOEN is 1. These are initialized when FIFOCLR is 1.

55.3.20 FIFO Follow Pointer (FIFOFP)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	FIFOFP[3:1]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	FIFOFP[3:0]	H'0	R/W	These bits indicate the number of the FIFO that is waiting for DMA transfer. These are incremented by one after transmission and wrap from H'F to H'0. These are valid when FIFOEN is 1 and the DMAONE bit triggers the DMA transfer. These are initialized when FIFOCLR is 1.

55.3.21 Receive Status FIFO Interrupt Mask (FIFORSMSK)

ビット:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FREM	–	–	–	TROVM	–	RSM[9]	RSM[8]	–	–	–	FPOVM	–	–	DMA TEM	VAL IDM
初期値:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	FREM	0	R/W	Masks the RS[15] bit interrupts of all the 16 FIFORS register planes. 1: Masks all the interrupts. 0: Masks no interrupts.
14 to 12	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
11	TROVM	0	R/W	Masks the TROV bit interrupts of all of the 16 FIFORS register planes. 1: Masks all the interrupts. 0: Masks no interrupts.
10	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
9	RSM[9]	0	R/W	Masks the RS[9] bit interrupts of all of the 16 FIFORS register planes. 1: Masks all the interrupts. 0: Masks no interrupts.
8	RSM[8]	0	R/W	Masks the RS[8] bit interrupts of all of the 16 FIFORS register planes. 1: Masks all the interrupts. 0: Masks no interrupts.
7 to 5	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	FPOVM	0	R/W	Masks the FPOV bit interrupts of all of the 16 FIFORS register planes. 1: Masks all the interrupts.. 0: Masks no interrupts.
3 to 2	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	DMATEM	0	R/W	Masks the DMATE bit interrupts of all of the 16 FIFORS register planes. 1: Masks all the interrupts. 0: Masks no interrupts.
0	VALIDM	0	R/W	Masks the VALID bit interrupts of all of the 16 FIFORS register planes. 1: Masks all the interrupts. 0: Masks no interrupts.

55.3.22 Receive Status FIFO Interrupt Source OR (FIFORSOR)

FIFORSOR shows the ORed value of each interrupt source of all the 16 FIFORS register planes.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FREO	—	—	—	TROVO	—	RSO[9]	RSO[8]	—	—	—	FPOVO	—	—	DMATE	VALID
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	FREO	0	R	Shows the ORed value of the RS[15] bits of all the 16 FIFORS register planes.
14 to 12	—	0	R	Reserved
11	TROVO	0	R	Shows the ORed value of the TROV bits of all the 16 FIFORS register planes.
10	—	0	R	Reserved
9	RSO[9]	0	R	Shows the ORed value of the TROV bits of all the 16 FIFORS register planes.
8	RSO[8]	0	R	Shows the ORed value of the TROV bits of all the 16 FIFORS register planes.
7 to 5	—	0	R	Reserved
4	FPOVO	0	R	Shows the ORed value of the FPOV bits of all the 16 FIFORS register planes.
3 to 2	—	0	R	Reserved
1	DMATEO	0	R	Shows the ORed value of the DMATE bits of all the 16 FIFORS register planes.
0	VALIDO	0	R	Shows the ORed value of the VALID bits of all the 16 FIFORS register planes.

55.3.23 FIFO Select (FIFOSEL)

FIFOSEL specifies the number of the FIFORS register to be accessed.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	FIFOSEL[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	FIFOSEL[3:0]	H'0	R/W	Specifies the number of FIFORS and FIFORFL to be accessed in hexadecimal value.

55.3.24 Receive Status FIFO (FIFORS)

There are 16 planes of FIFORS numbered from 0 to 15. Each of them is used sequentially beginning with plane 0 to store an interrupt source corresponding to each received frame.

This register is common to SIR/MIR/FIR modes. However, the RS[9] and RS[8] bit specifications differ between SIR and MIR/FIR modes. For details, see each bit description.

Set the desired plane number in the FIFOSEL register before making read/write access to it.

To avoid overrun, erase the specified FIFORS register by writing all 0s to it as soon as possible after the FIFORS register and the buffer RAM data are read.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FRE	—	—	—	TROV	—	RS[9]	RS[8]	—	—	—	FPOV	—	—	DMATE	VALID
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R/W	R	R/W	R/W	R	R	R	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	FRE	0	R/W	Frame Receive End Indicates that one frame has been received. This bit is common to SIR/MIR/FIR modes. 0: One frame has not been received. 1: One frame has been received.
14 to 12	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
11	TROV	0	R/W	Transfer Area Overflow Indicates that the quantity of the received data bytes has exceeded the buffer RAM area, causing a transfer area overflow. This bit is common to SIR/MIR/FIR modes. When a transfer area overflow occurs, the buffer RAM data may be overwritten before being read out. 0: A transfer area overflow has not occurred. 1: A transfer area overflow has occurred.
10	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
9	RS[9]	0	R/W	This bit specification differ between SIR and MIR/FIR modes. In SIR mode: Timeout Indicates that the interval between the received data bytes in the same frame exceeds the timeout time (1 ms or 10 ms) specified in IRCFR, causing a timeout. 0: A timeout has not occurred. 1: A timeout has occurred. In MIR/FIR modes: Abort Detection Indicates that an illegal pulse code has been detected in the received data (= abort detection). 0: No illegal pulse codes have been detected. 1: An abort has been detected.

Bit	Bit Name	Initial Value	R/W	Description
8	RS[8]	0	R/W	This bit specification differ between SIR and MIR/FIR modes. In SIR mode: Framing Error Indicates that no stop bit is appended to the received data, causing a framing error. 0: A framing error has not occurred. 1: A framing error has occurred. In MIR/FIR modes: CRC Error Indicates that a CRC error has occurred in the received data. 0: A CRC error has not occurred. 1: A CRC error has occurred.
7 to 5	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	FPOV	0	R/W	FIFO Pointer Overrun This bit is turned on when the serial engine block writes the next frame receive status if the VALID bit is 1. All other bits than FPOV in the FIFORS register are unchanged. 0: No FIFO pointer overrun has occurred. 1: A FIFO pointer overrun has occurred.
3 to 2	—	0	—	Reserved These bits are always read as 0. The write value should always be 0.
1	DMATE	0	R/W	DMA Transfer End This bit is turned on when one frame DMA transfer has completed. 0: A DMA transfer has not completed. 1: A DMA transfer has completed.

Bit	Bit Name	Initial Value	R/W	Description
0	VALID	0	R/W	FIFORS Valid This bit is turned on when the status information on a newly received frame is stored in the FIFORS register. 0: There is no valid status information. 1: There is valid status information.

55.3.25 Receive Frame Length FIFO (FIFORFL)

There are 16 planes of FIFORFL numbered from 0 to 15. Each of them is used sequentially beginning with plane 0 to store a received frame length.

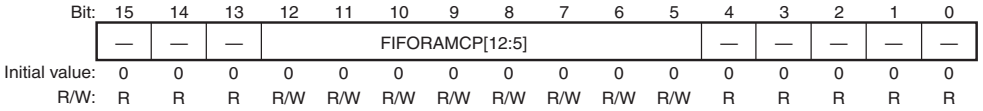
This register is common to SIR/MIR/FIR modes.

Set the desired plane number in the FIFOSEL register before making read/write access to it.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	FIFORFL[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	FIFORFL[3:0]	H'0	RW	Received Frame Length These bits indicate the number of data bytes received in the frame. In SIR-UART mode, the indicated number of data bytes includes framewrapping. In MIR and FIR modes, the indicated number of data bytes excludes framewrapping; only the IrLAP payload part is considered.

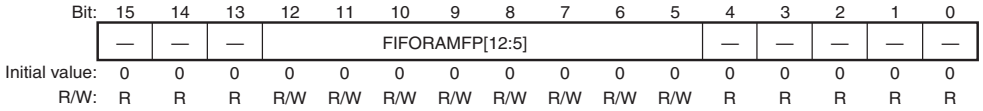
55.3.26 FIFORAM Current Pointer (FIFORAMCP)



Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	FIFORAMCP[12:5]								—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 5	FIFORAMCP [12:5]	H'0	RW	FIFORAM Current Pointer These bits represent the pointer to the buffer RAM that is used as FIFO by the serial engine, where the data to be received in the next one frame will be written. The pointer is updated when the data received in one frame is written. The pointer value always starts on a 32-bit boundary. The current FIFORAMCP indicates the value that is obtained by adding the previous FIFORFL (received data length) to the previous FIFORAMCP and then rounding up to the next 32-bit boundary.
4 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

55.3.27 FIFORAM Follow Pointer (FIFORAMFP)



Bit	Bit Name	Initial Value	R/W	Description
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 5	FIFORAMFP [12:5]	H'0	RW	FIFORAM Follow Pointer These bits provide the offset address when the received data in the buffer RAM that is used as FIFO is to be read. Set a value that is obtained by adding the FIFORFL (the previously received frame length) to the previous FIFORAMFP and then rounding up to the next 32-bit boundary. For DMA transfer, the value is calculated and set automatically. When reading the received data from the buffer RAM that is used as FIFO, read it sequentially from the start address of the buffer RAM with incrementing addresses.
4 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

55.3.28 Bus Interface Control (BIFCTL)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FIFO CLR	—	FIF OEN	—	—	—	—	BIG	DMA CLR	—	—	—	—	—	—	DMA ONE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R/W	R	R	R	R	R/W	R/W	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	FIFOCLR	0	R/W	FIFO Clear Write 1 then 0 to this bit to initialize the FIFO control block registers at a time. 0: Does not initialize the FIFO control block. 1: Initializes the FIFO control block. Registers to be affected: FIFOSEL, FIFOCP, FIFOFP, FIFORS[0-F], FIFORAMCP, FIFORAMFP, FIFO_RFL[0-F]
14	—	All 0	R	Reserved This bit is always read as 0. The write value should always be 0.
13	FIFOEN	0	R/W	FIFO Enable 0: Uses the receive buffer RAM as a single continuous area. 1: Uses the receive buffer RAM as 16 planes of FIFO.
12 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	BIG	0	R/W	Endian Switch 0: Little endian 1: Big endian
7	DMACLR	0	R/W	DMA Clear Write 1 then 0 to this bit to initialize the DMA control block registers at a time. 0: Does not initialize the DMA control block. 1: Initializes the DMA control block. Register to be affected: DMAONE

Bit	Bit Name	Initial Value	R/W	Description
6 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	DMAONE	0	R/W	DMA Single Request This bit initiates a DMA transfer request for one frame. This bit is cleared at the end of the DMA transfer automatically. The request must be initiated when there is a frame waiting for DMA transfer. 0: Does not request DMA transfer. 1: Requests DMA transfer for one frame.

55.4 Operation

55.4.1 Frame Format

The IrDA performs communication in the frame format shown in Figure 55.2. In SIR-UART mode, framewrapping through software is required, in which the XBOF, BOF, FCS, and EOF codes are appended before and after the payload data (shaded in the figure). In MIR and FIR modes, the hardware automatically performs framewrapping for the IrLAP payload.

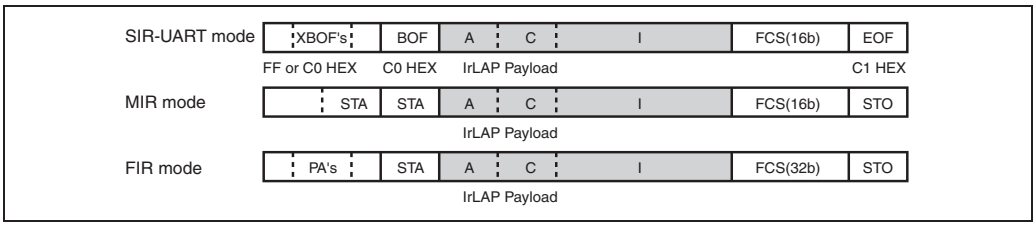


Figure 55.2 Frame Format

55.4.2 Buffer RAM

The IrDA incorporates a 5120-kbyte buffer RAM. In reception, the FIFOEN bit in the BIFCTL register can be used to switch between the non-FIFO and FIFO modes.

(1) Non-FIFO mode

In SIR-UART mode, one frame of framewrapped data is stored in this RAM, whereas in MIR and FIR modes, only the IrLAP payload part in one frame is stored.

Since the buffer RAM is allocated to the linear address space in terms of the CPU, the CPU can access data at any address in the buffer RAM area. When transmission is started, the SIR-UART or the MIR&FIR engine reads data sequentially, starting at H'000, the start address of the buffer RAM. Similarly, when reception is started, the SIR-UART or the MIR&FIR engine writes data sequentially, starting at H'000, the start address of the buffer RAM.

(2) FIFO mode

In transmission, the buffer RAM cannot be used in the FIFO mode, so the FIFOEN bit must be written to 0.

The buffer RAM can be used as up to 16 planes of FIFO only in reception by writing 1 to the FIFOEN bit.

The size of one FIFO plane varies from 0 to 5120 bytes depending on the number of received data bytes in one frame.

Receive operations are described in details below with examples.

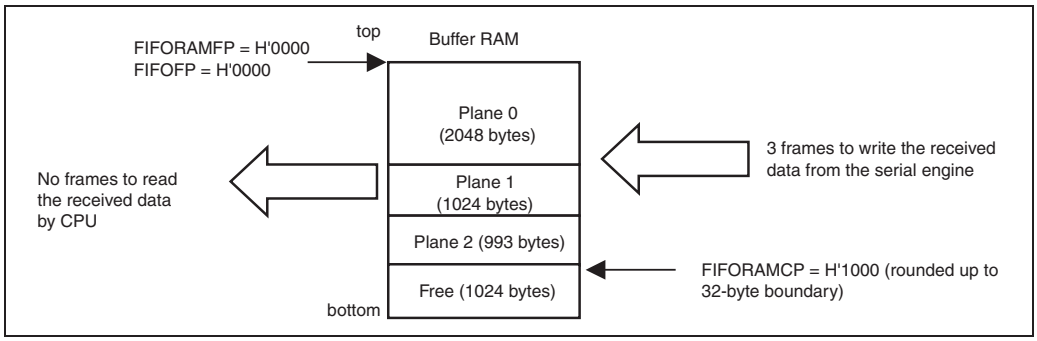


Figure 55.3 Buffer RAM FIFO Operation Example 1

In Example 1, 3 received frames are written from the serial engine to the buffer RAM and no received frames are read from the buffer RAM by the CPU. After these operations, FIFORAMCP points at H'1000 as 933 bytes of plane 2 is rounded up to 32-byte boundary. This leaves a free area with a size of 1024 bytes.

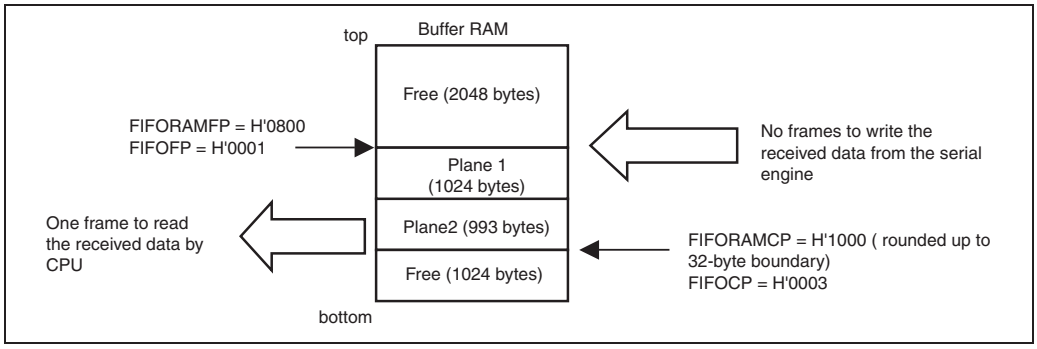


Figure 55.4 Buffer RAM FIFO Operation Example 2

Example 2 shows the buffer RAM after one frame of reading the received data by CPU. In this example, the size of free area is increased to 3072 bytes. FIFORAMFP points at H'0800. This pointer value is updated automatically at the end of a DMA transfer as long as it is initiated by the DAMONE register.

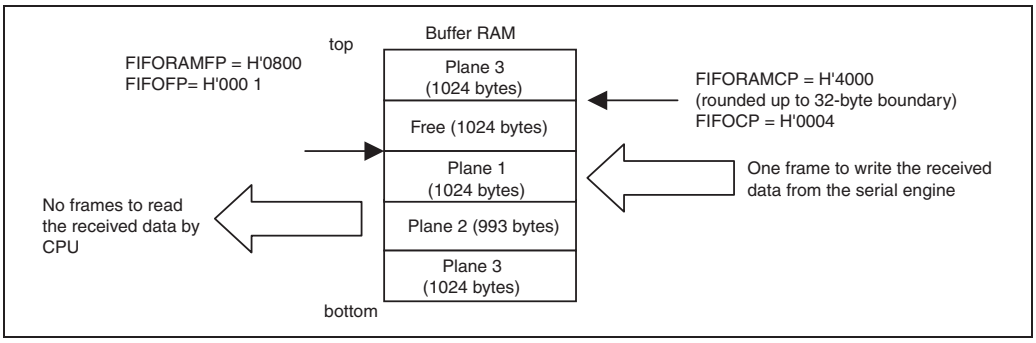


Figure 55.5 Buffer RAM FIFO Operation Example 3

Example 3 shows the buffer RAM after one frame (2048 bytes) of writing the received data from the serial engine to 3 planes. The size of free area is decreased to 1024 bytes. FIFORAMCP is wrapped around to H'0400.

55.4.3 DMA Transfer

The IrDA can generate DMA transfer requests in frame units to read the received data stored in the buffer RAM.

The DMA transfer control flow is shown below.

1) Initiate a serial reception with the FIFOEN bit set to 1.
2) Wait for the reception to complete (FRE=1, bit 15 in FIFORS).
3) Set up the DMAC module.
   (1) Set the value that is obtained by rounding up the FIFORFL register value pointed by the FIFOFP register to 32-byte boundary in DMATCR.

   To transfer more than one frame at a time, set the value that is obtained by rounding up the FIFORFL register values for all frames on frame-by-frame basis and summing up all the resulting values in DMATCR.
   (2) Set the DMA transfer size to 32 bytes (TS[3:0]=0100).
   (3) Set the destination address mode to increment (DM[1:0]=01).
   (4) Set the source address mode to increment (SM[1:0]=01).

(5) Set the resource selection to select DMA extended resource selector (RS[3:0]=1000).
(6) Set the DMA source address register to the start address of the IrDA buffer RAM (DMASAR=H'E6D00000).
(7) Set the DMA destination address register to the destination memory address.
(8) Select the IrDA module in the DMA extended resource selector (DMARS).
(9) Set the DMA enable (DE=1 in the DMACHCR register and DME=1 in the DMAOR register).

4) Start one frame transfer (DMAONE=1).
5) Wait for the read from the IrDA memory to complete (check if DMATE=1 in FIFO_RS).
Repeat from step 4) as required if more than one frame length is set in DMATCR during the DMAC module set-up.
6) Wait for the store to the destination memory to complete (check if TE=1 in DMACHCR).

55.4.4 Data Transfer

The IrDA is in SIR-UART mode after reset; it can be placed in MIR or FIR mode by modifying IRTMR.

(1) Transmission in SIR-UART Mode

In SIR-UART mode transmission, after transmit data with frame wrapping is written to the buffer RAM by the CPU or the DMAC, writing the number of data bytes to be transmitted to IRTFLR and then writing 1 to the TE bit in IRTCTR actually starts transmitting the data.

Once transmission is enabled, the SIR-UART engine reads one byte of data at a time from the buffer RAM to perform transmission. The SIR-UART engine continues reading data from the buffer RAM until it has read the EOF code or the quantity of data bytes equal to the number specified in IRTFLR. When the EOF code has been transmitted, the TE bit is cleared to 0 and a transmit end interrupt is generated simultaneously. This switches the mode to SIR-UART reception mode if auto-receive mode is set.

Notes: 1. If the ARMOD bit in IRTCTR is 1 when transmission has completed, the hardware automatically writes 1 to the RE bit in IRRCTR thus enabling SIR-UART mode reception.
In auto-receive mode, the received data overwrites the transmit data in the buffer RAM.
2. Set the correct transmit frame length to IRTFLR and set the correct EOF code (H'C1) to the buffer RAM. If the EOF code is not found within the byte position specified by

IRTFLR, a transmit end interrupt is not generated. If the incorrect EOF code is set, clear the TE bit to 0 and then set the bit to 1 to enable transmission again.

(2) Reception in SIR-UART Mode

In SIR-UART mode reception, writing 1 to the RE bit in IRRCTR enables reception. Once reception is enabled, the SIR-UART engine waits for the data to be received, and on receiving data, the SIR-UART engine writes one byte of data at a time to the buffer RAM. In this case, the SIR-UART engine writes the entire framewrapped data. Reading IRRFLR gives the number of bytes written to the buffer RAM.

When the EOF code has been successfully received and written to the buffer RAM, a receive end interrupt is generated and the RE bit in IRRCTR is cleared to 0 simultaneously.

If the quantity of the received data bytes with framewrapping exceeds the buffer RAM area, a transfer area overflow interrupt is generated. If the received data has some faults which subsequently lead to a missing stop bit, a framing error interrupt is generated.

If the receive pulses are interrupted during reception of a frame of data, thus disabling data reception for a specified time, a timeout interrupt is generated. The timeout time (no timeout, 1 ms, or 10 ms) can be specified in IRCFR.

Note: A receive end interrupt is not generated if either a transfer area overflow interrupt, a framing error interrupt, or a timeout interrupt is generated.

(3) Transmission in MIR and FIR Modes

In MIR and FIR mode transmission, after transmit data without framewrapping is written to the buffer RAM by the CPU or the DMAC, writing the number of data bytes to be transmitted to IRTFLR and then writing 1 to the TE bit in IRTCTR actually starts transmitting the data.

Once transmission is enabled, the MIR&FIR engine reads one byte of data at a time from the buffer RAM to perform transmission. In this case, the MIR&FIR engine appends the codes such as preamble (PA), start flag (STA), frame check sequence (FCS), and/or stop flag (STO) before and after the IrLAP payload data depending on the mode. The MIR&FIR engine reads the quantity of data bytes equal to the number specified in IRTFLR from the buffer RAM. When STO has been transmitted, the TE bit is cleared to 0 and a transmit end interrupt is generated simultaneously.

Note: If the ARMOD bit in IRTCTR is 1 when transmission has completed, the hardware automatically writes 1 to the RE bit in IRRCTR thus enabling MIR or FIR mode reception. In auto-receive mode, the received data overwrites the transmit data in the buffer RAM.

(4) Reception in MIR and FIR Modes

In MIR and FIR mode reception, writing 1 to the RE bit in IRRCTR enables reception. Once reception is enabled, the MIR&FIR engine waits for PA or STA depending on the mode. On confirming the appropriate STA sequence, the MIR&FIR engine regards the following received data as the IrLAP payload data, thus writing one byte of the data at a time to the buffer RAM.

When the STO flag has been received, a receive end interrupt is generated and the RE bit in IRRCTR is cleared to 0 simultaneously to complete reception.

After receiving the STO flag, the hardware performs a CRC check. If a CRC error is detected, a CRC error interrupt is generated. When reception has been successfully ended without a CRC error, only the IrLAP payload data is written to the buffer RAM; no CRC data is written. Reading IRRFLR indicates the number of bytes having been written to the buffer RAM.

If the quantity of the received data bytes without framewrapping exceeds the buffer RAM area, a transfer area overflow interrupt is generated. If an illegal code has been detected in the received data, an abort detection interrupt is generated.

Note: A receive end interrupt is not generated if either a transfer area overflow interrupt or an abort detection interrupt is generated.

55.4.5 Interrupts

It is possible to generate the SIR-UART mode interrupts, the MIR/FIR mode interrupts, or the FIFO mode interrupts that are selected by IRTMR.

The output of the SIR-UART mode interrupts and the MIR/FIR mode interrupts can be masked as required through the corresponding interrupt mask registers. The output of the FIFO mode interrupts can be masked on the basis of interrupt sources that are ORed between all of 16 planes of FIFO interrupt statuses. The sources of the generated interrupts can be determined through the corresponding interrupt source registers. The interrupt output pin continues outputting a low level signal until all the interrupt sources have been cleared or masked.

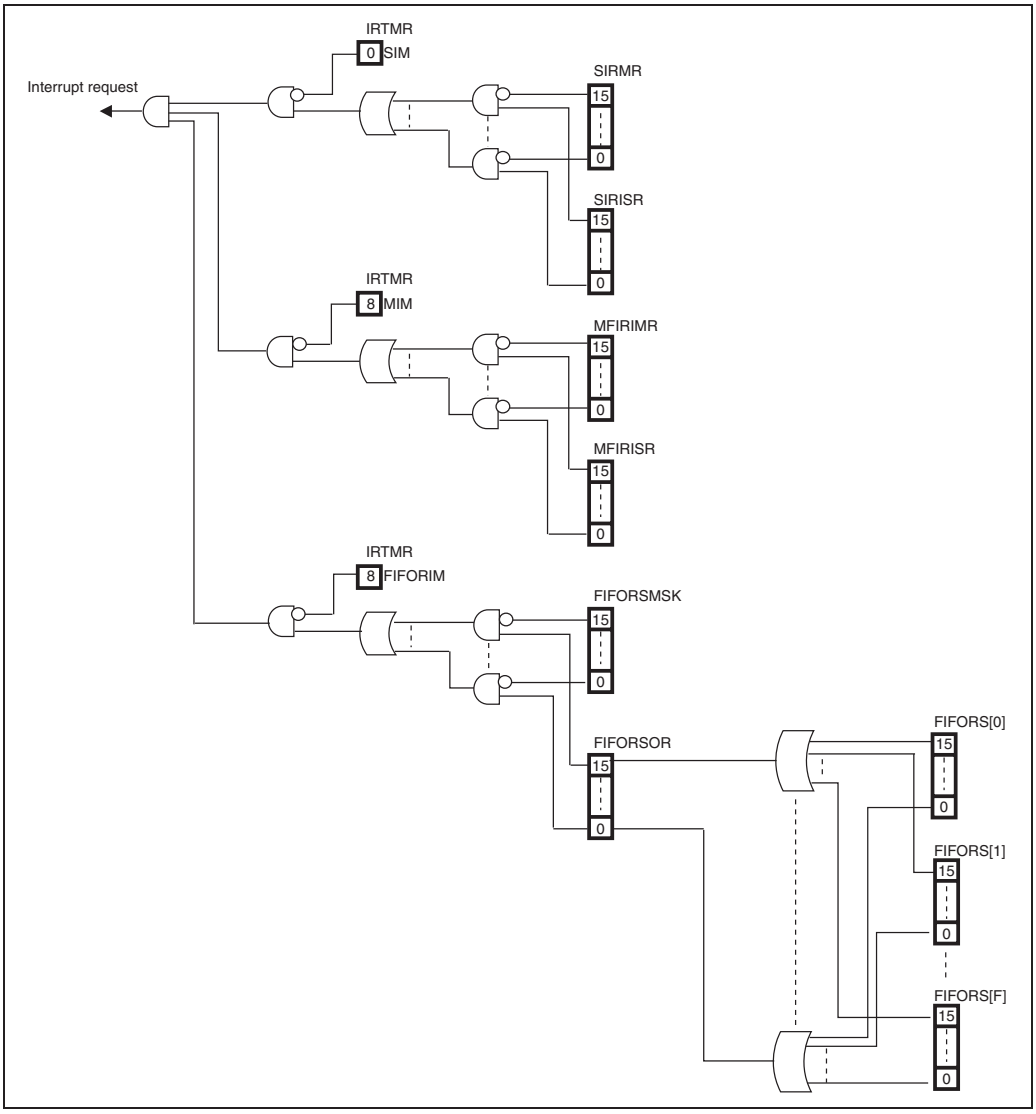


Figure 55.6 Interrupt Related Diagram

55.4.6 SIP Output and Abort

(1) SIP Output

In MIR and FIR modes, SIP is output to notify a device with a communication speed of 115.2 kbits/s or slower that communication is currently being performed in MIR or FIR mode. When 1 is written to the SIP bit in IRCFR, a 1.6-µs-wide SIP pulse is output within 8.7 µs. SIP must be output while transmission is disabled. In MIR and FIR modes, if transmission is enabled immediately after SIP has started to be output, the start of data transmission is suspended while SIP is output; transmission starts after the 8.7-µs duration. The 500-ms interval between SIPs should be measured using software.

(2) Abort

In MIR and FIR modes, the abort output function and abort detection function are available.

The abort output is started or terminated by setting the ABT bit in IRCFR to 1 or 0, respectively. Specifically, the abort state continues after PA and STA are transmitted depending on the mode. Abort output is different from normal data transmission in that it must be output while transmission is disabled.

In reception, if an illegal code has been detected between the STA flag and the following STO flag received, it is regarded as the abort state.

In SIR-UART mode, abort output and abort detection should be implemented through software. In transmission, the abort state is output by writing a character sequence indicating the abort state in the frame. In reception, the received frame is checked through software to see if it contains a character sequence indicating the abort state.

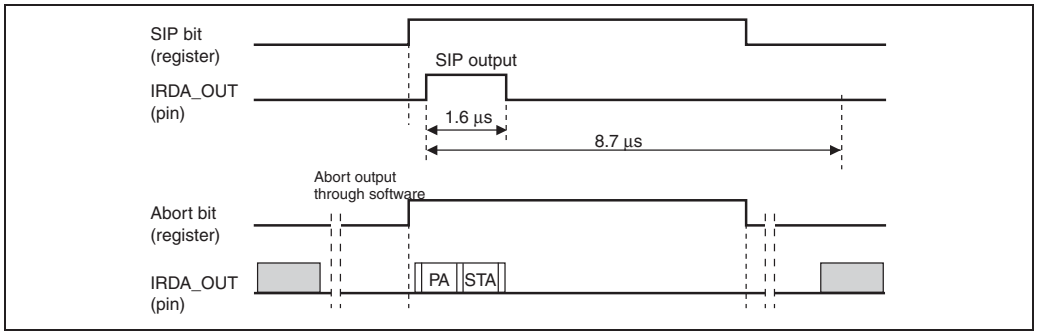


Figure 55.7 SIP Output and Abort Output

55.4.7 Pulse Modulation and Demodulation

Pulse modulation and demodulation of transmit and receive data are shown in Figure 55.4. In SIR-UART mode, either 3/16T or 1.63 μs can be selected through programming as the width of the pulse to be transmitted. In MIR and FIR modes, the pulse width is controlled through the hardware.

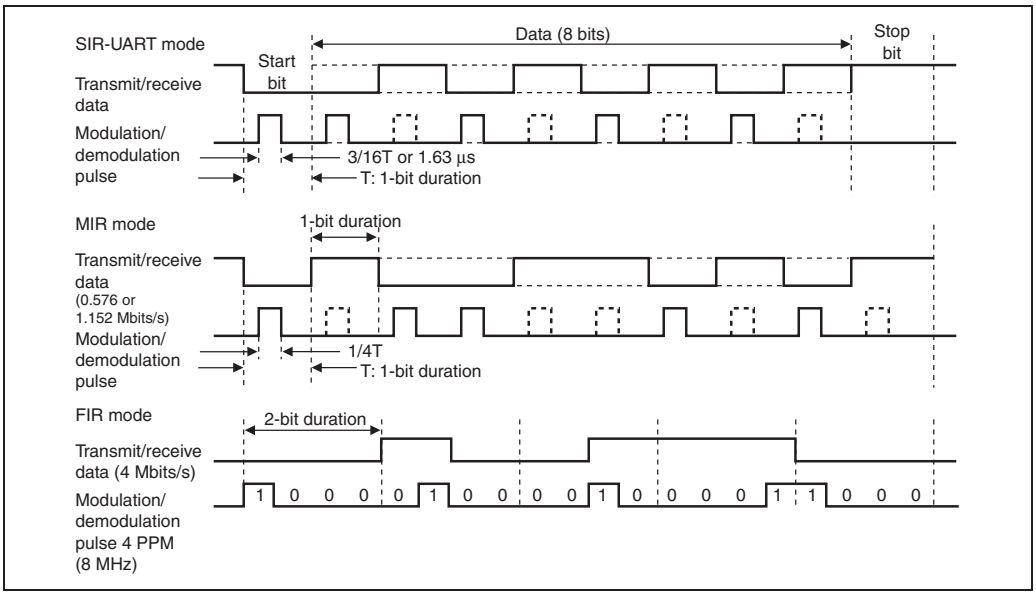


Figure 55.8 Pulse Modulation and Demodulation

55.4.8 Communication Clock

(1) Communication Clock in FIR Mode

In FIR mode, the 48-MHz input clock is used without modification for pulse modulation and demodulation.

(2) Communication Clock in MIR Mode

In MIR mode, the 48-MHz clock is used without modification as the communication clock.

In MIR mode, data is generated at a rate of 1.152 or 0.576 Mbits/s based on the 48-MHz clock; therefore, the variation point (leading edge) of each data bit may have a maximum of ±6.95-ns jitter compared to the case in which data is generated based on the communication clock given by 16 times the 1.152 Mbits/s rate (18.432 MHz). This results in a maximum of ±13.9-ns jitter between two arbitrary data variation points. This value is ±1.6% and ±0.8% for the transfer rates of 1.152 Mbits/s and 0.576 Mbits/s, respectively.

The IrDA standard allows ±0.1% rate tolerance in MIR mode.

If the input clock signal contains some error, the error accumulates between a certain pulse to the next pulse. The maximum error (±0.1% × 7) is produced when STA code B'01111110 is sent based on the clock with a tolerance of ±0.1%.

Therefore, the maximum IrDA jitter in MIR mode transmission is calculated as follows:

For 1.152 Mbits/s: ±1.6% + (±0.1%) × 7 = ±2.3%

For 0.576 Mbits/s: ±0.8% + (±0.1%) × 7 = ±1.5%

The above values fall within the ±2.9% range prescribed in the IrDA standard. The margin for each rate is as follows:

For 1.152 Mbits/s: 868 ns × (±0.6%) = ±5.2 ns

For 0.576 Mbits/s: 1,736 ns × (±1.4%) = ±24.3 ns

(3) Communication Clock in SIR-UART Mode

In SIR-UART mode, the communication clock frequency must be 16 times 115.2 kHz, that is, 1.8432 MHz. The frequency tolerance is ±0.87%. To satisfy this condition, the IrDA divides the frequency of the 48-MHz input clock signal by 26 to generate a 1.846-MHz internal communication clock signal. The resultant frequency error is +0.16%.

55.4.9 IrDA Operation Example

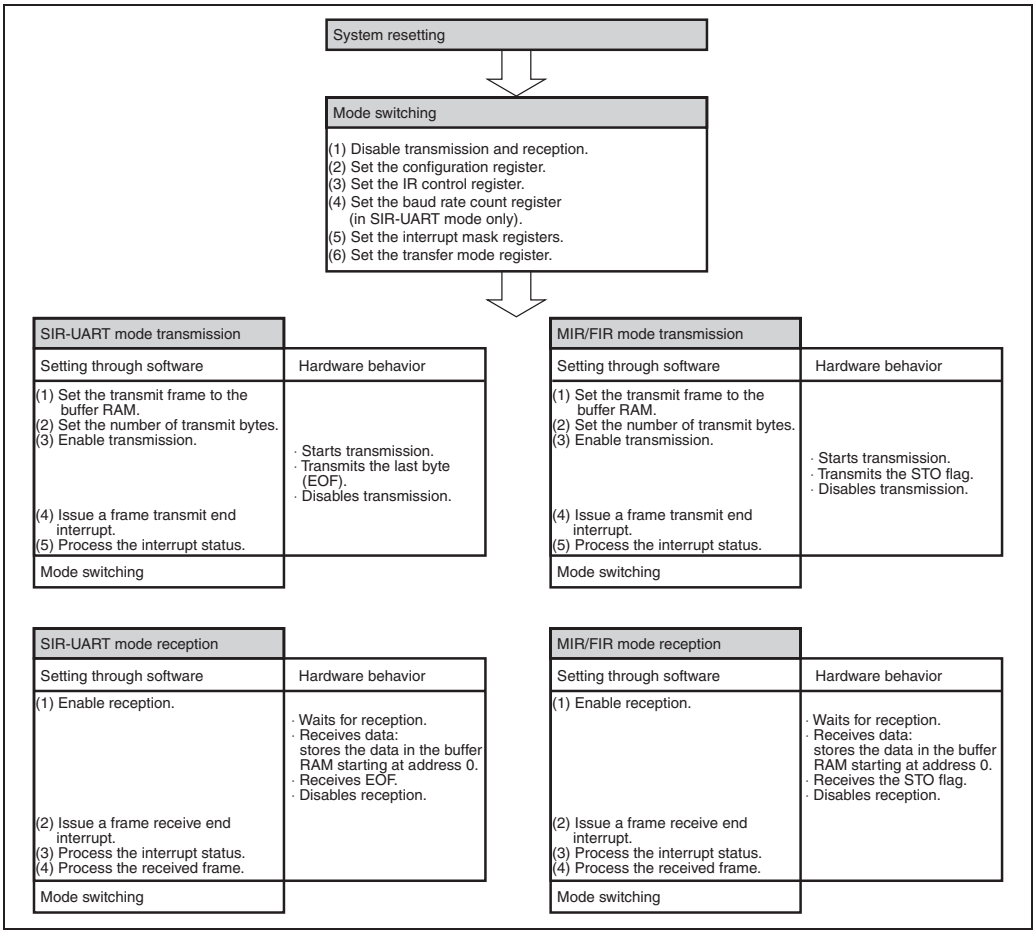


Figure 55.9 IrDA Operation Example

55.4.10 CRC Engine (16-Bit CRC)

(1) CRC Engine (16-Bit CRC) Configuration

The CRC engine consists of an input data register, a byte counter, a CRC engine calculation register (CRCCR), and a CRC engine output register (CRCOR). Table 55.5 summarizes the CRC engine functions. Figure 55.6 shows a configuration of the CRC engine.

Table 55.5 Summary of CRC Engine Functions

Item	Function
Generator polynomial	X16 + X12 + X5 + 1
Data input	Byte write
	CRC calculation in 8-bit units beginning with the lower bits
CRC output	16-bit CRC generator output
	The result of CRC calculation is shifted into the upper bits in order.
Maximum data length	4096 bytes

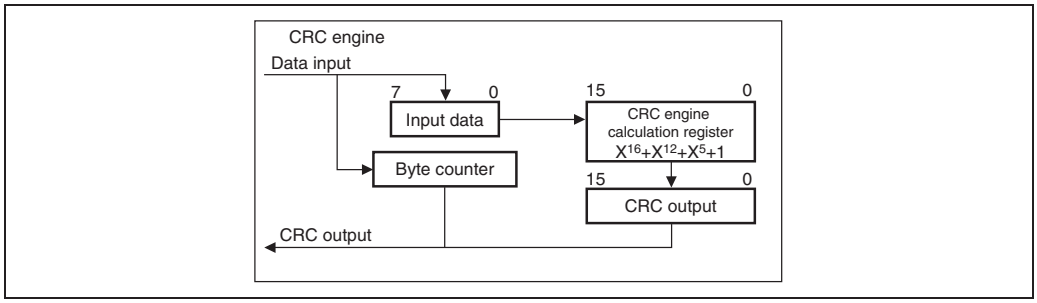


Figure 55.10 CRC Engine Configuration

(2) CRC Engine Operation

Writing 8-bit input data to the CRC engine starts CRC calculation in 8-bit units beginning with the lower bits to output a 16-bit calculation result. Figure 55.7 gives an overview of the CRC engine calculation.

An example of CRC calculation is shown here. After resetting the registers, write H'CC, H'F5, H'F1, and H'A7 as input data in that order. The resultant byte count will be H'4 and H'51DF will be output as the CRC calculation result.

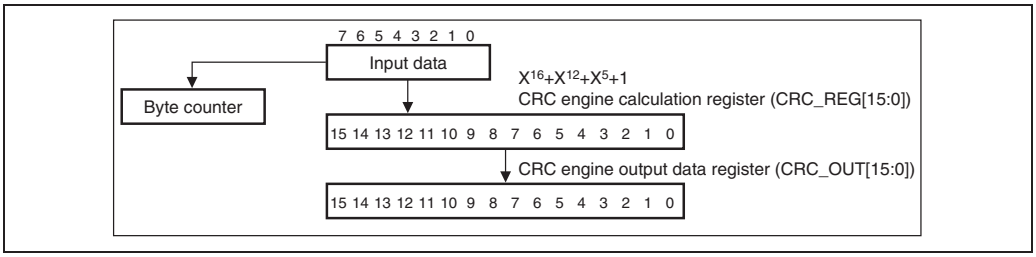


Figure 55.11 CRC Engine Operation

57. IO Port(GPIO)

57.2 Overview

IO Port(GPIO) consists of control registers to select functions and input or output direction of the multiplexed pins and general input/output port registers. Pin functions and input/output directions can be selected for each pin irrespective of operating mode of the LSI.

Table 57.1 List of Multiplexed Pins

Side	Power Gr	Pin name	I/O	Initial Function	Function0	Function1	Function2	Function3	Function4	Function5	Function6	Function7	IRQ	PullU/D	Tolerant	*2
D	VCCQ	BBIF2_TSCK	IO	0	PORT0	BBIF2_TSCK1								D		
D	VCCQ	BBIF2_TSYNC	IO	0	PORT1	BBIF2_TSYNC1								D		
D	VCCQ	BBIF2_TXD	O	0	PORT2	BBIF2_TXD1								-		
D	VCCQ	BBIF2_RXD	I	0	PORT3	BBIF2_RXD								D		
D	VCCQ	FSIACK	I	0	PORT4	FSIACK	FSIBCK						IRQ2	D		
D	VCCQ	FSIAILR	I	0	PORT5	FSIAILR	SCIFA4_RXD						IRQ2	D		
D	VCCQ	FSIAIBT	IO	0	PORT6	FSIAIBT	SCIFA4_TXD						IRQ0	U/D		
D	VCCQ	FSIAISLD	I	0	PORT7	FSIAISLD								D		
D	VCCQ	FSIAOMC	IO	0	PORT8	FSIAOMC	SCIFA5_RXD						IRQ3	D		
D	VCCQ	FSIAOLR	O	0	PORT9	FSIAOLR								-		
D	VCCQ	FSIAOBT	O	0	PORT10	FSIAOBT								-		
D	VCCQ	FSIAOSLD	O	0	PORT11	FSIAOSLD	FSIASPDIF							-		
D	VCCQ	FMSOCK	IO	0	PORT12	FMSOCK	SCIFA5_TXD						IRQ1	U/D		
D	VCCQ	FMSOOLR	IO	0	PORT13	FMSOOLR	FMSIOLR							D		
D	VCCQ	FMSOOBT	IO	0	PORT14	FMSOOBT	FMSIOBT							D		
D	VCCQ	FMSOSLD	O	0	PORT15	FMSOSLD	FSIASPDIF							-		
D	VCCQ	FMSOILR	IO	0	PORT16	FMSOILR	FMSIILR	VIO_CKO1					IRQ3	D		
D	VCCQ	FMSOIBT	IO	0	PORT17	FMSOIBT	FMSIIBT	VIO_CKO2					IRQ4	D		
D	VCCQ	FMSISLD	I	0	PORT18	FMSISLD		IDIN_1					IRQ5	D		
D	VCCQ	A0	IO	2	PORT19	A0	BS_							-		
D	VCCQ	A1	IO	1	PORT20	A1								-		
D	VCCQ	A2	IO	1	PORT21	A2								-		
D	VCCQ	A3	IO	1	PORT22	A3								-		
D	VCCQ	A4	IO	1	PORT23	A4/FOE								-		
D	VCCQ	A5	IO	1	PORT24	A5/FCDE								-		
D	VCCQ	A6	IO	1	PORT25	A6								-		
D	VCCQ	A7	IO	1	PORT26	A7								-		
D	VCCQ	A8	IO	1	PORT27	A8								-		
D	VCCQ	A9	IO	1	PORT28	A9								-		
D	VCCQ	A10	IO	1	PORT29	A10								-		
D	VCCQ	A11	IO	1	PORT30	A11								-		
D	VCCQ	A12	IO	1	PORT31	A12								-		
D	VCCQ	A13	IO	1	PORT32	A13								-		
D	VCCQ	A14	IO	1	PORT33	A14								-		
D	VCCQ	A15	IO	1	PORT34	A15								-		
D	VCCQ	A16	IO	1	PORT35	A16								-		
D	VCCQ	A17	IO	1	PORT36	A17	MSIOF0_TSYNC							-		*1
D	VCCQ	A18	IO	1	PORT37	A18	MSIOF0_TSCK							-		*1

Side	Power Gr	Pin name	I/O	Initial Function	Function0	Function1	Function2	Function3	Function4	Function5	Function 6	Functio n7	IRQ	PullU/D	Tolerant	*2
D	VCCQ	A19	IO	1	PORT38	A19	MSIOF0_RXD							-		*1
D	VCCQ	A20	IO	1	PORT39	A20	MSIOF0_RSCK	MSIOF1_TSCK					IRQ6	-		*1
D	VCCQ	A21	IO	1	PORT40	A21	MSIOF0_RSYNC	MSIOF1_TSYNC					IRQ7	-		*1
D	VCCQ	A22	IO	1	PORT41	A22	MSIOF0_MCK0	MSIOF1_TXD		GPI0			IRQ8	-		*1
D	VCCQ	A23	IO	1	PORT42	A23	MSIOF0_MCK1	MSIOF1_RXD		GPI1			IRQ9	-		*1
D	VCCQ	A24	IO	1	PORT43	A24	MSIOF0_SS1	MSIOF1_SS1	SCIFA3_CTS_	GPO0				-		*1
D	VCCQ	A25	IO	1	PORT44	A25	MSIOF0_SS2	MSIOF1_SS2	SCIFA3_RTS_	GPO1				-		
D	VCCQ	A26	IO	1	PORT45	A26	MSIOF0_TXD							-		
R	VCCQ	D0	IO	1	PORT46	D0/NAF0								U		
R	VCCQ	D1	IO	1	PORT47	D1/NAF1								U		
R	VCCQ	D2	IO	1	PORT48	D2/NAF2								U		
R	VCCQ	D3	IO	1	PORT49	D3/NAF3								U		
R	VCCQ	D4	IO	1	PORT50	D4/NAF4								U		
R	VCCQ	D5	IO	1	PORT51	D5/NAF5								U		
R	VCCQ	D6	IO	1	PORT52	D6/NAF6								U		
R	VCCQ	D7	IO	1	PORT53	D7/NAF7								U		
R	VCCQ	D8	IO	1	PORT54	D8/NAF8		MMCD1_0						U		
R	VCCQ	D9	IO	1	PORT55	D9/NAF9		MMCD1_1						U		
R	VCCQ	D10	IO	1	PORT56	D10/NAF10		MMCD1_2						U		
R	VCCQ	D11	IO	1	PORT57	D11/NAF11		MMCD1_3						U		
R	VCCQ	D12	IO	1	PORT58	D12/NAF12		MMCD1_4						U		
R	VCCQ	D13	IO	1	PORT59	D13/NAF13		MMCD1_5						U		
R	VCCQ	D14	IO	1	PORT60	D14/NAF14		MMCD1_6						U		
R	VCCQ	D15	IO	1	PORT61	D15/NAF15		MMCD1_7						U		
R	VCCQ	CS0_N	IO	1	PORT62	CS0_								-		
R	VCCQ	CS2_N	O	1	PORT63	CS2_								-		
R	VCCQ	CS4_N	O	1	PORT64	CS4_								-		
R	VCCQ	CS5A_N	IO	0	PORT65	CS5A_	FMSICK	VINT_I					IRQ10	U		
R	VCCQ	CS5B_N	O	0	PORT66	CS5B_	FCE1_	MMCCLK1						U/D		
R	VCCQ	CS6A_N	IO	0	PORT67	CS6A_		MMCCMD1					IRQ11	U		
R	VCCQ	FCE0_N	O	1	PORT68	FCE0_								-		
R	VCCQ	RD_N	IO	1	PORT69	RD_/FSC								-		
R	VCCQ	WE0_N	IO	1	PORT70	WE0_/FWE								-		
R	VCCQ	WE1_N	IO	1	PORT71	WE1_								-		
R	VCCQ	CKO	O	1	PORT72	CKO								-		
R	VCCQ	FRB	I	1	PORT73	FRB								U		
R	VCCQ	WAIT_N	I	1	PORT74	WAIT_								U/D		
R	VCCQ	RDWR	IO	0	PORT75	RDWR								U/D		
L	VCCQ	MEMC_AD0	IO	0	PORT76	MEMC_AD0	BBIF1_RXD		GP_RX_FLAG					U/D		*2
L	VCCQ	MEMC_AD1	IO	0	PORT77	MEMC_AD1	BBIF1_TSYNC		GP_RX_DATA					U/D		*2
L	VCCQ	MEMC_AD2	IO	0	PORT78	MEMC_AD2	BBIF1_TSCK		GP_TX_READY					U/D		*2
L	VCCQ	MEMC_AD3	IO	0	PORT79	MEMC_AD3	BBIF1_TXD		GP_RX_WAKE					U/D		*2
L	VCCQ	MEMC_AD4	IO	0	PORT80	MEMC_AD4	BBIF1_RSCK		MP_TX_FLAG				IRQ12	U/D		*2
L	VCCQ	MEMC_AD5	IO	0	PORT81	MEMC_AD5	BBIF1_RSYNC		MP_TX_DATA				IRQ13	U/D		*2
L	VCCQ	MEMC_AD6	IO	0	PORT82	MEMC_AD6	BBIF1_FLOW		MP_RX_READY				IRQ14	U/D		*2
L	VCCQ	MEMC_AD7	IO	0	PORT83	MEMC_AD7	BB_RX_FLOW_N		MP_TX_WAKE				IRQ15	U/D		*2
L	VCCQ	MEMC_AD8	IO	0	PORT84	MEMC_AD8	MSIOF1_RSCK		MMCD0_0				IRQ16	U/D		*2
L	VCCQ	MEMC_AD9	IO	0	PORT85	MEMC_AD9	MSIOF1_RSYNC		MMCD0_1				IRQ17	U/D		*2
L	VCCQ	MEMC_AD10	IO	0	PORT86	MEMC_AD10	MSIOF1_MCK0		MMCD0_2				IRQ18	U/D		*2
L	VCCQ	MEMC_AD11	IO	0	PORT87	MEMC_AD11	MSIOF1_MCK1		MMCD0_3				IRQ19	U/D		*2
L	VCCQ	MEMC_AD12	IO	0	PORT88	MEMC_AD12	MSIOF1_TSCK		MMCD0_4					U/D		*2
L	VCCQ	MEMC_AD13	IO	0	PORT89	MEMC_AD13	MSIOF1_TSYNC		MMCD0_5					U/D		*2
L	VCCQ	MEMC_AD14	IO	0	PORT90	MEMC_AD14	MSIOF1_TXD		MMCD0_6					U/D		*2
L	VCCQ	MEMC_AD15	IO	0	PORT91	MEMC_AD15	MSIOF1_RXD		MMCD0_7					U/D		*2
L	VCCQ	MEMC_CS0	IO	0	PORT92	MEMC_CS0	MSIOF1_SS1		MMCCMD0				IRQ20	U/D		*2
L	VCCQ	MEMC_BUSCLK	IO	0	PORT93	MEMC_BUSCLK/MEMC_A0	MSIOF1_SS2	TPU0TO2					IRQ21	U/D		*2

Side	Power Gr	Pin name	I/O	Initial Function	Function0	Function1	Function2	Function3	Function4	Function5	Function 6	Function7	IRQ	PullU/D	Tolerant	*2
L	VCCQ	MEMC_CS1	IO	0	PORT94	MEMC_CS1/MEMC_A1	SCIFA2_CTS1_						IRQ22	U/D		*2
L	VCCQ	MEMC_ADV	IO	0	PORT95	MEMC_ADV/MEMC_DREQ0	SCIFA2_RTS1_						IRQ23	U/D		*2
L	VCCQ	MEMC_WAIT	IO	0	PORT96	MEMC_WAIT/MEMC_DREQ1	SCIFA2_TXD1							U		*2
L	VCCQ	MEMC_NOE	IO	0	PORT97	MEMC_NOE	SCIFA2_RXD1							U/D		*2
L	VCCQ	MEMC_NWE	IO	0	PORT98	MEMC_NWE	SCIFA2_SCK1							U/D		*2
L	VCCQ	MEMC_INT	O	0	PORT99	MEMC_INT		TPU0TO2	MMCCLK0					U/D		*2
U	VCCQ	VIO_VD	IO	0	PORT100	VIO_VD								D		
U	VCCQ	VIO_HD	IO	0	PORT101	VIO_HD								D		
U	VCCQ	VIO_D0	IO	0	PORT102	VIO_D0								D		
U	VCCQ	VIO_D1	IO	0	PORT103	VIO_D1								D		
U	VCCQ	VIO_D2	IO	0	PORT104	VIO_D2								D		
U	VCCQ	VIO_D3	IO	0	PORT105	VIO_D3								D		
U	VCCQ	VIO_D4	IO	0	PORT106	VIO_D4								U		
U	VCCQ	VIO_D5	IO	0	PORT107	VIO_D5								U		
U	VCCQ	VIO_D6	IO	0	PORT108	VIO_D6								U		
U	VCCQ	VIO_D7	IO	0	PORT109	VIO_D7								U		
U	VCCQ	VIO_D8	IO	0	PORT110	VIO_D8	I2C_SCL2							U		
U	VCCQ	VIO_D9	IO	0	PORT111	VIO_D9	I2C_SDA2							U		
U	VCCQ	VIO_D10	IO	0	PORT112	VIO_D10		TPU0TO3					IRQ24	D		
U	VCCQ	VIO_D11	IO	0	PORT113	VIO_D11		IDIN_0	IDIN_1					D		
U	VCCQ	VIO_D12	IO	0	PORT114	VIO_D12	I2C_SCL3	EXTLP_0	OVCN_1					U		
U	VCCQ	VIO_D13	IO	0	PORT115	VIO_D13	I2C_SDA3	OVCN2_0	PWEN_1					U		
U	VCCQ	VIO_D14	IO	0	PORT116	VIO_D14	I2C_SCL4	PWEN_0	EXTLP_1					U		
U	VCCQ	VIO_D15	IO	0	PORT117	VIO_D15	I2C_SDA4	OVCN_0	OVCN2_1					U		
U	VCCQ	VIO_CLK	IO	0	PORT118	VIO_CLK								U		
U	VCCQ	VIO_FIELD	IO	0	PORT119	VIO_FIELD							IRQ25	U		
U	VCCQ	VIO_CKO	IO	0	PORT120	VIO_CKO								U		
L	VCCQ	LCDD0	IO	0	PORT121	LCDD0		KEYOUT7	KEYIN0				IRQ26	D		
L	VCCQ	LCDD1	IO	0	PORT122	LCDD1		KEYOUT6	KEYIN1				IRQ27	D		
L	VCCQ	LCDD2	IO	0	PORT123	LCDD2		KEYOUT5	KEYIN2				IRQ28	D		
L	VCCQ	LCDD3	IO	0	PORT124	LCDD3		KEYOUT4	KEYIN3					D		
L	VCCQ	LCDD4	IO	0	PORT125	LCDD4		KEYOUT3						D		
L	VCCQ	LCDD5	IO	0	PORT126	LCDD5		KEYOUT2						D		
L	VCCQ	LCDD6	IO	0	PORT127	LCDD6		KEYOUT1						D		
L	VCCQ	LCDD7	IO	0	PORT128	LCDD7		KEYOUT0						D		
L	VCCQ	LCDD8	IO	0	PORT129	LCDD8		KEYIN7					IRQ29	U/D		
L	VCCQ	LCDD9	IO	0	PORT130	LCDD9		KEYIN6					IRQ30	U/D		
L	VCCQ	LCDD10	IO	0	PORT131	LCDD10		KEYIN5						U/D		
L	VCCQ	LCDD11	IO	0	PORT132	LCDD11		KEYIN4						U/D		
L	VCCQ	LCDD12	IO	0	PORT133	LCDD12		KEYIN3						U/D		
L	VCCQ	LCDD13	IO	0	PORT134	LCDD13	MSIOF2_RSCK	KEYIN2						U/D		
L	VCCQ	LCDD14	IO	0	PORT135	LCDD14	MSIOF2_RSYNC	KEYIN1						U/D		
L	VCCQ	LCDD15	IO	0	PORT136	LCDD15	MSIOF2_MCK0	KEYIN0						D		
L	VCCQ	LCDD16	IO	0	PORT137	LCDD16	MSIOF2_MCK1	TS_SPSYNC2		I2C_SCL3S			IRQ12	D		
L	VCCQ	LCDD17	IO	0	PORT138	LCDD17	MSIOF2_SS1		PWEN_1				IRQ31	D		
L	VCCQ	LCDD18	IO	0	PORT139	LCDD18	MSIOF2_SS2	IROUT						D		
L	VCCQ	LCDD19	IO	0	PORT140	LCDD19	SCIFA3_CTS_	IRDA_OUT	IROUT					D		
L	VCCQ	LCDD20	IO	0	PORT141	LCDD20	SCIFA3_RTS_	IRDA_IN						D		
L	VCCQ	LCDD21	IO	0	PORT142	LCDD21	SCIFA3_SCK	IRDA_FIRSEL						D		
L	VCCQ	LCDD22	IO	0	PORT143	LCDD22	SCIFA3_TXD							U/D		
L	VCCQ	LCDD23	IO	0	PORT144	LCDD23	SCIFA3_RXD							D		
L	VCCQ	LCDHSYN	IO	0	PORT145	LCDHSYN		TS_SDAT2	LCDCS_	I2C_SDA3S			IRQ13	D		
L	VCCQ	LCDVSYN	IO	0	PORT146	LCDVSYN		TS_SDEN2		I2C_SCL4S			IRQ14	D		
L	VCCQ	LCDDCK	IO	0	PORT147	LCDDCK		TS_SCK2	LCDWR_	I2C_SDA4S			IRQ15	D		
L	VCCQ	LCDRD_N	IO	0	PORT148	LCDRD_	MSIOF2_TSYNC							D		
L	VCCQ	LCDDISP	IO	0	PORT149	LCDDISP	MSIOF2_TSCK		LCDRS					D		
L	VCCQ	LCDLCLK	IO	0	PORT150	LCDLCLK	MSIOF2_RXD							D		

Side	Power Gr	Pin name	I/O	Initial Function	Function0	Function1	Function2	Function3	Function4	Function5	Function 6	Function7	IRQ	PullU/D	Tolerant	*2
L	VCCQ	LCDDON	IO	0	PORT151	LCDDON	MSIOF2_TXD							D		
U	VCCQ	SCIFA0_TXD	IO	0	PORT152	SCIFA0_TXD								U/D		
U	VCCQ	SCIFA0_RXD	I	0	PORT153	SCIFA0_RXD								D		
U	VCCQ	SCIFA1_TXD	IO	0	PORT154	SCIFA1_TXD								U/D		
U	VCCQ	SCIFA1_RXD	I	0	PORT155	SCIFA1_RXD								D		
L	VCCQ	TS_SPSYNC	IO	0	PORT156	TS_SPSYNC1	SCIFA0_SCK							D		
L	VCCQ	TS_SDAT	IO	0	PORT157	TS_SDAT1	SCIFA0_RTS_							D		
L	VCCQ	TS_SDEN	I	0	PORT158	TS_SDEN1	SCIFA0_CTS_							D		
L	VCCQ	TS_SCK	IO	0	PORT159	TS_SCK1	SCIFA1_SCK							D		
L	VCCQ	TPUTO0	O	0	PORT160	TPU0TO0	SCIFA1_RTS_							-		
L	VCCQ	TPUTO1	IO	0	PORT161	TPU0TO1	SCIFA1_CTS_							D		
L	VCCQ	SCIFB_SCK	IO	0	PORT162	SCIFB_SCK			OVCN_1				IRQ0	D		
L	VCCQ	SCIFB_RTS_N	IO	0	PORT163	SCIFB_RTS_							IRQ4	D		
L	VCCQ	SCIFB_CTS_N	I	0	PORT164	SCIFB_CTS_							IRQ6	D		
L	VCCQ	SCIFB_TXD	IO	0	PORT165	SCIFB_TXD								D		
L	VCCQ	SCIFB_RXD	I	0	PORT166	SCIFB_RXD								D		
R	VCCQ_MC0	VBUS0_0	I	1	PORT167	VBUS0_0							IRQ7	D	O(5.0V)	
R	VCCQ_MC0	VBUS0_1	I	1	PORT168	VBUS0_1							IRQ8	D	O(5.0V)	
R	VCCQ_MC0	HPD	I	1	PORT169	HDMI_HPD							IRQ9	D	O(5.0V)	
R	VCCQ_MC0	CEC	I	1	*4	HDMI_CEC							IRQ16	D		
R	VCCQ_MC0	SDHICLK0	O	1	PORT171	SDHICLK0								-		
R	VCCQ_MC0	SDHICD0	IO	1	PORT172	SDHICD0							IRQ26	U/D		
R	VCCQ_MC0	SDHID0_0	IO	0	PORT173	SDHID0_0								U/D		
R	VCCQ_MC0	SDHID0_1	IO	0	PORT174	SDHID0_1								U/D		
R	VCCQ_MC0	SDHID0_2	IO	0	PORT175	SDHID0_2								U/D		
R	VCCQ_MC0	SDHID0_3	IO	0	PORT176	SDHID0_3								U/D		
R	VCCQ_MC0	SDHICMD0	IO	0	PORT177	SDHICMD0								U/D		
R	VCCQ_MC0	SDHIWP0	IO	1	PORT178	SDHIWP0								U/D		
R	VCCQ_MC1	SDHICLK1	O	0	PORT179	SDHICLK1								-		
R	VCCQ_MC1	SDHID1_0	IO	0	PORT180	SDHID1_0							IRQ27	U/D		
R	VCCQ_MC1	SDHID1_1	IO	0	PORT181	SDHID1_1							IRQ28	U/D		
R	VCCQ_MC1	SDHID1_2	IO	0	PORT182	SDHID1_2							IRQ29	U/D		
R	VCCQ_MC1	SDHID1_3	IO	0	PORT183	SDHID1_3							IRQ30	U/D		
R	VCCQ_MC1	SDHICMD1	IO	0	PORT184	SDHICMD1							IRQ31	U/D		
R	VCCQ_MC0	SDHICLK2	O	1	PORT185	SDHICLK2								-		
R	VCCQ_MC0	SDHID2_0	IO	1	PORT186	SDHID2_0								U/D		
R	VCCQ_MC0	SDHID2_1	IO	1	PORT187	SDHID2_1								U/D		
R	VCCQ_MC0	SDHID2_2	IO	1	PORT188	SDHID2_2								U/D		
R	VCCQ_MC0	SDHID2_3	IO	1	PORT189	SDHID2_3								U/D		
R	VCCQ_MC0	SDHICMD2	IO	1	PORT190	SDHICMD2								U/D		

[Notes] *1 When the value of the BSCMD pin is 1, general port(PORT*) are unconditionally selected.

*2 At the time of MFI boot, ACMFI-related pins(MEMC_*) are unconditionally selected.

*3 When using the pins for the trace or debug function, set up the debug function select register. They are switched to the trace or debug function regardless of the PORTxxCR setting. For details, see section 60, Debugging Specifications.

*4 Don’t use function 0 of CEC pin.

57.2 Register Description

The following registers are used in the GPIO.

Table57.2 Register Configuration

Side	Register name	Abbreviated name	R/W	Address	Initial value	Access size
D	PORT0 Port control register	PORT0CR	R/W	H'E6051000	H'A0	8,32
D	PORT1 Port control register	PORT1CR	R/W	H'E6051001	H'A0	8,32
D	PORT2 Port control register	PORT2CR	R/W	H'E6051002	H'10	8,32
D	PORT3 Port control register	PORT3CR	R/W	H'E6051003	H'A0	8,32
D	PORT4 Port control register	PORT4CR	R/W	H'E6051004	H'A0	8,32
D	PORT5 Port control register	PORT5CR	R/W	H'E6051005	H'A0	8,32
D	PORT6 Port control register	PORT6CR	R/W	H'E6051006	H'A0	8,32
D	PORT7 Port control register	PORT7CR	R/W	H'E6051007	H'A0	8,32
D	PORT8 Port control register	PORT8CR	R/W	H'E6051008	H'A0	8,32
D	PORT9 Port control register	PORT9CR	R/W	H'E6051009	H'10	8,32
D	PORT10 Port control register	PORT10CR	R/W	H'E605100A	H'10	8,32
D	PORT11 Port control register	PORT11CR	R/W	H'E605100B	H'10	8,32
D	PORT12 Port control register	PORT12CR	R/W	H'E605100C	H'A0	8,32
D	PORT13 Port control register	PORT13CR	R/W	H'E605100D	H'A0	8,32
D	PORT14 Port control register	PORT14CR	R/W	H'E605100E	H'A0	8,32
D	PORT15 Port control register	PORT15CR	R/W	H'E605100F	H'10	8,32
D	PORT16 Port control register	PORT16CR	R/W	H'E6051010	H'A0	8,32
D	PORT17 Port control register	PORT17CR	R/W	H'E6051011	H'A0	8,32
D	PORT18 Port control register	PORT18CR	R/W	H'E6051012	H'A0	8,32
D	PORT19 Port control register	PORT19CR	R/W	H'E6051013	H'12	8,32
D	PORT20 Port control register	PORT20CR	R/W	H'E6051014	H'11	8,32
D	PORT21 Port control register	PORT21CR	R/W	H'E6051015	H'11	8,32
D	PORT22 Port control register	PORT22CR	R/W	H'E6051016	H'11	8,32
D	PORT23 Port control register	PORT23CR	R/W	H'E6051017	H'11	8,32
D	PORT24 Port control register	PORT24CR	R/W	H'E6051018	H'11	8,32
D	PORT25 Port control register	PORT25CR	R/W	H'E6051019	H'11	8,32
D	PORT26 Port control register	PORT26CR	R/W	H'E605101A	H'11	8,32
D	PORT27 Port control register	PORT27CR	R/W	H'E605101B	H'11	8,32
D	PORT28 Port control register	PORT28CR	R/W	H'E605101C	H'11	8,32
D	PORT29 Port control register	PORT29CR	R/W	H'E605101D	H'11	8,32
D	PORT30 Port control register	PORT30CR	R/W	H'E605101E	H'11	8,32
D	PORT31 Port control register	PORT31CR	R/W	H'E605101F	H'11	8,32
D	PORT32 Port control register	PORT32CR	R/W	H'E6051020	H'11	8,32
D	PORT33 Port control register	PORT33CR	R/W	H'E6051021	H'11	8,32
D	PORT34 Port control register	PORT34CR	R/W	H'E6051022	H'11	8,32
D	PORT35 Port control register	PORT35CR	R/W	H'E6051023	H'11	8,32

Side	Register name	Abbreviated name	R/W	Address	Initial value	Access size
D	PORT36 Port control register	PORT36CR	R/W	H'E6051024	H'11	8,32
D	PORT37 Port control register	PORT37CR	R/W	H'E6051025	H'11	8,32
D	PORT38 Port control register	PORT38CR	R/W	H'E6051026	H'11	8,32
D	PORT39 Port control register	PORT39CR	R/W	H'E6051027	H'11	8,32
D	PORT40 Port control register	PORT40CR	R/W	H'E6051028	H'11	8,32
D	PORT41 Port control register	PORT41CR	R/W	H'E6051029	H'11	8,32
D	PORT42 Port control register	PORT42CR	R/W	H'E605102A	H'11	8,32
D	PORT43 Port control register	PORT43CR	R/W	H'E605102B	H'11	8,32
D	PORT44 Port control register	PORT44CR	R/W	H'E605102C	H'11	8,32
D	PORT45 Port control register	PORT45CR	R/W	H'E605102D	H'11	8,32
R	PORT46 Port control register	PORT46CR	R/W	H'E605202E	H'C1	8,32
R	PORT47 Port control register	PORT47CR	R/W	H'E605202F	H'C1	8,32
R	PORT48 Port control register	PORT48CR	R/W	H'E6052030	H'C1	8,32
R	PORT49 Port control register	PORT49CR	R/W	H'E6052031	H'C1	8,32
R	PORT50 Port control register	PORT50CR	R/W	H'E6052032	H'C1	8,32
R	PORT51 Port control register	PORT51CR	R/W	H'E6052033	H'C1	8,32
R	PORT52 Port control register	PORT52CR	R/W	H'E6052034	H'C1	8,32
R	PORT53 Port control register	PORT53CR	R/W	H'E6052035	H'C1	8,32
R	PORT54 Port control register	PORT54CR	R/W	H'E6052036	H'C1	8,32
R	PORT55 Port control register	PORT55CR	R/W	H'E6052037	H'C1	8,32
R	PORT56 Port control register	PORT56CR	R/W	H'E6052038	H'C1	8,32
R	PORT57 Port control register	PORT57CR	R/W	H'E6052039	H'C1	8,32
R	PORT58 Port control register	PORT58CR	R/W	H'E605203A	H'C1	8,32
R	PORT59 Port control register	PORT59CR	R/W	H'E605203B	H'C1	8,32
R	PORT60 Port control register	PORT60CR	R/W	H'E605203C	H'C1	8,32
R	PORT61 Port control register	PORT61CR	R/W	H'E605203D	H'C1	8,32
R	PORT62 Port control register	PORT62CR	R/W	H'E605203E	H'11	8,32
R	PORT63 Port control register	PORT63CR	R/W	H'E605203F	H'11	8,32
R	PORT64 Port control register	PORT64CR	R/W	H'E6052040	H'11	8,32
R	PORT65 Port control register	PORT65CR	R/W	H'E6052041	H'E0	8,32
R	PORT66 Port control register	PORT66CR	R/W	H'E6052042	H'C0	8,32
R	PORT67 Port control register	PORT67CR	R/W	H'E6052043	H'E0	8,32
R	PORT68 Port control register	PORT68CR	R/W	H'E6052044	H'11	8,32
R	PORT69 Port control register	PORT69CR	R/W	H'E6052045	H'11	8,32
R	PORT70 Port control register	PORT70CR	R/W	H'E6052046	H'11	8,32
R	PORT71 Port control register	PORT71CR	R/W	H'E6052047	H'11	8,32
R	PORT72 Port control register	PORT72CR	R/W	H'E6052048	H'11	8,32

Side	Register name	Abbreviated name	R/W	Address	Initial value	Access size
R	PORT73 Port control register	PORT73CR	R/W	H'E6052049	H'E1	8,32
R	PORT74 Port control register	PORT74CR	R/W	H'E605204A	H'E1	8,32
R	PORT75 Port control register	PORT75CR	R/W	H'E605204B	H'E0	8,32
L	PORT76 Port control register	PORT76CR	R/W	H'E605004C	H'80	8,32
L	PORT77 Port control register	PORT77CR	R/W	H'E605004D	H'80	8,32
L	PORT78 Port control register	PORT78CR	R/W	H'E605004E	H'80	8,32
L	PORT79 Port control register	PORT79CR	R/W	H'E605004F	H'80	8,32
L	PORT80 Port control register	PORT80CR	R/W	H'E6050050	H'80	8,32
L	PORT81 Port control register	PORT81CR	R/W	H'E6050051	H'80	8,32
L	PORT82 Port control register	PORT82CR	R/W	H'E6050052	H'80	8,32
L	PORT83 Port control register	PORT83CR	R/W	H'E6050053	H'80	8,32
L	PORT84 Port control register	PORT84CR	R/W	H'E6050054	H'C0	8,32
L	PORT85 Port control register	PORT85CR	R/W	H'E6050055	H'C0	8,32
L	PORT86 Port control register	PORT86CR	R/W	H'E6050056	H'C0	8,32
L	PORT87 Port control register	PORT87CR	R/W	H'E6050057	H'C0	8,32
L	PORT88 Port control register	PORT88CR	R/W	H'E6050058	H'C0	8,32
L	PORT89 Port control register	PORT89CR	R/W	H'E6050059	H'C0	8,32
L	PORT90 Port control register	PORT90CR	R/W	H'E605005A	H'C0	8,32
L	PORT91 Port control register	PORT91CR	R/W	H'E605005B	H'C0	8,32
L	PORT92 Port control register	PORT92CR	R/W	H'E605005C	H'E0	8,32
L	PORT93 Port control register	PORT93CR	R/W	H'E605005D	H'E0	8,32
L	PORT94 Port control register	PORT94CR	R/W	H'E605005E	H'E0	8,32
L	PORT95 Port control register	PORT95CR	R/W	H'E605005F	H'E0	8,32
L	PORT96 Port control register	PORT96CR	R/W	H'E6050060	H'C0	8,32
L	PORT97 Port control register	PORT97CR	R/W	H'E6050061	H'E0	8,32
L	PORT98 Port control register	PORT98CR	R/W	H'E6050062	H'E0	8,32
L	PORT99 Port control register	PORT99CR	R/W	H'E6050063	H'C0	8,32
U	PORT100 Port control register	PORT100CR	R/W	H'E6053064	H'A0	8,32
U	PORT101 Port control register	PORT101CR	R/W	H'E6053065	H'A0	8,32
U	PORT102 Port control register	PORT102CR	R/W	H'E6053066	H'A0	8,32
U	PORT103 Port control register	PORT103CR	R/W	H'E6053067	H'A0	8,32
U	PORT104 Port control register	PORT104CR	R/W	H'E6053068	H'A0	8,32
U	PORT105 Port control register	PORT105CR	R/W	H'E6053069	H'A0	8,32
U	PORT106 Port control register	PORT106CR	R/W	H'E605306A	H'E0	8,32
U	PORT107 Port control register	PORT107CR	R/W	H'E605306B	H'E0	8,32
U	PORT108 Port control register	PORT108CR	R/W	H'E605306C	H'E0	8,32
U	PORT109 Port control register	PORT109CR	R/W	H'E605306D	H'E0	8,32

Side	Register name	Abbreviated name	R/W	Address	Initial value	Access size
U	PORT110 Port control register	PORT110CR	R/W	H'E605306E	H'E0	8,32
U	PORT111 Port control register	PORT111CR	R/W	H'E605306F	H'E0	8,32
U	PORT112 Port control register	PORT112CR	R/W	H'E6053070	H'A0	8,32
U	PORT113 Port control register	PORT113CR	R/W	H'E6053071	H'A0	8,32
U	PORT114 Port control register	PORT114CR	R/W	H'E6053072	H'E0	8,32
U	PORT115 Port control register	PORT115CR	R/W	H'E6053073	H'E0	8,32
U	PORT116 Port control register	PORT116CR	R/W	H'E6053074	H'E0	8,32
U	PORT117 Port control register	PORT117CR	R/W	H'E6053075	H'E0	8,32
U	PORT118 Port control register	PORT118CR	R/W	H'E6053076	H'E0	8,32
U	PORT119 Port control register	PORT119CR	R/W	H'E6053077	H'E0	8,32
U	PORT120 Port control register	PORT120CR	R/W	H'E6053078	H'E0	8,32
L	PORT121 Port control register	PORT121CR	R/W	H'E6050079	H'A0	8,32
L	PORT122 Port control register	PORT122CR	R/W	H'E605007A	H'A0	8,32
L	PORT123 Port control register	PORT123CR	R/W	H'E605007B	H'A0	8,32
L	PORT124 Port control register	PORT124CR	R/W	H'E605007C	H'A0	8,32
L	PORT125 Port control register	PORT125CR	R/W	H'E605007D	H'A0	8,32
L	PORT126 Port control register	PORT126CR	R/W	H'E605007E	H'A0	8,32
L	PORT127 Port control register	PORT127CR	R/W	H'E605007F	H'A0	8,32
L	PORT128 Port control register	PORT128CR	R/W	H'E6050080	H'A0	8,32
L	PORT129 Port control register	PORT129CR	R/W	H'E6050081	H'A0	8,32
L	PORT130 Port control register	PORT130CR	R/W	H'E6050082	H'A0	8,32
L	PORT131 Port control register	PORT131CR	R/W	H'E6050083	H'A0	8,32
L	PORT132 Port control register	PORT132CR	R/W	H'E6050084	H'A0	8,32
L	PORT133 Port control register	PORT133CR	R/W	H'E6050085	H'A0	8,32
L	PORT134 Port control register	PORT134CR	R/W	H'E6050086	H'A0	8,32
L	PORT135 Port control register	PORT135CR	R/W	H'E6050087	H'A0	8,32
L	PORT136 Port control register	PORT136CR	R/W	H'E6050088	H'A0	8,32
L	PORT137 Port control register	PORT137CR	R/W	H'E6050089	H'A0	8,32
L	PORT138 Port control register	PORT138CR	R/W	H'E605008A	H'A0	8,32
L	PORT139 Port control register	PORT139CR	R/W	H'E605008B	H'A0	8,32
L	PORT140 Port control register	PORT140CR	R/W	H'E605008C	H'A0	8,32
L	PORT141 Port control register	PORT141CR	R/W	H'E605008D	H'A0	8,32
L	PORT142 Port control register	PORT142CR	R/W	H'E605008E	H'A0	8,32
L	PORT143 Port control register	PORT143CR	R/W	H'E605008F	H'A0	8,32
L	PORT144 Port control register	PORT144CR	R/W	H'E6050090	H'A0	8,32
L	PORT145 Port control register	PORT145CR	R/W	H'E6050091	H'A0	8,32
L	PORT146 Port control register	PORT146CR	R/W	H'E6050092	H'A0	8,32

Side	Register name	Abbreviated name	R/W	Address	Initial value	Access size
L	PORT147 Port control register	PORT147CR	R/W	H'E6050093	H'A0	8,32
L	PORT148 Port control register	PORT148CR	R/W	H'E6050094	H'A0	8,32
L	PORT149 Port control register	PORT149CR	R/W	H'E6050095	H'A0	8,32
L	PORT150 Port control register	PORT150CR	R/W	H'E6050096	H'A0	8,32
L	PORT151 Port control register	PORT151CR	R/W	H'E6050097	H'A0	8,32
U	PORT152 Port control register	PORT152CR	R/W	H'E6053098	H'A0	8,32
U	PORT153 Port control register	PORT153CR	R/W	H'E6053099	H'A0	8,32
U	PORT154 Port control register	PORT154CR	R/W	H'E605309A	H'A0	8,32
U	PORT155 Port control register	PORT155CR	R/W	H'E605309B	H'A0	8,32
L	PORT156 Port control register	PORT156CR	R/W	H'E605009C	H'A0	8,32
L	PORT157 Port control register	PORT157CR	R/W	H'E605009D	H'A0	8,32
L	PORT158 Port control register	PORT158CR	R/W	H'E605009E	H'A0	8,32
L	PORT159 Port control register	PORT159CR	R/W	H'E605009F	H'A0	8,32
L	PORT160 Port control register	PORT160CR	R/W	H'E60500A0	H'10	8,32
L	PORT161 Port control register	PORT161CR	R/W	H'E60500A1	H'A0	8,32
L	PORT162 Port control register	PORT162CR	R/W	H'E60500A2	H'A0	8,32
L	PORT163 Port control register	PORT163CR	R/W	H'E60500A3	H'A0	8,32
L	PORT164 Port control register	PORT164CR	R/W	H'E60500A4	H'A0	8,32
L	PORT165 Port control register	PORT165CR	R/W	H'E60500A5	H'A0	8,32
L	PORT166 Port control register	PORT166CR	R/W	H'E60500A6	H'A0	8,32
R	PORT167 Port control register	PORT167CR	R/W	H'E60520A7	H'A1	8,32
R	PORT168 Port control register	PORT168CR	R/W	H'E60520A8	H'A1	8,32
R	PORT169 Port control register	PORT169CR	R/W	H'E60520A9	H'A1	8,32
R	PORT170 Port control register	PORT170CR	R/W	H'E60520AA	H'A1	8,32
R	PORT171 Port control register	PORT171CR	R/W	H'E60520AB	H'11	8,32
R	PORT172 Port control register	PORT172CR	R/W	H'E60520AC	H'E1	8,32
R	PORT173 Port control register	PORT173CR	R/W	H'E60520AD	H'A0	8,32
R	PORT174 Port control register	PORT174CR	R/W	H'E60520AE	H'A0	8,32
R	PORT175 Port control register	PORT175CR	R/W	H'E60520AF	H'A0	8,32
R	PORT176 Port control register	PORT176CR	R/W	H'E60520B0	H'A0	8,32
R	PORT177 Port control register	PORT177CR	R/W	H'E60520B1	H'A0	8,32
R	PORT178 Port control register	PORT178CR	R/W	H'E60520B2	H'E1	8,32
R	PORT179 Port control register	PORT179CR	R/W	H'E60520B3	H'11	8,32
R	PORT180 Port control register	PORT180CR	R/W	H'E60520B4	H'A0	8,32
R	PORT181 Port control register	PORT181CR	R/W	H'E60520B5	H'A0	8,32
R	PORT182 Port control register	PORT182CR	R/W	H'E60520B6	H'A0	8,32
R	PORT183 Port control register	PORT183CR	R/W	H'E60520B7	H'A0	8,32

Side	Register name	Abbreviated name	R/W	Address	Initial value	Access size
R	PORT184 Port control register	PORT184CR	R/W	H'E60520B8	H'A0	8,32
R	PORT185 Port control register	PORT185CR	R/W	H'E60520B9	H'11	8,32
R	PORT186 Port control register	PORT186CR	R/W	H'E60520BA	H'A0	8,32
R	PORT187 Port control register	PORT187CR	R/W	H'E60520BB	H'A0	8,32
R	PORT188 Port control register	PORT188CR	R/W	H'E60520BC	H'A0	8,32
R	PORT189 Port control register	PORT189CR	R/W	H'E60520BD	H'A0	8,32
R	PORT190 Port control register	PORT190CR	R/W	H'E60520BE	H'A0	8,32
L	PORTL095_064 Data register	PORTL095_064DR	R/W	H'E6054008	H'00000000*3	32
L	PORTL127_096 Data register	PORTL127_096DR	R/W	H'E605400C	H'00000000*3	32
L	PORTL159_128 Data register	PORTL159_128DR	R/W	H'E6054010	H'00000000*3	32
L	PORTL191_160 Data register	PORTL191_160DR	R/W	H'E6054014	H'00000000*3	32
D	PORTD031_000 Data register	PORTD031_000DR	R/W	H'E6055000	H'00000000*3	32
D	PORTD063_032 Data register	PORTD063_032DR	R/W	H'E6055004	H'00000000*3	32
R	PORTR063_032 Data register	PORTR063_032DR	R/W	H'E6056004	H'00000000*3	32
R	PORTR095_064 Data register	PORTR095_064DR	R/W	H'E6056008	H'00000000*3	32
R	PORTR191_160 Data register	PORTR191_160DR	R/W	H'E6056014	H'00000000*3	32
U	PORTU127_096 Data register	PORTU127_096DR	R/W	H'E605700C	H'00000000*3	32
U	PORTU159_128 Data register	PORTU159_128DR	R/W	H'E6057010	H'00000000*3	32
L	PORTL095_064 Data set register	PORTL095_064DSR	R/W	H'E6054108/ H'E6074108*2	H'00000000*3	32
L	PORTL127_096 Data set register	PORTL127_096DSR	R/W	H'E605410C/ H'E607410C*2	H'00000000*3	32
L	PORTL159_128 Data set register	PORTL159_128DSR	R/W	H'E6054110/ H'E6074110*2	H'00000000*3	32
L	PORTL191_160 Data set register	PORTL191_160DSR	R/W	H'E6054114/ H'E6074114*2	H'00000000*3	32
D	PORTD031_000 Data set register	PORTD031_000DSR	R/W	H'E6055100/ H'E6075100*2	H'00000000*3	32
D	PORTD063_032 Data set register	PORTD063_032DSR	R/W	H'E6055104/ H'E6075104*2	H'00000000*3	32
R	PORTR063_032 Data set register	PORTR063_032DSR	R/W	H'E6056104/ H'E6076104*2	H'00000000*3	32
R	PORTR095_064 Data set register	PORTR095_064DSR	R/W	H'E6056108/ H'E6076108*2	H'00000000*3	32
R	PORTR191_160 Data set register	PORTR191_160DSR	R/W	H'E6056114/ H'E6076114*2	H'00000000*3	32
U	PORTU127_096 Data set register	PORTU127_096DSR	R/W	H'E605710C/ H'E607710C*2	H'00000000*3	32

Side	Register name	Abbreviated name	R/W	Address	Initial value	Access size
U	PORTU159_128 Data set register	PORTU159_128DSR	R/W	H'E6057110/ H'E6077110*2	H'00000000*3	32
L	PORTL095_064 Data clear register	PORTL095_064DCR	R/W	H'E6054208/ H'E6074208*2	H'00000000*3	32
L	PORTL127_096 Data clear register	PORTL127_096DCR	R/W	H'E605420C/ H'E607420C*2	H'00000000*3	32
L	PORTL159_128 Data clear register	PORTL159_128DCR	R/W	H'E6054210/ H'E6074210*2	H'00000000*3	32
L	PORTL191_160 Data clear register	PORTL191_160DCR	R/W	H'E6054214/ H'E6074214*2	H'00000000*3	32
D	PORTD031_000 Data clear register	PORTD031_000DCR	R/W	H'E6055200/ H'E6075200*2	H'00000000*3	32
D	PORTD063_032 Data clear register	PORTD063_032DCR	R/W	H'E6055204/ H'E6075204*2	H'00000000*3	32
R	PORTR063_032 Data clear register	PORTR063_032DCR	R/W	H'E6056204/ H'E6076204*2	H'00000000*3	32
R	PORTR095_064 Data clear register	PORTR095_064DCR	R/W	H'E6056208/ H'E6076208*2	H'00000000*3	32
R	PORTR191_160 Data clear register	PORTR191_160DCR	R/W	H'E6056214/ H'E6076214*2	H'00000000*3	32
U	PORTU127_096 Data clear register	PORTU127_096DCR	R/W	H'E605720C/ H'E607720C*2	H'00000000*3	32
U	PORTU159_128 Data clear register	PORTU159_128DCR	R/W	H'E6057210/ H'E6077210*2	H'00000000*3	32
	AP block LSI internal communication interrupt/power reset function register*1	CCOMIFAP	R/W	H'E6058000 H'E6078000*2	H'00000000	32
	AP block LSI internal communication interrupt/power reset source register*1	CCOMIEAP	R	H'E6058004 H'E6078004*2	H'00000000	32
	AP block LSI internal communication interrupt/power reset source clear register*1	CCOMICAP	W	H'E6058008 H'E6078008*2	H'00000000	32
	RT ->SYS LSI Internal communication interrupt/power reset function register*1	CCOMIFR2S	R/W	H'E6058060 H'E6078060*2	H'00000000	32
	RT ->SYS LSI Internal communication interrupt/power reset source register*1	CCOMIER2S	R	H'E6058064 H'E6078064*2	H'00000000	32
	RT ->SYS LSI Internal communication interrupt/power reset source clear register*1	CCOMICR2S	W	H'E6058068 H'E6078068*2	H'00000000	32
	SYS ->RT LSI Internal communication interrupt/power reset function register*1	CCOMIFS2R	R/W	H'E6058070 H'E6078070*2	H'00000000	32

Side	Register name	Abbreviated name	R/W	Address	Initial value	Access size
	SYS ->RT LSI Internal communication interrupt/power reset source register*1	CCOMIES2R	R	H'E6058074 H'E6078074*2	H'00000000	32
	SYS ->RT LSI Internal communication interrupt/power reset source clear register*1	CCOMICS2R	W	H'E6058078 H'E6078078*2	H'00000000	32
	Module function select register1	MSEL1CR	R/W	H'E605800C	H'00000000	32
	Module function select register3	MSEL3CR	R/W	H'E6058020	H'00000000	32
	Module function select register4	MSEL4CR	R/W	H'E6058024	H'00000000	32
	USB Control register2	USBCR2	R/W	H'E605810C	H'0A0A orH'0A8A	16
	USB Control register4	USBCR4	R/W	H'E6058130	H'0A0A orH'0A8A	16
	USC Control register1	USCCR1	R/W	H'E6058144	H'0000	16
	USC Control register2	USCCR2	R/W	H'E6058146	H'0000	16
	CKO Control register	CKOCR	R/W	H'E6058110	H'0003	16
	WE0 Control register	WE0CR	R/W	H'E6058112	H'0003	16
	WE1 Control register	WE1CR	R/W	H'E6058114	H'0003	16
	MMCCLK0 Control register	MMCCLK0CR	R/W	H'E6058118	H'0003	16
	MMCCLK1 Control register	MMCCLK1CR	R/W	H'E605811A	H'0003	16
	SDHICLK0 Control register	SDHICLK0CR	R/W	H'E6058122	H'0003	16
	SDHICLK1 Control register	SDHICLK1CR	R/W	H'E6058124	H'0003	16
	SDHICLK2 Control register	SDHICLK2CR	R/W	H'E6058120	H'0003	16
	VCCQ Domain set register	VCCQ18CR	R/W	H'E6058180	H'0003	16
	VCCQ Domain(BSC Pins) Set register	VCCQBSCCR	R/W	H'E6058182	H'0003	16
	VCCQ Domain(VIO Pins) Set register	VCCQVIOCR	R/W	H'E6058184	H'0003	16
	VCCQ Domain(LCD Pins) Set register	VCCQLCDCR	R/W	H'E6058186	H'0003	16
	VCCQ Domain(MFI Pins) Set register	VCCQMFICR	R/W	H'E6058188	H'0003	16
	VCCQ3 Domain set register	VCCQ3CR	R/W	H'E605818A	H'0003	16
	VCCQ_MC0 Domain set register	VCCQMC0CR	R/W	H'E605818C	H'0003	16
	VCCQ_MC1 Domain set register	VCCQMC1CR	R/W	H'E605818E	H'0003	16
	IIC Control register	IICCR	R/W	H'E60581A0	H'8003	16
	CPORT GPI Register	CGPI	R	H'E60581C4	-	16
	CPORT GPOSR/GPOR Register	CGPOSR/CGPOR	R/W	H'E60581C6 H'E60781C6*2	H'0000	16
	CPORT GPOR2SSR/GPOR2SR Register	CGPOR2SSR/CGPOR2SR	R/W	H'E60581CC H'E60781CC*2	H'0000	16
	CPORT GPOS2RSR/GPOS2RR Register	CGPOS2RSR/CGPOS2RR	R/W	H'E60581CE H'E60781CE*2	H'0000	16

Side	Register name	Abbreviated name	R/W	Address	Initial value	Access size
	USB PHY0 Interruption control registerAP	USBPHY0INTAP	R/W	H'E60781E0*2	H'0000	16
	USB PHY1 Interruption control registerAP	USBPHY1INTAP	R/W	H'E60781E2*2	H'0000	16

[Notes] *1 For details, see section 5.6, LSI Internal Communication Interrupt/Power Reset (Request to the AP Block) and section 5.7, LSI Internal Communication Interrupt/Power Reset (Request to SYS from RT), section 5.8, LSI Internal Communication Interrupt/Power Reset (Request to RT from SYS).

*2 Accessing Address H'E605XXXX, It is controlled by the GPIO semaphore of HPB.

Accessing Address H'E607XXXX, It is not controlled by the GPIO semaphore of HPB.

*3 When the IE bit of PORTnCR is set to 1, the level of the corresponding pin is read.

Table57.3 The state of the register in each processing mode

Abbreviated name	Reset*	C6 At the time of the interception of those other than a power supply domain
PORTxxxCR	Initialized	Retained
PORTxxxDR	Initialized	Retained
CCOMIFAP	Initialized	Retained
CCOMIEAP	Initialized	Retained
CCOMICAP	Initialized	Retained
CCOMIFR2S	Initialized	Retained
CCOMIER2S	Initialized	Retained
CCOMICR2S	Initialized	Retained
CCOMIFS2R	Initialized	Retained
CCOMIES2R	Initialized	Retained
CCOMICS2R	Initialized	Retained
MSEL1CR	Initialized	Retained
MSEL3CR	Initialized	Retained
MSEL4CR	Initialized	Retained
USBCR2	Initialized	Retained
USBCR4	Initialized	Retained
USCCR1	Initialized	Retained
USCCR2	Initialized	Retained
CKOCR	Initialized	Retained
WE0CR	Initialized	Retained
WE1CR	Initialized	Retained
MMCCLK0CR	Initialized	Retained
MMCCLK1CR	Initialized	Retained
SDHICLK0CR	Initialized	Retained
SDHICLK1CR	Initialized	Retained
SDHICLK2CR	Initialized	Retained
VCCQ18CR	Initialized	Retained
VCCQBSCCR	Initialized	Retained
VCCQVIOCR	Initialized	Retained
VCCQLCDCR	Initialized	Retained
VCCQMFICR	Initialized	Retained
VCCQ3CR	Initialized	Retained
VCCQMC0CR	Initialized	Retained
VCCQMC1CR	Initialized	Retained
IICCR	Initialized	Retained
CGPI	Initialized	Retained

Abbreviated name	Reset*	C6 At the time of the interception of those other than a power supply domain
CGPOSR/CGPOR	Initialized	Retained
CGPOR2SSR/CGPOR2SR	Initialized	Retained
CGPOS2RSR/CGPOS2RR	Initialized	Retained
USBPHY0INTAP	Initialized	Retained
USBPHY1INTAP	Initialized	Retained

[Notes] * For details of the Reset range, see section 1-D.

57.2.1 PORTn Control registerPORTnCR)

ビット：	7	6	5	4	3	2	1	0
	PULMD[1:0]		IE	OE	—	PTMD[2:0]		
初期値：								
R/W：	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit name	Initial value	R/W	Description
7, 6	PULMD[1:0]	Please refer Table59.1	R/W	Specify pull-up or pull-down of the port. 0x: Pull-up/pull-down OFF 10: Pull-down 11: Pull-up When a pull-up function is chosen in the case of a pin without a pull-up Operation and a write-in value cannot be guaranteed. When a pull-down function is chosen in the case of a pin without a pull-down Operation and a write-in value cannot be guaranteed.
5	IE	Please refer Table59.1	R/W	Enables or disables the input of the port. 0 : Input is disabled. 1 : Input is enabled. In the case of the pin only for an output, please always write in an initial value at the time of this register writing.
4	OE	Please refer Table59.1	R/W	Enables or disables the output of the port. 0 : Output is disabled. 1 : Output is enabled. In the case of the pin only for an input, please always write in an initial value at the time of this register writing.
3	-	0	R	Reserve bit This bit is always read as 0. The write value should always be 0.

Bit	Bit name	Initial value	R/W	Description
2 to 0	PTMD[2:0]	Please refer Table58.1	R/W	Pin Function Select. 000 : Select Function0. 001 : Select Function1. 010 : Select Function2. 011 : Select Function3. 100 : Select Function4. 101 : Select Function5. 110 : Select Function6. 111 : Select Function7. At the time of setting up the function in which a definition is not given, an operation and a write-in value are not guaranteed.

[Notes] To drive external pins specified as output Hi-Z, select function 0 (port function) and set the OE bit to 0.

PULMD is always effective, but IE and OE are effective only at the time of a selection of function 0.

57.2.2 Module function select register1 (MSEL1CR)

MSEL1CR is a 32-bit readable/writable register that selects module functions from multiplexed pin functions.

ビット:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MSEL 31	MSEL 30	MSEL 29	MSEL 28	MSEL 27	MSEL 26	–	–	–	–	–	–	–	–	–	MSEL 16
初期値:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R/W

ビット:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSEL 15	MSEL 14	MSEL 13	MSEL 12	–	–	MSEL 9	MSEL 8	MSEL 7	MSEL 6	–	MSEL 4	MSEL 3	MSEL 2	–	MSEL 0
初期値:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W

Bit	Bit name	Initial value	R/W	Description
31	MSEL31	0	R/W	IRQ31 Pin Setting 0 : The input of SDHICMD1 Pin(PORT184) is effective. 1 : The input of LCDD17 Pin(PORT138) is effective.
30	MSEL30	0	R/W	IRQ30 Pin Setting 0 : The input of SDHID1_3 Pin(PORT183) is effective. 1 : The input of LCDD9 Pin(PORT130) is effective.
29	MSEL29	0	R/W	IRQ29 Pin Setting 0 : The input of SDHID1_2 Pin(PORT182) is effective. 1 : The input of LCDD8 Pin(PORT129) is effective.
29	MSEL28	0	R/W	IRQ28 Pin Setting 0 : The input of SDHID1_1 Pin(PORT181) is effective. 1 : The input of LCDD2 Pin(PORT123) is effective.

Bit	Bit name	Initial value	R/W	Description
27	MSEL27	0	R/W	IRQ27 Pin Setting 0 : The input of SDHID1_0 Pin(PORT180) is effective. 1 : The input of LCDD1 Pin(PORT122) is effective.
26	MSEL26	0	R/W	IRQ26 Pin Setting 0 : The input of SDHICD0 Pin(PORT172) is effective. 1 : The input of LCDD0 Pin(PORT121) is effective.
25 to 17	-	All0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	MSEL16	0	R/W	IRQ16 Pin Setting 0 : The input of MEMC_AD8 Pin(PORT84) is effective. 1 : The input of CEC Pin(PORT170) is effective.
15	MSEL15	0	R/W	IRQ15 Pin Setting 0 : The input of MEMC_AD7 Pin(PORT83) is effective. 1 : The input of LCDDCK Pin(PORT147) is effective.
14	MSEL14	0	R/W	IRQ14 Pin Setting 0 : The input of MEMC_AD6 Pin(PORT82) is effective. 1 : The input of LCDVSYN Pin(PORT146) is effective.
13	MSEL13	0	R/W	IRQ13 Pin Setting 0 : The input of MEMC_AD5 Pin(PORT81) is effective. 1 : The input of LCDHSYN Pin(PORT145) is effective.
12	MSEL12	0	R/W	IRQ12 Pin Setting 0 : The input of MEMC_AD4 Pin(PORT80) is effective. 1 : The input of LCDD16 Pin(PORT137) is effective.
11, 10	-	All0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	MSEL9	0	R/W	IRQ9 Pin Setting 0 : The input of A23 Pin(PORT42) is effective. 1 : The input of HPD Pin(PORT169) is effective.
8	MSEL8	0	R/W	IRQ8 Pin Setting 0 : The input of VBUS0_1 Pin(PORT168) is effective. 1 : The input of A22 Pin(PORT41) is effective.
7	MSEL7	0	R/W	IRQ7 Pin Setting 0 : The input of VBUS0_0 Pin(PORT167) is effective. 1 : The input of A21 Pin(PORT40) is effective.
6	MSEL6	0	R/W	IRQ6 Pin Setting 0 : The input of A20 Pin(PORT39) is effective. 1 : The input of SCIFB_CTS_N Pin(PORT164) is effective.

Bit	Bit name	Initial value	R/W	Description
5	-	0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	MSEL4	0	R/W	IRQ4 Pin Setting 0 : The input of FMSOIBT Pin(PORT17) is effective. 1 : The input of SCIFB_RTS_N Pin(PORT163) is effective.
3	MSEL3	0	R/W	IRQ3 Pin Setting 0 : The input of FSIAOMC Pin(PORT8) is effective. 1 : The input of FMSOILR Pin(PORT16) is effective.
2	MSEL2	0	R/W	IRQ2 Pin Setting 0 : The input of FSIACK Pin(PORT4) is effective. 1 : The input of FSIAILR Pin(PORT5) is effective.
1	-	0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	MSEL0	0	R/W	IRQ0 Pin Setting 0 : The input of FSIAIBT Pin(PORT6) is effective. 1 : The input of SCIFB_SCK Pin(PORT162) is effective.

57.2.3 Module function selection register3 (MSEL3CR)

MSEL3CR is a 32-bit readable/writable register that selects module functions from multiplexed pin functions.

ビット:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	MSEL[27:26]		–	–	–	–	MSEL[21:20]		–	–	–	–
初期値:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R	R	R	R	R/W	R/W	R	R	R	R

ビット:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSEL 15	–	–	–	–	–	MSEL 9	–	–	MSEL 6	–	–	–	–	–	–
初期値:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R/W	R	R	R/W	R	R	R	R	R	R

Bit	Bit name	Initial value	R/W	Description
31 to 28	-	All0	R	Reserved These bits are always read as 0. The write value should always be 0.
27, 26	MSEL[27:26]	00	R/W	TSIF1 Pin Setting 00 :TSIF_xxx1 Select 01 :TSIF_xxx2 Select 10 : Reserved 11 : Reserved
25 to 22	-	All0	R	Reserved These bits are always read as 0. The write value should always be 0.
21, 20	MSEL[21:20]	00	R/W	TSIF0 Pin Setting 00 :TSIF_xxx1 Select 01 :TSIF_xxx2 Select 10 : Reserved 11 : Reserved
19 to 16	-	All0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	MSEL15	0	R/W	Debug monitor function Setting 0 : Uses the VIO pin for the debug monitor function. 1 : Uses the LCDD pin for the debug monitor function. (The detailed pin assignment is shown table 60.13.)
14 to 10	-	All0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	MSEL9	0	R/W	SCIFA3_CTS_ Pin Setting 0 :Select A24 Pin.(Function4 of PORT43) 1 :Select LCDD19 Pin.(Function2 of PORT140)
8, 7	-	All0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit name	Initial value	R/W	Description
6	MSEL6	0	R/W	LCDC Pin Setting 0 :Pins of LCDC0 module are effective. 1 :Pins of LCDC1 module are effective.
5 to 0	-	All0	R	Reserved These bits are always read as 0. The write value should always be 0.

57.2.4 Module function selection register4 (MSEL4CR)

MSEL4CR is a 32-bit readable/writable register that selects module functions from multiplexed pin functions.

ビット:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	MSEL19	MSEL18	MSEL17	MSEL16
初期値:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

ビット:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSEL15	MSEL14	–	–	–	MSEL10	–	–	–	MSEL6	–	MSEL4	–	–	MSEL1	–
初期値:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R	R	R/W	R	R	R	R/W	R	R/W	R	R	R/W	R

Bit	Bit name	Initial value	R/W	Description
31 to 20	-	All0	R	Reserved These bits are always read as 0. The write value should always be 0.
19	MSEL19	0	R/W	SDENC clock supply Setting 0 : The clock from CPG is effective. 1 : The clock from DV_CLKI Pin is effective.
18	MSEL18	0	R/W	KEYIN0 to KEYIN3 Pin Setting 0 : Select LCDD15 to LCDD12 Pin. (Function3 of PORT136 to 133) 1 : Select LCDD0 to LCDD3 Pin. (Function4 of PORT121 to 124)
17	MSEL17	0	R/W	IIC4 Pin Setting 0 : Select LCD Pin. (Function5 of PORT146 and 147) 1 : Select VIO Pin. (Function2 of PORT116 and 117)
16	MSEL16	0	R/W	IIC3 Pin Setting 0 : Select LCD Pin.(Function5 of PORT137 and 145) 1 : Select VIO Pin.(Function2 of PORT114 and 115)
15	MSEL15	0	R/W	MMC Pin Setting 0 :Select MFI Pin.(Function4 of PORT84-92 and 99) 1 :Select BSC Pin. (Function3 of PORT54-61, 66 and 67)
14	MSEL14	0	R/W	OVCN_1, IDIN_1 Pin Setting 0 :Select VIO Pin.(Function4 of PORT114 and 113) 1 :Select SCIFB and FMS Pin.(Function4 of PORT162 and Function3 of PORT18)

Bit	Bit name	Initial value	R/W	Description
13 to 11	-	All0	R	Reserved These bits are always read as 0. The write value should always be 0.
10	MSEL10	0	R/W	MSIOF1 Pin Setting 0 :Select BSC Pin.(Function3 of PORT39-44) 1 :Select MFI Pin.(Function2 of PORT88-93)
9 to 7	-	All0	R	Reserved These bits are always read as 0. The write value should always be 0.
6	MSEL6	0	R/W	MFI Pin function settings(Function1 of PORT93-96) 0 :Select ACMFI2. (MEMC_BUSCLK, MEMC_CS1, MEMC_ADV, MEMC_WAIT) 1 :Select ACMFI1. (MEMC_A0, MEMC_A1, MEMC_DREQ0, MEMC_DREQ1)
5	-	0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	MSEL4	0	R/W	RESETA Pin pullup Setting. 0 :pullup enable 1 :pullup disable
3, 2	-	All0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	MSEL1	0	R/W	EDEBGREQ Pin pull-up/down Setting. 0 : Pull-down 1 : Pull-up
0	-	0	R	Reserved These bits are always read as 0. The write value should always be 0.

57.2.5 USB Control register2 (USBCR2)

ビット：	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	USB_START	—	—	USB_COR[4:0]					USB_OFF	—	—	USB_CNT[4:0]				
初期値：	0	0	0	0	1	0	1	0	—	0	0	0	1	0	1	0
R/W：	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit	Bit name	Initial value	R/W	Description
15	USB_START	0	R/W	Start Bit 1: Writing 1 to this bit starts a countdown of the RCLK period. Set this bit to enable the USB-PHY0 after VBUS0_0 is detected. This bit is always read as 0. After setting the USB_COR bit, write 1 to this bit. [Note] Even if USB-PHY0 is put into Power ON state(USB_OFF=0), after it becomes Power OFF state(USB_OFF=1) it is reactivated when it starts up by writing in this bit 1. This transition of USB_OFF bit is reflected in USB_PHY_ON and USB_PHY_OFF bits of USB PHY0 Interruption control registerAP. Please issue software reset of USB module, after USB-PHY valid.
14, 13	-	All0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 8	USB_COR [4:0]	01010	R/W	Countdown Setting Specifies the countdown value till start. Note: The countdown starts with "this bit +1" : Valid value range: 0 to h'1E
7	USB_OFF	-	R	USB-PHY0 Power Shutoff Status This bit is read-only. 0: USB-PHY0 isolation cell* disabled, power ON This bit is cleared 0 when the counter value is all 0. The USB-PHY0 power is ON and USB communications are available. 1: USB-PHY0 isolation cell* enabled, power OFF This bit is set to 1 at reset or when VBUS0_0 is detected as low level. The USB-PHY0 power is OFF and USB communications are not available. This causes the VBUS signal supplied to USBHS to be low and the VBUS signal is disconnected even if the VBUS0_0 pin is high level.
6, 5	-	All0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit name	Initial value	R/W	Description
4 to 0	USB_CNT [4:0]	01010	R	Count Value When the count value is all 0, it means the USB-PHY0 isolation cell* is disabled and the power is ON. When VBUS0_0 is detected as low level, the USB_COR value is set.

[Notes]* The isolation cell prevents unknown value propagation by mask signal.

57.2.6 USB Control register4 (USBCR4)

ビット：	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	USB_START	—	—	USB_COR[4:0]					USB_OFF	—	—	USB_CNT[4:0]				
初期値：	0	0	0	0	1	0	1	0	—	0	0	0	1	0	1	0
R/W：	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit	Bit name	Initial value	R/W	Description
15	USB_START	0	R/W	Start Bit 1: Writing 1 to this bit starts a countdown of the RCLK period. Set this bit to enable the USB-PHY1 after VBUS0_1 is detected. This bit is always read as 0. After setting the USB_COR bit, write 1 to this bit. [Note] Even if USB-PHY1 is put into Power ON state(USB_OFF=0), after it becomes Power OFF state(USB_OFF=1) it is reactivated when it starts up by writing in this bit 1. This transition of USB_OFF bit is reflected in USB_PHY_ON and USB_PHY_OFF bits of USB PHY1 Interruption control registerAP.
14, 13	-	All0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 8	USB_COR [4:0]	01010	R/W	Countdown Setting Specifies the countdown value till start. Note: The countdown starts with "this bit +1" : Valid value range: 0 to h'1E
7	USB_OFF	-	R	USB-PHY1 Power Shutoff Status This bit is read-only. 0: USB-PHY1 isolation cell* disabled, power ON This bit is cleared 0 when the counter value is all 0. The USB-PHY1 power is ON and USB communications are available. 1: USB-PHY1 isolation cell* enabled, power OFF This bit is set to 1 at reset or when VBUS0_1 is detected as low level. The USB-PHY1 power is OFF and USB communications are not available. This causes the VBUS signal supplied to USBHS to be low and the VBUS signal is disconnected even if the VBUS0_1 pin is high level.
6, 5	-	All0	R	Reserved These bits are always read as 0. The write value should always be 0.
4 to 0	USB_CNT [4:0]	01010	R	Count Value When the count value is all 0, it means the USB-PHY1 isolation cell* is disabled and the power is ON. When VBUS0_1 is detected as low, the USB_COR value is set.

[Notes]* The isolation cell prevents unknown value propagation by mask signal.

57.2.7 USC Control register1 (USCCR1)

ビット:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VIF_MODE[1:0]		VOINT_CLR	VOINT_MASK	VOCLK_SEL[1:0]		VO RESET	VO SYNCE	VO MASTE	SPDIF SEL	–	–	–	USC_SEL[2:0]		
初期値:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W

Bit	Bit name	Initial value	R/W	Description
15, 14	VIF_MODE [1:0]	00	R/W	SPU2 outside interrupt/net synchronous signal input bit This register permit interrupt signal from the outside pin to SPU2 and the input of a net synchronous signal. 00: The interrupt signal to SPU2 is not permitted. A net synchronous signal is not input. 01: The interrupt signal to SPU2 is not permitted. The input from the VINT_I pin is input as a net synchronous signal. 10: The input from the VINT_I pin is considered as SPU2 outside interrupt. A net synchronous signal is not input. 11: The input from the IRQ pin is considered as SPU2 outside interrupt. The USCCR2 register is used for the select of IRQ pin. The input from the VINT_I pin is input as a net synchronous signal.
13	VOINT_CLR	0	R/W	VOSYNC interrupt clear bit 0: Interrupt from the VOSYNC module can be set. 1: Interrupt from the VOSYNC module is cleared. Please set 0 in this bit after it clears.
12	VOINT_MASK	0	R/W	VOSYNC interrupt mask bit 0: Interrupt from the VOSYNC module is masked. 1: Interrupt from the VOSYNC module is permitted.
11, 10	VOCLK_SEL [1:0]	00	R/W	The source clock of VOSYNC module selection bit The source clock that generates 8KHz is selected. 00: EXTAL1(26MHz) is a source clock of 8KHz. 01: EXTAL2(48MHz) is a source clock of 8KHz. 10: EXTAL1(27MHz) is a source clock of 8KHz. 11: Reserved.
9	VORESET	0	R/W	Reset is issued to the VOSYNC module. 0: The VOSYNC module usually operates. 1: Reset is issued to the VOSYNC module.
8	VOSYNCEN	0	R/W	Net synchronous signal effective bit 0: Even if a net synchronous signal is supplied, 8KHz is not generated. 1: 8KHz is generated based on a net synchronous signal.

Bit	Bit name	Initial value	R/W	Description
7	VOMASTER	0	R/W	VOSYNC master bit 0: 8KHz is generated based on a net synchronous signal. 1: A net synchronous signal is not used, and 8KHz is generated only from the source clock selected by the VOCLK_SEL bit.
6	SPDIFSEL	0	R/W	SPDIF port selection bit Either of two SPDIF ports that exist in FSI is selected. 0: SPDIF of port B is used. 1: SPDIF of port A is used.
5 to 3	-	All0	R	Reserved These bits are always read as 0. The write value should always be 0.
2 to 0	USC_SEL [2:0]	000	R/W	FSI/BBIF2 pins selection bit 000: General mode (BBIF2/FSI is connected with each external pin). 001: Through mode (FSI pins are connected with BBIF2 pins internally). 010: FSI-BBIF connection mode (BBIF module is connected with the FSI port internally). 011: Reserved. 100: FSI-VOSYNC master (SCLK/SYNC of FSI is supplied by VOSYNC). 101: Reserved. 110: FSI-BBIF connection mode (BBIF module is connected with the FSI port internally. SCLK/SYNC is supplied by VOSYNC). 111: Reserved.

57.2.8 USC Control register2 (USCCR2)

ビット:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	IRQ_INV	IRQ_MASK	VINT_IRQSEL[5:0]					
初期値:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit name	Initial value	R/W	Description
15 to 8	-	All0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	IRQ_INV	0	R/W	IRQ inversion bit 0: The input of IRQ pin is input to SPU2 as it is. 1: The input of IRQ is reversed and it is input to SPU2.
6	IRQ_MASK	0	R/W	It is a mask bit as for interrupt from IRQ pin to SPU2. 0: Interrupt from IRQ pin to SPU2 is masked. 1: The input from IRQ pin is input to SPU2 as interrupt.

Bit	Bit name	Initial value	R/W	Description
5 to 0	VINT_IRQ SEL[5:0]	000000	R/W	IRQ pins selection bit One of the 32 IRQ pins is used as interrupt of SPU2. IRQ of this bit value is selected as interrupt of SPU2.

57.2.9 CKO Control register (CKOCR)

ビット：	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DRV[1:0]	
初期値：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
R/W：	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit name	Initial value	R/W	Description
15 to 2	-	All0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	DRV[1:0]	11	R/W	Select the drivability when output. 00: Low drivability 01: Middle drivability 10: High drivability 11: Maximum drivability

57.2.10 WE0 Control register (WE0CR)

ビット：	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DRV[1:0]	
初期値：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
R/W：	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit name	Initial value	R/W	Description
15 to 2	-	All0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	DRV[1:0]	11	R/W	Select the drivability when output. 00: Low drivability 01: Middle drivability 10: High drivability 11: Maximum drivability

57.2.11 WE1 Control register (WE1CR)

ビット：	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DRV[1:0]	
初期値：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
R/W：	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit name	Initial value	R/W	Description
15 to 2	-	All0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	DRV[1:0]	11	R/W	Select the drivability when output. 00: Low drivability 01: Middle drivability 10: High drivability 11: Maximum drivability

57.2.12 MMCCLK0 Control register (MMCCLK0CR)

ビット：	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DRV[1:0]	
初期値：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
R/W：	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit name	Initial value	R/W	Description
15 to 2	-	All0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	DRV[1:0]	11	R/W	Select the drivability when output. 00: Low drivability 01: Middle drivability 10: High drivability 11: Maximum drivability

57.2.13 MMCCLK1 Control register (MMCCLK1CR)

ビット：	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DRV[1:0]	
初期値：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
R/W：	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit name	Initial value	R/W	Description
15 to 2	-	All0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit name	Initial value	R/W	Description
1, 0	DRV[1:0]	11	R/W	Select the drivability when output. 00: Low drivability 01: Middle drivability 10: High drivability 11: Maximum drivability

57.2.14 SDHICLK0 Control register (SDHICLK0CR)

ビット：	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DRV[1:0]	
初期値：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
R/W：	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit name	Initial value	R/W	Description
15 to 2	-	All0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	DRV[1:0]	11	R/W	Select the drivability when output. 00: Low drivability 01: Middle drivability 10: High drivability 11: Maximum drivability

57.2.15 SDHICLK1 Control register (SDHICLK1CR)

ビット：	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DRV[1:0]	
初期値：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
R/W：	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit name	Initial value	R/W	Description
15 to 2	-	All0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	DRV[1:0]	11	R/W	Select the drivability when output. 00: Low drivability 01: Middle drivability 10: High drivability 11: Maximum drivability

57.2.16 SDHICLK2 Control register (SDHICLK2CR)

ビット：	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DRV[1:0]	
初期値：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
R/W：	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit name	Initial value	R/W	Description
15 to 2	-	All0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	DRV[1:0]	11	R/W	Select the drivability when output. 00: Low drivability 01: Middle drivability 10: High drivability 11: Maximum drivability

57.2.17 VCCQ Domain setting register (VCCQ18CR)

ビット：	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	RSEL	—	—	DRV[1:0]	
初期値：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
R/W：	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R/W	R/W

Bit	Bit name	Initial value	R/W	Description
15 to 5	-	All0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	RSEL	0	R/W	Specifies the pull-up/pull-down resistance. 0: Low resistance 1: High resistance
3, 2	-	All0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	DRV[1:0]	11	R/W	Select the drivability when output. 00: Low drivability 01: Middle drivability 10: High drivability 11: Maximum drivability

57.2.18 VCCQ Domain(BSC Pins) Setting register (VCCQBSCCR)

ビット：	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DRV[1:0]	
初期値：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
R/W：	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit name	Initial value	R/W	Description
15 to 2	-	All0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	DRV[1:0]	11	R/W	Select the drivability when output. 00: Low drivability 01: Middle drivability 10: High drivability 11: Maximum drivability

57.2.19 VCCQ Domain(VIO Pins) Setting register (VCCQVIOCR)

ビット：	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DRV[1:0]	
初期値：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
R/W：	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit name	Initial value	R/W	Description
15 to 2	-	All0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	DRV[1:0]	11	R/W	Select the drivability when output. 00: Low drivability 01: Middle drivability 10: High drivability 11: Maximum drivability

57.2.20 VCCQ Domain(LCD Pins) Setting register (VCCQLCDCR)

ビット：	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DRV[1:0]	
初期値：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
R/W：	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit name	Initial value	R/W	Description
15 to 2	-	All0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit name	Initial value	R/W	Description
1, 0	DRV[1:0]	11	R/W	Select the drivability when output. 00: Low drivability 01: Middle drivability 10: High drivability 11: Maximum drivability

57.2.21 VCCQ Domain(MFI Pins) Setting register (VCCQMFICR)

ビット：	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DRV[1:0]	
初期値：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
R/W：	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit name	Initial value	R/W	Description
15 to 2	-	All0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	DRV[1:0]	11	R/W	Select the drivability when output. 00: Low drivability 01: Middle drivability 10: High drivability 11: Maximum drivability

57.2.22 VCCQ3 Domain setting register (VCCQ3CR)

ビット:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	RSEL	–	–	–	–
初期値:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R

Bit	Bit name	Initial value	R/W	Description
15 to 5	-	All0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	RSEL	0	R/W	Specifies the pull-up/pull-down resistance. 0: Low resistance 1: High resistance
1, 0	-	All1	R	Reserved These bits are always read as 0. The write value should always be 0.

57. 2. 23 VCCQ_MC0 Domain setting register (VCCQMC0CR)

ビット：	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	RSEL	—	—	DRV[1:0]	
初期値：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
R/W：	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R/W	R/W

Bit	Bit name	Initial value	R/W	Description
15 to 5	-	All0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	RSEL	0	R/W	Specifies the pull-up/pull-down resistance. 0: Low resistance 1: High resistance
3, 2	-	All0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	DRV[1:0]	11	R/W	Select the drivability when output. 00: Low drivability 01: Middle drivability 10: High drivability 11: Maximum drivability

57. 2. 24 VCCQ_MC1 Domain setting register (VCCQMC1CR)

ビット：	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	RSEL	—	—	DRV[1:0]	
初期値：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
R/W：	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R/W	R/W

Bit	Bit name	Initial value	R/W	Description
15 to 5	-	All0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	RSEL	0	R/W	Specifies the pull-up/pull-down resistance. 0: Low resistance 1: High resistance
3, 2	-	All0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit name	Initial value	R/W	Description
1, 0	DRV[1:0]	11	R/W	Select the drivability when output. 00: Low drivability 01: Middle drivability 10: High drivability 11: Maximum drivability

57. 2. 25 IIC Control register (IICCR)

ビット:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	IIC0_CONTA	IIC0_CONTB	IIC1_CONTA	IIC1_CONTB	–	HDMIIIC_STBY	IIC0_PS33E	IIC1_PS33E
初期値:	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit name	Initial value	R/W	Description
15	-	1	R	Reserved These bits are always read as 1. The write value should always be 1.
14 to 8	-	All0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	IIC0_CONTA	0	R/W	IIC0 tf Characteristics switching signal
6	IIC0_CONTB	0		CONTA CONTB tf Value VIH/VIL Value 0 0 Default Default 1 0 8ns or Smaller Default 0 1 Default VIH=20mV Decrease VIL=20mV increase 1 1 8ns or Smaller VIH=20mV Decrease VIL=20mV increase
5	IIC1_CONTA	0	R/W	IIC1tf Characteristics switching signal
4	IIC1_CONTB	0	R/W	CONTA CONTB tf Value VIH/VIL Value 0 0 Default Default 1 0 8ns or Smaller Default 0 1 Default VIH=20mV Decrease VIL=20mV increase 1 1 8ns or Smaller VIH=20mV Decrease VIL=20mV increase
3	-	0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	HDMIIIC_STBY	0	R/W	Controls the standby of the HDMI-IIC interface buffer (HDMI_SCL and HDMI_SDA pins). 0: Normal use 1: Standby The time from when this bit is cleared to 0 until the I2C buffer is powered up and operates stably is specified 600ns at a maximum.
1	IIC0_PS33E	0	R/W	Controls the Schmitt input of the IIC0_SCL and IIC0_SDA pins. If IO Voltage(VccQ) of IIC0_SCL and IIC0_SDA pins is 1.8V, and External pull-up voltage is 2.8V, please select “for 1.8V”. 0: For 1.8V 1: For 2.8V

Bit	Bit name	Initial value	R/W	Description
0	IIC1_PS33E	0	R/W	Controls the Schmitt input of the IIC1_SCL and IIC1_SDA pins(1.8V use/2.8V use). If IO Voltage(VccQ) of IIC1_SCL and IIC1_SDA pins is 1.8V, and External pull-up voltage is 2.8V, please select “for 1.8V”. 0: For 1.8V 1: For 2.8V

57. 2. 26 PORTL095_064 Data register (PORTL095_064DR)

Bit	Bit name	Description
31 to 0	PORTL095 to PORTL064	A Port Data Register for Function Numbers 095 to 064 in side L When the IE bit of PORTnCR is set to 1, the level of the corresponding pin is read. When the IE bit of PORTnCR is set to 0, the register value is read. If no corresponding port exists for the function number, 0 is read. When the OE bit of PORTnCR is set to 1, the write value is output from the pin.

57. 2. 27 PORTL127_096 Data register (PORTL127_096DR)

Bit	Bit name	Description
31 to 0	PORTL127 to PORTL096	A Port Data Register for Function Numbers 127 to 096 in side L When the IE bit of PORTnCR is set to 1, the level of the corresponding pin is read. When the IE bit of PORTnCR is set to 0, the register value is read. If no corresponding port exists for the function number, 0 is read. When the OE bit of PORTnCR is set to 1, the write value is output from the pin.

57. 2. 28 PORTL159_128 Data register (PORTL159_128DR)

Bit	Bit name	Description
31 to 0	PORTL159 to PORTL128	A Port Data Register for Function Numbers 159 to 128 in side L When the IE bit of PORTnCR is set to 1, the level of the corresponding pin is read. When the IE bit of PORTnCR is set to 0, the register value is read. If no corresponding port exists for the function number, 0 is read. When the OE bit of PORTnCR is set to 1, the write value is output from the pin.

57.2.29 PORTL191_160 Data register (PORTL191_160DR)

Bit	Bit name	Description
31 to 0	PORTL191 to PORTL160	A Port Data Register for Function Numbers 191 to 160 in side L When the IE bit of PORTnCR is set to 1, the level of the corresponding pin is read. When the IE bit of PORTnCR is set to 0, the register value is read. If no corresponding port exists for the function number, 0 is read. When the OE bit of PORTnCR is set to 1, the write value is output from the pin.

57.2.30 PORTD031_000 Data register (PORTD031_000DR)

Bit	Bit name	Description
31 to 0	PORTD031 to PORTD000	A Port Data Register for Function Numbers 031 to 000 in side D When the IE bit of PORTnCR is set to 1, the level of the corresponding pin is read. When the IE bit of PORTnCR is set to 0, the register value is read. If no corresponding port exists for the function number, 0 is read. When the OE bit of PORTnCR is set to 1, the write value is output from the pin.

57.2.31 PORTD063_032 Data register (PORTD063_032DR)

Bit	Bit name	Description
31 to 0	PORTD063 to PORTD032	A Port Data Register for Function Numbers 063 to 032 in side D When the IE bit of PORTnCR is set to 1, the level of the corresponding pin is read. When the IE bit of PORTnCR is set to 0, the register value is read. If no corresponding port exists for the function number, 0 is read. When the OE bit of PORTnCR is set to 1, the write value is output from the pin.

57. 2. 32 PORTR063_032 Data register (PORTR063_032DR)

Bit	Bit name	Description
31 to 0	PORTR063 to PORTR032	A Port Data Register for Function Numbers 063 to 032 in side R When the IE bit of PORTnCR is set to 1, the level of the corresponding pin is read. When the IE bit of PORTnCR is set to 0, the register value is read. If no corresponding port exists for the function number, 0 is read. When the OE bit of PORTnCR is set to 1, the write value is output from the pin.

57.2.33 PORTR095_064 Data register (PORTR095_064DR)

Bit	Bit name	Description
31 to 0	PORTR095 to PORTR064	A Port Data Register for Function Numbers 095 to 064 in side R When the IE bit of PORTnCR is set to 1, the level of the corresponding pin is read. When the IE bit of PORTnCR is set to 0, the register value is read. If no corresponding port exists for the function number, 0 is read. When the OE bit of PORTnCR is set to 1, the write value is output from the pin.

57.2.34 PORTR191_160 Data register (PORTR191_160DR)

Bit	Bit name	Description
31 to 0	PORTR191 to PORTR160	A Port Data Register for Function Numbers 191 to 160 in side R When the IE bit of PORTnCR is set to 1, the level of the corresponding pin is read. When the IE bit of PORTnCR is set to 0, the register value is read. If no corresponding port exists for the function number, 0 is read. When the OE bit of PORTnCR is set to 1, the write value is output from the pin.

57.2.35 PORTU127_096 Data register (PORTU127_096DR)

Bit	Bit name	Description
31 to 0	PORTU127 to PORTU096	A Port Data Register for Function Numbers 127 to 096 in side U When the IE bit of PORTnCR is set to 1, the level of the corresponding pin is read. When the IE bit of PORTnCR is set to 0, the register value is read. If no corresponding port exists for the function number, 0 is read. When the OE bit of PORTnCR is set to 1, the write value is output from the pin.

57.2.36 PORTU159_128 Data register (PORTU159_128DR)

Bit	Bit name	Description
31 to 0	PORTU159 to PORTU128	A Port Data Register for Function Numbers 159 to 128 in side U When the IE bit of PORTnCR is set to 1, the level of the corresponding pin is read. When the IE bit of PORTnCR is set to 0, the register value is read. If no corresponding port exists for the function number, 0 is read. When the OE bit of PORTnCR is set to 1, the write value is output from the pin.

57.2.37 PORTL095_064 Data set register (PORTL095_064DSR)

Bit	Bit name	Description
31 to 0	PORTL095 to PORTL064	A Data Set Register for Port Data Register PORTL095_064DR for Function Numbers 095 to 064 in side L When the IE bit of PORTnCR is set to 1, the level of the corresponding pin is read. When the IE bit of PORTnCR is set to 0, the PORTL095_064DR register value is read. If no corresponding port exists for the function number, 0 is read. When the OE bit of PORTnCR is set to 1, the desired bit is written to 1 by writing 1 to it and the corresponding pin outputs high. 0: Retains the state. 1: Sets to 1.

57.2.38 PORTL127_096 Data set register (PORTL127_096DSR)

Bit	Bit name	Description
31 to 0	PORTL127 to PORTL096	A Data Set Register for Port Data Register PORTL127_096DR for Function Numbers 127 to 096 in side L When the IE bit of PORTnCR is set to 1, the level of the corresponding pin is read. When the IE bit of PORTnCR is set to 0, the PORTL127_096DR register value is read. If no corresponding port exists for the function number, 0 is read. When the OE bit of PORTnCR is set to 1, the desired bit is written to 1 by writing 1 to it and the corresponding pin outputs high. 0: Retains the state. 1: Sets to 1.

57.2.39 PORTL159_128 Data set register (PORTL159_128DSR)

Bit	Bit name	Description
31 to 0	PORTL159 to PORTL128	A Data Set Register for Port Data Register PORTL159_128DR for Function Numbers 159 to 128 in side L When the IE bit of PORTnCR is set to 1, the level of the corresponding pin is read. When the IE bit of PORTnCR is set to 0, the PORTL159_128DR register value is read. If no corresponding port exists for the function number, 0 is read. When the OE bit of PORTnCR is set to 1, the desired bit is written to 1 by writing 1 to it and the corresponding pin outputs high. 0: Retains the state. 1: Sets to 1.

57.2.40 PORTL191_160 Data set register (PORTL191_160DSR)

Bit	Bit name	Description
31 to 0	PORTL191 to PORTL160	A Data Set Register for Port Data Register PORTL191_160DR for Function Numbers 191 to 160 in side L When the IE bit of PORTnCR is set to 1, the level of the corresponding pin is read. When the IE bit of PORTnCR is set to 0, the PORTL191_160DR register value is read. If no corresponding port exists for the function number, 0 is read. When the OE bit of PORTnCR is set to 1, the desired bit is written to 1 by writing 1 to it and the corresponding pin outputs high. 0: Retains the state. 1: Sets to 1.

57. 2. 41 PORTD031_000 Data set register (PORTD031_000DSR)

Bit	Bit name	Description
31 to 0	PORTD031 to PORTD000	A Data Set Register for Port Data Register PORTD031_000DR for Function Numbers 031 to 000 in side D When the IE bit of PORTnCR is set to 1, the level of the corresponding pin is read. When the IE bit of PORTnCR is set to 0, the PORTD031_000DR register value is read. If no corresponding port exists for the function number, 0 is read. When the OE bit of PORTnCR is set to 1, the desired bit is written to 1 by writing 1 to it and the corresponding pin outputs high. 0: Retains the state. 1: Sets to 1.

57. 2. 42 PORTD063_032 Data set register (PORTD063_032DSR)

Bit	Bit name	Description
31 to 0	PORTD063 to PORTD032	A Data Set Register for Port Data Register PORTD063_032DR for Function Numbers 063 to 032 in side D When the IE bit of PORTnCR is set to 1, the level of the corresponding pin is read. When the IE bit of PORTnCR is set to 0, the PORTD063_032DR register value is read. If no corresponding port exists for the function number, 0 is read. When the OE bit of PORTnCR is set to 1, the desired bit is written to 1 by writing 1 to it and the corresponding pin outputs high. 0: Retains the state. 1: Sets to 1.

57. 2. 43 PORTR063_032 Data set register (PORTR063_032DSR)

Bit	Bit name	Description
31 to 0	PORTR063 to PORTR032	A Data Set Register for Port Data Register PORTR063_032DR for Function Numbers 063 to 032 in side R When the IE bit of PORTnCR is set to 1, the level of the corresponding pin is read. When the IE bit of PORTnCR is set to 0, the PORTR063_032DR register value is read. If no corresponding port exists for the function number, 0 is read. When the OE bit of PORTnCR is set to 1, the desired bit is written to 1 by writing 1 to it and the corresponding pin outputs high. 0: Retains the state. 1: Sets to 1.

57. 2. 44 PORTR095_064 Data set register (PORTR095_064DSR)

Bit	Bit name	Description
31 to 0	PORTR095 to PORTR064	A Data Set Register for Port Data Register PORTR095_064DR for Function Numbers 095 to 064 in side R When the IE bit of PORTnCR is set to 1, the level of the corresponding pin is read. When the IE bit of PORTnCR is set to 0, the PORTR095_064DR register value is read. If no corresponding port exists for the function number, 0 is read. When the OE bit of PORTnCR is set to 1, the desired bit is written to 1 by writing 1 to it and the corresponding pin outputs high. 0: Retains the state. 1: Sets to 1.

57. 2. 45 PORTR191_160 Data set register (PORTR191_160DSR)

Bit	Bit name	Description
31 to 0	PORTR191 to PORTR160	A Data Set Register for Port Data Register PORTR191_160DR for Function Numbers 191 to 160 in side R When the IE bit of PORTnCR is set to 1, the level of the corresponding pin is read. When the IE bit of PORTnCR is set to 0, the PORTR191_160DR register value is read. If no corresponding port exists for the function number, 0 is read. When the OE bit of PORTnCR is set to 1, the desired bit is written to 1 by writing 1 to it and the corresponding pin outputs high. 0: Retains the state. 1: Sets to 1.

57. 2. 46 PORTU127_096 Data set register (PORTU127_096DSR)

Bit	Bit name	Description
31 to 0	PORTU127 to PORTU096	A Data Set Register for Port Data Register PORTU127_096DR for Function Numbers 127 to 096 in side U When the IE bit of PORTnCR is set to 1, the level of the corresponding pin is read. When the IE bit of PORTnCR is set to 0, the PORTU127_096DR register value is read. If no corresponding port exists for the function number, 0 is read. When the OE bit of PORTnCR is set to 1, the desired bit is written to 1 by writing 1 to it and the corresponding pin outputs high. 0: Retains the state. 1: Sets to 1.

57. 2. 47 PORTU159_128 Data set register (PORTU159_128DSR)

Bit	Bit name	Description
31 to 0	PORTU159 to PORTU128	A Data Set Register for Port Data Register PORTU159_128DR for Function Numbers 159 to 128 in side U When the IE bit of PORTnCR is set to 1, the level of the corresponding pin is read. When the IE bit of PORTnCR is set to 0, the PORTU159_128DR register value is read. If no corresponding port exists for the function number, 0 is read. When the OE bit of PORTnCR is set to 1, the desired bit is written to 1 by writing 1 to it and the corresponding pin outputs high. 0: Retains the state. 1: Sets to 1.

57. 2. 48 PORTL095_064 Data clear register (PORTL095_064DCR)

Bit	Bit name	Description
31 to 0	PORTL095 to PORTL064	A Data Clear Register for Port Data Register PORTL095_064DR for Function Numbers 095 to 064 in side L When the IE bit of PORTnCR is set to 1, the level of the corresponding pin is read. When the IE bit of PORTnCR is set to 0, the PORTL095_064DR register value is read. If no corresponding port exists for the function number, 0 is read. When the OE bit of PORTnCR is set to 1, the desired bit is written to 0 by writing 1 to it and the corresponding pin outputs low. 0: Retains the state. 1: Clears to 0.

57.2.49 PORTL127_096 Data clear register (PORTL127_096DCR)

Bit	Bit name	Description
31 to 0	PORTL127 to PORTL096	A Data Clear Register for Port Data Register PORTL127_096DR for Function Numbers 127 to 096 in side L When the IE bit of PORTnCR is set to 1, the level of the corresponding pin is read. When the IE bit of PORTnCR is set to 0, the PORTL127_096DR register value is read. If no corresponding port exists for the function number, 0 is read. When the OE bit of PORTnCR is set to 1, the desired bit is written to 0 by writing 1 to it and the corresponding pin outputs low. 0: Retains the state. 1: Clears to 0.

57.2.50 PORTL159_128 Data clear register (PORTL159_128DCR)

Bit	Bit name	Description
31 to 0	PORTL159 to PORTL128	A Data Clear Register for Port Data Register PORTL159_128DR for Function Numbers 159 to 128 in side L When the IE bit of PORTnCR is set to 1, the level of the corresponding pin is read. When the IE bit of PORTnCR is set to 0, the PORTL159_128DR register value is read. If no corresponding port exists for the function number, 0 is read. When the OE bit of PORTnCR is set to 1, the desired bit is written to 0 by writing 1 to it and the corresponding pin outputs low. 0: Retains the state. 1: Clears to 0.

57.2.51 PORTL191_160 Data clear register (PORTL191_160DCR)

Bit	Bit name	Description
31 to 0	PORTL191 to PORTL160	A Data Clear Register for Port Data Register PORTL191_160DR for Function Numbers 191 to 160 in side L When the IE bit of PORTnCR is set to 1, the level of the corresponding pin is read. When the IE bit of PORTnCR is set to 0, the PORTL191_160DR register value is read. If no corresponding port exists for the function number, 0 is read. When the OE bit of PORTnCR is set to 1, the desired bit is written to 0 by writing 1 to it and the corresponding pin outputs low. 0: Retains the state. 1: Clears to 0.

57.2.52 PORTD031_000 Data clear register (PORTD031_000DCR)

Bit	Bit name	Description
31 to 0	PORTD031 to PORTD000	A Data Clear Register for Port Data Register PORTD031_000DR for Function Numbers 031 to 000 in side D When the IE bit of PORTnCR is set to 1, the level of the corresponding pin is read. When the IE bit of PORTnCR is set to 0, the PORTD031_000DR register value is read. If no corresponding port exists for the function number, 0 is read. When the OE bit of PORTnCR is set to 1, the desired bit is written to 0 by writing 1 to it and the corresponding pin outputs low. 0: Retains the state. 1: Clears to 0.

57.2.53 PORTD063_032 Data clear register (PORTD063_032DCR)

Bit	Bit name	Description
31 to 0	PORTD063 to PORTD032	A Data Clear Register for Port Data Register PORTD063_032DR for Function Numbers 063 to 032 in side D When the IE bit of PORTnCR is set to 1, the level of the corresponding pin is read. When the IE bit of PORTnCR is set to 0, the PORTD063_032DR register value is read. If no corresponding port exists for the function number, 0 is read. When the OE bit of PORTnCR is set to 1, the desired bit is written to 0 by writing 1 to it and the corresponding pin outputs low. 0: Retains the state. 1: Clears to 0.

57.2.54 PORTR063_032 Data clear register (PORTR063_032DCR)

Bit	Bit name	Description
31 to 0	PORTR063 to PORTR032	A Data Clear Register for Port Data Register PORTR063_032DR for Function Numbers 063 to 032 in side R When the IE bit of PORTnCR is set to 1, the level of the corresponding pin is read. When the IE bit of PORTnCR is set to 0, the PORTR063_032DR register value is read. If no corresponding port exists for the function number, 0 is read. When the OE bit of PORTnCR is set to 1, the desired bit is written to 0 by writing 1 to it and the corresponding pin outputs low. 0: Retains the state. 1: Clears to 0.

57.2.55 PORTR095_064 Data clear register (PORTR095_064DCR)

Bit	Bit name	Description
31 to 0	PORTR095 to PORTR064	A Data Clear Register for Port Data Register PORTR095_064DR for Function Numbers 095 to 064 in side R When the IE bit of PORTnCR is set to 1, the level of the corresponding pin is read. When the IE bit of PORTnCR is set to 0, the PORTR095_064DR register value is read. If no corresponding port exists for the function number, 0 is read. When the OE bit of PORTnCR is set to 1, the desired bit is written to 0 by writing 1 to it and the corresponding pin outputs low. 0: Retains the state. 1: Clears to 0.

57. 2. 56 PORTR191_160 Data clear register (PORTR191_160DCR)

Bit	Bit name	Description
31 to 0	PORTR191 to PORTR160	A Data Clear Register for Port Data Register PORTR191_160DR for Function Numbers 191 to 160 in side R When the IE bit of PORTnCR is set to 1, the level of the corresponding pin is read. When the IE bit of PORTnCR is set to 0, the PORTR191_160DR register value is read. If no corresponding port exists for the function number, 0 is read. When the OE bit of PORTnCR is set to 1, the desired bit is written to 0 by writing 1 to it and the corresponding pin outputs low. 0: Retains the state. 1: Clears to 0.

57.2.57 PORTU127_096 Data clear register (PORTU127_096DCR)

Bit	Bit name	Description
31 to 0	PORTU127 to PORTU096	A Data Clear Register for Port Data Register PORTU127_096DR for Function Numbers 127 to 096 in side U When the IE bit of PORTnCR is set to 1, the level of the corresponding pin is read. When the IE bit of PORTnCR is set to 0, the PORTU127_096DR register value is read. If no corresponding port exists for the function number, 0 is read. When the OE bit of PORTnCR is set to 1, the desired bit is written to 0 by writing 1 to it and the corresponding pin outputs low. 0: Retains the state. 1: Clears to 0.

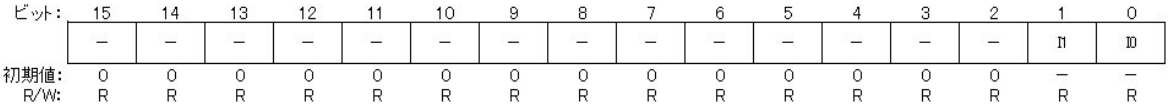
57.2.58 PORTU159_128 Data clear register (PORTU159_128DCR)

Bit	Bit name	Description
31 to 0	PORTU159 to PORTU128	A Data Clear Register for Port Data Register PORTU159_128DR for Function Numbers 159 to 128 in side U When the IE bit of PORTnCR is set to 1, the level of the corresponding pin is read. When the IE bit of PORTnCR is set to 0, the PORTU159_128DR register value is read. If no corresponding port exists for the function number, 0 is read. When the OE bit of PORTnCR is set to 1, the desired bit is written to 0 by writing 1 to it and the corresponding pin outputs low. 0: Retains the state. 1: Clears to 0.

57.2.59 CPORT GPI Register (CGPI)

CGPI is a 16-bit read-only register and the corresponding GPI pin level is read.

This register is contained in the AP block.

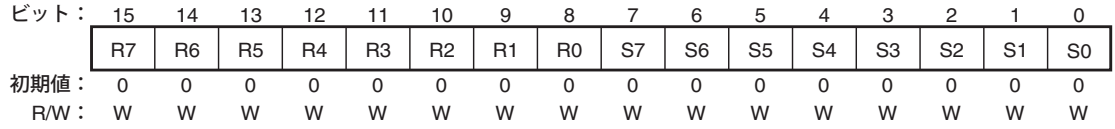


Bit	Bit name	Initial value	R/W	Description
15 -2	-	0	R	Reserved These bits are always read as 0.
1	I1	-	R	The level of the pin corresponding to GPI1 is read.
0	I0	-	R	The level of the pin corresponding to GPI0 is read.

57.2.60 CPORT GPO Set reset register (CGPOSR)

CGPOSR is a 16-bit write-only register that sets the output data of the general output ports in the AP block. This register shares addresses with CGPOR.

This register is contained in the AP block.



Bit	Bit name	Initial value	R/W	Description
15	R7	0	W	When this bit is set to 1, GPO7 outputs 0 (reset).
14	R6	0	W	When this bit is set to 1, GPO6 outputs 0 (reset).
13	R5	0	W	When this bit is set to 1, GPO5 outputs 0 (reset).
12	R4	0	W	When this bit is set to 1, GPO4 outputs 0 (reset).
11	R3	0	W	When this bit is set to 1, GPO3 outputs 0 (reset).
10	R2	0	W	When this bit is set to 1, GPO2 outputs 0 (reset).
9	R1	0	W	When this bit is set to 1, GPO1 outputs 0 (reset).
8	R0	0	W	When this bit is set to 1, GPO0 outputs 0 (reset).
7	S7	0	W	When this bit is set to 1, GPO7 outputs 1 (set).
6	S6	0	W	When this bit is set to 1, GPO6 outputs 1 (set).
5	S5	0	W	When this bit is set to 1, GPO5 outputs 1 (set).
4	S4	0	W	When this bit is set to 1, GPO4 outputs 1 (set).
3	S3	0	W	When this bit is set to 1, GPO3 outputs 1 (set).
2	S2	0	W	When this bit is set to 1, GPO2 outputs 1 (set).

Bit	Bit name	Initial value	R/W	Description
1	S1	0	W	When this bit is set to 1, GPO1 outputs 1 (set).
0	S0	0	W	When this bit is set to 1, GPO0 outputs 1 (set).

57.2.61 CPORT GPO Read register (CGPOR)

CGPOR is a 16-bit read-only register that reads the output data of the general output ports in the AP block. This register shares addresses with CGPOSR.

This register is contained in the AP block.

ビット：	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	D7	D6	D5	D4	D3	D2	D1	D0
初期値：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W：	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit name	Initial value	R/W	Description
15 to 8	-	All0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	D7	0	R	GPO7 output data
6	D6	0	R	GPO6 output data
5	D5	0	R	GPO5 output data
4	D4	0	R	GPO4 output data
3	D3	0	R	GPO3 output data
2	D2	0	R	GPO2 output data
1	D1	0	R	GPO1 output data
0	D0	0	R	GPO0 output data

57.2.62 CPORT GPOR2S Set reset register (CGPOR2SSR)

CGPOR2SSR is a 16-bit write-only register that sets the output data notifying the WakeUp factor from RT to SYS domain. This register shares addresses with CGPOR2SR.

This register is contained in the AP block.

ビット：	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	R7	R6	R5	R4	R3	R2	R1	R0	S7	S6	S5	S4	S3	S2	S1	S0
初期値：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W：	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Bit	Bit name	Initial value	R/W	Description
15	R7	0	W	When this bit is set to 1, GPOR2S7 outputs 0 (reset).
14	R6	0	W	When this bit is set to 1, GPOR2S6 outputs 0 (reset).
13	R5	0	W	When this bit is set to 1, GPOR2S5 outputs 0 (reset).
12	R4	0	W	When this bit is set to 1, GPOR2S4 outputs 0 (reset).
11	R3	0	W	When this bit is set to 1, GPOR2S3 outputs 0 (reset).
10	R2	0	W	When this bit is set to 1, GPOR2S2 outputs 0 (reset).
9	R1	0	W	When this bit is set to 1, GPOR2S1 outputs 0 (reset).
8	R0	0	W	When this bit is set to 1, GPOR2S0 outputs 0 (reset).
7	S7	0	W	When this bit is set to 1, GPOR2S7 outputs 1 (set).
6	S6	0	W	When this bit is set to 1, GPOR2S6 outputs 1 (set).
5	S5	0	W	When this bit is set to 1, GPOR2S5 outputs 1 (set).
4	S4	0	W	When this bit is set to 1, GPOR2S4 outputs 1 (set).
3	S3	0	W	When this bit is set to 1, GPOR2S3 outputs 1 (set).
2	S2	0	W	When this bit is set to 1, GPOR2S2 outputs 1 (set).
1	S1	0	W	When this bit is set to 1, GPOR2S1 outputs 1 (set).
0	S0	0	W	When this bit is set to 1, GPOR2S0 outputs 1 (set).

57.2.63 CPORT GPOR2S Read register (CGPOR2SR)

CGPOR2SR is a 16-bit read-only register that reads the output data notifying the WakeUp factor from RT to SYS domain. This register shares addresses with CGPOR2SSR.

This register is contained in the AP block.

ビット：	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	D7	D6	D5	D4	D3	D2	D1	D0
初期値：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W：	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit name	Initial value	R/W	Description
15 to 8	-	All0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	D7	0	R	GPOR2S7 output data
6	D6	0	R	GPOR2S6 output data
5	D5	0	R	GPOR2S5 output data
4	D4	0	R	GPOR2S4 output data
3	D3	0	R	GPOR2S3 output data
2	D2	0	R	GPOR2S2 output data
1	D1	0	R	GPOR2S1 output data
0	D0	0	R	GPOR2S0 output data

57.2.64 CPORT GPOS2R Set reset registerCGPOS2RSR)

CGPOS2RSR is a 16-bit write-only register that sets the output data notifying the WakeUp factor from SYS to RT domain. This register shares addresses with CGPOS2RR.

This register is contained in the AP block.

ビット：	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	R7	R6	R5	R4	R3	R2	R1	R0	S7	S6	S5	S4	S3	S2	S1	S0
初期値：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W：	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Bit	Bit name	Initial value	R/W	Description
15	R7	0	W	When this bit is set to 1, GPOS2R7 outputs 0 (reset).
14	R6	0	W	When this bit is set to 1, GPOS2R6 outputs 0 (reset).
13	R5	0	W	When this bit is set to 1, GPOS2R5 outputs 0 (reset).
12	R4	0	W	When this bit is set to 1, GPOS2R4 outputs 0 (reset).
11	R3	0	W	When this bit is set to 1, GPOS2R3 outputs 0 (reset).
10	R2	0	W	When this bit is set to 1, GPOS2R2 outputs 0 (reset).
9	R1	0	W	When this bit is set to 1, GPOS2R1 outputs 0 (reset).
8	R0	0	W	When this bit is set to 1, GPOS2R0 outputs 0 (reset).
7	S7	0	W	When this bit is set to 1, GPOS2R7 outputs 1 (set).
6	S6	0	W	When this bit is set to 1, GPOS2R6 outputs 1 (set).
5	S5	0	W	When this bit is set to 1, GPOS2R5 outputs 1 (set).
4	S4	0	W	When this bit is set to 1, GPOS2R4 outputs 1 (set).
3	S3	0	W	When this bit is set to 1, GPOS2R3 outputs 1 (set).
2	S2	0	W	When this bit is set to 1, GPOS2R2 outputs 1 (set).
1	S1	0	W	When this bit is set to 1, GPOS2R1 outputs 1 (set).
0	S0	0	W	When this bit is set to 1, GPOS2R0 outputs 1 (set).

57.2.65 CPORT GPOS2R Lead registerCGPOS2RR)

CGPOS2RR is a 16-bit read-only register that reads the output data notifying the WakeUp factor from SYS to RT domain. This register shares addresses with CGPOS2RSR.

This register is contained in the AP block.

ビット：	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	D7	D6	D5	D4	D3	D2	D1	D0
初期値：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W：	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit name	Initial value	R/W	Description
15 to 8	-	All0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	D7	0	R	GPOS2R7 output data
6	D6	0	R	GPOS2R6 output data
5	D5	0	R	GPOS2R5 output data
4	D4	0	R	GPOS2R4 output data
3	D3	0	R	GPOS2R3 output data
2	D2	0	R	GPOS2R2 output data
1	D1	0	R	GPOS2R1 output data
0	D0	0	R	GPOS2R0 output data

57. 2. 66 USB PHY0 Interruption control registerAP (USBPHY0INTAP)

ビット:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	USB_PHY_INT_EN	USB_PHY_ON_EN	USB_PHY_OFF_EN	USB_PHY_ON	USB_PHY_OFF
初期値:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit name	Initial value	R/W	Description
15 to 5	-	0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	USB_PHY_INT_EN	0	R/W	USB_PHY0 Interruption enable 0 :VBUS0_0 Interruption Effective 1 :VBUS1_0 Interruption Effective
3	USB_PHY_ON_EN	0	R/W	USB_PHY_ON Interruption enabling 0 :USB_OFF Interruption by negate edge detection is repealed. 1 :USB_OFF Interruption by negate edge detection is validated.
2	USB_PHY_OFF_EN	0	R/W	USB_PHY_OFF Interruption enabling 0 :USB_OFF Interruption by assert edge detection is repealed. 1 :USB_OFF Interruption by assert edge detection is validated.
1	USB_PHY_ON	0	R/W	USB_PHY_ON Status register When VBUS assert and USB_OFF bit of USBCR2 is cleared, This bit becomes 1. If you want to clear this bit, Please set this bit 1.
0	USB_PHY_OFF	0	R/W	USB_PHY_OFF Status register When VBUS negate and USB_OFF bit of USBCR2 is setted, This bit becomes 1 If you want to clear this bit, Please set this bit 1.

57.2.67 USB PHY1 Interruption control registerAP (USBPHY1INTAP)

ビット:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	USB_PHY_INT_EN	USB_PHY_ON_EN	USB_PHY_OFF_EN	USB_PHY_ON	USB_PHY_OFF
初期値:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit name	Initial value	R/W	Description
15 to 5	-	0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	USB_PHY_INT_EN	0	R/W	USB_PHY1 Interruption enable 0 :VBUS0_1 interruption effective 1 :VBUS1_1 interruption effective
3	USB_PHY_ON_EN	0	R/W	USB_PHY_ON Interruption enabling 0 :USB_OFF Interruption by negate edge detection is repealed. 1 :USB_OFF Interruption by negate edge detection is validated.
2	USB_PHY_OFF_EN	0	R/W	USB_PHY_OFF Interruption enabling 0 :USB_OFF Interruption by assert edge detection is repealed. 1 :USB_OFF Interruption by assert edge detection is validated.
1	USB_PHY_ON	0	R/W	USB_PHY_ON Status register When VBUS assert and USB_OFF bit of USBCR4 is cleared, This bit becomes 1. If you want to clear this bit, Please set this bit 1.
0	USB_PHY_OFF	0	R/W	USB_PHY_OFF Status register When VBUS negate and USB_OFF bit of USBCR4 is setted, This bit becomes 1 If you want to clear this bit, Please set this bit 1.

57.3 USB Hardware Configuration

The figure below shows the USB hardware configuration in this LSI.

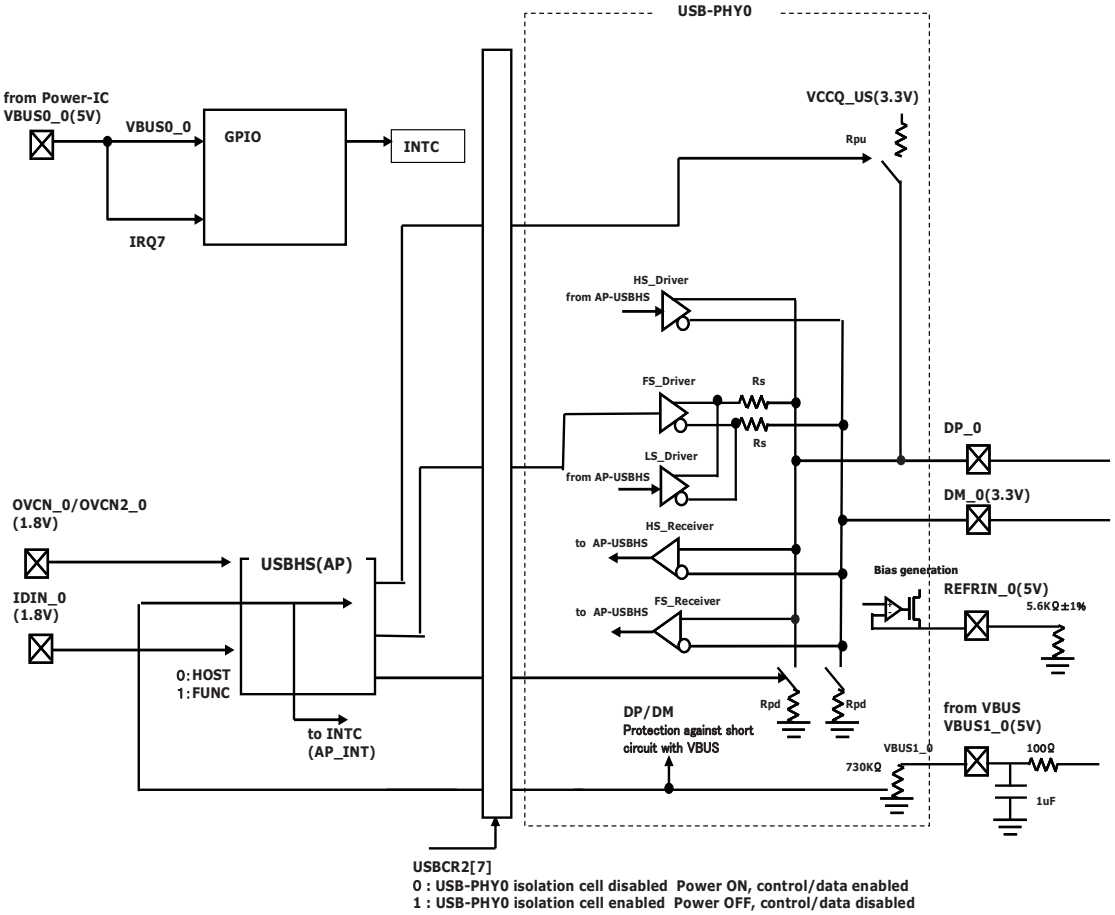


Figure57.1 Schematic Diagram of USB Hardware Configuration

57.4 USB PHY Hardware Configuration of interruption

The figure below shows the USB PHY hardware configuration of interruption in this LSI.

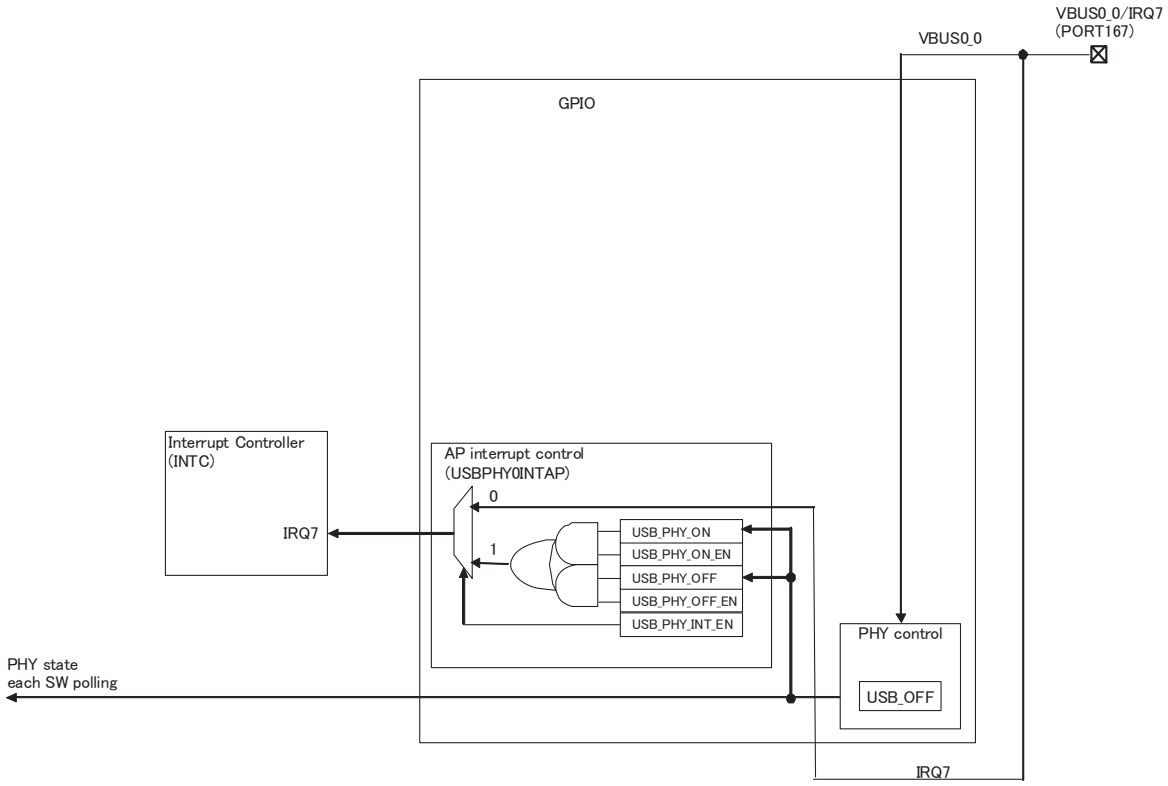


Figure57.2 USB PHY Hardware Configuration of interruption

57.5 PORT Control system

The figure below shows the PORT control configuration in this LSI.

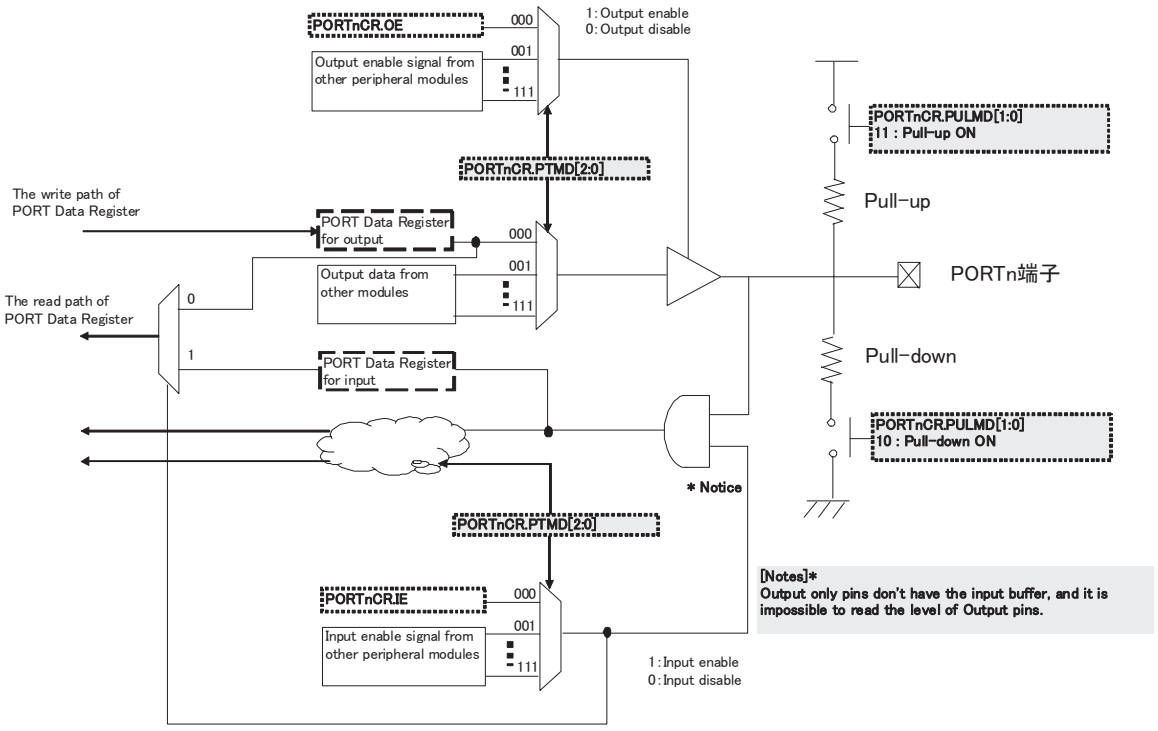


Figure57.3 Schematic view of PORT Control system

Section 58 User Debugging Interface (H-UDI)

The H-UDI is a serial interface, which conforms to the JTAG (IEEE 1149.4: IEEE Standard Test Access Port and Boundary-Scan Architecture) standard. The H-UDI is also used for emulator connection to the AP-RT core.

58.1 Features

The H-UDI is a serial interface that conforms to the JTAG standard. The H-UDI is also used for emulator connection to the AP-RT core. When using an emulator, H-UDI functions should not be used. Refer to the appropriate emulator users manual for the method of connecting the emulator.

The H-UDI has six pins: TCK, TMS, TDI, TDO, TRST_N, and ASEBRK_N/BRKACK. The pin functions except ASEBRK_N/BRKACK and serial communications protocol conform to the JTAG standard. This LSI has additional six pins for emulator connection (AUDSYNC, AUDCK, and AUDATA3 to AUDATA0). Whether these pins are allocated as external pins of this LSI depends on the settings of DBGMD21, DBGMD20, and DBGMDT pins. For details, see section 60, Debugging Specifications (DBG).

Figure 58.1 shows a block diagram of the H-UDI.

The H-UDI circuit includes the TAP (Test Access Port) controller and five registers (SDBPR, SDIR, SDDRH, SDDRL, and SDINT). SDBPR supports the JTAG bypass mode, SDIR is used for commands, SDDR is used for data, and SDINT is used for H-UDI interrupts. SDIR is directly accessed from the TDI and TDO pins.

The TAP controller and control registers are initialized by driving the TRST_N pin low or by applying the TCK signal for five or more clock cycles with the TMS pin set to 1. This initialization sequence is independent of the reset pin for this LSI. Other circuits are initialized by a normal reset.

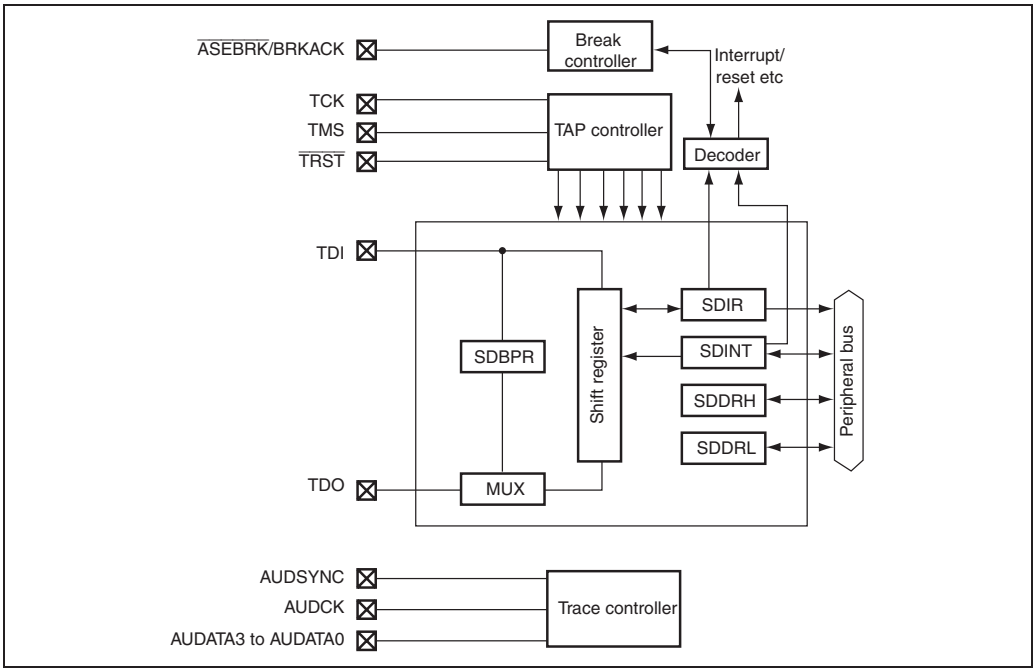


Figure 58.1 H-UDI Block Diagram

58.2 Input/Output Pins

Table 58.1 shows the pin configuration for the H-UDI.

Table 58.1 Pin Configuration

Name	Abbreviation	I/O	Function	When Not in Use
Clock	TCK	Input	Functions as the serial clock input pin stipulated in the JTAG standard. Data input to the H-UDI via the TDI pin or data output via the TDO pin is performed in synchronization with this signal.	Open*[1]
Mode	TMS	Input	Mode Select Input Changing this signal in synchronization with the TCK signal determines the significance of data input via the TDI pin. Its protocol conforms to the JTAG standard (IEEE standard 1149.1).	Open*[1]
Reset	TRST_N*[2]	Input	H-UDI Reset Input This signal is received asynchronously with a TCK signal. Asserting this signal resets the JTAG interface circuit. When a power is supplied, the TRST_N pin should be asserted for a given period regardless of whether or not the JTAG function is used, which differs from the JTAG standard.	Fixed to ground or $\overline{\text{RESET}}$ connection*[3]
Data input	TDI	Input	Data Input Data is sent to the H-UDI by changing this signal in synchronization with the TCK signal.	Open*[1]
Data output	TDO	Output	Data Output Data is read from the H-UDI in synchronization with the TCK signal.	Open
Emulator	ASEBRK_N/ BRKACK	I/O	Pins for an emulator	Open*[1]
Emulator	AUDSYNC, AUDCK, AUDATA3 to AUDATA0	Output	Pins for an emulator	Open

Notes: 1. This pin is pulled up in this LSI. When using interrupts or resets via the H-UDI or emulator, the use of external pull-up resistors will not cause any problem.
2. When using interrupts or resets via the H-UDI or emulator, the TRST_N pin should be designed so that it can be controlled independently and can be controlled to retain low level while the $\overline{\text{RESET}}$ pin is asserted at a power-on reset.

3. This pin should be connected to ground or $\overline{\text{RESET}}$ (or another signal with the same behavior). When this pin is fixed to ground, however, there is one problem. Since the TRST_N pin is pulled up within this LSI, a weak current flows when the pin is externally connected to a ground pin. The value of the current is determined by a resistance of the pull-up MOS for the port pin. Although this current does not affect the operation of this LSI, it consumes unnecessary power.

The TCK clock and the CPG of this LSI should be set to ensure that the frequency of the TCK clock is equal to or less than the frequency of HP ϕ in this LSI.

58.3 Register Descriptions

The H-UDI has the following registers.

Table 58.2 Register Configuration (1)

		CPU Side				
Register Name	**Abbreviation**	**R/W**	**Logical Address**	**Physical Address**	**Size**	**Initial Value*1**
Instruction register	SDIR	R	H'FC11 0000	H'FC11 0000	16	H'0EFF
Data register H	SDDR/SDDRH	R/W	H'FC11 0008	H'FC11 0008	32/16	Undefined
Data register L	SDDRL	R/W	H'FC11 000A	H'FC11 000A	16	Undefined
Interrupt source register	SDINT	R/W	H'FC11 0018	H'FC11 0018	16	H'0000
Bypass register	SDBPR*2	—	—	—	—	Undefined

Note: 1. The low level of the TRST_N pin or the Test-Logic-Reset state of the TAP controller initializes to these values.
2. SDBPR cannot be accessed from the CPU.

Table 58.3 Register Configuration (2)

		H-UDI Side		
Register Name	**Abbreviation**	**R/W**	**Size**	**Initial Value*1**
Instruction register	SDIR	R/W	32	H'FFFF FFFD (fixed value*2)
Data register H	SDDR/SDDRH*4	—	—	—
Data register L	SDDRL*4	—	—	—
Interrupt source register	SDINT	W*3	32	H'0000 0000
Bypass register	SDBPR	R/W	1	Undefined

Notes: 1. The low level of the TRST_N pin or the Test-Logic-Reset state of the TAP controller initializes to these values.
2. When reading via the H-UDI, the value is always H'FFFF FFFD.
3. Only 1 can be written to the LSB by the H-UDI interrupt command.
4. SDDR(SDDRH, SDDRL) cannot be accessed via the H-UDI.

Table 58.4 Register States in Each Operating Mode

Register Name	Abbreviation	Reset
Instruction register	SDIR	H'0EFF
Data register H	SDDR/SDDRH	Undefined
Data register L	SDDRL	Undefined
Interrupt source register	SDINT	H'0000

58.3.1 Instruction Register (SDIR)

SDIR is a 16-bit read-only register that can be read from the CPU. Commands are set via the serial input (TDI). SDIR is initialized by TRST_N or in the Test-Logic-Reset state and can be written by the H-UDI irrespective of the CPU mode. Operation is not guaranteed when a reserved command is set to this register.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TI								—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 8	TI	B'00001110	R	Test Instruction Bits 7 to 0 11111111: Bypass 0110xxxx: H-UDI reset negate 0111xxxx: H-UDI reset assert 101xxxxx: H-UDI interrupt 00001110: Initial state Other than above: Setting prohibited
7 to 0	—	All 1	R	Reserved These bits are always read as 1.

58.3.2 Data Register H and L (SDDRH and SDDRL)

SDDR is a 32-bit register that comprises two registers: SDDRH and SDDRL. SDDRH and SDDRL are also 16-bit registers that can be read from or written to by the CPU. SDDR as a 32-bit register can be read from or written to by the CPU. The register value is not initialized by a reset for the CPU but is initialized by TRST_N.

- SDDRH

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SDDRH data															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

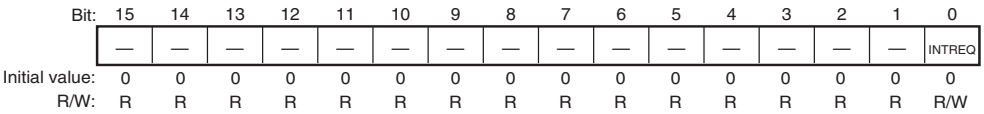
- SDDRL

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SDDRL data															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

58.3.3 Interrupt Source Register (SDINT)

SDINT is a 16-bit register that can be read from or written to by the CPU. Specifying an H-UDI interrupt command in SDIR via H-UDI pin (Update-IR) sets the INTREQ bit to 1. While an H-UDI interrupt command is set in SDIR, SDINT which is connected between the TDI and TDO pins can be read as a 32-bit register. In this case, the upper 16 bits will be 0 and the lower 16 bits represent the SDINT value.

Only 0 can be written to the INTREQ bit by the CPU. While this bit is set to 1, an interrupt request will continue to be generated. This bit, therefore, should be cleared by the interrupt handling routine. It is initialized by TRST_N or in the Test-Logic-Reset state.



Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	INTREQ
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 1	—	All 0	R	Reserved For reading from or writing to these bits, see General Precautions on Handling of Product.
0	INTREQ	0	R/W	Interrupt Request Indicates whether or not an interrupt by an H-UDI interrupt command has occurred. Clearing this bit to 0 by the CPU cancels an interrupt request. When writing 1 to this bit, the previous value is maintained.

58.4 Operation

58.4.1 TAP Control

Figure 58.2 shows the internal states of the TAP controller. The state transitions basically conform to the JTAG standard.

- State transitions occur according to the TMS value at the rising edge of the TCK signal.
- The TDI value is sampled at the rising edge of the TCK signal and shifted at the falling edge of the TCK signal.
- The TDO value is changed at the falling edge of the TCK signal. The TDO signal is in a Hi-Z state other than in the Shift-DR or Shift-IR state.
- A transition to the Test-Logic-Reset by clearing TRST_N to 0 is performed asynchronously with the TCK signal.

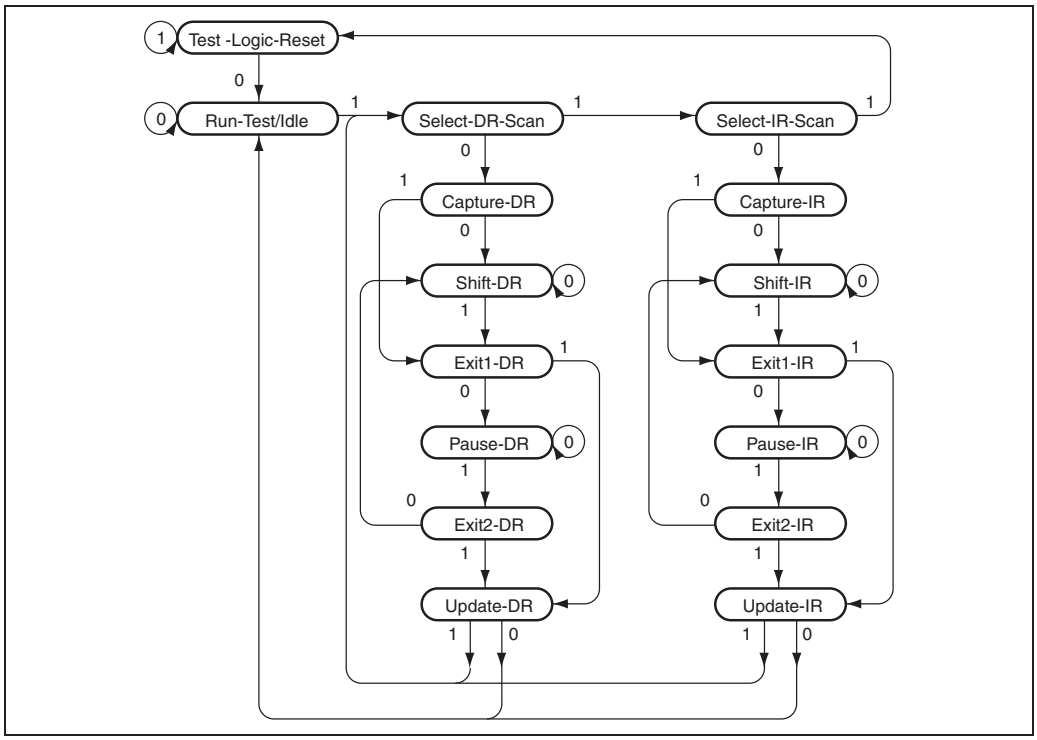


Figure 58.2 TAP Controller State Transitions

58.4.2 H-UDI Reset

The SDIR command can be used to reset the A3RI, A3RV, and A4R areas that include the AP-RT core. After the H-UDI reset assert command has been sent from the H-UDI pin, sending the H-UDI reset negate command resets the CPU (see figure 58.3). The required time between the H-UDI reset assert and H-UDI reset negate commands is the same as the time for holding the reset pin low in order to reset this LSI by a power-on reset.

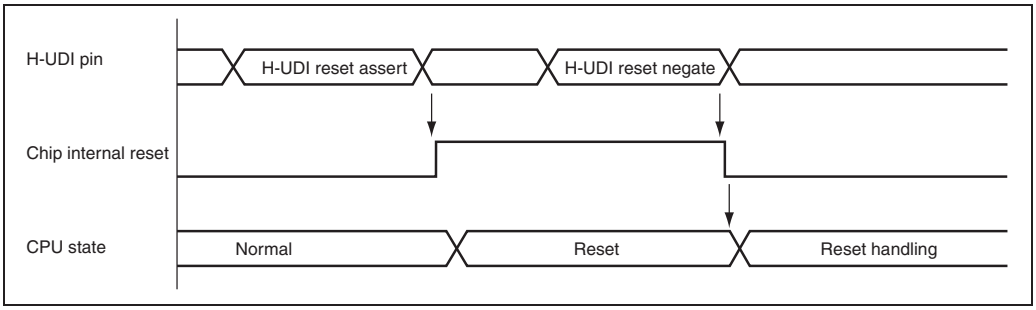


Figure 58.3 H-UDI Reset

58.4.3 H-UDI Interrupt

The H-UDI interrupt function generates an interrupt by setting the appropriate command in SDIR from the H-UDI. An H-UDI interrupt request signal is asserted when the INTREQ bit in SDINT is set to 1 by setting the appropriate command. Since the interrupt request signal is not negated until the INTREQ bit is cleared to 0 by software, it is not possible to lose the interrupt request. While an H-UDI interrupt command is set in SDIR, SDINT is connected between the TDI and TDO pins.

58.5 Usage Notes

- Once an SDIR command is set, it will be changed only by an assertion of the TRST_N signal, making the TAP controller Test-Logic-Reset state, or writing other commands from the H-UDI.
- The H-UDI is used for emulator connection to the AP-RT core. Therefore, H-UDI functions cannot be used when using an emulator.

Section 59 User Break Controller (UBC)

The user break controller (UBC) provides versatile functions to facilitate program debugging of the AP-RT core (SH4AL-DSP). The term "CPU" in this section refers to the AP-RT core. These functions help to ease creation of a self-monitor/debugger, which allows easy program debugging using this LSI alone, without using the in-circuit emulator. Various break conditions can be set in the UBC: instruction fetch or read/write access of an operand, operand size, data contents, address value, and program stop timing for instruction fetch.

59.1 Features

1. The following break conditions can be set.

   Break channels: Two (channels 0 and 1)

   User break conditions can be set independently for channels 0 and 1, and can also be set as a single sequential condition for the two channels, that is, a sequential break. (Sequential break involves two cases such that the channel 0 break condition is satisfied in a certain bus cycle and then the channel 1 break condition is satisfied in a different bus cycle, and vice versa.)

- Address

  When 40 bits containing ASID and 32-bit address are compared with the specified value, all the ASID bits can be compared or masked.

  32-bit address can be masked bit by bit, allowing the user to mask the address in desired page sizes such as lower 12 bits (4-Kbyte page) and lower 10 bits (1-Kbyte page).

  One address bus can be selected among three operand buses: operand address bus (SAB), X memory address bus (XAB), and Y memory address bus (YAB)

- Data

  32 bits can be masked only for channel 1.

  One data bus can be selected among three data buses: operand data bus (SDB), X memory data bus (XDB), and Y memory data bus (YDB)

- Bus cycle

  The program can break either for instruction fetch (PC break) or operand access.

- Read or write access

- Operand sizes

  Byte, word, and longword are supported.

2. The user-designated exception handling routine for the user break condition can be executed.
3. Pre-instruction-execution or post-instruction-execution can be selected as the PC break timing.
4. A maximum of $2^{12} - 1$ repetition counts can be specified as the break condition (available only for channel 1).

Figure 59.1 shows the UBC block diagram.

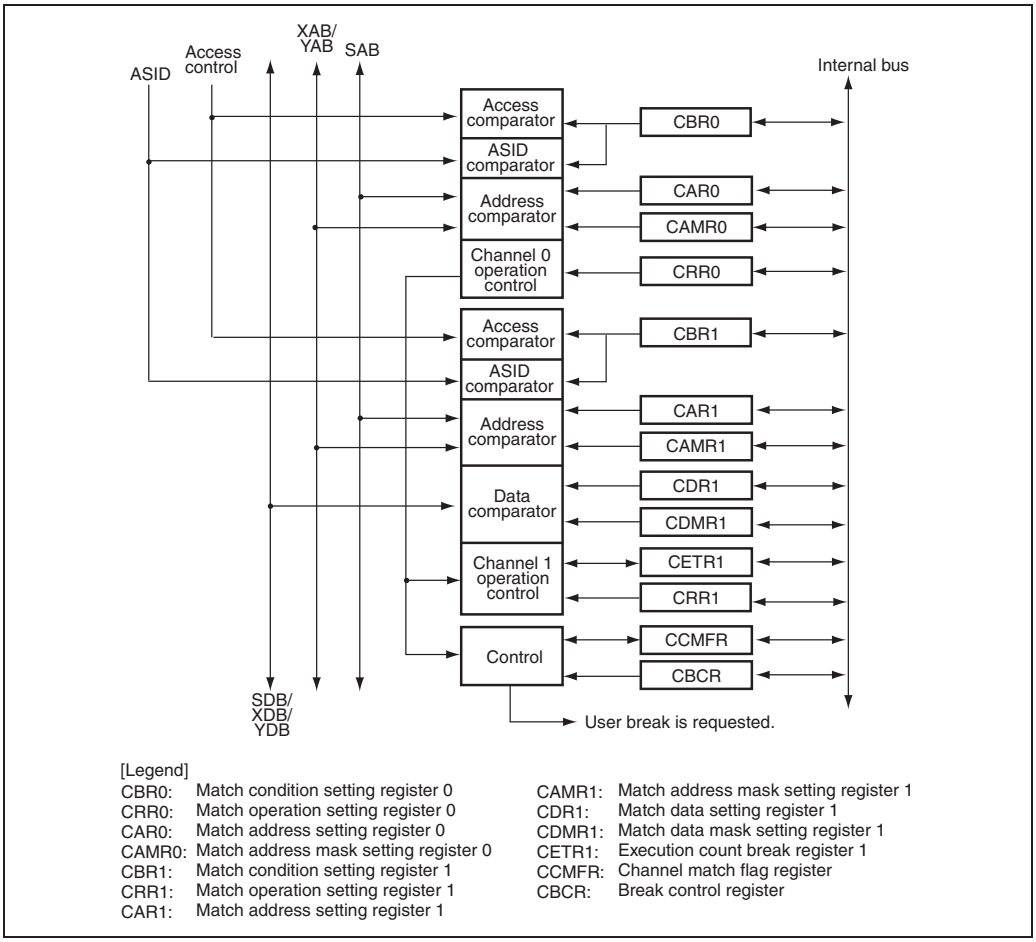


Figure 59.1 Block Diagram of UBC

59.2 Register Descriptions

The UBC has the following registers.

Table 59.1 Register Configuration

Register Name	Abbreviation	R/W	P4 Address	Area 7 Address	Access Size
Match condition setting register 0	CBR0	R/W	H'FF20 0000	H'FF20 0000	32
Match operation setting register 0	CRR0	R/W	H'FF20 0004	H'FF20 0004	32
Match address setting register 0	CAR0	R/W	H'FF20 0008	H'FF20 0008	32
Match address mask setting register 0	CAMR0	R/W	H'FF20 000C	H'FF20 000C	32
Match condition setting register 1	CBR1	R/W	H'FF20 0020	H'FF20 0020	32
Match operation setting register 1	CRR1	R/W	H'FF20 0024	H'FF20 0024	32
Match address setting register 1	CAR1	R/W	H'FF20 0028	H'FF20 0028	32
Match address mask setting register 1	CAMR1	R/W	H'FF20 002C	H'FF20 002C	32
Match data setting register 1	CDR1	R/W	H'FF20 0030	H'FF20 0030	32
Match data mask setting register 1	CDMR1	R/W	H'FF20 0034	H'FF20 0034	32
Execution count break register 1	CETR1	R/W	H'FF20 0038	H'FF20 0038	32
Channel match flag register	CCMFR	R/W	H'FF20 0600	H'FF20 0600	32
Break control register	CBCR	R/W	H'FF20 0620	H'FF20 0620	32

Table 59.2 Register States in Each Operating Mode

Register Name	Abbreviation	Power-On Reset	Sleep	Standby
Match condition setting register 0	CBR0	H'2000 0000	Retained	Retained
Match operation setting register 0	CRR0	H'0000 2000	Retained	Retained
Match address setting register 0	CAR0	Undefined	Retained	Retained
Match address mask setting register 0	CAMR0	Undefined	Retained	Retained
Match condition setting register 1	CBR1	H'2000 0000	Retained	Retained
Match operation setting register 1	CRR1	H'0000 2000	Retained	Retained
Match address setting register 1	CAR1	Undefined	Retained	Retained
Match address mask setting register 1	CAMR1	Undefined	Retained	Retained
Match data setting register 1	CDR1	Undefined	Retained	Retained
Match data mask setting register 1	CDMR1	Undefined	Retained	Retained
Execution count break register 1	CETR1	Undefined	Retained	Retained
Channel match flag register	CCMFR	H'0000 0000	Retained	Retained
Break control register	CBCR	H'0000 0000	Retained	Retained

The access size must be the same as the control register size. If the size is different, the register is not written to if attempted, and reading the register returns the undefined value. A desired break may not occur between the time when the instruction for rewriting the control register is executed and the time when the written value is actually reflected on the register. In order to confirm the exact timing when the control register is updated, read the data, which has been written most recently. The subsequent instructions are valid for the most recently written register value.

59.2.1 Match Condition Setting Registers 0 and 1 (CBR0 and CBR1)

CBR0 and CBR1 are readable/writable 32-bit registers which specify the break conditions for channels 0 and 1, respectively. The following break conditions can be set in the CBR0 and CBR1: (1) whether or not to include the match flag in the conditions, (2) whether or not to include the ASID, and the ASID value when included, (3) whether or not to include the data value, (4) operand size, (5) whether or not to include the execution count, (6) bus type, (7) instruction fetch cycle or operand access cycle, and (8) read or write access cycle.

- CBR0

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MFE	AIE	MFI						AIV							
Initial value:	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	SZ			—	—	—	—	CD		ID		—	RW		CE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W

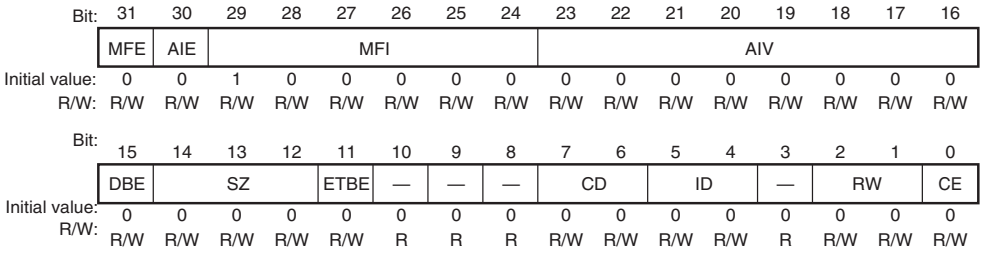
Bit	Bit Name	Initial Value	R/W	Description
31	MFE	0	R/W	Match Flag Enable Specifies whether or not to include the match flag value specified by the MFI bit of this register in the match conditions. When the specified match flag value is 1, the condition is determined to be satisfied. 0: The match flag is not included in the match conditions; thus, not checked. 1: The match flag is included in the match conditions.
30	AIE	0	R/W	ASID Enable Specifies whether or not to include the ASID specified by the AIV bit of this register in the match conditions. 0: The ASID is not included in the match conditions; thus, not checked. 1: The ASID is included in the match conditions.

Bit	Bit Name	Initial Value	R/W	Description
29 to 24	MFI	100000	R/W	Match Flag Specify Specify the match flag to be included in the match conditions. 000000: MF0 bit of the CCMFR register 000001: MF1 bit of the CCMFR register Others: Reserved (setting prohibited) Note: The initial value is the reserved value, but when 1 is written into CBR0[0], MFI must be set to 000000 or 000001. And note that the channel 0 is not hit when MFE bit of this register is 1 and MFI bits are 000000 in the condition of CCRMF.MF0 = 0.
23 to 16	AIV	All 0	R/W	ASID Specify Specify the ASID value to be included in the match conditions.
15	—	0	R	Reserved For read/write in this bit, refer to General Precautions on Handling of Product.
14 to 12	SZ	All 0	R/W	Operand Size Select Specify the operand size to be included in the match conditions. This bit is valid only when the operand access cycle is specified as a match condition. 000: The operand size is not included in the match conditions; thus, not checked (any operand size specifies the match condition).* 001: Byte access 010: Word access 011: Longword access Others: Reserved (setting prohibited)
11 to 8	—	All 0	R	Reserved For read/write in these bits, refer to General Precautions on Handling of Product.

Bit	Bit Name	Initial Value	R/W	Description
7, 6	CD	All 0	R/W	Bus Select Specify the bus to be included in the match conditions. This bit is valid only when the operand access cycle is specified as a match condition. 00: Operand bus for operand access 01: X bus for operand access 10: Y bus for operand access 11: Reserved (setting prohibited)
5, 4	ID	All 0	R/W	Instruction Fetch/Operand Access Select Specify the instruction fetch cycle or operand access cycle as the match condition. 00: Instruction fetch cycle or operand access cycle 01: Instruction fetch cycle 10: Operand access cycle 11: Instruction fetch cycle or operand access cycle
3	—	0	R	Reserved For read/write in this bit, refer to General Precautions on Handling of Product.
2, 1	RW	All 0	R/W	Bus Command Select Specify the read/write cycle as the match condition. This bit is valid only when the operand access cycle is specified as a match condition. 00: Read cycle or write cycle 01: Read cycle 10: Write cycle 11: Read cycle or write cycle
0	CE	0	R/W	Channel Enable Validates/invalidates the channel. If this bit is 0, all the other bits of this register are invalid. 0: Invalidates the channel. 1: Validates the channel.

Note: * If the data value is included in the match conditions, be sure to specify the operand size.

- CBR1



Bit	Bit Name	Initial Value	R/W	Description
31	MFE	0	R/W	Match Flag Enable Specifies whether or not to include the match flag value specified by the MFI bit of this register in the match conditions. When the specified match flag value is 1, the condition is determined to be satisfied. 0: The match flag is not included in the match conditions; thus, not checked. 1: The match flag is included in the match conditions.
30	AIE	0	R/W	ASID Enable Specifies whether or not to include the ASID specified by the AIV bit of this register in the match conditions. 0: The ASID is not included in the match conditions; thus, not checked. 1: The ASID is included in the match conditions.
29 to 24	MFI	100000	R/W	Match Flag Specify Specify the match flag to be included in the match conditions. 000000: The MF0 bit of the CCMFR register 000001: The MF1 bit of the CCMFR register Others: Reserved (setting prohibited) Note: The initial value is the reserved value, but when 1 is written into CBR1[0], MFI must be set to 000000 or 000001. And note that the channel 1 is not hit when MFE bit of this register is 1 and MFI bits are 000001 in the condition of CCRMF.MF1 = 0.

Bit	Bit Name	Initial Value	R/W	Description
23 to 16	AIV	All 0	R/W	ASID Specify Specify the ASID value to be included in the match conditions.
15	DBE	0	R/W	Data Value Enable*2 Specifies whether or not to include the data value in the match condition. This bit is valid only when the operand access cycle is specified as a match condition. 0: The data value is not included in the match conditions; thus, not checked. 1: The data value is included in the match conditions.
14 to 12	SZ	All 0	R/W	Operand Size Select Specify the operand size to be included in the match conditions. This bit is valid only when the operand access cycle is specified as a match condition. 000: The operand size is not included in the match condition; thus, not checked (any operand size specifies the match condition).*1 001: Byte access 010: Word access 011: Longword access Others: Reserved (setting prohibited)
11	ETBE	0	R/W	Execution Count Value Enable Specifies whether or not to include the execution count value in the match conditions. If this bit is 1 and the match condition satisfaction count matches the value specified by the CETR1 register, the operation specified by the CRR1 register is performed. 0: The execution count value is not included in the match conditions; thus, not checked. 1: The execution count value is included in the match conditions.
10 to 8	—	All 0	R	Reserved For read/write in these bits, refer to General Precautions on Handling of Product.

Bit	Bit Name	Initial Value	R/W	Description
7, 6	CD	All 0	R/W	Bus Select Specify the bus to be included in the match conditions. This bit is valid only when the operand access cycle is specified as a match condition. 00: Operand bus for operand access 01: X bus for operand access 10: Y bus for operand access 11: Reserved (setting prohibited)
5, 4	ID	All 0	R/W	Instruction Fetch/Operand Access Select Specify the instruction fetch cycle or operand access cycle as the match condition. 00: Instruction fetch cycle or operand access cycle 01: Instruction fetch cycle 10: Operand access cycle 11: Instruction fetch cycle or operand access cycle
3	—	0	R	Reserved For read/write in this bit, refer to General Precautions on Handling of Product.
2, 1	RW	All 0	R/W	Bus Command Select Specify the read/write cycle as the match condition. This bit is valid only when the operand access cycle is specified as a match condition. 00: Read cycle or write cycle 01: Read cycle 10: Write cycle 11: Read cycle or write cycle
0	CE	0	R/W	Channel Enable Validates/invalidates the channel. If this bit is 0, all the other bits in this register are invalid. 0: Invalidates the channel. 1: Validates the channel.

Notes: 1. If the data value is included in the match conditions, be sure to specify the operand size.

2. The OCBI instruction is handled as longword write access without the data value, and the PREF, OCBP, and OCBWB instructions are handled as longword read access without the data value. Therefore, do not include the data value in the match conditions for these instructions.

59.2.2 Match Operation Setting Registers 0 and 1 (CRR0 and CRR1)

CRR0 and CRR1 are readable/writable 32-bit registers which specify the operation to be executed when channels 0 and 1 satisfy the match condition, respectively. The following operations can be set in the CRR0 and CRR1 registers: (1) breaking at a desired timing for the instruction fetch cycle and (2) requesting a break.

- CRR0

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PCB	BIE
Initial value:	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All 0	R	Reserved For read/write in these bits, refer to General Precautions on Handling of Product.
13	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
12 to 2	—	All 0	R	Reserved For read/write in these bits, refer to General Precautions on Handling of Product.
1	PCB	0	R/W	PC Break Select Specifies either before or after instruction execution as the break timing for the instruction fetch cycle. This bit is invalid for breaks other than the ones for the instruction fetch cycle. 0: Sets the PC break before instruction execution. 1: Sets the PC break after instruction execution.
0	BIE	0	R/W	Break Enable Specifies whether or not to request a break when the match condition is satisfied for the channel. 0: Does not request a break. 1: Requests a break.

- CRR1

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

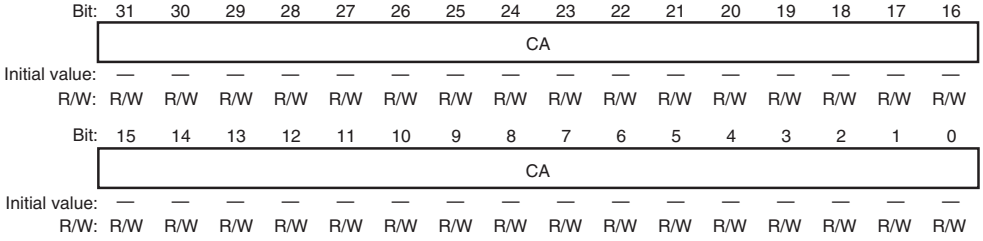
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PCB	BIE
Initial value:	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All 0	R	Reserved For read/write in these bits, refer to General Precautions on Handling of Product.
13	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
12 to 2	—	All 0	R	Reserved For read/write in these bits, refer to General Precautions on Handling of Product.
1	PCB	0	R/W	PC Break Select Specifies either before or after instruction execution as the break timing for the instruction fetch cycle. This bit is invalid for breaks other than ones for the instruction fetch cycle. 0: Sets the PC break before instruction execution. 1: Sets the PC break after instruction execution.
0	BIE	0	R/W	Break Enable Specifies whether or not to request a break when the match condition is satisfied for the channel. 0: Does not request a break. 1: Requests a break.

59.2.3 Match Address Setting Registers 0 and 1 (CAR0 and CAR1)

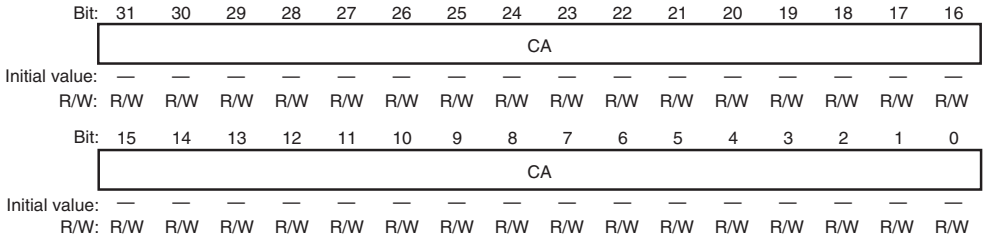
CAR0 and CAR1 are readable/writable 32-bit registers specifying the virtual address to be included in the break conditions for channels 0 and 1, respectively. One of three address buses to be included in the break condition is selected by the CD bit of the match condition setting registers (CBR0 and CBR1).

- CAR0



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	CA	Undefined	R/W	Compare Address Specify the address to be included in the break conditions. When the operand bus has been specified using the CBR0 register, specify the SAB address in CA[31:0]. When the X bus has been specified using the CBR0 register, specify the values of XAB15 to XAB1 in CA[31:17]. In this case, any values are specified in CA[16:0]. When the Y bus has been specified using the CBR0 register, specify the values of YAB15 to YAB1 in CA[15:1]. In this case, any values are specified in CA[31:16] and CA[0].

- CAR1



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	CA	Undefined	R/W	Compare Address Specify the address to be included in the break conditions. When the operand bus has been specified using the CBR1 register, specify the SAB address in CA[31:0]. When the X bus has been specified using the CBR1 register, specify the values of XAB15 to XAB1 in CA[31:17]. In this case, any values are specified in CA[16:0]. When the Y bus has been specified using the CBR1 register, specify the values of YAB15 to YAB1 in CA[15:1]. In this case, any values are specified in CA[31:16] and CA[0].

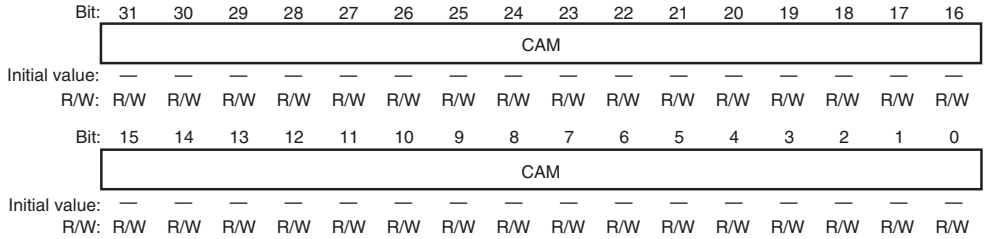
Table 59.3 Settings for Match Address Setting Register

Bus Selected Using CBR0, CBR1	CA[31:17]	CA[16]	CA[15:1]	CA[0]
Operand bus	SAB31 to SAB17	SAB16	SAB15 to SAB1	SAB0
X bus	XAB15 to XAB1	Don't care	Don't care	Don't care
Y bus	Don't care	Don't care	YAB15 to YAB1	Don't care

59.2.4 Match Address Mask Setting Registers 0 and 1 (CAMR0 and CAMR1)

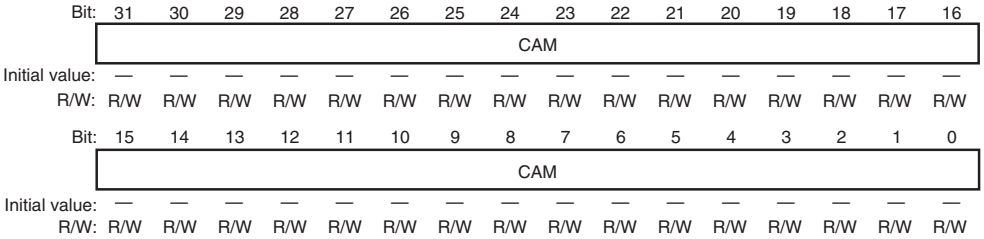
CMAR0 and CMAR1 are readable/writable 32-bit registers which specify the bits to be masked among the address bits specified by using the match address setting register of the corresponding channel. (Set the bits to be masked to 1.)

- CAMR0



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	CAM	Undefined	R/W	Compare Address Mask Specify the bits to be masked among the address bits, which are specified using the CAR0 register. (Set the bits to be masked to 1.) 0: Address bits CA[n] are included in the break condition. 1: Address bits CA[n] are masked and not included in the break condition. [n] = any values from 31 to 0

- CAMR1



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	CAM	Undefined	R/W	Compare Address Mask Specify the bits to be masked among the address bits, which are specified using the CAR1 register. (Set the bits to be masked to 1.) 0: Address bits CA[n] are included in the break condition. 1: Address bits CA[n] are masked and not included in the break condition. [n] = any values from 31 to 0

59.2.5 Match Data Setting Register 1 (CDR1)

CDR1 is a readable/writable 32-bit register which specifies the data value to be included in the break conditions for channel 1. One of three address buses to be included in the break condition is selected by the CD bit of the match condition setting register (CBR1).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CD															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CD															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	CD	Undefined	R/W	Compare Data Value Specify the data value to be included in the break conditions. When the operand bus has been specified using the CBR1 register, specify the SDB data value in CD[31:0]. When the X bus has been specified using the CBR1 register, specify the values of XDB15 to XDB0 in CD[31:16]. In this case, any values are specified in CD[15:0]. When the Y bus has been specified using the CBR1 register, specify the values of YDB15 to YDB0 in CD[15:0]. In this case, any values are specified in CD[31:16].

Table 59.4 Settings for Match Data Setting Register

Bus and Size Selected Using CBR1	CD[31:24]	CD[23:16]	CD[15:8]	CD[7:0]
Operand bus (byte)	Don't care	Don't care	Don't care	SDB7 to SDB0
Operand bus (word)	Don't care	Don't care	SDB15 to SDB8	SDB7 to SDB0
Operand bus (longword)	SDB31 to SDB24	SDB23 to SDB16	SDB15 to SDB8	SDB7 to SDB0
X bus (word)	XDB15 to XDB8	XDB7 to XDB0	Don't care	Don't care
X bus (longword)	XDB31 to XDB24	XDB23 to XDB16	XDB15 to XDB8	XDB7 to XDB0
Y bus (word)	Don't care	Don't care	YDB15 to YDB8	YDB7 to YDB0
Y bus (longword)	YDB31 to YDB24	YDB23 to YDB16	YDB15 to YDB8	YDB7 to YDB0

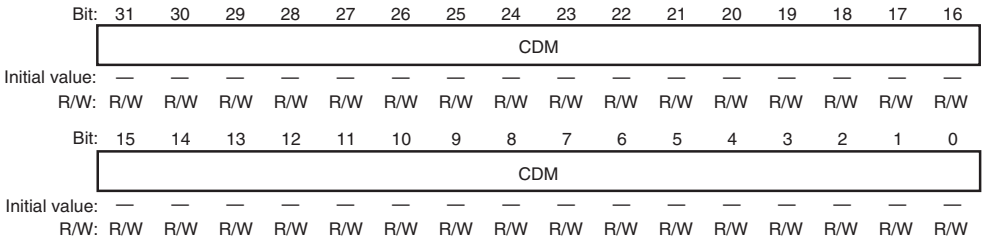
Notes: 1. If the data value is included in the match conditions, be sure to specify the operand size.

2. The OCBI instruction is handled as longword write access without the data value, and the PREF, OCBP, and OCBWB instructions are handled as longword read access without the data value. Therefore, do not include the data value in the match conditions for these instructions.

3. When the data value is included as the match condition on the operand bus for instructions MOVS.W @-As,Ds, MOVS.W @As,Ds, MOVS.W @As+,Ds, and MOVS.W @As+Ix,Ds, be sure to set the data in CD[15:0].

59.2.6 Match Data Mask Setting Register 1 (CDMR1)

CDMR1 is a readable/writable 32-bit register which specifies the bits to be masked among the data value bits specified using the match data setting register. (Set the bits to be masked to 1.)



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	CDM	Undefined	R/W	Compare Data Value Mask Specify the bits to be masked among the data value bits specified using the CDR1 register. (Set the bits to be masked to 1.) 0: Data value bits CD[n] are included in the break condition. 1: Data value bits CD[n] are masked and not included in the break condition. [n] = any values from 31 to 0

59.2.7 Execution Count Break Register 1 (CETR1)

CETR1 is a readable/writable 32-bit register which specifies the number of the channel hits before a break occurs. A maximum value of $2^{12} - 1$ can be specified. When the execution count value is included in the match conditions by using the match condition setting register, the value of this register is decremented by one every time the channel is hit. When the channel is hit after the register value reaches H'001, a break occurs.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	CET											
Initial value:	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved For read/write in these bits, refer to General Precautions on Handling of Product.
11 to 0	CET	Undefined	R/W	Execution Count Specify the execution count to be included in the break conditions.

59.2.8 Channel Match Flag Register (CCMFR)

CCMFR is a readable/writable 32-bit register, which indicates whether or not the match conditions have been satisfied for each channel. When a channel match condition has been satisfied, the corresponding flag bit is set to 1. To clear the flags, write the data containing value 0 for the bits to be cleared and value 1 for the other bits to this register. (The logical AND between the value which has been written and the current register value is actually written to the register.) Sequential operation using multiple channels is available by using these match flags.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MF1	MF0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved For read/write in these bits, refer to General Precautions on Handling of Product.
1	MF1	0	R/W	Channel 1 Condition Match Flag This flag is set to 1 when the channel 1 match condition has been satisfied. To clear the flag, write 0 to this bit. 0: Channel 1 match condition has not been satisfied. 1: Channel 1 match condition has been satisfied.
0	MF0	0	R/W	Channel 0 Condition Match Flag This flag is set to 1 when the channel 0 match condition has been satisfied. To clear the flag, write 0 to this bit. 0: Channel 0 match condition has not been satisfied. 1: Channel 0 match condition has been satisfied.

59.2.9 Break Control Register (CBCR)

CBCR is a readable/writable 32-bit register, which specifies whether or not to use the user break debugging support function. For details on the user break debugging support function, refer to section 59.4, User Break Debugging Support Function.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	UBDE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved For read/write in these bits, refer to General Precautions on Handling of Product.
0	UBDE	0	R/W	User Break Debugging Support Function Enable Specifies whether or not to use the user break debugging support function. 0: Does not use the user break debugging support function. 1: Uses the user break debugging support function.

59.3 Operation Description

59.3.1 Definition of Words Related to Accesses

"Instruction fetch" refers to an access in which an instruction is fetched. For example, fetching the instruction located at the branch destination after executing a branch instruction is an instruction access. "Operand access" refers to any memory access accompanying execution of an instruction. For example, accessing an address (PC + disp × 2 + 4) in the instruction MOV.W@(disp,PC),Rn is an operand access. "Data" is used in contrast to "address".

All types of operand access are classified into read or write access. Special care must be taken in using the following instructions.

- PREF, OCBP, and OCBWB: Instructions for a read access
- MOVCA.L and OCBI: Instructions for a write access
- TAS.B: Instruction for a single read access or a single write access

The operand access accompanying the PREF, OCBP, OCBWB, and OCBI instructions is access without the data value; therefore, do not include the data value in the match conditions for these instructions.

The operand size should be defined for all types of operand access. Available operand sizes are byte, word, and longword. For operand access accompanying the PREF, OCBP, OCBWB, MOVCA.L, and OCBI instructions, the operand size is defined as longword.

59.3.2 User Break Operation Sequence

The following describes the sequence from when the break condition is set until the user break exception handling is initiated.

1. Specify the operand size, bus, instruction fetch/operand access, and read/write as the match conditions using the match condition setting register (CBR0 or CBR1). Specify the break address using the match address setting register (CAR0 or CAR1), and specify the address mask condition using the match address mask setting register (CAMR0 or CAMR1). To include the ASID in the match conditions, set the AIE bit in the match condition setting register and specify the ASID value by the AIV bit in the same register. To include the data value in the match conditions, set the DBE bit in the match condition setting register; specify the break data using the match data setting register (CDR1); and specify the data mask condition using the match data mask setting register (CDMR1). To include the execution count in the match conditions, set the ETBE bit of the match condition setting register; and specify the execution count using the execution count break register (CETR1). To use the sequential break, set the MFE bit of the match condition setting register; and specify the number of the first channel using the MFI bit.
2. Specify whether or not to request a break when the match condition is satisfied and the break timing when the match condition is satisfied as a result of fetching the instruction using the match operation setting register (CRR0 or CRR1). After having set all the bits in the match condition setting register except the CE bit and the other necessary registers, set the CE bit and read the match condition setting register again. This ensures that the set values in the control registers are valid for the subsequent instructions immediately after reading the register. Setting the CE bit of the match condition setting register in the initial state after reset via the control registers may cause an undesired break.
3. When the match condition has been satisfied, the corresponding condition match flag (MF1 or MF0) in the channel match flag register (CCMFR) is set. A break is also requested to the CPU according to the set values in the match operation setting register (CRR0 or CRR1). The CPU operates differently according to the BL bit value of the SR register: when the BL bit is 0, the CPU accepts the break request and executes the specified exception handling; and when the BL bit is 1, the CPU does not execute the exception handling.
4. The match flags (MF1 and MF0) can be used to confirm whether or not the corresponding match condition has been satisfied. Although the flag is set when the condition is satisfied, it is not cleared automatically; therefore, write 0 to the flag bit by issuing a memory store instruction to the channel match flag register (CCMFR) in order to use the flag again.
5. Breaks may occur virtually at the same time for channels 0 and 1. In this case, only one break request is sent to the CPU; however, the two condition match flags corresponding to these breaks may be set.

6. While the BL bit in the SR register is 1, no break requests are accepted. However, whether or not the condition has been satisfied is determined. When the condition is determined to be satisfied, the corresponding condition match flag is set.
7. If the sequential break conditions are set, the condition match flag is set every time the match conditions are satisfied for each channel. When the conditions have been satisfied for the first channel in the sequence but not for the second channel in the sequence, clear the condition match flag for the first channel in the sequence in order to release the first channel in the sequence from the match state.

59.3.3 Instruction Fetch Cycle Break

1. If the instruction fetch cycle is set in the match condition setting register (CBR0 or CBR1), the instruction fetch cycle is handled as a match condition. To request a break upon satisfying the match condition, set the BIE bit in the match operation setting register (CRR0 or CRR1) of the corresponding channel. Either before or after executing the instruction can be selected as the break timing according to the PCB bit value. If the instruction fetch cycle is specified as a match condition, be sure to clear the LSB to 0 in the match address setting register (CAR0 or CAR1); otherwise, no break occurs.
2. If pre-instruction-execution break is specified for the instruction fetch cycle, the break is requested when the instruction is fetched and determined to be executed. Therefore, this function cannot be used for the instructions, which are fetched through overrun (i.e., the instructions fetched during branching or making transition to the interrupt routine but not executed). For priorities of pre-instruction-execution break and the other exceptions, refer to the SH4AL-DSP Software Manual. If pre-instruction-execution break is specified for the delayed slot of the delayed branch instruction, the break is requested before the delayed branch instruction is executed. However, do not specify pre-instruction-execution break for the delayed slot of the RTE instruction.
3. If post-instruction-execution break is specified for the instruction fetch cycle, the break is requested after the instruction which satisfied the match condition has been executed and before the next instruction is executed. Similar to pre-instruction-execution break, this function cannot be used for the instructions, which are fetched through overrun. For priorities of post-instruction-execution break and the other exceptions, refer to the SH4AL-DSP Software Manual. If post-instruction-execution break is specified for the delayed branch instruction and its delayed slot, the break does not occur until the first instruction at the branch destination.
4. If the instruction fetch cycle is specified as the channel 1 match condition, the DBE bit of match condition setting register CBR1 becomes invalid, the settings of match data setting register CDR1 and match data mask setting register CDMR1 are ignored. Therefore, the data value cannot be specified for the instruction fetch cycle break.

59.3.4 Operand Access Cycle Break

1. Table 59.5 shows the relation between the operand sizes specified using the match condition setting register (CBR0 or CBR1) and the address bits to be compared for the operand access cycle break.

Table 59.5 Relation between Operand Sizes and Address Bits to be Compared

Selected Operand Size	Address Bits to be Compared
Longword	Address bits A31 to A2
Word	Address bits A31 to A1
Byte	Address bits A31 to A0
Operand size is not included in the match conditions	Address bits A31 to A2 for longword access Address bits A31 to A1 for word access Address bits A31 to A0 for byte access

The above table means that if address H'0000 1003 is set in the match address setting register (CAR0 or CAR1), for example, the match condition is satisfied for the following access cycles (assuming that all the other conditions are satisfied):

— Longword access to address H'0000 1000
— Word access to address H'0000 1002
— Byte access to address H'0000 1003

2. When the data value is included in the channel 1 match conditions:
   If the data value is included in the match conditions, be sure to select the longword, word, or byte as the operand size using the operand size select bit (SZ) of the match condition setting register (CBR1), and also set the match data setting register (CDR1) and the match data mask setting register (CDMR1). With these settings, the match condition is satisfied when both of the address and data conditions are satisfied. The data value and mask control for byte access, word access, and longword access should be set in bits 7 to 0, 15 to 0, and 31 to 0 in the bits CDR1 and CDMR1, respectively. When the data value is included as the break condition for instructions MOVS.W @-As,Ds, MOVS.W @As,Ds, MOVS.W @As+,Ds, and MOVS.W @As+lx,Ds, be sure to set the data value and mask in the bits 15 to 0 of CDR1 and CDMR1.
3. The operand access accompanying the PREF, OCBP, OCBWB, and OCBI instructions are access without the data value; therefore, if the data value is included in the match conditions for these instructions, the match conditions will never be satisfied.

4. If the operand bus is selected, a break occurs after executing the instruction which has satisfied the conditions and immediately before executing the next instruction. However, if the data value is included in the match conditions, a break may occur after executing several instructions after the instruction which has satisfied the conditions; therefore, it is impossible to identify the instruction causing the break. If such a break has occurred for the delayed branch instruction or its delayed slot, the break does not occur until the first instruction at the branch destination.

   However, do not specify the operand break for the delayed slot of the RTE instruction. And if the data value is included in the match conditions, it is not allowed to set the break for the preceding the RTE instruction by one to six instructions.

59.3.5 X Memory or Y Memory Bus Cycle Break

1. The X memory or Y memory can be selected by using the bus select bit (CD bit) of the match condition setting register (CBR0 or CBR1). Both X memory and Y memory cannot be included at the same time in one channel much condition. When the X bus or Y bus/ operand access/read or write/word or longword are set in the match condition, the memory access of X bus or Y bus is treated as the match condition.
2. To specify the X memory address as the match condition, set the X memory address and mask in the upper 16-bit of the match address setting register (CAR0 or CAR1) and the match address mask setting register (CAMR0 or CAMR1). To specify the Y memory address as the match condition, set the Y memory address and mask in the lower 16-bit of the match address setting register (CAR0 or CAR1) and the match address mask setting register (CAMR0 or CAMR1). When the data value is included as the channel 1 match condition, the data value of the X bus is set in the upper 16-bit of the match data setting register (CDR1) and match data mask setting register (CDMR1); and the data value of Y bus is set in the lower 16-bit of those registers for word access. For longword access, 32-bit data value of the X or Y bus and mask are set in CDR1 and CDMR1.
3. The operand access break of the X or Y memory bus is occurred at the same timing as that of the operand bus. For details, see section 59.3.4, Operand Access Cycle Break.

59.3.6 Sequential Break

1. Sequential break conditions can be specified by setting the MFE and MFI bits in the match condition setting registers (CBR0 and CBR1). (Sequential break involves two cases such that channel 0 break condition is satisfied then channel 1 break condition is satisfied, and vice versa.) To use the sequential break function, clear the MFE bit of the match condition setting register and the BIE bit of the match operation setting register of the first channel in the sequence, and set the MFE bit and specify the number of the second channel in the sequence using the MFI bit in the match condition setting register of the second channel in the sequence. If the sequential break condition is set, the condition match flag is set every time the match condition is satisfied for each channel. When the condition has been satisfied for the first channel in the sequence but not for the second channel in the sequence, clear the condition match flag for the first channel in the sequence in order to release the first channel in the sequence from the match state.
2. As the sequential break conditions, the operand bus, X bus, or Y bus can be specified for the first and second channels in the sequence; the execution count break condition can also be specified for channel 1.
3. If the match conditions for the first and second channels in the sequence are satisfied within a significantly short time, sequential operation may not be guaranteed in some cases, as shown below.

- When the Match Condition is Satisfied at the Instruction Fetch Cycle for Both the First and Second Channels in the Sequence:

Instruction B is 0 instruction after instruction A	Equivalent to setting the same addresses; do not use this setting.
Instruction B is one instruction after instruction A	Sequential operation is not guaranteed.
Instruction B is two or more instructions after instruction A	Sequential operation is guaranteed.

- When the match condition is satisfied at the instruction fetch cycle for the first channel in the sequence whereas the match condition is satisfied at the operand access cycle for the second channel in the sequence:

Instruction B is 0 or one instruction after instruction A	Sequential operation is not guaranteed.
Instruction B is two or more instructions after instruction A	Sequential operation is guaranteed.

- When the match condition is satisfied at the operand access cycle for the first channel in the sequence whereas the match condition is satisfied at the instruction fetch cycle for the second channel in the sequence:

Instruction B is 0 to five instructions after instruction A	Sequential operation is not guaranteed.
Instruction B is six or more instructions after instruction A	Sequential operation is guaranteed.

- When the match condition is satisfied at the operand access cycle for both the first and second channels in the sequence:

Instruction B is 0 to five instructions after instruction A	Sequential operation is not guaranteed.
Instruction B is six or more instructions after instruction A	Sequential operation is guaranteed.

59.3.7 Program Counter Value to be Saved

When a break has occurred, the address of the instruction to be executed when the program restarts is saved in the SPC then the exception handling state is initiated. A unique instruction causing a break can be identified unless the data value is included in the match conditions.

- When the instruction fetch cycle (before instruction execution) is specified as the match condition:

  The address of the instruction which has satisfied the match conditions is saved in the SPC. The instruction which has satisfied the match conditions is not executed, but a break occurs instead. However, if the match conditions are satisfied for the delayed slot instruction, the address of the delayed branch instruction is saved in the SPC.
- When the instruction fetch cycle (after instruction execution) is specified as the match condition:

  The address of the instruction immediately after the instruction which has satisfied the match conditions is saved in the SPC. The instruction which has satisfied the match conditions is executed, then a break occurs before the next instruction. If the match conditions are satisfied for the delayed branch instruction or its delayed slot, these instructions are executed and the address of the branch destination is saved in the SPC.
- When the operand access (address only) is specified as the match condition:

  The address of the instruction immediately after the instruction which has satisfied the break conditions is saved in the SPC. The instruction which has satisfied the match conditions are executed, then a break occurs before the next instruction. However, if the conditions are satisfied for the delayed slot, the address of the branch destination is saved in the SPC.
- When the operand access (address and data) is specified as the match condition:

  If the data value is added to the match conditions, the instruction which has satisfied the match conditions is executed. A user break occurs before executing an instruction that is one through six instructions after the instruction which has satisfied the match conditions. The address of the instruction is saved in the SPC; thus, it is impossible to identify exactly where a break will occur. If the conditions are satisfied for the delayed slot instruction, the address of the branch destination is saved in the SPC. If a branch instruction follows the instruction which has satisfied the match conditions, a break may occur after the delayed instruction and delayed slot are executed. In this case, the address of the branch destination is also saved in the SPC.

59.4 User Break Debugging Support Function

By using the user break debugging support function, the branch destination address can be modified when the CPU accepts the user break request. Specifically, setting the UBDE bit of break control register CBCR to 1 allows branching to the address indicated by DBR instead of branching to the address indicated by the [VBR + offset]. Figure 59.2 shows the flowchart of the user break debugging support function.

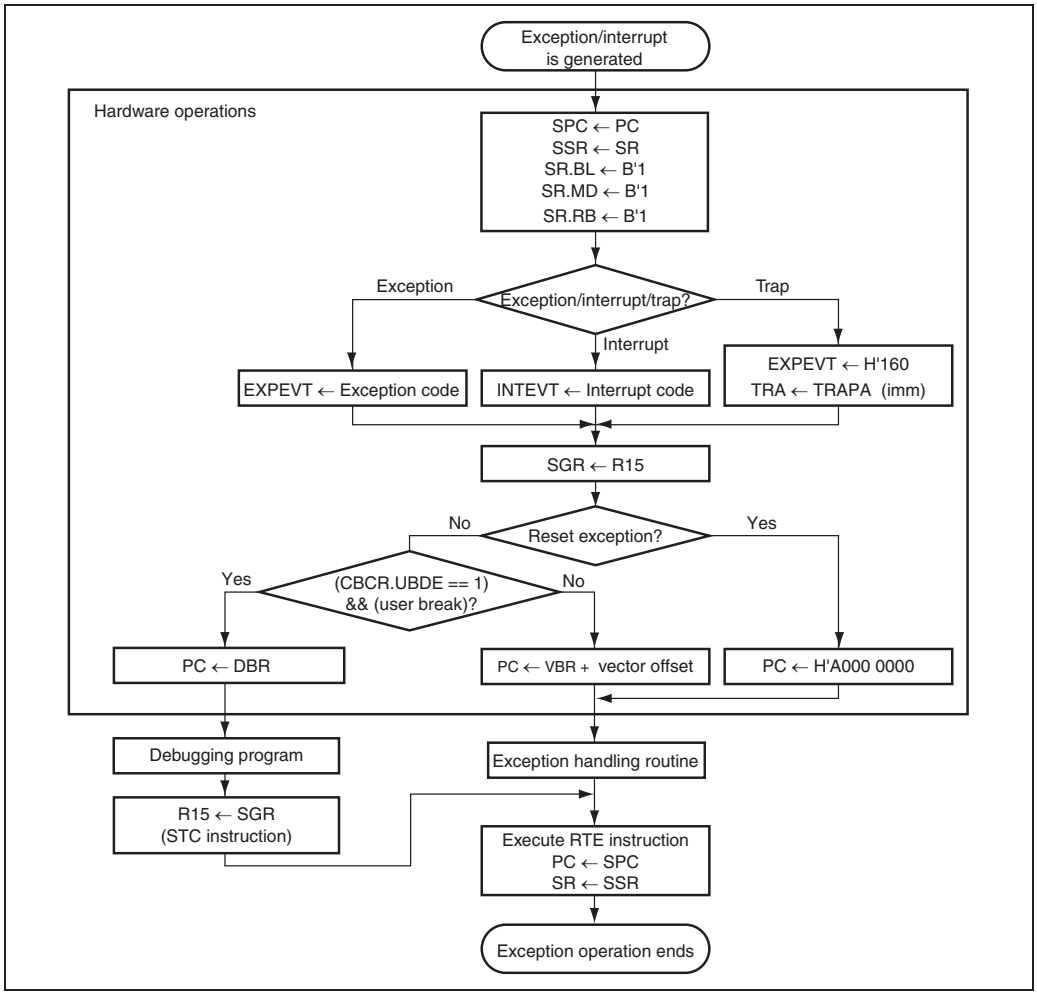


Figure 59.2 Flowchart of User Break Debugging Support Function

59.5 User Break Examples

(1) Match Conditions are Specified for an Instruction Fetch Cycle

- Example 1-1

  Register settings: CBR0 = H'00000013 / CRR0 = H'00002003 / CAR0 = H'00000404 / CAMR0 = H'00000000 / CBR1 = H'00000013 / CRR1 = H'00020001 / CAR1 = H'00008010 / CAMR1 = H'00000006 / CDR1 = H'00000000 / CDMR1 = H'00000000 / CETR1 = H'00000000 / CBCR = H'00000000

  Specified conditions: Independent for channels 0 and 1

  — Channel 0

  Address: H'00000404 / Address mask: H'00000000

  Bus cycle: Instruction fetch (after executing the instruction)

  ASID is not included in the conditions.

  — Channel 1:

  Address: H'00008010 / Address mask: H'00000006

  Data: H'00000000 / Data mask: H'00000000 / Execution count: H'00000000

  Bus cycle: Instruction fetch (before executing instruction)

  ASID, data values, and execution count are not included in the conditions.

  With the above settings, the user break occurs after executing the instruction at address H'00000404 or before executing the instruction at address H'00008010 to H'00008016.

- Example 1-2

  Register settings: CBR0 = H'40800013 / CRR0 = H'00002000 / CAR0 = H'00037226 / CAMR0 = H'00000000 / CBR1 = H'C0700013 / CRR1 = H'00002001 / CAR1 = H'0003722E / CAMR1 = H'00000000 / CDR1 = H'00000000 / CDMR1 = H'00000000 / CETR1 = H'00000000 / CBCR = H'00000000

  Specified conditions: Channel 0 → Channel1 sequential mode

  — Channel 0

  Address: H'00037226 / Address mask: H'00000000 / ASID: H'80

  Bus cycle: Instruction fetch (before executing the instruction)

— Channel 1

Address: H'0003722E / Address mask: H'00000000 / ASID: H'70

Data: H'00000000 / Data mask: H'00000000 / Execution count: H'00000000

Bus cycle: Instruction fetch (before executing the instruction)

Data values and execution count are not included in the conditions.

With the above settings, the user break occurs after executing the instruction at address H'00037226 where ASID is H'80 before executing the instruction at address H'0003722E where ASID is H'70.

- Example 1-3

  Register settings: CBR0 = H'00000013 / CRR0 = H'00002001 / CAR0 = H'00027128 / CAMR0 = H'00000000 / CBR1 = H'00000013 / CRR1 = H'00002001 / CAR1 = H'00031415 / CAMR1 = H'00000000 / CDR1 = H'00000000 / CDMR1 = H'00000000 / CETR1 = H'00000000 / CBCR = H'00000000

  Specified conditions: Independent for channels 0 and 1

  — Channel 0

  Address: H'00027128 / Address mask: H'00000000

  Bus cycle: Instruction fetch (before executing the instruction)

  ASID is not included in the conditions.

  — Channel 1

  Address: H'00031415 / Address mask: H'00000000

  Data: H'00000000 / Data mask: H'00000000 / Execution count: H'00000000

  Bus cycle: Instruction fetch (before executing the instruction)

  ASID, data values, and execution count are not included in the conditions.

  With the above settings, the user break occurs for channel 0 before executing the instruction at address H'00027128. No user break occurs for channel 1 since the instruction fetch is executed only at even addresses.

- Example 1-4

  Register settings: CBR0 = H'40800013 / CRR0 = H'00002000 / CAR0 = H'00037226 / CAMR0 = H'00000000 / CBR1 = H'C0700013 / CRR1 = H'00002001 / CAR1 = H'0003722E / CAMR1 = H'00000000 / CDR1 = H'00000000 / CDMR1 = H'00000000 / CETR1 = H'00000000 / CBCR = H'00000000

  Specified conditions: Channel 0 → Channel 1 sequential mode

  — Channel 0

    Address: H'00037226 / Address mask: H'00000000 / ASID: H'80

    Bus cycle: Instruction fetch (before executing the instruction)

  — Channel 1

    Address: H'0003722E / Address mask: H'00000000 / ASID: H'70

    Data: H'00000000 / Data mask: H'00000000 / Execution count: H'00000000

    Bus cycle: Instruction fetch (before executing the instruction)

    Data values and execution count are not included in the conditions.

  With the above settings, the user break occurs after executing the instruction at address H'00037226 where ASID is H'80 and before executing the instruction at address H'0003722E where ASID is H'70.

- Example 1-5

  Register settings: CBR0 = H'00000013 / CRR0 = H'00002001 / CAR0 = H'00000500 / CAMR0 = H'00000000 / CBR1 = H'00000813 / CRR1 = H'00002001 / CAR1 = H'00001000 / CAMR1 = H'00000000 / CDR1 = H'00000000 / CDMR1 = H'00000000 / CETR1 = H'00000005 / CBCR = H'00000000

  Specified conditions: Independent for channels 0 and 1

  — Channel 0

    Address: H'00000500 / Address mask: H'00000000

    Bus cycle: Instruction fetch (before executing the instruction)

    ASID is not included in the conditions.

  — Channel 1

    Address: H'00001000 / Address mask: H'00000000

    Data: H'00000000 / Data mask: H'00000000 / Execution count: H'00000005

    Bus cycle: Instruction fetch (before executing the instruction)

    Execution count: 5

    ASID and data values are not included in the conditions.

With the above settings, the user break occurs for channel 0 before executing the instruction at address H'00000500. The user break occurs for channel 1 after executing the instruction at address H'00001000 four times; before executing the instruction five times.

- Example 1-6

  Register settings: CBR0 = H'40800013 / CRR0 = H'00002003 / CAR0 = H'00008404 / CAMR0 = H'00000FFF / CBR1 = H'40700013 / CRR1 = H'00002001 / CAR1 = H'00008010 / CAMR1 = H'00000006 / CDR1 = H'00000000 / CDMR1 = H'00000000 / CETR1 = H'00000000 / CBCR = H'00000000

  Specified conditions: Independent for channels 0 and 1

  — Channel 0

  Address: H'00008404 / Address mask: H'00000FFF / ASID: H'80

  Bus cycle: Instruction fetch (after executing the instruction)

  — Channel 1

  Address: H'00008010 / Address mask: H'00000006 / ASID: H'70

  Data: H'00000000 / Data mask: H'00000000 / Execution count: H'00000000

  Bus cycle: Instruction fetch (before executing the instruction)

  Data values and execution count are not included in the conditions.

  With the above settings, the user break occurs after executing the instruction at address H'00008000 to H'00008FFE where ASID is H'80 or before executing the instruction at address H'00008010 to H'00008016 where ASID is H'70.

(2) Match Conditions are Specified for an Operand Access Cycle

- Example 2-1

  Register settings: CBR0 = H'40800023 / CRR0 = H'00002001 / CAR0 = H'00123456 / CAMR0 = H'00000000 / CBR1 = H'4070A025 / CRR1 = H'00002001 / CAR1 = H'000ABCDE / CAMR1 = H'000000FF / CDR1 = H'0000A512 / CDMR1 = H'00000000 / CETR1 = H'00000000 / CBCR = H'00000000

  Specified conditions: Independent for channels 0 and 1

  — Channel 0

  Address: H'00123456 / Address mask: H'00000000 / ASID: H'80

  Bus cycle: Operand bus, operand access, and read (operand size is not included in the conditions.)

  — Channel 1

  Address: H'000ABCDE / Address mask: H'000000FF / ASID: H'70

  Data: H'0000A512 / Data mask: H'00000000 / Execution count: H'00000000

  Bus cycle: Operand bus, operand access, write, and word size

Execution count is not included in the conditions.

With these settings, the user break occurs for channel 0 for the following accesses: longword read access to address H'000123454, word read access to address H'000123456, byte read access to address H'000123456 where ASID is H'80. The user break occurs for channel 1 when word H'A512 is written to address H'000ABC00 to H'000ABCFE where ASID is H'70.

- Example 2-2

  Register settings: CBR0 = H'00002023 / CRR0 = H'00002001 / CAR0 = H'01000000 / CAMR0 = H'00000000 / CBR1 = H'0000A0A5 / CRR1 = H'00002001 / CAR1 = H'0000F000 / CAMR1 = H'FFFF0000 / CDR1 = H'00004567 / CDMR1 = H'00000000 / CETR1 = H'00000000 / CBCR = H'00000000

  Specified conditions: Independent for channels 0 and 1

  — Channel 0

  Address: H'01000000 / Address mask: H'00000000

  Bus cycle: Operand bus, operand access, read, and word size

  ASID is not included in the conditions.

  — Channel 1

  Address: H'F0000 / Address mask: H'0000

  Data: H'00004567 /Data mask: H'00000000

  Bus cycle: Y bus, operand access, write, and word size

  ASID and execution count is not included in the conditions.

  With these settings, the user break occurs for channel 0 by word read access to address H'01000000. The user break occurs for channel 1 when word H'4567 is written to the Y memory address H'F000. The X or Y memory space can be specified by the CD bit of the match condition setting register (CBR0 or CBR1).

59.6 Usage Notes

- A desired break may not occur between the time when the instruction for rewriting the UBC register is executed and the time when the written value is actually reflected on the register.

  After the UBC register is updated, execute one of the following three methods.

  A. Read the updated UBC register, and execute a branch using the RTE instruction.

     (It is not necessary that a branch using the RTE instruction is next to a reading UBC register.)

  B. Execute the ICBI instruction for any address (including non-cacheable area).

     (It is not necessary that the ICBI instruction is next to a reading UBC register.)

  C. Set 0(initial value) to IRMCR.R1 before updating the UBC register and update with following sequence.

     a. Write the UBC register.

     b. Read the UBC register which is updated at 1.

     c. Write the value which is read at 2 to the UBC register.

Note: When two or more UBC registers are updated, executing these methods at each updating the UBC registers is not necessary. At only last updating the UBC register, execute one of these methods.

- The PCB bit of the CRR0 and CRR1 registers is valid only when the instruction fetch is specified as the match condition.
- If the sequential break conditions are set, the sequential break conditions are satisfied when the conditions for the first and second channels in the sequence are satisfied in this order. Therefore, if the conditions are set so that the conditions for channels 0 and 1 should be satisfied simultaneously for the same bus cycle, the sequential break conditions will not be satisfied, causing no break.
- For the SLEEP instruction, do not allow the post-instruction-execution break where the instruction fetch cycle is the match condition. For the instructions preceding the SLEEP instruction by one to five instructions, do not allow the break where the operand access is the match condition.
- If the user break and other exceptions occur for the same instruction, they are determined according to the specified priority. For the priority, refer to the SH4AL-DSP Software Manual. If the exception having the higher priority occurs, the user break does not occur.

  — The pre-instruction-execution break is accepted prior to any other exception.

— If the post-instruction-execution break and data access break have occurred simultaneously with the re-execution type exception (including the pre-instruction-execution break) having a higher priority, only the re-execution type exception is accepted, and no condition match flags are set. When the exception handling has finished thus clearing the exception source, and when the same instruction has been executed again, the break occurs setting the corresponding flag.

— If the post-instruction-execution break or operand access break has occurred simultaneously with the completion-type exception (TRAPA) having a higher priority, then no user break occurs; however, the condition match flag is set.

- When conditions have been satisfied simultaneously and independently for channels 0 and 1, resulting in identical SPC values for both of the breaks, the user break occurs only once. However, the condition match flags are set for both channels. For example,

  Instruction at address 110 (post-instruction-execution break for instruction fetch for channel 0) → SPC = 112, CCMFR.MF0 = 1

  Instruction at address 112 (pre-instruction-execution break for instruction fetch for channel 1) → SPC = 112, CCMFR.MF1 = 1
- It is not allowed to set the pre-instruction-execution break or the operand break in the delayed slot instruction of the RTE instruction. And if the data value is included in the match conditions of the operand break, do not set the break for the preceding the RTE instruction by one to six instructions.
- If the re-execution type exception and the post-instruction-execution break are in conflict for the instruction requiring two or more execution states, then the re-execution type exception occurs. Here, the CCMFR.MF0 (or CCMFR.MF1) bit may or may not be set to 1 when the break conditions have been satisfied.
- When the DSP extended function, repeated loop, is used, even if the break instruction is matched while all or part of instructions in the repeated loop are executed, break occurrence may be retained. For details, refer to the SH4AL-DSP Software Manual.

Section 60. Debugging Specifications (DBG)

60.1 External Pins Related to Debugging

This LSI incorporates two JTAG ports. Of these, one JTAG port is assigned to dedicated JTAG pins and the other is assigned and multiplexed with the SD card pins. There are a total of 29 additional external pins for debug function: 13 (Refer Table 60.3) for control and 16 for data tracing and monitoring. These 16 external pins are also used as the VIO pins.

First, the JTAG pins are explained in Table 60.1.

Table 60.1 JTAG Pins

Pin Name	Polarity	I/O	Description
TRST_N	N	IN	Ports dedicated to JTAG
TCK SWCLKTCK（SWD）	P	IN	
TMS	P	IN	
SWDIOTMS（SWD）	P	IN/OUT （SWD）	
TDI	P	IN	
TDO SWO0(SWD)	P	OUT	
EDBGREQ（ARM） ASEBRK/BRKACK（SH）	P	IN（ARM）	During connection with the ARM-ICE, this pin functions as the external break request to the ARM. During connection with the SH-ICE, meanwhile, this pin functions as the pin break request to the SH or as the internal break state notification
	N	IN/OUT（SH）	
RTCK SWO1 (SWD)	P	OUT	Return TCK for the ARM-ICE This is not use for the ASARM function.

Assignment of the SDHI0 pins to the JTAG system is explained in Table 60.2.

Table 60.2 SDHI0 Pins

Pin Name	Polarity	I/O	Description
SDHID0_1（TCLK、SWCLKTCK：SWD）	P	IN	JTAG ports
SDHICMD0 (TRST_N)	N	IN	
SDHID0_2 (TDI)	P	IN	
SDHICLK0（TDO、SWO0：SWD）	P	OUT	
SDHID0_0（TMS、SWDIOTMS：SWD）	P	IN	
SDHICD0	—	—	Not used as the JTAG.
SDHIWP0 (EDBGREQ: ARM, ASEBRK/BRKACK: SH)	P	IN (ARM)	During connection with the ARM-ICE, this pin functions as the external break request to the ARM. During connection with the SHX2-ICE, meanwhile, this pin functions as the pin break request to the SH or as the internal break state notification.
	N	IN/OUT (SH)	
SDHID0_3（RTCK 、SWO1：SWD）	P	OUT	Return TCK for the ARM-ICE This is not use for the ASARM function.

Note: In debugging modes, debugging functions do not depend on the PORTnCR register settings and are given priority.

A list of the control pins from various external components is shown in Table 60.3.

Table 60.3 Control Pins

Pin Name	Polarity	I/O	Description
DBGMD10	P	IN	DBGMD10 pin input dedicated to debugging control
DBGMD21	P	IN	DBGMD21 pin input dedicated to debugging control
DBGMD20	P	IN	DBGMD20 pin input dedicated to debugging control
DBGMD11	P	IN	DBGMD11 pin input dedicated to debugging control
DBGMDT2	P	IN	Pin dedicated to debugging control DBGMDT2 function
DBGMDT1	P	IN	Pin dedicated to debugging control DBGMDT1 function
DBGMDT0	P	IN	Pin dedicated to debugging control DBGMDT0 function MD12 function (during a reset, but masked during a diagnosis)
TST_N	N	IN	Pin dedicated to debugging control. TST_N function 1: normal mode 0: test mode
MD7	P	IN	MD7 function
MD6	P	IN	MD6 function Pin dedicated to debugging control (for test mode) Endian selection function
MD4	P	IN	MD4 function
MD3	P	IN	MD3 function
MD2	P	IN	MD2 function

Note: Detailed descriptions on TST_N, MD7,MD6,MD4, MD3, and MD2 functions are provided in the chapter of SYSC. Refer to section 13.3.1, Operation Modes, in the chapter.

60.2 Debugging Mode

A debugging mode is a mode in which a debugging operation can be performed through an ICE that is connected to a pin capable of connecting JTAG. This LSI provides the Pin switching mode as the debugging mode:

To use DBG function, Power ON D4 area.

To use Coresight function, select the Coresight debug port by the DBGREG1 register.

Descriptions on these modes are given below.

60.2.1 Pin Switching Mode

Pin switching mode is intended to connect JTAG pins with modules to be debugged by using information about the input of external control pins. Setting the external control pins enables referring to the content of the DBGREG1 register accessible from the CPU and connecting the JTAG pins with modules to be debugged.

The value of the register is specified through pins when the register is initialized. During normal operation, it is necessary for the CPU to access the register and specify its value. Note that in order to establish a connection with JTAG, it is not necessary for software to set the register for the combinations that only require the setting of the five dedicated control pins.

Table 60.4 shows the combinations of debugging resources and their corresponding register settings. Also, Table 60.5 shows the modes that only require pin settings for determining the ICE link destinations.

Table 60.4 Combinations of Register Values and Debugging Resource in Pin Switching Mode

Register Setting（DBGREG1）						JTAG	SDHI0
MD12	MD10	MD21,20	MD11	SDJ[1:0]	DSP[2:0]		
0	0	00	—	—	—	BoundarySCAN	Normal function
		10	0	—	—	Coresight	Normal function
			1	01	—	debugging port (JTAG)	SH-X2
		11	0	—	—	SH-X2	Normal function
			1	00	—		Coresigt debugging port (SWD)
				01	—		Coresight debugging port (JTAG)
	1	10	0	—	—	Not available	Coresight debugging port (JTAG)
		11	0	—	—	Not available	SH-X2
1	0	00	1	—	—	SPU	Normal function
		01	1	—	—	Coresigt	
		10	1	00	—	debugging port (SWD)	SH-X2
	1	00	1	—	—	Not available	Coresight
		01	1	00	—	SH-X2	debugging port (SWD)

Table 60.5 List of Debugging Link Destinations that Only Require Pin Settings

Pin Setting			JTAG	SDHI0
MD12,MD10	MD21,MD20	MD11		
00	10	0	Coresigt debugging port (JTAG)	Normal function
	11	0	SH-X2	Normal function
		1		Coresight debugging port (SWD)
01	10	0	Not available	Coresight debugging port (JTAG)
	11	0	Not available	SH-X2
10	00	1	SPU	Normal function
	01	1	Coresigt debugging port (SWD)	
	10	1		SH-X2
11	00	1	Not available	Coresight debugging port (SWD)
	01	1	SH-X2	

60.2.2 Cooperative Debugging Functions

This LSI supports cooperative debugging functions that generate break trigger to a specified core when either of the SH-X2 core, AP-ARM core, or external-LSI core enters a break state. The cooperative debugging functions support the break triggers in the following four directions:

- SH-X2 → AP-ARM
- AP-ARM → SH-X2
- AP-ARM → external-LSI
- external-LSI → AP-ARM

These cooperative debugging functions are enabled by setting the Cross Triger-IF of the Coresight. At initialization, the cooperative debugging functions are disabled.

To use cooperative debugging functions between external-LSI, set the external-LSI cooperative debugging functions (MDT[2:0]=010) shown in Table 60.9 Trace Functions. VIO_D2 is Input Pin (Signal from external-LSI to AP-ARM), VIO_D1 is Output Pin (Signal from AP-ARM to external LSI). These two signals are connected to Cross Triger-IF of Coresight.

60.2.3 Debugging Mode Setting at Shipment

Since only a secure boot is available in the settings at shipment of mass production version, directions or modes in which breaks can be performed are limited. In addition, the DBGREG1 register does not reflect the settings of pins (the seven external DBGMD10, DBGMD21, DBGMD20, DBGMD11, DBGMD2, DBGMD1, and DBGMDT0 pins). Even if an attempt to read from DBGREG1 is made, 0 is read from the bits intended to reflect the values of the DBGMD10, DBGMD21, DBGMD20, DBGMD11, DBGMD2, DBGMD1, and DBGMDT0 pins. However, setting the DBGREG1 register through the CPU by software allows a debug mode to be entered. After entering the debug mode, the values that have written by software can be read from DBGREG1. The debugging resource and the corresponding register setting at mass-production version of this LSI is listed in Table 60.6.

Table 60.6 Debugging resource and the corresponding register setting at mass-production

Register Setting (DBGREG1)				
MD12	**MD10**	**MD21**	**MD20**	**SDHI0**
0	1	1	0	AP-ARM

60.3 Register Descriptions

A list of implemented registers is summarized in Table 60.7. Of these registers, DBGREG1/2/9 can be accessed from both the CPU and JTAG pins, although they can be accessed only from the CPU if pin-switching mode is selected. The JTAG commands shown in the Table 60.7 serve as commands that will be entered upon access to a register from the emulator. Entering these commands makes it possible to access the corresponding register.

Only after write operations to the KEY register, it is possible to write to DBGREG1, DBGREG2. Note that the KEY register requires two phases of writing.

Table 60.7 Register Configuration

Register Name	Abbreviation	R/W	CPU Address*4	R/W	JTAG Command	Access Size
Debugging function selection register*3	DBGREG1	R/W	H'E610_0020/ H'E610_8020	R/W	B'0011_1000	32
LSI control register	DBGREG2	R/W	H'E610_0024/ H'E610_8024	R/W	B'1011_1000	32
KEY register	DBGREG9	R/W	H'E610_0040/ H'E610_8040	R/W	B'0010_0100	32
Access priority control register*3	DBGREG10	—	—*1	R/W	B'1010_0100	32

Notes: 1. Accessible only from the JTAG.
2. Accessible from the CPU only under software control.
3. Not a target for diagnosis.
4. Address H'E610_0XXX is a non semaphore-address of this register and accessing through this address is not controlled by HPB semaphore.
Address H'E610_8XXX is a semaphore-address of this register and accessing thorough this address is controlled by HPB semaphore.

The initialization condition of these registers is summarized in Table 60.8. Note that the initialization condition of each register depends on the ICE connection conditions and LSI modes such as normal and diagnosis.

Table 60.8 Register Initialization Conditions

ICE Connection Condition	Normal Mode
ICE is connected only to the JTAG pin	Initialization is performed only by a power-on reset (PRESET_N)
ICE is connected only to the SDHI0 pin	Initialization is performed by simultaneously asserting PRESET_N and TRST_N
ICE is connected to the JTAG and SDHI0 pins	Initialization is performed by simultaneously asserting PRESET_N and TRST_N

Note: In normal mode, initialization is performed only by asserting a power-on reset.

60.3.1 Debugging Function Selection Register (DBGREG1)

This register is intended to reflect the values entered into external pins. In pin switching mode, it is possible to perform read/write operations only from the CPU.

The values for external pins are set when initialization is performed.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MD11	MD10	MD21	MD20	—	—	—	—	MD12	—	—	—	—	—	SDJ[1:0]	
Initial value:	0	*	*	*	0	0	0	0	*	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R	R	R	R	R	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MDT[2:0]			DMON	—	—	—	—	MDA[7:0]							
Initial value:	*	*	*	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	MD11	Pin input	R/W	Selects resources to be connected to external pins. See Table 60.5.
30	MD10	Pin input	R/W	Selects resources to be connected to external pins. See Table 60.5.
29、28	MD21、MD20	Pin input	R/W	Selects resources to be connected to external pins. See Table 60.5.
27～24	—	All 0	R	Reserved
23	MD12	Pin input	R/W	Selects resources to be connected to external pins. See Table 60.5. The value of the DBGMDT[0] pin input is reflected in the initial value.
22～20	—	All 0	R	Reserved
19	—	unknown	R	Reserved
18	—	All 0	R	Reserved
17、16	SDJ[1:0]	00	R/W	Bits for setting details in order to connect external pins with modules to be debugged.
15～13	MDT[2:0]	Pin input	R/W	Equivalent to DBGMDT as pin input. It selects the trace function.
12～8	—	All 0	R	Reserved

Bit	Bit Name	Initial Value	R/W	Description
7～0	MDA[7:0]	H'00	R/W	Monitoring function selection bits for debugging

60.3.2 LSI Control Register (DBGREG2)

This is a register used to make reset-related settings. In pin switching mode, it is possible to perform read/write operations only from the CPU.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RSTEN	ARSTEN	RSTAEN	RSTBEN	—	—	ERREN	CORESTBYEN	—	—	APDBGHIST	SHDBGHIST	DBGHIST	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	SHRST	APRST	—	—	—	—	—	—	APSH_TRST	APARM_TRST	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R

Bit	Bit Name	Initial Value	R/W	Description
31	RSTEN	0	R/W	Prohibits the reset input to each CPU core during debugging. 0: Disables prohibiting control regarding the reset input. 1: Enables prohibiting control regarding the reset input.
30	ARSTEN	0	R/W	Prohibits the area reset issue upon power shutdown during debugging. 0: Disables prohibiting control regarding the area reset issue. 1: Enables prohibiting control regarding the area reset issue.
29	RSTAEN	0	R/W	Prohibits RESETA during debugging. 0: Disables prohibiting control. 1: Enables prohibiting control.
28	RSTBEN	0	R/W	Prohibits RESETB during debugging. 0: Disables prohibiting control. 1: Enables prohibiting control.
27, 26	—	0	R	Reserved

Bit	Bit Name	Initial Value	R/W	Description
25	ERREN	0	R/W	Prohibits the SHwy error response during debugging. 0: Disables prohibiting control. 1: Enables prohibiting control.
24	CORESTBYEN	0	R/W	Prohibits core standby during debugging. 0: Disables prohibiting control. 1: Enables prohibiting control.
23,22	—	0	R	Reserved
21	APDBGHIST	0	R	Indicates that the ICE of AP-ARM has a history of being ready for connecting. 0: The ICE of AP-ARM has never been ready for connecting before. 1: The ICE of AP-ARM has been ready for connecting before.
20	SHDBGHIST	0	R	Indicates that the ICE of SH has a history of being ready for connecting. 0: The ICE of SH has never been ready for connecting before. 1: The ICE of SH has been ready for connecting before.
19	DBGHIST	0	R	Indicates that any of the ICEs has a history of being ready for connecting. 0: The ICEs have never been ready for connecting before. 1: Any of the ICEs has been ready for connecting before.
18 to 11	—	0	R	Reserved
10	SHRST	0	R	Reports that SH is being reset. 0: Reset being negated 1: Reset being asserted
9	APRST	0	R	Reports that ARM on the system side is being reset. 0: Reset being negated 1: Reset being asserted
8 to 3	—	0	R	Reserved
2	APSH_TRST	0	R/W	Issues a reset to each APSH_JTAG circuit during debugging. 0: Issues no reset. 1: Issues a reset.
1	APARM_TRST	0	R/W	Issues a reset to each APARM_JTAG circuit during debugging. 0: Issues no reset. 1: Issues a reset.
0	—	0	R	Reserved

60.3.3 KEY Register (DBGREG9)

The DBGREG provides registers that control write operation to the DBGREG so that the DBGREG properly functions to establish a link with the ICE during debugging and prevents invalid access due to a program error from breaking the link. This register has a key role in preventing such invalid access. It is possible to perform read/write operations only from the CPU. It is not possible to perform read/write operations from the emulator.

Writing the KEY code into this register in two steps enables access to the DBGREG. Use the following procedure.

1. First, write 8'hA5 to bits 15 to bit 8. This enables writing to bit 0 in the KEY register.
2. Next, write 8'hA5 to bits 15 to bit 8 and 1'b1 to bit 0 at the same time to enable writing to the other DBGREG registers.

To disable access to the DBGREG, write 0 to all the bits in the DBGREG9 register.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	AID[7:0]								–	–	–	–	–	–	–	KEY
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	0	R	Reserved
15 to 8	AID[7:0]	H'00	R/W	KEY Bit Write Aid Use this bit to write a bit pattern (H'A5) to be written to the KEY bit.
7 to 1	—	0	R	Reserved

Bit	Bit Name	Initial Value	R/W	Description
0	KEY	0	R/W	DBGREG access control Provides access control to the DBGREG. 0: It is not possible to perform read/write operations from/to the DBGREG. 1: It is possible to perform read/write operations from/to the DBGREG. When writing 1 to this bit, be sure to write H'A5 to the AID bits at the same time.

60.3.4 Access Control Register (DBGREG10)

This register specifies settings for determining priority over writing to the DBGREG.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	AI1	AL0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	0	R	Reserved
1	AL1	0	R/W	DBGREG2 access priority control 0: Places priority on CPU access (initial value). 1: Places priority on JTAG access.
0	AL0	0	R/W	DBGREG1 access priority control 0: Places priority on CPU access (initial value). 1: Places priority on JTAG access.

60.4 Trace/Monitoring Functions for Debugging

This section explains how to specify settings for the following debugging functions: trace function from each core and monitoring function. This section also explains the assignment of I/O pins.

60.4.1 Trace Functions

Each of the CPU cores is provided with trace function. Since there are no pins dedicated to outputting trace data, the MDT[2:0] bits in the DBGREG1 register are set to output the data through the VIO pins or the SDHI card pins and to specify trace data.

Table 60.9 shows the MDT[2:0] values and their respective output pins. For more details on the output pins and function assignments, refer to the corresponding tables.

Table 60.9 List of Trace Functions

MDT [2:0]	Function Summary	Output Pin	Refer to	Remark
000	Normal function	—	—	—
001	AP-ARM ETM11 trace data	VIO_D15 to VIO_D0	Table 60.10	—
010	External-LSI cooperative debugging function	VIO_D15 to VIO_D0		—
011	SH-X2 AUD trace data	VIO_D15 to VIO_D0		—
100	Monitoring function for debugging	—	—	*3
101	AP-ARM ETM11 trace data	SDHI0*1, SDHI1*2	Table 60.11	—
111	SH-X2 AUD trace data	SDHI1*2		—

Note: 1. SDHI0 represents the SDHICLK0/SDHICD0/SDHID0_[3:0]/SDHICMD0/SDHIWP0 pins
2. SDHI1 represents the SDHICLK1/SDHID1_[3:0]/SDHICMD1 pins
3. Details on the monitoring function are given in the next section, 60.4.2.

The VIO pins (VIO_D15 to VIO_D0) and changes in their pin functions after enabling the trace function are listed in Table 60.10. The SDHI0/1 pins and changes in their pin functions after enabling the trace function are also listed in Table 60.11.

Table 60.10 VIO Pins and Changes in their Functions

Pin	AP-ETM11 Trace Data	External-LSI cooperative debugging function	SH-AUD Trace Data
VIO_D15	0	—	0
VIO_D14	0	—	0
VIO_D13	0	—	0
VIO_D12	1	—	0
VIO_D11	TRACECTL	—	0
VIO_D10	TRACEDATA1_0	—	0
VIO_D9	TRACEDATA1_7	—	0
VIO_D8	TRACEDATA1_6	—	0
VIO_D7	TRACEDATA1_5	—	0
VIO_D6	TRACEDATA1_4	—	0
VIO_D5	TRACEDATA1_3	—	AUDATA3
VIO_D4	TRACEDATA1_2	—	AUDATA2
VIO_D3	TRACEDATA1_1	—	AUDATA1
VIO_D2	0	CTIREQ **(External-LSI→mobileAP4)**	AUDATA0
VIO_D1	0	CTIACK **(mobileAP4→External-LSI)**	AUDSYNC
VIO_D0	TRACECLK1	—	AUDCLK

Table 60.11 SDHI0/1 Pins and Changes in their Functions

Pin	AP-ETM11 Trace Data	SH-AUD Trace Data
SDHICLK0	0	—
SDHICD0	1	—
SDHICMD0	TRACECTL	—
SDHIWP0	TRACEDATA1_0	—
SDHID0_3	TRACEDATA1_7	—
SDHID0_2	TRACEDATA1_6	—
SDHID0_1	TRACEDATA1_5	—
SDHID0_0	TRACEDATA1_4	—
SDHICLK1	TRACEDATA1_3	AUDATA3
SDHICMD1	TRACEDATA1_2	AUDATA2
SDHID1_3	TRACEDATA1_1	AUDATA1
SDHID1_2	0	AUDATA0
SDHID1_1	0	AUDSYNC
SDHID1_0	TRACECLK1	AUDCLK

60.4.2 Monitoring Functions for Debugging

The monitoring functions are provided as a debugging function in order to monitor the internal state of the LSI through external pins. Since there are no pins dedicated to the monitoring function, the MDA[7:0] bits in the DBGREG1 register are set to output monitoring data through the VIO pins or the SDHI card pins and to specify monitoring settings (note that DBGREG1.MDT[2:0] is assumed to be 100).

Table 60.12 lists the MDA[7:0] values and their respective output pins. For more details on the output pins and function assignments, refer to the corresponding tables listed.

Table 60.12 List of Monitoring Functions for Debugging

MDA[6:0]	Function Summary	I/O Pins	Refer to	Remarks
000_1000	SBSC1 performance monitor 0	SDHI0*[1], SDHI1*[2]	Table 60.13	*[3]
000_1001	SBSC1 performance monitor 1	VIO_D15 to VIO_D0	Table 60.14	*[3]
		SDHI0*[1], SDHI1*[2]		*[5]
000_1110	AP DMAC transfer monitor 1	VIO_D15 to VIO_D0	Table 60.15	—

MDA[6:0]	Function Summary	I/O Pins	Refer to	Remarks
0000_1111	AP DMAC transfer monitor 2	VIO_D15 to VIO_D0	Table 60.15	—
0010_0001	Clock monitor	VIO_D15 to VIO_D0	Table 60.16	—
0010_0010	CPU sleep mode monitor	VIO_D15 to VIO_D0	Table 60.16	—
0010_0011	AP interrupt monitor 1	VIO_D15 to VIO_D0	Table 60.17	—
0010_0100	AP interrupt monitor 2	VIO_D15 to VIO_D0	Table 60.17	—
0010_0101	AP interrupt monitor 3	VIO_D15 to VIO_D0	Table 60.17	—
0010_0110	AP interrupt monitor 4	VIO_D15 to VIO_D0	Table 60.18	—
0010_1001	Power-off status monitor 1	VIO_D15 to VIO_D0	Table 60.19	—
0011 0100	DMAC status monitor 1	VIO_D15 to VIO_D0	Table 60.20	—
0011 0101	DMAC status monitor 2	VIO_D15 to VIO_D0	Table 60.20	—
0011 0110	DMAC status monitor 3	VIO_D15 to VIO_D0	Table 60.20	—
0011 0111	DMAC status monitor 4	VIO_D15 to VIO_D0	Table 60.21	—
0011 1000	DMAC status monitor 5	VIO_D15 to VIO_D0	Table 60.21	—
0011 1001	HPB semaphore monitor 1	VIO_D15 to VIO_D0	Table 60.22	—
0011 1010	HPB semaphore monitor 2	VIO_D15 to VIO_D0	Table 60.22	—
0011_1011	SHwy state monitor 9	VIO_D15 to VIO_D0	Table 60.24	—
0011_1100	SHwy state monitor 10	VIO_D15 to VIO_D0	Table 60.24	—
0110 0110	CPORTR2S/S2R debug monitor	VIO_D15～VIO_D0	Table 60.25	—
0111 0010	HPB semaphore monitor 4	VIO_D15～VIO_D0	Table 60.23	—
0111 0011	HPB semaphore monitor 5	VIO_D15～VIO_D0	Table 60.23	—
0111 1000	AP clock monitor	VIO_D15～VIO_D0	Table 60.26	—
0111 1001	MFIM semaphore monitor	VIO_D15～VIO_D0	Table 60.27	—
0111 1010	Internal signal monitor of MSIOF0	LCDD23～LCDD0*4	Table 60.28	—
0111 1011	Internal signal monitor of MSIOF1	LCDD23～LCDD0*4	Table 60.28	—
0111 1110	IIC monitor 1	LCDD23～LCDD0*4	Table 60.29	—
0111 1111	IIC monitor 2	VIO_D15～VIO_D0	Table 60.30	—

Note: 1. SDHI0 represents the SDHICLK0/SDHICD0/SDHID0_[3:0]/SDHICMD0/SDHIWP0 pins
2. SDHI1 represents the SDHICLK1/SDHID1_[3:0]/SDHICMD1 pins
3. This monitor signal does not pass the TDBG module because the PAD is directly connected to the corresponding module. The TDBG module only outputs selection signal to the PAD.
4. To use this monitoring functions, set MSEL15 to 1.

5. This monitoring functions cannot be used with MSEL15=1.
   To use this monitoring functions, set MSEL15 to 0.

In the following section, the monitoring signals assigned to the VIO pins (VIO_D15 to VIO_D0) and the SDHI0/1 pins are listed. The monitoring signals are available after enabling the monitoring functions.

60.4.2.1 SBSC1 Performance Monitor 0

These functions monitor the performance and internal signals of the SBSC1 (BSC for AP-ARM DDR-SDRAM). Details on the pin assignments are given in Table 60.13

Table 60.13 Details on Pin Assignments for SBSC1

Pin	SBSC1 Performance Monitor 0
VIO_D15	–
VIO_D14	–
VIO_D13	–
VIO_D12	–
VIO_D11	–
VIO_D10	–
VIO_D9	–
VIO_D8	–
VIO_D7	–
VIO_D6	–
VIO_D5	–
VIO_D4	–
VIO_D3	–
VIO_D2	–
VIO_D1	–
VIO_D0	–
SDHICLK0	SBSC1_CLK
SDHICD0	–
SDHICMD0	SBSC1_RW

Pin	SBSC1 Performance Monitor 0
SDHIWP0	—
SDHID0_3	SBSC1_CAS
SDHID0_2	SBSC1_RAS
SDHID0_1	SBSC1_CS0
SDHID0_0	SBSC1_CS1
SDHICLK1	—
SDHICMD1	SBSC1_CKE0
SDHID1_3	SBSC1_CKE1
SDHID1_2	SBSC1_BA2
SDHID1_1	SBSC1_BA1
SDHID1_0	SBSC1_BA0

60.4.2.2 SBSC1 Performance Monitor 1

These functions monitor the addresses of the SBSC1 (BSC for AP-ARM DDR-SDRAM).

Details on the pin assignments are given in Table 60.14.

Table 60.14 Details on Pin Assignments for SBSC1

Pin	SBSC1 Performance Monitor 1
VIO_D15	—
VIO_D14	SBSC1_ADR14
VIO_D13	SBSC1_ADR13
VIO_D12	SBSC1_ADR12
VIO_D11	SBSC1_ADR11
VIO_D10	SBSC1_ADR10
VIO_D9	SBSC1_ADR9
VIO_D8	SBSC1_ADR8
VIO_D7	SBSC1_ADR7
VIO_D6	SBSC1_ADR6
VIO_D5	SBSC1_ADR5
VIO_D4	SBSC1_ADR4
VIO_D3	SBSC1_ADR3

Pin	SBSC1 Performance Monitor 1
VIO_D2	SBSC1_ADR2
VIO_D1	SBSC1_ADR1
VIO_D0	SBSC1_ADR0
SDHICLK0	SBSC1_CLK
SDHICD0	—
SDHICMD0	SBSC1_RW
SDHIWP0	—
SDHID0_3	SBSC1_CAS
SDHID0_2	SBSC1_RAS
SDHID0_1	SBSC1_CS0
SDHID0_0	SBSC1_CS1
SDHICLK1	—
SDHICMD1	SBSC1_CKE0
SDHID1_3	SBSC1_CKE1
SDHID1_2	SBSC1_BA2
SDHID1_1	SBSC1_BA1
SDHID1_0	SBSC1_BA0

These monitoring functions are also capable of monitoring performance and internal access as well as address.

60.4.2.3 AP DMAC Transfer Monitors

Details on pin assignments for AP DMAC transfer monitor are given in Table 60.15.

Table 60.15 Details on Pin Assignments for AP DMAC Transfer Monitors

Pin	AP DMAC Transfer Monitor 1	AP DMAC Transfer Monitor 2
VIO_D15	0	0
VIO_D14	0	0
VIO_D13	0	0
VIO_D12	0	0
VIO_D11	RTDMAC transfer request ch5	DMAC2 transfer request ch5
VIO_D10	RTDMAC transfer request ch4	DMAC2 transfer request ch4
VIO_D9	RTDMAC transfer request ch3	DMAC2 transfer request ch3
VIO_D8	RTDMAC transfer request ch2	DMAC2 transfer request ch2
VIO_D7	RTDMAC transfer request ch1	DMAC2 transfer request ch1
VIO_D6	RTDMAC transfer request ch0	DMAC2 transfer request ch0
VIO_D5	DMAC1 transfer request ch5	DMAC3 transfer request ch5
VIO_D4	DMAC1 transfer request ch4	DMAC3 transfer request ch4
VIO_D3	DMAC1 transfer request ch3	DMAC3 transfer request ch3
VIO_D2	DMAC1 transfer request ch2	DMAC3 transfer request ch2
VIO_D1	DMAC1 transfer request ch1	DMAC3 transfer request ch1
VIO_D0	DMAC1 transfer request ch0	DMAC3 transfer request ch0

60.4.2.4 Clock/CPU Sleep Mode Monitors

Table 60.16 gives details on the pin assignments for the following monitors, clock monitor for monitoring clocks output from CPG, and CPU sleep mode monitor for monitoring the sleep status of the CPU.

Table 60.16 Details on Pin Assignments for Clock/CPU Sleep Mode Monitor

Pin	Clock Monitor	CPU Sleep Mode Monitor
VIO_D15	0	0
VIO_D14	0	0
VIO_D13	0	0
VIO_D12	0	A3SM area power-off status monitors
VIO_D11	0	A4R area power-off status monitors
VIO_D10	0	A4LC area power-off status monitors
VIO_D9	0	0
VIO_D8	SPCK	0
VIO_D7	ZXCK	0
VIO_D6	CPCLK	SH-X2 core standby
VIO_D5	ZB3CLK	AP-ARM core standby
VIO_D4	ZGCLK	0
VIO_D3	ZCLK	0
VIO_D2	BCLK	SH-X2 sleep request
VIO_D1	ZSCLK	AP-ARM sleep request
VIO_D0	ICLK	0

60.4.2.5 Interrupt Monitors

Table 60.17 and Table 60.18 gives details on the pin assignments for interrupt requests from internal modules.

Table 60.17 Details on Pin Assignments for Interrupt Monitor (1)

Pin	AP-system Interrupt Monitor 1	AP-system Interrupt Monitor 2	AP-system Interrupt Monitor 3
VIO_D15	LCD0_AB	0	0
VIO_D14	LCD0_OV	0	0
VIO_D13	LCD0_REF	0	0
VIO_D12	LCDC1 interrupt request	0	0
VIO_D11	VPU interrupt request	0	0
VIO_D10	SGX interrupt request	0	0
VIO_D9	JPU interrupt request	0	0
VIO_D8	LCDC0 interrupt request	EVTCODEA8	EVTCODESA8
VIO_D7	RT interrupt level 3	EVTCODEA7	EVTCODESA7
VIO_D6	RT interrupt level 2	EVTCODEA6	EVTCODESA6
VIO_D5	RT interrupt level 1	EVTCODEA5	EVTCODESA5
VIO_D4	RT interrupt level 0	EVTCODEA4	EVTCODESA4
VIO_D3	SY interrupt level 3	EVTCODEA3	EVTCODESA3
VIO_D2	SY interrupt level 2	EVTCODEA2	EVTCODESA2
VIO_D1	SY interrupt level 1	EVTCODEA1	EVTCODESA1
VIO_D0	SY interrupt level 0	EVTCODEA0	EVTCODESA0

Table 60.18 Details on Pin Assignments for Interrupt Monitor (2)

Pin	AP-system Interrupt Monitor 4
VIO_D15	CEU interrupt request
VIO_D14	JPU6E interrupt request
VIO_D13	DSI-TX interrupt request
VIO_D12	CSI-RX interrupt request
VIO_D11	periisp interrupt request
VIO_D10	–
VIO_D9	2D-DMAC interrupt request

Pin	AP-system Interrupt Monitor 4
VIO_D8	0
VIO_D7	0
VIO_D6	VEU4 interrupt request
VIO_D5	VEU3 interrupt request
VIO_D4	VEU2 interrupt request
VIO_D3	VEU1 interrupt request
VIO_D2	BEU3 interrupt request
VIO_D1	BEU2 interrupt request
VIO_D0	BEU1 interrupt request

60.4.2.6 Power-off Status Monitors

Table 60.19 gives details on the pin assignments for the power-off status monitors.

Table 60.19 Details on Pin Assignments for Power-off Status Monitors

Pin	Power-off Status Monitor 1
VIO_D15	0
VIO_D14	0
VIO_D13	0
VIO_D12	A4LC area
VIO_D11	A4MP area
VIO_D10	D4 area
VIO_D9	0
VIO_D8	A4R area
VIO_D7	RT-CPU core standby
VIO_D6	A3RV area
VIO_D5	0
VIO_D4	A4S area
VIO_D3	A3SG area
VIO_D2	A3SP area
VIO_D1	A3SM area
VIO_D0	SYS-CPU core standby

60.4.2.7 DMAC status Monitors

These monitors are used to monitor status of the DMAC.

Table 60.20, Table 60.21 gives details on pin assignments for the DMAC status monitors.

Table 60.20 Details on Pin Assignments for DMAC Status Monitors (1)

Pin	DMAC status Monitors 1	DMAC status Monitors 2	DMAC status Monitors 3
VIO_D15	0	0	0
VIO_D14	0	0	0
VIO_D13	0	0	0
VIO_D12	RTDMAC DINT	RTDMAC2 DINT	DMAC1 DINT
VIO_D11	RTDMAC HE ch5	RTDMAC2 HE ch5	DMAC1 HE ch5
VIO_D10	RTDMAC TE ch5	RTDMAC2 TE ch5	DMAC1 TE ch5
VIO_D9	RTDMAC HE ch4	RTDMAC2 HE ch4	DMAC1 HE ch4
VIO_D8	RTDMAC TE ch4	RTDMAC2 TE ch4	DMAC1 TE ch4
VIO_D7	RTDMAC HE ch3	RTDMAC2 HE ch3	DMAC1 HE ch3
VIO_D6	RTDMAC TE ch3	RTDMAC2 TE ch3	DMAC1 TE ch3
VIO_D5	RTDMAC HE ch2	RTDMAC2 HE ch2	DMAC1 HE ch2
VIO_D4	RTDMAC TE ch2	RTDMAC2 TE ch2	DMAC1 TE ch2
VIO_D3	RTDMAC HE ch1	RTDMAC2 HE ch1	DMAC1 HE ch1
VIO_D2	RTDMAC TE ch1	RTDMAC2 TE ch1	DMAC1 TE ch1
VIO_D1	RTDMAC HE ch0	RTDMAC2 HE ch0	DMAC1 HE ch0
VIO_D0	RTDMAC TE ch0	RTDMAC2 TE ch0	DMAC1 TE ch0

Table 60.21 Details on Pin Assignments for DMAC Status Monitors (2)

Pin	DMAC status Monitors 4	DMAC status Monitors 5
VIO_D15	0	0
VIO_D14	0	0
VIO_D13	0	0
VIO_D12	DMAC2 DINT	DMAC3 DINT
VIO_D11	DMAC2 HE ch5	DMAC3 HE ch5
VIO_D10	DMAC2 TE ch5	DMAC3 TE ch5
VIO_D9	DMAC2 HE ch4	DMAC3 HE ch4

Pin	DMAC status Monitors 4	DMAC status Monitors 5
VIO_D8	DMAC2 TE ch4	DMAC3 TE ch4
VIO_D7	DMAC2 HE ch3	DMAC3 HE ch3
VIO_D6	DMAC2 TE ch3	DMAC3 TE ch3
VIO_D5	DMAC2 HE ch2	DMAC3 HE ch2
VIO_D4	DMAC2 TE ch2	DMAC3 TE ch2
VIO_D3	DMAC2 HE ch1	DMAC3 HE ch1
VIO_D2	DMAC2 TE ch1	DMAC3 TE ch1
VIO_D1	DMAC2 HE ch0	DMAC3 HE ch0
VIO_D0	DMAC2 TE ch0	DMAC3 TE ch0

60.4.2.8 HPB Semaphore Monitor

This monitors are used to monitor semaphore of the HPB.

Table 60.22, Table 60.23 gives details on pin assignments for the HPB Semaphore Monitor.

Table 60.22 Details on Pin Assignments for the HPB Semaphore Monitor (1)

Pin	HPB Semaphore Monitor 1	HPB Semaphore Monitor 2
VIO_D15	0	0
VIO_D14	CPG semaphore acquired by Coretex	SYSC semaphore acquired by Coretex
VIO_D13	CPG semaphore acquired by SH	SYSC semaphore acquired by SH
VIO_D12	CPG semaphore released forcibly by time out	SYSC semaphore released forcibly by time out
VIO_D11	CPG semaphore released forcibly by Master CPU	SYSC semaphore released forcibly by Master CPU
VIO_D10	0	0
VIO_D9	Coretex CPG access error	Coretex SYSC access error
VIO_D8	Coretex CPG access error	SH SYSC access error
VIO_D7	0	0
VIO_D6	0	0
VIO_D5	0	0
VIO_D4	0	0
VIO_D3	0	0
VIO_D2	0	0
VIO_D1	0	0
VIO_D0	0	0

Table 60.23 Details on Pin Assignments for the HPB Semaphore Monitor (2)

Pin	HPB Semaphore Monitor 4	HPB Semaphore Monitor 5
VIO_D15	0	0
VIO_D14	GPIO semaphore acquired by Coretex	DBG semaphore acquired by Coretex
VIO_D13	GPIO semaphore acquired by SH	DBG semaphore acquired by SH
VIO_D12	GPIO semaphore released forcibly by time out	DBG semaphore forced release by time out

Pin	HPB Semaphore Monitor 4	HPB Semaphore Monitor 5
VIO_D11	GPIO semaphore released forcibly by Master CPU	DBG semaphore forced release by Master CPU
VIO_D10	0	0
VIO_D9	Coretex GPIO access error	Coretex DBG access error
VIO_D8	SH GPIO access error	SH DBG access error
VIO_D7	Reserved	0
VIO_D6	Reserved	CMT2 semaphore acquired by Coretex
VIO_D5	Reserved	CMT2 semaphore acquired by SH
VIO_D4	Reserved	CMT2 semaphore forced release by time out
VIO_D3	Reserved	CMT2 forced release by Master CPU
VIO_D2	Reserved	0
VIO_D1	Reserved	Coretex CMT2 access error
VIO_D0	Reserved	SH CMT2 access error

60.4.2.9 SHwy Status Monitors

The SHwy monitors are used to monitor the status or the SHwy. Table 60.24 shows details on the pin assignments for the SHwy monitors.

Table 60.24 Details on Pin Assignments for SHwy Status Monitor

Pin	SHwy Status Monitor 9	SHwy Status Monitor 10
VIO_D15	GPR Resp. HS0 (Cortex-A8)	GPR Req. HS0 (SBSC1)
VIO_D14	GPR Resp. HS1 (ICB)	GPR Req. HS1 (ICB)
VIO_D13	GPR Resp. HS2 (others)	0
VIO_D12	GPR Resp. RT0 (SHX)	GPR Req. COM2 (BSC)
VIO_D11	0	0
VIO_D10	0	GPR Resp. RT0 (SHX)
VIO_D9	GPR Req. RT0 (HSGPR)	GPR Resp. RT1 (others)
VIO_D8	GPR Req. RT1 (others)	GPR Resp. HS0 (Cortex-A8)
VIO_D7	GPR Req. HS0 (SBSC1)	GPR Resp. HS1 (ICB)
VIO_D6	GPR Req. HS1 (ICB)	GPR Resp. HS2 (others)
VIO_D5	GPR Req. HS2 (ComGPR)	GPR Resp. HS3 (ComGPR)
VIO_D4	GPR Req. HS3 (others)	GPR Resp. HS4 (RTGPR)
VIO_D3	0	GPR Resp. COM0 (HSGPR)
VIO_D2	GPR Req. COM1 (HSGPR)	0
VIO_D1	GPR Req. COM2 (BSC)	0
VIO_D0	GPR Req. COM3 (others)	GPR Resp. COM3 (others)

60.4.2.10 CPORTR2S/S2R Debugging Monitors

Table 60.25 shows details on the pin assignments for the CPORTR2S/S2R debugging monitors.

Table 60.25 Details on Pin Assignments for CPORTR2S/S2R Debugging Monitors

Pin	CPORTR2S/S2R Debugging Monitors
VIO_D15	0
VIO_D14	0
VIO_D13	0
VIO_D12	0
VIO_D11	0
VIO_D10	0
VIO_D9	0
VIO_D8	0
VIO_D7	0
VIO_D6	0
VIO_D5	GPOS2R[2]
VIO_D4	GPOS2R[1]
VIO_D3	GPOS2R[0]
VIO_D2	GPOR2S[2]
VIO_D1	GPOR2S[1]
VIO_D0	GPOR2S[0]

60.4.2.11 AP Clock Monitors

Table 60.26 shows details on the pin assignments for the AP clock monitors.

Table 60.26 Details on Pin Assignments for AP Clock Monitors

Pin	AP Clock Monitors
VIO_D15	FMSIΦ
VIO_D14	FMSOΦ
VIO_D13	FSIAΦ
VIO_D12	SUBΦ
VIO_D11	SPUΦ
VIO_D10	ISPBΦ
VIO_D9	ISPMΦ
VIO_D8	HDMIΦ
VIO_D7	DSITΦ
VIO_D6	DSIPΦ
VIO_D5	VOUΦ
VIO_D4	M1Φ
VIO_D3	CSIRΦ
VIO_D2	HPΦ
VIO_D1	main clock (EXTAL1) x 1/2
VIO_D0	0

60.4.2.12 MFIM Semaphore Monitors

Table 60.27 shows details on the pin assignments for the MFIM semaphore monitors.

Table 60.27 Details on Pin Assignments for MFIM Semaphore Monitors

Pin	MFIM Semaphore Monitors
VIO_D15	0
VIO_D14	0
VIO_D13	0
VIO_D12	0
VIO_D11	0
VIO_D10	0
VIO_D9	0
VIO_D8	0
VIO_D7	mf_sm4moni[7]
VIO_D6	mf_sm4moni[6]
VIO_D5	mf_sm4moni[5]
VIO_D4	mf_sm4moni[4]
VIO_D3	mf_sm4moni[3]
VIO_D2	mf_sm4moni[2]
VIO_D1	mf_sm4moni[1]
VIO_D0	mf_sm4moni[0]

60.4.2.13 MSIOF0-1 Internal Signals Monitors

These monitoring functions are used to monitor the internal signals of MSIOF0, MSIOF1.

Table 60.28 shows details on the pin assignments for the MSIOF0-1 internal signals Monitors.

To use this monitoring function, set MSEL15 to 1.

Table 60.28 Details on Pin Assignments for MSIOF0-1 Internal Signals Monitors

Pin	MSIOF0 Monitor	MSIOF1 Monitor
LCDD23	0	0
LCDD22	0	0
LCDD21	0	0
LCDD20	0	0
LCDD19	SISTR.TFOVF (transmission FIFO overflow)	SISTR.TFOVF (transmission FIFO overflow)
LCDD18	SISTR.TFUDF (transmission FIFO underflow)	SISTR.TFUDF (transmission FIFO underflow)
LCDD17	SISTR.RFOVF (reseption FIFO overflow)	SISTR.RFOVF (reseption FIFO overflow)
LCDD16	SISTR.RFUDF (reseption FIFO underflow)	SISTR.RFUDF (reseption FIFO underflow)
LCDD15	SIFCTR.TFUA[6] (transmission FIFO usable erea)	SIFCTR.TFUA[6] (transmission FIFO usable erea)
LCDD14	SIFCTR.TFUA[5] (transmission FIFO usable erea)	SIFCTR.TFUA[5] (transmission FIFO usable erea)
LCDD13	SIFCTR.TFUA[4] (transmission FIFO usable erea)	SIFCTR.TFUA[4] (transmission FIFO usable erea)
LCDD12	SIFCTR.TFUA[3] (transmission FIFO usable erea)	SIFCTR.TFUA[3] (transmission FIFO usable erea)
LCDD11	SIFCTR.TFUA[2] (transmission FIFO usable erea)	SIFCTR.TFUA[2] (transmission FIFO usable erea)
LCDD10	SIFCTR.TFUA[1] (transmission FIFO usable erea)	SIFCTR.TFUA[1] (transmission FIFO usable erea)

Pin	MSIOF0 Monitor	MSIOF1 Monitor
LCDD9	SIFCTR.TFUA[0] (transmission FIFO usable erea)	SIFCTR.TFUA[0] (transmission FIFO usable erea)
LCDD8	SIFCTR.RFUA[8] (reseption FIFO usable erea)	SIFCTR.RFUA[8] (reseption FIFO usable erea)
LCDD7	SIFCTR.RFUA[7] (reseption FIFO usable erea)	SIFCTR.RFUA[7] (reseption FIFO usable erea)
LCDD6	SIFCTR.RFUA[6] (reseption FIFO usable erea)	SIFCTR.RFUA[6] (reseption FIFO usable erea)
LCDD5	SIFCTR.RFUA[5] (reseption FIFO usable erea)	SIFCTR.RFUA[5] (reseption FIFO usable erea)
LCDD4	SIFCTR.RFUA[4] (reseption FIFO usable erea)	SIFCTR.RFUA[4] (reseption FIFO usable erea)
LCDD3	SIFCTR.RFUA[3] (reseption FIFO usable erea)	SIFCTR.RFUA[3] (reseption FIFO usable erea)
LCDD2	SIFCTR.RFUA[2] (reseption FIFO usable erea)	SIFCTR.RFUA[2] (reseption FIFO usable erea)
LCDD1	SIFCTR.RFUA[1] (reseption FIFO usable erea)	SIFCTR.RFUA[1] (reseption FIFO usable erea)
LCDD0	SIFCTR.RFUA[0] (reseption FIFO usable erea)	SIFCTR.RFUA[0] (reseption FIFO usable erea)

60.4.2.14 IIC Monitors

Table 60.29, Table 60.30 shows details on the pin assignments for the IIC monitors.

To use this monitoring functions 1, set MSEL15 to 1.

Table 60.29 Details on Pin Assignments for IIC Monitors 1

Pin	IIC Monitor 1
LCDD23	0
LCDD22	0
LCDD21	0
LCDD20	0
LCDD19	0
LCDD18	0
LCDD17	REQ monitor (SCL0/SDA0 Pins — IIC0)
LCDD16	ACK monitor (SCL0/SDA0 Pins — IIC0)
LCDD15	REQ monitor (SCL0/SDA0 Pins — IIC1)
LCDD14	ACK monitor (SCL0/SDA0 Pins — IIC1)
LCDD13	0
LCDD12	ACK monitor (SCL0/SDA0 Pins — IICB)
LCDD11	REQ monitor (SCL1/SDA1 Pins — IIC0)
LCDD10	ACK monitor (SCL1/SDA1 Pins — IIC0)
LCDD9	REQ monitor (SCL1/SDA1 Pins — IIC1)
LCDD8	ACK monitor (SCL1/SDA1 Pins — IIC1)
LCDD7	0
LCDD6	0
LCDD5	0
LCDD4	0
LCDD3	0
LCDD2	0
LCDD1	0
LCDD0	0

Table 60.30 Details on Pin Assignments for IIC Monitors 2

Pin	IICMonitor 2
VIO_D15	0
VIO_D14	0
VIO_D13	0
VIO_D12	0
VIO_D11	ICSR.AL monitor of IIC0
VIO_D10	ICSR.WAIT monitor of IIC0
VIO_D9	ICCR.TRS monitor of IIC0
VIO_D8	ICSR.AL monitor of IIC1
VIO_D7	ICSR.WAIT monitor of IIC1
VIO_D6	ICCR.TRS monitor of IIC1
VIO_D5	ICSR.AL monitor of IIC2
VIO_D4	ICSR.WAIT monitor of IIC2
VIO_D3	ICCR.TRS monitor of IIC2
VIO_D2	0
VIO_D1	0
VIO_D0	0

60.5 Support Debugging Function Using GPIO Internal Register Settings

The MSEL15 function in the [15] bit in the GPIO can change I/O function pins, described in section, 60.4.2, from the VIO pins to the LCDD pins. Table 60.32 shows the correspondence between these pins.

For details, refer to the chapter of GPIO.

Table 60.31 GPIO Internal Register

Register Name	Abbreviation	R/W	CPU Address	Initial Value	Access Size
Module Selection Function Register 3	MSEL3CR	R/W	H'E605_8020	H'0000_0000	32

Table 60.32 LCDD Pin Assignments for Monitoring Functions

Pin	Assigned Function
LCDD15	Monitoring function corresponding to VIO_D15
LCDD14	Monitoring function corresponding to VIO_D14
LCDD13	Monitoring function corresponding to VIO_D13
LCDD12	Monitoring function corresponding to VIO_D12
LCDD11	Monitoring function corresponding to VIO_D11
LCDD10	Monitoring function corresponding to VIO_D10
LCDD9	Monitoring function corresponding to VIO_D9
LCDD8	Monitoring function corresponding to VIO_D8
LCDD7	Monitoring function corresponding to VIO_D7
LCDD6	Monitoring function corresponding to VIO_D6
LCDD5	Monitoring function corresponding to VIO_D5
LCDD4	Monitoring function corresponding to VIO_D4
LCDD3	Monitoring function corresponding to VIO_D3
LCDD2	Monitoring function corresponding to VIO_D2
LCDD1	Monitoring function corresponding to VIO_D1
LCDD0	Monitoring function corresponding to VIO_D0

60.6 Power Supply Control Function

During debugging with the emulator, all the areas are always powered on by default. In this case, even if the SYSC perform power cutoff a certain area, a power shutdown sequence is performed but the actual power supply status of each area does not change (always powered on). This behavior of power control can be selectable by SYSC registers, and it is possible to cutoff the power supply of the specified area.

For details on register settings, refer to the section 13, System Controller (SYSC).

60.7 Overview of Debugging Functions for ARM Core Blocks

To support the debugging functions, the AP-ARM incorporates the Embedded ICE-RT, and ETM, ETB circuits as component for the Coresight System. The Embedded ICE-RT circuit is incorporated in the Cortex-A8 core (AP-ARM) as standard. Connecting this ICE-RT circuit to the corresponding ICE (such as a RealView-ICE manufactured by ARM Ltd.) allows program execution control and memory dumping.

The ETM component monitor the ARM operating status, then output the monitoring results to the external device as trace information. Using the appropriate ICE trace options allows the debugger on the ICE to trace ARM core execution status without breaking the program running in the ARM core.

The ETB component accumulates trace information in the built-in trace SRAM. The ETB captures trace data from the ETM component and it can accumulate trace data until the capacity (4 KB) of the trace SRAM is reached. The accumulated trace information can be accessed via the debugger of the ARM or via the Debug-APB bus of the Cortex-A8.

Table 60.33 shows detail on the debugging functions incorporated in the AP-ARM.

Table 60.33 ARM Core Configuration

Block		AP-ARM
Installed CPU core		Cortex-A8
Execution control mechanism		Embedded ICE-RT
Trace mechanism		ETM component
	r2p1 (Cortex-A8 version)	r0p2
	V3.3	v3.2
	Protocol version	(No definition)
	Trace output data width	8 bits
	Trace clock system	Half Rate-Clocking
	Upper limit for trace data rate	200MHz
	Variable function for trace data rate	Enabled (controlled by CPG)
	Number of address comparators	
	Number of data comparators	
	Memory map decoder	
	Counter	
	Sequencer	
	Number of FIFO stages	
	Control system used when trace FIFO is full	Suppressing trace output
Trace buffer		ETB component
	Module version	r2p1 (Cortex-A8 version)
	Trace SRAM capacity	4KB
	Connection bus	Debug-APB-Bus of Coresight System

Section 61 USB High-Speed DMAC (USBHS0-DMAC)

61.1 Features

- Two types of clock: ZSϕ and USBHS0 local bus clock (48 MHz), which are asynchronously absorbed in the local bus bridge
- The SHwy bus interface functions are implemented.

The SHwy bus interface handles data transfer with the memory and register settings.

- Data communication is performed using the local DMA protocol.
- Supports two channels that can work concurrently.
- Interrupts

— Setting count end interrupt

— Transfer end interrupt upon receiving a short packet from the USB-IP
This function allows generation of an interrupt even in the case where DMA transfer ends after receiving data less than the transfer size set in the DMAC.

— Timeout interrupt
A timeout interrupt can be generated after the specified cycles after the last USBHS0 transfer request. (This interrupt is used for the timeout when the final packet received is Max packet.)

— Interrupts can also be generated when a NULL packet is received or an address error is detected.

Table 61.1 Main Functions of This Module

Item	Description
Application	Transfer between USB-IP (FIFO) and SHwy bus (4-Gbyte arbitrary space)
Purpose of DMA transfer	High-speed data transfer between USB-IP and SHwy bus
DMA transfer end notification to the software	Interrupt signals (Transfer count end, USB-IP short packet reception, timeout, etc.)
Transfer space/transfer address direction	4-Gbyte arbitrary space (forward direction) to 4-Gbyte arbitrary space (forward direction)
Maximum transfer count	16,777,216
Transfer unit	8, 16, or 32 bytes
Control signals generated	Address/data read/data write conforming to the USB-IP local bus interface and SHwy bus protocols
Number of channels	2 (parallel operation enabled, round-robin control)
Bus specification	SHwy bus (SuperHyWay 64 bits), local bus (USB-IP local bus)
Clock	SHwy clock (130 MHz), USB local bus clock (48 MHz)
Max. Transfer rate	IN transfer: About 350 Mbps (in 32-byte transfer mode) OUT transfer: About 340 Mbps (in 32-byte transfer mode)

Table 61.2 Bus Access Type

	Supported Access Type
SHwy bus access (USBHS0-DMAC master)	8-byte read/write 16-byte read/write 32-byte read/write
USBHS0-DMAC register setting	4-byte read/write 8-byte read/write

The configuration of this module is shown below.

This module is provided with buffers and bus bridges and controls transfers between the SHwy bus and USB High-Speed module (USBHS0).

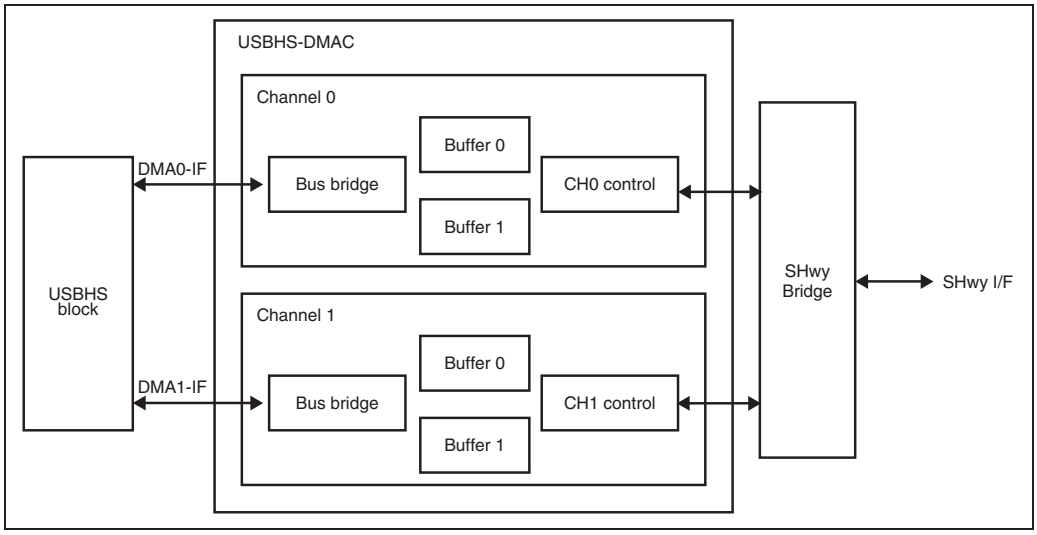


Figure 61.1 USBHS0-DMAC Configuration

61.2 Register Map

Table 61.3 shows the register configuration. Table 61.4 shows the register states in each processing mode.

Table 61.3 Register Configuration

Register Name	Abbreviation	R/W	Address	Access Size
VCR register	USBDMA_VCR	R/W	USBDMA_BASE+H'00	32
Software reset register	USBDMA_SWR	R/W	USBDMA_BASE+H'08	32
DMA interrupt source register	USBDMA_DMICR	R	USBDMA_BASE+H'10	32
DMA source address register_0	USBDMA_SAR_0	R/W	USBDMA_BASE+H'20	32
DMA destination address register_0	USBDMA_DAR_0	R/W	USBDMA_BASE+H'24	32
DMA transfer count register_0	USBDMA_TCR_0	R/W	USBDMA_BASE+H'28	32
DMA timeout count register_0	USBDMA_TOCNTR_0	R	USBDMA_BASE+H'2C	32
DMA timeout constant register_0	USBDMA_TOCSTR_0	R/W	USBDMA_BASE+H'30	32
DMA channel control register_0	USBDMA_CHCR_0	R/W	USBDMA_BASE+H'34	32
DMA final transaction valid data transfer enable register_0	USBDMA_TEND_0	R/W	USBDMA_BASE+H'38	32
DMA source address register_1	USBDMA_SAR_1	R/W	USBDMA_BASE+H'40	32
DMA destination address register_1	USBDMA_DAR_1	R/W	USBDMA_BASE+H'44	32
DMA transfer count register_1	USBDMA_TCR_1	R/W	USBDMA_BASE+H'48	32
DMA timeout count register_1	USBDMA_TOCNTR_1	R	USBDMA_BASE+H'4C	32
DMA timeout constant register_1	USBDMA_TOCSTR_1	R/W	USBDMA_BASE+H'50	32
DMA channel control register_1	USBDMA_CHCR_1	R/W	USBDMA_BASE+H'54	32
DMA final transaction valid data transfer enable register_1	USBDMA_TEND_1	R/W	USBDMA_BASE+H'58	32
DMA operation register	USBDMA_DMAOR	R/W	USBDMA_BASE+H'60	32

Note: USBDMA_BASE=H'E68A0000

Table 61.4 Register States in Each Processing Mode

Register Abbreviation	Power-On Reset	Software Standby	Module Standby	Sleep
USBDMA_VCR	Initialized	Retained	Retained	Retained
USBDMA_SWR	Initialized	Retained	Retained	Retained
USBDMA_DMICR	Initialized	Retained	Retained	Retained
USBDMA_SAR_0	Initialized	Retained	Retained	Retained
USBDMA_DAR_0	Initialized	Retained	Retained	Retained
USBDMA_TCR_0	Initialized	Retained	Retained	Retained
USBDMA_TOCNTR_0	Initialized	Retained	Retained	Retained
USBDMA_TOCSTR_0	Initialized	Retained	Retained	Retained
USBDMA_CHCR_0	Initialized	Retained	Retained	Retained
USBDMA_TEND_0	Initialized	Retained	Retained	Retained
USBDMA_SAR_1	Initialized	Retained	Retained	Retained
USBDMA_DAR_1	Initialized	Retained	Retained	Retained
USBDMA_TCR_1	Initialized	Retained	Retained	Retained
USBDMA_TOCNTR_1	Initialized	Retained	Retained	Retained
USBDMA_TOCSTR_1	Initialized	Retained	Retained	Retained
USBDMA_CHCR_1	Initialized	Retained	Retained	Retained
USBDMA_TEND_1	Initialized	Retained	Retained	Retained
USBDMA_DMAOR	Initialized	Retained	Retained	Retained

61.2.1 VCR Register (USBDMA_VCR)

[Address=USBDMA_BASE+H'00]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ERR_SNT	ERR_RCV
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	ERR_SNT	0	R/W	Send Error Response 0: No error is generated. [Clearing condition] Writing 0 after reading 1. 1: An error is generated.
0	ERR_RCV	0	R/W	Receive Error Response 0: No error is generated. [Clearing condition] Writing 0 after reading 1. 1: An error is generated.

61.2.2 Software Reset Register (USBDMA_SWR)

[Address=USBDMA_BASE+H'08]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SWR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	SWR	0	R/W	Software Reset 0: Cancels reset. 1: Resets entire system. Note: On software reset, this bit should be held high for long enough until the internal circuit stabilizes. When this bit is set to 1, it is recommended to allow several tens of clocks if operating at 130MHz for a reset period before clearing the reset (setting this bit to 0) as a precaution.

61.2.3 DMA Interrupt Source Register (USBDMA_DMICR)

[Address=USBDMA_BASE+H'10]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SH BSY1	—	—	—	—	—	—	—	SH BSY0	—	—	—	—	—	—	AE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	TR1	BUF1	RW1	NULL1	TO1	SP1	TE1	—	TR0	BUF0	RW0	NULL0	TO0	SP0	TE0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	SHBSY1	0	R	CH1 SHwy Bus Busy Flag Monitor 0: The SHwy bus is idle. 1: The SHwy bus is busy.
30 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23	SHBSY0	0	R	CH0 SHwy Bus Busy Flag Monitor 0: The SHwy bus is idle. 1: The SHwy bus is busy.
22 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	AE	0	R	Address Error Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (AE in the DMA operation register is reflected.)
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
14	TR1	0	R	CH1 Transaction End: Receive Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (TR in the channel 1 control register is reflected.)
13	BUF1	0	R	CH1 Buffer End Detect Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (BUF in the channel 1 control register is reflected.)
12	RW1	0	R	CH1 Final Buffer Access Detect Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (RW in the channel 1 control register is reflected.)
11	NULL1	0	R	CH1 NULL Packet Receive Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (NULL in the channel 1 control register is reflected.)
10	TO1	0	R	CH1 Timeout Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (TO in the channel 1 control register is reflected.)
9	SP1	0	R	CH1 Short Packet Receive Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (SP in the channel 1 control register is reflected.)
8	TE1	0	R	CH1 Transfer End Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (TE in the channel 1 control register is reflected.)
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
6	TR0	0	R	CH0 Transaction End Detect Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (TR in the channel 0 control register is reflected.)
5	BUF0	0	R	CH0 Buffer End Detect Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (BUF in the channel 0 control register is reflected.)
4	RW0	0	R	CH0 RWEND Receive Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (RW in the channel 0 control register is reflected.)
3	NULL0	0	R	CH0 NULL Receive Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (NULL in the channel 0 control register is reflected.)
2	TO0	0	R	CH0 Timeout Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (TO in the channel 0 control register is reflected.)
1	SP0	0	R	CH0 Short Packet Receive Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (SP in the channel 0 control register is reflected.)
0	TE0	0	R	CH0 Transfer End Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (TE in the channel 0 control register is reflected.)

61.2.4 DMA Source Address Register_0 to 1 (USBDMA_SAR_0 to 1)

[Address=USBDMA_BASE+H'20,H'40]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SAR[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SAR[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	SAR31 to SAR0	All 0	R/W	Source Address (0x00000000 to 0xFFFFFFFF (4 Gbytes)) Set a value of 8-byte, 16-byte, or 32-byte boundary. Indicate the next transfer source address during a DMA transfer.

61.2.5 DMA Destination Address Register_0 to 1 (USBDMA_DAR_0 to 1)

[Address=USBDMA_BASE+H'24,H'44]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DAR[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DAR[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DAR31 to DAR0	All 0	R/W	Destination Address (0x00000000 to 0xFFFFFFFF (4 Gbytes)) Set a value of 8-byte, 16-byte, or 32-byte boundary. Indicate the next transfer destination address during a DMA transfer.

61.2.6 DMA Transfer Count Register_0 to 1 (USBDMA_TCR_0 to 1)

[Address=USBDMA_BASE+H'28,H'48]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	TCR[23:16]							
Initial value:	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TCR[15:0]															
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	TCR23 to TCR0	H'FF FFFF*	R/W	Transfer Count • When 0x000001 is set, total transfer volume is as follows: Transfer size = 32 bytes: 32 × 1 bytes Transfer size = 16 bytes: 16 × 1 bytes Transfer size = 8 bytes: 8 × 1 bytes • When 0xFFFFFF is set, 16,777,215 times • When 0x000000 is set, 16,777,216 times (maximum) • Indicate 0 when a DMA transfer completes successfully.

Note: * To read this register, read the internal transfer counter value (the TCR counter value) directly. This register is read as all 1 after a reset is cleared because the initial value of the TCR counter is all 1 (0xFFFFFF). When DMA is enabled (DE in DMACHCR is asserted), the TCR counter is loaded with the value set in this register and decrements during DMA transfers. This means that the remaining transfer count is read back. Note that the read value may be different from the one set in this register due to this reason.

61.2.7 DMA Timeout Count Register_0 to 1 (USBDMA_TOCNTR_0 to 1)

[Address=USBDMA_BASE+H'2C,H'4C]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	TOCNTR[21:16]					
Initial value:	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TOCNTR[15:0]															
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
21 to 0	TOCNTR21 to TOCNTR0	H'3F FFFF	R	Timeout Counter Value (0x000000 to 0x27AC40) Indicate the remaining timeout count during timeout counting. (Countable up to 0x3FFFFF (approximately 32 ms) by the hardware. See the TOCSTR register.)

61.2.8 DMA Timeout Constant Register_0 to 1 (USBDMA_TOCSTR_0 to 1)

[Address=USBDMA_BASE+H'30,H'50]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	TOCSTR[21:16]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TOCSTR[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
21 to 0	TOCSTR21 to TOCSTR0	H'00 0000	R/W	Timeout Constant Value (0x000000 to 0x27AC40) Sst a timeout value (at 130 MHz cycle). The maximum timeout time is approximately 20 ms. (Setting up to 0x3FFFFF (approximately 32 ms) is allowed by the hardware.)

61.2.9 DMA Channel Control Register_0 to 1 (USBDMA_CHCR_0 to 1)

[Address=USBDMA_BASE+H'34,H'54]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	FTE	—	—	—	SPIM	TRE	BUFE	RWE	NULLE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TR	BUF	RW	NULL	PRI[3:0]				TS[1:0]		IE	TOE	TO	SP	TE	DE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W*	R/W*	R/W*	R/W*	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W*	R/W*	R/W*	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	FTE	0	(R)/W	Forced TE Set Register When a NULL packet is received, the TE bit is forced to 1 to terminate the transfer by setting 1 in this register. (The DREQE bit of the UDSB-IP should also be controlled accordingly. For details on the control procedure and restrictions, see section 61.3.2(3).) This bit is always read as 0. 0: No effect (nothing happens). 1: Forces the TE bit to 1.
23 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	SPIM	0	R/W	Short Packet Receive Interrupt Mask Enables or disables the reflection of the short packet (SP) receive flag in the interrupt signal. If this bit is set to 1, no interrupts are generated when an SP is received. However, the SP receive flag (the SP bit) is set regardless of this register setting. 0: The short packet receive interrupt is enabled (default). 1: The short packet receive interrupt is disabled.

Bit	Bit Name	Initial Value	R/W	Description
19	TRE	0	R/W	Transaction End Detect Interrupt Flag Enable Enables or disables the reflection of TR in the interrupt signal and the DMA stop/restart control. (When this bit is set to 0, the TR bit is always 0.) 0: The TR flag is disabled. 1: The TR flag is enabled.
18	BUFE	0	R/W	Buffer End Detect Interrupt Flag Enable Enables or disables the reflection of BUF in the interrupt signal and the DMA stop/restart control. (When this bit is set to 0, the BUF bit is always 0.) 0: The BUF flag is disabled. 1: The BUF flag is enabled.
17	RWE	0	R/W	Final Buffer Access Detect Interrupt Flag Enable Enables or disables the reflection of RW in the interrupt signal and the DMA stop/restart control. (When this bit is set to 0, the RW bit is always 0.) 0: The RW flag is disabled. 1: The RW flag is enabled.
16	NULLE	0	R/W	NULL Receive Interrupt Flag Enable Enables or disables the reflection of the NULL receive interrupt flag (NULL) in the interrupt signal. 0: The NULL receive interrupt flag is disabled. 1: The NULL receive interrupt flag is enabled.
15	TR	0	R/W*	Transaction End Detect Interrupt Flag When the transaction end is detected, an interrupt is generated. 0: DMA transfer is in progress or suspended. [Clearing condition] Writing 0 after reading 1. 1: An transaction end receive interrupt is generated.

Bit	Bit Name	Initial Value	R/W	Description
14	BUF	0	R/W*	Buffer End Detect Interrupt Flag When the end of the buffer is detected, an interrupt is generated. 0: DMA transfer is in progress or suspended. [Clearing condition] Writing 0 after reading 1. 1: A buffer end detect interrupt is generated.
13	RW	0	R/W*	Final Buffer Access Detect Interrupt Flag When the final access to the buffer is detected, an interrupt is generated. 0: DMA transfer is in progress or suspended. [Clearing condition] Writing 0 after reading 1. 1: A final buffer access detect interrupt is generated.
12	NULL	0	R/W*	NULL Receive Interrupt Flag When NULL packet is received, an interrupt is generated. 0: DMA transfer is in progress or suspended. [Clearing condition] Writing 0 after reading 1. 1: A NULL packet receive interrupt is generated.
11 to 8	PRI3 to PRI0	All 0	R/W	Priority Set the value of the priority signal to be output to the SHwy bus. 0000: Priority 0 (lowest) 0001: Priority 1 : 1111: Priority 15 (highest)

Bit	Bit Name	Initial Value	R/W	Description
7, 6	TS1 to TS0	00	R/W	MA Transfer Size 00: 8 bytes 01: 16 bytes 10: 32 bytes 11: Setting prohibited Specify the same transfer size and address boundary when setting addresses in DMASAR and DMADAR as a transfer source and transfer destination. If TS = 11 is set, an address error is generated and DMA transfer is disabled.
5	IE	0	R/W	Interrupt Enable Enables or disables an interrupt request to the CPU when DMA transfer ends. When AE, TE, SP, TO, NULL, RW, BUF, or TR bit is set with this bit set to 1, an interrupt request is output to the CPU. However, when the TRE, BUFE, RWE, NULLE, or TOE bit is set to disabled, no interrupt due to TR, BUF, RW, NULL, or TO is generated. 0: An interrupt request is disabled. 1: An interrupt request is enabled.
4	TOE	0	R/W	Timeout Enable Enables or disables the reflection of the timeout flag (TO) in the interrupt. 0: Timeout flag is disabled. 1: Timeout flag is enabled.
3	TO	0	R/W*	Timeout Flag After a transfer request REQ is negated, a timeout interrupt is generated after the specified cycles. (Used for timeout when the final packet is Max packet.) 0: DMA transfer is in progress or suspended. [Clearing condition] Writing 0 after reading 1. 1: Timeout is generated.

Bit	Bit Name	Initial Value	R/W	Description
2	SP	0	R/W*	Short Packet Receive Flag A transfer end interrupt is generated upon receiving a short packet from the USB-IP. For example, if DMA transfer size is set to 1 MB but actual data transfer is 900 KB, this interrupt is generated when transfer of 900 KB finishes. 0: DMA transfer is in progress or suspended. [Clearing condition] Writing 0 after reading 1. 1: A short packet is received.
1	TE	0	R/W*	Transfer End Flag When a DMA transfer ends with DMATCR = 0, the TE bit is set to 1. When a DMA address error occurs before DMATCR is cleared to 0 and the transfer is suspended by clearing the DE bit and the DME bit in DMAOR, the TE bit is not set to 1. To clear the TE bit, write 0 after reading 1.When TE = 1, DMA transfer is disabled even if the DE bit is set to 1. 0: DMA transfer is in progress or suspended. [Clearing condition] Writing 0 after reading 1. 1: DMA transfer end (TCR = 0)
0	DE	0	R/W	DMA Enable Enables or disables DMA transfer. Setting the DME bit in DMAOR and the DE bit for the corresponding channel to 1 starts a DMA transfer, provided that all interrupt flags are 0. Clearing the DE bit to 0 suspends the ongoing transfer after the transfer of one transaction is completed. 0: DMA transfer is disabled. 1: DMA transfer is enabled.

Note: * Only writing 0 to clear the flag is enabled.

61.2.10 DMA Final Transaction Valid Data Transfer Enable Register_0 to 1 (USBDMA_TEND_0 to 1)

[Address=USBDMA_BASE+H'38,H'58]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	EDTEN[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EDTEN[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	EDTEN31 to EDTEN0	H'00000000	R/W	Final Transaction Valid Data Transfer Enable (valid only for IN transfers) Specify valid data size in units of bytes in the final transaction of data transfer. (See section 61.3.2) 0x80000000: 32 bytes × (n-1) + 1 byte 0xC0000000: 32 bytes × (n-1) + 2 bytes : 0xFFFFFFFF: 32 bytes × (n-1) + 32 bytes Notes: 1. n: Transfer count setting (TCR) 2. For the 8-byte transfer, set EDTEN23 to EDTEN0 to 0. For the 16-byte transfer, set EDTEN15 to EDTEN0 to 0.

61.2.11 DMA Operation Register (USBDMA_DMAOR)

[Address=USBDMA_BASE+H'60]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	TID[1:0]		RM	PR[1:0]		AE	DME
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W*	R/W*	R/W	R/W	R/W	R/W*	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6, 5	TID1 and TID0	00	R/W*	Response Error Channel Identity Information TID1 indicates the channel 1 error information, and TID0 indicates the channel 0 error information. TID1 0: No error 1: Channel 1 response packet error TID0 0: No error 1: Channel 0 response packet error [Setting condition] When a CH0 (1) response error occurs [Clearing condition] Clearing ERR_RCV in VCR (Channel 0/channel 1 concurrent clear)
4	RM	0	R/W	Response Error Mask Mode 0: A response error is output. 1: A response error is masked.

Bit	Bit Name	Initial Value	R/W	Description
3, 2	PR1 to PR0	All 0	R/W	Priority Mode Specify the priority of channels to execute transactions when transfer requests are made simultaneously in both channel 0 and channel 1 as follows: 00: Channel 0 > Channel 1 01: Channel 1 > Channel 0 10: Setting prohibited (If PR = 10 is set, channel 0 > channel 1) 11: Round-robin mode
1	AE	0	R/W*	Address Error Flag Indicates that an address error interrupt occurred when setting SAR or DAR. This flag is set to 1 when the value of SAR or DAR differs from the transfer size (TS) boundary, and when the TS bits are set to 11 (setting prohibited). When the AE bit is set to 1, DMA transfer is not enabled even if the DE bit in DMACHCR and the DME bit in DMAOR are set to 1. 0: No address error interrupt is generated by the DMAC. [Clearing condition] Setting SAR and DAR to values that match the transfer size boundary. 1: An address error interrupt is generated.
0	DME	0	R/W	DMA Master Enable Enables or disables DMA transfers for all channels. When the DME bit and the DE bit in USBDMA_CHCR are set to 1, DMA transfer is enabled, provided that all interrupt flags in USBDMA_CHCR of the transfer channel are 0. Clearing the DME bit suspends the DMA transfer for all channels. 0: DMA transfer for all channels is disabled. 1: DMA transfer for all channels is enabled.

Note: * Only writing 0 to clear the flag is enabled.

61.3 Operation

61.3.1 Interrupt/Error Detection Function

This section describes the interrupt/error detection function that is implemented in this module.

Table 61.5 lists the mask, source, and flag registers for each interrupt type.

Table 61.5 Registers by Interrupts/Errors

	Interrupt Generation	Interrupt Mask Register	Interrupt Mask Register (Individual Mask)	Source Register	Flag Register
Transfer count end	O	CHCR_x.IE	—	DMICR.TEx	CHCR_x.TE
Short packet receive	O	CHCR_x.IE	CHCR_x.SPIM	DMICR.SPx	CHCR_x.SP
NULL packet receive	O	CHCR_x.IE	CHCR_x.NULLE	DMICR.NULLx	CHCR_x.NULL
Timeout	O	CHCR_x.IE	CHCR_x.TOE	DMICR.TOx	CHCR_x.TO
Transaction end detect	O	CHCR_x.IE	CHCR_x.TRE*	DMICR.TRx	CHCR_x.TR
Buffer end detect	O	CHCR_x.IE	CHCR_x.BUFE*	DMICR.BUFx	CHCR_x.BUF
Final buffer access detect	O	CHCR_x.IE	CHCR_x.RWE※	DMICR.RWx	CHCR_x.RW
Address error	O	CHCR_x.IE	—	DMICR.AE	DMAOR.AE
Response packet error	—	—	—	—	VCR.ERR_SNT VCR.ERR_RCV

Note: These registers not only mask interrupt generation but also disable error processing (flag sources and flag clearing).

Table 61.6 shows the processing to be executed when different interrupts occur. DMA transfer control is not affected when the NULL packet receive, timeout, or response packet error interrupt occurs. When the transfer count end interrupt occurs, processing is restarted. Processing can be resumed or restarted after interrupts occur from other sources.

Table 61.6 Processing to be Executed When Interrupts Occur (Suspend/Resume/Restart)

	Suspend/ Resume	Terminate/ Restart	Suspend/Resume/Restart Control Mask Register
Transfer count end	—	o	—
Short packet receive	O	O	—
NULL packet receive	—	O*	—
Timeout	—	O	—
Transaction end detect	O	O	CHCR_x.TRE
Buffer end detect	O	O	CHCR_x.BUFE
Final buffer access detect	O	O	CHCR_x.RWE
Address error	O	O	—
Response packet error	—	—	—

The internal circuit is reloaded register values when restarted, but not when resumed.

* When a NULL packet is received, processing is forced to be terminated and restarted by the FTE register (see section 61.3.2 (3)).

Table 61.7 lists the interrupt generating conditions.

Table 61.7 Interrupt Generating Conditions

Interrupt Name	Interrupt Conditions
Transfer count end interrupt	When the final data transfer of the specified transfer count (in the TCR register) completes IN transfer: When the final access to USB-IP completes OUT transfer: When the data transmission to the SHwy completes
Short packet receive interrupt	When the data transfer at the time the end of a transaction is detected completes
NULL packet receive interrupt	When a NULL packet is detected or the forced TE register is set
Timeout interrupt	When the specified time elapses after the last transfer request
Transaction end detect interrupt	When the end of a transaction is detected
Buffer end detect interrupt	When the end of the buffer is detected
Final buffer access detect interrupt	When the final access to the buffer is detected
Address error interrupt	When invalid access to the DMAC register is attempted (With invalid SAR/DAR values or invalid transfer size (TS) specified)
Response packet error	Error Transmission (err_snt) When accessed by a transaction that is not supported Error Reception (err_rcv) When received a response packet error from the system

Figure 61.2 shows a block diagram of the interrupt circuit.

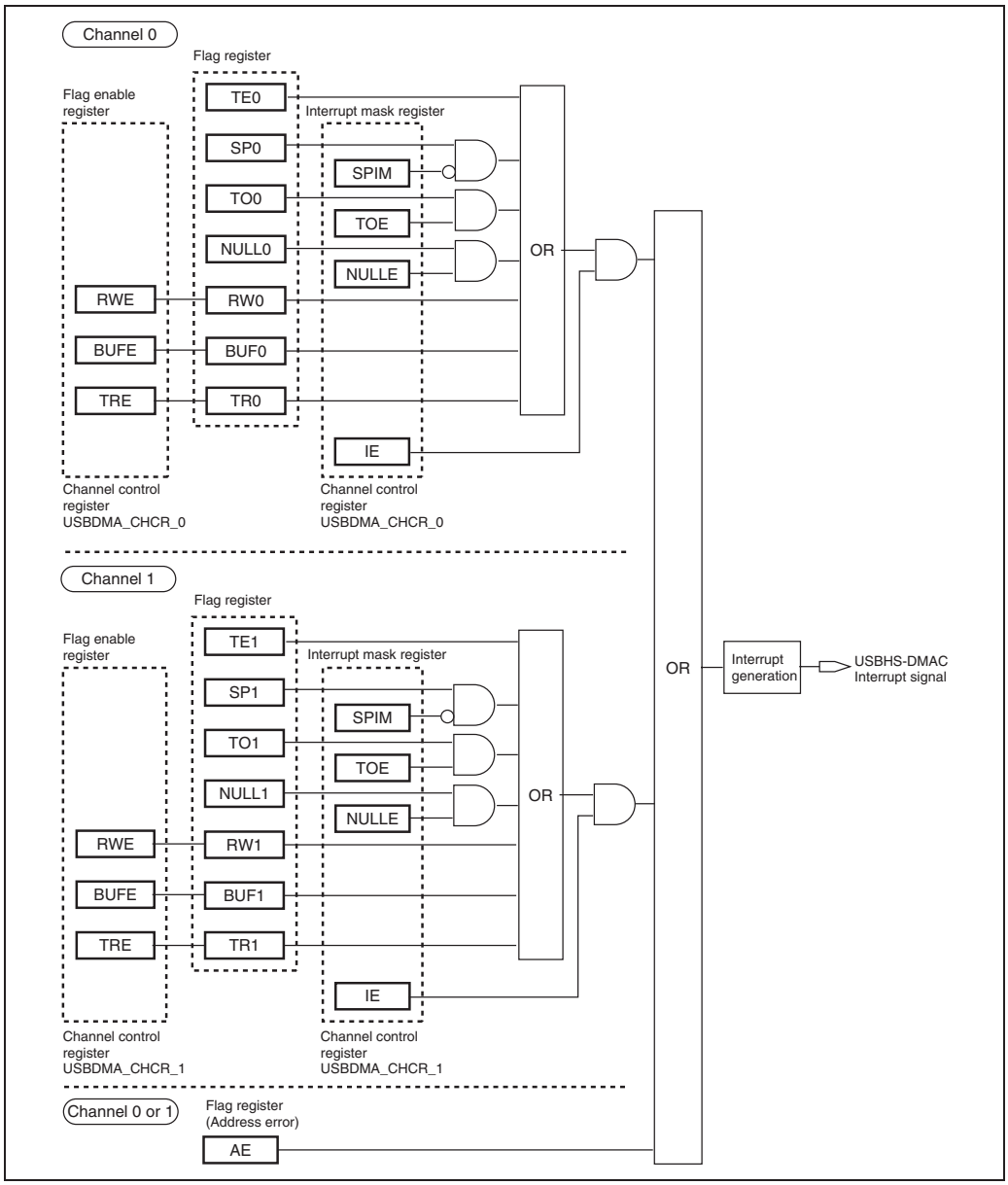


Figure 61.2 Block Diagram of Interrupt Circuit

(1) Transfer Count Ed Interrupt (TE Flag)

Can be generated when the specified number of transfers complete or the FTE bit in the channel control register (USBDMA_CHCR_0 to USBDMA_CHCR_1) is set to 1. When the IE bit in the USBDMA_CHCR_0 to USBDMA_CHCR_1 is set to 0, no interrupts are generated. However, the TE bit in USBDMA_CHCR_0 to USBDMA_CHCR_1 and the TE0 or TE1 bit in the interrupt source register (USBDMA_DMICR) are set to 1 regardless of the IE bit setting.

The internal transfer counter is loaded with the value set in the USBDMA_TCR_x register and decrements based on the SHwy clock every time one transaction (8-/16-/32-byte) completes. When the transfer count value reaches 0 (the end of a transfer count), the counter sets the TE (transfer end) flag from 0 to 1 (when the FTE bit is set, it is reflected on the TE flag immediately). The TE bit is cleared by writing 0 to it after reading it as 1 by software.

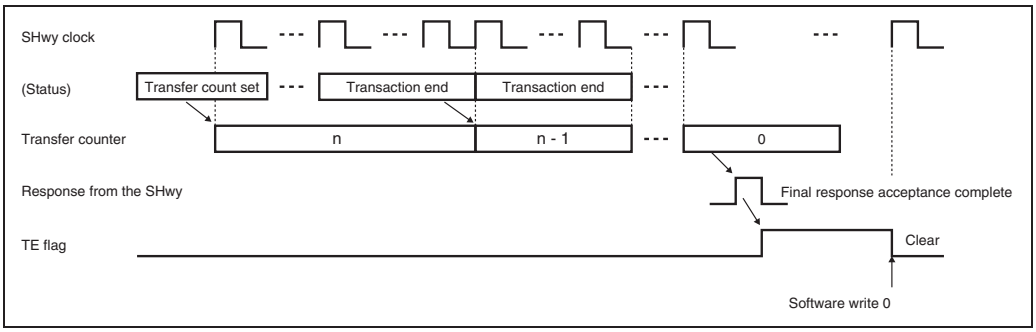


Figure 61.3 Transfer Count End Interrupt (TE) Generation Timing

(2) Short packet receive interrupt (SP flag)

Can be generated when a short packet is detected. When the SPIM bit in the USBDMA_CHCR_x register is set to 1, no interrupts are generated. However, the SP bit (SP flag) in the USBDMA_CHCR_x register and the SP0 or SP1 bit in the USBDMA_DMICR register are set to 1, regardless of the SPIM bit setting. The SP bit is cleared by writing 0 to it after reading it as 1 by software.

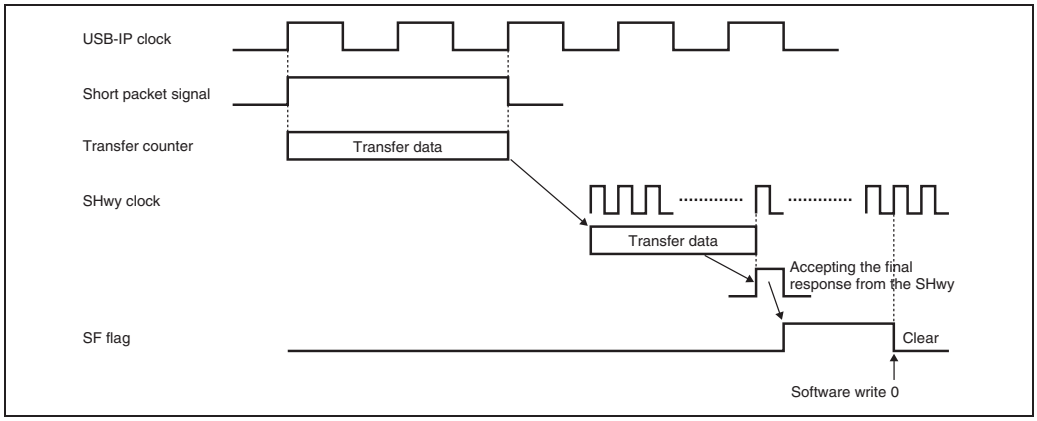


Figure 61.4 Short Packet Receive Interrupt (SP) Generation Timing

(3) NULL packet receive interrupt (NULL flag)

Can be generated when a NULL packet is detected. When the NULLE bit in the USBDMA_CHCR_x register is set to 0, no interrupts are generated. However, the NULL bit (NULL flag) in the USBDMA_CHCR_x register and the NULL0 or NULL1 bit in the USBDMA_DMICR register are set to 1, regardless of the NULLE bit setting. Note also that the DMA transfer control in this module, such as stop, suspend, or resume, is not affected when a NULL packet is received. The software is responsible for implementing special processing if necessary since in this module this interrupt is designed only to signal the software that a NULL packet is received.

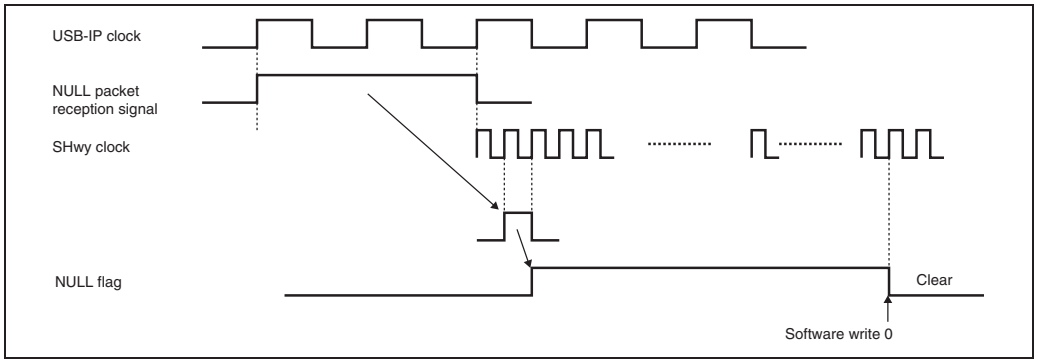


Figure 61.5 NULL Packet Receive Interrupt (NULL) Generation Timing

(4) Timeout interrupt (TO flag)

Can be generated when the time period that is specified in the timeout constant register (USBDMA_TOCSTR_0 or USBDMA_TOCSTR_1) elapses after the final transfer request is received from the USB-IP. On detecting the final transfer request, the internal counter is loaded with the value set in the USBDMA_TOCSTR_x register and starts counting down. When the counter reaches 0, it generates a timeout interrupt. Note that the DMA transfer control in this module, such as stop, suspend, or resume, is not affected when a timeout interrupt occurs. The TO bit is cleared by writing 0 to it after reading it as 1 by software. Figure 61.6 and 61.7 show the timeout interrupt generation timing.

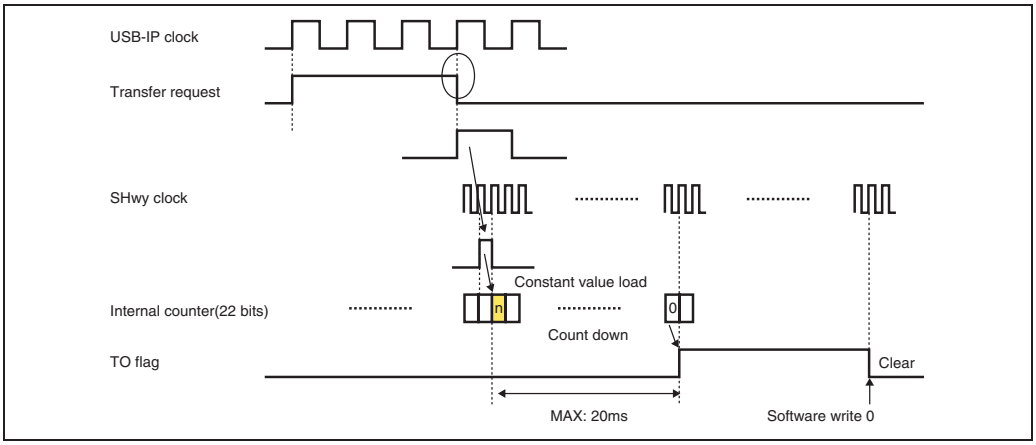


Figure 61.6 Timeout Interrupt (TO) Generation Timing

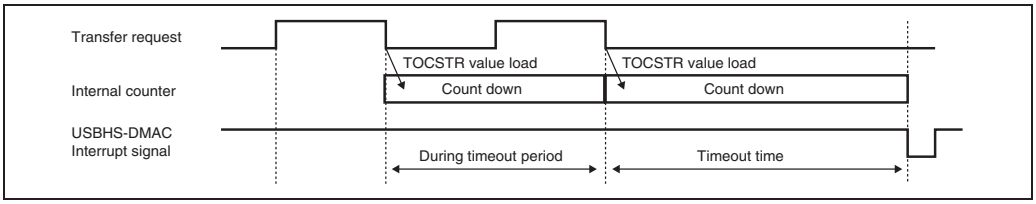


Figure 61.7 Timeout Interrupt Timing

The functions described in 61.3.1(5) to 61.3.1(9) are added to detect and notify the transitions on an individual signal line to the software, but no use is defined. They can be used as required.

(5) Transaction end detect interrupt (TR flag)

Can be generated when the end of a transaction is detected within the USB-IP. Note that the TR bit in the USBDMA_CHCR_x register and the TR0 or TR1 bit in the USBDMA_DMICR register are not reflected in the interrupt signal when the TRE bit in the USBDMA_CHCR_x register is set to 0.

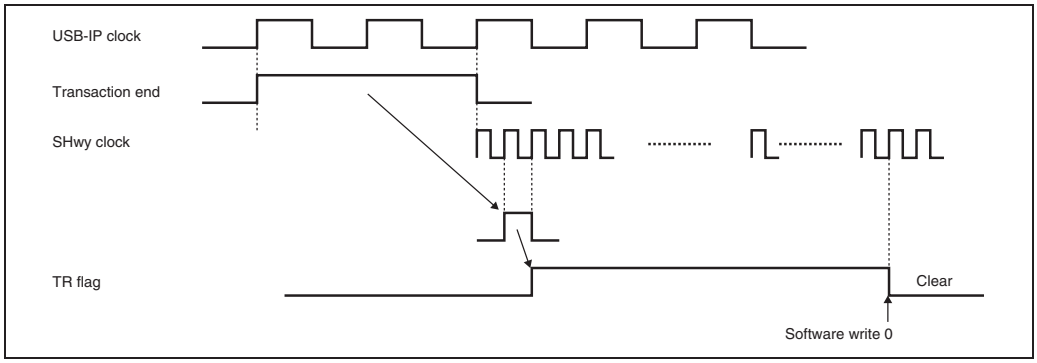


Figure 61.8 Transaction End Detect Interrupt Timing

(6) Buffer end detect interrupt (BUF flag)

Can be generated when the end of the buffer in the USB-IP is detected. Note that the BUF bit in the USBDMA_CHCR_x register and the BUF0 or BUF1 bit in the USBDMA_DMICR register are not reflected in the interrupt signal when the BUFE bit in the USBDMA_CHCR_x register is set to 0.

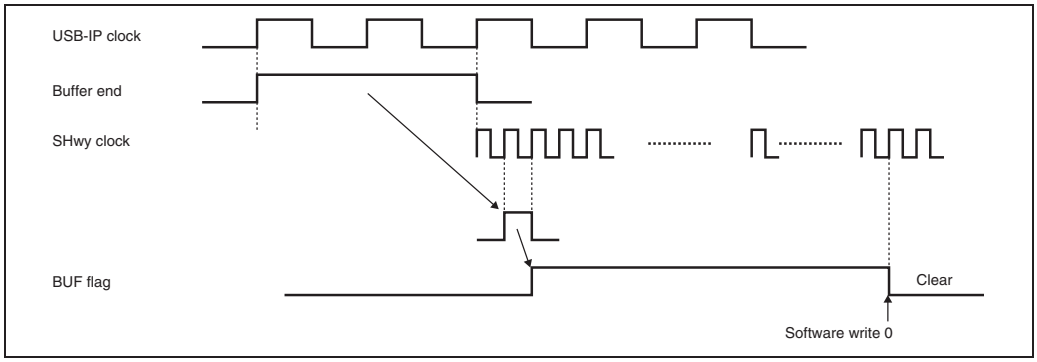


Figure 61.9 Buffer End Detect Interrupt Timing

(7) Final buffer access detect interrupt (RW flag)

Can be generated when the final access to the buffer in the USB-IP is detected. Note that the RW bit in the USBDMA_CHCR_x register and the RW0 or RW1 bit in the USBDMA_DMICR register are not reflected in the interrupt signal when the RWE bit in the USBDMA_CHCR_x register is set to 0.

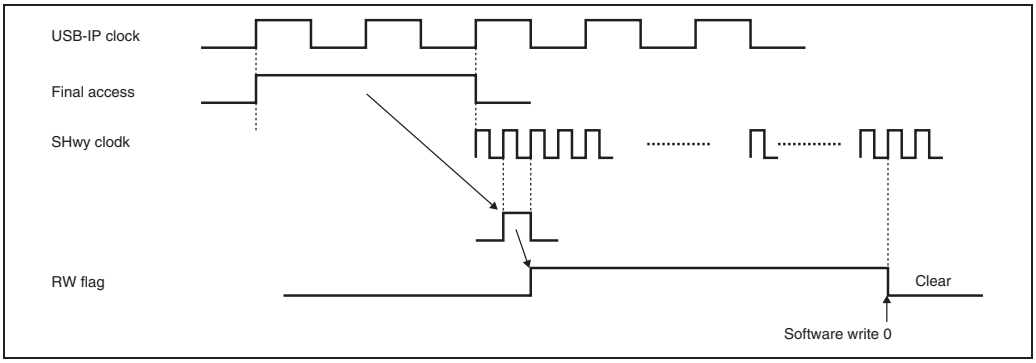


Figure 61.10 Final Buffer Access Detect Interrupt Timing

(8) Address error detection

This is a flag that indicates an address error interrupts has occurred when setting the source address register (USBDMA_SAR0 to USBDMA_SAR1) and the destination address register (USBDMA_DAR0 to USBDMA_DAR1). When the value written to the USBDMA_SAR or USBDMA_DAR register differs from the transfer size (TS) boundary, and when the TS bits are set to 11 (setting prohibited), the AE bit in the USBDMA_DMAOR register is set to 1. There is no distinction between CH0 and CH1 for an address error (the AE bit is set to 1 when an address error occurs on CH0 or CH1).

While the AE is set, no DMA transfer is allowed even if the DE bit in the USBDMA_CHCR_x register and the DME bit in the USBDMA_DMAOR register are set to 1. The address error interrupt is cleared by setting correct addresses in USBDMA_SAR_x and USBDMA_DAR_x.

Table 61.8 Address Error Detection Conditions When Setting Transfer Sizes

Transfer Size	Address Error Detection Conditions
TS=00 (8-byte transfer)	When data that is not aligned to 8-byte boundaries is written to the SAR/DAR registers (Writes to the SAR/DAR registers are valid.)
TS=01 (16-byte transfer)	When data that is not aligned to 16-byte boundaries is written to the SAR/DAR registers (Writes to the SAR/DAR registers are valid.)
TS=10 (32-byte transfer)	When data that is not aligned to 32-byte boundaries is written to the SAR/DAR registers (Writes to the SAR/DAR registers are valid.)
—	When b'11 (setting prohibited) is written to the TS register (Writes to the TS register are valid.)

(9) Response packet error detection

This function reports response packet errors when the interface between the SHwy and this module is accessed in ways that are not listed in table 61.2.

(a) Transmitting response packet errors

When a response packet error occurs during accessing from the SHwy to this module, the err_snt bit in the USBDMA_VCR register is set to 1.* The error signal is also sent to the SHwy bus if the RM bit in the USBDMA_DMAOR register is 0. If the RM bit is set to 1, the error signal is masked (0 is signaled).

Note: When a response packet error occurs, the err_snt bit is set to 1 regardless of the RM bit setting. The err_snt bit is cleared by writing 0 after reading 1.

Table 61.9 Response Packet Error Generation

USBDMA_DMAOR (RM bit) Setting	1 (Mask Mode)	0 (Normal Mode)
Response packet error signal notification to SHwy	Signals the fixed value (0) to the SHwy bus without determining if there is a response packet error.	Reports a response packet error to the SHwy bus when its is accessed with a transfer size other than those supported in this module (4-byte read/write and 8-byte read).

(b) Receiving response packet errors

When a response packet error occurs during accessing from this module to the SHwy, the err_rcv bit in the USBDMA_VCR register is set to 1. The TID bit in the USBDMA_DMAOR register indicates on which channel of this module the error has occurred (TID[1]=1 means it has occurred on CH1 and TID[0]=1 on CH0).

The err_rcv bit is cleared by writing 0 after reading 1.

61.3.2 DMA Transfer Function

(1) Operating mode

The following operating modes (1) to (3) are supported according to the setting of the PR bit in the DMA operation register (USBDMA_DMAOR).

(a) CH0 first control

Forces CH1 to wait to start a DMA transfer until a DMA transfer completes on CH0.

When there is a timing conflict in starting a DMA transfer between CH0 and CH1, CH0 takes precedence over CH1. If a DMA transfer is in progress on CH1 when CH0 tries to start a DMA transfer, CH0 waits to start it until the ongoing DMA transfer completes on CH1.

(b) CH1 first control

Forces CH0 to wait to start a DMA transfer until a DMA transfer completes on CH1.

When there is a timing conflict in starting a DMA transfer between CH1 and CH0, CH1 takes precedence over CH0. If a DMA transfer is in progress on CH0 when CH1 tries to start a DMA transfer, CH1 waits to start it until the ongoing DMA transfer completes on CH0.

(c) Round-robin control

Assigns the lowest priority to the last channel that has completed a transfer. In the initial state, CH0 takes precedence over CH1.

When there is a timing conflict in starting a DMA transfer between CH0 and CH1, the channel with a higher priority is granted to start the transfer and the lower priority channel is forced to wait. If a DMA transfer is in progress on the lower priority channel when the higher priority channel tries to start a DMA transfer, the higher priority channel waits to start it until the ongoing DMA transfer completes on the lower priority channel.

Figure 61.11 shows an overview of the processing of the SHwy bridge in each operating mode.

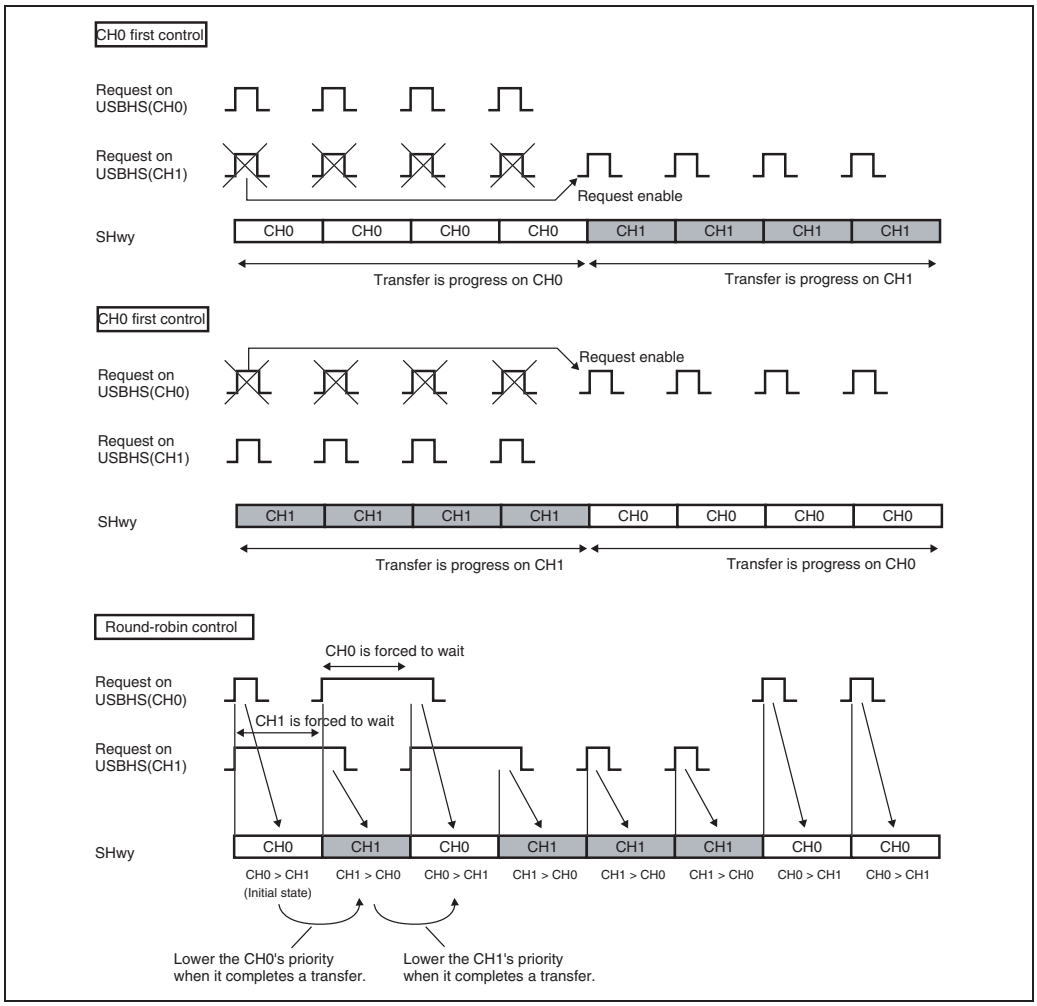


Figure 61.11 Overview of SHwy Bridge Processing in Each Mode

(2) Transfer size

The transfer size on the SHwy can be selected by setting the channel control register (the TS bit).

8-, 16-, and 32-byte can be set for each channel independently.

The following consideration should be observed during IN transfers.

The minimum transfer size that can be set to the TS bit is 8 bytes while the USB-IP can control transfers in 1-byte units. For example, if valid transfer data that is "8 x (n-1) + α" (α is less than 7 bytes) in size is to be transferred to the USB-IP with the transfer size set to 8 bytes and the transfer count set to n, α is transferred as a valid transfer unit by controlling byte enables according to the DMA final transaction valid data transfer enable register (the EDTEN bits) setting. Likewise, data is transferred in "transfer size x transfer count" (the final transaction is controlled by EDTEN) for 16- and 32-byte transfer sizes. The EDTEN setting is valid only for IN transfer and is don't care for OUT transfer.

Figure 61.12 shows an example of EDTEN setting. When only EDTEN31 in EDTEN31 to EDTEN0 is 1 , one byte is enabled. When only EDTEN31 and EDTEN30 in EDTEN31 to EDTEN0 are 1 , two bytes are enabled. Therefore, the total transfer volumes in the example shown above are calculated as "(32 bytesx(n-1)) bytes+10 bytes" for 32-byte transfer, "(16 bytesx(n-1)) bytes+7 bytes" for 16-byte transfer, and "(8 bytesx(n-1)) bytes+2 bytes" for 8-byte transfer. EDTEN15 to EDTEN0 in 16-byte transfer, EDTEN23 to EDTEN0 in 8-byte transfer are invalid (their values are ignored).

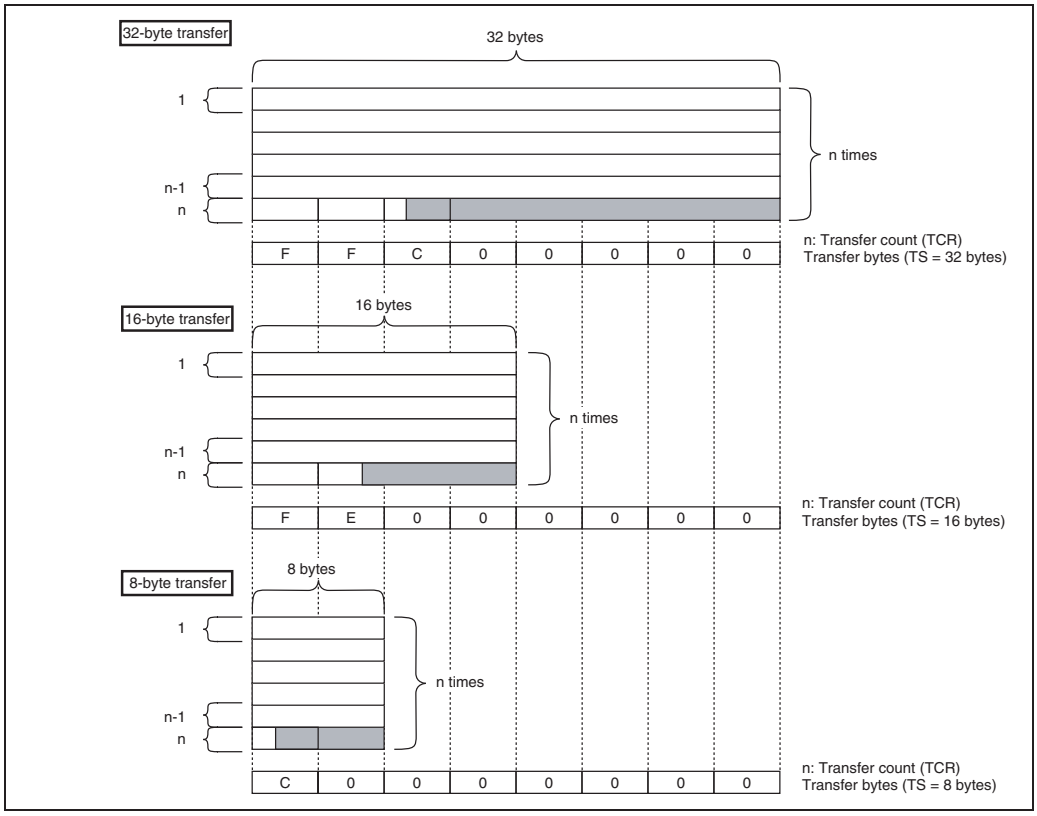


Figure 61.12 Example of Final Transaction Valid Data Transfer Enable (EDTEN) Setting

(3) DMA transfer flow

After the DMA source address register (USBDMA_SAR), DMA destination address register (USBDMA_DAR), DMA transfer count register (USBDMA_TCR), DMA channel control register (USBDMA_CHCR), final valid data transfer enable register (USBDMA_TEND), and DMA operation register (USBDMA_DMAOR) are set appropriately, the DMAC starts data transfer in the following sequence. The DMA timeout constant register (USBDMA_TOCSTR) may also need to be set.

If the transfer enabling conditions are set as DE=1, DME=1, TE=0, AE=0, SP=0, and (TR=0, BUF=0, RW=0), transfers are performed according to the transfer request enables and transfer requests from the USB-IP. The transfer direction (IN/OUT transfer) is determined by the direction signal from the USB-IP. The transfer size is determined by the setting of TS1 to TS0.

Every time one SHwy transaction (in the transfer size specified in the TS bit) completes, the internal counter of this module decrements the USBDMA_TCR value by one. When the specified transfer count ends (the USBDMA_TCR value reaches 0), it means all transfers complete. At this time, an USBHS0-DMAC interrupt is generated if the IE bit in the USBDMA_CHCR register is set to 1.

When a NULL packet is received, transfer can be stopped or restarted by setting FTE=1 after negating the DREQE register of the USBHS0 module. Follow the steps described later in "Control when a NULL packet is received".

Table 61.10 shows the conditions for each DMA transfer.

Table 61.10 DMA Transfer Conditions

Transfer enabling condition	TE=0, SP=0, (*TR=0, BUF=0, RW=0)
Transfer (starting) condition	When a transfer request is enabled by the USB-IP When a transfer request is issued by the USB-IP
Transfer completing (then restarting) condition	When the transfer count ends (the TE flag is set to 1), (can be restarted by setting DE and DME to 1.) When FTE=1 (when DREQE=1 in the USBHS0 module is also set), and the steps described later should be followed. When reset (can enter into standby state by releasing the reset.)
Transfer suspending (then resuming) condition	When DE=0 or DME=0 (can be resumed by setting DE=1 or DME=1.) When SP=1 (can be resumed by clearing the SP flag.) When RW=1, BUF=1, and TR=1 (can be resumed by clearing the RW, BUF, and TR flag.)* When the module stops (can be resumed by resuming the module.)

Note: * Can be ignored when the RWE, BUFE, and TRE registers are disabled (set to 0).

Figure 61.13 illustrates the high-level DMA transfer flow.

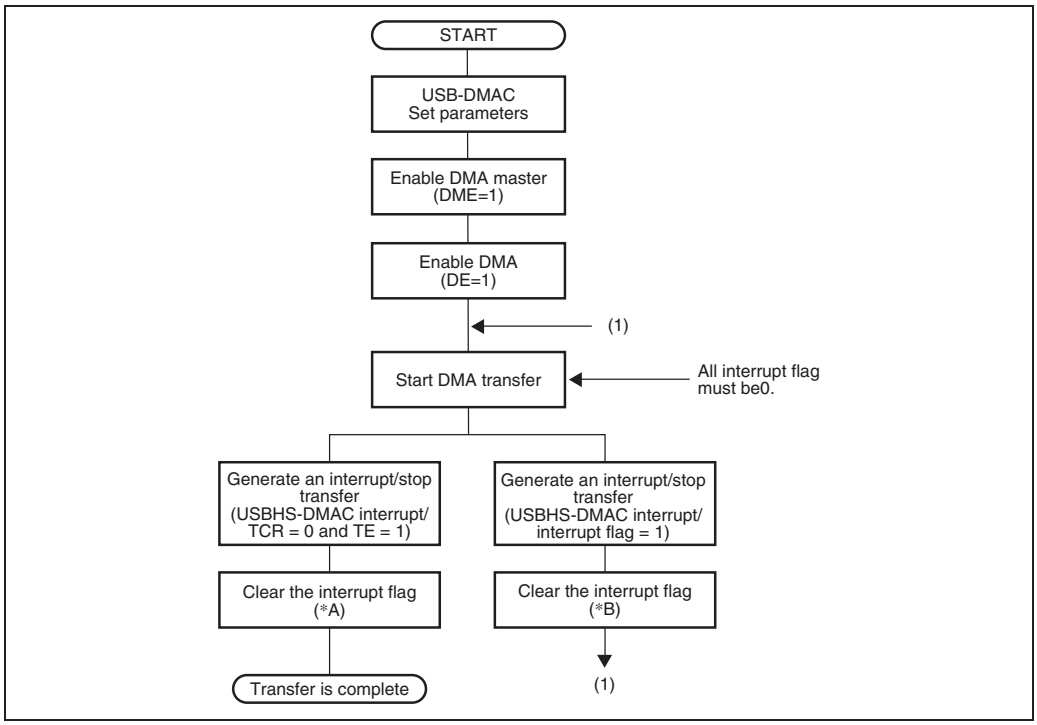


Figure 61.13 DMA Transfer Flow Overview

Where A and B apply to the following flags:

(Note that RW, BUF, and TR are not set when RWE, BUFE, and TRE are disabled, respectively.)

* A: TE flag

* B: SP,(RW,BUF,TR) flags

When to change USB-DMAC parameters

USB-DMAC parameters (such as destination address or transfer count) should be changed while all interrupt flags are cleared and DE=0 and DME=0 are set (a transfer is started with the latest parameters when DME=1 and DE=1 are set). Furthermore, USB-DMAC parameters should not be changed while the DMA is enabled (DME=1 and DE=1).

What to do if freeze

If a transfer should freeze during operation, issue a software reset after setting DE=0 and DME=0 and clearing all interrupt flags. All hardware except configuration registers is initialized. Restart by setting DME and DE to 1 after updating USB-DMAC parameters if necessary.

Control when a timeout occurs

Since this module assumes bus access in the transfer units listed in table 61.2, it cannot be restarted when a timeout occurs in an irregular case where it is being accessed with any size that are not in the table. This irregular case should be handled by software, such as by issuing a software reset (to both CH0 and CH1).

Control when a NULL packet is received

When a NULL packet is received during a DMA transfer, the DMA transfer can be suspended and resumed on each channel independently by controlling the FTE bit of this module and the DREQE bit of the USBHS0 module in the following sequence.

[Control sequence]

During a DMA transfer (A)

(1) A NULL packet is received (an interrupt is generated and the NULL flag is detected).

(2) The DREQE bit of the USBHS0 module is negated (=0).

(3) Wait for the internal bus to be stabilized.

(4) Perform three actions at the same time; setting the FTE bit, clearing the NULL bit and negating the DE bit.

An interrupt is generated due to TE.

(5) Clear the interrupt caused by TE.

(6) Set the parameters (such as TCR or DAR) for the next transfer.

(7) Assert the DE bit (=1). The DMA is restarted.

(8) Assert the DREQE bit (=1).

Start a DMA transfer (B).

[Restrictions]

1) FTE bit set timing

   If this module is accessing the SHwy (SHBSYx bit=1) when setting the FTE bit, you need to wait to set the FTE register until this module's internal buffer is empty and the SHwy bus access is complete (SHBSYx bit=0). Note that if you accidentally set the FTE register while an SHwy bus access is in progress, the transfer fails and transfer data may be lost or the transfer may be unable to be restarted.

2) DREQE register assert (negate clear) timing

   It is necessary to allow at least 20clk@ZSϕ after the DE bit is asserted and before the DREQE is asserted. This is because DREQE needs to be asserted after transfers enabled by the DE bit are ready internally to be started. Asserting DREQE immediately after DE may cause malfunction such as initiating unnecessary bus access.

3) Fractional byte and NULL packet reception

   This module assumes bus access in the transfer units listed in table 61.2 and goes out of control when it receives a NULL packet in an unsupported transfer unit. Therefore, data transfer in any transfer unit that is not in the table is prohibited.

4) IN/OUT switching after NULL packet reception

   After a NULL is received, transfers cannot be restarted with the transfer direction switched from OUT to IN. This is because this module still considers the terminated transfer as an OUT transfer until the transfer count reaches its end. Note that if you switch the transfer direction to IN transfer accidentally after a NULL packet is received, a conflict occurs between an IN and an OUT transfers, which may cause illegal bus access.

   Use CH0 and CH1 with their transfer direction fixed, or if the transfer direction needs to be switched on the same channel, make sure to do it every time a transfer completes successfully due to the end of transfer count or is terminated by software reset.

Figure 61.14 shows the state transitions for DMA transfers.

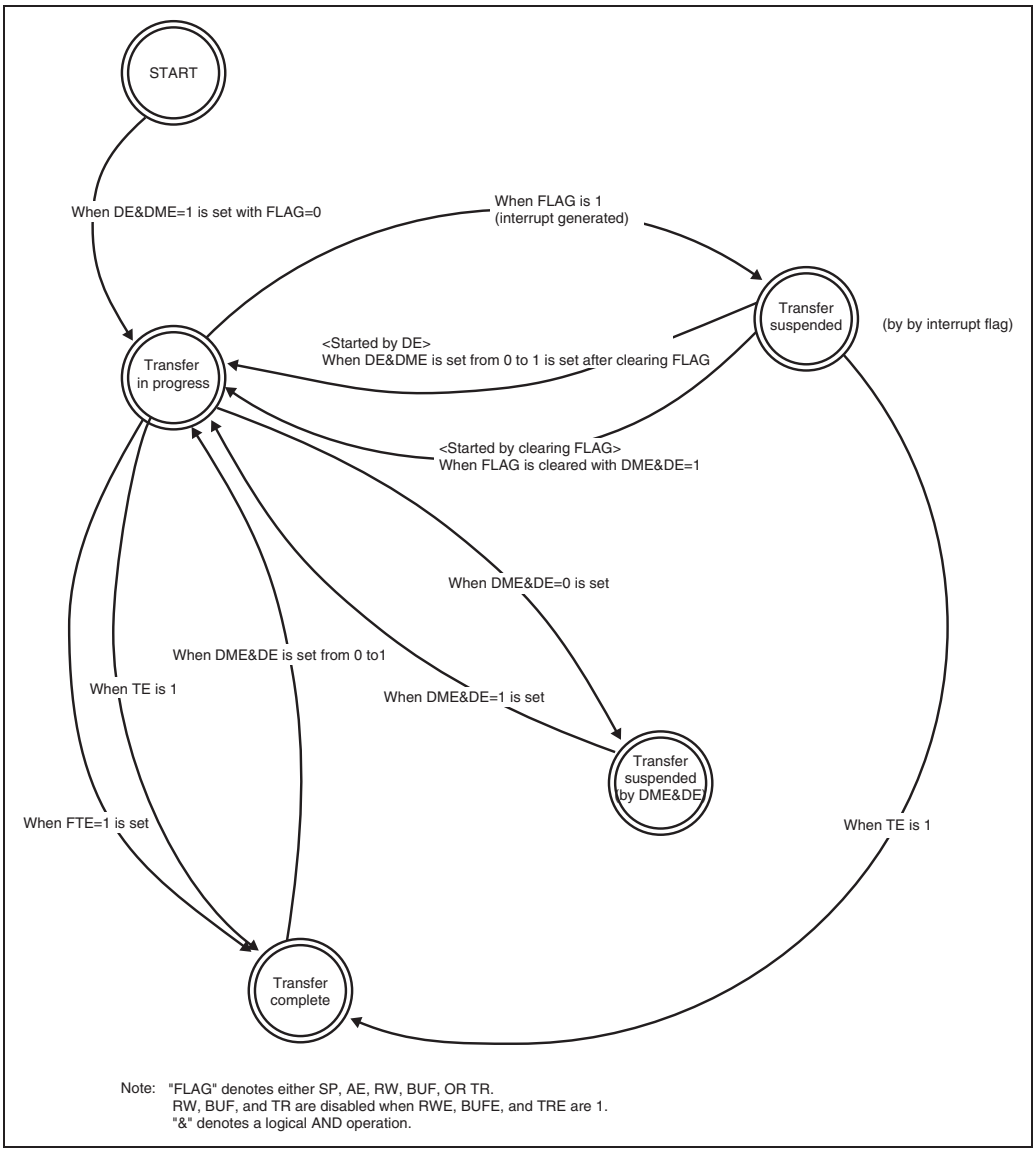


Figure 61.14 State Transitions for DMA Transfer

(4) Control Sequence

Figure 61.15 shows an outline of the control sequence of this module.

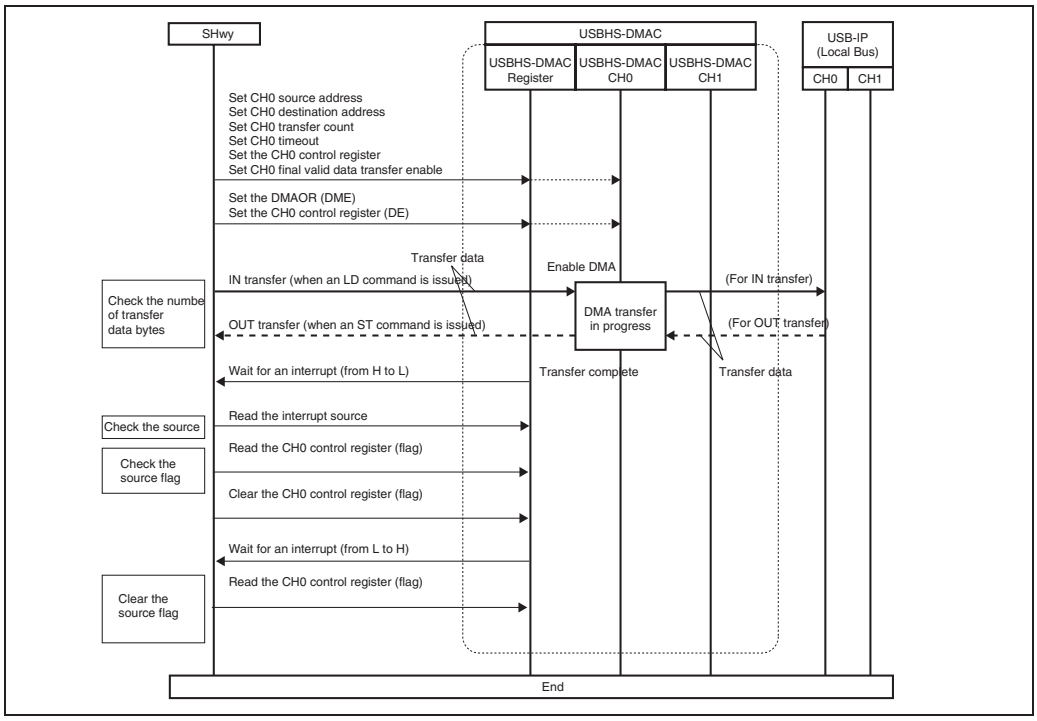


Figure 61.15 Control Sequence Overview

(5) Internal Buffer Configuration

This module has 64 bytes (64 bitsx8 words) of internal buffer for each of two channels. Thus, the total capacity of this module's internal buffers is 128 bytes (1024 bits).

The internal buffers are composed of two planes each of which is organized as 64 bits x 4 words and are readable /writable on per-plane basis from the USB-IP local bus or SHwy bus (plane 1 is writable when plane 0 is readable or vice versa). For 16-byte transfers, only 2 words in plane 0 and 2 words in plane 1 are used. For 8-byte transfers, only 1 word in plane 0 and 1 word in plane 1 are used.

Note that these internal buffers cannot be accessed directly by software.

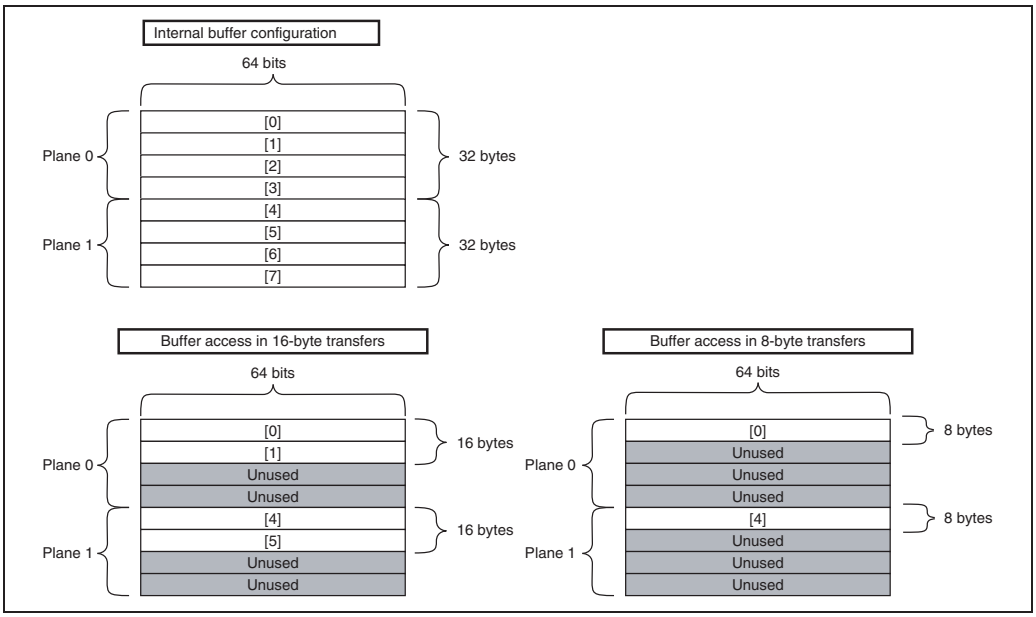


Figure 61.16 Internal Buffer Configuration and Used Area for Each Transfer Size

(6) Internal Buffer Control (Hardware Control, For reference)

(a) IN transfer (from SHwy to USB)

Retrieves transfer data from a source on the SHwy bus and writes it to this module's internal buffer. Reads the written data from the internal buffer and writes it to the USB-IP.

Figure 61.17 shows how the planes of this module's internal buffers are controlled during an IN transfer. In this figure, "read' and 'write" indicate read/write operations to this module's internal buffers.

When a write to plane 0 or plane 1 is complete, the writable plane flag is toggled (every time 2 words* and 1 word* are written for 16-byte and 8-byte transfers, respectively). When a read from plane 0 or plane 1 and a transfer the read data to the USB-IP are complete, the readable plane flag is toggled (every time 2 words* and 1 word* are read for 16-byte and 8-byte transfers, respectively). Access to the SHwy is prohibited during the period when both the writable plane flag and readable plane flag are set on the same plane as a read/write access conflict may occur.

* 1 word=64 bits

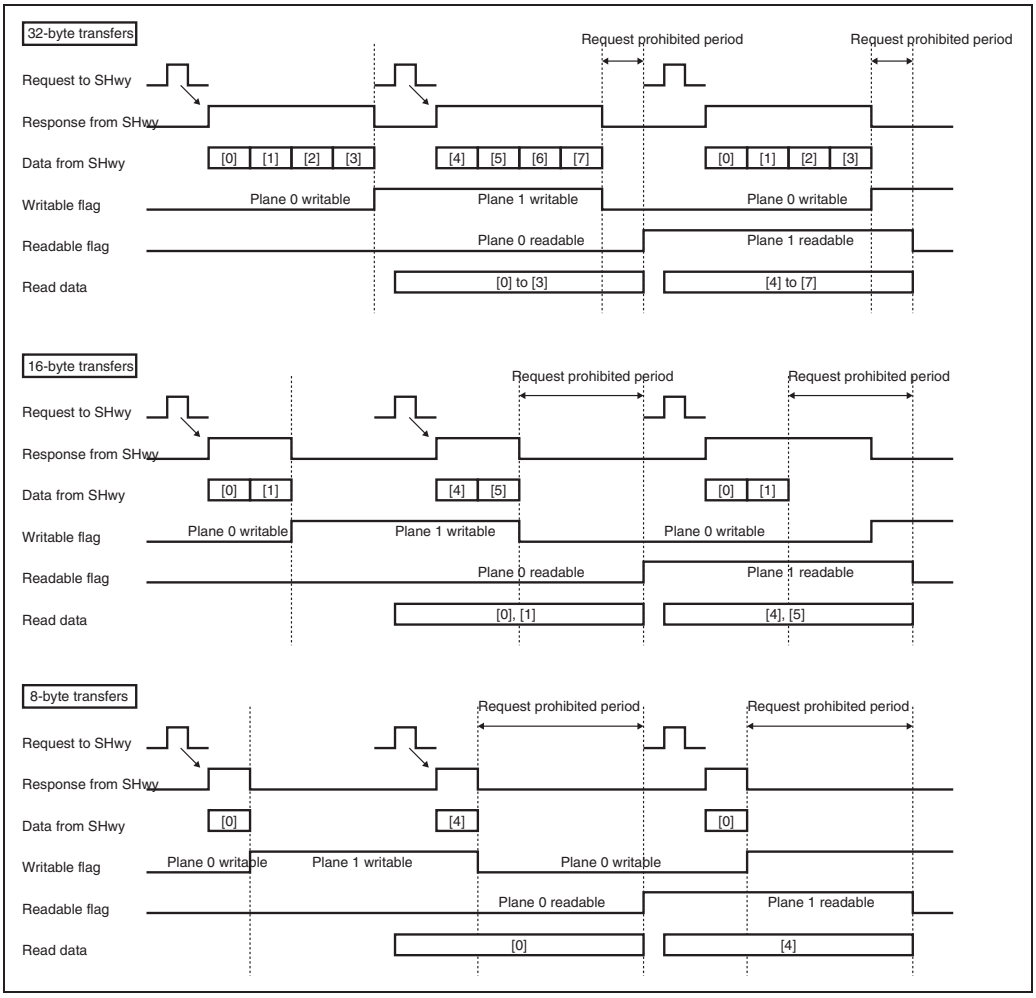


Figure 61.17 Read/Write Control for Internal Buffer: From SHwy to USB (IN Transfer)

(b) OUT transfer (from USB to SHwy)

Writes data read from the USB-IP to the internal buffers. Reads the written data from this module's internal buffers and writes it to the destination on the SHwy bus (OUT transfer).

Figure 61.18 shows how the planes of this module's internal buffers are controlled during an OUT transfer. In this figure, "read' and 'write" indicate read/write operations to this module's internal buffers.

When a write to plane 0 or plane 1 is complete, the writable plane flag is toggled (every time 2 words* and 1 word* are written for 16-byte and 8-byte transfers, respectively). When a read from plane 0 or plane 1 is complete, the readable plane flag is toggled (every time 2 words* and 1 word* are read for 16-byte and 8-byte transfers, respectively). Access to the SHwy is prohibited during the period when both the writable plane flag and readable plane flag are set the same plane as a read/write access conflict may occur.

* 1 word=64 bits

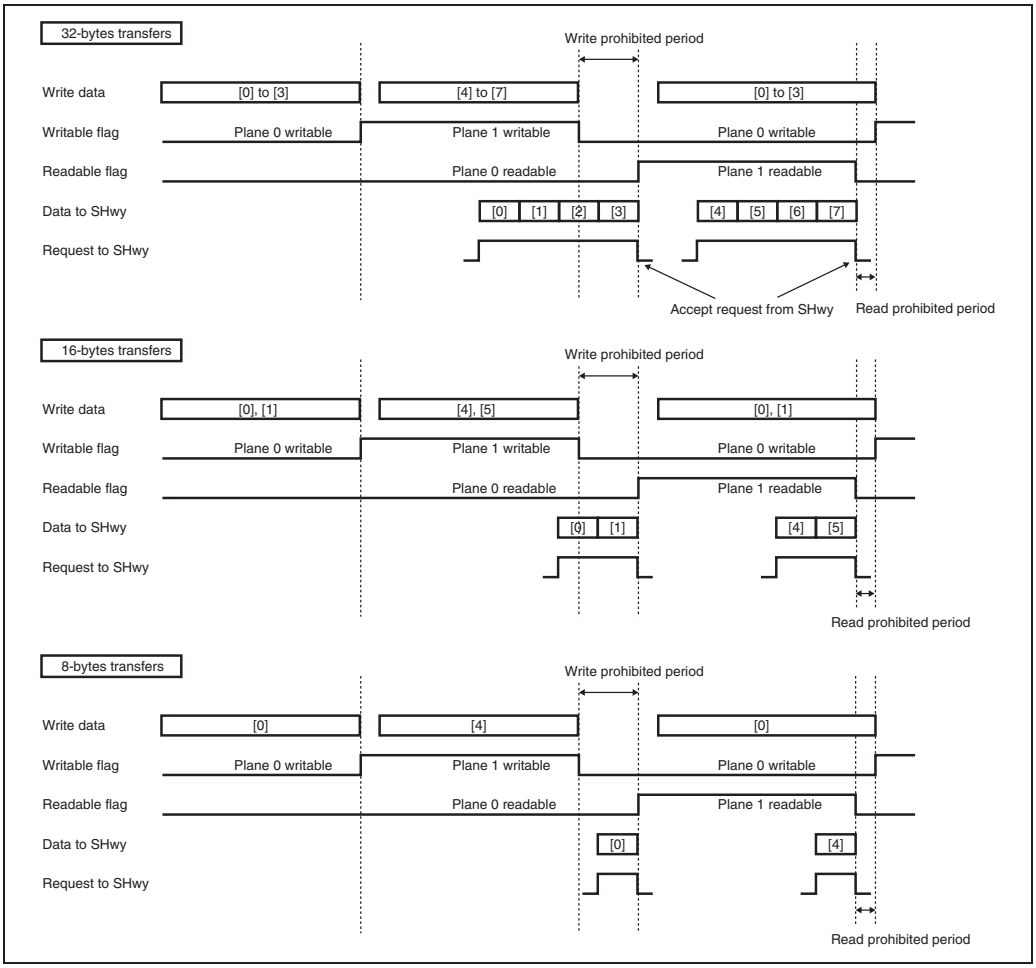


Figure 61.18 Read/Write Control for Internal Buffer: From USB to SHwy (OUT Transfer)

Section 62 USB High-Speed DMAC (USBHS1-DMAC)

62.1 Features

- Two types of clock: ZSϕ and USBHS1 local bus clock (48 MHz), which are asynchronously absorbed in the local bus bridge
- The SHwy bus interface functions are implemented.

The SHwy bus interface handles data transfer with the memory and register settings.

- Data communication is performed using the local DMA protocol.
- Supports two channels that can work concurrently.
- Interrupts

— Setting count end interrupt

— Transfer end interrupt upon receiving a short packet from the USB-IP
This function allows generation of an interrupt even in the case where DMA transfer ends after receiving data less than the transfer size set in the DMAC.

— Timeout interrupt
A timeout interrupt can be generated after the specified cycles after the last USBHS1 transfer request. (This interrupt is used for the timeout when the final packet received is Max packet.)

— Interrupts can also be generated when a NULL packet is received or an address error is detected.

Table 62.1 Main Functions of This Module

Item	Description
Application	Transfer between USB-IP (FIFO) and SHwy bus (4-Gbyte arbitrary space)
Purpose of DMA transfer	High-speed data transfer between USB-IP and SHwy bus
DMA transfer end notification to the software	Interrupt signals (Transfer count end, USB-IP short packet reception, timeout, etc.)
Transfer space/transfer address direction	4-Gbyte arbitrary space (forward direction) to 4-Gbyte arbitrary space (forward direction)
Maximum transfer count	16,777,216
Transfer unit	8, 16, or 32 bytes
Control signals generated	Address/data read/data write conforming to the USB-IP local bus interface and SHwy bus protocols
Number of channels	2 (parallel operation enabled, round-robin control)
Bus specification	SHwy bus (SuperHyWay 64 bits), local bus (USB-IP local bus)
Clock	SHwy clock (130 MHz), USB local bus clock (48 MHz)
Max. Transfer rate	IN transfer: About 350 Mbps (in 32-byte transfer mode) OUT transfer: About 340 Mbps (in 32-byte transfer mode)

Table 62.2 Bus Access Type

	Supported Access Type
SHwy bus access (USBHS1-DMAC master)	8-byte read/write 16-byte read/write 32-byte read/write
USBHS1-DMAC register setting	4-byte read/write 8-byte read/write

The configuration of this module is shown below.

This module is provided with buffers and bus bridges and controls transfers between the SHwy bus and USB High-Speed module (USBHS1).

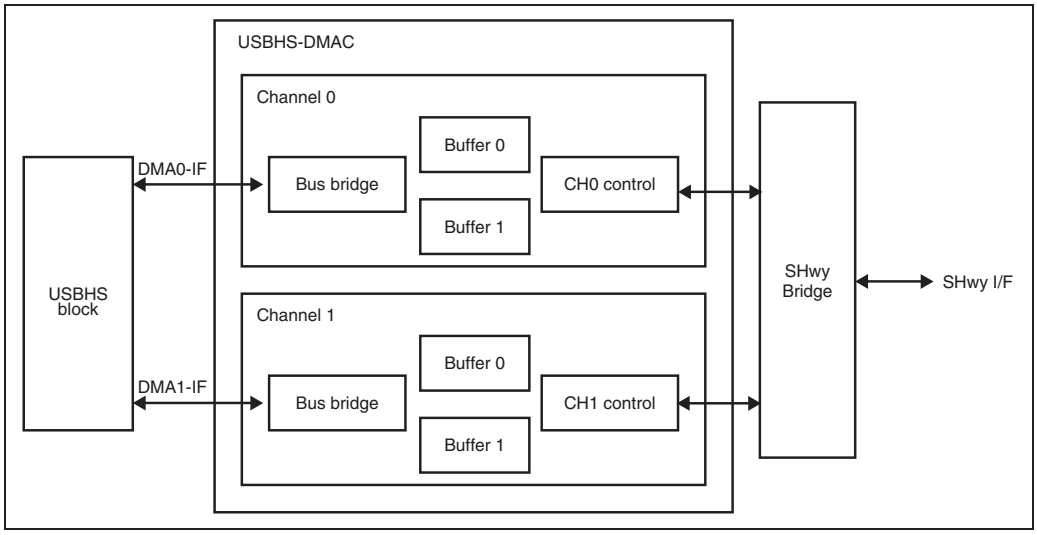


Figure 62.1 USBHS1-DMAC Configuration

62.2 Register Map

Table 62.3 shows the register configuration. Table 62.4 shows the register states in each processing mode.

Table 62.3 Register Configuration

Register Name	Abbreviation	R/W	Address	Access Size
VCR register	USBDMA_VCR	R/W	USBDMA_BASE+H'00	32
Software reset register	USBDMA_SWR	R/W	USBDMA_BASE+H'08	32
DMA interrupt source register	USBDMA_DMICR	R	USBDMA_BASE+H'10	32
DMA source address register_0	USBDMA_SAR_0	R/W	USBDMA_BASE+H'20	32
DMA destination address register_0	USBDMA_DAR_0	R/W	USBDMA_BASE+H'24	32
DMA transfer count register_0	USBDMA_TCR_0	R/W	USBDMA_BASE+H'28	32
DMA timeout count register_0	USBDMA_TOCNTR_0	R	USBDMA_BASE+H'2C	32
DMA timeout constant register_0	USBDMA_TOCSTR_0	R/W	USBDMA_BASE+H'30	32
DMA channel control register_0	USBDMA_CHCR_0	R/W	USBDMA_BASE+H'34	32
DMA final transaction valid data transfer enable register_0	USBDMA_TEND_0	R/W	USBDMA_BASE+H'38	32
DMA source address register_1	USBDMA_SAR_1	R/W	USBDMA_BASE+H'40	32
DMA destination address register_1	USBDMA_DAR_1	R/W	USBDMA_BASE+H'44	32
DMA transfer count register_1	USBDMA_TCR_1	R/W	USBDMA_BASE+H'48	32
DMA timeout count register_1	USBDMA_TOCNTR_1	R	USBDMA_BASE+H'4C	32
DMA timeout constant register_1	USBDMA_TOCSTR_1	R/W	USBDMA_BASE+H'50	32
DMA channel control register_1	USBDMA_CHCR_1	R/W	USBDMA_BASE+H'54	32
DMA final transaction valid data transfer enable register_1	USBDMA_TEND_1	R/W	USBDMA_BASE+H'58	32
DMA operation register	USBDMA_DMAOR	R/W	USBDMA_BASE+H'60	32

Note: USBDMA_BASE=H'E68C0000

Table 62.4 Register States in Each Processing Mode

Register Abbreviation	Power-On Reset	Software Standby	Module Standby	Sleep
USBDMA_VCR	Initialized	Retained	Retained	Retained
USBDMA_SWR	Initialized	Retained	Retained	Retained
USBDMA_DMICR	Initialized	Retained	Retained	Retained
USBDMA_SAR_0	Initialized	Retained	Retained	Retained
USBDMA_DAR_0	Initialized	Retained	Retained	Retained
USBDMA_TCR_0	Initialized	Retained	Retained	Retained
USBDMA_TOCNTR_0	Initialized	Retained	Retained	Retained
USBDMA_TOCSTR_0	Initialized	Retained	Retained	Retained
USBDMA_CHCR_0	Initialized	Retained	Retained	Retained
USBDMA_TEND_0	Initialized	Retained	Retained	Retained
USBDMA_SAR_1	Initialized	Retained	Retained	Retained
USBDMA_DAR_1	Initialized	Retained	Retained	Retained
USBDMA_TCR_1	Initialized	Retained	Retained	Retained
USBDMA_TOCNTR_1	Initialized	Retained	Retained	Retained
USBDMA_TOCSTR_1	Initialized	Retained	Retained	Retained
USBDMA_CHCR_1	Initialized	Retained	Retained	Retained
USBDMA_TEND_1	Initialized	Retained	Retained	Retained
USBDMA_DMAOR	Initialized	Retained	Retained	Retained

62.2.1 VCR Register (USBDMA_VCR)

[Address=USBDMA_BASE+H'00]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ERR_SNT	ERR_RCV
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	ERR_SNT	0	R/W	Send Error Response 0: No error is generated. [Clearing condition] Writing 0 after reading 1. 1: An error is generated.
0	ERR_RCV	0	R/W	Receive Error Response 0: No error is generated. [Clearing condition] Writing 0 after reading 1. 1: An error is generated.

62.2.2 Software Reset Register (USBDMA_SWR)

[Address=USBDMA_BASE+H'08]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SWR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	SWR	0	R/W	Software Reset 0: Cancels reset. 1: Resets entire system. Note: On software reset, this bit should be held high for long enough until the internal circuit stabilizes. When this bit is set to 1, it is recommended to allow several tens of clocks if operating at 130MHz for a reset period before clearing the reset (setting this bit to 0) as a precaution.

62.2.3 DMA Interrupt Source Register (USBDMA_DMICR)

[Address=USBDMA_BASE+H'10]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SHBSY1	—	—	—	—	—	—	—	SHBSY0	—	—	—	—	—	—	AE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	TR1	BUF1	RW1	NULL1	TO1	SP1	TE1	—	TR0	BUF0	RW0	NULL0	TO0	SP0	TE0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	SHBSY1	0	R	CH1 SHwy Bus Busy Flag Monitor 0: The SHwy bus is idle. 1: The SHwy bus is busy.
30 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23	SHBSY0	0	R	CH0 SHwy Bus Busy Flag Monitor 0: The SHwy bus is idle. 1: The SHwy bus is busy.
22 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	AE	0	R	Address Error Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (AE in the DMA operation register is reflected.)
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
14	TR1	0	R	CH1 Transaction End: Receive Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (TR in the channel 1 control register is reflected.)
13	BUF1	0	R	CH1 Buffer End Detect Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (BUF in the channel 1 control register is reflected.)
12	RW1	0	R	CH1 Final Buffer Access Detect Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (RW in the channel 1 control register is reflected.)
11	NULL1	0	R	CH1 NULL Packet Receive Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (NULL in the channel 1 control register is reflected.)
10	TO1	0	R	CH1 Timeout Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (TO in the channel 1 control register is reflected.)
9	SP1	0	R	CH1 Short Packet Receive Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (SP in the channel 1 control register is reflected.)
8	TE1	0	R	CH1 Transfer End Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (TE in the channel 1 control register is reflected.)
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
6	TR0	0	R	CH0 Transaction End Detect Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (TR in the channel 0 control register is reflected.)
5	BUF0	0	R	CH0 Buffer End Detect Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (BUF in the channel 0 control register is reflected.)
4	RW0	0	R	CH0 RWEND Receive Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (RW in the channel 0 control register is reflected.)
3	NULL0	0	R	CH0 NULL Receive Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (NULL in the channel 0 control register is reflected.)
2	TO0	0	R	CH0 Timeout Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (TO in the channel 0 control register is reflected.)
1	SP0	0	R	CH0 Short Packet Receive Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (SP in the channel 0 control register is reflected.)
0	TE0	0	R	CH0 Transfer End Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (TE in the channel 0 control register is reflected.)

62.2.4 DMA Source Address Register_0 to 1 (USBDMA_SAR_0 to 1)

[Address=USBDMA_BASE+H'20,H'40]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SAR[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SAR[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	SAR31 to SAR0	All 0	R/W	Source Address (0x00000000 to 0xFFFFFFFF (4 Gbytes)) Set a value of 8-byte, 16-byte, or 32-byte boundary. Indicate the next transfer source address during a DMA transfer.

62.2.5 DMA Destination Address Register_0 to 1 (USBDMA_DAR_0 to 1)

[Address=USBDMA_BASE+H'24,H'44]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DAR[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DAR[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DAR31 to DAR0	All 0	R/W	Destination Address (0x00000000 to 0xFFFFFFFF (4 Gbytes)) Set a value of 8-byte, 16-byte, or 32-byte boundary. Indicate the next transfer destination address during a DMA transfer.

62.2.6 DMA Transfer Count Register_0 to 1 (USBDMA_TCR_0 to 1)

[Address=USBDMA_BASE+H'28,H'48]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	TCR[23:16]							
Initial value:	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TCR[15:0]															
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	TCR23 to TCR0	H'FF FFFF*	R/W	Transfer Count • When 0x000001 is set, total transfer volume is as follows: Transfer size = 32 bytes: 32 × 1 bytes Transfer size = 16 bytes: 16 × 1 bytes Transfer size = 8 bytes: 8 × 1 bytes • When 0xFFFFFF is set, 16,777,215 times • When 0x000000 is set, 16,777,216 times (maximum) • Indicate 0 when a DMA transfer completes successfully.

Note: * To read this register, read the internal transfer counter value (the TCR counter value) directly. This register is read as all 1 after a reset is cleared because the initial value of the TCR counter is all 1 (0xFFFFFF). When DMA is enabled (DE in DMACHCR is asserted), the TCR counter is loaded with the value set in this register and decrements during DMA transfers. This means that the remaining transfer count is read back. Note that the read value may be different from the one set in this register due to this reason.

62.2.7 DMA Timeout Count Register_0 to 1 (USBDMA_TOCNTR_0 to 1)

[Address=USBDMA_BASE+H'2C,H'4C]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	TOCNTR[21:16]					
Initial value:	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TOCNTR[15:0]															
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
21 to 0	TOCNTR21 to TOCNTR0	H'3F FFFF	R	Timeout Counter Value (0x000000 to 0x27AC40) Indicate the remaining timeout count during timeout counting. (Countable up to 0x3FFFFF (approximately 32 ms) by the hardware. See the TOCSTR register.)

62.2.8 DMA Timeout Constant Register_0 to 1 (USBDMA_TOCSTR_0 to 1)

[Address=USBDMA_BASE+H'30,H'50]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	TOCSTR[21:16]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TOCSTR[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
21 to 0	TOCSTR21 to TOCSTR0	H'00 0000	R/W	Timeout Constant Value (0x000000 to 0x27AC40) Sst a timeout value (at 130 MHz cycle). The maximum timeout time is approximately 20 ms. (Setting up to 0x3FFFFF (approximately 32 ms) is allowed by the hardware.)

62.2.9 DMA Channel Control Register_0 to 1 (USBDMA_CHCR_0 to 1)

[Address=USBDMA_BASE+H'34,H'54]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	FTE	—	—	—	SPIM	TRE	BUFE	RWE	NULLE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TR	BUF	RW	NULL	PRI[3:0]				TS[1:0]		IE	TOE	TO	SP	TE	DE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W*	R/W*	R/W*	R/W*	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W*	R/W*	R/W*	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	FTE	0	(R)/W	Forced TE Set Register When a NULL packet is received, the TE bit is forced to 1 to terminate the transfer by setting 1 in this register. (The DREQE bit of the UDSB-IP should also be controlled accordingly. For details on the control procedure and restrictions, see section 62.3.2(3).) This bit is always read as 0. 0: No effect (nothing happens). 1: Forces the TE bit to 1.
23 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	SPIM	0	R/W	Short Packet Receive Interrupt Mask Enables or disables the reflection of the short packet (SP) receive flag in the interrupt signal. If this bit is set to 1, no interrupts are generated when an SP is received. However, the SP receive flag (the SP bit) is set regardless of this register setting. 0: The short packet receive interrupt is enabled (default). 1: The short packet receive interrupt is disabled.

Bit	Bit Name	Initial Value	R/W	Description
19	TRE	0	R/W	Transaction End Detect Interrupt Flag Enable Enables or disables the reflection of TR in the interrupt signal and the DMA stop/restart control. (When this bit is set to 0, the TR bit is always 0.) 0: The TR flag is disabled. 1: The TR flag is enabled.
18	BUFE	0	R/W	Buffer End Detect Interrupt Flag Enable Enables or disables the reflection of BUF in the interrupt signal and the DMA stop/restart control. (When this bit is set to 0, the BUF bit is always 0.) 0: The BUF flag is disabled. 1: The BUF flag is enabled.
17	RWE	0	R/W	Final Buffer Access Detect Interrupt Flag Enable Enables or disables the reflection of RW in the interrupt signal and the DMA stop/restart control. (When this bit is set to 0, the RW bit is always 0.) 0: The RW flag is disabled. 1: The RW flag is enabled.
16	NULLE	0	R/W	NULL Receive Interrupt Flag Enable Enables or disables the reflection of the NULL receive interrupt flag (NULL) in the interrupt signal. 0: The NULL receive interrupt flag is disabled. 1: The NULL receive interrupt flag is enabled.
15	TR	0	R/W*	Transaction End Detect Interrupt Flag When the transaction end is detected, an interrupt is generated. 0: DMA transfer is in progress or suspended. [Clearing condition] Writing 0 after reading 1. 1: An transaction end receive interrupt is generated.

Bit	Bit Name	Initial Value	R/W	Description
14	BUF	0	R/W*	Buffer End Detect Interrupt Flag When the end of the buffer is detected, an interrupt is generated. 0: DMA transfer is in progress or suspended. [Clearing condition] Writing 0 after reading 1. 1: A buffer end detect interrupt is generated.
13	RW	0	R/W*	Final Buffer Access Detect Interrupt Flag When the final access to the buffer is detected, an interrupt is generated. 0: DMA transfer is in progress or suspended. [Clearing condition] Writing 0 after reading 1. 1: A final buffer access detect interrupt is generated.
12	NULL	0	R/W*	NULL Receive Interrupt Flag When NULL packet is received, an interrupt is generated. 0: DMA transfer is in progress or suspended. [Clearing condition] Writing 0 after reading 1. 1: A NULL packet receive interrupt is generated.
11 to 8	PRI3 to PRI0	All 0	R/W	Priority Set the value of the priority signal to be output to the SHwy bus. 0000: Priority 0 (lowest) 0001: Priority 1 : 1111: Priority 15 (highest)

Bit	Bit Name	Initial Value	R/W	Description
7, 6	TS1 to TS0	00	R/W	MA Transfer Size 00: 8 bytes 01: 16 bytes 10: 32 bytes 11: Setting prohibited Specify the same transfer size and address boundary when setting addresses in DMASAR and DMADAR as a transfer source and transfer destination. If TS = 11 is set, an address error is generated and DMA transfer is disabled.
5	IE	0	R/W	Interrupt Enable Enables or disables an interrupt request to the CPU when DMA transfer ends. When AE, TE, SP, TO, NULL, RW, BUF, or TR bit is set with this bit set to 1, an interrupt request is output to the CPU. However, when the TRE, BUFE, RWE, NULLE, or TOE bit is set to disabled, no interrupt due to TR, BUF, RW, NULL, or TO is generated. 0: An interrupt request is disabled. 1: An interrupt request is enabled.
4	TOE	0	R/W	Timeout Enable Enables or disables the reflection of the timeout flag (TO) in the interrupt. 0: Timeout flag is disabled. 1: Timeout flag is enabled.
3	TO	0	R/W*	Timeout Flag After a transfer request REQ is negated, a timeout interrupt is generated after the specified cycles. (Used for timeout when the final packet is Max packet.) 0: DMA transfer is in progress or suspended. [Clearing condition] Writing 0 after reading 1. 1: Timeout is generated.

Bit	Bit Name	Initial Value	R/W	Description
2	SP	0	R/W*	Short Packet Receive Flag A transfer end interrupt is generated upon receiving a short packet from the USB-IP. For example, if DMA transfer size is set to 1 MB but actual data transfer is 900 KB, this interrupt is generated when transfer of 900 KB finishes. 0: DMA transfer is in progress or suspended. [Clearing condition] Writing 0 after reading 1. 1: A short packet is received.
1	TE	0	R/W*	Transfer End Flag When a DMA transfer ends with DMATCR = 0, the TE bit is set to 1. When a DMA address error occurs before DMATCR is cleared to 0 and the transfer is suspended by clearing the DE bit and the DME bit in DMAOR, the TE bit is not set to 1. To clear the TE bit, write 0 after reading 1.When TE = 1, DMA transfer is disabled even if the DE bit is set to 1. 0: DMA transfer is in progress or suspended. [Clearing condition] Writing 0 after reading 1. 1: DMA transfer end (TCR = 0)
0	DE	0	R/W	DMA Enable Enables or disables DMA transfer. Setting the DME bit in DMAOR and the DE bit for the corresponding channel to 1 starts a DMA transfer, provided that all interrupt flags are 0. Clearing the DE bit to 0 suspends the ongoing transfer after the transfer of one transaction is completed. 0: DMA transfer is disabled. 1: DMA transfer is enabled.

Note: * Only writing 0 to clear the flag is enabled.

62.2.10 DMA Final Transaction Valid Data Transfer Enable Register_0 to 1 (USBDMA_TEND_0 to 1)

[Address=USBDMA_BASE+H'38,H'58]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	EDTEN[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EDTEN[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	EDTEN31 to EDTEN0	H'00000000	R/W	Final Transaction Valid Data Transfer Enable (valid only for IN transfers) Specify valid data size in units of bytes in the final transaction of data transfer. (See section 62.3.2) 0x80000000: 32 bytes × (n-1) + 1 byte 0xC0000000: 32 bytes × (n-1) + 2 bytes : 0xFFFFFFFF: 32 bytes × (n-1) + 32 bytes Notes: 1. n: Transfer count setting (TCR) 2. For the 8-byte transfer, set EDTEN23 to EDTEN0 to 0. For the 16-byte transfer, set EDTEN15 to EDTEN0 to 0.

62.2.11 DMA Operation Register (USBDMA_DMAOR)

[Address=USBDMA_BASE+H'60]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	TID[1:0]		RM	PR[1:0]		AE	DME
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W*	R/W*	R/W	R/W	R/W	R/W*	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6, 5	TID1 and TID0	00	R/W*	Response Error Channel Identity Information TID1 indicates the channel 1 error information, and TID0 indicates the channel 0 error information. TID1 0: No error 1: Channel 1 response packet error TID0 0: No error 1: Channel 0 response packet error [Setting condition] When a CH0 (1) response error occurs [Clearing condition] Clearing ERR_RCV in VCR (Channel 0/channel 1 concurrent clear)
4	RM	0	R/W	Response Error Mask Mode 0: A response error is output. 1: A response error is masked.

Bit	Bit Name	Initial Value	R/W	Description
3, 2	PR1 to PR0	All 0	R/W	Priority Mode Specify the priority of channels to execute transactions when transfer requests are made simultaneously in both channel 0 and channel 1 as follows: 00: Channel 0 > Channel 1 01: Channel 1 > Channel 0 10: Setting prohibited (If PR = 10 is set, channel 0 > channel 1) 11: Round-robin mode
1	AE	0	R/W*	Address Error Flag Indicates that an address error interrupt occurred when setting SAR or DAR. This flag is set to 1 when the value of SAR or DAR differs from the transfer size (TS) boundary, and when the TS bits are set to 11 (setting prohibited). When the AE bit is set to 1, DMA transfer is not enabled even if the DE bit in DMACHCR and the DME bit in DMAOR are set to 1. 0: No address error interrupt is generated by the DMAC. [Clearing condition] Setting SAR and DAR to values that match the transfer size boundary. 1: An address error interrupt is generated.
0	DME	0	R/W	DMA Master Enable Enables or disables DMA transfers for all channels. When the DME bit and the DE bit in USBDMA_CHCR are set to 1, DMA transfer is enabled, provided that all interrupt flags in USBDMA_CHCR of the transfer channel are 0. Clearing the DME bit suspends the DMA transfer for all channels. 0: DMA transfer for all channels is disabled. 1: DMA transfer for all channels is enabled.

Note: * Only writing 0 to clear the flag is enabled.

62.3 Operation

62.3.1 Interrupt/Error Detection Function

This section describes the interrupt/error detection function that is implemented in this module.

Table 62.5 lists the mask, source, and flag registers for each interrupt type.

Table 62.5 Registers by Interrupts/Errors

	Interrupt Generation	Interrupt Mask Register	Interrupt Mask Register (Individual Mask)	Source Register	Flag Register
Transfer count end	O	CHCR_x.IE	—	DMICR.TEx	CHCR_x.TE
Short packet receive	O	CHCR_x.IE	CHCR_x.SPIM	DMICR.SPx	CHCR_x.SP
NULL packet receive	O	CHCR_x.IE	CHCR_x.NULLE	DMICR.NULLx	CHCR_x.NULL
Timeout	O	CHCR_x.IE	CHCR_x.TOE	DMICR.TOx	CHCR_x.TO
Transaction end detect	O	CHCR_x.IE	CHCR_x.TRE*	DMICR.TRx	CHCR_x.TR
Buffer end detect	O	CHCR_x.IE	CHCR_x.BUFE*	DMICR.BUFx	CHCR_x.BUF
Final buffer access detect	O	CHCR_x.IE	CHCR_x.RWE※	DMICR.RWx	CHCR_x.RW
Address error	O	CHCR_x.IE	—	DMICR.AE	DMAOR.AE
Response packet error	—	—	—	—	VCR.ERR_SNT VCR.ERR_RCV

Note: These registers not only mask interrupt generation but also disable error processing (flag sources and flag clearing).

Table 62.6 shows the processing to be executed when different interrupts occur. DMA transfer control is not affected when the NULL packet receive, timeout, or response packet error interrupt occurs. When the transfer count end interrupt occurs, processing is restarted. Processing can be resumed or restarted after interrupts occur from other sources.

Table 62.6 Processing to be Executed When Interrupts Occur (Suspend/Resume/Restart)

	Suspend/ Resume	Terminate/ Restart	Suspend/Resume/Restart Control Mask Register
Transfer count end	—	o	—
Short packet receive	O	O	—
NULL packet receive	—	O*	—
Timeout	—	O	—
Transaction end detect	O	O	CHCR_x.TRE
Buffer end detect	O	O	CHCR_x.BUFE
Final buffer access detect	O	O	CHCR_x.RWE
Address error	O	O	—
Response packet error	—	—	—

The internal circuit is reloaded register values when restarted, but not when resumed.

* When a NULL packet is received, processing is forced to be terminated and restarted by the FTE register (see section 62.3.2 (3)).

Table 62.7 lists the interrupt generating conditions.

Table 62.7 Interrupt Generating Conditions

Interrupt Name	Interrupt Conditions
Transfer count end interrupt	When the final data transfer of the specified transfer count (in the TCR register) completes IN transfer: When the final access to USB-IP completes OUT transfer: When the data transmission to the SHwy completes
Short packet receive interrupt	When the data transfer at the time the end of a transaction is detected completes
NULL packet receive interrupt	When a NULL packet is detected or the forced TE register is set
Timeout interrupt	When the specified time elapses after the last transfer request
Transaction end detect interrupt	When the end of a transaction is detected
Buffer end detect interrupt	When the end of the buffer is detected
Final buffer access detect interrupt	When the final access to the buffer is detected
Address error interrupt	When invalid access to the DMAC register is attempted (With invalid SAR/DAR values or invalid transfer size (TS) specified)
Response packet error	Error Transmission (err_snt) When accessed by a transaction that is not supported Error Reception (err_rcv) When received a response packet error from the system

Figure 62.2 shows a block diagram of the interrupt circuit.

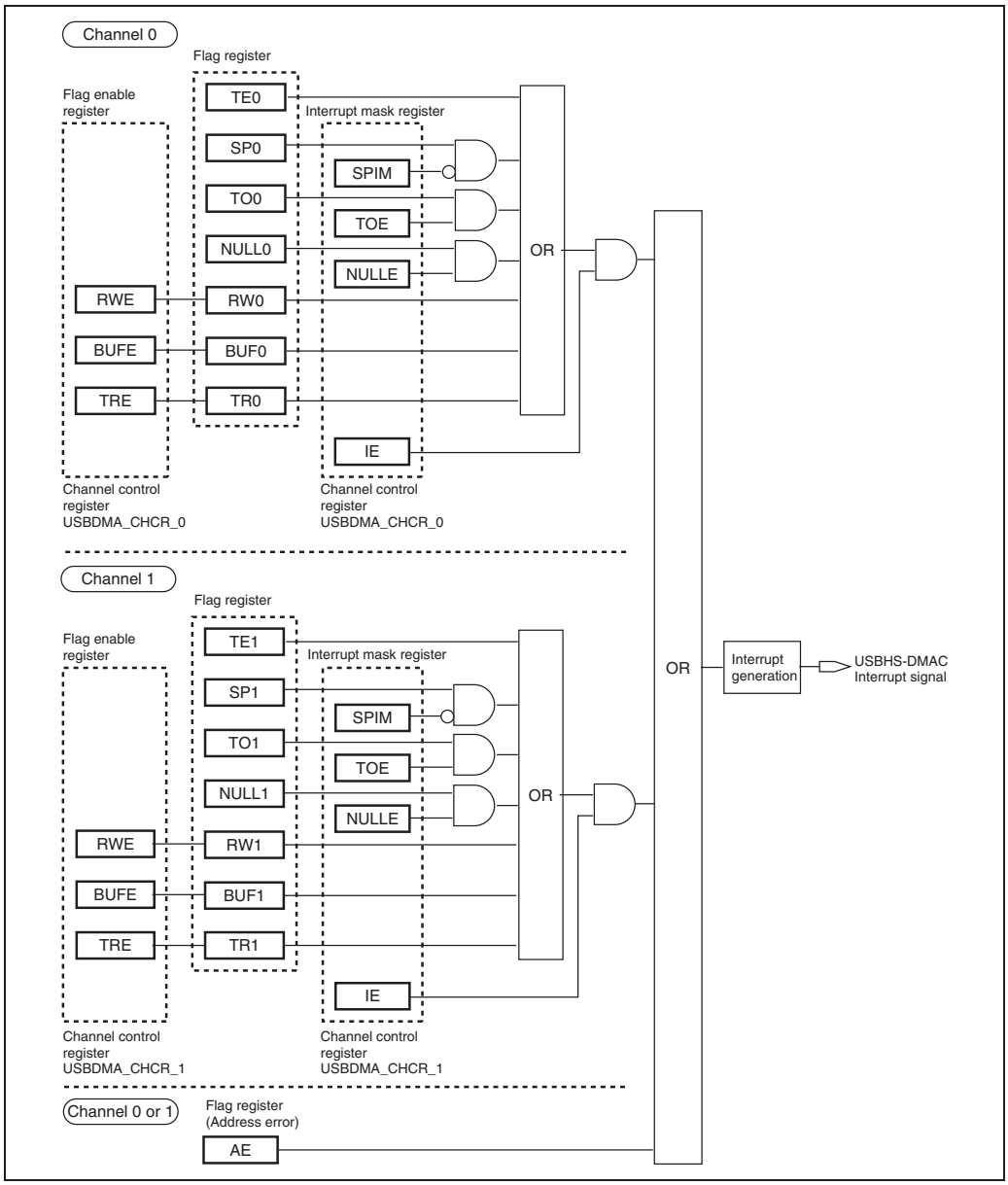


Figure 62.2 Block Diagram of Interrupt Circuit

(1) Transfer Count Ed Interrupt (TE Flag)

Can be generated when the specified number of transfers complete or the FTE bit in the channel control register (USBDMA_CHCR_0 to USBDMA_CHCR_1) is set to 1. When the IE bit in the USBDMA_CHCR_0 to USBDMA_CHCR_1 is set to 0, no interrupts are generated. However, the TE bit in USBDMA_CHCR_0 to USBDMA_CHCR_1 and the TE0 or TE1 bit in the interrupt source register (USBDMA_DMICR) are set to 1 regardless of the IE bit setting.

The internal transfer counter is loaded with the value set in the USBDMA_TCR_x register and decrements based on the SHwy clock every time one transaction (8-/16-/32-byte) completes. When the transfer count value reaches 0 (the end of a transfer count), the counter sets the TE (transfer end) flag from 0 to 1 (when the FTE bit is set, it is reflected on the TE flag immediately). The TE bit is cleared by writing 0 to it after reading it as 1 by software.

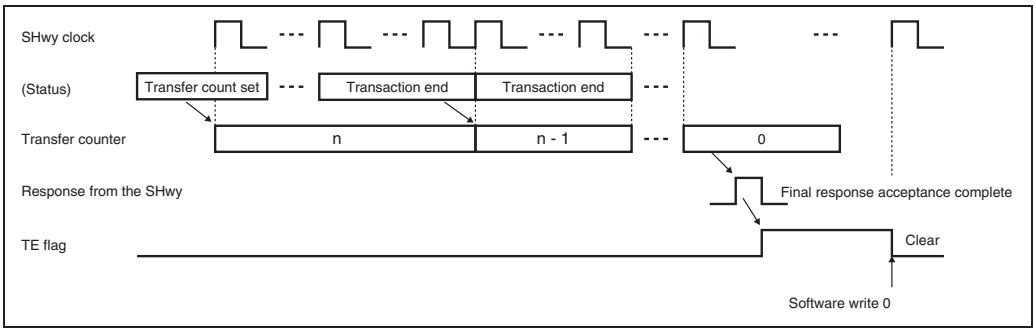


Figure 62.3 Transfer Count End Interrupt (TE) Generation Timing

(2) Short packet receive interrupt (SP flag)

Can be generated when a short packet is detected. When the SPIM bit in the USBDMA_CHCR_x register is set to 1, no interrupts are generated. However, the SP bit (SP flag) in the USBDMA_CHCR_x register and the SP0 or SP1 bit in the USBDMA_DMICR register are set to 1, regardless of the SPIM bit setting. The SP bit is cleared by writing 0 to it after reading it as 1 by software.

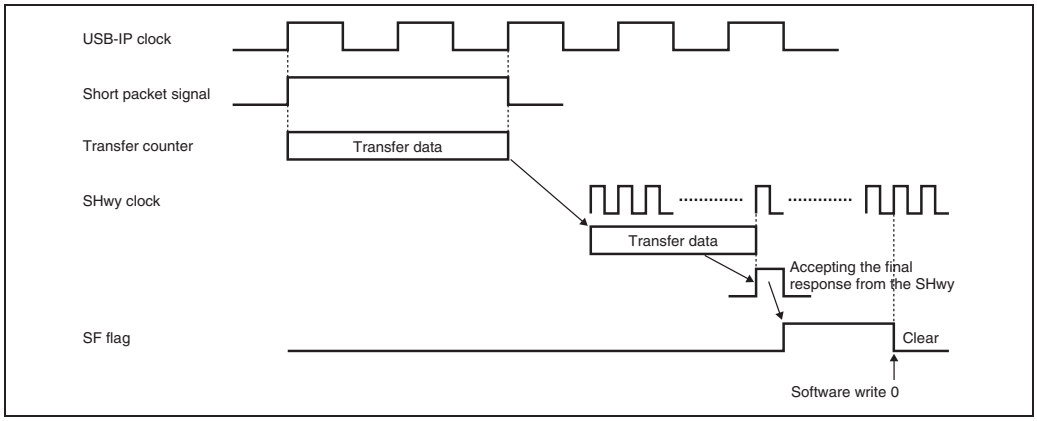


Figure 62.4 Short Packet Receive Interrupt (SP) Generation Timing

(3) NULL packet receive interrupt (NULL flag)

Can be generated when a NULL packet is detected. When the NULLE bit in the USBDMA_CHCR_x register is set to 0, no interrupts are generated. However, the NULL bit (NULL flag) in the USBDMA_CHCR_x register and the NULL0 or NULL1 bit in the USBDMA_DMICR register are set to 1, regardless of the NULLE bit setting. Note also that the DMA transfer control in this module, such as stop, suspend, or resume, is not affected when a NULL packet is received. The software is responsible for implementing special processing if necessary since in this module this interrupt is designed only to signal the software that a NULL packet is received.

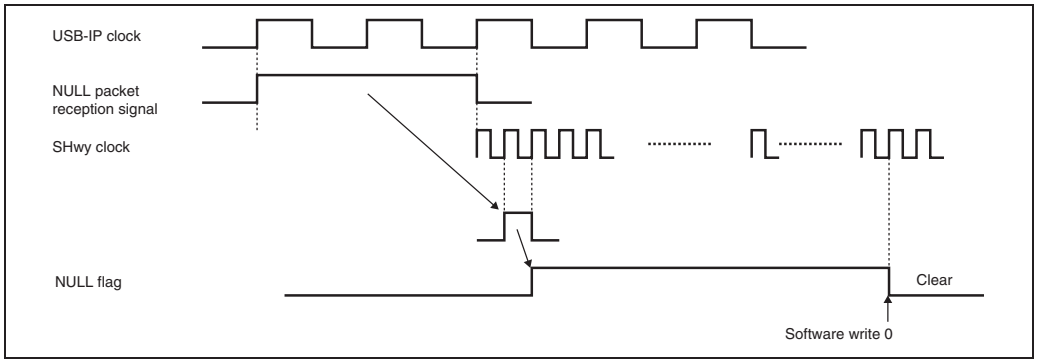


Figure 62.5 NULL Packet Receive Interrupt (NULL) Generation Timing

(4) Timeout interrupt (TO flag)

Can be generated when the time period that is specified in the timeout constant register (USBDMA_TOCSTR_0 or USBDMA_TOCSTR_1) elapses after the final transfer request is received from the USB-IP. On detecting the final transfer request, the internal counter is loaded with the value set in the USBDMA_TOCSTR_x register and starts counting down. When the counter reaches 0, it generates a timeout interrupt. Note that the DMA transfer control in this module, such as stop, suspend, or resume, is not affected when a timeout interrupt occurs. The TO bit is cleared by writing 0 to it after reading it as 1 by software. Figure 62.6 and 62.7 show the timeout interrupt generation timing.

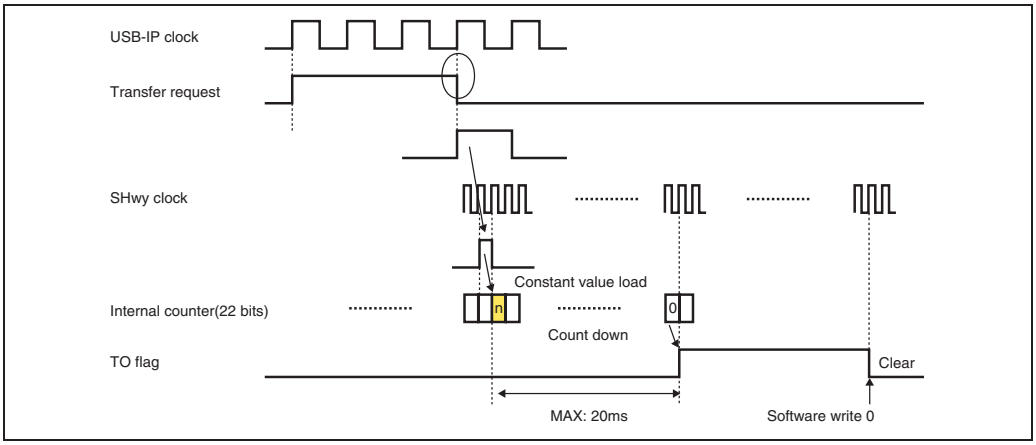


Figure 62.6 Timeout Interrupt (TO) Generation Timing

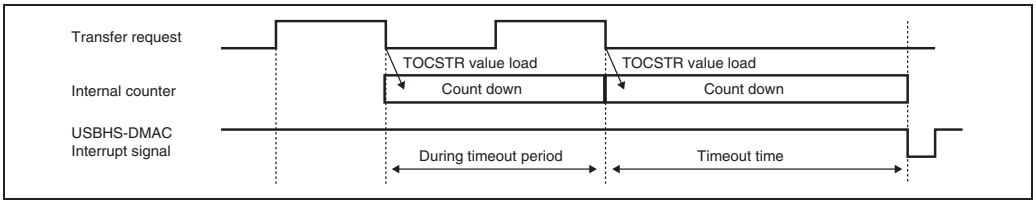


Figure 62.7 Timeout Interrupt Timing

The functions described in 62.3.1(5) to 62.3.1(9) are added to detect and notify the transitions on an individual signal line to the software, but no use is defined. They can be used as required.

(5) Transaction end detect interrupt (TR flag)

Can be generated when the end of a transaction is detected within the USB-IP. Note that the TR bit in the USBDMA_CHCR_x register and the TR0 or TR1 bit in the USBDMA_DMICR register are not reflected in the interrupt signal when the TRE bit in the USBDMA_CHCR_x register is set to 0.

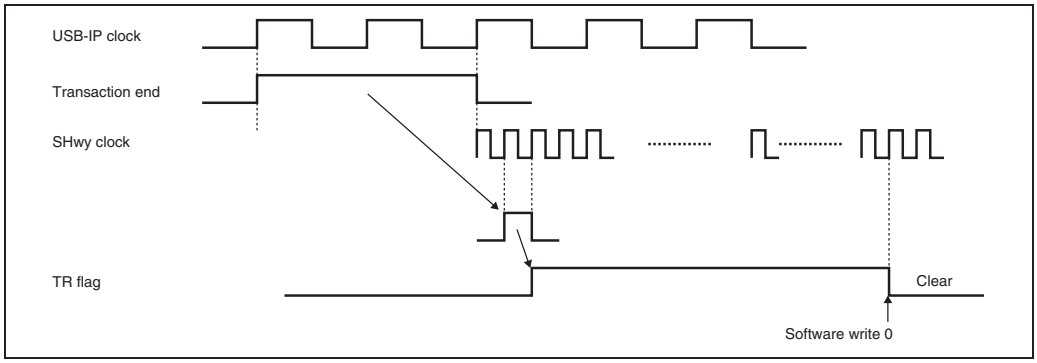


Figure 62.8 Transaction End Detect Interrupt Timing

(6) Buffer end detect interrupt (BUF flag)

Can be generated when the end of the buffer in the USB-IP is detected. Note that the BUF bit in the USBDMA_CHCR_x register and the BUF0 or BUF1 bit in the USBDMA_DMICR register are not reflected in the interrupt signal when the BUFE bit in the USBDMA_CHCR_x register is set to 0.

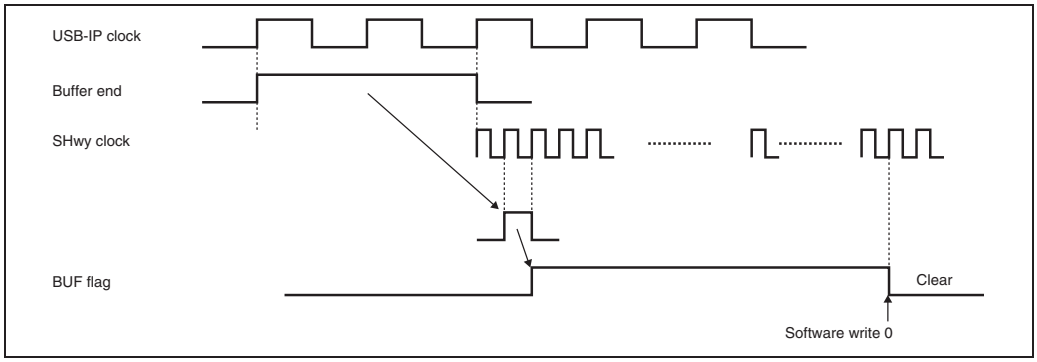


Figure 62.9 Buffer End Detect Interrupt Timing

(7) Final buffer access detect interrupt (RW flag)

Can be generated when the final access to the buffer in the USB-IP is detected. Note that the RW bit in the USBDMA_CHCR_x register and the RW0 or RW1 bit in the USBDMA_DMICR register are not reflected in the interrupt signal when the RWE bit in the USBDMA_CHCR_x register is set to 0.

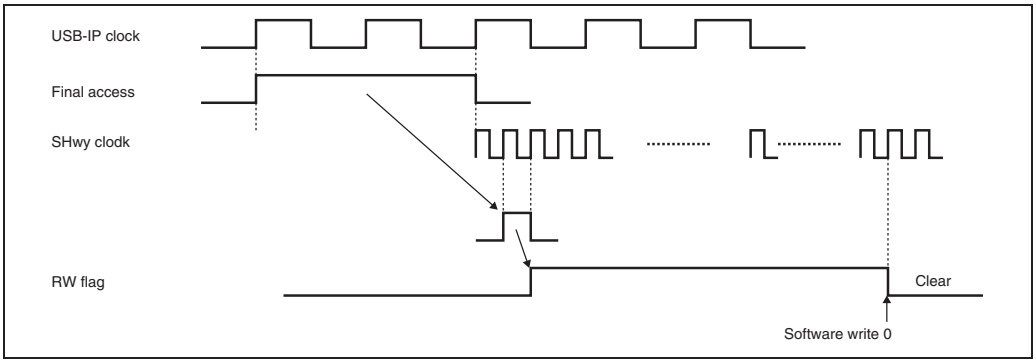


Figure 62.10 Final Buffer Access Detect Interrupt Timing

(8) Address error detection

This is a flag that indicates an address error interrupts has occurred when setting the source address register (USBDMA_SAR0 to USBDMA_SAR1) and the destination address register (USBDMA_DAR0 to USBDMA_DAR1). When the value written to the USBDMA_SAR or USBDMA_DAR register differs from the transfer size (TS) boundary, and when the TS bits are set to 11 (setting prohibited), the AE bit in the USBDMA_DMAOR register is set to 1. There is no distinction between CH0 and CH1 for an address error (the AE bit is set to 1 when an address error occurs on CH0 or CH1).

While the AE is set, no DMA transfer is allowed even if the DE bit in the USBDMA_CHCR_x register and the DME bit in the USBDMA_DMAOR register are set to 1. The address error interrupt is cleared by setting correct addresses in USBDMA_SAR_x and USBDMA_DAR_x.

Table 62.8 Address Error Detection Conditions When Setting Transfer Sizes

Transfer Size	Address Error Detection Conditions
TS=00 (8-byte transfer)	When data that is not aligned to 8-byte boundaries is written to the SAR/DAR registers (Writes to the SAR/DAR registers are valid.)
TS=01 (16-byte transfer)	When data that is not aligned to 16-byte boundaries is written to the SAR/DAR registers (Writes to the SAR/DAR registers are valid.)
TS=10 (32-byte transfer)	When data that is not aligned to 32-byte boundaries is written to the SAR/DAR registers (Writes to the SAR/DAR registers are valid.)
—	When b'11 (setting prohibited) is written to the TS register (Writes to the TS register are valid.)

(9) Response packet error detection

This function reports response packet errors when the interface between the SHwy and this module is accessed in ways that are not listed in table 62.2.

(a) Transmitting response packet errors

When a response packet error occurs during accessing from the SHwy to this module, the err_snt bit in the USBDMA_VCR register is set to 1.* The error signal is also sent to the SHwy bus if the RM bit in the USBDMA_DMAOR register is 0. If the RM bit is set to 1, the error signal is masked (0 is signaled).

Note: When a response packet error occurs, the err_snt bit is set to 1 regardless of the RM bit setting. The err_snt bit is cleared by writing 0 after reading 1.

Table 62.9 Response Packet Error Generation

USBDMA_DMAOR (RM bit) Setting	1 (Mask Mode)	0 (Normal Mode)
Response packet error signal notification to SHwy	Signals the fixed value (0) to the SHwy bus without determining if there is a response packet error.	Reports a response packet error to the SHwy bus when its is accessed with a transfer size other than those supported in this module (4-byte read/write and 8-byte read).

(b) Receiving response packet errors

When a response packet error occurs during accessing from this module to the SHwy, the err_rcv bit in the USBDMA_VCR register is set to 1. The TID bit in the USBDMA_DMAOR register indicates on which channel of this module the error has occurred (TID[1]=1 means it has occurred on CH1 and TID[0]=1 on CH0).

The err_rcv bit is cleared by writing 0 after reading 1.

62.3.2 DMA Transfer Function

(1) Operating mode

The following operating modes (1) to (3) are supported according to the setting of the PR bit in the DMA operation register (USBDMA_DMAOR).

(a) CH0 first control

Forces CH1 to wait to start a DMA transfer until a DMA transfer completes on CH0.

When there is a timing conflict in starting a DMA transfer between CH0 and CH1, CH0 takes precedence over CH1. If a DMA transfer is in progress on CH1 when CH0 tries to start a DMA transfer, CH0 waits to start it until the ongoing DMA transfer completes on CH1.

(b) CH1 first control

Forces CH0 to wait to start a DMA transfer until a DMA transfer completes on CH1.

When there is a timing conflict in starting a DMA transfer between CH1 and CH0, CH1 takes precedence over CH0. If a DMA transfer is in progress on CH0 when CH1 tries to start a DMA transfer, CH1 waits to start it until the ongoing DMA transfer completes on CH0.

(c) Round-robin control

Assigns the lowest priority to the last channel that has completed a transfer. In the initial state, CH0 takes precedence over CH1.

When there is a timing conflict in starting a DMA transfer between CH0 and CH1, the channel with a higher priority is granted to start the transfer and the lower priority channel is forced to wait. If a DMA transfer is in progress on the lower priority channel when the higher priority channel tries to start a DMA transfer, the higher priority channel waits to start it until the ongoing DMA transfer completes on the lower priority channel.

Figure 62.11 shows an overview of the processing of the SHwy bridge in each operating mode.

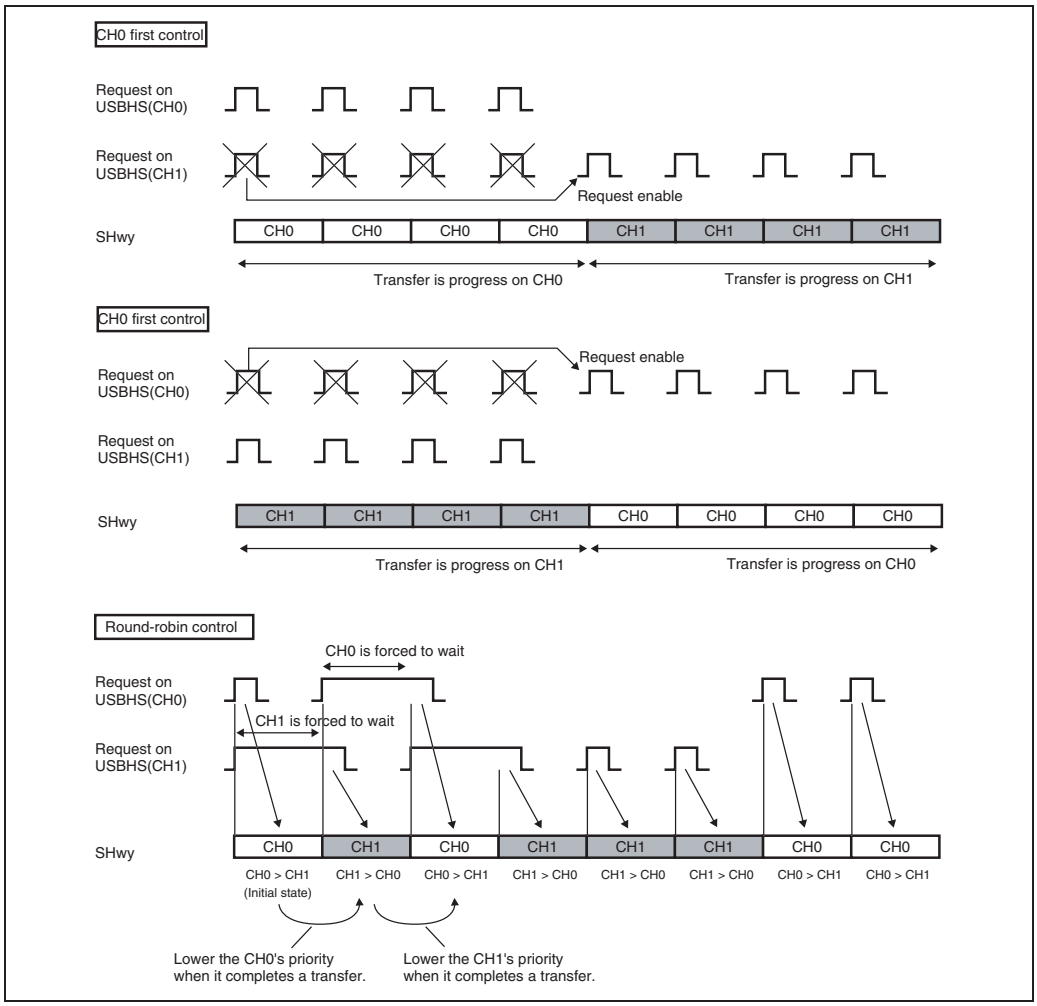


Figure 62.11 Overview of SHwy Bridge Processing in Each Mode

(2) Transfer size

The transfer size on the SHwy can be selected by setting the channel control register (the TS bit).

8-, 16-, and 32-byte can be set for each channel independently.

The following consideration should be observed during IN transfers.

The minimum transfer size that can be set to the TS bit is 8 bytes while the USB-IP can control transfers in 1-byte units. For example, if valid transfer data that is "8 x (n-1) + α" (α is less than 7 bytes) in size is to be transferred to the USB-IP with the transfer size set to 8 bytes and the transfer count set to n, α is transferred as a valid transfer unit by controlling byte enables according to the DMA final transaction valid data transfer enable register (the EDTEN bits) setting. Likewise, data is transferred in "transfer size x transfer count" (the final transaction is controlled by EDTEN) for 16- and 32-byte transfer sizes. The EDTEN setting is valid only for IN transfer and is don't care for OUT transfer.

Figure 62.12 shows an example of EDTEN setting. When only EDTEN31 in EDTEN31 to EDTEN0 is 1 , one byte is enabled. When only EDTEN31 and EDTEN30 in EDTEN31 to EDTEN0 are 1 , two bytes are enabled. Therefore, the total transfer volumes in the example shown above are calculated as "(32 bytesx(n-1)) bytes+10 bytes" for 32-byte transfer, "(16 bytesx(n-1)) bytes+7 bytes" for 16-byte transfer, and "(8 bytesx(n-1)) bytes+2 bytes" for 8-byte transfer. EDTEN15 to EDTEN0 in 16-byte transfer, EDTEN23 to EDTEN0 in 8-byte transfer are invalid (their values are ignored).

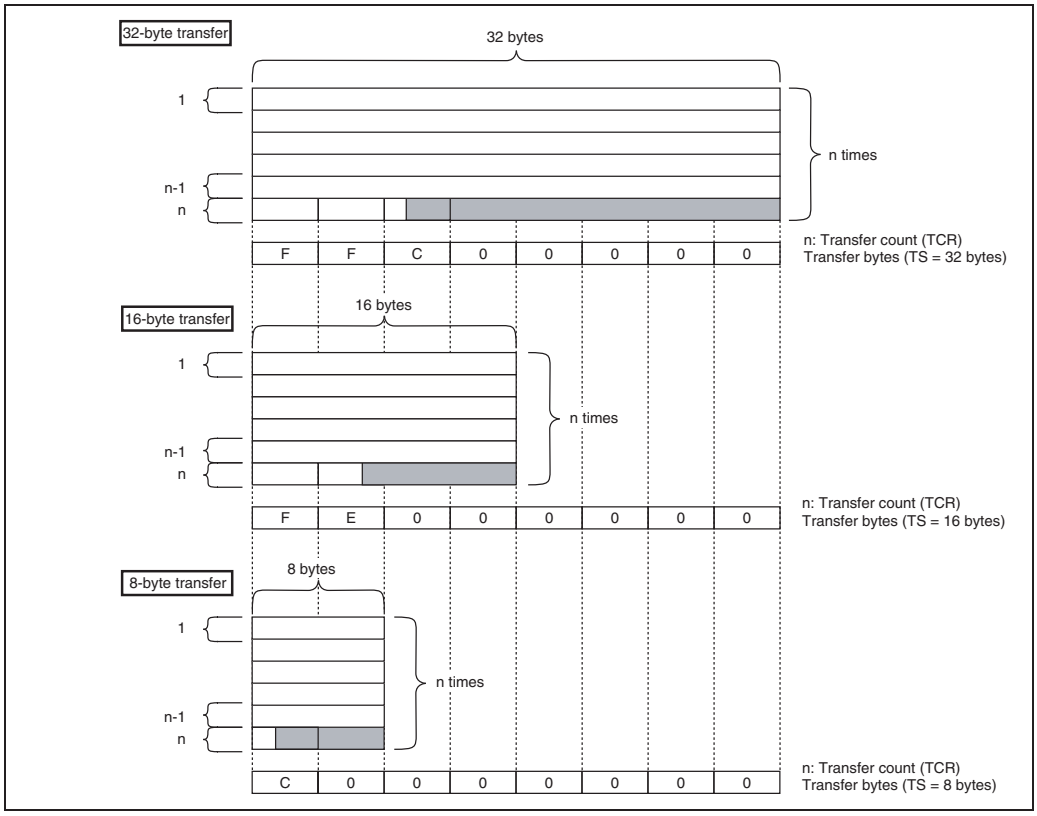


Figure 62.12 Example of Final Transaction Valid Data Transfer Enable (EDTEN) Setting

(3) DMA transfer flow

After the DMA source address register (USBDMA_SAR), DMA destination address register (USBDMA_DAR), DMA transfer count register (USBDMA_TCR), DMA channel control register (USBDMA_CHCR), final valid data transfer enable register (USBDMA_TEND), and DMA operation register (USBDMA_DMAOR) are set appropriately, the DMAC starts data transfer in the following sequence. The DMA timeout constant register (USBDMA_TOCSTR) may also need to be set.

If the transfer enabling conditions are set as DE=1, DME=1, TE=0, AE=0, SP=0, and (TR=0, BUF=0, RW=0), transfers are performed according to the transfer request enables and transfer requests from the USB-IP. The transfer direction (IN/OUT transfer) is determined by the direction signal from the USB-IP. The transfer size is determined by the setting of TS1 to TS0.

Every time one SHwy transaction (in the transfer size specified in the TS bit) completes, the internal counter of this module decrements the USBDMA_TCR value by one. When the specified transfer count ends (the USBDMA_TCR value reaches 0), it means all transfers complete. At this time, an USBHS1-DMAC interrupt is generated if the IE bit in the USBDMA_CHCR register is set to 1.

When a NULL packet is received, transfer can be stopped or restarted by setting FTE=1 after negating the DREQE register of the USBHS1 module. Follow the steps described later in "Control when a NULL packet is received".

Table 62.10 shows the conditions for each DMA transfer.

Table 62.10 DMA Transfer Conditions

Transfer enabling condition	TE=0, SP=0, (*TR=0, BUF=0, RW=0)
Transfer (starting) condition	When a transfer request is enabled by the USB-IP When a transfer request is issued by the USB-IP
Transfer completing (then restarting) condition	When the transfer count ends (the TE flag is set to 1), (can be restarted by setting DE and DME to 1.) When FTE=1 (when DREQE=1 in the USBHS1 module is also set), and the steps described later should be followed. When reset (can enter into standby state by releasing the reset.)
Transfer suspending (then resuming) condition	When DE=0 or DME=0 (can be resumed by setting DE=1 or DME=1.) When SP=1 (can be resumed by clearing the SP flag.) When RW=1, BUF=1, and TR=1 (can be resumed by clearing the RW, BUF, and TR flag.)* When the module stops (can be resumed by resuming the module.)

Note: * Can be ignored when the RWE, BUFE, and TRE registers are disabled (set to 0).

Figure 62.13 illustrates the high-level DMA transfer flow.

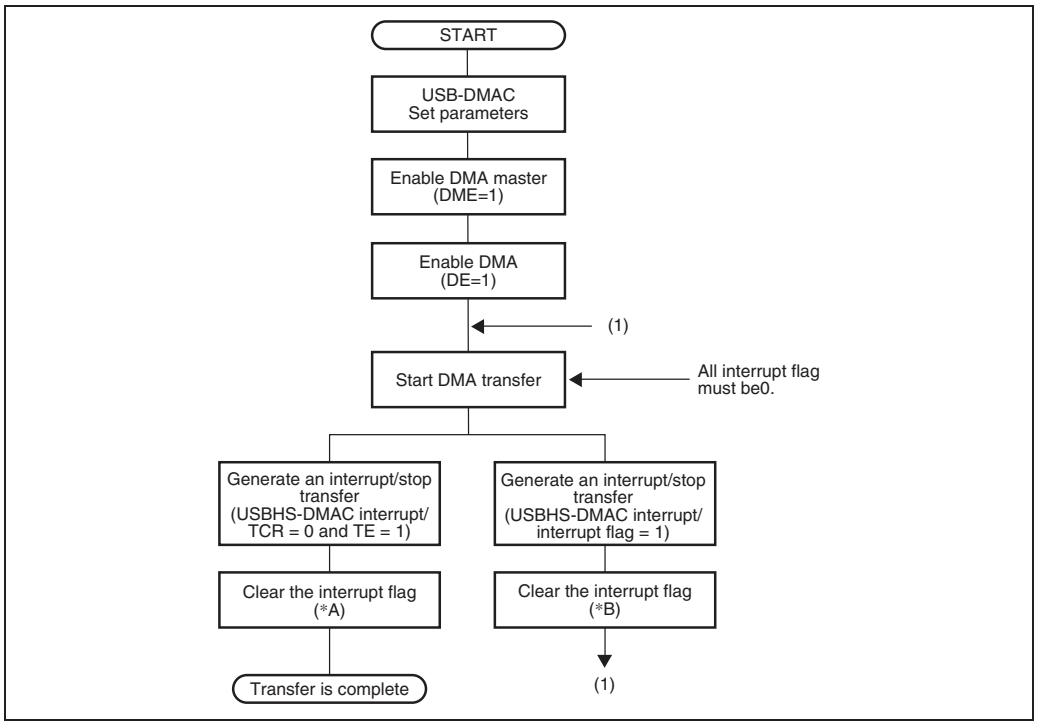


Figure 62.13 DMA Transfer Flow Overview

Where A and B apply to the following flags:

(Note that RW, BUF, and TR are not set when RWE, BUFE, and TRE are disabled, respectively.)

* A: TE flag

* B: SP,(RW,BUF,TR) flags

When to change USB-DMAC parameters

USB-DMAC parameters (such as destination address or transfer count) should be changed while all interrupt flags are cleared and DE=0 and DME=0 are set (a transfer is started with the latest parameters when DME=1 and DE=1 are set). Furthermore, USB-DMAC parameters should not be changed while the DMA is enabled (DME=1 and DE=1).

What to do if freeze

If a transfer should freeze during operation, issue a software reset after setting DE=0 and DME=0 and clearing all interrupt flags. All hardware except configuration registers is initialized. Restart by setting DME and DE to 1 after updating USB-DMAC parameters if necessary.

Control when a timeout occurs

Since this module assumes bus access in the transfer units listed in table 62.2, it cannot be restarted when a timeout occurs in an irregular case where it is being accessed with any size that are not in the table. This irregular case should be handled by software, such as by issuing a software reset (to both CH0 and CH1).

Control when a NULL packet is received

When a NULL packet is received during a DMA transfer, the DMA transfer can be suspended and resumed on each channel independently by controlling the FTE bit of this module and the DREQE bit of the USBHS1 module in the following sequence.

[Control sequence]

During a DMA transfer (A)

(1) A NULL packet is received (an interrupt is generated and the NULL flag is detected).

(2) The DREQE bit of the USBHS1 module is negated (=0).

(3) Wait for the internal bus to be stabilized.

(4) Perform three actions at the same time; setting the FTE bit, clearing the NULL bit and negating the DE bit.

An interrupt is generated due to TE.

(5) Clear the interrupt caused by TE.

(6) Set the parameters (such as TCR or DAR) for the next transfer.

(7) Assert the DE bit (=1). The DMA is restarted.

(8) Assert the DREQE bit (=1).

Start a DMA transfer (B).

[Restrictions]

1) FTE bit set timing

   If this module is accessing the SHwy (SHBSYx bit=1) when setting the FTE bit, you need to wait to set the FTE register until this module's internal buffer is empty and the SHwy bus access is complete (SHBSYx bit=0). Note that if you accidentally set the FTE register while an SHwy bus access is in progress, the transfer fails and transfer data may be lost or the transfer may be unable to be restarted.

2) DREQE register assert (negate clear) timing

   It is necessary to allow at least 20clk@ZSϕ after the DE bit is asserted and before the DREQE is asserted. This is because DREQE needs to be asserted after transfers enabled by the DE bit are ready internally to be started. Asserting DREQE immediately after DE may cause malfunction such as initiating unnecessary bus access.

3) Fractional byte and NULL packet reception

   This module assumes bus access in the transfer units listed in table 62.2 and goes out of control when it receives a NULL packet in an unsupported transfer unit. Therefore, data transfer in any transfer unit that is not in the table is prohibited.

4) IN/OUT switching after NULL packet reception

   After a NULL is received, transfers cannot be restarted with the transfer direction switched from OUT to IN. This is because this module still considers the terminated transfer as an OUT transfer until the transfer count reaches its end. Note that if you switch the transfer direction to IN transfer accidentally after a NULL packet is received, a conflict occurs between an IN and an OUT transfers, which may cause illegal bus access.

   Use CH0 and CH1 with their transfer direction fixed, or if the transfer direction needs to be switched on the same channel, make sure to do it every time a transfer completes successfully due to the end of transfer count or is terminated by software reset.

Figure 62.14 shows the state transitions for DMA transfers.

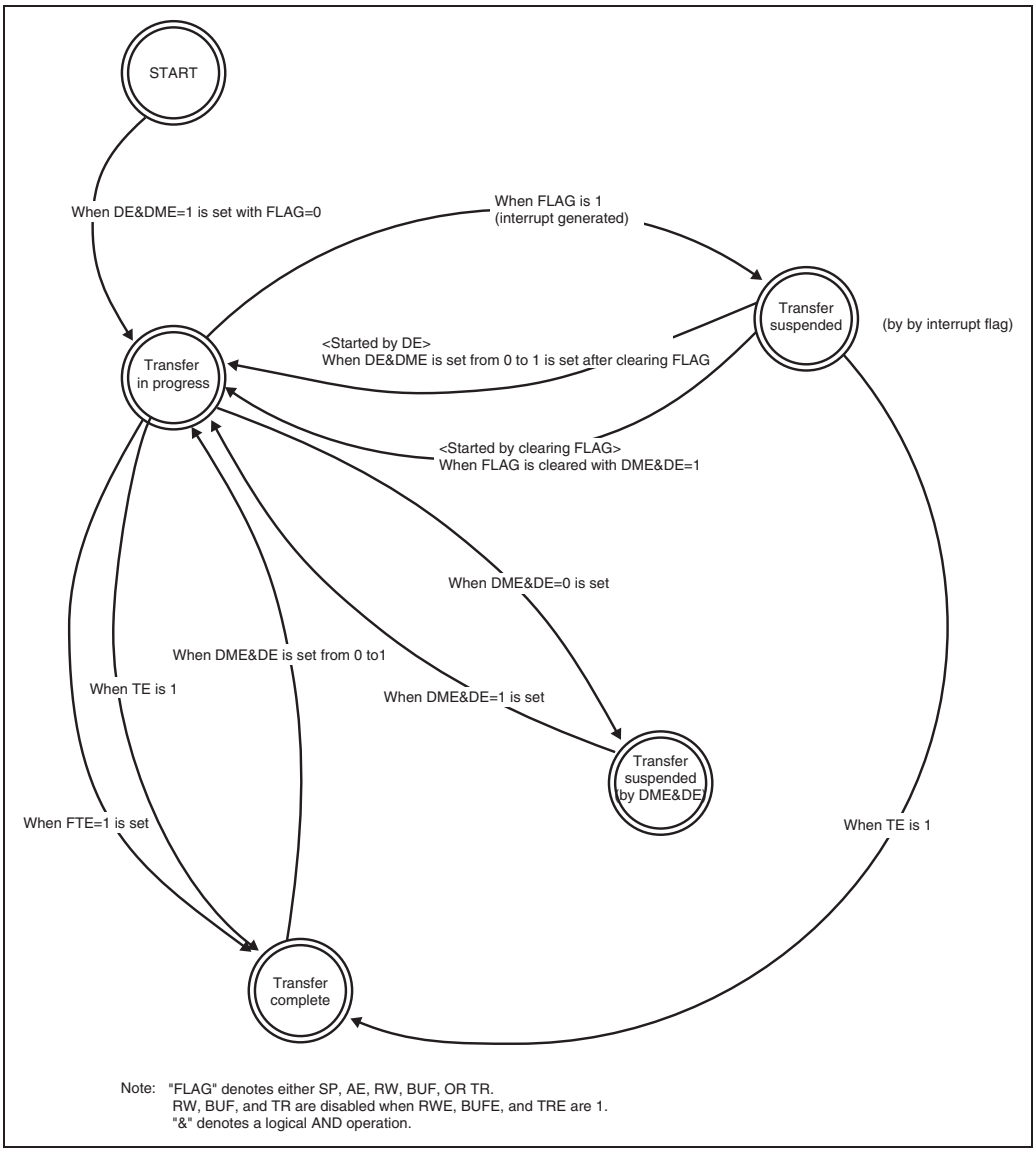


Figure 62.14 State Transitions for DMA Transfer

(4) Control Sequence

Figure 62.15 shows an outline of the control sequence of this module.

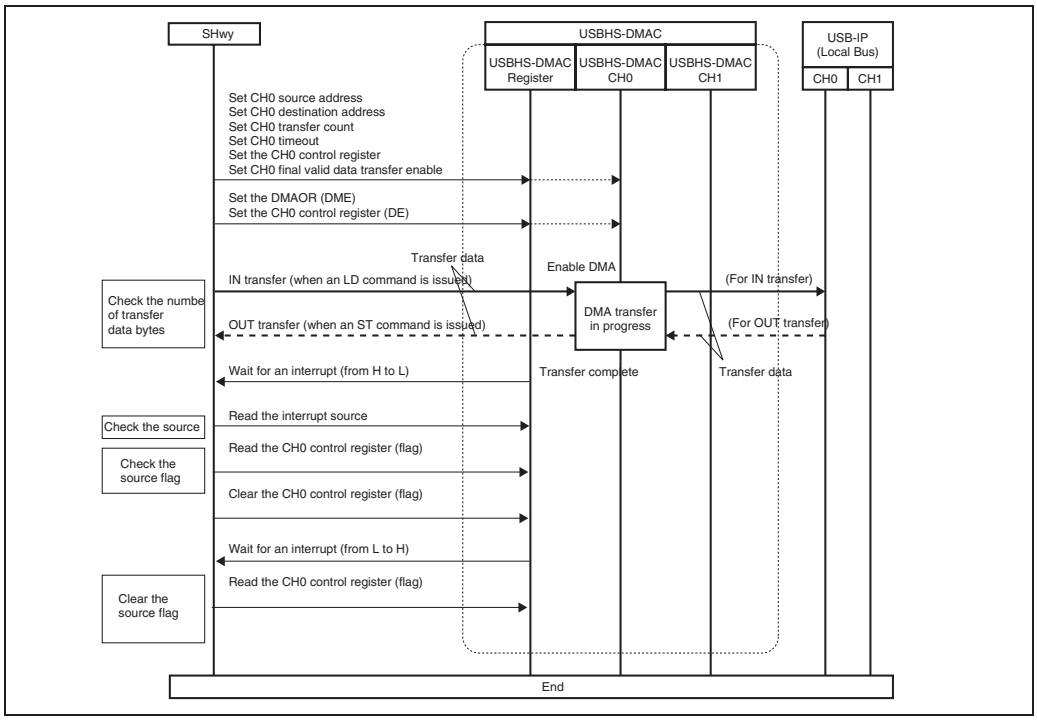


Figure 62.15 Control Sequence Overview

(5) Internal Buffer Configuration

This module has 64 bytes (64 bitsx8 words) of internal buffer for each of two channels. Thus, the total capacity of this module's internal buffers is 128 bytes (1024 bits).

The internal buffers are composed of two planes each of which is organized as 64 bits x 4 words and are readable /writable on per-plane basis from the USB-IP local bus or SHwy bus (plane 1 is writable when plane 0 is readable or vice versa). For 16-byte transfers, only 2 words in plane 0 and 2 words in plane 1 are used. For 8-byte transfers, only 1 word in plane 0 and 1 word in plane 1 are used.

Note that these internal buffers cannot be accessed directly by software.

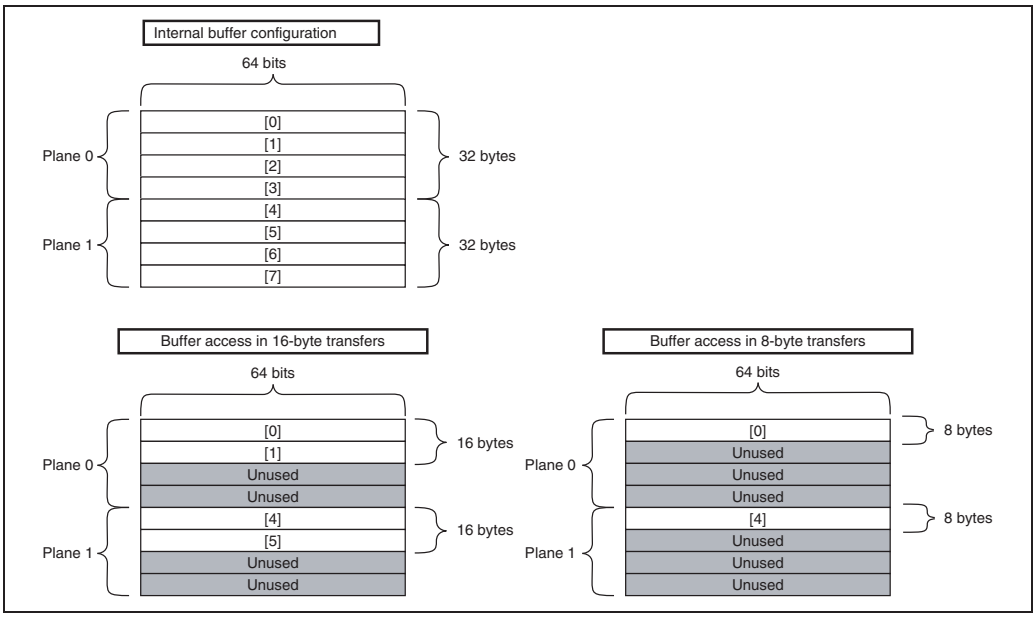


Figure 62.16 Internal Buffer Configuration and Used Area for Each Transfer Size

(6) Internal Buffer Control (Hardware Control, For reference)

(a) IN transfer (from SHwy to USB)

Retrieves transfer data from a source on the SHwy bus and writes it to this module's internal buffer. Reads the written data from the internal buffer and writes it to the USB-IP.

Figure 62.17 shows how the planes of this module's internal buffers are controlled during an IN transfer. In this figure, "read' and 'write" indicate read/write operations to this module's internal buffers.

When a write to plane 0 or plane 1 is complete, the writable plane flag is toggled (every time 2 words* and 1 word* are written for 16-byte and 8-byte transfers, respectively). When a read from plane 0 or plane 1 and a transfer the read data to the USB-IP are complete, the readable plane flag is toggled (every time 2 words* and 1 word* are read for 16-byte and 8-byte transfers, respectively). Access to the SHwy is prohibited during the period when both the writable plane flag and readable plane flag are set on the same plane as a read/write access conflict may occur.

* 1 word=64 bits

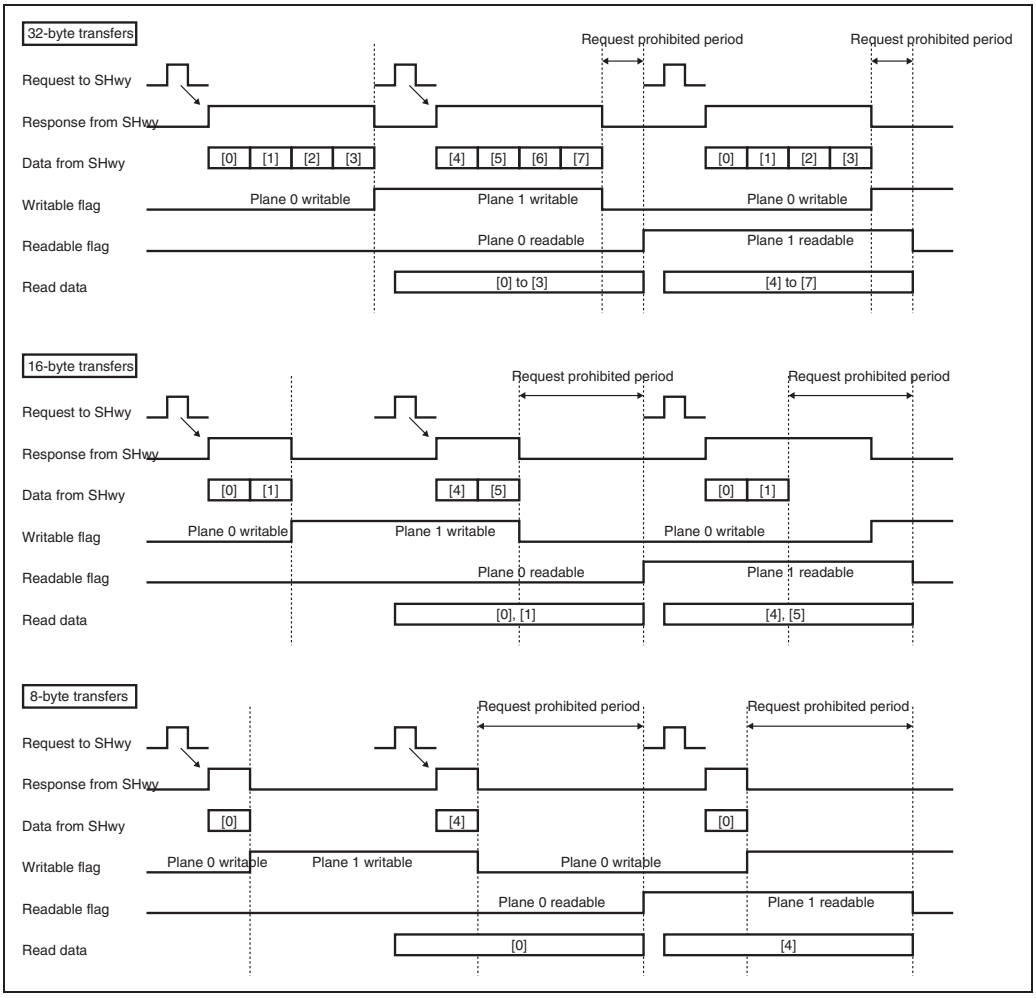


Figure 62.17 Read/Write Control for Internal Buffer: From SHwy to USB (IN Transfer)

(b) OUT transfer (from USB to SHwy)

Writes data read from the USB-IP to the internal buffers. Reads the written data from this module's internal buffers and writes it to the destination on the SHwy bus (OUT transfer).

Figure 62.18 shows how the planes of this module's internal buffers are controlled during an OUT transfer. In this figure, "read' and 'write" indicate read/write operations to this module's internal buffers.

When a write to plane 0 or plane 1 is complete, the writable plane flag is toggled (every time 2 words* and 1 word* are written for 16-byte and 8-byte transfers, respectively). When a read from plane 0 or plane 1 is complete, the readable plane flag is toggled (every time 2 words* and 1 word* are read for 16-byte and 8-byte transfers, respectively). Access to the SHwy is prohibited during the period when both the writable plane flag and readable plane flag are set the same plane as a read/write access conflict may occur.

* 1 word=64 bits

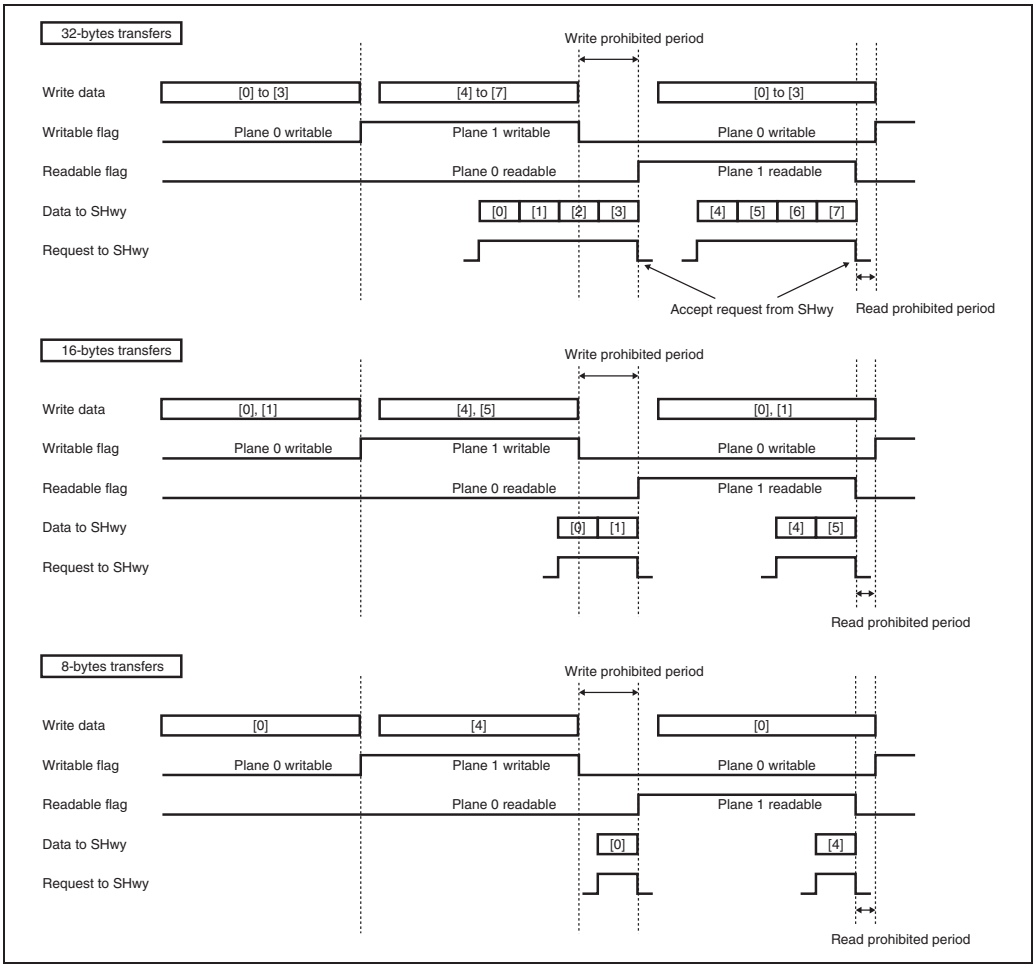


Figure 62.18 Read/Write Control for Internal Buffer: From USB to SHwy (OUT Transfer)

Appendix A Package Dimensions

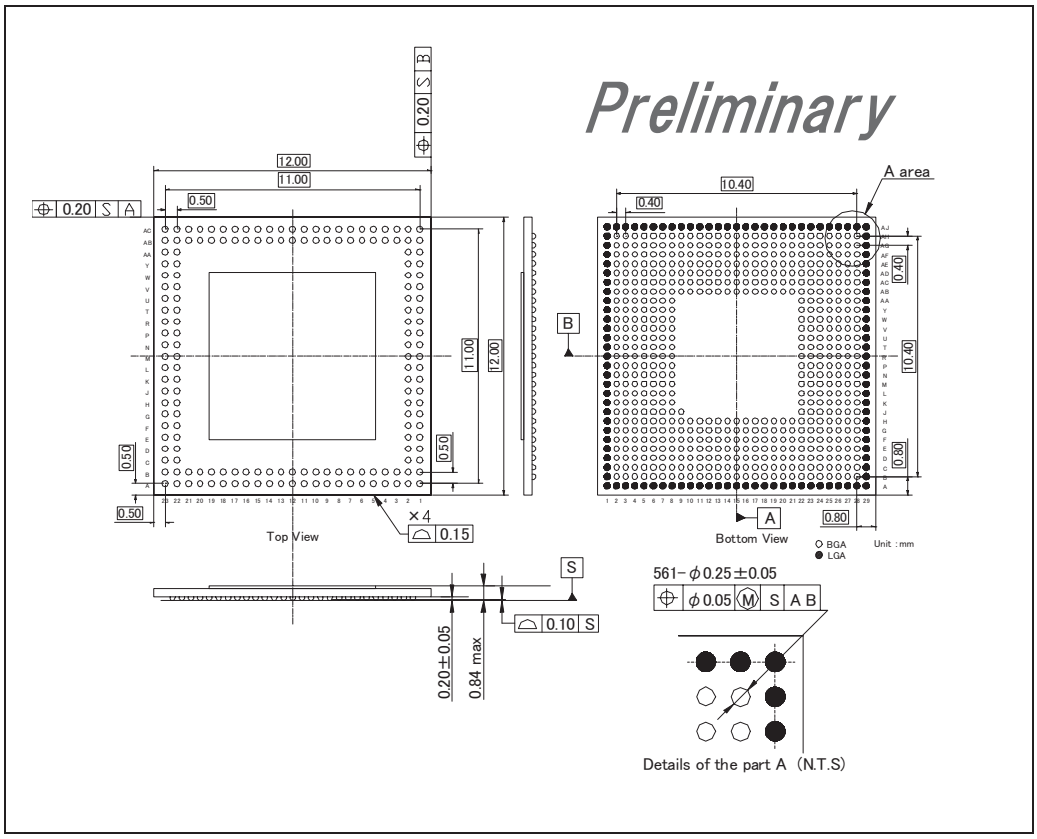


Figure A.1 Package Dimensions (Preliminary)

Appendix B MMFROM Program Functional Specifications

B.1 Overview

This section defines the functional specifications for an MMFROM program (hereafter referred to as mask ROM) loaded to the SH-Mobile AP4 (hereafter referred to as AP4).

The program will be executed when the AP4 is activated. After the initial settings have been made in the LSI, a program in the external device is executed or a program is downloaded from the USB or ACMFI.

B.1.1 Operating Modes

The AP4 has the following boot modes which can be selected by the MD pins as shown in table B.1.

- BSC boot mode (expansion boot options are included)
- BSC development boot mode (expansion boot options are included)
- NAND(4) boot mode
- NAND(4) development boot mode
- NAND(5) boot mode
- NAND(5) development boot mode
- eSD boot mode
- eSD development boot mode
- eMMC boot mode 1A (MFI pins, user area)
- eMMC boot mode 1B (BSC pins, user area)
- eMMC boot mode 2A (MFI pins, boot partition)
- eMMC boot mode 2B (BSC pins, boot partition)
- eMMC development boot mode 1A (MFI pins, user area)
- eMMC development boot mode 1B (BSC pins, user area)
- eMMC development boot mode 2A (MFI pins, boot partition)
- eMMC development boot mode 2B (BSC pins, boot partition)
- Forcible USB boot mode
- MFI1 boot mode (ADDEMUX)
- MFI1 development boot mode (ADDEMUX)

- MFI2 boot mode (ADMUX)
- MFI2 development boot mode (ADMUX)

The above modes which are initiated from mask ROM are described in this section.

The mode can be determined by referencing the MD7, MD6, MD4, MD3, and MD2 bits in RESCNT (SYSC register).

Table B.1 MD Pin Settings

TST	MD4	MD3	MD2	MD6	MD7	Mode Name	Secure Function	Remarks
1	0	0	0	1	0	MFI2 development boot (ADMUX)	No	
1	0	0	0	1	1	MFI1 development boot (ADDEMUX)	No	
1	0	0	1	0	0	MFI2 boot (ADMUX)	Yes	
1	0	0	1	0	1	MFI1 boot (ADDEMUX)	Yes	
1	0	0	1	1	0	MFI2 boot (ADMUX)	Yes	
1	0	0	1	1	1	MFI1 boot (ADDEMUX)	Yes	
1	0	1	0	0	0	eMMC development boot 2B	No	
1	0	1	0	0	1	eMMC development boot 2A	No	
1	0	1	0	1	0	eMMC development boot 1B	No	
1	0	1	0	1	1	eMMC development boot 1A	No	
1	0	1	1	0	0	eMMC boot 2B	Yes	
1	0	1	1	0	1	eMMC boot 2A	Yes	
1	0	1	1	1	0	eMMC boot 1B	Yes	
1	0	1	1	1	1	eMMC boot 1A	Yes	
1	1	0	0	1	0	NAND(4) development boot	No	
1	1	0	0	1	1	NAND(5) development boot	No	
1	1	0	1	0	0	Reserved	Yes	
1	1	0	1	0	1	Reserved	Yes	
1	1	0	1	1	0	NAND(4) boot	Yes	
1	1	0	1	1	1	NAND(5) boot	Yes	
1	1	1	0	0	0	BSC development boot	No	
1	1	1	0	0	1	eSD development boot	No	
1	1	1	0	1	0	Reserved	No	
1	1	1	0	1	1	Reserved	No	
1	1	1	1	0	0	BSC boot	Yes	
1	1	1	1	0	1	eSD boot	Yes	
1	1	1	1	1	0	Forcible USB boot	Yes	
1	1	1	1	1	1	Reserved	Yes	

Note: eMMC boot modes

1A: Uses the MFI pins and boots from the user area.

1B: Uses the BSC pins and boots from the user area.

2A: Uses the MFI pins and boots from the boot partition.

2B: Uses the BSC pins and boots from the boot partition.

B.2 Notes on Hardware Configuration

B.2.1 RAM

The mask ROM uses MERAM as a work area and stack.

The SDRAM related registers (SBSC) are not set.

B.2.2 Connected Device

- For BSC boot mode and BSC development boot mode

  A device that can be accessed with a 16-bit bus and the AP4 initial settings needs to be connected to CS0 (asynchronous bus).

  When performing clock up, the BSC must operate with the AP4 initial settings and the BSC module clock must be 100 MHz.

  When the copy boot option is specified, a program is read out from the lower address in the address order as 16-bit data, and then copied to MERAM.
- For NAND(4) boot mode, NAND(5) boot mode, NAND(4) development boot mode, and NAND(5) development boot mode

  A device with the NAND interface must be connected to the FLCTL and the following conditions (a) to (f) must be met. (For the FLCTL settings, refer to appendix B.7, Settings.)

  (a) The size of one page must be 1 Kbyte + 32 words (16 bits).

  (b) The following command codes must be used.
  - Read command: Cycle 1: 00h, cycle 2: 30h

    The address data issued at the address stage must be 4 bytes or 5 bytes.

    For NAND(4) boot mode and NAND(4) development boot mode: 4 bytes

    For NAND(5) boot mode and NAND(5) development boot mode: 5 bytes
  - Reset command: FFh
  - Status command: 70h

    (In the status data, bit 6 indicates the status as 1: Ready, 0: Busy)

  (c) Connection must conform to the FLCTL pin configuration.
  - The Ready/Busy pin is connected to the FRB pin.
  - The Chipenable pin is connected to the FCE1 pin (multiplexed CS5B/FCE1 pin).

  (d) The device must be able to use 4-symbol ECC for the requested ECC correction. (ECC of four symbols is used.)

(e) Operation must be at 13 MHz with 8-cycle pitch. In addition, operation must be performed with the following clocks when clock up is set.
- 400 MHz is specified: 100 MHz, 16-cycle pitch
- 800 MHz is specified: 100 MHz, 8-cycle pitch

(f) The device can be booted when the first command sent to NAND is a reset command and the next command is a read command with address 0 specified.

- For eSD boot mode and eSD development boot mode

  Only one eSD device that can be connected to the SDHI1 should be connected. Also, the eSD device needs to meet the following conditions (a) to (d).

  (a) The device must satisfy the eSD (Embedded SD) Specification Version 2.10.

  (b) VDDH and VDDF of the device must be between 2.7 V and 3.6 V.

  (c) Physical partition ID #1 must be already created or can be created in the device.

  (d) The device must support the FAST BOOT mode.

- For eMMC boot mode 1A, eMMC boot mode 1B, eMMC development boot mode 1A, and eMMC development boot mode 1B

  Only one eMMC device that can be connected to the MMCIF should be connected. Since the port pins are multiplexed, either the MFI pins or BSC pins are selected depending on the mode.

  Also, the eMMC device needs to meet the following conditions (a) to (d).

  (a) The eMMC device must satisfy the MMCA 4.2 (JESD84-A42) standard.

  (b) The physical format specifications must be satisfied (see appendix B.6.4).

  (c) The power-on time must be within 25 ms.

  (d) Access to the eMMC device in 8 bits or 4 bits must be possible.

- For eMMC boot mode 2A, eMMC boot mode 2B, eMMC development boot mode 2A, and eMMC development boot mode 2B

  Only one eMMC device that can be connected to the MMCIF should be connected. Since the port pins are multiplexed, either the MFI pins or BSC pins are selected depending on the mode. Boot operation mode is used in these modes.

  Also, the eMMC device needs to meet the following conditions (a) to (g).

  (a) The eMMC device must satisfy the MMCA 4.3 (JESD84-A43) or MMCA 4.4 (JESD84-A44) standard.

  (b) The power-on time must be within 25 ms.

  (c) BOOT_PARTITION_ENABLE in PARTITION_CONFIG of EXT_CSD must be set to H'1 or H'2.

  (d) BOOT_ACK in PARTITION_CONFIG of EXT_CSD must be set to H'1.

  (e) BOOT_BUS_WIDTH of EXT_CSD must be set to H'2 (8-bit bus).

(f) A program that satisfies the physical format specifications (see appendix B.6.5) must be written in the boot partition.

(g) The eMMC device must be in the pre-boot state when eMMC boot mode operation starts. (Connecting NBRSTOUT to RST_n is recommended in an MMCA 4.4 device. For an MMCA 4.3 device, circuitry that allows the card power source to be turned on and off in synchronization with the reset signal is recommended.)

B.2.3 WDT Kick Processing

Mask ROM can be operated with the hardware initial values without setting channel 0 in the RWDT.

The counter of channel 0 in the RWDT needs to be cleared at regular intervals within the module that takes over processing from mask ROM.

In this section, the above process of regularly clearing the channel 0 counter in the RWDT is referred to as the WDT kick processing.

Mask ROM performs the WDT kick processing.

For details on how to set and clear the WDT, refer to section 12, RCLK Watchdog Timer (RWDT).

B.3 Functional Description

Mask ROM has the following functions.

- Function to perform mode transition by setting standby control registers and reference the mode transition result (boot control interface function)
- Function to reference the VRL4 (Verification Record List version 4) and execute a program in the device connected to CS0 of the BSC (BSC boot function)
- Function to reference the VRL4 and execute a program in the device connected to the FLCTL (NAND boot function)
- Function to download a program from the USB (USB download function)
- Function to transfer a program from the MFI and execute it (MFI boot function)
- Function to execute the secure check (secure boot function)
- Function to reference the VRL4 and execute a program in the device connected to the SDHI1 (eSD boot function)
- Function to reference the VRL4 and execute a program in the device connected to the MMCIF (eMMC boot function)

Table B.2 Boot Modes and Functions

Boot Mode	Boot Function	Boot Control Interface Function	USB Download Function	Secure Boot Function	Remarks
BSC boot mode	BSC boot function	O	O	O	
BSC development boot mode		O	O		
NAND boot mode	NAND boot function	O	O	O	
NAND development boot mode		O	O		
eSD boot mode	eSD boot function	O	O	O	
eSD development boot mode		O	O		
eMMC boot mode	eMMC boot function	O	O	O	
eMMC development boot mode		O	O		
MFI boot mode	MFI boot function			O	
MFI development boot mode					
Forcible USB boot mode	USB download only		O	O	

B.3.1 Boot Control Interface Function

The boot control interface function enables switching between the USB download function and boot functions of each boot mode by setting standby flag registers B2 and B3 (STBCHRB2 and STBCHRB3).

STBCHRB2 and STBCHRB3 are initialized only by a power-on reset using the $\overline{\text{RESETP}}$ pin. Making use of this characteristic, a mode transition in mask ROM is achieved by setting these registers to generate a power-on reset through software. Several bits which are provided for controlling mask ROM operation can be used to make a transition to the USB download function from a program other than mask ROM.

Table B.3 STBCHRB2 Settings

Bit	Name	Description	Remarks
7 to 5	Reserved		Rewriting is prohibited.
4	Reboot count over flag	Executes USB download depending on the reboot count. 0: Transition to USB download due to reboot count does not occur 1: Reboot count is equal to or higher than the predefined value	Rewriting is prohibited.
3	Secure error flag	Executes USB download when a secure check error occurs. 0: Secure check not performed 1: Secure check error	Rewriting is prohibited.
2	Mode pin specification flag	Mode pins are used to specify forcible USB boot. 0: Mode pins not checked 1: Forcible download by mode pin specification	Rewriting is prohibited.
1	Invalid VRL4 format flag	Executes USB download when the VRL4 format of the boot device is invalid. 0: Signature not checked 1: USB download due to invalid signature	Rewriting is prohibited.
0	Processing status flag	Executes USB download when there was an unpredictable error during mask ROM processing. 0: Processing has finished 1: During processing	Rewriting is prohibited.

Table B.4 STBCHRB3 Settings

Bit	Name	Description	Remarks
7 to 4	Reboot counter	Predefined reboot count The number of times reboot is performed is counted. A transition to USB download is made when the reboot count has reached the boot option setting at reboot.	Clearing by the user is possible. The counter must be cleared when the reboot check option has been specified. Only BSC boot is valid.
3 to 1	Reserved		
0	User specification	0: No specification 1: Specifies to transit to USB download	Rewriting by the user is possible. The secure check after transiting to USB download will be performed depending on the boot mode.

B.3.2 BSC Boot Function

The BSC boot function is used to initiate a program written to an external device in BSC boot mode or BSC development boot mode.

The external device write format needs to be in accordance with the description in appendix B.6.1, Flash ROM Format (VRL4 Format) (hereafter referred to as VRL4 format).

Description on operations:

1. When the signature value in the external device is the predefined value (value indicating that writing has been performed (VRL4 format)), the start address of the area to be booted is set as the boot address.

   When the copy size in the VRL4 is a value other than 0, the following operation can be selected as a copy boot option: copy a program for the specified size (up to 64 Kbytes while including the VRL4) to the fixed MERAM address and set the fixed MERAM address as the boot address. In this case, read operations, including the VRL4 format confirmation, start reading data from the lower address in 2-byte units in the address order.
2. A format check is performed for the VRL4 at the beginning of the boot address, and if the secure function is used, a secure check is performed for the specified area.
3. If the result of step 2 is correct, execution jumps to the start address of the VRL4.

   (If the result of step 2 is erroneous, a transition is made to the USB download function.)

B.3.3 NAND Boot Function

The NAND boot function is used to initiate a program written to a NAND device in NAND(4) boot mode, NAND(5) boot mode, NAND(4) development boot mode, or NAND(5) development boot mode.

The NAND device write format needs to be in accordance with the description in appendix B.6.2, NAND Physical Format, and data in the VRL4 format is stored. This function expands a program in MERAM according to the NAND physical format, performs the VRL4 format check and secure check as like the BSC boot function, and then performs boot processing.

Description on operations:

Carry out the NAND physical block format expansion with steps 1 to 4 and then perform step 5.

1. Read data from the beginning of the control block of the page (reading from pages 0 to 127), and search for the beginning of the boot block (H'5A5A).
2. On finding the beginning of the boot block, copy the data areas of that page to MERAM.
   Calculate the copy size of the boot block and the number of pages to be read from the VRL4 data structure in MERAM.
   (When an ECC error occurs, search for the next boot block (return to step 1).)
   (When the VRL4 data structure is erroneous, search for the next boot block (return to step 1).)
3. Read boot options from the beginning of the boot block with a valid VRL4 header, which was found first and perform clock up processing.
4. Continue to read sequentially from the next page of the found boot block. On finding a page with a page identifier of H'A5A5, determine it as a boot block and copy it to MERAM. Perform this until the specified number of pages has been found.
   (When an ECC error occurs, the block is determined as an invalid block. Start reading the next page.)
   (When an identifier of H'5A5A is found, carry out step 2.)
   (When the specified number of pages has been found, whether there is a subsequent page with a page identifier of H'A5A5 is not investigated.)
   (When the specified number of pages is not yet met after reading up to page 127, a transition is made to the USB download function.)
5. When boot block reading has completed, boot is performed from MERAM. (When a secure boot error occurs, a transition is made to the USB download function.)

- Definition of boot block

  The boot program code is stored in data areas and is configured with two or more pages. The identification data of the first page is H'5A5A, and the identification data of subsequent pages is H'A5A5.

  The data format has a structure in which the VRL4 is stored at the beginning and the boot program code is stored after that.

  More than one boot block can be located in pages 0 to 127.

  (Locating more than one boot block increases the error tolerance.)

B.3.4 eSD Boot Function

The eSD boot function is used to initiate a program written to an eSD device in eSD boot mode or eSD development boot mode.

The program to be written to the eSD device should be in a format conforming to the VRL4 format and should be stored in physical partition #1 of the eSD device.

Description on operations:

1. Read data from the sector 0 area in physical partition #1 of the eSD device and perform the VRL4 format check. (The FAST_BOOT function is used for reading data from the eSD device.)
2. If no errors were found by the format check, the program for the copy size in the VRL4 format and the secure data (288 bytes) are read from the eSD device and copied to the fixed MERAM address. (The maximum size of the program to be copied is 64 Kbytes + 288 bytes (VRL4 format is also included).)
3. When the secure function is used, a secure library is called and a secure check is applied to the specified area.
4. If no error has occurred performing steps 1 to 3, execution jumps to the start address of the program copied to MERAM.

   (If an error has occurred performing steps 1 to 3, the eSD boot function is aborted and a transition is made to the USB download function.)

B.3.5 eMMC Boot Function (MFI Pins/BSC Pins, User Area)

The eMMC boot function (1A/1B) is used to initiate a program written to an eMMC device in eMMC boot mode or eMMC development boot mode. The MMC port pins are multiplexed and the MD pins are used to select from among the MFI pins and BSC pins.

The program to be written to the eMMC device should be in a format conforming to the VRL4 format and should be stored in sector 1 of the eMMC device.

H'0000 must be set for the "boot option" in the VRL4 format. A value other than 0 must be set for the copy size.

Description on operations:

1. Read data from sector 1 (512 bytes) of the eMMC device and perform the VRL4 format check.
2. If no errors were found by the format check, the program for the copy size in the VRL4 format and the secure data (288 bytes) are read from the eMMC device and copied to the fixed MERAM address. (The maximum size of the program to be copied is 64 Kbytes (VRL4 format is also included).)
3. When the secure function is used, a secure library is called and a secure check is applied to the specified area.
4. If no error has occurred performing steps 1 to 3, execution jumps to the start address of the program copied to MERAM.

   (If an error has occurred performing steps 1 to 3, the eMMC boot function is aborted and a transition is made to the USB download function.)

B.3.6 eMMC Boot Function (MFI Pins/BSC Pins, Boot Partition)

The eMMC boot function (2A/2B) is used to initiate a program written to an eMMC device in eMMC boot mode or eMMC development boot mode. The MMC port pins are multiplexed and the MD pins are used to select from among the MFI pins and BSC pins. Boot operation mode is used as the boot mode.

The program to be written to the eMMC device should be in a format conforming to the VRL4 format and it should be stored in sector 0 of boot partition 1 or 2, which has been enabled in advance in the eMMC device.

H'0000 must be set for the "boot option" in the VRL4 format. A value other than 0 must be set for the copy size.

Description on operations:

1. In boot operation mode, 128 Kbytes of data is read from the boot partition that has been enabled in the eMMC device, and copied to MERAM. The copy size is 128 Kbytes regardless of the copy size in the VRL4 format.
2. Perform the VRL4 format check for the data read out from sector 0.
3. When the secure function is used, a secure library is called and a secure check is applied to the specified area.
4. If no error has occurred performing steps 1 to 3, execution jumps to the start address of the program copied to MERAM.
   (If an error has occurred performing steps 1 to 3, the eMMC boot function is aborted and a transition is made to the USB download function.)

B.3.7 USB Download Function

The USB download function is used to transfer a program from the PC to RAM via the USB and execute it in case the VRL4 in an external device does not satisfy the conditions of the predefined value (value indicating that writing has been performed (VRL4 format)) in BSC boot mode, BSC development boot mode, NAND(4) boot mode, NAND(5) boot mode, NAND(4) development boot mode, NAND(5) development boot mode, eSD boot mode, eSD development boot mode, eMMC boot mode (1A, 1B, 2A, 2B), and eMMC development boot mode (1A, 1B, 2A, 2B), or does not satisfy the conditions of the NAND physical format in NAND(4) boot mode, NAND(5) boot mode, NAND(4) development boot mode, and NAND(5) development boot mode.

Mask ROM downloads a program from the PC to a specified RAM area and calls the beginning of the subroutine program defined in the VRL4. Note that the download destination address before the first subroutine call operation takes place is limited to the MERAM area.

Note: When the secure function is selected, a subroutine call is made after the secure check was performed according to the VRL4.
When the secure function is not selected, a subroutine call is made according to the VRL4.
Even in forcible USB boot mode, a transition is made to this function.
A transition to this function can also be made by using the boot control interface function.

Description on operations:

1. Mask ROM reads the signature of the start address of the external device.
   If the signature value does not match the predefined value (value indicating that writing has been performed (VRL4 format)), a transition is made to the USB download function, the USB is enabled, and USB connection is waited for.
   In NAND(4) boot mode, NAND(5) boot mode, NAND(4) development boot mode, and NAND(5) development boot mode, if the specifications of the NAND physical format (appendix B.6.2, NAND Physical Format) are not satisfied, a transition is made to this function, the USB is enabled, and USB connection is waited for.
2. After the PC and USB are connected, a program can be transferred from the PC. After transfer has finished, the transfer destination start address is called. A subroutine call is made when executing the transfer program. The USB is not disconnected here.

B.3.8 Secure Boot Function

The secure boot function is used to perform the secure check of the boot program before it is initiated in BSC boot mode, NAND(4) boot mode, NAND(5) boot mode, forcible USB boot mode, eSD boot mode, eMMC boot mode (1A, 1B, 2A, 2B), MFI1 boot mode, and MFI2 boot mode.

B.3.9 MFI Boot Function

The MFI boot function is used to expand a program and boot it in MFI1 boot mode, MFI1 development boot mode, MFI2 boot mode, or MFI2 development boot mode via the ACMFI1 (ADDEMUX) or ACMFI2 (ADMUX).

B.4 Address Map

Figure B.1 shows the address map.

After a reset is canceled, program execution starts from address H'0000 0000.

Mask ROM addresses: H'0000 0000 to H'0000 FFFF
(located at physical addresses H'E6B0 0000 to H'E6B0 FFFF)

External device addresses: From H'2000 0000 (CS0)

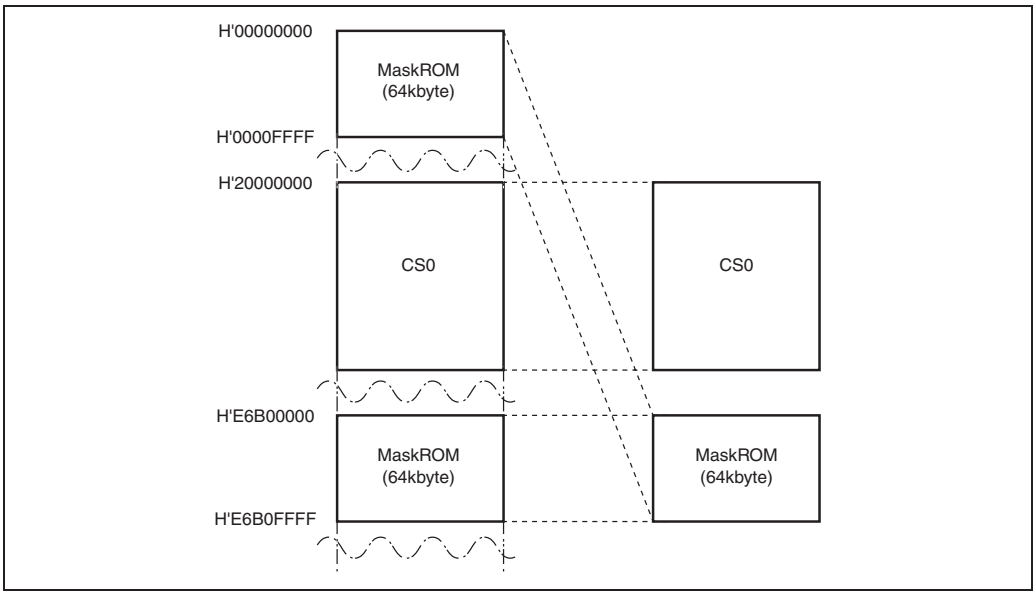


Figure B.1 Address Map at Boot

B.4.1 Addresses for Expansion by USB Download Function

A program transferred by the USB download function is expanded from the following addresses in MERAM.

H'E55B 0000 to H'E55F FFFF

B.4.2 Addresses Used for Work RAM

When mask ROM is executed, the following resources are used.

Table B.5 Addresses Used for Work RAM

Name	Address	Usage	Remarks
MFRAM	H'E6B92000 to H'E6B97FFF	MFI parameter area	
MERAM	H'E558 0000 to H'E55A FFFF	Stack, work RAM	
	H'E55B 0000 to H'E55F FFFF	Area for USB download	
		Area for copy option expansion	

B.5 General Flowcharts

B.5.1 Mask ROM Mode Determination Sequence Flow

The sequence for determining the boot mode at AP4 power-on is shown in figure B.2.

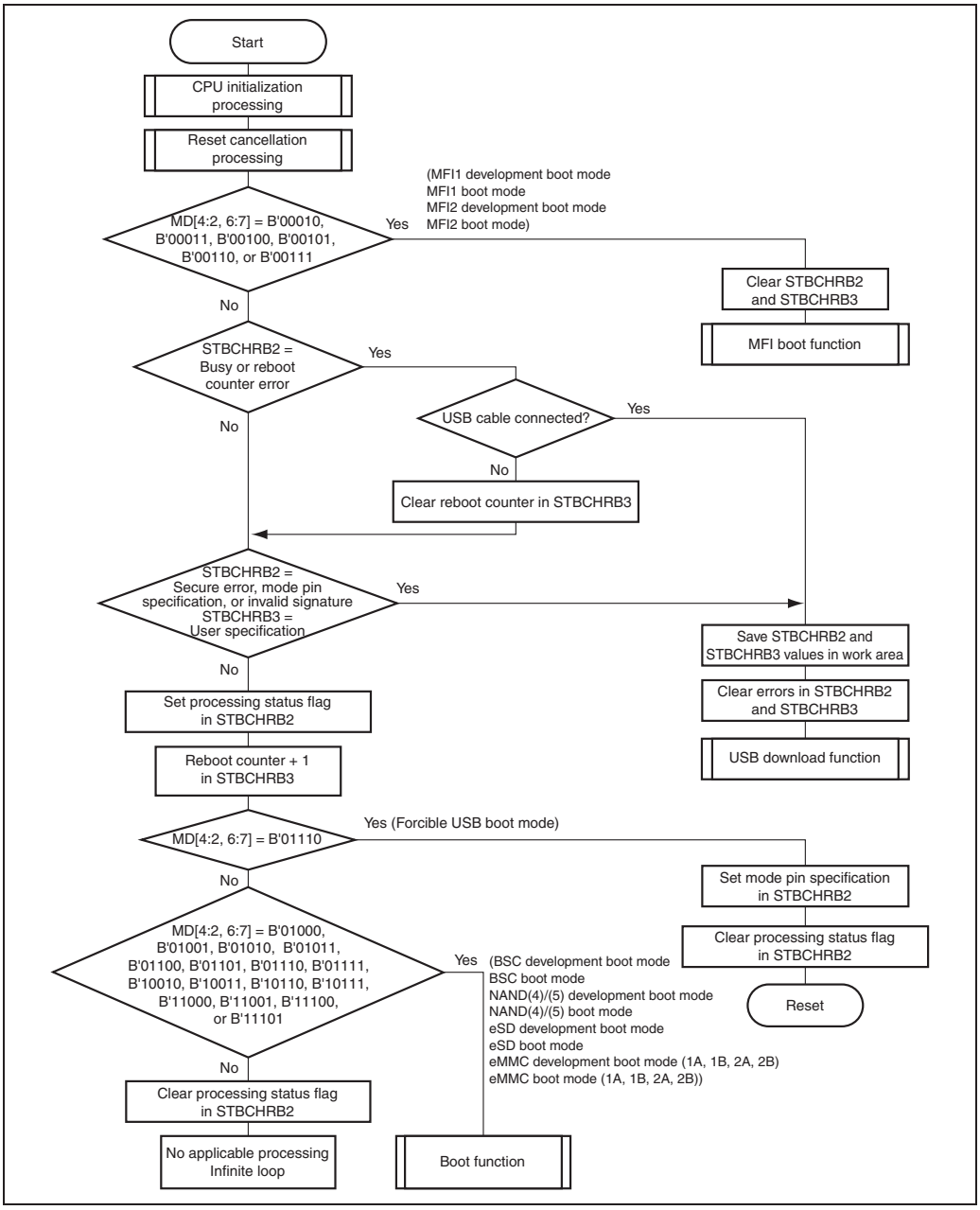


Figure B.2 AP4 Boot Mode Determination Sequence

B.5.2 Boot Processing Flow for Each Boot Function

(a) Boot Function Processing

The processing at boot is shown in figure B.3.

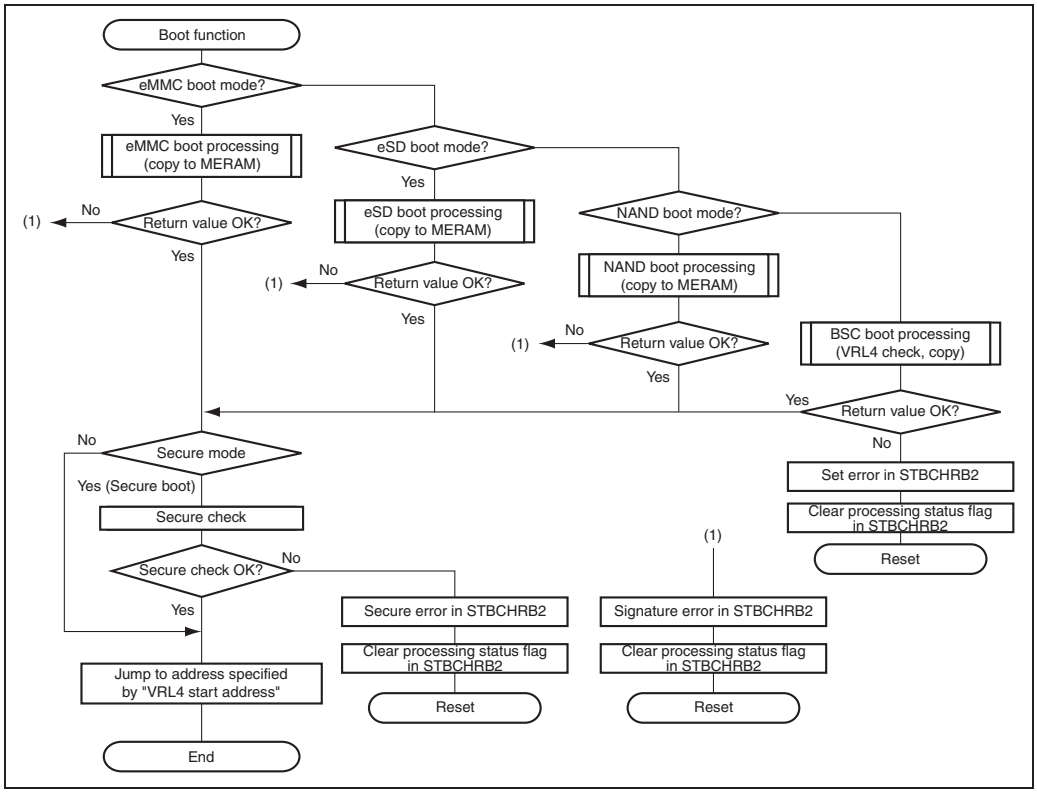


Figure B.3 Normal Mode Flow

(b) BSC Boot Processing

The BSC boot processing is shown in figure B.4.

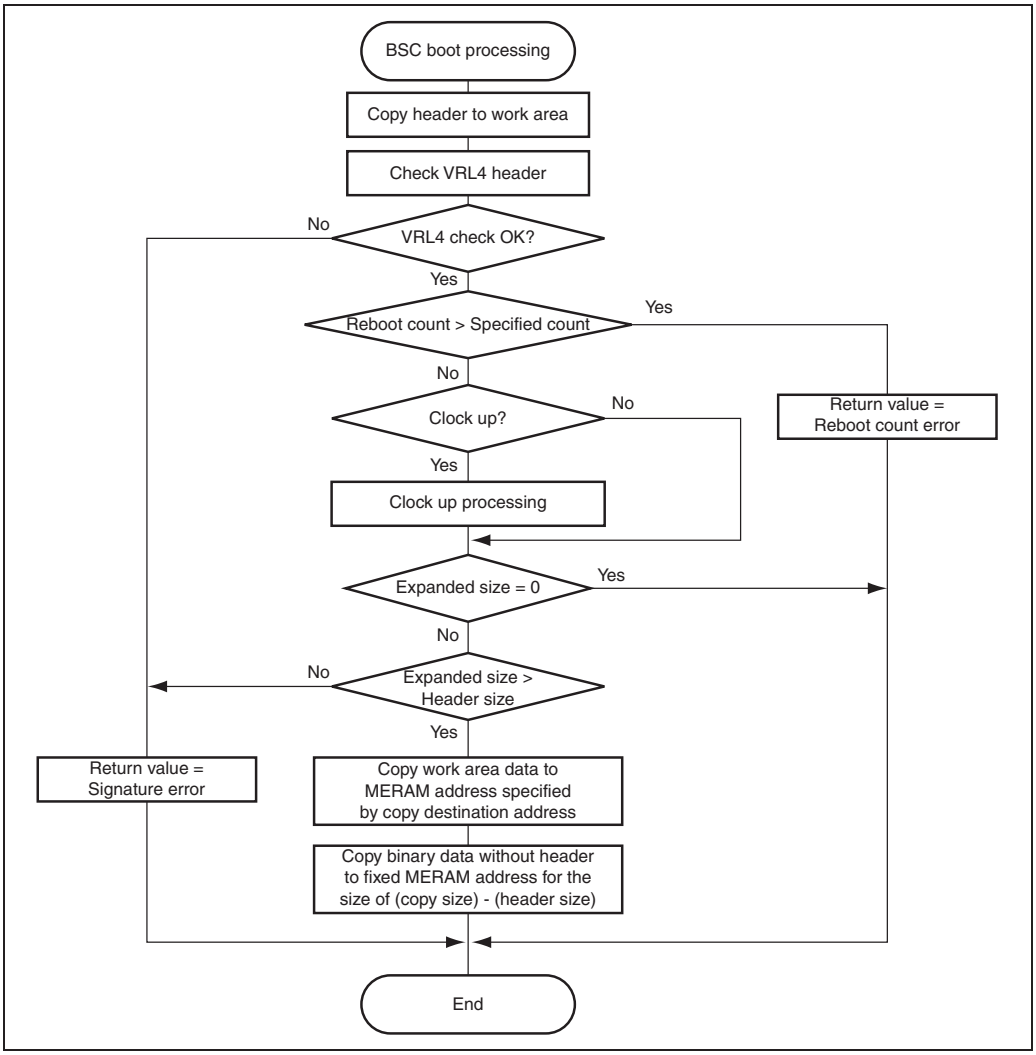


Figure B.4 BSC Boot Processing Flow

(c) NAND Boot Processing

The NAND boot processing is shown in figure B.5.

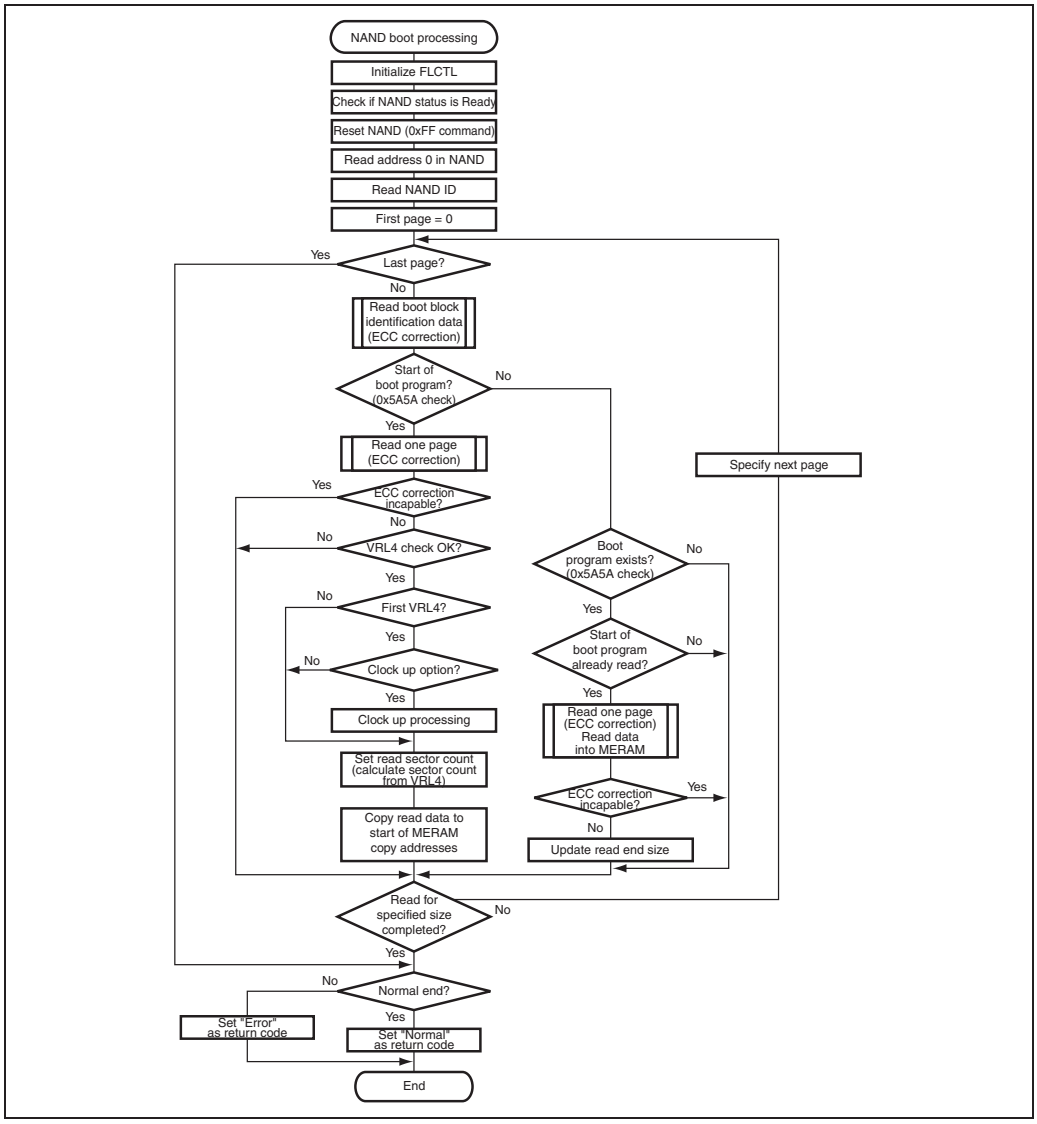


Figure B.5 NAND Boot Processing Flow

(d) ECC Correction Processing

The ECC correction processing at NAND read is shown in figure B.6.

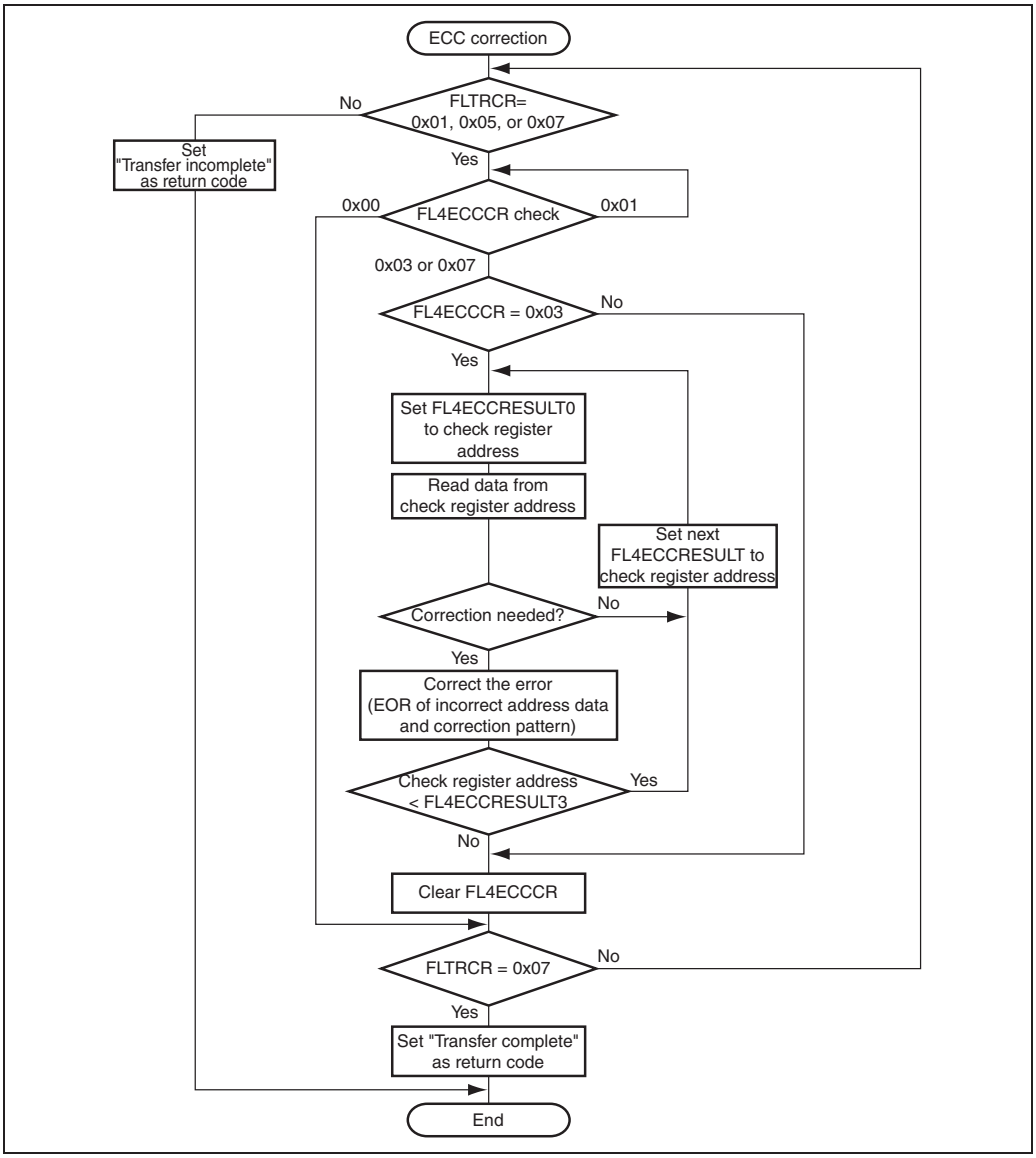


Figure B.6 ECC Correction Processing Flow

(e) eSD Boot Processing

The eSD boot processing is shown in figure B.7.

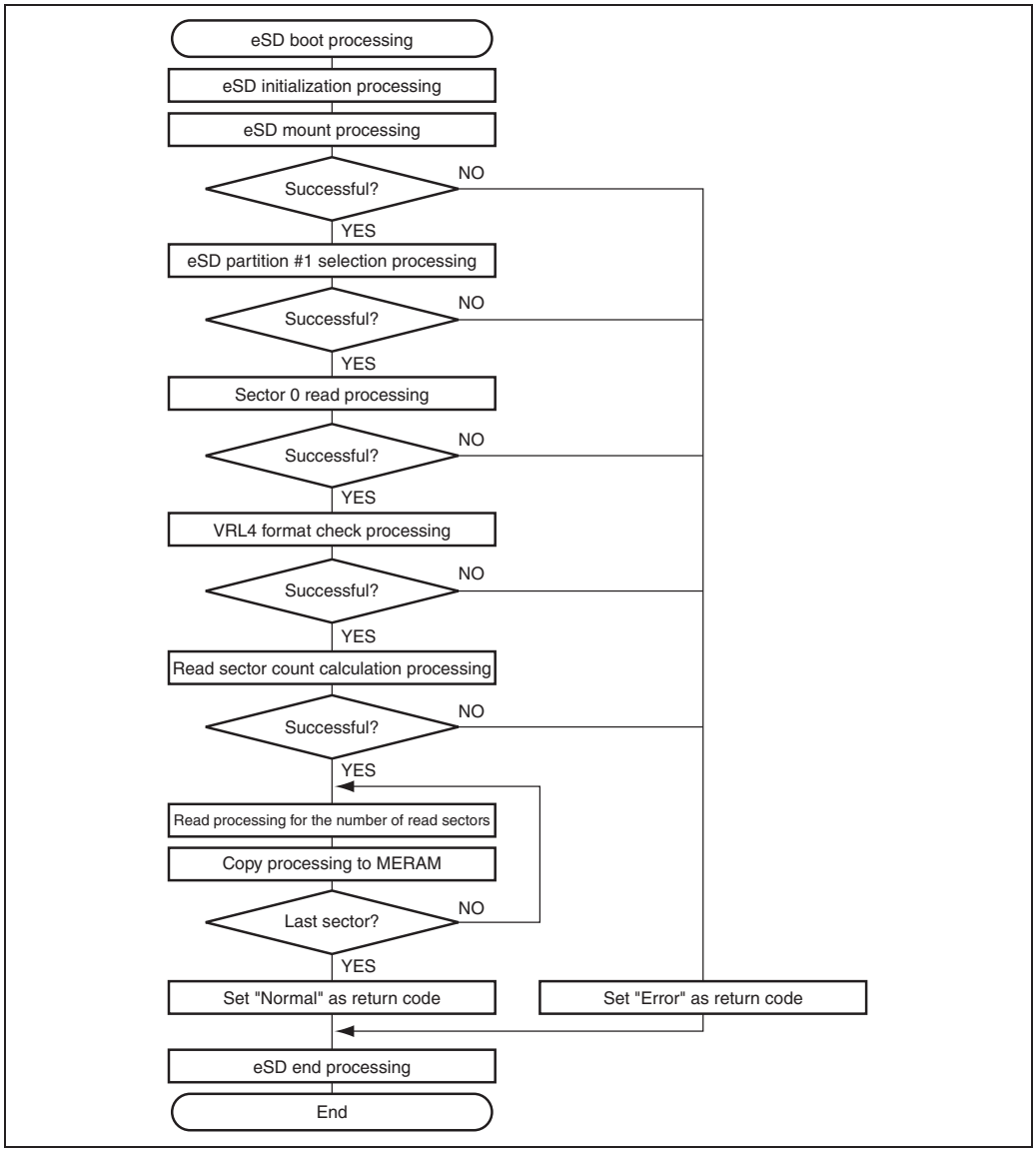


Figure B.7 eSD Boot Processing Flow

(f) eMMC Boot 1A, eMMC Boot 1B Processing

The eMMC boot 1A/1B processing is shown in figure B.8.

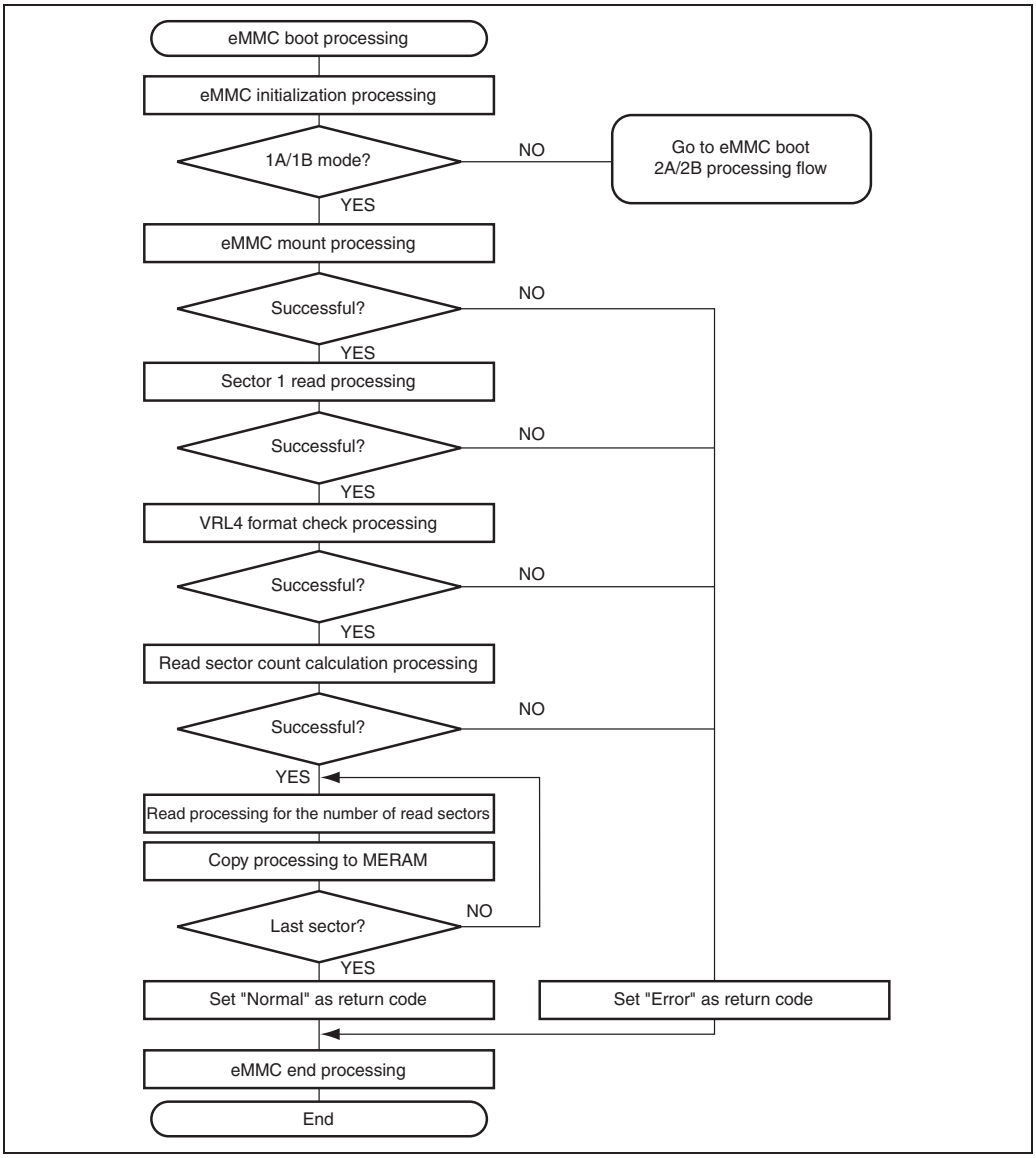


Figure B.8 eMMC Boot 1A, eMMC Boot 1B Processing Flow

(g) eMMC Boot 2A, eMMC Boot 2B Processing

The eMMC boot 2A/2B processing is shown in figure B.9.

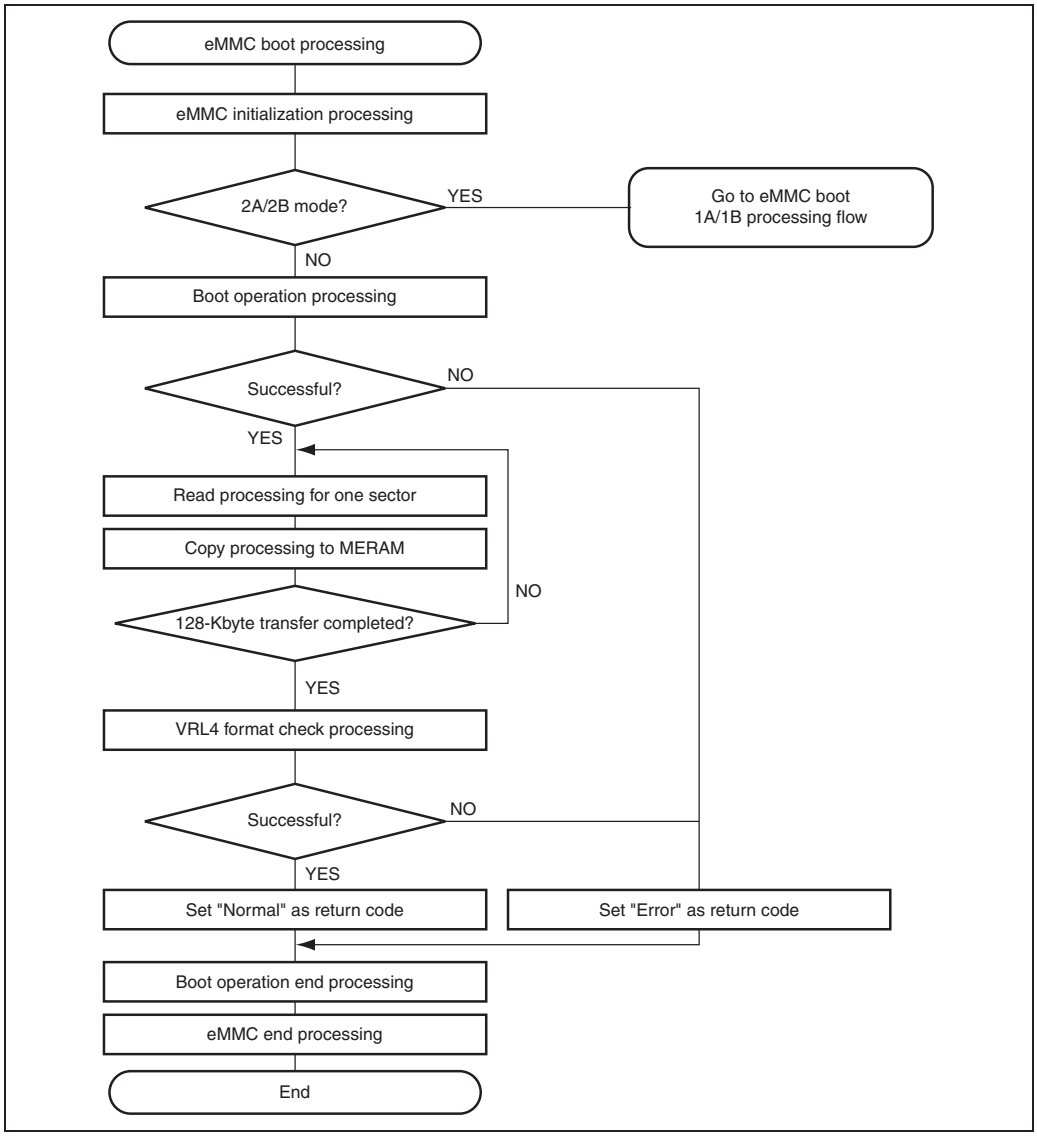


Figure B.9 eMMC Boot 2A, eMMC Boot 2B Processing Flow

(h) MFI1 Boot Processing

The MFI1 boot processing is shown in figure B.10.

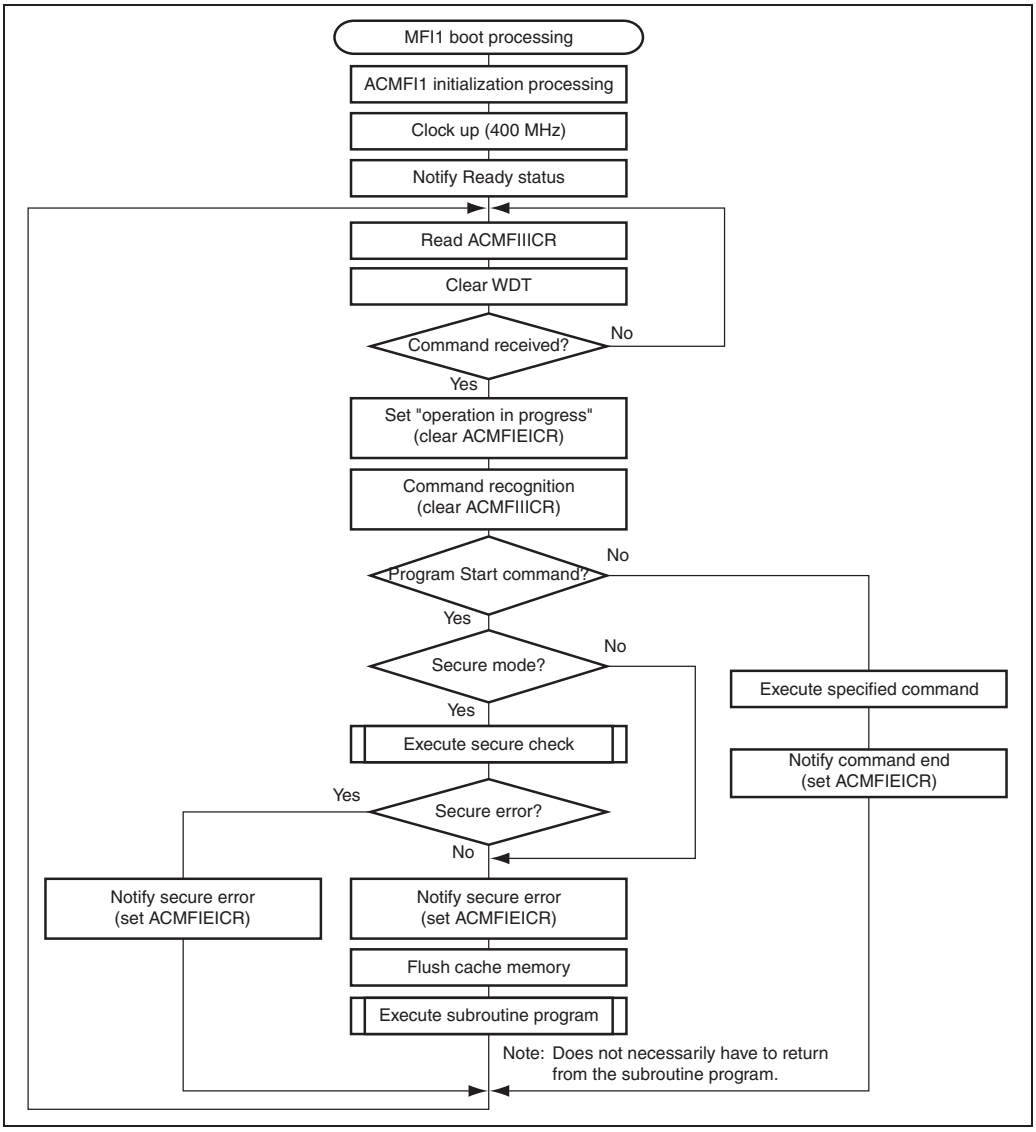


Figure B.10 MFI1 Boot Processing Flow

(i) MFI2 Boot Processing

The MFI2 boot processing is shown in figure B.11.

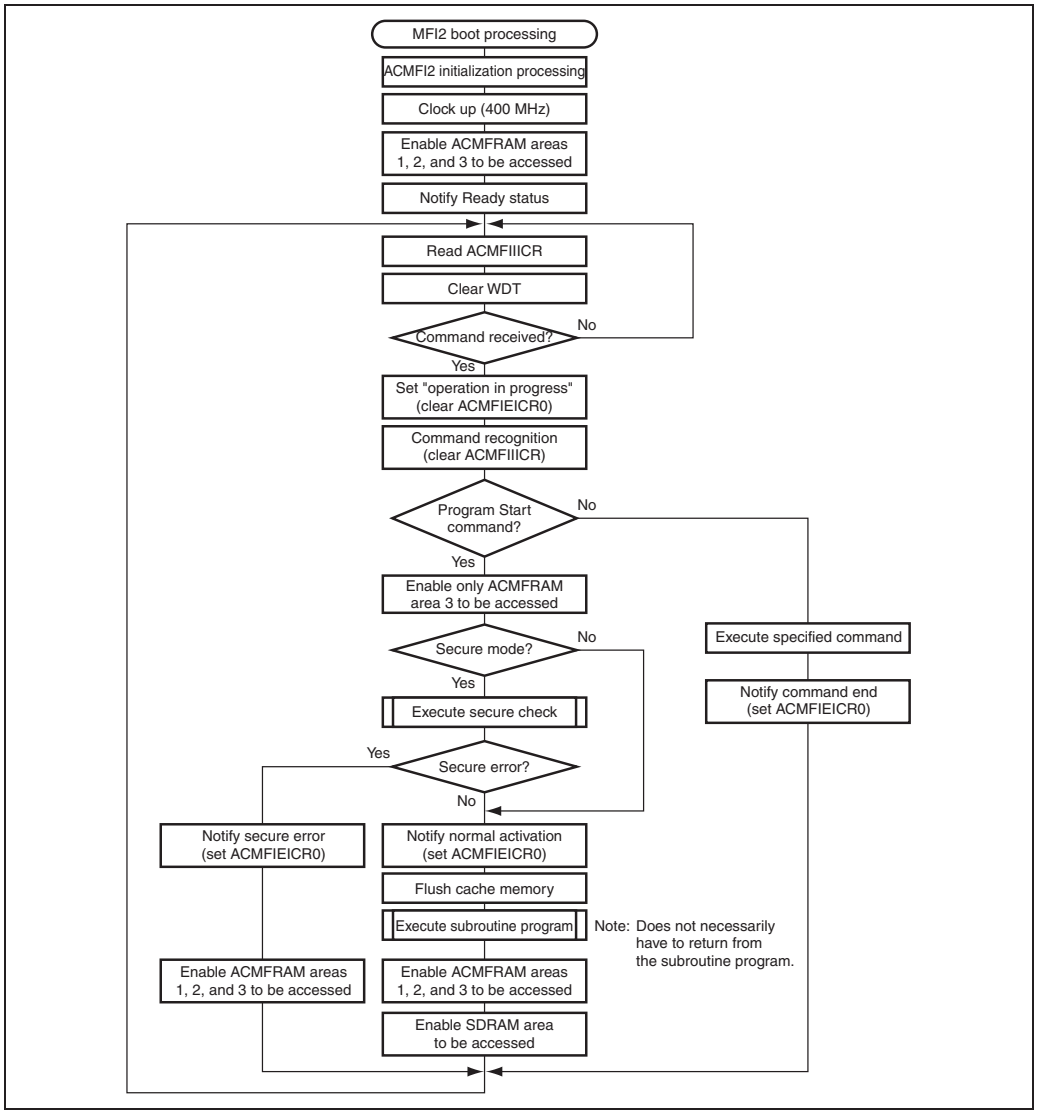


Figure B.11 MFI2 Boot Processing Flow

B.5.3 USB Download Flow

A flowchart for the USB download function is shown in figure B.12.

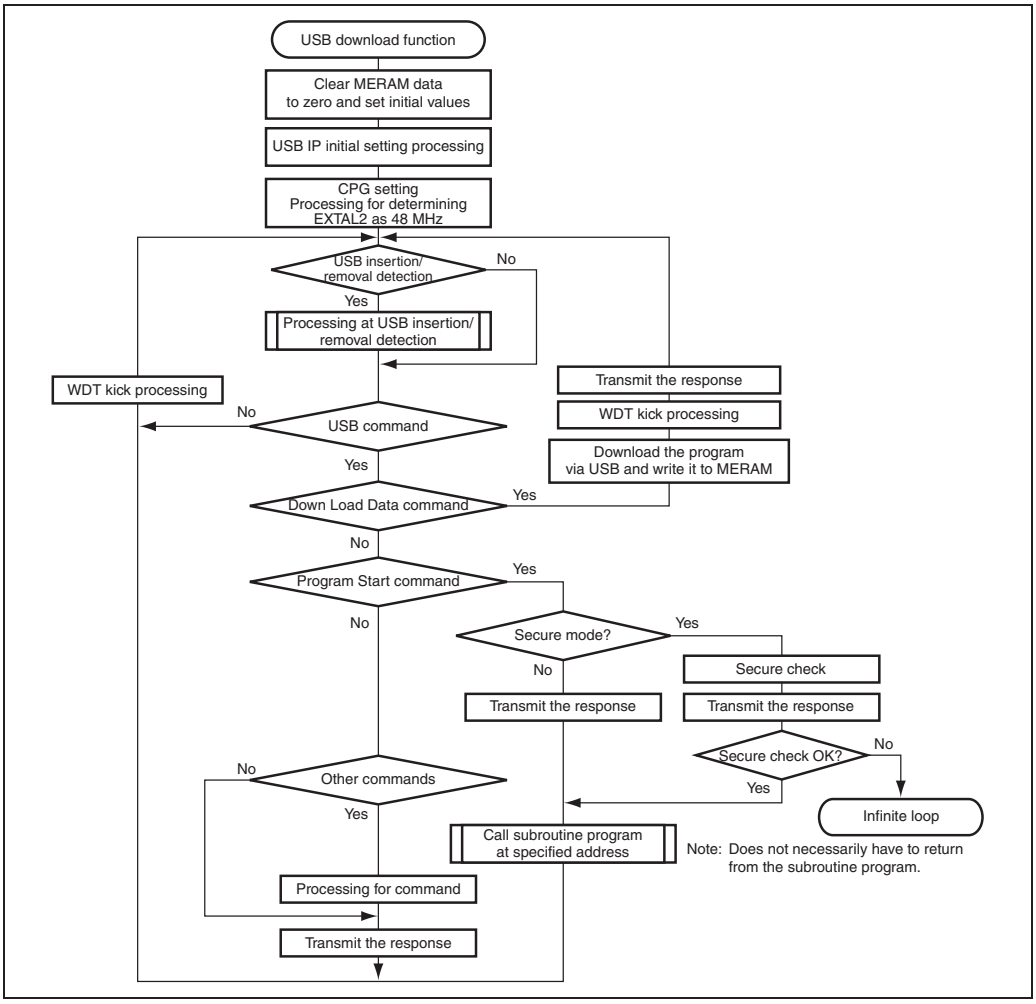


Figure B.12 USB Download Boot Processing Flow

In the USB download function, mask ROM controls the USB device and performs transmit and receive processes. After the Program Start command has been received, the result is sent as the response. If the result is normal, execution jumps to the beginning of the received data.

The USB disconnection processing does not take place here.

B.5.4 USB Insertion/Removal Detection Flow

A flowchart for the USB insertion/removal detection during USB download is shown in figure B.13.

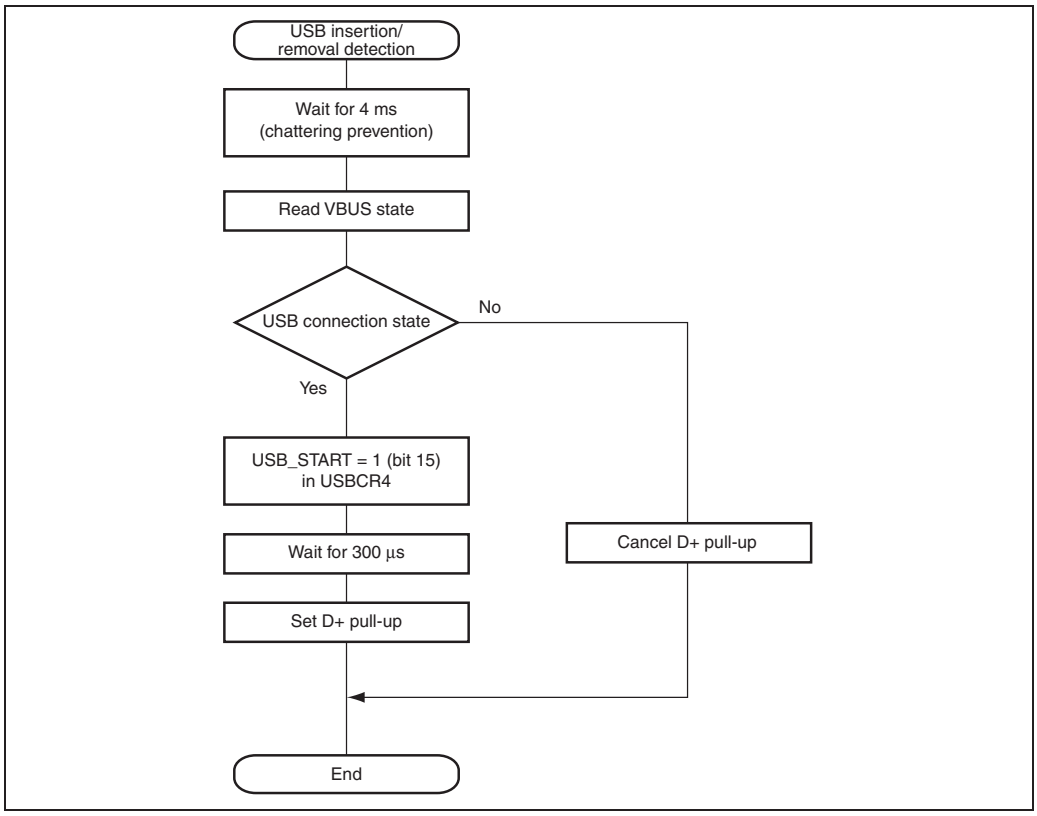


Figure B.13 USB Insertion/Removal Detection Flow

In VBUS detection during USB download, after connection has been detected, the power supply break control register (USBCR4) is controlled. Set the USB_START bit in USBCR4 to 1, wait for 300 μs, and then pull up D+ (default value of USB_COR is used without change).

When disconnection has been detected, pull-up of D+ is canceled.

B.5.5 Secure Check Flow

A flowchart for the secure check is shown in figure B.14.

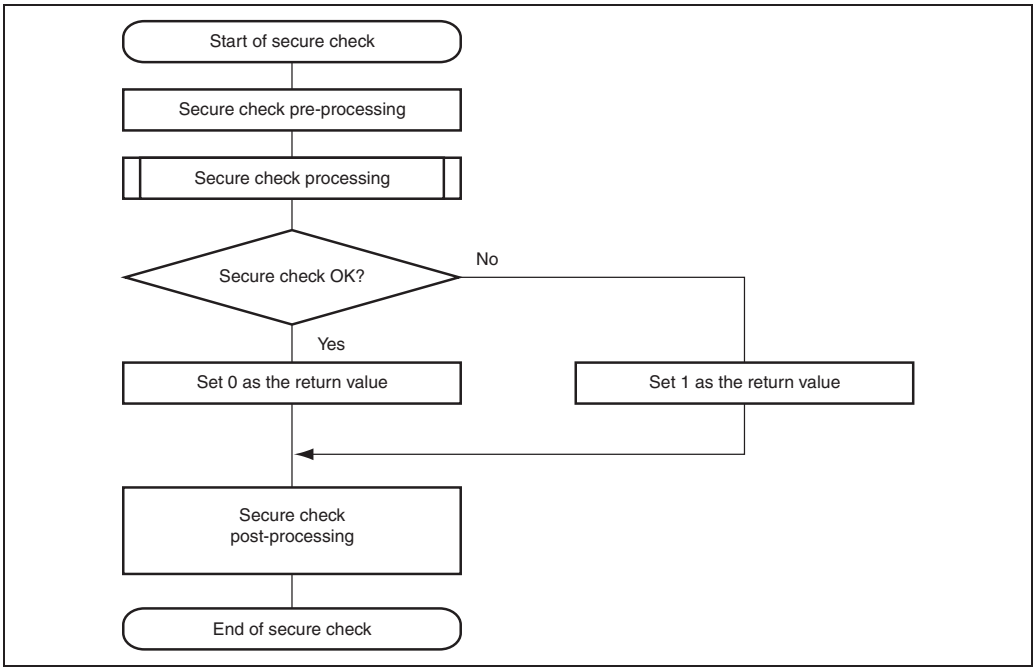


Figure B.14 Secure Check Flow

B.5.6 CPU Initialization Processing

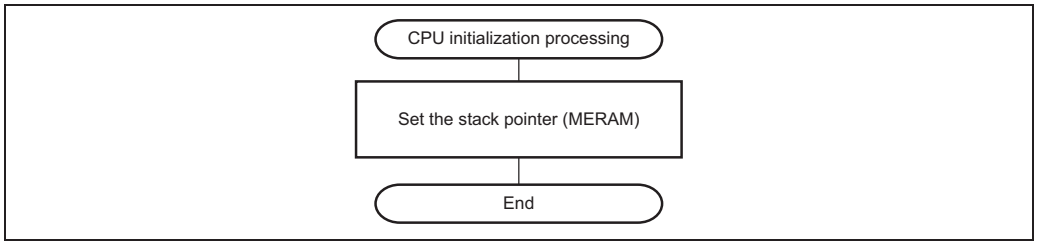


Figure B.15 CPU Initialization Processing Flow

B.6 Formats

B.6.1 Flash ROM Format (VRL4 Format)

This format is a header for a boot block used in all boot modes.

A program is expanded in on-chip ROM according to each boot mode and started according to the flash ROM format (VRL4 format) (a program is started directly without being expanded when the copy boot option for BSC boot mode or BSC development boot has not been specified).

The flash ROM format includes the VRL4 specifications that are used by the secure boot function.

Table B.6 Flash ROM Formats

Offset	Size	Name	Value Evaluation	Remarks
+ H'00	4	Magic number 1	Performed	H'EA000000 must be specified.
+ H'04	4	Reserved	Performed	A value between H'56 and H'2C40 must be specified.
+ H'08	4	Magic number 2	Not performed	H'E59FF008 must be specified.
+ H'0C	4	Reserved	Not performed	
+ H'10	2	Copy size	Performed	The size of the copy option is specified. Copy boot is not performed for H'0000.
+ H'12	2	Boot options	Performed	Clock up specification of 2 bits (bits 14 and 15). Reboot count specification of 3 bits (bits 11, 12, and 13). Other bits are reserved (bits 10 to 0).
+ H'14	4	Reserved	Performed	A value between H'0001 and H'03FF must be specified.
+ H'18	4	Start address	Not performed	Program start address is specified.
+ H'1C	4	Reserved	Not performed	
+ H'20	4	Reserved	Not performed	
+ H'24	308	Reserved	Not performed	

- Magic number: The specified bit pattern is stored.
- Copy size: Size (bytes) of the expanded program.

  Used in BSC boot, BSC development boot, NAND(4) boot, NAND(5) boot, NAND(4) development boot, NAND(5) development boot, eSD boot, eSD development boot, eMMC boot (1A, 1B, 2A, 2B), and eMMC development boot (1A, 1B, 2A, 2B) modes.

  A value between H'0 and H'FFFF must be specified.
- Boot options: The options for boot operation by each function are specified.

  Used in BSC boot, BSC development boot, NAND(4) boot, NAND(5) boot, NAND(4) development boot, and NAND(5) development boot modes.

  — Clock up specification (Used in BSC boot, BSC development boot, NAND(4) boot, NAND(5) boot, NAND(4) development boot, and NAND(5) development boot modes.)

  — Reboot count specification (Used in BSC boot and BSC development boot modes.)
- Start address: Address at which to start execution after copy.

  The specified address is called after the copy processing.

  Since the header will also be copied, specify the address carefully.

  The start address should be aligned to a 4-byte boundary.
- Reserved: Reserved area.

  Only the items for which value evaluation is to be performed are evaluated at boot.

Note: All data is stored in the little endian format.

The VRL4 format in secure mode is specified separately.

The area to transfer the copy size is not specified because it is fixed to MERAM.

Specify 0 for areas not used by the boot options.

B.6.1.1 Clock Up Option

(a) For BSC boot function

Clock up specification (bits 14 and 15):

B'00: Clock setting A (SYS-CPU 800 MHz (see "Clock up SYS-CPU 800 MHz" in appendix B.7, Settings))

B'10: Clock setting B (SYS-CPU 400 MHz (see "Clock up SYS-CPU 400 MHz" in appendix B.7, Settings))

B'01: Reserved (same as clock setting D)

B'11: Clock setting D (Do not make this setting.)

(b) For NAND boot function

For the clock up option when using the NAND boot function, refer to appendix B.6.2, NAND Physical Format.

B.6.1.2 Copy Size

(a) For BSC boot function

When zero bytes are specified as the copy size, expansion is not performed.

When a value other than zero bytes is specified, data for the copy size is copied from offset 0.

If the specified size is not a multiple of 4, copy is performed with the size rounded up to a multiple of 4. Details of the operation are shown in figure B.16.

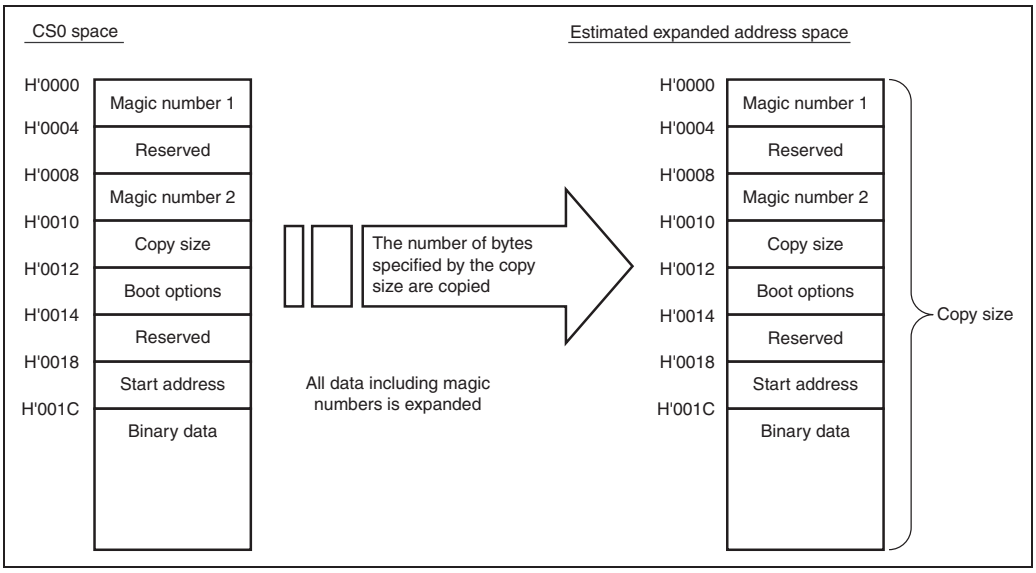


Figure B.16 Expansion Processing for Boot Function

The expansion size of mask ROM includes the VRL4 size.

(b) For NAND boot function

For the copy size when using the NAND boot function, refer to appendix B.6.2, NAND Physical Format.

(c) For eSD boot function

For the copy size when using the eSD boot function, refer to appendix B.6.3, eSD Physical Format.

B.6.1.3 Reboot Count Specification

(a) For BSC boot function

Reboot count specification (reboot count for transition to USB download)

0: This function is disabled

1 to 7: Reboot count to trigger a transition to USB download

B.6.2 NAND Physical Format

In NAND(4) boot mode, NAND(5) boot mode, NAND(4) development boot mode, and NAND(5) development boot mode, the boot program including the VRL4 is stored in the format described in this section.

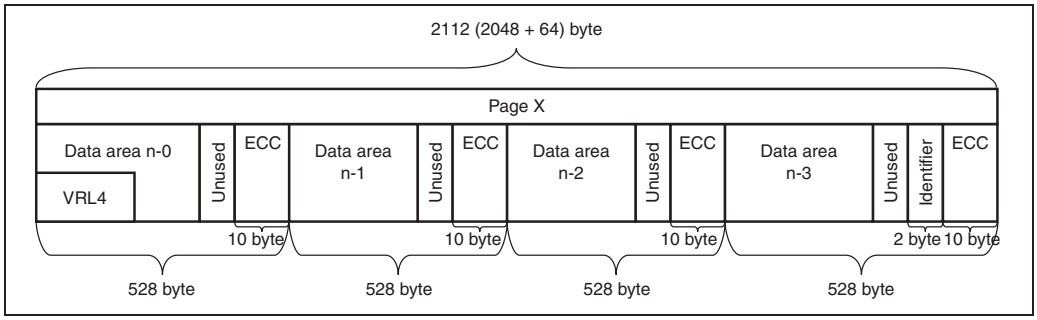


Figure B.17 NAND Page Format

Table B.7 NAND Page Format

Item		Offset	Size	Description
Data area n-0	VRL4	From H'000	—	Locate VRL4 at the start of the area (n = 0 only). (Should conform to VRL4 specifications)
		H'010, H'011	2	VRL4 copy size area Specify the boot program size including VRL4. The size will be rounded up to 2048-byte units.
		H'012, H'013	—	VRL4 boot option Only the clock up specification can be set.
		H'014 to m		VRL4 (continued from above) m is 344 in the VRL4 specifications, but an offset of H'20 or higher will not be inspected.
		H'000 to H'1FF	512	Boot program
Unused area n-0		H'200 to H'205	6	Unused
ECC n-0		H'206 to H'20F	10	ECC of offsets H'0 to H'205
Data area n-1		H'210 to H'40F	512	Boot program
Unused area n-1		H'410 to H'415	6	Unused
ECC n-1		H'416 to H'41F	10	ECC of offsets H'210 to H'415
Data area n-2		H'420 to H'61F	512	Boot program
Unused area n-2		H'620 to H'625	6	Unused
ECC n-2		H'626 to H'62F	10	ECC of offsets H'420 to H'625
Data area n-3		H'630 to H'82F	512	Boot program
Control code area n-3		H'830 to H'833	4	Unused
Identifier for page n		H'834 to H'835	2	Store the boot block identification data Identification data: H'5A5A: First page H'A5A5: Second and subsequent pages Other than above: Invalid page
ECC n-3		H'836 to H'83F	10	ECC of offsets H'630 to H'835

The data areas are expanded in MERAM as shown in figure B.18.

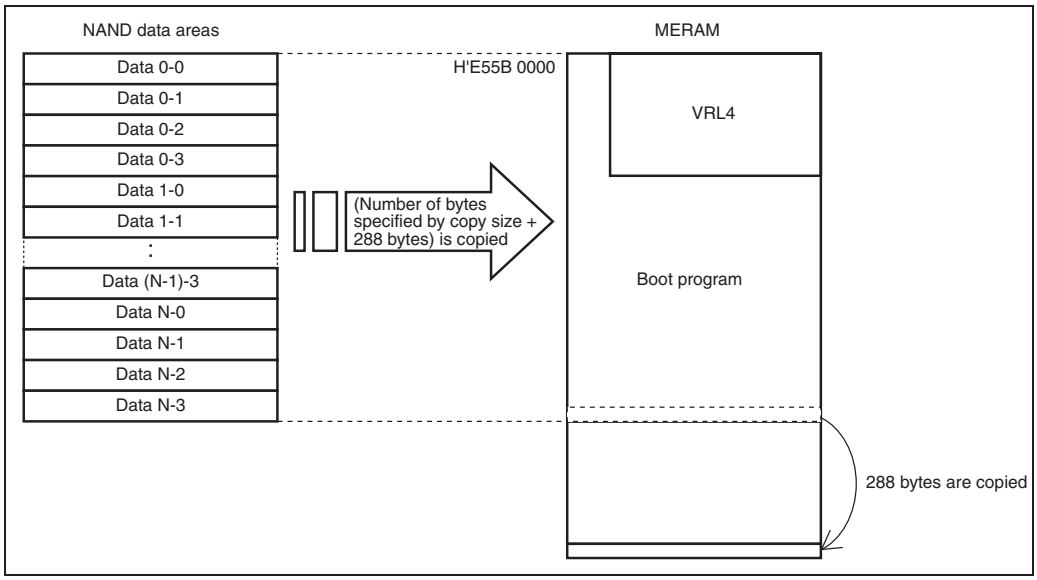


Figure B.18 NAND Data Area Expansion in MERAM

The boot option definitions in the VRL4 format used in these modes are shown below.

- Clock up specification (bits 14 and 15)
  - B'00: Clock setting A (SYS-CPU 800 MHz (see "Clock up SYS-CPU 800 MHz" in appendix B.7, Settings))
  - B'10: Clock setting B (SYS-CPU 400 MHz (see "Clock up SYS-CPU 400 MHz" in appendix B.7, Settings))
  - B'01: Reserved
  - B'11: Clock setting D (Do not make this setting.)
- Copy size specification (specification of the size to be copied)

  Data for the copy size is copied from offset 0.

  If the specified size is not a multiple of 4, copy is performed with the size rounded up to a multiple of 4.

Page X that includes data areas 0 to N is searched as shown in figure B.19.

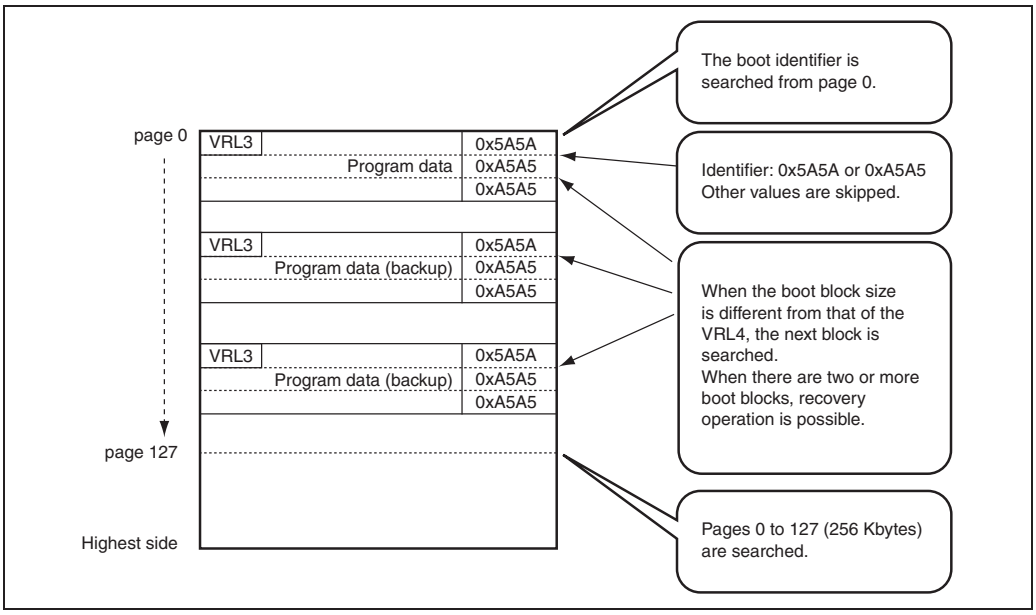


Figure B.19 NAND Block Search

B.6.3 eSD Physical Format

In eSD boot mode and eSD development boot mode, the boot program including the VRL4 format is stored in physical partition #1 of the eSD device in the format shown in figure B.20.

In addition, the boot program of the eSD device is expanded in MERAM, as shown in figure B.20.

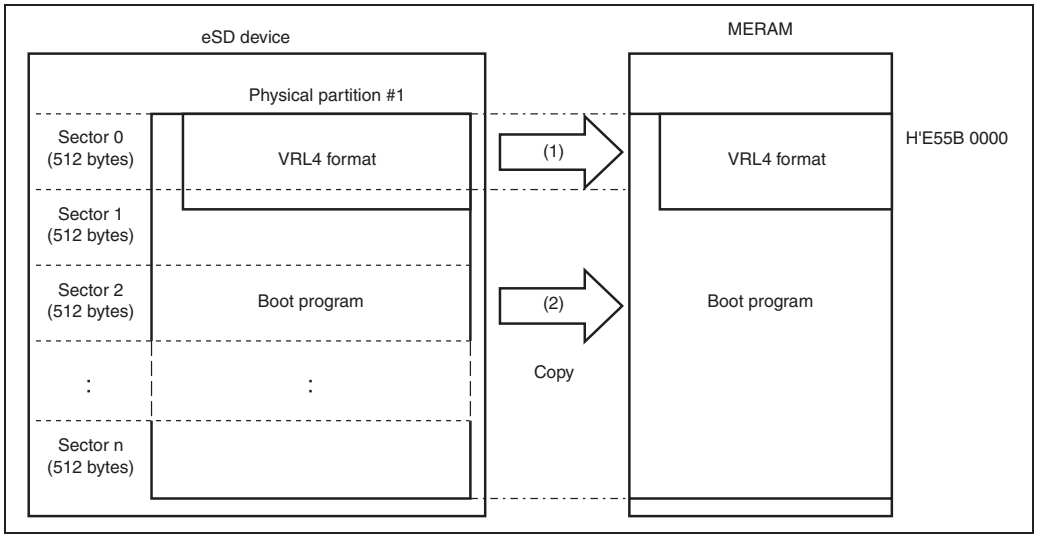


Figure B.20 eSD Physical Format and MERAM Expansion by eSD Boot Function

First, set physical partition #1 in the eSD device.

Next, read data from sector 0 at operation (1), determine the copy size (number of sectors to be copied), and expand the boot program in MERAM for the remaining copy size (number of sectors to be copied) at operation (2).

The boot option definitions in the VRL4 format used by the eSD boot function are shown below.

- Clock up specification (bits 14 and 15)
  Disabled
  Note: In eSD boot modes, the clock setting is the same for all. Operation is performed with SYSCPU as 400 MHz and SDHI as 100 MHz.
  The clock setting for the eSD card is 390 KHz when initializing the eSD card and 25 MHz when reading data from the eSD device.

- Reboot count specification (reboot count for transition to USB download)
  Disabled
- Copy destination specification (expansion address when the copy option is specified)
  Disabled
- Copy size specification (specification of the size to be copied)
  Size of the data to be copied.

  Note: When zero bytes are specified, a transition is made to the USB download function. When a value other than zero bytes is specified, the boot program is copied for the size specified to be copied from sector 0.

  When this size is rounded up to a multiple of 4, the size to be copied is obtained by adding 288 to that value. (In reality, copy is performed in sectors. Therefore, even if the calculated value is not a multiple of 512, data will be copied from the eSD device for a multiple of 512.)

B.6.4 eMMC 1A/1B Physical Format

In eMMC boot mode 1A, eMMC boot mode 1B, eMMC development boot mode 1A, and eMMC development boot mode 1B, the boot program (user program) including the VRL4 format is stored in sector 1 of the eMMC device in the format shown in figure B.21.

In addition, the boot program of the eMMC device is expanded in MERAM, as shown in figure B.21.

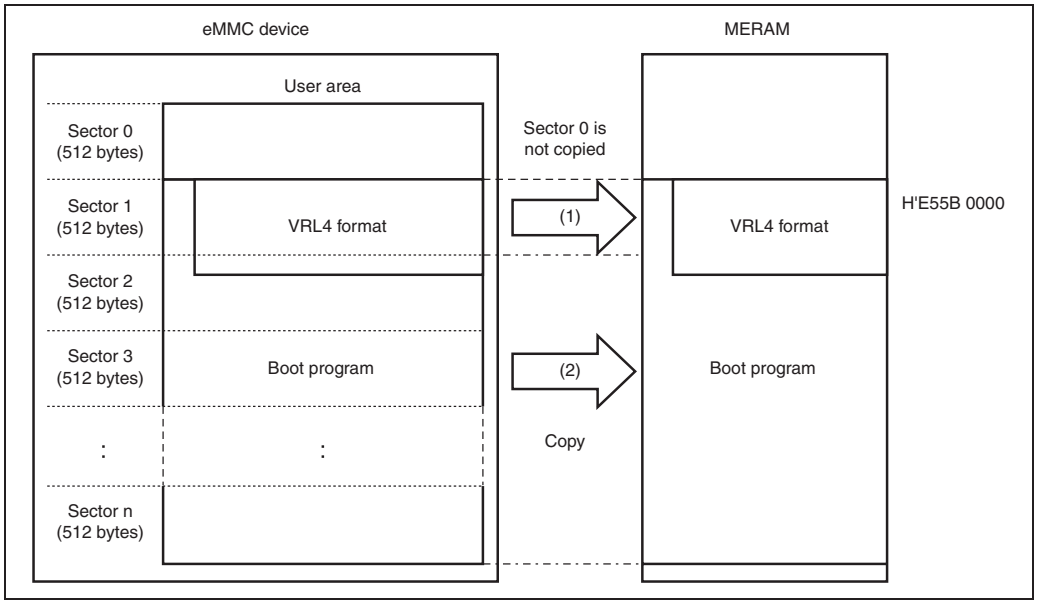


Figure B.21 eMMC 1A/1B Physical Format and MERAM Expansion by eMMC Boot Function

Read data from sector 1 at operation (1), determine the copy size (number of sectors to be copied), and expand the boot program in MERAM for the remaining copy size (number of sectors to be copied) at operation (2).

The boot option definitions in the VRL4 format used by the eMMC boot function are shown below. H'0000 must be set for the boot options (2 bytes).

- Clock up specification (bits 14 and 15)
  Disabled (B'00 must be set)
  Note: In eMMC boot modes, the clock setting is the same for all. Operation is performed with SYSCPU as 400 MHz and MMC as 100 MHz.
  The clock setting for the eMMC card is 390 KHz when initializing the eMMC card and 50 MHz or 25 MHz when reading data from the eMMC device in accordance with the eMMC device.
- Reboot count specification (reboot count for transition to USB download)
  Disabled (B'000 must be set)
- Copy destination specification (expansion address when the copy option is specified)
  Disabled (B'0 must be set)
- Copy size specification (specification of the size to be copied)
  Size of the data to be copied.
  Note: When zero bytes are specified, a transition is made to the USB download function. When a value other than zero bytes is specified, the boot program is copied for the size specified to be copied.
  When this size is rounded up to a multiple of 4, the size to be copied is obtained by adding 288 to that value. (In reality, copy is performed in sectors. Therefore, even if the calculated value is not a multiple of 512, data will be copied from the eMMC device for a multiple of 512.)

B.6.5 eMMC 2A/2B Physical Format

In eMMC boot mode 2A, eMMC boot mode 2B, eMMC development boot mode 2A, and eMMC development boot mode 2B, the boot program (user program) including the VRL4 format is stored at the beginning of the boot area partition of the eMMC device in the format shown in figure B.22.

In addition, the boot program of the eMMC device is expanded in MERAM, as shown in figure B.22.

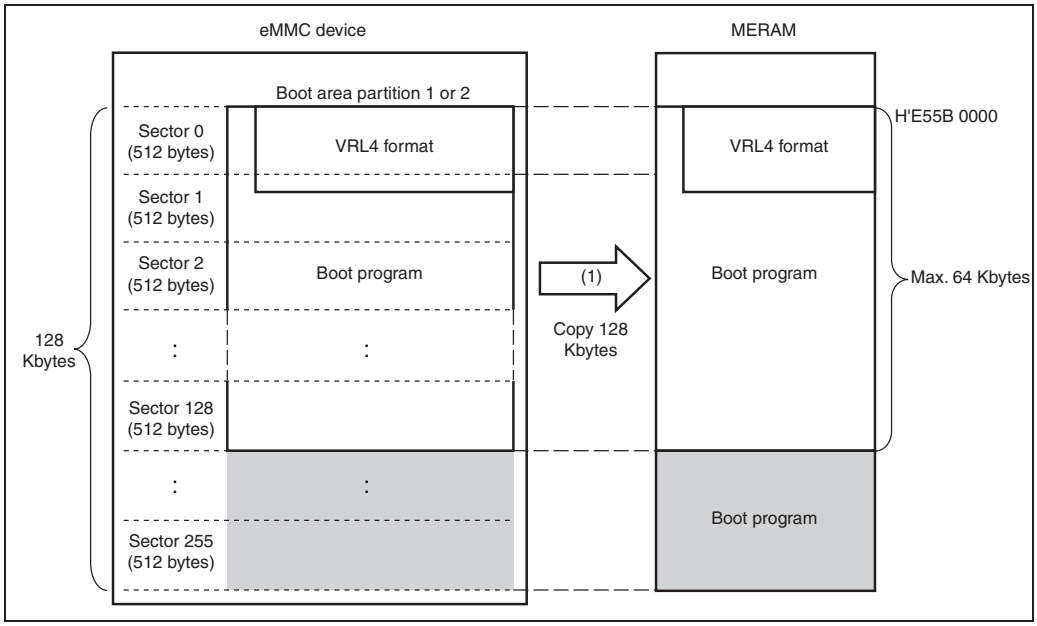


Figure B.22 eMMC 2A/2B Physical Format and MERAM Expansion by eMMC Boot Function

At operation (1), copy 128 Kbytes of data to MERAM by the boot operation. Read data from the boot partition that has been enabled by the eMMC device (boot partition 1 or 2). The copy size is 128 Kbytes regardless of the copy size specified in the VRL4 format. As the maximum boot program size is 64 Kbytes, the latter 64 Kbytes contain invalid data.

The boot option definitions in the VRL4 format used by the eMMC boot function are shown below. H'0000 must be set for the boot options (2 bytes).

- Clock up specification (bits 14 and 15)
  Disabled (B'00 must be set)
  Note: In eMMC boot modes, the clock setting is the same for all. Operation is performed with SYSCPU as 400 MHz and MMC as 100 MHz.
  The clock setting for the eMMC card is 390 KHz when initializing the eMMC card and 12.5 MHz when reading data from the eMMC device.
- Reboot count specification (reboot count for transition to USB download)
  Disabled (B'000 must be set)
- Copy destination specification (expansion address when the copy option is specified)
  Disabled (B'0 must be set)
- Copy size specification (specification of the size to be copied)
  Size of the data to be copied. Though 128 Kbytes are copied regardless of this value in these modes, set the correct value (boot program size).
  Note: When zero bytes are specified, a transition is made to the USB download function after copy has finished.

B.6.6 Message Format between Windows PC and AP4 for USB Download Function

B.6.6.1 Used Class

Communication is performed using the USB communication class.

A USB serial driver of Windows XP standard is used on the PC side. At this time, the applications on the PC side are used as COMx ports.

An inf file needs to be prepared to install the USB serial driver of Windows XP standard.

Note: In the USB download function, operation with several machines connected to the same PC is not guaranteed.
USB transfer is performed by full-speed transfer.

B.6.6.2 Descriptors

(1) Device Descriptors

Field	Value (Hexadecimal)
bLength	12
bDescriptorType	01
bcdUSB	0200
bDeviceClass	02
bDeviceSubClass	00
bDeviceProtocol	00
bMaxPakcetSize0	40
idVendor	045B
idProduct	0055
bcdDevice	0000
iManufacturer	01
iProduct	02
iSerialNumber	00
bNumConfigurations	01

(2) Configuration Descriptors

Field	Value (Hexadecimal)
bLength	09
bDescriptorType	02
wTotalLength	0043
bNumInterfaces	02
bConfigurationValue	01
iConfiguration	00
bmAttributes	C0
MaxPower	01

(j) Interface Descriptors (Communication Class)

Field	Value (Hexadecimal)
bLength	09
bDescriptorType	04
bInterfaceNumber	00
bAlternateSetting	00
bNumEndpoints	01
bInterfaceClass	02
bInterfaceSubClass	02
bInterfaceProtocol	01
iInterface	01

(k) Interface Descriptors (Data Class)

Field	Value (Hexadecimal)
bLength	09
bDescriptorType	04
bInterfaceNumber	01
bAlternateSetting	00
bNumEndpoints	02
bInterfaceClass	0A
bInterfaceSubClass	00
bInterfaceProtocol	00
iInterface	02

(l) Header Functional Descriptors

Field	Value (Hexadecimal)
bFunctionLength	05
bDescriptorType	24
bDescriptorSubtype	00
bcdCDC	0110

(m) Abstract Control Management Functional Descriptors

Field	Value (Hexadecimal)
bFunctionLength	04
bDescriptorType	24
bDescriptorSubtype	02
bmCapabilities	00

(n) Union Functional Descriptors

Field	Value (Hexadecimal)
bFunctionLength	05
bDescriptorType	24
bDescriptorSubtype	06
bMasterInterface	00
bSlaveInterface0	01

(o) Call Management Functional Descriptors

Field	Value (Hexadecimal)
bFunctionLength	05
bDescriptorType	24
bDescriptorSubtype	01
bmCapabilities	03
bDataInterface	01

(p) Endpoint Descriptors (Interrupt-IN)

Field	Value (Hexadecimal)
bLength	07
bDescriptorType	05
bEndpointAddress	83
bmAttributes	03
wMaxPacketSize	0010
bInterval	10

(q) Endpoint Descriptors (Bulk-IN)

Field	Value (Hexadecimal)
bLength	07
bDescriptorType	05
bEndpointAddress	81
bmAttributes	02
wMaxPacketSize	0040
bInterval	02

(r) Endpoint Descriptors (Bulk-OUT)

Field	Value (Hexadecimal)
bLength	07
bDescriptorType	05
bEndpointAddress	02
bmAttributes	02
wMaxPacketSize	0040
bInterval	02

(s) STRING Descriptors

1. "Renesas"
2. "SH-MobileAP4 Firmware Downloader"

B.6.6.3 List of Commands and Responses

(1) Commands (Data from PC Side)

Command	Description	Code
Initialize Request	Sets the AP4 clock.	H'A0
Status Request	Confirms the condition of the status.	H'A1
Down Load Start	Notifies the start of download.	H'A2
Down Load Data	Transmits the download data.	H'A3
Down Load End Confirm*	Notifies the end of download.	H'A4
Program Start	Makes a subroutine call.	H'A5
Get Version	Acquires mask ROM version information.	H'AF

Note: * The Down Load End Confirm command can be used after the Down Load Data command has been issued.

(t) Responses (Data from AP4 Side)

Command	Description	Code
Command Response	Returns the response for the command.	H'B0
Down Load Response	Returns the download state.	H'B1
Down Load End Status	Returns the state after download.	H'B2
Version Information	Returns the mask ROM version information.	H'BF

B.6.6.4 Commands (Data from PC Side)

(Refer to appendix B.6.6.6, Details of Commands.)

- Other than Down Load Data

CMD	LEN	DATA1	DATA2	...

CMD: 1 byte, command code

LEN: 1 byte, data length (from DATA1 to end of DATA)

DATA: x bytes, data (number of bytes specified by LEN)

- Down Load Data

CMD	LEN (Upper)	LEN (Lower)	SEQNO (Upper)	SEQNO (Lower)	DATA1	DATA2	...	Checksum (Upper)	Checksum (Lower)

CMD: 1 byte, command code

LEN: 2 bytes, data length (from SEQNO to end of checksum)

SEQNO: 2 bytes, sequence number (from 0 to 65535)

DATA: x bytes, download data

Checksum: 2 bytes, checksum data

B.6.6.5 Responses (Data from AP4 Side)

(Refer to appendix B.6.6.7, Details of Responses.)

RES	LEN	DATA1	DATA2	...

RES: 1 byte, response code

LEN: 1 byte, data length (from DATA1 to end of DATA)

DATA: x bytes, data (number of bytes specified by LEN)

B.6.6.6 Details of Commands

(1) Initialize Request

Sets the clock for the AP4.

After receiving this command, the AP4 sets the clock and returns "Command Response (H'B0)".

CMD	LEN	CLOCK
H'A0	H'01	MODE

CLOCK MODE
- H'00: Clock setting A (SYS-CPU 800 MHz (see "Clock up SYS-CPU 800 MHz" in appendix B.7, Settings))
- H'01: Clock setting B (SYS-CPU 400 MHz (see "Clock up SYS-CPU 400 MHz" in appendix B.7, Settings))
- H'02: Reserved
- H'03: Clock setting D (Do not make this setting.)

(u) Status Request

Confirms the condition of the AP4 status.

After receiving this command, the AP4 immediately returns "Command Response (H'B0)".

CMD	LEN	KIND
H'A1	H'01	

KIND
- H'00: Confirms the command acceptance ready state
- H'01: Acquires the USB operating state (clock setting, and whether MERAM address restriction is applied or not)
- H'02: Acquires the return value from the subroutine call (4-byte return value from subroutine)
- H'03: Acquires the condition for a transition to USB download (standby flag register value)
- H'04: Acquires version information of the device
- H'03: Acquires RESCNT

(v) Down Load Start

Notifies the AP4 that download has started.

After receiving this command, the AP4 immediately returns "Down Load Response (H'B1)".

CMD H'A2	LEN H'08	ADDRESS (Highest)	ADDRESS (Second)	ADDRESS (Third)	ADDRESS (Lowest)	SIZE (Highest)	SIZE (Second)	SIZE (Third)	SIZE (Lowest)

ADDRESS: Download destination address (RAM address)*

DATA: Total size of binary data, including the header, that is to be downloaded by the download command

Note: * The address and size settings must be within the MERAM download area before the Program Start command is executed. If the MERAM area is exceeded, an error is returned.

(w) Down Load Data

Transmits the download data to the AP4.

After receiving this command, the AP4 immediately returns "Down Load Response (H'B1)".

CMD H'A3	LEN (Upper)	LEN (Lower)	SEQNO (Upper)	SEQNO (Lower)	DATA1	DATA2	...	Checksum (Upper)	Checksum (Lower)

LEN: Data length*[1]

SEQNO: Sequence number (The sequence number is incremented sequentially from 0 (max. 65535))

DATA: Download file*[2]

Checksum: Enter 2's complement of the value obtained by adding one byte each to DATA (discard the overflow of 2 bytes).

Notes: 1. Set a value of 6 bytes or more to LEN. If LEN exceeds 30704 bytes, it should be divided. An even value must be set to LEN.
2. Data is packetized sequentially from address 0 in bytes.

(x) Down Load End Confirm

Notifies the AP4 that transmission of download data has finished.

After receiving this command, the AP4 calculates the checksum and returns "Down Load End Status (H'B2)".

CMD H'A4	LEN H'02	Checksum (Upper)	Checksum (Lower)

Checksum: Enter the checksum (2's complement) of the total binary data of the download program (variable length).

(y) Program Start

Notifies the AP4 that download of data has started.

After receiving this command, the AP4 performs the secure check and makes a subroutine call to the last address specified by the Down Load Start command. Before calling the subroutine, the AP4 returns "Command Response (H'B0)". When the secure function is selected, a secure check is carried out and the result is returned. To acquire the return value from the subroutine, use the Status Request command.

CMD H'A5	LEN H'00

Note: For the subroutine format, use the following for reference.
(When a program is executed more than once at the same address, processes such as flushing I-Cache at the start and end of the subroutine are required.)

```
unsigned long func(void){
   Processing
return err;
}
```

(z) Get Version

Acquires the mask ROM version of the AP4.

After receiving this command, the AP4 acquires the version information and returns "Version Information (H'BF)".

The Get Version command must be transmitted before the Down Load Start command.

Note: Transmission of the Get Version command is arbitrary.

CMD H'AF	LEN H'00

B.6.6.7 Details of Responses

(1) Command Response

Returns the return value for the Initialize Request, Status Request, and Program Start commands.

CMD H'B0	LEN H'0x	DATA1	DATA2	...

LEN: Size of DATA

DATA:

- Response for Initialize Request
  DATA1: H'00: OK
  H'01: Error
- Response for Status Request
  When KIND is H'00
  DATA1: Ready state
  In the Busy state, no response is returned because it is waiting for the response.
  When KIND is H'01
  DATA1: CLOCK MODE value set by the Initialize Request command
  DATA2: With/without MERAM address restriction
  H'00: No restriction (subroutine call by the Program Start command already made)
  H'01: Restriction applied

When KIND is H'02

DATA1 to DATA4: Return value from subroutine call (4 bytes) (DATA1 to MSB)

Note: H'0000 0000 when no subroutine call is made

When KIND is H'03

DATA1: Value of standby flag register STBCHRB2

DATA2: Value of standby flag register STBCHRB3

When KIND is H'04

DATA1 to DATA4: Value of AP4 version information (CCCR value) (DATA1 to MSB)

DATA5 to DATA8: Fixed at 0

When KIND is H'05

DATA1 to DATA4: RESCNT value (bits other than MD4, MD3, MD2, MD6, and MD7 are fixed at 0)

- Response for Program Start

  DATA1: State before the program was called

  H'00: Normal activation

  H'01: Download error

  H'02: Secure error

  Note: When the response is H'00, a subroutine call is made after sending the response. For other responses, no subroutine call is made.

(aa) Down Load Response

Notifies that download data has been received.

CMD	LEN	DATA1	DATA2
H'B1	H'02	SEQ	STATUS

SEQ H'00: Success

H'01: Fail–SEQNO error (STATUS: Result of checksum value is returned (H'00 or H'02))

STATUS H'00: Success

H'01: Fail–CMD error (CMD sequence error or the specified address or size exceeds the range)

H'02: Fail–Checksum error in download of data

(bb) Down Load End Status

After download has completed, calculates the checksum and notifies whether download has finished successfully.

CMD	LEN	DATA1	DATA2	DATA3
H'B2	H'03	STATUS	Checksum (Upper)	Checksum (Lower)

STATUS H'00: Success
H'01: Fail (checksum error in download file)
H'02: Fail (secure error)

(cc) Version Information

Notifies the mask ROM version information.

CMD	LEN	DATA1	DATA2	...	DATA16
H'BF	H'10	Version[0]	Version[1]		Version[15]

DATA: Returns the class, date, and creation number of mask ROM (16 bytes).
Data format: "ROM_yymmdd_nn" for the AP4

Note: yy: Year, mm: Month, dd: Day, nn: Version number for each creation
Example: ROM_081020_01 (software version 01 created on October 20, 2008)

B.6.6.8 Timing Chart

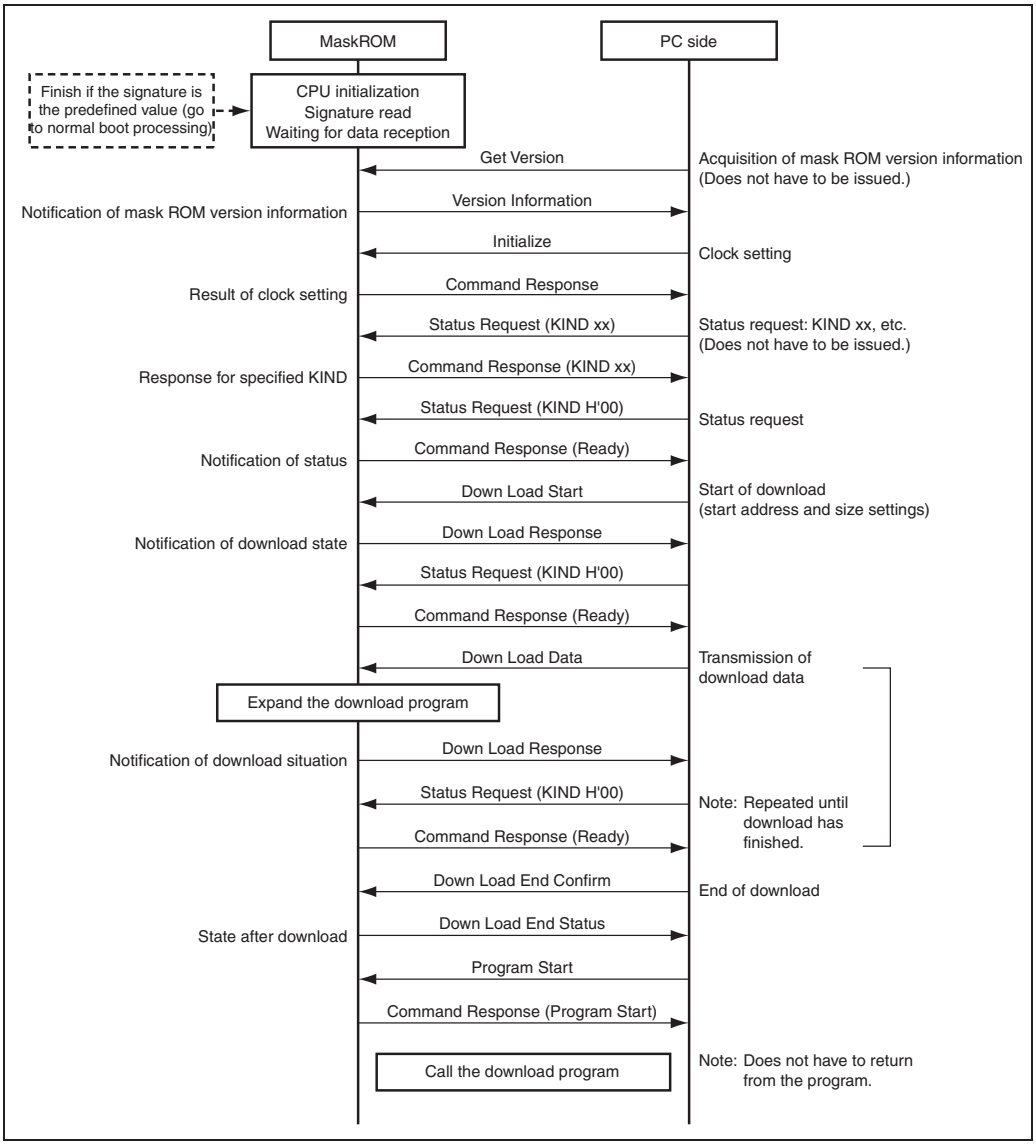


Figure B.23 USB Download Function

B.6.7 Message Format between ACPU and CCPU for MFI Boot Function

B.6.7.1 MFI Message Map

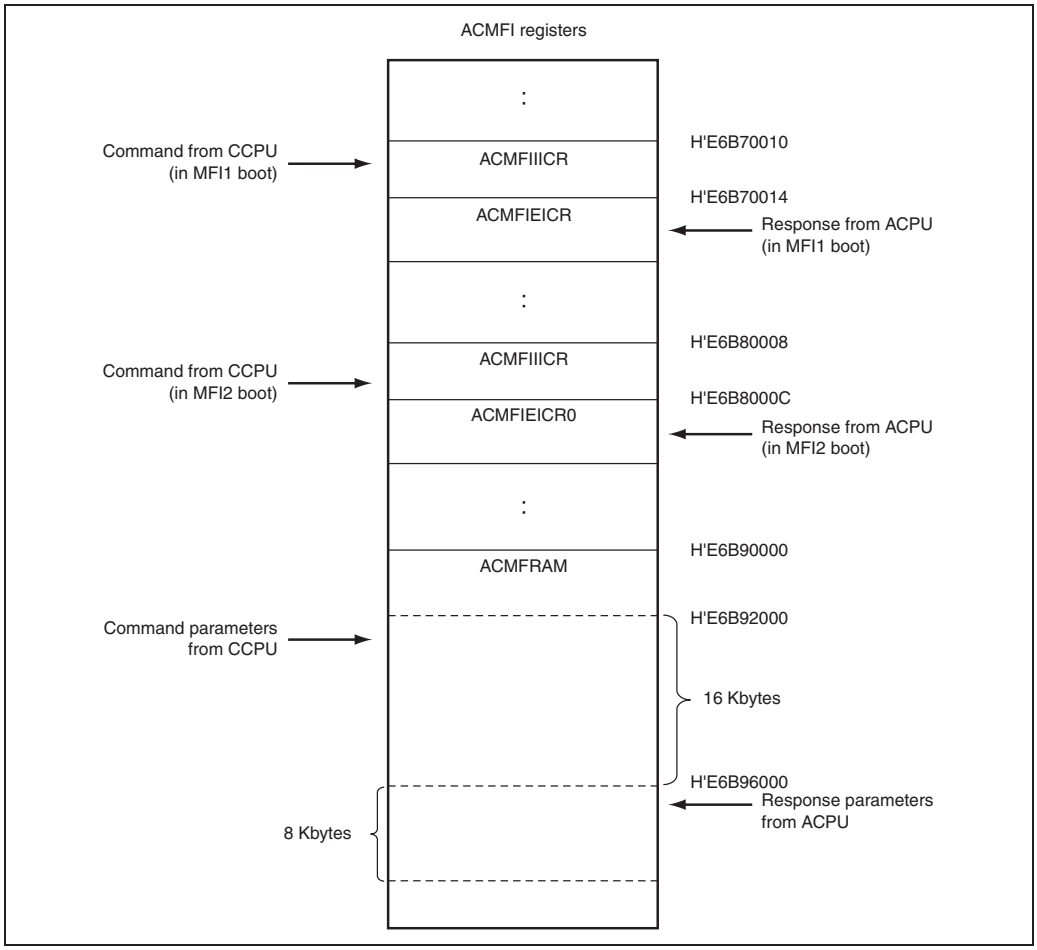


Figure B.24 MFI Message Map

B.6.7.2 List of Commands and Responses

(1) Commands (Data from CCPU Side)

Command	Description	Code (LSB is Command Issuance Bit)
Initialize Request	Sets the AP4 clock.	B'0000 001x
Status Request	Confirms the condition of the status.	B'0000 01H'
Get Version	Acquires mask ROM version information.	B'0000 011x
Program Start	Makes a subroutine call.	B'0000 10H'

(dd) Responses (Data from ACPU Side)

Command	Description	Code (LSB is ACPU Notification Bit)
Initialize complete	Notifies the end of Initialize Request.	B'0000 001x
Status notify	Confirms the condition of the status.	B'0000 01H'
Version notify	Notifies the mask ROM version information.	B'0000 011x
Program complete	Notifies the response for Program Start.	B'0000 10H'
Ready notify	Notifies that the Ready state is entered.	B'1000 00H'
Not Support Command Error	Receives an unsupported command.	B'0111 111x

B.6.7.3 Details of MFI Commands

(1) Initialize Request

Sets the clock for the AP4.

After receiving this command, the AP4 sets the clock and returns "Initialize complete (B'0000 001x)".

This command is arbitrary. (It does not have to be issued when operation continues to be at 400 MHz.)

Clock setting: 4 bytes (Specify it at the beginning of the command parameter area from the CCPU in 32 bits.)
0: 400 MHz
1: 800 MHz

(ee) Status Request

Confirms the condition of the AP4 status.

After receiving this command, the AP4 immediately returns "Status notify (B'0000 01H')".

(This command does not have parameters.)

(ff) Get Version

Acquires the mask ROM version of the AP4.

After receiving this command, the AP4 acquires the version information and returns "Version notify (B'0000 011x)".

Note: Transmission of the Get Version command is arbitrary.

(This command does not have parameters.)

(gg) Program Start

Notifies the AP4 that download of data has started.

(Locate the VRL4 format from the beginning of the command parameter area from the CCPU.)

After receiving this command, the AP4 makes a subroutine call to the start address of the MFRAM command parameter area. Before calling the subroutine, the AP4 returns "Program complete (B'0000 10H')". When the secure function is selected, a secure check is carried out and the result is returned. To acquire the return value from the subroutine, use the Status Request command.

On returning from the subroutine that was called after this command had been issued, cancel protection of the MFRAM area (command parameter and response parameter areas) and SDRAM area.

Note: The protection function is not available in MFI1 boot and MFI1 development boot modes.
For the subroutine format, use the following for reference.

```
unsigned long func(void){
   Processing
return err;
}
```

B.6.7.4 Details of MFI Responses

(1) Initialize complete

Returns the return value in response to the Initialize Request command.

After receiving the Initialize Request command, the CPU clock is set and that result is returned.

Setting result: 4 bytes (Returns it from the beginning of the response parameter area from the ACPU in 32 bits.)
0: OK
1: Error

(hh) Status notify

Notifies the status information in response to the Status Request command.

State: 4 bytes (Returns it from the beginning of the response parameter area from the ACPU in 32 bits.)
0: Ready state (The response is not returned for states other than Ready.)

Clock state: 4 bytes (Returns it from 4 + (beginning of the response parameter area from the ACPU) in 32 bits.)
0: 400 MHz
1: 800 MHz (Initialize Request setting)

Return value: 4 bytes (Returns it from 8 + (beginning of the response parameter area from the ACPU) in 32 bits.)
Return value from the command executed by the Program Start command

Reserved: 4 bytes (Returns it from 12 + (beginning of the response parameter area from the ACPU) in 32 bits.)
Fixed at 0

Device version: 8 bytes (Returns it from 16 + (beginning of the response parameter area from the ACPU) in 64 bits.)
CCCR value (offset0)
Fixed at 0 (offset4)

Boot setting: 4 bytes (Returns it from 24 + (beginning of the response parameter area from the ACPU) in 32 bits.)
Value of MD2 to MD7 bits in RESCNT

(ii) Version Information

Notifies the mask ROM version information in response to the Get Version command.

DATA: 16 bytes (Returns it from the beginning of the response parameter area from the ACPU.)
Returns the class, date, and creation number of mask ROM.
Data format: "ROM_yymmdd_nn" for the AP4

Note: yy: Year, mm: Month, dd: Day, nn: Version number for each creation
Example: ROM_080320_01 (software version 01 created on March 20, 2008)

(jj) Program complete

Notifies the result of the Program Start command.

After receiving the Program Start command, the secure check is performed (if the secure function is selected) and that result is notified just before program execution starts.

Confirm the return value after program execution by using the Status Request command.

Result: 4 bytes (Returns it from the beginning of the response parameter area from the ACPU.)
0: Normal activation (start of program execution)
1: Reserved
2: Secure error

(kk) Ready notify

Notifies that after activation following power supply or reset cancellation, the ACPU is activated in MFI boot mode and notifies that it has become ready to receive commands (MFRAM area (command parameter and response parameter areas) is protected).

After the response from the ACPU is confirmed, the CCPU clears the interrupt with the Ready notify value.

(There are no response parameters from the ACPU.)

Note: The protection function is not available in MFI1 boot and MFI1 development boot modes.

(ll) Not Support Command Error

This response is returned when the command sent from the CCPU is an unrecognizable command (unsupported command).

(There are no response parameters from the ACPU.)

B.6.7.5 MFI Timing Chart

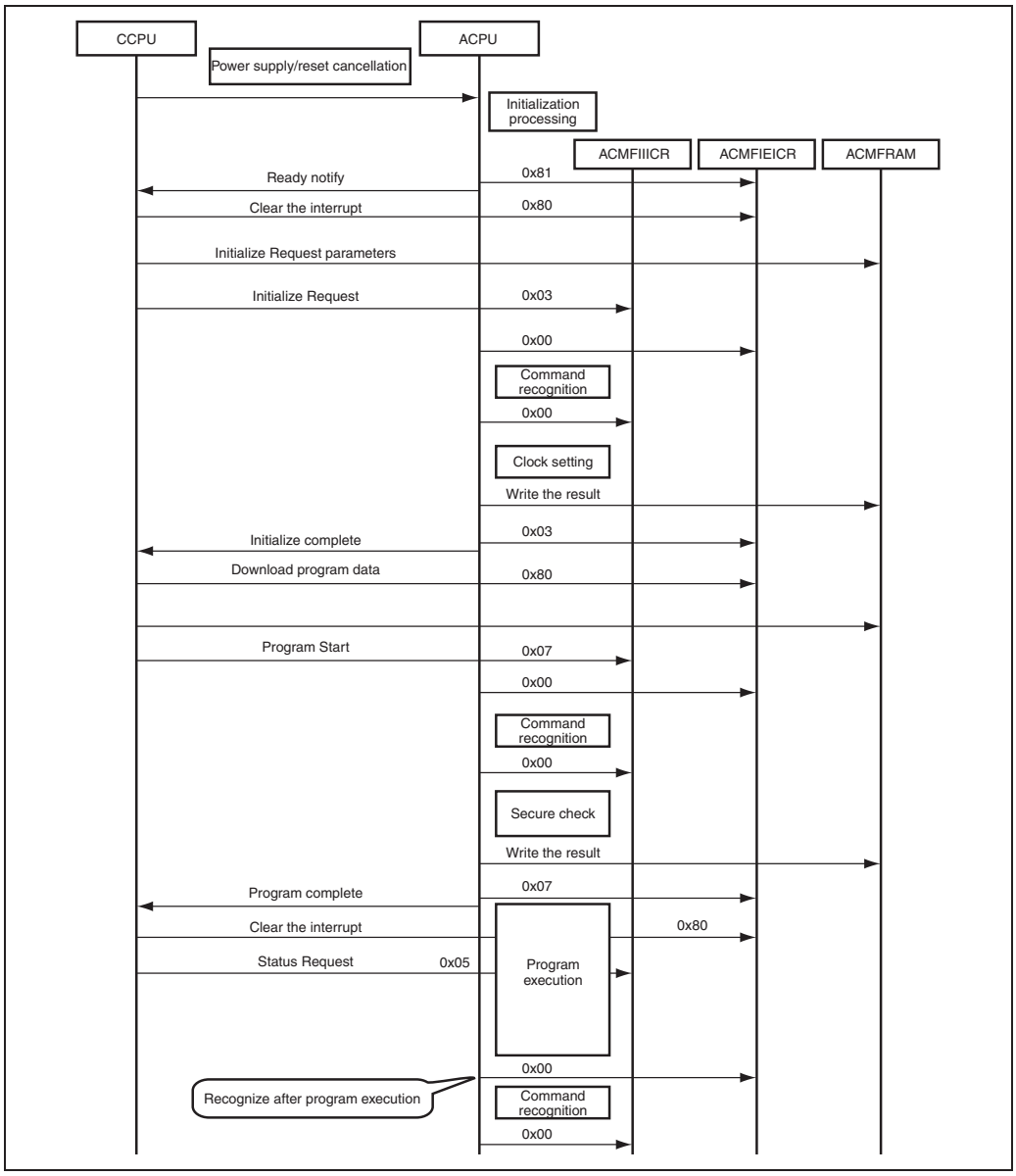


Figure B.25 MFI Download Function

B.7 Settings

Table B.8 List of Settings

Setting Condition	Register Name	Address	Setting	Remarks
All-time setting	RWTCSRA0	H'E6020004	| H'A580	
Clock up SYS-CPU 400 MHz	FRQCRA	H'E6150000	H'2D3305C3	Confirm that the KICK bit in FRQCRB is cleared before making this setting.
	FRQCRC	H'E61500E0	H'1E43353E	
	FRQCRB	H'E6150004	H'01331050 | H'80000000	Wait until the KICK bit (bit 31) is cleared.
	FRQCRD	H'E61500E4	H'00003000	Wait until the DDRPCHG bit (bit 31) is cleared.
	PLLC01CR	H'E6150028	H'00004000	Loop until the PLL01E bit is set.
Clock up SYS-CPU 800 MHz	FRQCRA	H'E6150000	H'2D1305C3	Confirm that the KICK bit in FRQCRB is cleared before making this setting.
	FRQCRC	H'E61500E0	H'1E43353E	
	FRQCRB	H'E6150004	H'00331050 | H'80000000	Wait until the KICK bit (bit 31) is cleared.
	FRQCRD	H'E61500E4	H'00003000	Wait until the DDRPCHG bit (bit 31) is cleared.
	PLLC01CR	H'E6150028	H'00004000	Loop until the PLL01E bit is set.
Cache setting			MRC p15,0,R2,c1,c0,0 ORR R2, R2, #H'1800 MCR p15,0,R2,c1,c0,0	L1 I-Cache, PFP ON
USB download only	SUBUSBCKCR	H'E6150080	& H'00004000	Wait until bit 14 is set to 1.
	SUBUSBCKCR	H'E6150080	|= H'00000100	
	SUBUSBCKCR	H'E6150080	= (USBCKCR & H'FFFFFF3F) | H'00000080	48 MHz is selected for EXTAL2.
	PLLC2CR	H' E615002C	&= H'7FFFFFFF	A frequency other than 48 MHz is selected for EXTAL2.
	SUBUSBCKCR	H'E6150080	= (SUBUSBCKCR & H'FFFFFF00 | H'0000004C)	
	PLLC2CR	H' E615002C	= (PLLC2CR & H'E0FFFFFF | H'17000000)	

Setting Condition	Register Name	Address	Setting	Remarks
USB download only	PLLC2CR	H' E615002C	= (PLLC2CR | H'80000000)	A frequency other than 48 MHz is selected for EXTAL2.
			while ((PLLC2CR & H'80000000)==H'00000000)	
	SUBUSBCKCR	H'E6150080	&= H'FFFFFEFF	
NAND boot only	PORT66CR	H'E6052042	H'12	Function 2 (FCE1) is selected.
	SMSTPCR3	H'E615013C	&= ~H'00008000	
	SRCR3	H'E61580B8	&= ~H'00008000	
	SMSTPCR2	H'E6150138	&= ~H'00040000	
	SRCR2	H'E61580B0	&= ~H'00040000	
	DMA1RS_0	H'FE009000	H'8783	
	FLCMNCR	H'E6A30000	H'00180211	
	FLCMDCR	H'E6A30004	H'00010000	
	FLCMCDR	H'E6A30008	H'000000FF	Reset
	FLDTCNTR	H'E6A30014	H'00000000	
	FLBSYTMR	H'E6A3001C	H'00000000	
	FLTRCR	H'E6A3002C	H'01	Wait until bit 1 is set to 1.
	FLCMNCR	H'E6A30000	H'00180201	
	FLTRCR	H'E6A3002C	H'00	
	FLCMNCR	H'E6A30000	H'00180211	
	FLCMDCR	H'E6A30004	H'02010000	
	FLCMCDR	H'E6A30008	H' 00000070	Status read
	FLDTCNTR	H'E6A30014	H' 00000002	
	FLBSYTMR	H'E6A3001C	H'00000000	
	FLTRCR	H'E6A3002C	H'01	Wait until bit 1 is set to 1.
	FLCMNCR	H'E6A30000	H'00180201	
	FLTRCR	H'E6A3002C	H'00	
	DMA1TCR_0	H'FE008028	H'00000020	
	DMA1TCR_1	H'FE008038	H'00000001	
	DMA1SAR_0	H'FE008020	H'E6A30050	
	DMA1DAR_0	H'FE008024	Buffer address	
	DMA1SAR_1	H'FE008030	H'E6A30060	

Setting Condition	Register Name	Address	Setting	Remarks
NAND boot only	DMA1DAR_1	H'FE008034	Buffer address	
	FLINTDMACR	H'E6A30018	H'000C0000	
	FLINTDMACR	H'E6A30018	H'00000000	
	DMA1CHCR_0	H'FE00802C	H'00004819	
	DMA1CHCR_1	H'FE00803C	H'00004819	
	FLCMNCR	H'E6A30000	H'00DC0611	
	FLCMDCR	H'E6A30004	H'87030001	1-sector read H'070F0001 for NAND(4)
	FLCMCDR	H'E6A30008	H'00003000	
	FLINTDMACR	H'E6A30018	H'00530000	
	FLADR	H'E6A3000C	NAND address	
	FLADR2	H'E6A3003C	H'00000000	
	FLBSYTMR	H'E6A3001C	H'00000000	
	FLHOLDCR	H'E6A30038	H'00000001	
	DMA1OR	H'FE008060	H'0001	
	FLTRCR	H'E6A3002C	H'01	
	FLTRCR	H'E6A3002C	—	Transfer state check
	FL4ECCCR	H'E6A30090	H'00000000	Clear this register after the check.
	DMA1CHCR_0	H'FE00802C	—	Confirm bit 1.
	DMA1CHCR_1	H'FE00803C	—	Confirm bit 1.
	FLTRCR	H'E6A3002C	—	Confirm bit 1.
	FL4ECCCR	H'E6A30090	H'00000000	Clear this register after the check.
	FLCMNCR	H'E6A30000	H'00DC0601	
	FLTRCR	H'E6A3002C	H'00	
	DMA1OR	H'FE008060	H'0000	
eSD boot only	PORT179CR	H'E60520B3	H'11	
	PORT180CR	H'E60520B4	H'C1	
	PORT181CR	H'E60520B5	H'C1	
	PORT182CR	H'E60520B6	H'C1	
	PORT183CR	H'E60520B7	H'C1	

Setting Condition	Register Name	Address	Setting	Remarks
eSD boot only	PORT184CR	H'E60520B8	H'C1	
	MSTP3	H'E615013C	&= H'FFFFDFFF	Manipulate only bit 13.
eMMC boot only	MSTP3	H'E615013C	&=~H'00001000	Clear the module stop state of the MMC.
eMMC boot 1A, eMMC boot 2A, eMMC development boot 1A, and eMMC development boot 2A only	PORT84CR	H'E6050054	H'C4	MEMC_AD8 -> MMCD0_0 (function 4)
	PORT85CR	H'E6050055	H'C4	MEMC_AD9 -> MMCD0_1 (function 4)
	PORT86CR	H'E6050056	H'C4	MEMC_AD10 -> MMCD0_2 (function 4)
	PORT87CR	H'E6050057	H'C4	MEMC_AD11 -> MMCD0_3 (function 4)
	PORT88CR	H'E6050058	H'C4	MEMC_AD12 -> MMCD0_4 (function 4)
	PORT89CR	H'E6050059	H'C4	MEMC_AD13 -> MMCD0_5 (function 4)
	PORT90CR	H'E605005A	H'C4	MEMC_AD14 -> MMCD0_6 (function 4)
	PORT91CR	H'E605005B	H'C4	MEMC_AD15 -> MMCD0_7 (function 4)
	PORT92CR	H'E605005C	H'C4	MEMC_CS0 -> MMCCMD0 (function 4)
	PORT99CR	H'E6050063	H'14	MEMC_INT -> MMCCLK0 (function 4)
	MSEL4CR	H'E6058024	&=~H'00008000	MMC pin setting (MFI in the background)
eMMC boot 1B, eMMC boot 2B, eMMC development boot 1B, and eMMC development boot 2B only	PORT54CR	H'E6052036	H'C3	D8 -> MMCD0_0 (function 3)
	PORT55CR	H'E6052037	H'C3	D9 -> MMCD0_1 (function 3)
	PORT56CR	H'E6052038	H'C3	D10 -> MMCD0_2 (function 3)
	PORT57CR	H'E6052039	H'C3	D11 -> MMCD0_3 (function 3)
	PORT58CR	H'E605203A	H'C3	D12 -> MMCD0_4 (function 3)

Setting Condition	Register Name	Address	Setting	Remarks
eMMC boot 1B, eMMC boot 2B, eMMC development boot 1B, and eMMC development boot 2B only	PORT59CR	H'E605203B	H'C3	D13 -> MMCD0_5 (function 3)
	PORT60CR	H'E605203C	H'C3	D14 -> MMCD0_6 (function 3)
	PORT61CR	H'E605203D	H'C3	D15 -> MMCD0_7 (function 3)
	PORT67CR	H'E6052043	H'C3	CS6A_ -> MMCCMD0 (function 3)
	PORT66CR	H'E6052042	H'13	CS5B_ -> MMCCLK0 (function 3)
	MSEL4CR	H'E6058024	|=H'00008000	MMC pin setting (BSC in the background)

Appendix G Register List

G.1 Register Configuration of Bus Functions

G.1.1 Register Configuration of SHwy Bus Functions (RealTime GPR)

Register Name	Abbreviation	R/W	Initial Value	Address	Access Size
PRI control register	RTPRPRICR	R/W	H'0000 001E	H'FF800018	32
HS-GPR arbitration register 1	RTPRARCR11	R/W	H'0000 0000	H'FF800030	32
HS-GPR arbitration register 2	RTPRARCR12	R/W	H'0000 0000	H'FF800038	32
Error contorol register	RTPRERRMSK	R/W	H'0000 0000	H'FF800090	32

G.1.2 Register Configuration of SHwy Bus Functions (HS GPR)

Register Name	Abbreviation	R/W	Initial Value	Address	Access Size
PRI control register	HSPRPRICR	R/W	H'0000 0000	H'FFA00018	32
SBSC1 arbitration register 1	HSPRARCR11	R/W	H'0000 0000	H'FFA00030	32
SBSC1 arbitration register 2	HSPRARCR12	R/W	H'0000 0000	H'FFA00038	32
SBSC1 arbitration register 3	HSPRARCR13	R/W	H'0000 0000	H'FFA00040	32
ICB arbitration register 1	HSPRARCR21	R/W	H'0000 0000	H'FFA00050	32
ICB arbitration register 2	HSPRARCR22	R/W	H'0000 0000	H'FFA00058	32
ICB arbitration register 3	HSPRARCR23	R/W	H'0000 0000	H'FFA00060	32
COM-GPR arbitration register 1	HSPRARCR31	R/W	H'0000 0000	H'FFA00070	32
COM-GPR arbitration register 2	HSPRARCR32	R/W	H'0000 0000	H'FFA00078	32
COM-GPR arbitration register 3	HSPRARCR33	R/W	H'0000 0000	H'FFA00080	32
Error control register	HSPRERRMSK	R/W	H'0000 0000	H'FFA00090	32
SBSC1 priority setting register 1	HSPRPRICNT11	R/W	H'4040 4040	H'FFA000A0	32
SBSC1 priority setting register 2	HSPRPRICNT12	R/W	H'0000 4040	H'FFA000A8	32
SBSC1 priority setting register 3	HSPRPRICNT13	R/W	H'0000 0000	H'FFA000B0	32

G.1.3 Register Configuration of SHwy Bus Functions (Com GPR)

Register Name	Abbreviation	R/W	Initial Value	Address	Access Size
PRI control register	CMPRPRICR	R/W	H'0000 01FF	H'FF700018	32
SBSC1 arbitration register 1	CMPRARCR11	R/W	H'0000 0000	H'FF700030	32
SBSC1 arbitration register 2	CMPRARCR12	R/W	H'0000 0000	H'FF700038	32
SBSC1 arbitration register 3	CMPRARCR13	R/W	H'0000 0000	H'FF700040	32
SBSC1 arbitration register 4	CMPRARCR14	R/W	H'0000 0000	H'FF700048	32
SBSC1 arbitration register 5	CMPRARCR15	R/W	H'0000 0000	H'FF700050	32

Register Name	Abbreviation	R/W	Initial Value	Address	Access Size
HS-GPR arbitration register 1	CMPRARCR21	R/W	H'0000 0000	H'FF700060	32
HS-GPR arbitration register 2	CMPRARCR22	R/W	H'0000 0000	H'FF700068	32
HS-GPR arbitration register 3	CMPRARCR23	R/W	H'0000 0000	H'FF700070	32
HS-GPR arbitration register 4	CMPRARCR24	R/W	H'0000 0000	H'FF700078	32
HS-GPR arbitration register 5	CMPRARCR25	R/W	H'0000 0000	H'FF700080	32
Error control register	CMPRERRMSK	R/W	H'0000 0000	H'FF700090	32
SBSC1 priority setting register 1	CMPRPRICNT11	R/W	H'4040 4040	H'FF7000A0	32
SBSC1 priority setting register 2	CMPRPRICNT12	R/W	H'4040 4040	H'FF7000A8	32
SBSC1 priority setting register 3	CMPRPRICNT13	R/W	H'0000 0040	H'FF7000B0	32
SBSC1 priority setting register 3	CMPRPRICNT14	R/W	H'0000 0000	H'FF7000B8	32

G.1.4 Register Configuration of SHWYSTAT

Register Name	Abbreviation	R/W	Initial Value	Address	Access Size
Transaction statistics control register	SHST??CR	R/W	H'0000 0000	H'XXXX0000	32
Interrupt control register	SHST??IR	R/W	H’0000 0000	H’XXXX0004	32
DMA transfer control register	SHST??DMR	R/W	H’0000 0000	H’XXXX0008	32
DMA transfer data register	SHST??DATA	R	Undefined	H’XXXX0100	32
Measurement count register	SHST??CNT	R/W	H’0000 0000	H’XXXX000C	32
Measurement cycle count set register	SHST??TN	R/W	H’0000 0000	H’XXXX0010	32
Pass request count register	SHST??TR	R/W	H'0000 0000	H'XXXX0014	32
Address mask register 1	SHST??AM1	R/W	H’0000 0000	H’XXXX0018	32
Address mask register 2	SHST??AM2	R/W	H’0000 0000	H’XXXX001C	32
Transaction mask register	SHST??TM	R/W	H’0000 0000	H’XXXX0020	32
Transaction statistics register 00	SHST??SR00	R	H'0000 FFFF	H'XXXX0030	32
Transaction statistics register 01	SHST??SR01	R	H'0000 0000	H'XXXX0034	32
Transaction statistics register 02	SHST??SR02	R	H’0000 0000	H’XXXX0038	32
Transaction statistics register 10	SHST??SR10	R	H'0000 FFFF	H'XXXX003C	32
Transaction statistics register 11	SHST??SR11	R	H'0000 0000	H'XXXX0040	32
Transaction statistics register 12	SHST??SR12	R	H’0000 0000	H’XXXX0044	32
Transaction statistics register 20	SHST??SR20	R	H'0000 FFFF	H'XXXX0048	32
Transaction statistics register 21	SHST??SR21	R	H'0000 0000	H'XXXX004C	32
Transaction statistics register 22	SHST??SR22	R	H'0000 0000	H'XXXX0050	32
Transaction statistics register 30	SHST??SR30	R	H'0000 FFFF	H'XXXX0054	32
Transaction statistics register 31	SHST??SR31	R	H'0000 0000	H'XXXX0058	32
Transaction statistics register 32	SHST??SR32	R	H'0000 0000	H'XXXX005C	32
Transaction statistics register 40	SHST??SR40	R	H'0000 FFFF	H'XXXX0060	32
Transaction statistics register 41	SHST??SR41	R	H'0000 0000	H'XXXX0064	32
Transaction statistics register 42	SHST??SR42	R	H'0000 0000	H'XXXX0068	32
Transaction statistics register 50	SHST??SR50	R	H'0000 FFFF	H'XXXX006C	32

Register Name	Abbreviation	R/W	Initial Value	Address	Access Size
Transaction statistics register 51	SHST??SR51	R	H'0000 0000	H'XXXX0070	32
Transaction statistics register 52	SHST??SR52	R	H'0000 0000	H'XXXX0074	32
Transaction statistics register 60	SHST??SR60	R	H'0000 FFFF	H'XXXX0078	32
Transaction statistics register 61	SHST??SR61	R	H'0000 0000	H'XXXX007C	32
Transaction statistics register 70	SHST??SR70	R	H'0000 FFFF	H'XXXX0080	32
Transaction statistics register 71	SHST??SR71	R	H'0000 0000	H'XXXX0084	32
Transaction statistics register 80	SHST??SR80	R	H'0000 FFFF	H'XXXX0088	32
Transaction statistics register 81	SHST??SR81	R	H'0000 0000	H'XXXX008C	32
Transaction statistics register 90	SHST??SR90	R	H'0000 FFFF	H'XXXX0090	32
Transaction statistics register 91	SHST??SR91	R	H'0000 0000	H'XXXX0094	32
Transaction statistics register 100	SHST??SR100	R	H'0000 FFFF	H'XXXX0098	32
Transaction statistics register 101	SHST??SR101	R	H'0000 0000	H'XXXX009C	32
Transaction statistics register 110	SHST??SR110	R	H'0000 FFFF	H'XXXX00A0	32
Transaction statistics register 111	SHST??SR111	R	H'0000 0000	H'XXXX00A4	32

??: RT/HS/CM

XXXX: RT=H'FFCF, HS=H'E6F3, CM=H'E6F2

G.1.5 Register Configuration of HPB Control

Register Name	Register Abbreviation	R/W	Initial Value	Address	Access Size
HPB control register 0	HPBCTRL0	R/W	H'0000 0000	H'E6001010	32
HPB control register 1	HPBCTRL1	R/W	H'0000 0000	H'E6001014	32
HPB control register 2	HPBCTRL2	R/W	H'0000 0000	H'E6001018	32
Common Chip Code register	CCCR	R	-	H'E600101C	32
HPB control register 4	HPBCTRL4	R/W	H'0000 0000	H'E6001024	32
HPB control register 5	HPBCTRL5	R/W	H'0000 088C	H'E6001028	32

G.1.6 Register Configuration of HPB Semaphore Control

Register Name	Abbreviation	R/W	Initial Value	Address	Access Size
Master ID register	MPSRC	R/W	–	H'E6001600	32
Master access control register	MPACCTL	R/W	H'0000 0000	H'E6001604	32
GPIO semaphore acquisition ID register	SMGPIOSRC	R/W	H'0000 0000	H'E6001820	32
GPIO semaphore error register	SMGPIOERR	R/W	H'0000 0000	H'E6001824	32
GPIO semaphore timeout setting register	SMGPIOTIME	R/W	H'7FFF FFFF	H'E6001828	32
GPIO semaphore timeout counter	SMGPIOCNT	R	H'0000 0000	H'E600182C	32

Register Name	Abbreviation	R/W	Initial Value	Address	Access Size
DBG semaphore acquisition ID register	SMDBGSRC	R/W	H'0000 0000	H'E6001830	32
DBG semaphore error register	SMDBGERR	R/W	H'0000 0000	H'E6001834	32
DBG semaphore timeout setting register	SMDBGTIME	R/W	H'7FFF FFFF	H'E6001838	32
DBG semaphore timeout counter	SMDBGCNT	R	H'0000 0000	H'E600183C	32
CMT2 semaphore acquisition ID register	SMCMT2SRC	R/W	H'0000 0000	H'E6001840	32
CMT2 semaphore error register	SMCMT2ERR	R/W	H'0000 0000	H'E6001844	32
CMT2 semaphore timeout setting register	SMCMT2TIME	R/W	H'7FFF FFFF	H'E6001848	32
CMT2 semaphore timeout counter	SMCMT2CNT	R	H'0000 0000	H'E600184C	32
CPGLA semaphore acquisition ID register	SMCPGASRC	R/W	H'0000 0000	H'E6001850	32
CPGLA semaphore error register	SMCPGAERR	R/W	H'0000 0000	H'E6001854	32
CPGLA semaphore timeout setting register	SMCPGATIME	R/W	H'7FFF FFFF	H'E6001858	32
CPGLA semaphore timeout counter	SMCPGACNT	R	H'0000 0000	H'E600185C	32
SYSC semaphore acquisition ID register	SMSYSCSRC	R/W	H'0000 0000	H'E6001870	32
SYSC semaphore error register	SMSYSCERR	R/W	H'0000 0000	H'E6001874	32
SYSC semaphore timeout setting register	SMSYSCTIME	R/W	H'7FFF FFFF	H'E6001878	32
SYSC semaphore timeout counter	SMSYSCCNT	R	H'0000 0000	H'E600187C	32

G.1.7 Register Configuration of Security Function

Register Name	Abbreviation	R/W	Initial Value	Address	Access Size
RBAR protection setting register	GRDRBAR	R/W	H'0000 0000	H'E6001500	32
SBAR protection setting register	GRDSBAR	R/W	H'0000 0000	H'E6001504	32

G.2 Register Configuration of AP-System Core

Register Name	Abbreviation	R/W	Address	Access Size
Priority register	APARMPRI	R/W	H'E6F1 0000	32
Address translation area register	APARMBAREA	R/W	H'E6F1 0020	32

G.3 Register Configuration of IPMMU

Register Name	Abbreviation	R/W	Address *1	Access Size
IPMMU control register 1	IMCTR1	R/W	H'xxxx x000	32
IPMMU control register 2	IMCTR2	R/W	H'xxxx x004	32
IPMMU status register	IMSTR	R/W	H'xxxx x008	32
IPMMU exception address register	IMEAR	R/W	H'xxxx x00C	32
IPMMU ASID register	IMASID	R/W	H'xxxx x010	32
IPMMU translation table base register	IMTTBR	R/W	H'xxxx x014	32
IPMMU translation table base control register	IMTTBCR	R/W	H'xxxx x018	32
IPMMU DMAC channel enable control register *2	IMDCEN	R/W	H'xxxx x020	32
IPMMU PMB address array 0 to IPMMU PMB address array 15	IMPMBA0 to IMPMBA15	R/W	H'xxxx x080 to H'xxxx x0BC	32
IPMMU PMB data array 0 to IPMMU PMB data array 15	IMPMBD0 to IMPMBD15	R/W	H'xxxx x0C0 to H'xxxx x0FC	32

*1 The "xxxx x" parts in the Address column are as follows according to IPMMUs:
IPMMUI: FE951
IPMMUR: FFC30
IPMMUR2:FFC40

*2 IMDCEN exist only on IPMMUR and IPMMUR2

G.4 Register Configuration of INTC

G.4.1 Register Configuration of INTCA

Register Name	Abbreviation	R/W	Address	Access Size
Interrupt control register 1A	ICR1A	R/W	H'E690 0000	32
Interrupt control register 2A	ICR2A	R/W	H'E690 0004	32
Interrupt control register 3A	ICR3A	R/W	H'E690 0008	32
Interrupt control register 4A	ICR4A	R/W	H'E690 000C	32
Interrupt flag register	INTFLGA	R	H'E698 0018	32
Interrupt event register	INTEVTA	R/W	H'E698 0020	32
Interrupt level register A	INTLVLA	R/W	H'E698 0030	8
Interrupt level register B	INTLVLB	R/W	H'E698 0034	8

Register Name	Abbreviation	R/W	Address	Access Size
AP-Realtime core individual interrupt source register	INTEVTAS	R	H'E694 0100	32
AP-Realtime core interrupt mask register	INTSMASK	R/W	H'E694 0104	16
Interrupt priority register 00A	INTPRI00A	R/W	H'E690 0010	32
Interrupt priority register 10A	INTPRI10A	R/W	H'E690 0014	32
Interrupt priority register 20A	INTPRI20A	R/W	H'E690 0018	32
Interrupt priority register 30A	INTPRI30A	R/W	H'E690 001C	32
Interrupt source register 00A	INTREQ00A	R/W	H'E690 0020	8
Interrupt source register 10A	INTREQ10A	R/W	H'E690 0024	8
Interrupt source register 20A	INTREQ20A	R/W	H'E690 0028	8
Interrupt source register 30A	INTREQ30A	R/W	H'E690 002C	8
Interrupt mask register 00A	INTMSK00A	R/W	H'E690 0040	8
Interrupt mask register 10A	INTMSK10A	R/W	H'E690 0044	8
Interrupt mask register 20A	INTMSK20A	R/W	H'E690 0048	8
Interrupt mask register 30A	INTMSK30A	R/W	H'E690 004C	8
Interrupt mask clear register 00A	INTMSKCLR00A	W	H'E690 0060	8
Interrupt mask clear register 10A	INTMSKCLR10A	W	H'E690 0064	8
Interrupt mask clear register 20A	INTMSKCLR20A	W	H'E690 0068	8
Interrupt mask clear register 30A	INTMSKCLR30A	W	H'E690 006C	8
FIQ status register A	FIQSRA	R/W	H'E698 00C0	16
User interrupt mask level register A	USERIMASKA	R/W	H'E69C 0000	32
Peripheral interrupt priority register AA	IPRAA	R/W	H'E694 0000	16
Peripheral interrupt priority register BA	IPRBA	R/W	H'E694 0004	16
Peripheral interrupt priority register CA	IPRCA	R/W	H'E694 0008	16
Peripheral interrupt priority register DA	IPRDA	R/W	H'E694 000C	16
Peripheral interrupt priority register EA	IPREA	R/W	H'E694 0010	16
Peripheral interrupt priority register FA	IPRFA	R/W	H'E694 0014	16
Peripheral interrupt priority register GA	IPRGA	R/W	H'E694 0018	16
Peripheral interrupt priority register HA	IPRHA	R/W	H'E694 001C	16
Peripheral interrupt priority register IA	IPRIA	R/W	H'E694 0020	16
Peripheral interrupt priority register JA	IPRJA	R/W	H'E694 0024	16
Peripheral interrupt priority register KA	IPRKA	R/W	H'E694 0028	16
Peripheral interrupt priority register LA	IPRLA	R/W	H'E694 002C	16
Peripheral interrupt priority register MA	IPRMA	R/W	H'E694 0030	16
Peripheral interrupt priority register NA	IPRNA	R/W	H'E694 0034	16
Peripheral interrupt priority register OA	IPROA	R/W	H'E694 0038	16
Peripheral interrupt priority register AA3	IPRAA3	R/W	H'E695 0000	16
Peripheral interrupt priority register BA3	IPRBA3	R/W	H'E695 0004	16
Peripheral interrupt priority register CA3	IPRCA3	R/W	H'E695 0008	16
Peripheral interrupt priority register DA3	IPRDA3	R/W	H'E695 000C	16
Peripheral interrupt priority register EA3	IPREA3	R/W	H'E695 0010	16
Peripheral interrupt priority register FA3	IPRFA3	R/W	H'E695 0014	16
Peripheral interrupt priority register GA3	IPRGA3	R/W	H'E695 0018	16
Peripheral interrupt priority register HA3	IPRHA3	R/W	H'E695 001C	16

Register Name	Abbreviation	R/W	Address	Access Size
Peripheral interrupt priority register IA3	IPRIA3	R/W	H'E695 0020	16
Peripheral interrupt priority register JA3	IPRJA3	R/W	H'E695 0024	16
Peripheral interrupt priority register KA3	IPRKA3	R/W	H'E695 0028	16
Peripheral interrupt priority register LA3	IPRLA3	R/W	H'E695 002C	16
Peripheral interrupt priority register MA3	IPRMA3	R/W	H'E695 0030	16
Peripheral interrupt priority register NA3	IPRNA3	R/W	H'E695 0034	16
Peripheral interrupt priority register OA3	IPROA3	R/W	H'E695 0038	16
Peripheral interrupt priority register PA3	IPRPA3	R/W	H'E695 003C	16
Peripheral interrupt priority register RA3	IPRRA3	R/W	H'E6950040	16
Peripheral interrupt priority register SA3	IPRSA3	R/W	H'E6950044	16
Peripheral interrupt priority register SA3	IPRSA3	R/W	H'E6950048	16
Peripheral interrupt priority register TA3	IPRTA3	R/W	H'E695004C	16
Peripheral interrupt priority register UA3	IPRUA3	R/W	H'E6950050	16
Peripheral interrupt mask register 0A	IMR0A	R/W	H'E694 0080	8
Peripheral interrupt mask register 1A	IMR1A	R/W	H'E694 0084	8
Peripheral interrupt mask register 2A	IMR2A	R/W	H'E694 0088	8
Peripheral interrupt mask register 3A	IMR3A	R/W	H'E694 008C	8
Peripheral interrupt mask register 4A	IMR4A	R/W	H'E694 0090	8
Peripheral interrupt mask register 5A	IMR5A	R/W	H'E694 0094	8
Peripheral interrupt mask register 6A	IMR6A	R/W	H'E694 0098	8
Peripheral interrupt mask register 7A	IMR7A	R/W	H'E694 009C	8
Peripheral interrupt mask register 8A	IMR8A	R/W	H'E694 00A0	8
Peripheral interrupt mask register 9A	IMR9A	R/W	H'E694 00A4	8
Peripheral interrupt mask register 10A	IMR10A	R/W	H'E694 00A8	8
Peripheral interrupt mask register 11A	IMR11A	R/W	H'E694 00AC	8
Peripheral interrupt mask register 12A	IMR12A	R/W	H'E694 00B0	8
Peripheral interrupt mask register 13A	IMR13A	R/W	H'E694 00B4	8
Peripheral interrupt mask register 0A3	IMR0A3	R/W	H'E695 0080	8
Peripheral interrupt mask register 1A3	IMR1A3	R/W	H'E695 0084	8
Peripheral interrupt mask register 2A3	IMR2A3	R/W	H'E695 0088	8
Peripheral interrupt mask register 3A3	IMR3A3	R/W	H'E695 008C	8
Peripheral interrupt mask register 4A3	IMR4A3	R/W	H'E695 0090	8
Peripheral interrupt mask register 5A3	IMR5A3	R/W	H'E695 0094	8
Peripheral interrupt mask register 6A3	IMR6A3	R/W	H'E695 0098	8
Peripheral interrupt mask register 7A3	IMR7A3	R/W	H'E695 009C	8
Peripheral interrupt mask register 8A3	IMR8A3	R/W	H'E69500A0	8
Peripheral interrupt mask register 9A3	IMR9A3	R/W	H'E69500A4	8
Peripheral interrupt mask register 10A3	IMR10A3	R/W	H'E69500A8	8
Peripheral interrupt mask clear register 0A	IMCR0A	W	H'E694 00C0	8
Peripheral interrupt mask clear register 1A	IMCR1A	W	H'E694 00C4	8
Peripheral interrupt mask clear register 2A	IMCR2A	W	H'E694 00C8	8
Peripheral interrupt mask clear register 3A	IMCR3A	W	H'E694 00CC	8
Peripheral interrupt mask clear register 4A	IMCR4A	W	H'E694 00D0	8
Peripheral interrupt mask clear register 5A	IMCR5A	W	H'E694 00D4	8

Register Name	Abbreviation	R/W	Address	Access Size
Peripheral interrupt mask clear register 6A	IMCR6A	W	H'E694 00D8	8
Peripheral interrupt mask clear register 7A	IMCR7A	W	H'E694 00DC	8
Peripheral interrupt mask clear register 8A	IMCR8A	W	H'E694 00E0	8
Peripheral interrupt mask clear register 9A	IMCR9A	W	H'E694 00E4	8
Peripheral interrupt mask clear register 10A	IMCR10A	W	H'E694 00E8	8
Peripheral interrupt mask clear register 11A	IMCR11A	W	H'E694 00EC	8
Peripheral interrupt mask clear register 12A	IMCR12A	W	H'E694 00F0	8
Peripheral interrupt mask clear register 13A	IMCR13A	W	H'E694 00F4	8
Peripheral interrupt mask clear register 0A3	IMCR0A3	W	H'E695 00C0	8
Peripheral interrupt mask clear register 1A3	IMCR1A3	W	H'E695 00C4	8
Peripheral interrupt mask clear register 2A3	IMCR2A3	W	H'E695 00C8	8
Peripheral interrupt mask clear register 3A3	IMCR3A3	W	H'E695 00CC	8
Peripheral interrupt mask clear register 4A3	IMCR4A3	W	H'E695 00D0	8
Peripheral interrupt mask clear register 5A3	IMCR5A3	W	H'E695 00D4	8
Peripheral interrupt mask clear register 6A3	IMCR6A3	W	H'E695 00D8	8
Peripheral interrupt mask clear register 7A3	IMCR7A3	W	H'E695 00DC	8
Peripheral interrupt mask clear register 8A3	IMCR8A3	W	H'E69500E0	8
Peripheral interrupt mask clear register 9A3	IMCR9A3	W	H'E69500E4	8
Peripheral interrupt mask clear register 10A3	IMCR10A3	W	H'E69500E8	8
Peripheral interrupt mask register 0AS	IMR0AS	R/W	H'E694 0180	8
Peripheral interrupt mask register 1AS	IMR1AS	R/W	H'E694 0184	8
Peripheral interrupt mask register 2AS	IMR2AS	R/W	H'E694 0188	8
Peripheral interrupt mask register 3AS	IMR3AS	R/W	H'E694 018C	8
Peripheral interrupt mask register 4AS	IMR4AS	R/W	H'E694 0190	8
Peripheral interrupt mask register 5AS	IMR5AS	R/W	H'E694 0194	8
Peripheral interrupt mask register 6AS	IMR6AS	R/W	H'E694 0198	8
Peripheral interrupt mask register 7AS	IMR7AS	R/W	H'E694 019C	8
Peripheral interrupt mask register 8AS	IMR8AS	R/W	H'E694 01A0	8
Peripheral interrupt mask register 9AS	IMR9AS	R/W	H'E694 01A4	8
Peripheral interrupt mask register 10AS	IMR10AS	R/W	H'E694 01A8	8
Peripheral interrupt mask register 11AS	IMR11AS	R/W	H'E694 01AC	8
Peripheral interrupt mask register 12AS	IMR12AS	R/W	H'E694 01B0	8
Peripheral interrupt mask register 13AS	IMR13AS	R/W	H'E694 01B4	8
Peripheral interrupt mask register 0AS3	IMR0AS3	R/W	H'E695 0180	8
Peripheral interrupt mask register 1AS3	IMR1AS3	R/W	H'E695 0184	8
Peripheral interrupt mask register 2AS3	IMR2AS3	R/W	H'E695 0188	8
Peripheral interrupt mask register 3AS3	IMR3AS3	R/W	H'E695 018C	8
Peripheral interrupt mask register 4AS3	IMR4AS3	R/W	H'E695 0190	8
Peripheral interrupt mask register 5AS3	IMR5AS3	R/W	H'E695 0194	8
Peripheral interrupt mask register 6AS3	IMR6AS3	R/W	H'E695 0198	8
Peripheral interrupt mask register 7AS3	IMR7AS3	R/W	H'E695 019C	8
Peripheral interrupt mask register 8AS3	IMR8AS3	R/W	H'E69501A0	8
Peripheral interrupt mask register 9AS3	IMR9AS3	R/W	H'E69501A4	8
Peripheral interrupt mask register 10AS3	IMR10AS3	R/W	H'E69501A8	8

Register Name	Abbreviation	R/W	Address	Access Size
Peripheral interrupt mask clear register 0AS	IMCR0AS	W	H'E694 01C0	8
Peripheral interrupt mask clear register 1AS	IMCR1AS	W	H'E694 01C4	8
Peripheral interrupt mask clear register 2AS	IMCR2AS	W	H'E694 01C8	8
Peripheral interrupt mask clear register 3AS	IMCR3AS	W	H'E694 01CC	8
Peripheral interrupt mask clear register 4AS	IMCR4AS	W	H'E694 01D0	8
Peripheral interrupt mask clear register 5AS	IMCR5AS	W	H'E694 01D4	8
Peripheral interrupt mask clear register 6AS	IMCR6AS	W	H'E694 01D8	8
Peripheral interrupt mask clear register 7AS	IMCR7AS	W	H'E694 01DC	8
Peripheral interrupt mask clear register 8AS	IMCR8AS	W	H'E694 01E0	8
Peripheral interrupt mask clear register 9AS	IMCR9AS	W	H'E694 01E4	8
Peripheral interrupt mask clear register 10AS	IMCR10AS	W	H'E694 01E8	8
Peripheral interrupt mask clear register 11AS	IMCR11AS	W	H'E694 01EC	8
Peripheral interrupt mask clear register 12AS	IMCR12AS	W	H'E694 01F0	8
Peripheral interrupt mask clear register 13AS	IMCR13AS	W	H'E694 01F4	8
Peripheral interrupt mask clear register 0AS3	IMCR0AS3	W	H'E695 01C0	8
Peripheral interrupt mask clear register 1AS3	IMCR1AS3	W	H'E695 01C4	8
Peripheral interrupt mask clear register 2AS3	IMCR2AS3	W	H'E695 01C8	8
Peripheral interrupt mask clear register 3AS3	IMCR3AS3	W	H'E695 01CC	8
Peripheral interrupt mask clear register 4AS3	IMCR4AS3	W	H'E695 01D0	8
Peripheral interrupt mask clear register 5AS3	IMCR5AS3	W	H'E695 01D4	8
Peripheral interrupt mask clear register 6AS3	IMCR6AS3	W	H'E695 01D8	8
Peripheral interrupt mask clear register 7AS3	IMCR7AS3	W	H'E695 01DC	8
Peripheral interrupt mask clear register 8AS3	IMCR8AS3	W	H'E69501E0	8
Peripheral interrupt mask clear register 9AS3	IMCR9AS3	W	H'E69501E4	8
Peripheral interrupt mask clear register 10AS3	IMCR10AS3	W	H'E69501E8	8
IRQ status check register0	ISCR0	R/W	H'E690 00C4	32
IRQ status check register1	ISCR1	R/W	H'E690 00C8	32
Pulse interrupt flag register 0A	IFLG0A	R/W	H'E694 0110	8
Pseudo-interrupt setting register 0A	SIR0A	R/W	H'E694 0114	8
DIRC interrupt setting register 0A	DIRCR	R/W	H'E694 0118	8
Secure control register	LIFEC_SEC_SRC	R/W	H'E611 0008	32

G.4.2 Register Configuration of INTCS

Register Name	Abbreviation	R/W	Address	Access Size
Interrupt control register 0S	ICR0S	R/W	H'FFD1 0000	32
Interrupt control register 1S	ICR1S	R/W	H'FFD1 0004	32
Interrupt control register 2S	ICR2S	R/W	H'FFD1 0008	32
Interrupt control register 3S	ICR3S	R/W	H'FFD1 000C	32
Interrupt control register 3	ICR3	R/W	H'E605 8040	32
Interrupt control register 4	ICR4	R/W	H'E605 8044	32
Interrupt control register 5	ICR5	R/W	H'E605 8048	32

Register Name	Abbreviation	R/W	Address	Access Size
Interrupt control register 6	ICR6	R/W	H'E605 804C	32
Interrupt control register 7	ICR7	R/W	H'E605 8050	32
Interrupt control register 8	ICR8	R/W	H'E605 8054	32
Interrupt control register 9	ICR9	R/W	H'E605 8058	32
Interrupt control register 10	ICR10	R/W	H'E605 805C	32
Interrupt priority register 00S	INTPRI00S	R/W	H'FFD1 0010	32
Interrupt priority register 10S	INTPRI10S	R/W	H'FFD1 0014	32
Interrupt priority register 20S	INTPRI20S	R/W	H'FFD1 0018	32
Interrupt priority register 30S	INTPRI30S	R/W	H'FFD1 001C	32
Interrupt source register 00S	INTREQ00S	R/W	H'FFD1 0020	8
Interrupt source register 10S	INTREQ10S	R/W	H'FFD1 0024	8
Interrupt source register 20S	INTREQ20S	R/W	H'FFD1 0028	8
Interrupt source register 30S	INTREQ30S	R/W	H'FFD1 002C	8
Interrupt mask register 00S	INTMSK00S	R/W	H'FFD1 0040	8
Interrupt mask register 10S	INTMSK10S	R/W	H'FFD1 0044	8
Interrupt mask register 20S	INTMSK20S	R/W	H'FFD1 0048	8
Interrupt mask register 30S	INTMSK30S	R/W	H'FFD1 004C	8
Interrupt mask clear register 00S	INTMSKCLR00S	W	H'FFD1 0060	8
Interrupt mask clear register 10S	INTMSKCLR10S	W	H'FFD1 0064	8
Interrupt mask clear register 20S	INTMSKCLR20S	W	H'FFD1 0068	8
Interrupt mask clear register 30S	INTMSKCLR30S	W	H'FFD1 006C	8
AP-System core individual interrupt source register	INTEVTSA	R	H'FFD2 0100	32
NMI flag control register S	NMIFCRS	R/W	H'FFD3 00C0	16
AP-System core interrupt mask register	INTAMASK	R/W	H'FFD2 0104	16
User interrupt mask level register S	USERIMASKS	R/W	H'FFD4 0000	32
Peripheral interrupt priority register AS	IPRAS	R/W	H'FFD2 0000	16
Peripheral interrupt priority register BS	IPRBS	R/W	H'FFD2 0004	16
Peripheral interrupt priority register CS	IPRCS	R/W	H'FFD2 0008	16
Peripheral interrupt priority register DS	IPRDS	R/W	H'FFD2 000C	16
Peripheral interrupt priority register ES	IPRES	R/W	H'FFD2 0010	16
Peripheral interrupt priority register FS	IPRFS	R/W	H'FFD2 0014	16
Peripheral interrupt priority register GS	IPRGS	R/W	H'FFD2 0018	16
Peripheral interrupt priority register HS	IPRHS	R/W	H'FFD2 001C	16
Peripheral interrupt priority register IS	IPRIS	R/W	H'FFD2 0020	16
Peripheral interrupt priority register JS	IPRJS	R/W	H'FFD2 0024	16
Peripheral interrupt priority register KS	IPRKS	R/W	H'FFD2 0028	16
Peripheral interrupt priority register LS	IPRLS	R/W	H'FFD2 002C	16
Peripheral interrupt priority register MS	IPRMS	R/W	H'FFD2 0030	16
Peripheral interrupt priority register AS3	IPRAS3	R/W	H'FFD5 0000	16
Peripheral interrupt priority register BS3	IPRBS3	R/W	H'FFD5 0004	16
Peripheral interrupt priority register CS3	IPRCS3	R/W	H'FFD5 0008	16
Peripheral interrupt priority register DS3	IPRDS3	R/W	H'FFD5 000C	16
Peripheral interrupt priority register ES3	IPRES3	R/W	H'FFD5 0010	16

Register Name	Abbreviation	R/W	Address	Access Size
Peripheral interrupt priority register FS3	IPRFS3	R/W	H'FFD5 0014	16
Peripheral interrupt priority register GS3	IPRGS3	R/W	H'FFD5 0018	16
Peripheral interrupt priority register HS3	IPRHS3	R/W	H'FFD5 001C	16
Peripheral interrupt priority register IS3	IPRIS3	R/W	H'FFD5 0020	16
Peripheral interrupt priority register JS3	IPRJS3	R/W	H'FFD5 0024	16
Peripheral interrupt priority register KS3	IPRKS3	R/W	H'FFD5 0028	16
Peripheral interrupt priority register LS3	IPRLS3	R/W	H'FFD5 002C	16
Peripheral interrupt priority register MS3	IPRMS3	R/W	H'FFD5 0030	16
Peripheral interrupt priority register NS3	IPRNS3	R/W	H'FFD5 0034	16
Peripheral interrupt priority register OS3	IPROS3	R/W	H'FFD5 0038	16
Peripheral interrupt priority register PS3	IPRPS3	R/W	H'FFD5003C	16
Peripheral interrupt mask register 0S	IMR0S	R/W	H'FFD2 0080	8
Peripheral interrupt mask register 1S	IMR1S	R/W	H'FFD2 0084	8
Peripheral interrupt mask register 2S	IMR2S	R/W	H'FFD2 0088	8
Peripheral interrupt mask register 3S	IMR3S	R/W	H'FFD2 008C	8
Peripheral interrupt mask register 4S	IMR4S	R/W	H'FFD2 0090	8
Peripheral interrupt mask register 5S	IMR5S	R/W	H'FFD2 0094	8
Peripheral interrupt mask register 6S	IMR6S	R/W	H'FFD2 0098	8
Peripheral interrupt mask register 7S	IMR7S	R/W	H'FFD2 009C	8
Peripheral interrupt mask register 8S	IMR8S	R/W	H'FFD2 00A0	8
Peripheral interrupt mask register 9S	IMR9S	R/W	H'FFD2 00A4	8
Peripheral interrupt mask register 10S	IMR10S	R/W	H'FFD2 00A8	8
Peripheral interrupt mask register 11S	IMR11S	R/W	H'FFD2 00AC	8
Peripheral interrupt mask register 12S	IMR12S	R/W	H'FFD2 00B0	8
Peripheral interrupt mask register 0S3	IMR0S3	R/W	H'FFD5 0080	8
Peripheral interrupt mask register 1S3	IMR1S3	R/W	H'FFD5 0084	8
Peripheral interrupt mask register 2S3	IMR2S3	R/W	H'FFD5 0088	8
Peripheral interrupt mask register 3S3	IMR3S3	R/W	H'FFD5 008C	8
Peripheral interrupt mask register 4S3	IMR4S3	R/W	H'FFD5 0090	8
Peripheral interrupt mask register 5S3	IMR5S3	R/W	H'FFD5 0094	8
Peripheral interrupt mask register 6S3	IMR6S3	R/W	H'FFD5 0098	8
Peripheral interrupt mask register 7S3	IMR7S3	R/W	H'FFD5 009C	8
Peripheral interrupt mask clear register 0S	IMCR0S	W	H'FFD2 00C0	8
Peripheral interrupt mask clear register 1S	IMCR1S	W	H'FFD2 00C4	8
Peripheral interrupt mask clear register 2S	IMCR2S	W	H'FFD2 00C8	8
Peripheral interrupt mask clear register 3S	IMCR3S	W	H'FFD2 00CC	8
Peripheral interrupt mask clear register 4S	IMCR4S	W	H'FFD2 00D0	8
Peripheral interrupt mask clear register 5S	IMCR5S	W	H'FFD2 00D4	8
Peripheral interrupt mask clear register 6S	IMCR6S	W	H'FFD2 00D8	8
Peripheral interrupt mask clear register 7S	IMCR7S	W	H'FFD2 00DC	8
Peripheral interrupt mask clear register 8S	IMCR8S	W	H'FFD2 00E0	8
Peripheral interrupt mask clear register 9S	IMCR9S	W	H'FFD2 00E4	8
Peripheral interrupt mask clear register 10S	IMCR10S	W	H'FFD2 00E8	8
Peripheral interrupt mask clear register 11S	IMCR11S	W	H'FFD2 00EC	8

Register Name	Abbreviation	R/W	Address	Access Size
Peripheral interrupt mask clear register 12S	IMCR12S	W	H'FFD2 00F0	8
Peripheral interrupt mask clear register 0S3	IMCR0S3	W	H'FFD5 00C0	8
Peripheral interrupt mask clear register 1S3	IMCR1S3	W	H'FFD5 00C4	8
Peripheral interrupt mask clear register 2S3	IMCR2S3	W	H'FFD5 00C8	8
Peripheral interrupt mask clear register 3S3	IMCR3S3	W	H'FFD5 00CC	8
Peripheral interrupt mask clear register 4S3	IMCR4S3	W	H'FFD5 00D0	8
Peripheral interrupt mask clear register 5S3	IMCR5S3	W	H'FFD5 00D4	8
Peripheral interrupt mask clear register 6S3	IMCR6S3	W	H'FFD5 00D8	8
Peripheral interrupt mask clear register 7S3	IMCR7S3	W	H'FFD5 00DC	8
Peripheral interrupt mask register 0SA	IMR0SA	R/W	H'FFD2 0180	8
Peripheral interrupt mask register 1SA	IMR1SA	R/W	H'FFD2 0184	8
Peripheral interrupt mask register 2SA	IMR2SA	R/W	H'FFD2 0188	8
Peripheral interrupt mask register 3SA	IMR3SA	R/W	H'FFD2 018C	8
Peripheral interrupt mask register 4SA	IMR4SA	R/W	H'FFD2 0190	8
Peripheral interrupt mask register 5SA	IMR5SA	R/W	H'FFD2 0194	8
Peripheral interrupt mask register 6SA	IMR6SA	R/W	H'FFD2 0198	8
Peripheral interrupt mask register 7SA	IMR7SA	R/W	H'FFD2 019C	8
Peripheral interrupt mask register 8SA	IMR8SA	R/W	H'FFD2 01A0	8
Peripheral interrupt mask register 9SA	IMR9SA	R/W	H'FFD2 01A4	8
Peripheral interrupt mask register 10SA	IMR10SA	R/W	H'FFD2 01A8	8
Peripheral interrupt mask register 11SA	IMR11SA	R/W	H'FFD2 01AC	8
Peripheral interrupt mask register 12SA	IMR12SA	R/W	H'FFD2 01B0	8
Peripheral interrupt mask register 0SA3	IMR0SA3	R/W	H'FFD5 0180	8
Peripheral interrupt mask register 1SA3	IMR1SA3	R/W	H'FFD5 0184	8
Peripheral interrupt mask register 2SA3	IMR2SA3	R/W	H'FFD5 0188	8
Peripheral interrupt mask register 3SA3	IMR3SA3	R/W	H'FFD5 018C	8
Peripheral interrupt mask register 4SA3	IMR4SA3	R/W	H'FFD5 0190	8
Peripheral interrupt mask register 5SA3	IMR5SA3	R/W	H'FFD5 0194	8
Peripheral interrupt mask register 6SA3	IMR6SA3	R/W	H'FFD5 0198	8
Peripheral interrupt mask register 7SA3	IMR7SA3	R/W	H'FFD5 019C	8
Peripheral interrupt mask clear register 0SA	IMCR0SA	W	H'FFD2 01C0	8
Peripheral interrupt mask clear register 1SA	IMCR1SA	W	H'FFD2 01C4	8
Peripheral interrupt mask clear register 2SA	IMCR2SA	W	H'FFD2 01C8	8
Peripheral interrupt mask clear register 3SA	IMCR3SA	W	H'FFD2 01CC	8
Peripheral interrupt mask clear register 4SA	IMCR4SA	W	H'FFD2 01D0	8
Peripheral interrupt mask clear register 5SA	IMCR5SA	W	H'FFD2 01D4	8
Peripheral interrupt mask clear register 6SA	IMCR6SA	W	H'FFD2 01D8	8
Peripheral interrupt mask clear register 7SA	IMCR7SA	W	H'FFD2 01DC	8
Peripheral interrupt mask clear register 8SA	IMCR8SA	W	H'FFD2 01E0	8
Peripheral interrupt mask clear register 9SA	IMCR9SA	W	H'FFD2 01E4	8
Peripheral interrupt mask clear register 10SA	IMCR10SA	W	H'FFD2 01E8	8
Peripheral interrupt mask clear register 11SA	IMCR11SA	W	H'FFD2 01EC	8
Peripheral interrupt mask clear register 12SA	IMCR12SA	W	H'FFD2 01F0	8
Peripheral interrupt mask clear register 0SA3	IMCR0SA3	W	H'FFD5 01C0	8

Register Name	Abbreviation	R/W	Address	Access Size
Peripheral interrupt mask clear register 1SA3	IMCR1SA3	W	H'FFD5 01C4	8
Peripheral interrupt mask clear register 2SA3	IMCR2SA3	W	H'FFD5 01C8	8
Peripheral interrupt mask clear register 3SA3	IMCR3SA3	W	H'FFD5 01CC	8
Peripheral interrupt mask clear register 4SA3	IMCR4SA3	W	H'FFD5 01D0	8
Peripheral interrupt mask clear register 5SA3	IMCR5SA3	W	H'FFD5 01D4	8
Peripheral interrupt mask clear register 6SA3	IMCR6SA3	W	H'FFD5 01D8	8
Peripheral interrupt mask clear register 7SA3	IMCR7SA3	W	H'FFD5 01DC	8
Pulse interrupt flag register 0S	IFLG0S	R/W	H'FFD2 0110	8
Pseudo-interrupt register 0S	SIR0S	R/W	H'FFD2 0114	8

G.4.3 Register Configuration of LSI Internal Communication Interrupt/Wakeup Function (Request to AP Block)

Register Name	Abbreviation	R/W	Address	Access Size
AP block LSI internal communication interrupt/wakeup function register	CCOMIFAP	R/W	H'E605 8000	32
AP block LSI internal communication interrupt/wakeup source register	CCOMIEAP	R	H'E605 8004	32
AP block LSI internal communication interrupt/wakeup source clear register	CCOMICAP	W	H'E605 8008	32

G.4.4 Register Configuration of LSI Internal Communication Interrupt/Wakeup Function (Request to SYS)

Register Name	Abbreviation	R/W	Address	Access Size
SYS domain LSI internal communication interrupt/wakeup function register	CCOMIFR2S	R/W	H'E605 XXXX	32
SYS domain LSI internal communication interrupt/wakeup source register	CCOMIER2S	R	H'E605 XXXX	32
SYS domain LSI internal communication interrupt/wakeup source clear register	CCOMICR2S	W	H'E605 XXXX	32

G.4.5 Register Configuration of LSI Internal Communication Interrupt/Wakeup Function (Request to RT)

Register Name	Abbreviation	R/W	Address	Access Size

Register Name	Abbreviation	R/W	Address	Access Size
RT domain LSI internal communication interrupt/wakeup function register	CCOMIFS2R	R/W	H'E605 XXXX	32
RT domain LSI internal communication interrupt/wakeup source register	CCOMIES2R	R	H'E605 XXXX	32
RT domain LSI internal communication interrupt/wakeup source clear register	CCOMICS2R	W	H'E605 XXXX	32

G.5 Register Configuration of BSC

Register Name	Abbreviation	R/W	Address	Access Size
Common control register	CMNCR	R/W	H'FEC1 0000	32
CS0 space bus control register	CS0BCR	R/W	H'FEC1 0004	32
CS2 space bus control register	CS2BCR	R/W	H'FEC1 0008	32
CS4 space bus control register	CS4BCR	R/W	H'FEC1 0010	32
CS5A space bus control register	CS5ABCR	R/W	H'FEC1 0014	32
CS6A space bus control register	CS6ABCR	R/W	H'FEC1 001C	32
CS0 space wait control register	CS0WCR	R/W	H'FEC1 0024	32
CS2 space wait control register	CS2WCR	R/W	H'FEC1 0028	32
CS4 space wait control register	CS4WCR	R/W	H'FEC1 0030	32
CS5A space wait control register	CS5AWCR	R/W	H'FEC1 0034	32
CS6A space wait control register	CS6AWCR	R/W	H'FEC1 003C	32
Reset bus wait counter	RBWTCNT	-	H'FEC1 0054	32
Busy control register	BUSYCR	R/W	H'FEC1 0058	32
Burst ROM timing control register	BROMTIMCR	R/W	H'FEC1 0070	32
Memory protection area settings register 00	BPTCR00	R/W	H'FEC1 0090	32
Memory protection area settings register 01	BPTCR01	R/W	H'FEC1 0094	32
Memory protection area settings register 02	BPTCR02	R/W	H'FEC1 0098	32
Memory protection area settings register 03	BPTCR03	R/W	H'FEC1 009C	32
Memory protection area settings register 04	BPTCR04	R/W	H'FEC1 00A0	32
Memory protection area settings register 05	BPTCR05	R/W	H'FEC1 00A4	32
Memory protection area settings register 06	BPTCR06	R/W	H'FEC1 00A8	32
Memory protection area settings register 07	BPTCR07	R/W	H'FEC1 00AC	32
Memory protection area settings register 08	BPTCR08	R/W	H'FEC1 00B0	32

Register Name	Abbreviation	R/W	Address	Access Size
Memory protection area settings register 09	BPTCR09	R/W	H'FEC1 00B4	32
Memory protection area settings register 10	BPTCR10	R/W	H'FEC1 00B8	32
Memory protection area settings register 11	BPTCR11	R/W	H'FEC1 00BC	32
Memory protection area settings register 12	BPTCR12	R/W	H'FEC1 00C0	32
Memory protection area settings register 13	BPTCR13	R/W	H'FEC1 00C4	32
Memory protection area settings register 14	BPTCR14	R/W	H'FEC1 00C8	32
Memory protection area settings register 15	BPTCR15	R/W	H'FEC1 00CC	32
Memory protection area settings register 16	BPTCR16	R/W	H'FEC1 00D0	32
Memory protection area settings register 17	BPTCR17	R/W	H'FEC1 00D4	32
Memory protection area settings register 18	BPTCR18	R/W	H'FEC1 00D8	32
Memory protection area settings register 19	BPTCR19	R/W	H'FEC1 00DC	32
Memory protection area settings register 20	BPTCR20	R/W	H'FEC1 00E0	32
Memory protection area settings register 21	BPTCR21	R/W	H'FEC1 00E4	32
Memory protection area settings register 22	BPTCR22	R/W	H'FEC1 00E8	32
Memory protection area settings register 23	BPTCR23	R/W	H'FEC1 00EC	32
Memory protection area settings register 24	BPTCR24	R/W	H'FEC1 00F0	32
Memory protection area settings register 25	BPTCR25	R/W	H'FEC1 00F4	32
Memory protection area settings register 26	BPTCR26	R/W	H'FEC1 00F8	32
Memory protection area settings register 27	BPTCR27	R/W	H'FEC1 00FC	32
Memory protection area settings register 28	BPTCR28	R/W	H'FEC1 0100	32
Memory protection area settings register 29	BPTCR29	R/W	H'FEC1 0104	32
Memory protection area settings register 30	BPTCR30	R/W	H'FEC1 0108	32
Memory protection area settings register 31	BPTCR31	R/W	H'FEC1 010C	32

Register Name	Abbreviation	R/W	Address	Access Size
BS_N assert period control register	BSWCR	R/W	H'FEC1 0110	32
CS0 space wait control register 2	CS0WCR2	R/W	H'FEC1 0224	32
CS2 space wait control register 2	CS2WCR2	R/W	H'FEC1 0228	32
CS4 space wait control register 2	CS4WCR2	R/W	H'FEC1 0230	32

G.6 Register Configuration of SBSC

Register Name	Abbreviation	R/W	Address	Access Size
SDRAM control register 0A	SDCR0A	R/W	H'FE40 0008	32
SDRAM control register 1A	SDCR1A	R/W	H'FE40 000C	32
SDRAM control register 0SA	SDCR0SA	R/W	H'FE40 0018	32
SDRAM Common wait control register0A	SDWCRC0A	R/W	H'FE40 0040	32
SDRAM Common wait control register1A	SDWCRC1A	R/W	H'FE40 0044	32
SDRAM Common wait control register2A	SDWCRC2A	R/W	H'FE40 0064	32
SDRAM wait control register00A	SDWCR00A	R/W	H'FE40 0048	32
SDRAM wait control register01A	SDWCR01A	R/W	H'FE40 004C	32
Power-down control register 0A	SDPDCR0A	R/W	H'FE40 0058	32
Extend bank mode registerA	EBMCRA	R/W	H'FE40 0014	32
SDRAM pin control register A	SDPCRA	R/W	H'FE40 0010	32
Refresh timer control/status register A	RTCSRA	R/W	H'FE40 0020	32*1
Refresh timer counter A	RTCNTA	R/W	H'FE40 0024	32*1
Refresh time constant register A	RTCORA	R/W	H'FE40 0028	32*1
Refresh time constant register HA	RTCORHA	R/W	H'FE40 002C	32*1
Refresh time constant registerSA	RTCORSA	R/W	H'FE40 0030	32*1
Refresh time constant registerSHA	RTCORSHA	R/W	H'FE40 0034	32*1
Refresh count register A	RFCRA	R/W	H'FE40 0038	32*1
Burst refresh count register A	BSTRCNTA	R/W	H'FE40 003C	32
SDRAM mode register A*2	SDMRA	R/W	H'FE5x xxxx	8/32
SDRAM mode register addres/commod register0A	SDMRACR0A	R/W	H'FE40 0084	32
SDRAM mode register addres/commod register1A	SDMRACR1A	R/W	H'FE40 0088	32
SDRAM mode register temp control registerA	SDMRTMPCRA	R/W	H'FE40 008C	32
SDRAM mode register temp monitor registerA	SDMRTMPMONA	R/W	H'FE40 0090	32
SDRAM mode register temp monitor mask registerA	SDMRTMPMSKA	R/W	H'FE40 0094	32

Register Name	Abbreviation	R/W	Address	Access Size
SDRAM General-purpose down counter down counterA	SDGENCNTA	R/W	H'FE40 009C	32
SDRAM drivability control register 0A	SDDRVCR0A	R/W	H'FE40 00B4	32
SDRAM drivability control register 1A	SDDRVCR1A	R/W	H'FE40 00B8	32
Memory protected area division register0A	SDPTDIVCR0A	R/W	H'FE40 00F0	32
Memory protected area division register1A	SDPTDIVCR1A	R/W	H'FE40 00F4	32
Memory protected area division register2A	SDPTDIVCR2A	R/W	H'FE40 00F8	32
Memory protected area setting register0A	SDPTCR0A	R/W	H'FE40 0100	32
Memory protected area setting register1A	SDPTCR1A	R/W	H'FE40 0104	32
Memory protected area setting register2A	SDPTCR2A	R/W	H'FE40 0108	32
Memory protected area setting register3A	SDPTCR3A	R/W	H'FE40 010C	32
DLL control register0A	DLLCNT0A	R/W	H'FE40 0354	32
SBSC monitor register0A	SBSCMON0A	R	H'FE40 0358	32

*1. To prevent the erroneous writing, 32-bit write operations only are performed when the upper 16 bits of the write data are H'A55A. Otherwise, write operations are not performed. The upper 16 bits of the data are read as H'0000.

*2. The entity of this register is in SDRAM. Data is written to the register in the SDRAM by accessing the register space for it. For details, refer to section 7.6.2 (3),LPDDR2-S4 internal register access function.

G.7 Register Configuration of DMAC

Register Name	Abbreviation	R/W	Address	Access Size
DMA1 source address register_0	DMA1SAR_0	R/W	H'FE00 8020	32
DMA1 destination address register_0	DMA1DAR_0	R/W	H'FE00 8024	32
DMA1 transfer count register_0	DMA1TCR_0	R/W	H'FE00 8028	32
DMA1 channel control register_0	DMA1CHCR_0	R/W	H'FE00 802C	32
DMA1 source address register_1	DMA1SAR_1	R/W	H'FE00 8030	32
DMA1 destination address register_1	DMA1DAR_1	R/W	H'FE00 8034	32
DMA1 transfer count register_1	DMA1TCR_1	R/W	H'FE00 8038	32
DMA1 channel control register_1	DMA1CHCR_1	R/W	H'FE00 803C	32
DMA1 source address register_2	DMA1SAR_2	R/W	H'FE00 8040	32
DMA1 destination address register_2	DMA1DAR_2	R/W	H'FE00 8044	32

Register Name	Abbreviation	R/W	Address	Access Size
DMA1 transfer count register_2	DMA1TCR_2	R/W	H'FE00 8048	32
DMA1 channel control register_2	DMA1CHCR_2	R/W	H'FE00 804C	32
DMA1 source address register_3	DMA1SAR_3	R/W	H'FE00 8050	32
DMA1 destination address register_3	DMA1DAR_3	R/W	H'FE00 8054	32
DMA1 transfer count register_3	DMA1TCR_3	R/W	H'FE00 8058	32
DMA1 channel control register_3	DMA1CHCR_3	R/W	H'FE00 805C	32
DMA1 operation register	DMA1OR	R/W	H'FE00 8060	16
DMA1 source address register_4	DMA1SAR_4	R/W	H'FE00 8070	32
DMA1 destination address register_4	DMA1DAR_4	R/W	H'FE00 8074	32
DMA1 transfer count register_4	DMA1TCR_4	R/W	H'FE00 8078	32
DMA1 channel control register_4	DMA1CHCR_4	R/W	H'FE00 807C	32
DMA1 source address register_5	DMA1SAR_5	R/W	H'FE00 8080	32
DMA1 destination address register_5	DMA1DAR_5	R/W	H'FE00 8084	32
DMA1 transfer count register_5	DMA1TCR_5	R/W	H'FE00 8088	32
DMA1 channel control register_5	DMA1CHCR_5	R/W	H'FE00 808C	32
DMA1 source address register B_0	DMA1SARB_0	R/W	H'FE00 8120	32
DMA1 destination address register B_0	DMA1DARB_0	R/W	H'FE00 8124	32
DMA1 transfer count register B_0	DMA1TCRB_0	R/W	H'FE00 8128	32
DMA1 channel control register B_0	DMA1CHCRB_0	R/W	H'FE00 812C	32
DMA1 source address register B_1	DMA1SARB_1	R/W	H'FE00 8130	32
DMA1 destination address register B_1	DMA1DARB_1	R/W	H'FE00 8134	32
DMA1 transfer count register B_1	DMA1TCRB_1	R/W	H'FE00 8138	32
DMA1 channel control register B_1	DMA1CHCRB_1	R/W	H'FE00 813C	32
DMA1 source address register B_2	DMA1SARB_2	R/W	H'FE00 8140	32
DMA1 destination address register B_2	DMA1DARB_2	R/W	H'FE00 8144	32
DMA1 transfer count register B_2	DMA1TCRB_2	R/W	H'FE00 8148	32
DMA1 channel control register B_2	DMA1CHCRB_2	R/W	H'FE00 814C	32
DMA1 source address register B_3	DMA1SARB_3	R/W	H'FE00 8150	32
DMA1 destination address register B_3	DMA1DARB_3	R/W	H'FE00 8154	32
DMA1 transfer count register B_3	DMA1TCRB_3	R/W	H'FE00 8158	32
DMA1 channel control register B_3	DMA1CHCRB_3	R/W	H'FE00 815C	32
DMA1 source address register B_4	DMA1SARB_4	R/W	H'FE00 8170	32
DMA1 destination address register B_4	DMA1DARB_4	R/W	H'FE00 8174	32
DMA1 transfer count register B_4	DMA1TCRB_4	R/W	H'FE00 8178	32
DMA1 channel control register B_4	DMA1CHCRB_4	R/W	H'FE00 817C	32
DMA1 source address register B_5	DMA1SARB_5	R/W	H'FE00 8180	32
DMA1 destination address register B_5	DMA1DARB_5	R/W	H'FE00 8184	32
DMA1 transfer count register B_5	DMA1TCRB_5	R/W	H'FE00 8188	32
DMA1 channel control register B_5	DMA1CHCRB_5	R/W	H'FE00 818C	32
DMA1 channel clear register_0	DMA1CHCLR_0	R/W	H'FE00 8220	32
DMA1 channel clear register_1	DMA1CHCLR_1	R/W	H'FE00 8230	32
DMA1 channel clear register_2	DMA1CHCLR_2	R/W	H'FE00 8240	32
DMA1 channel clear register_3	DMA1CHCLR_3	R/W	H'FE00 8250	32
DMA1 channel clear register_4	DMA1CHCLR_4	R/W	H'FE00 8270	32

Register Name	Abbreviation	R/W	Address	Access Size
DMA1 channel clear register_5	DMA1CHCLR_5	R/W	H'FE00 8280	32
DMA1 extended resource selector_0	DMA1RS_0	R/W	H'FE00 9000	16
DMA1 extended resource selector_1	DMA1RS_1	R/W	H'FE00 9004	16
DMA1 extended resource selector_2	DMA1RS_2	R/W	H'FE00 9008	16
DMA2 source address register_0	DMA2SAR_0	R/W	H'FE01 8020	32
DMA2 destination address register_0	DMA2DAR_0	R/W	H'FE01 8024	32
DMA2 transfer count register_0	DMA2TCR_0	R/W	H'FE01 8028	32
DMA2 channel control register_0	DMA2CHCR_0	R/W	H'FE01 802C	32
DMA2 source address register_1	DMA2SAR_1	R/W	H'FE01 8030	32
DMA2 destination address register_1	DMA2DAR_1	R/W	H'FE01 8034	32
DMA2 transfer count register_1	DMA2TCR_1	R/W	H'FE01 8038	32
DMA2 channel control register_1	DMA2CHCR_1	R/W	H'FE01 803C	32
DMA2 source address register_2	DMA2SAR_2	R/W	H'FE01 8040	32
DMA2 destination address register_2	DMA2DAR_2	R/W	H'FE01 8044	32
DMA2 transfer count register_2	DMA2TCR_2	R/W	H'FE01 8048	32
DMA2 channel control register_2	DMA2CHCR_2	R/W	H'FE01 804C	32
DMA2 source address register_3	DMA2SAR_3	R/W	H'FE01 8050	32
DMA2 destination address register_3	DMA2DAR_3	R/W	H'FE01 8054	32
DMA2 transfer count register_3	DMA2TCR_3	R/W	H'FE01 8058	32
DMA2 channel control register_3	DMA2CHCR_3	R/W	H'FE01 805C	32
DMA2 operation register	DMA2OR	R/W	H'FE01 8060	16
DMA2 source address register_4	DMA2SAR_4	R/W	H'FE01 8070	32
DMA2 destination address register_4	DMA2DAR_4	R/W	H'FE01 8074	32
DMA2 transfer count register_4	DMA2TCR_4	R/W	H'FE01 8078	32
DMA2 channel control register_4	DMA2CHCR_4	R/W	H'FE01 807C	32
DMA2 source address register_5	DMA2SAR_5	R/W	H'FE01 8080	32
DMA2 destination address register_5	DMA2DAR_5	R/W	H'FE01 8084	32
DMA2 transfer count register_5	DMA2TCR_5	R/W	H'FE01 8088	32
DMA2 channel control register_5	DMA2CHCR_5	R/W	H'FE01 808C	32
DMA2 source address register B_0	DMA2SARB_0	R/W	H'FE01 8120	32
DMA2 destination address register B_0	DMA2DARB_0	R/W	H'FE01 8124	32
DMA2 transfer count register B_0	DMA2TCRB_0	R/W	H'FE01 8128	32
DMA2 channel control register B_0	DMA2CHCRB_0	R/W	H'FE01 812C	32
DMA2 source address register B_1	DMA2SARB_1	R/W	H'FE01 8130	32
DMA2 destination address register B_1	DMA2DARB_1	R/W	H'FE01 8134	32
DMA2 transfer count register B_1	DMA2TCRB_1	R/W	H'FE01 8138	32
DMA2 channel control register B_1	DMA2CHCRB_1	R/W	H'FE01 813C	32
DMA2 source address register B_2	DMA2SARB_2	R/W	H'FE01 8140	32
DMA2 destination address register B_2	DMA2DARB_2	R/W	H'FE01 8144	32
DMA2 transfer count register B_2	DMA2TCRB_2	R/W	H'FE01 8148	32
DMA2 channel control register B_2	DMA2CHCRB_2	R/W	H'FE01 814C	32
DMA2 source address register B_3	DMA2SARB_3	R/W	H'FE01 8150	32
DMA2 destination address register B_3	DMA2DARB_3	R/W	H'FE01 8154	32
DMA2 transfer count register B_3	DMA2TCRB_3	R/W	H'FE01 8158	32

Register Name	Abbreviation	R/W	Address	Access Size
DMA2 channel control register B_3	DMA2CHCRB_3	R/W	H'FE01 815C	32
DMA2 source address register B_4	DMA2SARB_4	R/W	H'FE01 8170	32
DMA2 destination address register B_4	DMA2DARB_4	R/W	H'FE01 8174	32
DMA2 transfer count register B_4	DMA2TCRB_4	R/W	H'FE01 8178	32
DMA2 channel control register B_4	DMA2CHCRB_4	R/W	H'FE01 817C	32
DMA2 source address register B_5	DMA2SARB_5	R/W	H'FE01 8180	32
DMA2 destination address register B_5	DMA2DARB_5	R/W	H'FE01 8184	32
DMA2 transfer count register B_5	DMA2TCRB_5	R/W	H'FE01 8188	32
DMA2 channel control register B_5	DMA2CHCRB_5	R/W	H'FE01 818C	32
DMA2 channel clear register_0	DMA2CHCLR_0	R/W	H'FE01 8220	32
DMA2 channel clear register_1	DMA2CHCLR_1	R/W	H'FE01 8230	32
DMA2 channel clear register_2	DMA2CHCLR_2	R/W	H'FE01 8240	32
DMA2 channel clear register_3	DMA2CHCLR_3	R/W	H'FE01 8250	32
DMA2 channel clear register_4	DMA2CHCLR_4	R/W	H'FE01 8270	32
DMA2 channel clear register_5	DMA2CHCLR_5	R/W	H'FE01 8280	32
DMA2 extended resource selector_0	DMA2RS_0	R/W	H'FE01 9000	16
DMA2 extended resource selector_1	DMA2RS_1	R/W	H'FE01 9004	16
DMA2 extended resource selector_2	DMA2RS_2	R/W	H'FE01 9008	16
DMA3 source address register_0	DMA3SAR_0	R/W	H'FE02 8020	32
DMA3 destination address register_0	DMA3DAR_0	R/W	H'FE02 8024	32
DMA3 transfer count register_0	DMA3TCR_0	R/W	H'FE02 8028	32
DMA3 channel control register_0	DMA3CHCR_0	R/W	H'FE02 802C	32
DMA3 source address register_1	DMA3SAR_1	R/W	H'FE02 8030	32
DMA3 destination address register_1	DMA3DAR_1	R/W	H'FE02 8034	32
DMA3 transfer count register_1	DMA3TCR_1	R/W	H'FE02 8038	32
DMA3 channel control register_1	DMA3CHCR_1	R/W	H'FE02 803C	32
DMA3 source address register_2	DMA3SAR_2	R/W	H'FE02 8040	32
DMA3 destination address register_2	DMA3DAR_2	R/W	H'FE02 8044	32
DMA3 transfer count register_2	DMA3TCR_2	R/W	H'FE02 8048	32
DMA3 channel control register_2	DMA3CHCR_2	R/W	H'FE02 804C	32
DMA3 source address register_3	DMA3SAR_3	R/W	H'FE02 8050	32
DMA3 destination address register_3	DMA3DAR_3	R/W	H'FE02 8054	32
DMA3 transfer count register_3	DMA3TCR_3	R/W	H'FE02 8058	32
DMA3 channel control register_3	DMA3CHCR_3	R/W	H'FE02 805C	32
DMA3 operation register	DMA3OR	R/W	H'FE02 8060	16
DMA3 source address register_4	DMA3SAR_4	R/W	H'FE02 8070	32
DMA3 destination address register_4	DMA3DAR_4	R/W	H'FE02 8074	32
DMA3 transfer count register_4	DMA3TCR_4	R/W	H'FE02 8078	32
DMA3 channel control register_4	DMA3CHCR_4	R/W	H'FE02 807C	32
DMA3 source address register_5	DMA3SAR_5	R/W	H'FE02 8080	32
DMA3 destination address register_5	DMA3DAR_5	R/W	H'FE02 8084	32
DMA3 transfer count register_5	DMA3TCR_5	R/W	H'FE02 8088	32
DMA3 channel control register_5	DMA3CHCR_5	R/W	H'FE02 808C	32
DMA3 source address register B_0	DMA3SARB_0	R/W	H'FE02 8120	32

Register Name	Abbreviation	R/W	Address	Access Size
DMA3 destination address register B_0	DMA3DARB_0	R/W	H'FE02 8124	32
DMA3 transfer count register B_0	DMA3TCRB_0	R/W	H'FE02 8128	32
DMA3 channel control register B_0	DMA3CHCRB_0	R/W	H'FE02 812C	32
DMA3 source address register B_1	DMA3SARB_1	R/W	H'FE02 8130	32
DMA3 destination address register B_1	DMA3DARB_1	R/W	H'FE02 8134	32
DMA3 transfer count register B_1	DMA3TCRB_1	R/W	H'FE02 8138	32
DMA3 channel control register B_1	DMA3CHCRB_1	R/W	H'FE02 813C	32
DMA3 source address register B_2	DMA3SARB_2	R/W	H'FE02 8140	32
DMA3 destination address register B_2	DMA3DARB_2	R/W	H'FE02 8144	32
DMA3 transfer count register B_2	DMA3TCRB_2	R/W	H'FE02 8148	32
DMA3 channel control register B_2	DMA3CHCRB_2	R/W	H'FE02 814C	32
DMA3 source address register B_3	DMA3SARB_3	R/W	H'FE02 8150	32
DMA3 destination address register B_3	DMA3DARB_3	R/W	H'FE02 8154	32
DMA3 transfer count register B_3	DMA3TCRB_3	R/W	H'FE02 8158	32
DMA3 channel control register B_3	DMA3CHCRB_3	R/W	H'FE02 815C	32
DMA3 source address register B_4	DMA3SARB_4	R/W	H'FE02 8170	32
DMA3 destination address register B_4	DMA3DARB_4	R/W	H'FE02 8174	32
DMA3 transfer count register B_4	DMA3TCRB_4	R/W	H'FE02 8178	32
DMA3 channel control register B_4	DMA3CHCRB_4	R/W	H'FE02 817C	32
DMA3 source address register B_5	DMA3SARB_5	R/W	H'FE02 8180	32
DMA3 destination address register B_5	DMA3DARB_5	R/W	H'FE02 8184	32
DMA3 transfer count register B_5	DMA3TCRB_5	R/W	H'FE02 8188	32
DMA3 channel control register B_5	DMA3CHCRB_5	R/W	H'FE02 818C	32
DMA3 channel clear register_0	DMA3CHCLR_0	R/W	H'FE02 8220	32
DMA3 channel clear register_1	DMA3CHCLR_1	R/W	H'FE02 8230	32
DMA3 channel clear register_2	DMA3CHCLR_2	R/W	H'FE02 8240	32
DMA3 channel clear register_3	DMA3CHCLR_3	R/W	H'FE02 8250	32
DMA3 channel clear register_4	DMA3CHCLR_4	R/W	H'FE02 8270	32
DMA3 channel clear register_5	DMA3CHCLR_5	R/W	H'FE02 8280	32
DMA3 extended resource selector_0	DMA3RS_0	R/W	H'FE02 9000	16
DMA3 extended resource selector_1	DMA3RS_1	R/W	H'FE02 9004	16
DMA3 extended resource selector_2	DMA3RS_2	R/W	H'FE02 9008	16

G.8 Register Configuration of RTDMAC

Register Name	Abbreviation	R/W	Address	Access Size
RTDMAC source address register_0	RDM1SAR_0	R/W	H'FFC1 8020	32
RTDMAC destination address register_0	RDM1DAR_0	R/W	H'FFC1 8024	32
RTDMAC transfer count register_0	RDM1TCR_0	R/W	H'FFC1 8028	32
RTDMAC channel control register_0	RDM1CHCR_0	R/W	H'FFC1 802C	32
RTDMAC source address register_1	RDM1SAR_1	R/W	H'FFC1 8030	32
RTDMAC destination address register_1	RDM1DAR_1	R/W	H'FFC1 8034	32

Register Name	Abbreviation	R/W	Address	Access Size
RTDMAC transfer count register_1	RDM1TCR_1	R/W	H'FFC1 8038	32
RTDMAC channel control register_1	RDM1CHCR_1	R/W	H'FFC1 803C	32
RTDMAC source address register_2	RDM1SAR_2	R/W	H'FFC1 8040	32
RTDMAC destination address register_2	RDM1DAR_2	R/W	H'FFC1 8044	32
RTDMAC transfer count register_2	RDM1TCR_2	R/W	H'FFC1 8048	32
RTDMAC channel control register_2	RDM1CHCR_2	R/W	H'FFC1 804C	32
RTDMAC source address register_3	RDM1SAR_3	R/W	H'FFC1 8050	32
RTDMAC destination address register_3	RDM1DAR_3	R/W	H'FFC1 8054	32
RTDMAC transfer count register_3	RDM1TCR_3	R/W	H'FFC1 8058	32
RTDMAC channel control register_3	RDM1CHCR_3	R/W	H'FFC1 805C	32
RTDMAC operation register	RDM1OR	R/W	H'FFC1 8060	16
RTDMAC source address register_4	RDM1SAR_4	R/W	H'FFC1 8070	32
RTDMAC destination address register_4	RDM1DAR_4	R/W	H'FFC1 8074	32
RTDMAC transfer count register_4	RDM1TCR_4	R/W	H'FFC1 8078	32
RTDMAC channel control register_4	RDM1CHCR_4	R/W	H'FFC1 807C	32
RTDMAC source address register_5	RDM1SAR_5	R/W	H'FFC1 8080	32
RTDMAC destination address register_5	RDM1DAR_5	R/W	H'FFC1 8084	32
RTDMAC transfer count register_5	RDM1TCR_5	R/W	H'FFC1 8088	32
RTDMAC channel control register_5	RDM1CHCR_5	R/W	H'FFC1 808C	32
RTDMAC source address register B_0	RDM1SARB_0	R/W	H'FFC1 8120	32
RTDMAC destination address register B_0	RDM1DARB_0	R/W	H'FFC1 8124	32
RTDMAC transfer count register B_0	RDM1TCRB_0	R/W	H'FFC1 8128	32
RTDMAC channel control register B_0	RDM1CHCRB_0	R/W	H'FFC1 812C	32
RTDMAC source address register B_1	RDM1SARB_1	R/W	H'FFC1 8130	32
RTDMAC destination address register B_1	RDM1DARB_1	R/W	H'FFC1 8134	32
RTDMAC transfer count register B_1	RDM1TCRB_1	R/W	H'FFC1 8138	32
RTDMAC channel control register B_1	RDM1CHCRB_1	R/W	H'FFC1 813C	32
RTDMAC source address register B_2	RDM1SARB_2	R/W	H'FFC1 8140	32
RTDMAC destination address register B_2	RDM1DARB_2	R/W	H'FFC1 8144	32
RTDMAC transfer count register B_2	RDM1TCRB_2	R/W	H'FFC1 8148	32
RTDMAC channel control register B_2	RDM1CHCRB_2	R/W	H'FFC1 814C	32
RTDMAC source address register B_3	RDM1SARB_3	R/W	H'FFC1 8150	32
RTDMAC destination address register B_3	RDM1DARB_3	R/W	H'FFC1 8154	32
RTDMAC transfer count register B_3	RDM1TCRB_3	R/W	H'FFC1 8158	32
RTDMAC channel control register B_3	RDM1CHCRB_3	R/W	H'FFC1 815C	32
RTDMAC source address register B_4	RDM1SARB_4	R/W	H'FFC1 8170	32
RTDMAC destination address register B_4	RDM1DARB_4	R/W	H'FFC1 8174	32
RTDMAC transfer count register B_4	RDM1TCRB_4	R/W	H'FFC1 8178	32
RTDMAC channel control register B_4	RDM1CHCRB_4	R/W	H'FFC1 817C	32
RTDMAC source address register B_5	RDM1SARB_5	R/W	H'FFC1 8180	32
RTDMAC destination address register B_5	RDM1DARB_5	R/W	H'FFC1 8184	32
RTDMAC transfer count register B_5	RDM1TCRB_5	R/W	H'FFC1 8188	32
RTDMAC channel control register B_5	RDM1CHCRB_5	R/W	H'FFC1 818C	32
RTDMAC channel clear register_0	RDM1CHCLR_0	R/W	H'FFC1 8220	32

Register Name	Abbreviation	R/W	Address	Access Size
RTDMAC channel clear register_1	RDM1CHCLR_1	R/W	H'FFC1 8230	32
RTDMAC channel clear register_2	RDM1CHCLR_2	R/W	H'FFC1 8240	32
RTDMAC channel clear register_3	RDM1CHCLR_3	R/W	H'FFC1 8250	32
RTDMAC channel clear register_4	RDM1CHCLR_4	R/W	H'FFC1 8270	32
RTDMAC channel clear register_5	RDM1CHCLR_5	R/W	H'FFC1 8280	32
RTDMAC extended resource selector_0	RDM1RS_0	R/W	H'FFC1 9000	16
RTDMAC extended resource selector_1	RDM1RS_1	R/W	H'FFC1 9004	16
RTDMAC extended resource selector_2	RDM1RS_2	R/W	H'FFC1 9008	16
RTDMAC2 transfer count register_0	RDM2TCR_0	R/W	H'FFC2 8028	32
RTDMAC2 channel control register_0	RDM2CHCR_0	R/W	H'FFC2 802C	32
RTDMAC2 source address register_1	RDM2SAR_1	R/W	H'FFC2 8030	32
RTDMAC2 destination address register_1	RDM2DAR_1	R/W	H'FFC2 8034	32
RTDMAC2 transfer count register_1	RDM2TCR_1	R/W	H'FFC2 8038	32
RTDMAC2 channel control register_1	RDM2CHCR_1	R/W	H'FFC2 803C	32
RTDMAC2 source address register_2	RDM2SAR_2	R/W	H'FFC2 8040	32
RTDMAC2 destination address register_2	RDM2DAR_2	R/W	H'FFC2 8044	32
RTDMAC2 transfer count register_2	RDM2TCR_2	R/W	H'FFC2 8048	32
RTDMAC2 channel control register_2	RDM2CHCR_2	R/W	H'FFC2 804C	32
RTDMAC2 source address register_3	RDM2SAR_3	R/W	H'FFC2 8050	32
RTDMAC2 destination address register_3	RDM2DAR_3	R/W	H'FFC2 8054	32
RTDMAC2 transfer count register_3	RDM2TCR_3	R/W	H'FFC2 8058	32
RTDMAC2 channel control register_3	RDM2CHCR_3	R/W	H'FFC2 805C	32
RTDMAC2 operation register	RDM2OR	R/W	H'FFC2 8060	16
RTDMAC2 source address register_4	RDM2SAR_4	R/W	H'FFC2 8070	32
RTDMAC2 destination address register_4	RDM2DAR_4	R/W	H'FFC2 8074	32
RTDMAC2 transfer count register_4	RDM2TCR_4	R/W	H'FFC2 8078	32
RTDMAC2 channel control register_4	RDM2CHCR_4	R/W	H'FFC2 807C	32
RTDMAC2 source address register_5	RDM2SAR_5	R/W	H'FFC2 8080	32
RTDMAC2 destination address register_5	RDM2DAR_5	R/W	H'FFC2 8084	32
RTDMAC2 transfer count register_5	RDM2TCR_5	R/W	H'FFC2 8088	32
RTDMAC2 channel control register_5	RDM2CHCR_5	R/W	H'FFC2 808C	32
RTDMAC2 source address register B_0	RDM2SARB_0	R/W	H'FFC2 8120	32
RTDMAC2 destination address register B_0	RDM2DARB_0	R/W	H'FFC2 8124	32
RTDMAC2 transfer count register B_0	RDM2TCRB_0	R/W	H'FFC2 8128	32
RTDMAC2 channel control register B_0	RDM2CHCRB_0	R/W	H'FFC2 812C	32
RTDMAC2 source address register B_1	RDM2SARB_1	R/W	H'FFC2 8130	32
RTDMAC2 destination address register B_1	RDM2DARB_1	R/W	H'FFC2 8134	32
RTDMAC2 transfer count register B_1	RDM2TCRB_1	R/W	H'FFC2 8138	32
RTDMAC2 channel control register B_1	RDM2CHCRB_1	R/W	H'FFC2 813C	32
RTDMAC2 source address register B_2	RDM2SARB_2	R/W	H'FFC2 8140	32
RTDMAC2 destination address register B_2	RDM2DARB_2	R/W	H'FFC2 8144	32
RTDMAC2 transfer count register B_2	RDM2TCRB_2	R/W	H'FFC2 8148	32
RTDMAC2 channel control register B_2	RDM2CHCRB_2	R/W	H'FFC2 814C	32
RTDMAC2 source address register B_3	RDM2SARB_3	R/W	H'FFC2 8150	32

Register Name	Abbreviation	R/W	Address	Access Size
RTDMAC2 destination address register B_3	RDM2DARB_3	R/W	H'FFC2 8154	32
RTDMAC2 transfer count register B_3	RDM2TCRB_3	R/W	H'FFC2 8158	32
RTDMAC2 channel control register B_3	RDM2CHCRB_3	R/W	H'FFC2 815C	32
RTDMAC2 source address register B_4	RDM2SARB_4	R/W	H'FFC2 8170	32
RTDMAC2 destination address register B_4	RDM2DARB_4	R/W	H'FFC2 8174	32
RTDMAC2 transfer count register B_4	RDM2TCRB_4	R/W	H'FFC2 8178	32
RTDMAC2 channel control register B_4	RDM2CHCRB_4	R/W	H'FFC2 817C	32
RTDMAC2 source address register B_5	RDM2SARB_5	R/W	H'FFC2 8180	32
RTDMAC2 destination address register B_5	RDM2DARB_5	R/W	H'FFC2 8184	32
RTDMAC2 transfer count register B_5	RDM2TCRB_5	R/W	H'FFC2 8188	32
RTDMAC2 channel control register B_5	RDM2CHCRB_5	R/W	H'FFC2 818C	32
RTDMAC2 channel clear register_0	RDM2CHCLR_0	R/W	H'FFC2 8220	32
RTDMAC2 channel clear register_1	RDM2CHCLR_1	R/W	H'FFC2 8230	32
RTDMAC2 channel clear register_2	RDM2CHCLR_2	R/W	H'FFC2 8240	32
RTDMAC2 channel clear register_3	RDM2CHCLR_3	R/W	H'FFC2 8250	32
RTDMAC2 channel clear register_4	RDM2CHCLR_4	R/W	H'FFC2 8270	32
RTDMAC2 channel clear register_5	RDM2CHCLR_5	R/W	H'FFC2 8280	32
RTDMAC2 extended resource selector_0	RDM2RS_0	R/W	H'FFC2 9000	16
RTDMAC2 extended resource selector_1	RDM2RS_1	R/W	H'FFC2 9004	16
RTDMAC2 extended resource selector_2	RDM2RS_2	R/W	H'FFC2 9008	16

G.9 Register Configuration of DREQPAK

Register Name	Abbreviation	R/W	Initial Value	Address	Access Size (Bits)	Target DMA Request (Extended Link Selector MID+RID)
SCIFB pack target address register 0	SCBPKTADR0	R/W	H'0000	H'E6C38000	16	SCIFB transmission H'3D
SCIFB pack total size register 0L	SCBPKTSIZER0L	R/W	H'0000	H'E6C38002	16	
SCIFB pack total size register 0H	SCBPKTSIZER0H	R/W	H'0000	H'E6C38004	16	
SCIFB pack control register 0	SCBPKCTLR0	R/W	H'0000	H'E6C38006	16	
SCIFB pack status register 0L	SCBPKSTATR0L	R/W	H'0000	H'E6C38008	16	
SCIFB pack status register 0H	SCBPKSTATR0H	R/W	H'0000	H'E6C3800A	16	
SCIFB pack data register 0	SCBPKDATAR0	R/W	Undefined	H'E6C39000	16	
SCIFB pack target address register 1	SCBPKTADR1	R/W	H'0000	H'E6C3800C	16	SCIFB reception

Register Name	Abbreviation	R/W	Initial Value	Address	Access Size (Bits)	Target DMA Request (Extended Link Selector MID+RID)
SCIFB pack total size register 1L	SCBPKTSIZER1	R/W	H'0000	H'E6C3800E	16	H'3E
SCIFB pack total size register 1H	SCBPKTSIZER1	R/W	H'0000	H'E6C38010	16	
SCIFB pack control register 1	SCBPKCTLR1	R/W	H'0000	H'E6C38012	16	
SCIFB pack status register 1L	SCBPKSTATR1	R/W	H'0000	H'E6C38014	16	
SCIFB pack status register 1H	SCBPKSTATR1	R/W	H'0000	H'E6C38016	16	
SCIFB pack data register 1	SCBPKDATAR1	R/W	Undefined	H'E6C3A000	16	
SCIFA0 pack target address register 0	SC0PKTADR0	R/W	H'0000	H'E6C48000	16	SCIFA0 transmission
SCIFA0 pack total size register 0L	SC0PKTSIZER0L	R/W	H'0000	H'E6C48002	16	H'21
SCIFA0 pack total size register 0H	SC0PKTSIZER0H	R/W	H'0000	H'E6C48004	16	
SCIFA0 pack control register 0	SC0PKCTLR0	R/W	H'0000	H'E6C48006	16	
SCIFA0 pack status register 0L	SC0PKSTATR0L	R/W	H'0000	H'E6C48008	16	
SCIFA0 pack status register 0H	SC0PKSTATR0H	R/W	H'0000	H'E6C4800A	16	
SCIFA0 pack data register 0	SC0PKDATAR0	R/W	Undefined	H'E6C49000	16	
SCIFA0 pack target address register 1	SC0PKTADR1	R/W	H'0000	H'E6C4800C	16	SCIFA0 reception
SCIFA0 pack total size register 1L	SC0PKTSIZER1	R/W	H'0000	H'E6C4800E	16	H'22
SCIFA0 pack total size register 1H	SC0PKTSIZER1	R/W	H'0000	H'E6C48010	16	
SCIFA0 pack control register 1	SC0PKCTLR1	R/W	H'0000	H'E6C48012	16	
SCIFA0 pack status register 1L	SC0PKSTATR1	R/W	H'0000	H'E6C48014	16	
SCIFA0 pack status register 1H	SC0PKSTATR1	R/W	H'0000	H'E6C48016	16	
SCIFA0 pack data register 1	SC0PKDATAR1	R/W	Undefined	H'E6C4A000	16	

Register Name	Abbreviation	R/W	Initial Value	Address	Access Size (Bits)	Target DMA Request (Extended Link Selector MID+RID)
SCIFA1 pack target address register 0	SC1PKTADR0	R/W	H'0000	H'E6C58000	16	SCIFA1 transmission H'25
SCIFA1 pack total size register 0L	SC1PKTSIZER0L	R/W	H'0000	H'E6C58002	16	
SCIFA1 pack total size register 0H	SC1PKTSIZER0H	R/W	H'0000	H'E6C58004	16	
SCIFA1 pack control register 0	SC1PKCTLR0	R/W	H'0000	H'E6C58006	16	
SCIFA1 pack status register 0L	SC1PKSTATR0L	R/W	H'0000	H'E6C58008	16	SCIFA1 transmission H'25
SCIFA1 pack status register 0H	SC1PKSTATR0H	R/W	H'0000	H'E6C5800A	16	
SCIFA1 pack data register 0	SC1PKDATAR0	R/W	Undefined	H'E6C59000	16	
SCIFA1 pack target address register 1	SC1PKTADR1	R/W	H'0000	H'E6C5800C	16	
SCIFA1 pack total size register 1L	SC1PKTSIZER1	R/W	H'0000	H'E6C5800E	16	SCIFA1 reception H'26
SCIFA1 pack total size register 1H	SC1PKTSIZER1	R/W	H'0000	H'E6C58010	16	
SCIFA1 pack control register 1	SC1PKCTLR1	R/W	H'0000	H'E6C58012	16	
SCIFA1 pack status register 1L	SC1PKSTATR1	R/W	H'0000	H'E6C58014	16	
SCIFA1 pack status register 1H	SC1PKSTATR1	R/W	H'0000	H'E6C58016	16	
SCIFA1 pack data register 1	SC1PKDATAR1	R/W	Undefined	H'E6C5A000	16	
SCIFA2 pack target address register 0	SC2PKTADR0	R/W	H'0000	H'E6C68000	16	SCIFA2 transmission H'29
SCIFA2 pack total size register 0L	SC2PKTSIZER0L	R/W	H'0000	H'E6C68002	16	
SCIFA2 pack total size register 0H	SC2PKTSIZER0H	R/W	H'0000	H'E6C68004	16	
SCIFA2 pack control register 0	SC2PKCTLR0	R/W	H'0000	H'E6C68006	16	
SCIFA2 pack status register 0L	SC2PKSTATR0L	R/W	H'0000	H'E6C68008	16	
SCIFA2 pack status register 0H	SC2PKSTATR0H	R/W	H'0000	H'E6C6800A	16	

Register Name	Abbreviation	R/W	Initial Value	Address	Access Size (Bits)	Target DMA Request (Extended Link Selector MID+RID)
SCIFA2 pack data register 0	SC2PKDATAR0	R/W	Undefined	H'E6C69000	16	
SCIFA2 pack target address register 1	SC2PKTADR1	R/W	H'0000	H'E6C6800C	16	SCIFA2 reception
SCIFA2 pack total size register 1L	SC2PKTSIZER1	R/W	H'0000	H'E6C6800E	16	H'2A
SCIFA2 pack total size register 1H	SC2PKTSIZER1	R/W	H'0000	H'E6C68010	16	
SCIFA2 pack control register 1	SC2PKCTLR1	R/W	H'0000	H'E6C68012	16	
SCIFA2 pack status register 1L	SC2PKSTATR1	R/W	H'0000	H'E6C68014	16	
SCIFA2 pack status register 1H	SC2PKSTATR1	R/W	H'0000	H'E6C68016	16	
SCIFA2 pack data register 1	SC2PKDATAR1	R/W	Undefined	H'E6C6A000	16	
SCIFA3 pack target address register 0	SC3PKTADR0	R/W	H'0000	H'E6C78000	16	SCIFA3 transmission
SCIFA3 pack total size register 0L	SC3PKTSIZER0L	R/W	H'0000	H'E6C78002	16	H'2D
SCIFA3 pack total size register 0H	SC3PKTSIZER0H	R/W	H'0000	H'E6C78004	16	
SCIFA3 pack control register 0	SC3PKCTLR0	R/W	H'0000	H'E6C78006	16	
SCIFA3 pack status register 0L	SC3PKSTATR0L	R/W	H'0000	H'E6C78008	16	
SCIFA3 pack status register 0H	SC3PKSTATR0H	R/W	H'0000	H'E6C7800A	16	
SCIFA3 pack data register 0	SC3PKDATAR0	R/W	Undefined	H'E6C79000	16	
SCIFA3 pack target address register 1	SC3PKTADR1	R/W	H'0000	H'E6C7800C	16	SCIFA3 reception
SCIFA3 pack total size register 1L	SC3PKTSIZER1	R/W	H'0000	H'E6C7800E	16	H'2E
SCIFA3 pack total size register 1H	SC3PKTSIZER1	R/W	H'0000	H'E6C78010	16	
SCIFA3 pack control register 1	SC3PKCTLR1	R/W	H'0000	H'E6C78012	16	
SCIFA3 pack status register 1L	SC3PKSTATR1	R/W	H'0000	H'E6C78014	16	

Register Name	Abbreviation	R/W	Initial Value	Address	Access Size (Bits)	Target DMA Request (Extended Link Selector MID+RID)
SCIFA3 pack status register 1H	SC3PKSTATR1	R/W	H'0000	H'E6C78016	16	
SCIFA3 pack data register 1	SC3PKDATAR1	R/W	Undefined	H'E6C7A000	16	
SCIFA4 pack target address register 0	SC4PKTADR0	R/W	H'0000	H'E6C88000	16	SCIFA4 transmission
SCIFA4 pack total size register 0L	SC4PKTSIZER0L	R/W	H'0000	H'E6C88002	16	H'39
SCIFA4 pack total size register 0H	SC4PKTSIZER0H	R/W	H'0000	H'E6C88004	16	
SCIFA4 pack control register 0	SC4PKCTLR0	R/W	H'0000	H'E6C88006	16	
SCIFA4 pack status register 0L	SC4PKSTATR0L	R/W	H'0000	H'E6C88008	16	
SCIFA4 pack status register 0H	SC4PKSTATR0H	R/W	H'0000	H'E6C8800A	16	
SCIFA4 pack data register 0	SC4PKDATAR0	R/W	Undefined	H'E6C89000	16	
SCIFA4 pack target address register 1	SC4PKTADR1	R/W	H'0000	H'E6C8800C	16	SCIFA4 reception
SCIFA4 pack total size register 1L	SC4PKTSIZER1	R/W	H'0000	H'E6C8800E	16	H'3A
SCIFA4 pack total size register 1H	SC4PKTSIZER1	R/W	H'0000	H'E6C88010	16	
SCIFA4 pack control register 1	SC4PKCTLR1	R/W	H'0000	H'E6C88012	16	
SCIFA4 pack status register 1L	SC4PKSTATR1	R/W	H'0000	H'E6C88014	16	
SCIFA4 pack status register 1H	SC4PKSTATR1	R/W	H'0000	H'E6C88016	16	
SCIFA4 pack data register 1	SC4PKDATAR1	R/W	Undefined	H'E6C8A000	16	
SCIFA5 pack target address register 0	SC5PKTADR0	R/W	H'0000	H'E6CB8000	16	SCIFA5 transmission
SCIFA5 pack total size register 0L	SC5PKTSIZER0L	R/W	H'0000	H'E6CB8002	16	H'35
SCIFA5 pack total size register 0H	SC5PKTSIZER0H	R/W	H'0000	H'E6CB8004	16	
SCIFA5 pack control register 0	SC5PKCTLR0	R/W	H'0000	H'E6CB8006	16	

Register Name	Abbreviation	R/W	Initial Value	Address	Access Size (Bits)	Target DMA Request (Extended Link Selector MID+RID)
SCIFA5 pack status register 0L	SC5PKSTATR0L	R/W	H'0000	H'E6CB8008	16	
SCIFA5 pack status register 0H	SC5PKSTATR0H	R/W	H'0000	H'E6CB800A	16	
SCIFA5 pack data register 0	SC5PKDATAR0	R/W	Undefined	H'E6CB9000	16	
SCIFA5 pack target address register 1	SC5PKTADR1	R/W	H'0000	H'E6CB800C	16	SCIFA5 reception
SCIFA5 pack total size register 1L	SC5PKTSIZER1	R/W	H'0000	H'E6CB800E	16	H'36
SCIFA5 pack total size register 1H	SC5PKTSIZER1	R/W	H'0000	H'E6CB8010	16	
SCIFA5 pack control register 1	SC5PKCTLR1	R/W	H'0000	H'E6CB8012	16	
SCIFA5 pack status register 1L	SC5PKSTATR1	R/W	H'0000	H'E6CB8014	16	
SCIFA5 pack status register 1H	SC5PKSTATR1	R/W	H'0000	H'E6CB8016	16	
SCIFA5 pack data register 1	SC5PKDATAR1	R/W	Undefined	H'E6CBA000	16	
BBIF1 pack target address register 0	BB1PKTADR0	R/W	H'0000 0000	H'E6C98000	32	BBIF1 transmission
BBIF1 pack total size register 0	BB1PKTSIZER0	R/W	H'0000 0000	H'E6C98004	32	H'59
BBIF1 pack control register 0	BB1PKCTLR0	R/W	H'0000 0000	H'E6C98008	32	
BBIF1 pack status register 0	BB1PKSTATR0	R/W	H'0000 0000	H'E6C9800C	32	
BBIF1 pack data register 0	BB1PKDATAR0	R/W	Undefined	H'E6C99000	32	
BBIF1 pack target address register 1	BB1PKTADR1	R/W	H'0000 0000	H'E6C98010	32	BBIF1 reception
BBIF1 pack total size register 1	BB1PKTSIZER1	R/W	H'0000 0000	H'E6C98014	32	H'5A
BBIF1 pack control register 1	BB1PKCTLR1	R/W	H'0000 0000	H'E6C98018	32	
BBIF1 pack status register 1	BB1PKSTATR1	R/W	H'0000 0000	H'E6C9801C	32	
BBIF1 pack data register 1	BB1PKDATAR1	R/W	Undefined	H'E6C9A000	32	
BBIF2 pack target address register 0	BB2PKTADR0	R/W	H'0000 0000	H'E6CA8000 H'FFFA8000	32	BBIF2 transmission

Register Name	Abbreviation	R/W	Initial Value	Address	Access Size (Bits)	Target DMA Request (Extended Link Selector MID+RID)
BBIF2 pack total size register 0	BB2PKTSIZER0	R/W	H'0000 0000	H'E6CA8004 H'FFFA8004	32	H'5D
BBIF2 pack control register 0	BB2PKCTLR0	R/W	H'0000 0000	H'E6CA8008 H'FFFA8008	32	
BBIF2 pack status register 0	BB2PKSTATR0	R/W	H'0000 0000	H'E6CA800C H'FFFA800C	32	
BBIF2 pack data register 0	BB2PKDATAR0	R/W	Undefined	H'E6CA9000 H'FFFA9000	32	
BBIF2 pack target address register 1	BB2PKTADR1	R/W	H'0000 0000	H'E6CA8010 H'FFFA8010	32	BBIF2 reception
BBIF2 pack total size register 1	BB2PKTSIZER1	R/W	H'0000 0000	H'E6CA8014 H'FFFA8014	32	H'5E
BBIF2 pack control register 1	BB2PKCTLR1	R/W	H'0000 0000	H'E6CA8018 H'FFFA8018	32	
BBIF2 pack status register 1	BB2PKSTATR1	R/W	H'0000 0000	H'E6CA801C H'FFFA801C	32	
BBIF2 pack data register 1	BB2PKDATAR1	R/W	Undefined	H'E6CAA000 H'FFFAA000	32	
MSIOF0 pack target address register 0	MS0PKTADR0	R/W	H'0000 0000	H'FFF18000	32	MSIOF0 transmission
MSIOF0 pack total size register 0	MS0PKTSIZER0	R/W	H'0000 0000	H'FFF18004	32	H'51
MSIOF0 pack control register 0	MS0PKCTLR0	R/W	H'0000 0000	H'FFF18008	32	
MSIOF0 pack status register 0	MS0PKSTATR0	R/W	H'0000 0000	H'FFF1800C	32	
MSIOF0 pack data register 0	MS0PKDATAR0	R/W	Undefined	H'FFF19000	32	
MSIOF0 pack target address register 1	MS0PKTADR1	R/W	H'0000 0000	H'FFF18010	32	MSIOF0 reception
MSIOF0 pack total size register 1	MS0PKTSIZER1	R/W	H'0000 0000	H'FFF18014	32	H'52
MSIOF0 pack control register 1	MS0PKCTLR1	R/W	H'0000 0000	H'FFF18018	32	
MSIOF0 pack status register 1	MS0PKSTATR1	R/W	H'0000 0000	H'FFF1801C	32	
MSIOF0 pack data register 1	MS0PKDATAR1	R/W	Undefined	H'FFF1A000	32	

Register Name	Abbreviation	R/W	Initial Value	Address	Access Size (Bits)	Target DMA Request (Extended Link Selector MID+RID)
MSIOF1 pack target address register 0	MS1PKTADR0	R/W	H'0000 0000	H'E6E18000	32	MSIOF1 transmission
MSIOF1 pack total size register 0	MS1PKTSIZER0	R/W	H'0000 0000	H'E6E18004	32	H'55
MSIOF1 pack control register 0	MS1PKCTLR0	R/W	H'0000 0000	H'E6E18008	32	
MSIOF1 pack status register 0	MS1PKSTATR0	R/W	H'0000 0000	H'E6E1800C	32	
MSIOF1 pack data register 0	MS1PKDATAR0	R/W	H'0000 0000	H'E6E19000	32	
MSIOF1 pack target address register 1	MS1PKTADR1	R/W	H'0000 0000	H'E6E18010	32	MSIOF1 reception
MSIOF1 pack total size register 1	MS1PKTSIZER1	R/W	H'0000 0000	H'E6E18014	32	H'56
MSIOF1 pack control register 1	MS1PKCTLR1	R/W	H'0000 0000	H'E6E18018	32	
MSIOF1 pack status register 1	MS1PKSTATR1	R/W	H'0000 0000	H'E6E1801C	32	
MSIOF1 pack data register 1	MS1PKDATAR1	R/W	Undefined	H'E6E1A000	32	
MSIOF2 pack target address register 0	MS2PKTADR0	R/W	H'0000 0000	H'E6E08000	32	MSIOF2 transmission
MSIOF2 pack total size register 0	MS2PKTSIZER0	R/W	H'0000 0000	H'E6E08004	32	H'41
MSIOF2 pack control register 0	MS2PKCTLR0	R/W	H'0000 0000	H'E6E08008	32	
MSIOF2 pack status register 0	MS2PKSTATR0	R/W	H'0000 0000	H'E6E0800C	32	
MSIOF2 pack data register 0	MS2PKDATAR0	R/W	H'0000 0000	H'E6E09000	32	
MSIOF2 pack target address register 1	MS2PKTADR1	R/W	H'0000 0000	H'E6E08010	32	MSIOF2 reception
MSIOF2 pack total size register 1	MS2PKTSIZER1	R/W	H'0000 0000	H'E6E08014	32	H'42
MSIOF2 pack control register 1	MS2PKCTLR1	R/W	H'0000 0000	H'E6E08018	32	
MSIOF2 pack status register 1	MS2PKSTATR1	R/W	H'0000 0000	H'E6E0801C	32	

Register Name	Abbreviation	R/W	Initial Value	Address	Access Size (Bits)	Target DMA Request (Extended Link Selector MID+RID)
MSIOF2 pack data register 1	MS2PKDATAR1	R/W	Undefined	H'E6E0A000	32	
HSI pack target address register 0	HSIPKTADR0	R/W	H'0000 0000	H'E6A48000	32	HSI transmission H'09
HSI pack total size register 0	HSIPKTSIZER0	R/W	H'0000 0000	H'E6A48004	32	
HSI pack control register 0	HSIPKCTLR0	R/W	H'0000 0000	H'E6A48008	32	
HSI pack status register 0	HSIPKSTATR0	R/W	H'0000 0000	H'E6A4800C	32	
HSI pack data register 0	HSIPKDATAR0	R/W	Undefined	H'E6A49000	32	
HSI pack target address register 1	HSIPKTADR1	R/W	H'0000 0000	H'E6A48010	32	HSI reception H'0A
HSI pack total size register 1	HSIPKTSIZER1	R/W	H'0000 0000	H'E6A48014	32	
HSI pack control register 1	HSIPKCTLR1	R/W	H'0000 0000	H'E6A48018	32	
HSI pack status register 1	HSIPKSTATR1	R/W	H'0000 0000	H'E6A4801C	32	
HSI pack data register 1	HSIPKDATAR1	R/W	Undefined	H'E6A49010	32	
HSI pack target address register 2	HSIPKTADR2	R/W	H'0000 0000	H'E6A48020	32	HSI transmission H'0D
HSI pack total size register 2	HSIPKTSIZER2	R/W	H'0000 0000	H'E6A48024	32	
HSI pack control register 2	HSIPKCTLR2	R/W	H'0000 0000	H'E6A48028	32	
HSI pack status register 2	HSIPKSTATR2	R/W	H'0000 0000	H'E6A4802C	32	
HSI pack data register 2	HSIPKDATAR2	R/W	Undefined	H'E6A49020	32	
HSI pack target address register 3	HSIPKTADR3	R/W	H'0000 0000	H'E6A48030	32	HSI reception H'0E
HSI pack total size register 3	HSIPKTSIZER3	R/W	H'0000 0000	H'E6A48034	32	
HSI pack control register 3	HSIPKCTLR3	R/W	H'0000 0000	H'E6A48038	32	
HSI pack status register 3	HSIPKSTATR3	R/W	H'0000 0000	H'E6A4803C	32	
HSI pack data register 3	HSIPKDATAR3	R/W	Undefined	H'E6A49030	32	

Register Name	Abbreviation	R/W	Initial Value	Address	Access Size (Bits)	Target DMA Request (Extended Link Selector MID+RID)
HSI pack target address register 4	HSIPKTADR4	R/W	H'0000 0000	H'E6A48040	32	HSI transmission H'11
HSI pack total size register 4	HSIPKTSIZER4	R/W	H'0000 0000	H'E6A48044	32	
HSI pack control register 4	HSIPKCTLR4	R/W	H'0000 0000	H'E6A48048	32	
HSI pack status register 4	HSIPKSTATR4	R/W	H'0000 0000	H'E6A4804C	32	
HSI pack data register 4	HSIPKDATAR4	R/W	Undefined	H'E6A49040	32	
HSI pack target address register 5	HSIPKTADR5	R/W	H'0000 0000	H'E6A48050	32	HSI reception H'12
HSI pack total size register 5	HSIPKTSIZER5	R/W	H'0000 0000	H'E6A48054	32	
HSI pack control register 5	HSIPKCTLR5	R/W	H'0000 0000	H'E6A48058	32	
HSI pack status register 5	HSIPKSTATR5	R/W	H'0000 0000	H'E6A4805C	32	
HSI pack data register 5	HSIPKDATAR5	R/W	Undefined	H'E6A49050	32	
HSI pack target address register 6	HSIPKTADR6	R/W	H'0000 0000	H'E6A48060	32	HSI transmission H'15
HSI pack total size register 6	HSIPKTSIZER6	R/W	H'0000 0000	H'E6A48064	32	
HSI pack control register 6	HSIPKCTLR6	R/W	H'0000 0000	H'E6A48068	32	
HSI pack status register 6	HSIPKSTATR6	R/W	H'0000 0000	H'E6A4806C	32	
HSI pack data register 6	HSIPKDATAR6	R/W	Undefined	H'E6A49060	32	
HSI pack target address register 7	HSIPKTADR7	R/W	H'0000 0000	H'E6A48070	32	HSI reception H'16
HSI pack total size register 7	HSIPKTSIZER7	R/W	H'0000 0000	H'E6A48074	32	
HSI pack control register 7	HSIPKCTLR7	R/W	H'0000 0000	H'E6A48078	32	
HSI pack status register 7	HSIPKSTATR7	R/W	H'0000 0000	H'E6A4807C	32	
HSI pack data register 7	HSIPKDATAR7	R/W	Undefined	H'E6A49070	32	
TSIF0 pack target address register 0	TS0PKTADR0	R/W	H'0000	H'FFE88000	32	TSIF0 reception

Register Name	Abbreviation	R/W	Initial Value	Address	Access Size (Bits)	Target DMA Request (Extended Link Selector MID+RID)
TSIF0 pack total size register 0	TS0PKTSIZER0L	R/W	H'0000	H'FFE88004	32	H'EA
TSIF0 pack control register 0	TS0PKCTLR0	R/W	H'0000	H'FFE88008	32	
TSIF0 pack status register 0	TS0PKSTATR0H	R/W	H'0000	H'FFE8800C	32	
TSIF0 pack data register 0	TS0PKDATAR0	R/W	Undefined	H'FFE89000	32	
TSIF1 pack target address register 0	TS1PKTADR0	R/W	H'0000	H'FFE98000	32	TSIF0 reception
TSIF1 pack total size register 0	TS1PKTSIZER0L	R/W	H'0000	H'FFE98004	32	H'EE
TSIF1 pack control register 0	TS1PKCTLR0	R/W	H'0000	H'FFE98008	32	
TSIF1 pack status register 0	TS1PKSTATR0H	R/W	H'0000	H'FFE9800C	32	
TSIF1 pack data register 0	TS1PKDATAR0	R/W	Undefined	H'FFE99000	32	

G.10 Register Configuration of DDM

Register Name	Register Abbreviation	R/W	Initial Value	Address	Access Size (Bits)
DDM interrupt source mask register	DDIREQMSK	R/W	H'00000000	H'FE080008	32
DDM interrupt source register	DDIREQSTA	R	H'00000000	H'FE08000C	32
DDM start source polarity reversal register 1	DDINTINV1	R/W	H'00000000	H'FE080010	32
DDM start source polarity reversal register 2	DDINTINV2	R/W	H'00000000	H'FE080014	32
DDM CH1 start source mask register 1	DDINTMSK11	R/W	H'00000000	H'FE080030	32
DDM CH1 start source mask register 2	DDINTMSK12	R/W	H'00000000	H'FE080034	32
DDM CH1 start source mask register 3	DDINTMSK13	R/W	H'00000000	H'FE080038	32
DDM CH1 start source mask register 4	DDINTMSK14	R/W	H'00000000	H'FE08003C	32
DDM CH1 start source mask register 5	DDINTMSK15	R/W	H'00000000	H'FE080040	32
DDM CH1 descriptor pointer	DDPTR1	R/W	H'00000000	H'FE080050	32

Register Name	Register Abbreviation	R/W	Initial Value	Address	Access Size (Bits)
DDM CH1 control register	DDCTRL1	R/W	H'80000000	H'FE080054	32
DDM CH2 start source mask register 1	DDINTMSK21	R/W	H'00000000	H'FE080060	32
DDM CH2 start source mask register 2	DDINTMSK22	R/W	H'00000000	H'FE080064	32
DDM CH2 start source mask register 3	DDINTMSK23	R/W	H'00000000	H'FE080068	32
DDM CH2 start source mask register 4	DDINTMSK24	R/W	H'00000000	H'FE08006C	32
DDM CH2 start source mask register 5	DDINTMSK25	R/W	H'00000000	H'FE080070	32
DDM CH2 descriptor pointer	DDPTR2	R/W	H'00000000	H'FE080080	32
DDM CH2 control register	DDCTRL2	R/W	H'80000000	H'FE080084	32
DDM CH3 start source mask register 1	DDINTMSK31	R/W	H'00000000	H'FE080090	32
DDM CH3 start source mask register 2	DDINTMSK32	R/W	H'00000000	H'FE080094	32
DDM CH3 start source mask register 3	DDINTMSK33	R/W	H'00000000	H'FE080098	32
DDM CH3 start source mask register 4	DDINTMSK34	R/W	H'00000000	H'FE08009C	32
DDM CH3 start source mask register 5	DDINTMSK35	R/W	H'00000000	H'FE0800A0	32
DDM CH3 descriptor pointer	DDPTR3	R/W	H'00000000	H'FE0800B0	32
DDM CH3 control register	DDCTRL3	R/W	H'80000000	H'FE0800B4	32
DDM CH4 start source mask register 1	DDINTMSK41	R/W	H'00000000	H'FE0800C0	32
DDM CH4 start source mask register 2	DDINTMSK42	R/W	H'00000000	H'FE0800C4	32
DDM CH4 start source mask register 3	DDINTMSK43	R/W	H'00000000	H'FE0800C8	32
DDM CH4 start source mask register 4	DDINTMSK44	R/W	H'00000000	H'FE0800CC	32
DDM CH4 start source mask register 5	DDINTMSK45	R/W	H'00000000	H'FE0800D0	32
DDM CH4 descriptor pointer	DDPTR4	R/W	H'00000000	H'FE0800E0	32
DDM CH4 control register	DDCTRL4	R/W	H'80000000	H'FE0800E4	32
DDM CH5 start source mask register 1	DDINTMSK51	R/W	H'00000000	H'FE0800F0	32
DDM CH5 start source mask register 2	DDINTMSK52	R/W	H'00000000	H'FE0800F4	32
DDM CH5 start source mask register 3	DDINTMSK53	R/W	H'00000000	H'FE0800F8	32
DDM CH5 start source mask register 4	DDINTMSK54	R/W	H'00000000	H'FE0800FC	32

Register Name	Register Abbreviation	R/W	Initial Value	Address	Access Size (Bits)
DDM CH5 start source mask register 5	DDINTMSK55	R/W	H'00000000	H'FE080100	32
DDM CH5 descriptor pointer	DDPTR5	R/W	H'00000000	H'FE080110	32
DDM CH5 control register	DDCTRL5	R/W	H'80000000	H'FE080114	32
DDM CH6 start source mask register 1	DDINTMSK61	R/W	H'00000000	H'FE080120	32
DDM CH6 start source mask register 2	DDINTMSK62	R/W	H'00000000	H'FE080124	32
DDM CH6 start source mask register 3	DDINTMSK63	R/W	H'00000000	H'FE080128	32
DDM CH6 start source mask register 4	DDINTMSK64	R/W	H'00000000	H'FE08012C	32
DDM CH6 start source mask register 5	DDINTMSK65	R/W	H'00000000	H'FE080130	32
DDM CH6 descriptor pointer	DDPTR6	R/W	H'00000000	H'FE080140	32
DDM CH6 control register	DDCTRL6	R/W	H'80000000	H'FE080144	32
DDM CH7 start source mask register 1	DDINTMSK71	R/W	H'00000000	H'FE080150	32
DDM CH7 start source mask register 2	DDINTMSK72	R/W	H'00000000	H'FE080154	32
DDM CH7 start source mask register 3	DDINTMSK73	R/W	H'00000000	H'FE080158	32
DDM CH7 start source mask register 4	DDINTMSK74	R/W	H'00000000	H'FE08015C	32
DDM CH7 start source mask register 5	DDINTMSK75	R/W	H'00000000	H'FE080160	32
DDM CH7 descriptor pointer	DDPTR7	R/W	H'00000000	H'FE080170	32
DDM CH7 control register	DDCTRL7	R/W	H'80000000	H'FE080174	32
DDM CH8 start source mask register 1	DDINTMSK81	R/W	H'00000000	H'FE080180	32
DDM CH8 start source mask register 2	DDINTMSK82	R/W	H'00000000	H'FE080184	32
DDM CH8 start source mask register 3	DDINTMSK83	R/W	H'00000000	H'FE080188	32
DDM CH8 start source mask register 4	DDINTMSK84	R/W	H'00000000	H'FE08018C	32
DDM CH8 start source mask register 5	DDINTMSK85	R/W	H'00000000	H'FE080190	32
DDM CH8 descriptor pointer	DDPTR8	R/W	H'00000000	H'FE0801A0	32
DDM CH8 control register	DDCTRL8	R/W	H'80000000	H'FE0801A4	32

G.11 Register Configuration of CPGA

Register Name	Abbreviation	R/W	Address	Access Size
frequency control register A	FRQCRA	R/W	H'E615 0000	32
frequency control register B	FRQCRB	R/W	H'E615 0004	32
frequency control register C	FRQCRC	R/W	H'E615 00E0	32
frequency control register D	FRQCRD	R/W	H'E615 00E4	32
Video clock frequency control register 1	VCLKCR1	R/W	H'E615 0008	32
Video clock frequency control register 2	VCLKCR2	R/W	H'E615 000C	32
Video clock frequency control register 3	VCLKCR3	R/W	H'E615 001C	32
FMSI clock frequency control register	FMSICKCR	R/W	H'E615 0010	32
FMSO clock frequency control register	FMSOCKCR	R/W	H'E615 0014	32
FSIA clock frequency control register	FSIACKCR	R/W	H'E615 0018	32
FSIB clock frequency control register	FSIBCKCR	R/W	H'E615 0090	32
SUB clock frequency control register	SUBCKCR	R/W	H'E615 0080	32
SPU clock frequency control register	SPUCKCR	R/W	H'E615 0084	32
VOU clock frequency control register	VOUCKCR	R/W	H'E615 0088	32
HDMI clock frequency control register	HDMICKCR	R/W	H'E615 0094	32
MIPI DSI TX Link clock frequency control register	DSITCKCR	R/W	H'E615 0060	32
MIPI DSI PHY0 clock frequency control register	DSI0PCKCR	R/W	H'E615 0064	32
MIPI DSI PHY1 clock frequency control register	DSI1PCKCR	R/W	H'E615 0098	32
Music player mode register	MPMODE	R/W	H'E615 00CC	32
Realtime standby control register	RTSTBCR	R/W	H'E615 0020	32
System standby control register	SYSTBCR	R/W	H'E615 0024	32
PLLC0 and PLLC1 control register	PLLC01CR	R/W	H'E615 0028	32
PLLC0 and PLLC1 stop condition register	PLLC01STPCR	R/W	H'E61500C8	32
PLLC2 control register	PLLC2CR	R/W	H'E615 002C	32
Module stop status register 0	MSTPSR0	R	H'E615 0030	32
Module stop status register 1	MSTPSR1	R	H'E615 0038	32
Module stop status register 2	MSTPSR2	R	H'E615 0040	32
Module stop status register 3	MSTPSR3	R	H'E615 0048	32
Module stop status register 4	MSTPSR4	R	H'E615 004C	32
Realtime module stop control register 0	RMSTPCR0 *2	R/W	H'E615 0110	32
Realtime module stop control register 1	RMSTPCR1 *2	R/W	H'E615 0114	32
Realtime module stop control register 2	RMSTPCR2 *2	R/W	H'E615 0118	32

Register Name	Abbreviation	R/W	Address	Access Size
Realtime module stop control register 3	RMSTPCR3 *2	R/W	H'E615 011C	32
Realtime module stop control register 4	RMSTPCR4 *2	R/W	H'E615 0120	32
System module stop control register 0	SMSTPCR0 *2	R/W	H'E615 0130	32
System module stop control register 1	SMSTPCR1 *2	R/W	H'E615 0134	32
System module stop control register 2	SMSTPCR2 *2	R/W	H'E615 0138	32
System module stop control register 3	SMSTPCR3 *2	R/W	H'E615 013C	32
System module stop control register 4	SMSTPCR4 *2	R/W	H'E615 0140	32
Software reset register 0	SRCR0	R/W	H'E615 80A0 *1	32
Software reset register 1	SRCR1	R/W	H'E615 80A8 *1	32
Software reset register 2	SRCR2	R/W	H'E615 80B0 *1	32
Software reset register 3	SRCR3	R/W	H'E615 80B8 *1	32
Software reset register 4	SRCR4	R/W	H'E615 80BC *1	32
Status register	ASTAT	R	H'E615 0054	32
Clock source control register	CKSCR	R/W	H'E615 00C0	32
VREF control register	VREFCR	R/W	H'E615 0108	32

*1 Write access to a register allocated to address H'E615 8*** can be controlled through HPB semaphores. Obtain a semaphore before writing a register and release it after completing the write access.

*2 RMSTPCRn and SMSTPCRn might be collectively written as MSTPCRn.

G.12 Register Configuration of RWDT

Register Name	Abbreviation	R/W	Address*3	Access Size
RCLK watchdog timer counter 0	RWTCNT0	R/W	H'E602 0000 H'E702 0000	8/16*1
RCLK watchdog timer control/status register A0	RWTCSRA0	R/W	H'E602 0004 H'E702 0004	8/16*2
RCLK watchdog timer control/status register B0	RWTCSRB0	R/W	H'E602 0008 H'E702 0008	8/16*2
RCLK watchdog timer counter 1	RWTCNT1	R/W	H'E603 0000 H'E703 0000	8/16*1
RCLK watchdog timer control/status register A1	RWTCSRA1	R/W	H'E603 0004 H'E703 0004	8/16*2

Register Name	Abbreviation	R/W	Address*3	Access Size
RCLK watchdog timer control/status register B1	RWTCSRB1	R/W	H'E603 0008 H'E703 0008	8/16*2

*1 Write is performed in 16 bits and read in 8 bits.

*2 This register is accessible both from HPBC (E6 space) and HPBD (E7 space).

G.13 Register Configuration of SYSC

Register Name	Abbreviation	R/W	Address	Access Size	Access permission
Standby Flag Register0	STBCHR0	R/W	H'E618 0000	8/32	ALL
Standby Flag Register 1	STBCHR1	R/W	H'E618 0001	8/32	ALL
Standby Flag Register 2	STBCHR2	R/W	H'E618 0002	8/32	ALL
Standby Flag Register 3	STBCHR3	R/W	H'E618 0003	8/32	ALL
RT Power Down Control Register	RPDCR	R/W	H'E618 0004	32	RT
SYS Power Down Control Register	SPDCR	R/W	H'E618 0008	32	SYS
RT Wakeup Control Register	RWUCR	R/W	H'E618 0010	32	RT
SYS Wakeup Control Register	SWUCR	R/W	H'E618 0014	32	SYS
RT Boot Address Register	RBAR	R/W	H'E618 001C	32	ALL
SYS Boot Address Register	SBAR	R/W	H'E618 0020	32	ALL
WakeUpR Factor Mask Register	WUPRMSK	R/W	H'E618 0028	32	ALL
WakeUpS Factor Mask Register	WUPSMSK	R/W	H'E618 002C	32	ALL
Standby Flag Register B0	STBCHRB0	R/W	H'E618 0040	8/32	ALL
Standby Flag Register B1	STBCHRB1	R/W	H'E618 0041	8/32	ALL
Standby Flag Register B2	STBCHRB2	R/W	H'E618 0042	8/32	ALL
Standby Flag Register B3	STBCHRB3	R/W	H'E618 0043	8/32	ALL
WakeUpR Factor Mask Register2	WUPRMSK2	R/W	H'E618 0044	32	ALL
WakeUpS Factor Mask Register2	WUPSMSK2	R/W	H'E618 0048	32	ALL
A4S Area Power Control Register	A4SPOWCR	R/W	H'E618 0O4C	32	ALL
Power Status Register	PSTR	R	H'E618 0080	32	ALL
EXTAL2 State Monitor Register	EXSTMON2	R	H'E618 0088	32	ALL
EXTAL1 State Monitor Register	EXSTMON1	R	H'E618 008C	32	ALL
WakeUpR Factor Register	WUPRFAC	R	H'E618 0094	32	ALL
WakeUpS Factor Register	WUPSFAC	R	H'E618 0098	32	ALL

Register Name	Abbreviation	R/W	Address	Access Size	Access permission
RT Reset Flag Register	RRSTFR	R/(W) *3	H'E618 00B0	32	RT
SYS Reset Flag Register	SRSTFR	R/(W) *3	H'E618 00B4	32	SYS
Debug mode Power Control Register	DGBPOWCR	R/W	H'E618 00C0	32	ALL
RT Write Block Control Register	RWBCR	R/W	H'E618 0200	32	ALL
SYS Write Block Control Register	SWBCR	R/W	H'E618 0204	32	ALL
EXTAL2 Mask Count Register	EXMSKCNT2	R/W	H'E618 0210	32	ALL
EXTAL1 Mask Count Register	EXMSKCNT1	R/W	H'E618 0214	32	ALL
Reset Control Register	RESCNT	R/W	H'E618801C*1	32	ALL
Reset Control Register2	RESCNT2	R/W	H'E6188020*1	32	ALL
WakeUp Area Selection Register	WUPSEL	R/W	H'E618 0228	32	ALL
IRQ Detection Mode Control Register	IRQCR	R/W	H'E618 022C	32	ALL
EXTAL1 Clock Stop Control Register	APSCSTP	R/W	H'E618 0234	32	ALL
IRQ Detection Mode Control Register 2	IRQCR2	R/W	H'E618 0238	32	ALL
IRQ Detection Mode Control Register 3	IRQCR3	R/W	H'E618 0244	32	ALL
IRQ Detection Mode Control Register 4	IRQCR4	R/W	H'E618 0248	32	ALL
EXTAL1 Control Register	SYCKENMSK	R/W	H'E618 024C	32	ALL
WakeUp Area Selection Register2	WUPSEL2	R/W	H'E618 0250	32	ALL
A4S Area Power Control Register2	PDNSEL	R/W	H'E618 0254	32	ALL

*1 Registers with address H'E618 8*** should be updated through HPB semaphore. Please release the semaphore bit once the write accesses to these registers is completed. (Refer Appendix A for semaphore register details)

*2 The CPU number which can access these registers is registered in one of the semaphore registers. Please don't access these registers from CPU's other than this CPU.

*3 To clear the flag write `0`. Please write 1 to other flag to avoid unintentional clears.

G.14 Register Configuration of TMU

Register Name	Abbreviation	R/W	Address	Access Size
Timer start register 0	TSTR 0	R/W	H'FFF6 0004	8
Timer constant register0_0	TCOR0_0	R/W	H'FFF6 0008	32
Timer counter0_0	TCNT0_0	R/W	H'FFF6 000C	32
Timer control register0_0	TCR0_0	R/W	H'FFF6 0010	16
Timer constant register0_1	TCOR0_1	R/W	H'FFF6 0014	32
Timer counter0_1	TCNT0_1	R/W	H'FFF6 0018	32
Timer control register0_1	TCR0_1	R/W	H'FFF6 001C	16
Timer constant register0_2	TCOR0_2	R/W	H'FFF6 0020	32
Timer counter0_2	TCNT0_2	R/W	H'FFF6 0024	32
Timer control register0_2	TCR0_2	R/W	H'FFF6 0028	16
Timer start register 1	TSTR 1	R/W	H'FFF7 0004	8
Timer constant register1_0	TCOR1_0	R/W	H'FFF7 0008	32
Timer counter1_0	TCNT1_0	R/W	H'FFF7 000C	32
Timer control register1_0	TCR1_0	R/W	H'FFF7 0010	16
Timer constant register1_1	TCOR1_1	R/W	H'FFF7 0014	32
Timer counter1_1	TCNT1_1	R/W	H'FFF7 0018	32
Timer control register1_1	TCR1_1	R/W	H'FFF7 001C	16
Timer constant register1_2	TCOR1_2	R/W	H'FFF7 0020	32
Timer counter1_2	TCNT1_2	R/W	H'FFF7 0024	32
Timer control register1_2	TCR1_2	R/W	H'FFF7 0028	16

G.15 Register Configuration of TPU

Register Name	Abbreviation	R/W	Address	Access Size
Timer start register	TPU0_TSTR	R/W	H'E660 0000 H'E760 0000	16
Timer control register 0	TPU0_TCR0	R/W	H'E660 0010 H'E760 0010	16
Timer mode register 0	TPU0_TMDR0	R/W	H'E660 0014 H'E760 0014	16
Timer I/O control register 0	TPU0_TIOR0	R/W	H'E660 0018 H'E760 0018	16
Timer interrupt enable register 0	TPU0_TIER0	R/W	H'E660 001C H'E760 001C	16
Timer status register 0	TPU0_TSR0	R/W	H'E660 0020 H'E760 0020	16
Timer counter 0	TPU0_TCNT0	R/W	H'E660 0024 H'E760 0024	16
Timer general register 0A	TPU0_TGR0A	R/W	H'E660 0028 H'E760 0028	16

Register Name	Abbreviation	R/W	Address	Access Size
Timer general register 0B	TPU0_TGR0B	R/W	H'E660 002C H'E760 002C	16
Timer general register 0C	TPU0_TGR0C	R/W	H'E660 0030 H'E760 0030	16
Timer general register 0D	TPU0_TGR0D	R/W	H'E660 0034 H'E760 0034	16
Timer control register 1	TPU0_TCR1	R/W	H'E660 0050 H'E760 0050	16
Timer mode register 1	TPU0_TMDR1	R/W	H'E660 0054 H'E760 0054	16
Timer I/O control register 1	TPU0_TIOR1	R/W	H'E660 0058 H'E760 0058	16
Timer interrupt enable register 1	TPU0_TIER1	R/W	H'E660 005C H'E760 005C	16
Timer status register 1	TPU0_TSR1	R/W	H'E660 0060 H'E760 0060	16
Timer counter 1	TPU0_TCNT1	R/W	H'E660 0064 H'E760 0064	16
Timer general register 1A	TPU0_TGR1A	R/W	H'E660 0068 H'E760 0068	16
Timer general register 1B	TPU0_TGR1B	R/W	H'E660 006C H'E760 006C	16
Timer general register 1C	TPU0_TGR1C	R/W	H'E660 0070 H'E760 0070	16
Timer general register 1D	TPU0_TGR1D	R/W	H'E660 0074 H'E760 0074	16
Timer control register 2	TPU0_TCR2	R/W	H'E660 0090 H'E760 0090	16
Timer mode register 2	TPU0_TMDR2	R/W	H'E660 0094 H'E760 0094	16
Timer I/O control register 2	TPU0_TIOR2	R/W	H'E660 0098 H'E760 0098	16
Timer interrupt enable register 2	TPU0_TIER2	R/W	H'E660 009C H'E760 009C	16
Timer status register 2	TPU0_TSR2	R/W	H'E660 00A0 H'E760 00A0	16
Timer counter 2	TPU0_TCNT2	R/W	H'E660 00A4 H'E760 00A4	16
Timer general register 2A	TPU0_TGR2A	R/W	H'E660 00A8 H'E760 00A8	16
Timer general register 2B	TPU0_TGR2B	R/W	H'E660 00AC H'E760 00AC	16
Timer general register 2C	TPU0_TGR2C	R/W	H'E660 00B0 H'E760 00B0	16

Register Name	Abbreviation	R/W	Address	Access Size
Timer general register 2D	TPU0_TGR2D	R/W	H'E660 00B4 H'E760 00B4	16
Timer control register 3	TPU0_TCR3	R/W	H'E660 00D0 H'E760 00D0	16
Timer mode register 3	TPU0_TMDR3	R/W	H'E660 00D4 H'E760 00D4	16
Timer I/O control register 3	TPU0_TIOR3	R/W	H'E660 00D8 H'E760 00D8	16
Timer interrupt enable register 3	TPU0_TIER3	R/W	H'E660 00DC H'E760 00DC	16
Timer status register 3	TPU0_TSR3	R/W	H'E660 00E0 H'E760 00E0	16
Timer counter 3	TPU0_TCNT3	R/W	H'E660 00E4 H'E760 00E4	16
Timer general register 3A	TPU0_TGR3A	R/W	H'E660 00E8 H'E760 00E8	16
Timer general register 3B	TPU0_TGR3B	R/W	H'E660 00EC H'E760 00EC	16
Timer general register 3C	TPU0_TGR3C	R/W	H'E660 00F0 H'E760 00F0	16
Timer general register 3D	TPU0_TGR3D	R/W	H'E660 00F4 H'E760 00F4	16
Motor control configuration register*	TPU0_TMIR	R/W	H'E660 0100 H'E760 0100	16
Motor deceleration (stop) transition configuration register*	TPU0_TMRR	R/W	H'E660 0104 H'E760 0104	16
Motor control status register*	TPU0_TMSR	R	H'E660 0108 H'E760 0108	16
Motor operation pattern storage register 0*	TPU0_TMMPR0	R/W	H'E660 0110 H'E760 0110	16
Motor operation pattern storage register 1*	TPU0_TMMPR1	R/W	H'E660 0114 H'E760 0114	16
Motor stop pattern storage register 0*	TPU0_TMSPR0	R/W	H'E660 0118 H'E760 0118	16
Motor stop pattern storage register 1*	TPU0_TMSPR1	R/W	H'E660 011C H'E760 011C	16
Motor output pattern storage register*	TPU0_TMOPR	R/W	H'E660 0120 H'E760 0120	16
Motor acceleration the number of steps register*	TPU0_TMASR	R/W	H'E660 0130 H'E760 0130	16
Motor normal the number of steps register*	TPU0_TMTSR	R/W	H'E660 0134 H'E760 0134	16
Motor deceleration the number of steps register*	TPU0_TMRSR	R/W	H'E660 0138 H'E760 0138	16

Register Name	Abbreviation	R/W	Address	Access Size
Motor control sequence counter register*	TPU0_TMSCR	R/W	H'E660 0140 H'E760 0140	16
Motor control normal counter register*	TPU0_TMTCR	R	H'E660 0144 H'E760 0144	16

* Use only when stepping motor control is performed.

G.16 Register Configuration of CMT0

Register Name	Abbreviation	R/W	Address	Access Size
Compare match timer start register	CMSTR	R/W	H'FFCA 0000	16
Compare match timer control/status register	CMCSR	R/W	H'FFCA 0060	16
Compare match timer counter	CMCNT	R/W	H'FFCA 0064	32
Compare match timer constant register	CMCOR	R/W	H'FFCA 0068	32

G.17 Register Configuration of CMT1

Register Name	Abbreviation	R/W	Address		Access Size
			Regular	Shadow	
Compare match timer start register	CMSTR	R/W	H'E613 8000	H'E713 8000	16
Compare match timer control/status register 0	CMCSR0	R/W	H'E613 8010	H'E713 8010	16
Compare match timer control/status register 1	CMCSR1	R/W	H'E613 8020	H'E713 8020	16
Compare match timer control/status register 2	CMCSR2	R/W	H'E613 8030	H'E713 8030	16
Compare match timer control/status register 3	CMCSR3	R/W	H'E613 8040	H'E713 8040	16
Compare match timer control/status register 4	CMCSR4	R/W	H'E613 8050	H'E713 8050	16
Compare match timer control/status register 5	CMCSR5	R/W	H'E613 8060	H'E713 8060	16
Compare match timer control/status register H0	CMCSRH0	R/W	H'E613 8110	H'E713 8110	16
Compare match timer control/status register H1	CMCSRH1	R/W	H'E613 8120	H'E713 8120	16
Compare match timer control/status register H2	CMCSRH2	R/W	H'E613 8130	H'E713 8130	16

Register Name	Abbreviation	R/W	Address		Access Size
			Regular	Shadow	
Compare match timer control/status register H3	CMCSRH3	R/W	H'E613 8140	H'E713 8140	16
Compare match timer control/status register H4	CMCSRH4	R/W	H'E613 8150	H'E713 8150	16
Compare match timer control/status register H5	CMCSRH5	R/W	H'E613 8160	H'E713 8160	16
Compare match timer counter 0	CMCNT0	R/W	H'E613 8014	H'E713 8014	32
Compare match timer counter 1	CMCNT1	R/W	H'E613 8024	H'E713 8024	32
Compare match timer counter 2	CMCNT2	R/W	H'E613 8034	H'E713 8034	32
Compare match timer counter 3	CMCNT3	R/W	H'E613 8044	H'E713 8044	32
Compare match timer counter 4	CMCNT4	R/W	H'E613 8054	H'E713 8054	32
Compare match timer counter 5	CMCNT5	R/W	H'E613 8064	H'E713 8064	32
Compare match timer counter H0	CMCNTH0	R/W	H'E613 8114	H'E713 8114	16
Compare match timer counter H1	CMCNTH1	R/W	H'E613 8124	H'E713 8124	16
Compare match timer counter H2	CMCNTH2	R/W	H'E613 8134	H'E713 8134	16
Compare match timer counter H3	CMCNTH3	R/W	H'E613 8144	H'E713 8144	16
Compare match timer counter H4	CMCNTH4	R/W	H'E613 8154	H'E713 8154	16
Compare match timer counter H5	CMCNTH5	R/W	H'E613 8164	H'E713 8164	16
Compare match timer constant register 0	CMCOR0	R/W	H'E613 8018	H'E713 8018	32
Compare match timer constant register 1	CMCOR1	R/W	H'E613 8028	H'E713 8028	32
Compare match timer constant register 2	CMCOR2	R/W	H'E613 8038	H'E713 8038	32
Compare match timer constant register 3	CMCOR3	R/W	H'E613 8048	H'E713 8048	32
Compare match timer constant register 4	CMCOR4	R/W	H'E613 8058	H'E713 8058	32
Compare match timer constant register 5	CMCOR5	R/W	H'E613 8068	H'E713 8068	32
Compare match timer constant register H0	CMCORH0	R/W	H'E613 8118	H'E713 8118	16
Compare match timer constant register H1	CMCORH1	R/W	H'E613 8128	H'E713 8128	16
Compare match timer constant register H2	CMCORH2	R/W	H'E613 8138	H'E713 8138	16
Compare match timer constant register H3	CMCORH3	R/W	H'E613 8148	H'E713 8148	16
Compare match timer constant register H4	CMCORH4	R/W	H'E613 8158	H'E713 8158	16
Compare match timer constant register H5	CMCORH5	R/W	H'E613 8168	H'E713 8168	16
Compare match timer counter 3 backup 0	CMCNT3BK0	R	H'E613 8080	H'E713 8080	32

Register Name	Abbreviation	R/W	Address		Access Size
			Regular	Shadow	
Compare match timer counter 3 backup 1	CMCNT3BK1	R	H'E613 8084	H'E713 8084	32
Compare match timer match control/status register 0	CMCSRM0	R/W	H'E613 8090	H'E713 8090	16
Compare match timer match control/status register 3	CMCSRM3	R/W	H'E613 80C0	H'E713 80C0	16
Compare match timer match counter 0	CMCNTM0	R/W	H'E613 8094	H'E713 8094	32
Compare match timer match counter 3	CMCNTM3	R/W	H'E613 80C4	H'E713 80C4	32

G.18 Register Configuration of CMT2

Register Name	Abbreviation	R/W	Address		Access Size
			Regular	Shadow	
Compare match timer start register	CM2STR	R/W	H'E613 0000 H'E613 4000	H'E713 0000 H'E713 4000	16
Compare match timer control/status register	CM2CSR	R/W	H'E613 0040 H'E613 4040	H'E713 0040 H'E713 4040	16
Compare match timer counter	CM2CNT	R/W	H'E613 0044 H'E613 4044	H'E713 0044 H'E713 4044	32
Compare match timer constant register	CM2COR	R/W	H'E613 0048 H'E613 4048	H'E713 0048 H'E713 4048	32

* Accessing to H'E6130XXX, H'E7130XXX is off the subject of HPB semaphore.
Accessing to H'E6134XXX, H'E7134XXX is a subject of HPB semaphore.

G.19 Register Configuration of CMT3

Register Name	Abbreviation	R/W	Address		Access Size
			Regular	Shadow	
Compare match timer start register	CM3STR	R/W	H'E614 0000	H'E714 0000	16
Compare match timer control/status register	CM3CSR	R/W	H'E614 0040	H'E714 0040	16
Compare match timer counter	CM3CNT	R/W	H'E614 0044	H'E714 0044	32
Compare match timer constant register	CM3COR	R/W	H'E614 0048	H'E714 0048	32

G.20 Register Configuration of CMT4

Register Name	Abbreviation	R/W	Address		Access Size
			Regular	Shadow	
Compare match timer start register	CM4STR	R/W	H'E614 8000	H'E714 8000	16
Compare match timer control/status register	CM4CSR	R/W	H'E614 8040	H'E714 8040	16
Compare match timer counter	CM4CNT	R/W	H'E614 8044	H'E714 8044	32
Compare match timer constant register	CM4COR	R/W	H'E614 8048	H'E714 8048	32

G.21 Register Configuration of SCIFA

Register Name	Abbreviation	R/W	Address		Access Size
			Regular	Shadow	
Serial mode register A0	SCASMR0	R/W	H'E6C4 0000	H'E7C4 0000	16
Bit rate register A0	SCABRR0	R/W	H'E6C4 0004	H'E7C4 0004	8
Serial control register A0	SCASCR0	R/W	H'E6C4 0008	H'E7C4 0008	16
Transmit data stop register A0	SCATDSR0	R/W	H'E6C4 000C	H'E7C4 000C	8
FIFO error count register A0	SCAFER0	R	H'E6C4 0010	H'E7C4 0010	16
Serial status register A0	SCASSR0	R/W*	H'E6C4 0014	H'E7C4 0014	16
FIFO control register A0	SCAFCR0	R/W	H'E6C4 0018	H'E7C4 0018	16
FIFO data count register A0	SCAFDR0	R	H'E6C4 001C	H'E7C4 001C	16
Transmit FIFO data register A0	SCAFTDR0	W	H'E6C4 0020	H'E7C4 0020	8
Receive FIFO data register A0	SCAFRDR0	R	H'E6C4 0024	H'E7C4 0024	8
Serial port control register A0	SCAPCR0	R/W	H'E6C4 0030	H'E7C4 0030	16
Serial port data register A0	SCAPDR0	R/W	H'E6C4 0034	H'E7C4 0034	16
Serial mode register A1	SCASMR1	R/W	H'E6C5 0000	H'E7C5 0000	16
Bit rate register A1	SCABRR1	R/W	H'E6C5 0004	H'E7C5 0004	8
Serial control register A1	SCASCR1	R/W	H'E6C5 0008	H'E7C5 0008	16
Transmit data stop register A1	SCATDSR1	R/W	H'E6C5 000C	H'E7C5 000C	8
FIFO error count register A1	SCAFER1	R	H'E6C5 0010	H'E7C5 0010	16
Serial status register A1	SCASSR1	R/W*	H'E6C5 0014	H'E7C5 0014	16
FIFO control register A1	SCAFCR1	R/W	H'E6C5 0018	H'E7C5 0018	16
FIFO data count register A1	SCAFDR1	R	H'E6C5 001C	H'E7C5 001C	16
Transmit FIFO data register A1	SCAFTDR1	W	H'E6C5 0020	H'E7C5 0020	8
Receive FIFO data register A1	SCAFRDR1	R	H'E6C5 0024	H'E7C5 0024	8
Serial port control register A1	SCAPCR1	R/W	H'E6C5 0030	H'E7C5 0030	16
Serial port data register A1	SCAPDR1	R/W	H'E6C5 0034	H'E7C5 0034	16
Serial mode register A2	SCASMR2	R/W	H'E6C6 0000	H'E7C6 0000	16
Bit rate register A2	SCABRR2	R/W	H'E6C6 0004	H'E7C6 0004	8
Serial control register A2	SCASCR2	R/W	H'E6C6 0008	H'E7C6 0008	16
Transmit data stop register A2	SCATDSR2	R/W	H'E6C6 000C	H'E7C6 000C	8
FIFO error count register A2	SCAFER2	R	H'E6C6 0010	H'E7C6 0010	16

Register Name	Abbreviation	R/W	Address		Access Size
			Regular	Shadow	
Serial status register A2	SCASSR2	R/W*	H'E6C6 0014	H'E7C6 0014	16
FIFO control register A2	SCAFCR2	R/W	H'E6C6 0018	H'E7C6 0018	16
FIFO data count register A2	SCAFDR2	R	H'E6C6 001C	H'E7C6 001C	16
Transmit FIFO data register A2	SCAFTDR2	W	H'E6C6 0020	H'E7C6 0020	8
Receive FIFO data register A2	SCAFRDR2	R	H'E6C6 0024	H'E7C6 0024	8
Serial port control register A2	SCAPCR2	R/W	H'E6C6 0030	H'E7C6 0030	16
Serial port data register A2	SCAPDR2	R/W	H'E6C6 0034	H'E7C6 0034	16
Serial mode register A3	SCASMR3	R/W	H'E6C7 0000	H'E7C7 0000	16
Bit rate register A3	SCABRR3	R/W	H'E6C7 0004	H'E7C7 0004	8
Serial control register A3	SCASCR3	R/W	H'E6C7 0008	H'E7C7 0008	16
Transmit data stop register A3	SCATDSR3	R/W	H'E6C7 000C	H'E7C7 000C	8
FIFO error count register A3	SCAFER3	R	H'E6C7 0010	H'E7C7 0010	16
Serial status register A3	SCASSR3	R/W*	H'E6C7 0014	H'E7C7 0014	16
FIFO control register A3	SCAFCR3	R/W	H'E6C7 0018	H'E7C7 0018	16
FIFO data count register A3	SCAFDR3	R	H'E6C7 001C	H'E7C7 001C	16
Transmit FIFO data register A3	SCAFTDR3	W	H'E6C7 0020	H'E7C7 0020	8
Receive FIFO data register A3	SCAFRDR3	R	H'E6C7 0024	H'E7C7 0024	8
Serial port control register A3	SCAPCR3	R/W	H'E6C7 0030	H'E7C7 0030	16
Serial port data register A3	SCAPDR3	R/W	H'E6C7 0034	H'E7C7 0034	16
Serial mode register A4	SCASMR4	R/W	H'E6C8 0000	H'E7C8 0000	16
Bit rate register A4	SCABRR4	R/W	H'E6C8 0004	H'E7C8 0004	8
Serial control register A4	SCASCR4	R/W	H'E6C8 0008	H'E7C8 0008	16
Transmit data stop register A4	SCATDSR4	R/W	H'E6C8 000C	H'E7C8 000C	8
FIFO error count register A4	SCAFER4	R	H'E6C8 0010	H'E7C8 0010	16
Serial status register A4	SCASSR4	R/W*	H'E6C8 0014	H'E7C8 0014	16
FIFO control register A4	SCAFCR4	R/W	H'E6C8 0018	H'E7C8 0018	16
FIFO data count register A4	SCAFDR4	R	H'E6C8 001C	H'E7C8 001C	16
Transmit FIFO data register A4	SCAFTDR4	W	H'E6C8 0020	H'E7C8 0020	8
Receive FIFO data register A4	SCAFRDR4	R	H'E6C8 0024	H'E7C8 0024	8
Serial port control register A4	SCAPCR4	R/W	H'E6C8 0030	H'E7C8 0030	16
Serial port data register A4	SCAPDR4	R/W	H'E6C8 0034	H'E7C8 0034	16
Serial mode register A5	SCASMR5	R/W	H'E6CB 0000	H'E7CB 0000	16
Bit rate register A5	SCABRR5	R/W	H'E6CB 0004	H'E7CB 0004	8
Serial control register A5	SCASCR5	R/W	H'E6CB 0008	H'E7CB 0008	16
Transmit data stop register A5	SCATDSR5	R/W	H'E6CB 000C	H'E7CB 000C	8
FIFO error count register A5	SCAFER5	R	H'E6CB 0010	H'E7CB 0010	16
Serial status register A5	SCASSR5	R/W*	H'E6CB 0014	H'E7CB 0014	16
FIFO control register A5	SCAFCR5	R/W	H'E6CB 0018	H'E7CB 0018	16
FIFO data count register A5	SCAFDR5	R	H'E6CB 001C	H'E7CB 001C	16
Transmit FIFO data register A5	SCAFTDR5	W	H'E6CB 0020	H'E7CB 0020	8
Receive FIFO data register A5	SCAFRDR5	R	H'E6CB 0024	H'E7CB 0024	8
Serial port control register A5	SCAPCR5	R/W	H'E6CB 0030	H'E7CB 0030	16
Serial port data register A5	SCAPDR5	R/W	H'E6CB 0034	H'E7CB 0034	16

* To clear the flags, 0s can only be written to bits 9 to 7, 5, 4, 1, and 0.

G.22 Register Configuration of SCIFB

Register Name	Abbreviation	R/W	Address		Access Size
			Regular	Shadow	
Serial mode register B	SCBSMR	R/W	H'E6C3 0000	H'E7C3 0000	16
Bit rate register B	SCBBRR	R/W	H'E6C3 0004	H'E7C3 0004	8
Serial control register B	SCBSCR	R/W	H'E6C3 0008	H'E7C3 0008	16
Transmit data stop register B	SCBTDSR	R/W	H'E6C3 000C	H'E7C3 000C	16
FIFO error count register B	SCBFER	R	H'E6C3 0010	H'E7C3 0010	16
Serial status register B	SCBSSR	R/W*	H'E6C3 0014	H'E7C3 0014	16
FIFO control register B	SCBFCR	R/W	H'E6C3 0018	H'E7C3 0018	16
Receive data count compare register B	SCBRCER	R/W	H'E6C3 0028	H'E7C3 0028	16
Multibyte set register B	SCBMBR	R/W	H'E6C3 002C	H'E7C3 002C	16
Serial port control register B	SCBPCR	R/W	H'E6C3 0030	H'E7C3 0030	16
Serial port data register B	SCBPDR	R/W	H'E6C3 0034	H'E7C3 0034	16
Transmit FIFO data count register B	SCBTFDR	R	H'E6C3 0038	H'E7C3 0038	16
Receive FIFO data count register B	SCBRFDR	R	H'E6C3 003C	H'E7C3 003C	16
Transmit FIFO data register B	SCBFTDR	W	H'E6C3 0040	H'E7C3 0040	8
Receive FIFO data register B	SCBFRDR	R	H'E6C3 0060	H'E7C3 0060	8

* To clear the flags, 0s can only be written to bits 13, 9, 8, 7, 5, 4, 1, and 0.

G.23 Register Configuration of MSIOF

Register Name	Abbreviation	R/W	Address	Access Size
MSIOF0 transmit mode register 1	SI0TMDR1	R/W	H'FFF1 0000	32
MSIOF0 transmit mode register 2	SI0TMDR2	R/W	HFFF1 0004	32
MSIOF0 transmit mode register 3	SI0TMDR3	R/W	H'FFF1 0008	32
MSIOF0 receive mode register 1	SI0RMDR1	R/W	H'FFF1 0010	32
MSIOF0 receive mode register 2	SI0RMDR2	R/W	H'FFF1 0014	32
MSIOF0 receive mode register 3	SI0RMDR3	R/W	H'FFF1 0018	32
MSIOF0 transmit clock select register	SI0TSCR	R/W	H'FFF1 0020	16
MSIOF0 receive clock select register	SI0RSCR	R/W	H'FFF1 0022	16
MSIOF0 control register	SI0CTR	R/W	H'FFF1 0028	32
MSIOF0 FIFO control register	SI0FCTR	R/W	H'FFF1 0030	32
MSIOF0 status register	SI0STR	R/W	H'FFF1 0040	32

Register Name	Abbreviation	R/W	Address	Access Size
MSIOF0 interrupt enable register	SI0IER	R/W	H'FFF1 0044	32
MSIOF0 transmit control data register 1	SI0TDR1	W	H'FFF1 0048	16/32
MSIOF0 transmit control data register 2	SI0TDR2	W	H'FFF1 004C	16/32
MSIOF0 transmit FIFO data register	SI0TFDR	W	H'FFF1 0050	8/16/32
MSIOF0 receive control data register 1	SI0RDR1	R	H'FFF1 0058	16/32
MSIOF0 receive control data register 2	SI0RDR2	R	H'FFF1 005C	16/32
MSIOF0 receive FIFO data register	SI0RFDR	R	H'FFF1 0060	8/16/32
MSIOF1 transmit mode register 1	SI1TMDR1	R/W	H'E6E1 0000 H'E7E1 0000	32
MSIOF1 transmit mode register 2	SI1TMDR2	R/W	HE6E1 0004 HE7E1 0004	32
MSIOF1 transmit mode register 3	SI1TMDR3	R/W	H'E6E1 0008 H'E7E1 0008	32
MSIOF1 receive mode register 1	SI1RMDR1	R/W	H'E6E1 0010 H'E7E1 0010	32
MSIOF1 receive mode register 2	SI1RMDR2	R/W	H'E6E1 0014 H'E7E1 0014	32
MSIOF1 receive mode register 3	SI1RMDR3	R/W	H'E6E1 0018 H'E7E1 0018	32
MSIOF1 transmit clock select register	SI1TSCR	R/W	H'E6E1 0020 H'E7E1 0020	16
MSIOF1 receive clock select register	SI1RSCR	R/W	H'E6E1 0022 H'E7E1 0022	16
MSIOF1 control register	SI1CTR	R/W	H'E6E1 0028 H'E7E1 0028	32
MSIOF1 FIFO control register	SI1FCTR	R/W	H'E6E1 0030 H'E7E1 0030	32
MSIOF1 status register	SI1STR	R/W	H'E6E1 0040 H'E7E1 0040	32
MSIOF1 interrupt enable register	SI1IER	R/W	H'E6E1 0044 H'E7E1 0044	32
MSIOF1 transmit control data register 1	SI1TDR1	W	H'E6E1 0048 H'E7E1 0048	16/32
MSIOF1 transmit control data register 2	SI1TDR2	W	H'E6E1 004C H'E7E1 004C	16/32
MSIOF1 transmit FIFO data register	SI1TFDR	W	H'E6E1 0050 H'E7E1 0050	8/16/32
MSIOF1 receive control data register 1	SI1RDR1	R	H'E6E1 0058 H'E7E1 0058	16/32
MSIOF1 receive control data register	SI1RDR2	R	H'E6E1 005C	16/32

Register Name	Abbreviation	R/W	Address	Access Size
2			H'E7E1 005C	
MSIOF1 receive FIFO data register	SI1RFDR	R	H'E6E1 0060 H'E7E1 0060	8/16/32
MSIOF2 transmit mode register 1	SI2TMDR1	R/W	H'E6E0 0000 H'E7E0 0000	32
MSIOF2 transmit mode register 2	SI2TMDR2	R/W	HE6E0 0004 HE7E0 0004	32
MSIOF2 transmit mode register 3	SI2TMDR3	R/W	H'E6E0 0008 H'E7E0 0008	32
MSIOF2 receive mode register 1	SI2RMDR1	R/W	H'E6E0 0010 H'E7E0 0010	32
MSIOF2 receive mode register 2	SI2RMDR2	R/W	H'E6E0 0014 H'E7E0 0014	32
MSIOF2 receive mode register 3	SI2RMDR3	R/W	H'E6E0 0018 H'E7E0 0018	32
MSIOF2 transmit clock select register	SI2TSCR	R/W	H'E6E0 0020 H'E7E0 0020	16
MSIOF2 receive clock select register	SI2RSCR	R/W	H'E6E0 0022 H'E7E0 0022	16
MSIOF2 control register	SI2CTR	R/W	H'E6E0 0028 H'E7E0 0028	32
MSIOF2 FIFO control register	SI2FCTR	R/W	H'E6E0 0030 H'E7E0 0030	32
MSIOF2 status register	SI2STR	R/W	H'E6E0 0040 H'E7E0 0040	32
MSIOF2 interrupt enable register	SI2IER	R/W	H'E6E0 0044 H'E7E0 0044	32
MSIOF2 transmit control data register 1	SI2TDR1	R/W	H'E6E0 0048 H'E7E0 0048	16/32
MSIOF2 transmit control data register 2	SI2TDR2	R/W	H'E6E0 004C H'E7E0 004C	16/32
MSIOF2 transmit FIFO data register	SI2TFDR	W	H'E6E0 0050 H'E7E0 0050	8/16/32
MSIOF2 receive control data register 1	SI2RDR1	R	H'E6E0 0058 H'E7E0 0058	16/32
MSIOF2 receive control data register 2	SI2RDR2	R	H'E6E0 005C H'E7E0 005C	16/32
MSIOF2 receive FIFO data register	SI2RFDR	R	H'E6E0 0060 H'E7E0 0060	8/16/32

Note: The MSIOF0 registers (address: H'FFF1 xxxx) are located in the realtime domain, and the MSIOF1 registers (address: H'E6E1 xxxx/H'E76E xxxx) and the MSIOF2 registers (address: H'E6E0 xxxx/H'E7E0 xxxx) are located in the system domain.

G.24 Register Configuration of BBIF1

Register Name	Abbreviation	R/W	Address	Access Size
BBIF1 transmit mode register 1	SITMDR1	R/W	H'E6C90000 H'E7C90000	32
BBIF1 transmit mode register 2	SITMDR2	R/W	HE6C90004 HE7C90004	32
BBIF1 transmit mode register 3	SITMDR3	R/W	H'E6C90008 H'E7C90008	32
BBIF1 receive mode register 1	SIRMDR1	R/W	H'E6C90010 H'E7C90010	32
BBIF1 receive mode register 2	SIRMDR2	R/W	H'E6C90014 H'E7C90014	32
BBIF1 receive mode register 3	SIRMDR3	R/W	H'E6C90018 H'E7C90018	32
BBIF1 transmit clock select register	SITSCR	R/W	H'E6C90020 H'E7C90020	16
BBIF1 control register	SICTR	R/W	H'E6C90028 H'E7C90028	32
BBIF1 FIFO control register	SIFCTR	R/W	H'E6C90030 H'E7C90030	32
BBIF1 status register	SISTR	R/W	H'E6C90040 H'E7C90040	32
BBIF1 interrupt enable register	SIIER	R/W	H'E6C90044 H'E7C90044	32
BBIF1 transmit control data register 1	SITDR1	W	H'E6C90048 H'E7C90048	16/32
BBIF1 transmit control data register 2	SITDR2	W	H'E6C9004C H'E7C9004C	16/32
BBIF1 transmit FIFO data register	SITFDR	W	H'E6C90050 H'E7C90050	16/32
BBIF1 receive control data register 1	SIRDR1	R	H'E6C90058 H'E7C90058	16/32
BBIF1 receive control data register 2	SIRDR2	R	H'E6C9005C H'E7C9005C	16/32
BBIF1 receive FIFO data register	SIRFDR	R	H'E6C90060 H'E7C90060	16/32
BBIF1 flow control register	SIFLCTR	R/W	H'E6C90064 H'E7C90064	32

G.25 Register Configuration of BBIF2

Register Name	Abbreviation	R/W	Address	Access Size

Register Name	Abbreviation	R/W	Address	Access Size
BBIF2 transmit mode register 1	SITMDR1	R/W	H'E6CA0000 H'E7CA0000 H'FFFA0000	32
BBIF2 transmit mode register 2	SITMDR2	R/W	HE6CA0004 HE7CA0004 HFFFA0004	32
BBIF2 transmit mode register 3	SITMDR3	R/W	H'E6CA0008 H'E7CA0008 H'FFFA0008	32
BBIF2 receive mode register 1	SIRMDR1	R/W	H'E6CA0010 H'E7CA0010 H'FFFA0010	32
BBIF2 receive mode register 2	SIRMDR2	R/W	H'E6CA0014 H'E7CA0014 H'FFFA0014	32
BBIF2 receive mode register 3	SIRMDR3	R/W	H'E6CA0018 H'E7CA0018 H'FFFA0018	32
BBIF2 transmit clock select register	SITSCR	R/W	H'E6CA0020 H'E7CA0020 H'FFFA0020	16
BBIF2 control register	SICTR	R/W	H'E6CA0028 H'E7CA0028 H'FFFA0028	32
BBIF2 FIFO control register	SIFCTR	R/W	H'E6CA0030 H'E7CA0030 H'FFFA0030	32
BBIF2 status register	SISTR	R/W	H'E6CA0040 H'E7CA0040 H'FFFA0040	32
BBIF2 interrupt enable register	SIIER	R/W	H'E6CA0044 H'E7CA0044 H'FFFA0044	32
BBIF2 transmit control data register 1	SITDR1	R/W	H'E6CA0048 H'E7CA0048 H'FFFA0048	16/32
BBIF2 transmit control data register 2	SITDR2	R/W	H'E6CA004C H'E7CA004C H'FFFA004C	16/32
BBIF2 transmit FIFO data register	SITFDR	W	H'E6CA0050 H'E7CA0050 H'FFFA0050	16/32
BBIF2 receive control data register 1	SIRDR1	R	H'E6CA0058 H'E7CA0058	16/32

Register Name	Abbreviation	R/W	Address	Access Size
			H'FFFA0058	
BBIF2 receive control data register 2	SIRDR2	R	H'E6CA005C H'E7CA005C H'FFFA005C	16/32
BBIF2 receive FIFO data register	SIRFDR	R	H'E6CA0060 H'E7CA0060 H'FFFA0060	16/32

Note: H'FFFAxxxx and H'E6CAxxxx (or H'E7CAxxxx) are used when making an access from the realtime domain and system domain, respectively.

G.26 Register Configuration of HSI

Register Name	Abbreviation	R/W	Address	Initial Value	Access Size
TX control register	HSI_TXCR	R/W	H'E6A40000	H'00000000	32
TX ready negation control register	HSI_TXRNCR	R/W	H'E6A40004	H'00000000	32
TX timeout control register	HSI_TXTOCR	R/W	H'E6A40008	H'00000000	32
TX break control register	HSI_TXBRKCR	R/W	H'E6A4000C	H'00000000	32
TXFIFO status register	HSI_TXFSR	R	H'E6A40020	H'00000000	32
RX control register	HSI_RXCR	R/W	H'E6A40030	H'00000000	32
RX timeout detection time period control register	HSI_RXTOCR	R/W	H'E6A40034	H'00000000	32
RX tailing bit detection time period control register	HSI_RXTLCR	R/W	H'E6A40038	H'00000000	32
Receiver drain timeout detection time period control register	HSI_RXDTOCR	R/W	H'E6A4003C	H'00000000	32
RX burst count constraint register	HSI_RXBCCR	R/W	H'E6A40040	H'00000000	32
RX FIFO status register	HSI_RXFSR	R	H'E6A40050	H'00000000	32
TXDMA control register	HSI_DMATXCR	R/W	H'E6A40060	H'00000000	32
RXDMA control register	HSI_DMARXCR	R/W	H'E6A40064	H'00000000	32
Interrupt control register	HSI_IRQCR	R/W	H'E6A40070	H'00000000	32
Interrupt status register	HSI_IRQSR	R/W	H'E6A40080	H'00000001	32
IO port control register	HSI_IOCR	R/W	H'E6A40090	H'00000000	32
TXCH_ID register (bank 0)	HSI_TX_CH0	W	H'E6A400B0	Undefined	32
TX data window (bank 0)	HSI_TX_DATA0	W	H'E6A400B4	Undefined	32
TXCH_ID register (bank 1)	HSI_TX_CH1	W	H'E6A400B8	Undefined	32
TX data window (bank 1)	HSI_TX_DATA1	W	H'E6A400BC	Undefined	32
TXCH_ID register (bank 2)	HSI_TX_CH2	W	H'E6A400C0	Undefined	32
TX data window (bank 2)	HSI_TX_DATA2	W	H'E6A400C4	Undefined	32
TXCH_ID register (bank 3)	HSI_TX_CH3	W	H'E6A400C8	Undefined	32
TX data window (bank 3)	HSI_TX_DATA3	W	H'E6A400CC	Undefined	32

Register Name	Abbreviation	R/W	Address	Initial Value	Access Size
TXCH_ID status register	HSI_TX_CHSR	R/W	H'E6A400F0	Undefined	32
TXCH_ID/data window (bank 0)	HSI_TX_CHDATA0	W	H'E6A40100	Undefined	32
TXCH_ID/data window (bank 1)	HSI_TX_CHDATA1	W	H'E6A40104	Undefined	32
TXCH_ID/data window (bank 2)	HSI_TX_CHDATA2	W	H'E6A40108	Undefined	32
TXCH_ID/data window (bank 3)	HSI_TX_CHDATA3	W	H'E6A4010C	Undefined	32
RXCH_ID register (bank 0)	HSI_RX_CH0	R	H'E6A40130	Undefined	32
RX data window (bank 0)	HSI_RX_DATA0	R	H'E6A40134	Undefined	32
RXCH_ID register (bank 1)	HSI_RX_CH1	R	H'E6A40138	Undefined	32
RX data window (bank 1)	HSI_RX_DATA1	R	H'E6A4013C	Undefined	32
RXCH_ID register (bank 2)	HSI_RX_CH2	R	H'E6A40140	Undefined	32
RX data window (bank 2)	HSI_RX_DATA2	R	H'E6A40144	Undefined	32
RXCH_ID register (bank 3)	HSI_RX_CH3	R	H'E6A40148	Undefined	32
RX data window (bank 3)	HSI_RX_DATA3	R	H'E6A4014C	Undefined	32
RXCH_ID status register	HSI_RX_CHSR	R/W	H'E6A40170	Undefined	32
RXCH_ID/data window (bank 0)	HSI_RX_CHDATA0	R	H'E6A40180	Undefined	32
RXCH_ID/data window (bank 1)	HSI_RX_CHDATA1	R	H'E6A40184	Undefined	32
RXCH_ID/data window (bank 2)	HSI_RX_CHDATA2	R	H'E6A40188	Undefined	32
RXCH_ID/data window (bank 3)	HSI_RX_CHDATA3	R	H'E6A4018C	Undefined	32

G.27 Register Configuration of MMCIF

Register Name	Abbreviation	R/W	Address	Access Size
Command setting register	CE_CMD_SET	R/W	H'E6BD0000	16, 32
Argument register	CE_ARG	R/W	H'E6BD0008	16, 32
Argument register for automatically-issued CMD12	CE_ARG_CMD12	R/W	H'E6BD000C	16, 32
Command control register	CE_CMD_CTRL	R/W	H'E6BD0010	16, 32
Transfer block setting register	CE_BLOCK_SET	R/W	H'E6BD0014	16, 32
Clock control register	CE_CLK_CTRL	R/W	H'E6BD0018	16, 32
Buffer access configuration register	CE_BUF_ACC	R/W	H'E6BD001c	16, 32
Response register 3	CE_RESP3	R/W	H'E6BD0020	16, 32
Response register 2	CE_RESP2	R/W	H'E6BD0024	16, 32
Response register 1	CE_RESP1	R/W	H'E6BD0028	16, 32
Response register 0	CE_RESP0	R/W	H'E6BD002C	16, 32
Response register for automatically-issued CMD12	CE_RESP_CMD12	R/W	H'E6BD0030	16, 32
Data register	CE_DATA	R/W	H'E6BD0034	16*, 32
Boot Operation setting register	CE_BOOT	R/W	H'E6BD003C	16, 32
Interrupt flag register	CE_INT	R/W	H'E6BD0040	16, 32
Interrupt enable register	CE_INT_MASK	R/W	H'E6BD0044	16, 32
Status register 1	CE_HOST_STS1	R/W	H'E6BD0048	16, 32
Status register 2	CE_HOST_STS2	R/W	H'E6BD004C	16, 32

Register Name	Abbreviation	R/W	Address	Access Size
Version register	CE_VERSION	R/W	H'E6BD007C	16, 32

Note: Do not access registers other than those shown above.

* For 16-bit access, H'E6BD0034 is the only address for access.

G.28 Register Configuration of FLCTL

Register Name	Abbreviation	R/W	Address	Access Size
Common control register	FLCMNCR	R/W	H'E6A3 0000	32
Command control register	FLCMDCR	R/W	H'E6A3 0004	32
Command code register	FLCMCDR	R/W	H'E6A3 0008	32
Address register	FLADR	R/W	H'E6A3 000C	32
Address register 2	FLADR2	R/W	H'E6A3 003C	32
Data register	FLDATAR	R/W	H'E6A3 0010	32
Data counter register	FLDTCNTR	R/W	H'E6A3 0014	32
Interrupt DMA control register	FLINTDMACR	R/W	H'E6A3 0018	32
Ready busy timeout setting register	FLBSYTMR	R/W	H'E6A3 001C	32
Ready busy timeout counter	FLBSYCNT	R	H'E6A3 0020	32
Data FIFO register	FLDTFIFO	R/W	H'E6A3 0024/ H'E6A3 0050	32
Control code FIFO register	FLECFIFO	R/W	H'E6A3 0028/ H'E6A3 0060	32
Transfer control register	FLTRCR	R/W	H'E6A3 002C	8
Bus occupation period setting register	FLHOLDCR	R/W	H'E6A3 0038	32
4-symbol ECCRESULT1	FL4ECCRESULT1	R	H'E6A3 0080	32
4-symbol ECCRESULT2	FL4ECCRESULT2	R	H'E6A3 0084	32
4-symbol ECCRESULT3	FL4ECCRESULT3	R	H'E6A3 0088	32
4-symbol ECCRESULT4	FL4ECCRESULT4	R	H'E6A3 008C	32
4-symbol ECC control register	FL4ECCCR	R/W	H'E6A3 0090	32
ECC error count register	FL4ECCCNT	R/W	H'E6A3 0094	32
Error address indication register	FLERRADR	R/W	H'E6A3 0098	32

G.29 Register Configuration of MFI

G.29.1 Register Configuration of MFIM

Register Name	Abbreviation	R/W	Address	Access Size
MMFROM	MMFROM	R	H'E6B0 0000 to	32, 16, 8

Register Name	Abbreviation	R/W	Address	Access Size
			H'E6B0 FFFF	

G.29.2 Register Configuration of MFIS

Register Name	Abbreviation	R/W	Address	Access Size
MMFROM	**MMFROM**	**R**	**H'E6B0 0000 to H'E6B0 FFFF**	**32, 16, 8**
MFIS index register	MFISIDX	R/W	H'E6A6 0000	32
MFIS general status register	MFISGSR	R/W	H'E6A6 0004	32
MFIS status/control register	MFISSCR	R/W	H'E6A6 0008	32
MFIS memory control register	MFISMCR	R/W	H'E6A6 000C	32
MFIS internal interrupt control register	MFISIICR	R/W	H'E6A6 0010	32
MFIS external interrupt control register	MFISEICR	R/W	H'E6A6 0014	32
MFIS address register	MFISADR	R/W	H'E6A6 0018	32
MFIS data register	MFISDATA	R/W	H'E6A6 001C	32
MFIS semaphore register	MFISSM4	R/W	H'E6A6 0080	32
SMFRAM	SMFRAM	R/W	H'E6A7 0000 to H'E6A7 03FF	32, 16, 8

G.30 Register Configuration of ACMFI1

Register Name	Abbreviation	R/W	Address	Access Size
ACMFI index register	ACMFIIDX	R/W	H'E6B7 0000	32
ACMFI general status register	ACMFIGSR	R/W	H'E6B7 0004	32
ACMFI status/control register	ACMFISCR	R/W	H'E6B7 0008	32
ACMFI memory control register	ACMFIMCR	R/W	H'E6B7 000C	32
ACMFI internal interrupt control register	ACMFIIICR	R/W	H'E6B7 0010	32
ACMFI external interrupt control register	ACMFIEICR	R/W	H'E6B7 0014	32
ACMFI address register	ACMFIADR	R/W	H'E6B7 0018	32
ACMFI data register	ACMFIDATA	R/W	H'E6B7 001C	32
ACMFI register control register	ACMFIRCR	R/W	H'E6B7 0020	32
ACMFI address register (for DMA write)	ACMFIADRW	R/W	H'E6B7 0044	32
ACMFI address register (for DMA read)	ACMFIADRR	R/W	H'E6B7 0048	32
ACMFI data register (for DMA write)	ACMFIDATAW	R/W	H'E6B7 004C	32
ACMFI data register (for DMA read)	ACMFIDATAR	R/W	H'E6B7 0050	32

Register Name	Abbreviation	R/W	Address	Access Size
ACMFI memory control register (for DMA write)	ACMFIMCRW	R/W	H'E6B7 0054	32
ACMFI memory control register (for DMA read)	ACMFIMCRR	R/W	H'E6B7 0058	32
ACMFI transfer number register (for DMA write)	ACMFIDNRW	R	H'E6B7 005C	32
ACMFI transfer number register (for DMA read)	ACMFIDNRR	R	H'E6B7 0060	32
ACMFI transfer size register (for DMA write)	ACMFISIZEW	R/W	H'E6B7 0064	32
ACMFI transfer size register (for DMA read)	ACMFISIZER	R/W	H'E6B7 0068	32
ACMFI semaphore register	ACMFISM4	R/W	H'E6B7 0080	32
ACMFI internal RAM	ACMFRAM	R/W	H'E6B9 0000 to H'E6B9 FFFF	32, 16, 8

Note: Access size shows access size from on-chip CPU. Access size from external device via AC parallel interface 1 is 16bit.

G.31 Register Configuration of ACMFI2

G.31.1 Register Configuration of access from on-chip CPU

Register Name	Abbreviation	R/W	Address	Access Size
ACMFI general status register	ACMFIGSR	R/W	H'E6B80000	32
ACMFI semaphore register	ACMFISM4	R/W	H'E6B80004	32
ACMFI internal interrupt control register	ACMFIIICR	R/W	H'E6B80008	32
ACMFI external interrupt control register 0	ACMFIEICR0	R/W	H'E6B8000C	32
ACMFI indirect access control register	ACMFIIDACR	R	H'E6B80010	32
ACMFI indirect access address register	ACMFIIDAA	R	H'E6B80014	32
ACMFI indirect access data register	ACMFIIDAD	R	H'E6B80018	32
(Reserve)		R	H'E6B8001C	32
ACMFI synchronous transfer control register	ACMFISYNC	R	H'E6B80020	32
ACMFI synchronous transfer address register	ACMFISYNCA	R	H'E6B80024	32
ACMFI synchronous transfer status register	ACMFISYNCS	R	H'E6B80028	32

Register Name	Abbreviation	R/W	Address	Access Size
ACMFI synchronous transfer status mask register	ACMFISYNCMASK	R/W	H'E6B8002C	32
ACMFI address protection register	ACMFIPTCR	R/W	H'E6B80030	32
ACMFI protection error address register	ACMFIPTCERA	R	H'E6B80034	32
ACMFRAM protection register	ACRAMPTCR	R/W	H'E6B80038	32
ACMFI external interrupt control register 1	ACMFIEICR1	R/W	H'E6B8003C	32
ACMFI internal RAM	ACMFRAM	R/W	H'E6B90000 to H'E6B9FFFF	32, 16, 8

G.31.2 Register Configuration of access from external device

Register Name	Abbreviation	R/W	Address(*)	Access Size
ACMFI general status register	ACMFIGSR	R/W	H'00000	16
ACMFI semaphore register	ACMFISM4	R/W	H'00004	16
ACMFI internal interrupt control register	ACMFIIICR	R/W	H'00008	16
ACMFI external interrupt control register 0	ACMFIEICR0	R/W	H'0000C	16
ACMFI indirect access control register	ACMFIIDACR	R/W	H'00010	16
ACMFI indirect access address register	ACMFIIDAA	R/W	H'00014	16
ACMFI indirect access data register	ACMFIIDAD	R/W	H'00018	16
(Reserve)		R	H'0001C	16
ACMFI synchronous transfer control register	ACMFISYNC	R/W	H'00020	16
ACMFI synchronous transfer address register	ACMFISYNCA	R/W	H'00024	16
ACMFI synchronous transfer status register	ACMFISYNCS	R/W	H'00028	16
ACMFI synchronous transfer status mask register	ACMFISYNCMASK	R/W	H'0002C	16
ACMFI address protection register	ACMFIPTCR	R	H'00030	16
ACMFI protection error address register	ACMFIPTCERA	R	H'00034	16
ACMFRAM protection register	ACRAMPTCR	R	H'00038	16
ACMFI external interrupt control register 1	ACMFIEICR1	R/W	H'0003C	16
ACMFI internal RAM	ACMFRAM	R/W	H'10000 to H'1 FFFF	16

* Access from external device to the above-mentioned register group is possible only in case of asynchronous access (MEMC_CS0 use). Note that the external input address is 2-byte boundary. 1bit right shift of the above-mentioned address is fundamentally equivalent to the external address PIN.

G.32 Register Configuration of USBHS0

Register Name	Abbreviation	R/W	Address	Access Size
System configuration control register	SYSCFG	R/W	H'E689 0000	16
CPU bus wait register	BUSWAIT	R/W	H'E689 0002	16
System configuration status register	SYSSTS	R	H'E689 0004	16
Device state control register	DVSTCTR	R/W	H'E689 0008	16
Test mode register	TESTMODE	R/W	H'E689 000C	16
CFIFO port register	CFIFO	R/W	H'E689 0014	32
CFIFO port select register	CFIFOSEL	R/W	H'E689 0020	16
CFIFO port control register	CFIFOCTR	R/W	H'E689 0022	16
D0FIFO port select register	D0FIFOSEL	R/W	H'E689 0028	16
D0FIFO port control register	D0FIFOCTR	R/W	H'E689 002A	16
D1FIFO port select register	D1FIFOSEL	R/W	H'E689 002C	16
D1FIFO port control register	D1FIFOCTR	R/W	H'E689 002E	16
Interrupt enable register 0	INTENB0	R/W	H'E689 0030	16
Interrupt enable register 1	INTENB1	R/W	H'E689 0032	16
BRDY interrupt enable register	BRDYENB	R/W	H'E689 0036	16
NRDY interrupt enable register	NRDYENB	R/W	H'E689 0038	16
BEMP interrupt enable register	BEMPENB	R/W	H'E689 003A	16
SOF output configuration register	SOFCFG	R/W	H'E689 003C	16
Interrupt status register 0	INTSTS0	R/W	H'E689 0040	16
Interrupt status register 1	INTSTS1	R/W	H'E689 0042	16
BRDY interrupt status register	BRDYSTS	R/W	H'E689 0046	16
NRDY interrupt status register	NRDYSTS	R/W	H'E689 0048	16
BEMP interrupt status register	BEMPSTS	R/W	H'E689 004A	16
Frame number register	FRMNUM	R/W	H'E689 004C	16
m frame number register	UFRMNUM	R/W	H'E689 004E	16
USB address register	USBADDR	R	H'E689 0050	16
USB request type register	USBREQ	R	H'E689 0054	16
USB request value register	USBVAL	R	H'E689 0056	16
USB request index register	USBINDX	R	H'E689 0058	16
USB request length register	USBLENG	R	H'E689 005A	16
DCP configuration register	DCPCFG	R/W	H'E689 005C	16
DCP maximum packet size register	DCPMAXP	R/W	H'E689 005E	16
DCP control register	DCPCTR	R/W	H'E689 0060	16
Pipe window select register	PIPESEL	R/W	H'E689 0064	16

Register Name	Abbreviation	R/W	Address	Access Size
Pipe configuration register	PIPECFG	R/W	H'E689 0068	16
Pipe buffer register	PIPEBUF	R/W	H'E689 006A	16
Pipe maximum packet size register	PIPEMAXP	R/W	H'E689 006C	16
Pipe cycle control register	PIPEPERI	R/W	H'E689 006E	16
Pipe 1 control register	PIPE1CTR	R/W	H'E689 0070	16
Pipe 2 control register	PIPE2CTR	R/W	H'E689 0072	16
Pipe 3 control register	PIPE3CTR	R/W	H'E689 0074	16
Pipe 4 control register	PIPE4CTR	R/W	H'E689 0076	16
Pipe 5 control register	PIPE5CTR	R/W	H'E689 0078	16
Pipe 6 control register	PIPE6CTR	R/W	H'E689 007A	16
Pipe 7 control register	PIPE7CTR	R/W	H'E689 007C	16
Pipe 8 control register	PIPE8CTR	R/W	H'E689 007E	16
Pipe 9 control register	PIPE9CTR	R/W	H'E689 0080	16
Pipe 1 transaction counter enable register	PIPE1TRE	R/W	H'E689 0090	16
Pipe 1 transaction counter register	PIPE1TRN	R/W	H'E689 0092	16
Pipe 2 transaction counter enable register	PIPE2TRE	R/W	H'E689 0094	16
Pipe 2 transaction counter register	PIPE2TRN	R/W	H'E689 0096	16
Pipe 3 transaction counter enable register	PIPE3TRE	R/W	H'E689 0098	16
Pipe 3 transaction counter register	PIPE3TRN	R/W	H'E689 009A	16
Pipe 4 transaction counter enable register	PIPE4TRE	R/W	H'E689 009C	16
Pipe 4 transaction counter register	PIPE4TRN	R/W	H'E689 009E	16
Pipe 5 transaction counter enable register	PIPE5TRE	R/W	H'E689 00A0	16
Pipe 5 transaction counter register	PIPE5TRN	R/W	H'E689 00A2	16
Device address 0 configuration register	DEVADD0	R/W	H'E689 00D0	16
Device address 1 configuration register	DEVADD1	R/W	H'E689 00D2	16
Device address 2 configuration register	DEVADD2	R/W	H'E689 00D4	16
Device address 3 configuration register	DEVADD3	R/W	H'E689 00D6	16
Device address 4 configuration register	DEVADD4	R/W	H'E689 00D8	16
Device address 5 configuration register	DEVADD5	R/W	H'E689 00DA	16
Device address 6 configuration register	DEVADD6	R/W	H'E689 00DC	16
Device address 7 configuration register	DEVADD7	R/W	H'E689 00DE	16

Register Name	Abbreviation	R/W	Address	Access Size
Device address 8 configuration register	DEVADD8	R/W	H'E689 00E0	16
Device address 9 configuration register	DEVADD9	R/W	H'E689 00E2	16
Device address A configuration register	DEVADDA	R/W	H'E689 00E4	16

G.33 Register Configuration of USBHS1

Register Name	Abbreviation	R/W	Address	Access Size
System configuration control register	SYSCFG	R/W	H'E68B 0000	16
CPU bus wait register	BUSWAIT	R/W	H'E68B 0002	16
System configuration status register	SYSSTS	R	H'E68B 0004	16
Device state control register	DVSTCTR	R/W	H'E68B 0008	16
Test mode register	TESTMODE	R/W	H'E68B 000C	16
CFIFO port register	CFIFO	R/W	H'E68B 0014	32
CFIFO port select register	CFIFOSEL	R/W	H'E68B 0020	16
CFIFO port control register	CFIFOCTR	R/W	H'E68B 0022	16
D0FIFO port select register	D0FIFOSEL	R/W	H'E68B 0028	16
D0FIFO port control register	D0FIFOCTR	R/W	H'E68B 002A	16
D1FIFO port select register	D1FIFOSEL	R/W	H'E68B 002C	16
D1FIFO port control register	D1FIFOCTR	R/W	H'E68B 002E	16
Interrupt enable register 0	INTENB0	R/W	H'E68B 0030	16
Interrupt enable register 1	INTENB1	R/W	H'E68B 0032	16
BRDY interrupt enable register	BRDYENB	R/W	H'E68B 0036	16
NRDY interrupt enable register	NRDYENB	R/W	H'E68B 0038	16
BEMP interrupt enable register	BEMPENB	R/W	H'E68B 003A	16
SOF output configuration register	SOFCFG	R/W	H'E68B 003C	16
Interrupt status register 0	INTSTS0	R/W	H'E68B 0040	16
Interrupt status register 1	INTSTS1	R/W	H'E68B 0042	16
BRDY interrupt status register	BRDYSTS	R/W	H'E68B 0046	16
NRDY interrupt status register	NRDYSTS	R/W	H'E68B 0048	16
BEMP interrupt status register	BEMPSTS	R/W	H'E68B 004A	16
Frame number register	FRMNUM	R/W	H'E68B 004C	16
m frame number register	UFRMNUM	R/W	H'E68B 004E	16
USB address register	USBADDR	R	H'E68B 0050	16
USB request type register	USBREQ	R	H'E68B 0054	16
USB request value register	USBVAL	R	H'E68B 0056	16
USB request index register	USBINDX	R	H'E68B 0058	16
USB request length register	USBLENG	R	H'E68B 005A	16
DCP configuration register	DCPCFG	R/W	H'E68B 005C	16
DCP maximum packet size register	DCPMAXP	R/W	H'E68B 005E	16

Register Name	Abbreviation	R/W	Address	Access Size
DCP control register	DCPCTR	R/W	H'E68B 0060	16
Pipe window select register	PIPESEL	R/W	H'E68B 0064	16
Pipe configuration register	PIPECFG	R/W	H'E68B 0068	16
Pipe buffer register	PIPEBUF	R/W	H'E68B 006A	16
Pipe maximum packet size register	PIPEMAXP	R/W	H'E68B 006C	16
Pipe cycle control register	PIPEPERI	R/W	H'E68B 006E	16
Pipe 1 control register	PIPE1CTR	R/W	H'E68B 0070	16
Pipe 2 control register	PIPE2CTR	R/W	H'E68B 0072	16
Pipe 3 control register	PIPE3CTR	R/W	H'E68B 0074	16
Pipe 4 control register	PIPE4CTR	R/W	H'E68B 0076	16
Pipe 5 control register	PIPE5CTR	R/W	H'E68B 0078	16
Pipe 6 control register	PIPE6CTR	R/W	H'E68B 007A	16
Pipe 7 control register	PIPE7CTR	R/W	H'E68B 007C	16
Pipe 8 control register	PIPE8CTR	R/W	H'E68B 007E	16
Pipe 9 control register	PIPE9CTR	R/W	H'E68B 0080	16
Pipe A control register	PIPEACTR	R/W	H'E68B 0082	16
Pipe B control register	PIPEBCTR	R/W	H'E68B 0084	16
Pipe C control register	PIPECCTR	R/W	H'E68B 0086	16
Pipe D control register	PIPEDCTR	R/W	H'E68B 0088	16
Pipe E control register	PIPEECTR	R/W	H'E68B 008A	16
Pipe F control register	PIPEFCTR	R/W	H'E68B 008C	16
Pipe 1 transaction counter enable register	PIPE1TRE	R/W	H'E68B 0090	16
Pipe 1 transaction counter register	PIPE1TRN	R/W	H'E68B 0092	16
Pipe 2 transaction counter enable register	PIPE2TRE	R/W	H'E68B 0094	16
Pipe 2 transaction counter register	PIPE2TRN	R/W	H'E68B 0096	16
Pipe 3 transaction counter enable register	PIPE3TRE	R/W	H'E68B 0098	16
Pipe 3 transaction counter register	PIPE3TRN	R/W	H'E68B 009A	16
Pipe 4 transaction counter enable register	PIPE4TRE	R/W	H'E68B 009C	16
Pipe 4 transaction counter register	PIPE4TRN	R/W	H'E68B 009E	16
Pipe 5 transaction counter enable register	PIPE5TRE	R/W	H'E68B 00A0	16
Pipe 5 transaction counter register	PIPE5TRN	R/W	H'E68B 00A2	16
Pipe B transaction counter enable register	PIPEBTRE	R/W	H'E68B 00A4	16
Pipe B transaction counter register	PIPEBTRN	R/W	H'E68B 00A6	16
Pipe C transaction counter enable register	PIPECTRE	R/W	H'E68B 00A8	16
Pipe C transaction counter register	PIPECTRN	R/W	H'E68B 00AA	16
Pipe D transaction counter enable register	PIPEDTRE	R/W	H'E68B 00AC	16
Pipe D transaction counter register	PIPEDTRN	R/W	H'E68B 00AE	16

Register Name	Abbreviation	R/W	Address	Access Size
Pipe E transaction counter enable register	PIPEETRE	R/W	H'E68B 00B0	16
Pipe E transaction counter register	PIPEETRN	R/W	H'E68B 00B2	16
Pipe F transaction counter enable register	PIPEFTRE	R/W	H'E68B 00B4	16
Pipe F transaction counter register	PIPEFTRN	R/W	H'E68B 00B6	16
Pipe 9 transaction counter enable register	PIPE9TRE	R/W	H'E68B 00B8	16
Pipe 9 transaction counter register	PIPE9TRN	R/W	H'E68B 00BA	16
Pipe A transaction counter enable register	PIPEATRE	R/W	H'E68B 00BC	16
Pipe A transaction counter register	PIPEATRN	R/W	H'E68B 00BE	16
Device address 0 configuration register	DEVADD0	R/W	H'E68B 00D0	16
Device address 1 configuration register	DEVADD1	R/W	H'E68B 00D2	16
Device address 2 configuration register	DEVADD2	R/W	H'E68B 00D4	16
Device address 3 configuration register	DEVADD3	R/W	H'E68B 00D6	16
Device address 4 configuration register	DEVADD4	R/W	H'E68B 00D8	16
Device address 5 configuration register	DEVADD5	R/W	H'E68B 00DA	16
Device address 6 configuration register	DEVADD6	R/W	H'E68B 00DC	16
Device address 7 configuration register	DEVADD7	R/W	H'E68B 00DE	16
Device address 8 configuration register	DEVADD8	R/W	H'E68B 00E0	16
Device address 9 configuration register	DEVADD9	R/W	H'E68B 00E2	16
Device address A configuration register	DEVADDA	R/W	H'E68B 00E4	16

G.34 Register Configuration of CEU

Register Name	Abbreviation	R/W	Addresses			Access Size
			Address (Plane A)	Address (Plane B)	Mirror Address	
Capture start register	CAPSR	R/W	H'FE91 0000	-	-	32
Capture control register	CAPCR	R/W	H'FE91 0004	-	-	32

Register Name	Abbreviation	R/W	Addresses			Access Size
			Address (Plane A)	Address (Plane B)	Mirror Address	
Capture interface control register*	CAMCR	R/W	H'FE91 0008	-	-	32
Capture interface cycle register*	CMCYR	R/W	H'FE91 000C	-	-	32
Capture interface offset register	CAMOR	R/W	H'FE91 0010	H'FE91 1010	H'FE91 2010	32
Capture interface width register	CAPWR	R/W	H'FE91 0014	H'FE91 1014	H'FE91 2014	32
Capture interface input format register	CAIFR	R/W	H'FE91 0018	-	-	32
Camera strobe control register	CSTCR	R/W	H'FE91 0020	-	-	32
Camera strobe emission count register	CSECR	R/W	H'FE91 0024	-	-	32
CEU register control register	CRCNTR	R/W	H'FE91 0028	-	-	32
CEU register forcible control register	CRCMPR	R/W	H'FE91 002C	-	-	32
Capture filter control register	CFLCR	R/W	H'FE91 0030	H'FE91 1030	H'FE91 2030	32
Capture filter size clip register	CFSZR	R/W	H'FE91 0034	H'FE91 1034	H'FE91 2034	32
Capture destination width register	CDWDR	R/W	H'FE91 0038	H'FE91 1038	H'FE91 2038	32
Capture data address Y register	CDAYR	R/W	H'FE91 003C	H'FE91 103C	H'FE91 203C	32
Capture data address C register	CDACR	R/W	H'FE91 0040	H'FE91 1040	H'FE91 2040	32
Capture data bottom-field address Y register	CDBYR	R/W	H'FE91 0044	H'FE91 1044	H'FE91 2044	32
Capture data bottom-field address C register	CDBCR	R/W	H'FE91 0048	H'FE91 1048	H'FE91 2048	32
Capture bundle destination size register	CBDSR	R/W	H'FE91 004C	H'FE91 104C	H'FE91 204C	32
Firewall operating control register	CFWCR	R/W	H'FE91 005C	-	-	32
Capture low-pass filter control register	CLFCR	R/W	H'FE91 0060	H'FE91 1060	H'FE91 2060	32
Capture data output control register	CDOCR	R/W	H'FE91 0064	H'FE91 1064	H'FE91 2064	32

Register Name	Abbreviation	R/W	Addresses			Access Size
			Address (Plane A)	Address (Plane B)	Mirror Address	
Capture data complexity level register	CDDCR	R/W	H'FE91 0068	H'FE91 1068	H'FE91 2068	32
Capture data complexity level address register	CDDAR	R/W	H'FE91 006C	H'FE91 106C	H'FE91 206C	32
Capture event interrupt enable register	CEIER	R/W	H'FE91 0070	-	-	32
Capture event flag clear register	CETCR	R/W	H'FE91 0074	-	-	32
Capture status register	CSTSR	R	H'FE91 007C	-	-	32
Capture software reset register	CSRTR	R/W	H'FE91 0080	-	-	32
Capture data capacity register	CDSSR	R/W	H'FE91 0084	-	-	32
Capture data address Y register 2	CDAYR2	R/W	H'FE91 0090	H'FE91 1090	H'FE91 2090	32
Capture data address C register 2	CDACR2	R/W	H'FE91 0094	H'FE91 1094	H'FE91 2094	32
Capture data bottom-field address Y register 2	CDBYR2	R/W	H'FE91 0098	H'FE91 1098	H'FE91 2098	32
Capture data bottom-field address C register 2	CDBCR2	R/W	H'FE91 009C	H'FE91 109C	H'FE91 209C	32

* After changing the setting of a register (CAMCR or CMCYR) that is determined by the external module characteristics, do not start capture until at least 10 external input clock cycles have elapsed.

G.35 Register Configuration of VEU

Register Name	Abbreviation	R/W	Address	Access Size
VEU0 start register	VE0STR	R/W	H'FE92 0000	32
VEU0 source memory width register	VE0SWR	R/W	H'FE92 0010	32
VEU0 source size register	VE0SSR	R/W	H'FE92 0014	32
VEU0 source address Y register	V0SAYR	R/W	H'FE92 0018	32
VEU0 source address C register	V0SACR	R/W	H'FE92 001C	32
VEU0 bundle source size register	V0BSSR	R/W	H'FE92 0020	32

Register Name	Abbreviation	R/W	Address	Access Size
VEU0 destination memory width register	VE0DWR	R/W	H'FE92 0030	32
VEU0 destination address Y register	V0DAYR	R/W	H'FE92 0034	32
VEU0 destination address C register	V0DACR	R/W	H'FE92 0038	32
VEU0 transform control register	V0TRCR	R/W	H'FE92 0050	32
VEU0 resize filter control register	V0RFCR	R/W	H'FE92 0054	32
VEU0 resize filter size clip register	V0RFSR	R/W	H'FE92 0058	32
VEU0 enhance register	VE0NHR	R/W	H'FE92 005C	32
VEU0 resize filter sub control register	V0RSCR	R/W	H'FE92 0064	32
VEU0 resize filter size clip offset register	V0RSOR	R/W	H'FE92 0068	32
VEU0 filter mode control register	V0FMCR	R/W	H'FE92 0070	32
VEU0 vertical tap coefficient register	V0VTCR	R/W	H'FE92 0074	32
VEU0 horizontal tap coefficient register	V0HTCR	R/W	H'FE92 0078	32
VEU0 designated color register	V0APCR	R/W	H'FE92 0080	32
VEU0 conversion color register	VE0CCR	R/W	H'FE92 0084	32
VEU0 fill color specification register	V0FLCR	RW	H'FE92 0088	32
VEU0 address fixed register	V0AFXR	R/W	H'FE92 0090	32
VEU0 swapping register	V0SWPR	R/W	H'FE92 0094	32
VEU0 event interrupt enable register	VE0IER	R/W	H'FE92 00A0	32
VEU0 event register	VE0VTR	R/W	H'FE92 00A4	32
VEU0 status register	V0STAR	R	H'FE92 00B0	32
VEU0 module reset register	V0BSRR	R/W	H'FE92 00B4	32
VEU0 resize passband register	V0RPBR	R/W	H'FE92 00C8	32
VEU1 start register	VE1STR	R/W	H'FE92 4000	32
VEU1 source memory width register	VE1SWR	R/W	H'FE92 4010	32
VEU1 source size register	VE1SSR	R/W	H'FE92 4014	32
VEU1 source address Y register	V1SAYR	R/W	H'FE92 4018	32
VEU1 source address C register	V1SACR	R/W	H'FE92 401C	32
VEU1 bundle source size register	V1BSSR	R/W	H'FE92 4020	32
VEU1 destination memory width register	VE1DWR	R/W	H'FE92 4030	32
VEU1 destination address Y register	V1DAYR	R/W	H'FE92 4034	32
VEU1 destination address C register	V1DACR	R/W	H'FE92 4038	32
VEU1 transform control register	V1TRCR	R/W	H'FE92 4050	32
VEU1 resize filter control register	V1RFCR	R/W	H'FE92 4054	32
VEU1 resize filter size clip register	V1RFSR	R/W	H'FE92 4058	32
VEU1 enhance register	VE1NHR	R/W	H'FE92 405C	32
VEU1 resize filter sub control register	V1RSCR	R/W	H'FE92 4064	32
VEU1 resize filter size clip offset register	V1RSOR	R/W	H'FE92 4068	32
VEU1 filter mode control register	V1FMCR	R/W	H'FE92 4070	32

Register Name	Abbreviation	R/W	Address	Access Size
VEU1 vertical tap coefficient register	V1VTCR	R/W	H'FE92 4074	32
VEU1 horizontal tap coefficient register	V1HTCR	R/W	H'FE92 4078	32
VEU1 designated color register	V1APCR	R/W	H'FE92 4080	32
VEU1 conversion color register	VE1CCR	R/W	H'FE92 4084	32
VEU1 fill color specification register	V1FLCR	RW	H'FE92 4088	32
VEU1 address fixed register	V1AFXR	R/W	H'FE92 4090	32
VEU1 swapping register	V1SWPR	R/W	H'FE92 4094	32
VEU1 event interrupt enable register	VE1IER	R/W	H'FE92 40A0	32
VEU1 event register	VE1VTR	R/W	H'FE92 40A4	32
VEU1 status register	V1STAR	R	H'FE92 40B0	32
VEU1 module reset register	V1BSRR	R/W	H'FE92 40B4	32
VEU1 resize passband register	V1RPBR	R/W	H'FE92 40C8	32
VEU2 start register	VE2STR	R/W	H'FE92 8000	32
VEU2 source memory width register	VE2SWR	R/W	H'FE92 8010	32
VEU2 source size register	VE2SSR	R/W	H'FE92 8014	32
VEU2 source address Y register	V2SAYR	R/W	H'FE92 8018	32
VEU2 source address C register	V2SACR	R/W	H'FE92 801C	32
VEU2 bundle source size register	V2BSSR	R/W	H'FE92 8020	32
VEU2 destination memory width register	VE2DWR	R/W	H'FE92 8030	32
VEU2 destination address Y register	V2DAYR	R/W	H'FE92 8034	32
VEU2 destination address C register	V2DACR	R/W	H'FE92 8038	32
VEU2 transform control register	V2TRCR	R/W	H'FE92 8050	32
VEU2 resize filter control register	V2RFCR	R/W	H'FE92 8054	32
VEU2 resize filter size clip register	V2RFSR	R/W	H'FE92 8058	32
VEU2 enhance register	VE2NHR	R/W	H'FE92 805C	32
VEU2 resize filter sub control register	V2RSCR	R/W	H'FE92 8064	32
VEU2 resize filter size clip offset register	V2RSOR	R/W	H'FE92 8068	32
VEU2 filter mode control register	V2FMCR	R/W	H'FE92 8070	32
VEU2 vertical tap coefficient register	V2VTCR	R/W	H'FE92 8074	32
VEU2 horizontal tap coefficient register	V2HTCR	R/W	H'FE92 8078	32
VEU2 designated color register	V2APCR	R/W	H'FE92 8080	32
VEU2 conversion color register	VE2CCR	R/W	H'FE92 8084	32
VEU2 fill color specification register	V2FLCR	RW	H'FE92 8088	32
VEU2 address fixed register	V2AFXR	R/W	H'FE92 8090	32
VEU2 swapping register	V2SWPR	R/W	H'FE92 8094	32
VEU2 event interrupt enable register	VE2IER	R/W	H'FE92 80A0	32
VEU2 event register	VE2VTR	R/W	H'FE92 80A4	32
VEU2 status register	V2STAR	R	H'FE92 80B0	32
VEU2 module reset register	V2BSRR	R/W	H'FE92 80B4	32

Register Name	Abbreviation	R/W	Address	Access Size
VEU2 resize passband register	V2RPBR	R/W	H'FE92 80C8	32
VEU2 resize interpolation setting register	VEUAD2_RSZ_ITP	R/W	H'FE92 8180	32
VEU2 horizontal FIR filter coefficient Y/G pixel setting 0	VEUAD2_FCOE_HY0	R/W	H'FE92 8200	32
VEU2 horizontal FIR filter coefficient Y/G pixel setting 1	VEUAD2_FCOE_HY1	R/W	H'FE92 8204	32
VEU2 horizontal FIR filter coefficient Y/G pixel setting 2	VEUAD2_FCOE_HY2	R/W	H'FE92 8208	32
VEU2 horizontal FIR filter coefficient Cb/B pixel setting 0	VEUAD2_FCOE_HCB0	R/W	H'FE92 8210	32
VEU2 horizontal FIR filter coefficient Cb/B pixel setting 1	VEUAD2_FCOE_HCB1	R/W	H'FE92 8214	32
VEU2 horizontal FIR filter coefficient Cb/B pixel setting 2	VEUAD2_FCOE_HCB2	R/W	H'FE92 8218	32
VEU2 horizontal FIR filter coefficient Cr/R pixel setting 0	VEUAD2_FCOE_HCR0	R/W	H'FE92 8220	32
VEU2 horizontal FIR filter coefficient Cr/R pixel setting 1	VEUAD2_FCOE_HCR1	R/W	H'FE92 8224	32
VEU2 horizontal FIR filter coefficient Cr/R pixel setting 2	VEUAD2_FCOE_HCR2	R/W	H'FE92 8228	32
VEU2 vertical FIR filter coefficient Y/G pixel setting 0	VEUAD2_FCOE_VY0	R/W	H'FE92 8230	32
VEU2 vertical FIR filter coefficient Y/G pixel setting 1	VEUAD2_FCOE_VY1	R/W	H'FE92 8234	32
VEU2 vertical FIR filter coefficient Y/G pixel setting 2	VEUAD2_FCOE_VY2	R/W	H'FE92 8238	32
VEU2 vertical FIR filter coefficient Cb/B pixel setting 0	VEUAD2_FCOE_VCB0	R/W	H'FE92 8240	32
VEU2 vertical FIR filter coefficient Cb/B pixel setting 1	VEUAD2_FCOE_VCB1	R/W	H'FE92 8244	32
VEU2 vertical FIR filter coefficient Cb/B pixel setting 2	VEUAD2_FCOE_VCB2	R/W	H'FE92 8248	32
VEU2 vertical FIR filter coefficient Cr/R pixel setting 0	VEUAD2_FCOE_VCR0	R/W	H'FE92 8250	32
VEU2 vertical FIR filter coefficient Cr/R pixel setting 1	VEUAD2_FCOE_VCR1	R/W	H'FE92 8254	32
VEU2 vertical FIR filter coefficient Cr/R pixel setting 2	VEUAD2_FCOE_VCR2	R/W	H'FE92 8258	32
VEU2 FIR filter calculation optional setting register	VEUAD2_FCOE_FSWT	R/W	H'FE92 8260	32
VEU2 alpha resize clip threshold setting register	VEUAD2_ALPTH	R/W	H'FE92 8300	32
VEU2 resize clip value setting register	VEUAD2_ALPVAL	R/W	H'FE92 8304	32
VEU3 start register	VE3STR	R/W	H’FE92 C000	32
VEU3 source memory width register	VE3SWR	R/W	H’FE92 C010	32
VEU3 source size register	VE3SSR	R/W	H’FE92 C014	32
VEU3 source address Y register	V3SAYR	R/W	H’FE92 C018	32
VEU3 source address C register	V3SACR	R/W	H’FE92 C01C	32

Register Name	Abbreviation	R/W	Address	Access Size
VEU3 bundle source size register	V3BSSR	R/W	H'FE92 C020	32
VEU3 destination memory width register	VE3DWR	R/W	H'FE92 C030	32
VEU3 destination address Y register	V3DAYR	R/W	H'FE92 C034	32
VEU3 destination address C register	V3DACR	R/W	H'FE92 C038	32
VEU3 transform control register	V3TRCR	R/W	H'FE92 C050	32
VEU3 resize filter control register	V3RFCR	R/W	H'FE92 C054	32
VEU3 resize filter size clip register	V3RFSR	R/W	H'FE92 C058	32
VEU3 enhance register	VE3NHR	R/W	H'FE92 C05C	32
VEU3 resize filter sub control register	V3RSCR	R/W	H'FE92 C064	32
VEU3 resize filter size clip offset register	V3RSOR	R/W	H'FE92 C068	32
VEU3 filter mode control register	V3FMCR	R/W	H'FE92 C070	32
VEU3 vertical tap coefficient register	V3VTCR	R/W	H'FE92 C074	32
VEU3 horizontal tap coefficient register	V3HTCR	R/W	H'FE92 C078	32
VEU3 designated color register	V3APCR	R/W	H'FE92 C080	32
VEU3 conversion color register	VE3CCR	R/W	H'FE92 C084	32
VEU3 fill color specification register	V3FLCR	RW	H'FE92 C088	32
VEU3 address fixed register	V3AFXR	R/W	H'FE92 C090	32
VEU3 swapping register	V3SWPR	R/W	H'FE92 C094	32
VEU3 event interrupt enable register	VE3IER	R/W	H'FE92 C0A0	32
VEU3 event register	VE3VTR	R/W	H'FE92 C0A4	32
VEU3 status register	V3STAR	R	H'FE92 C0B0	32
VEU3 module reset register	V3BSRR	R/W	H'FE92 C0B4	32
VEU3 resize passband register	V3RPBR	R/W	H'FE92 C0C8	32
VEU3 resize interpolation setting register	VEUAD3_RSZ_ITP	R/W	H'FE92 C180	32
VEU3 horizontal FIR filter coefficient Y/G pixel setting 0	VEUAD3_FCOE_HY0	R/W	H'FE92 C200	32
VEU3 horizontal FIR filter coefficient Y/G pixel setting 1	VEUAD3_FCOE_HY1	R/W	H'FE92 C204	32
VEU3 horizontal FIR filter coefficient Y/G pixel setting 2	VEUAD3_FCOE_HY2	R/W	H'FE92 C208	32
VEU3 horizontal FIR filter coefficient Cb/B pixel setting 0	VEUAD3_FCOE_HCB0	R/W	H'FE92 C210	32
VEU3 horizontal FIR filter coefficient Cb/B pixel setting 1	VEUAD3_FCOE_HCB1	R/W	H'FE92 C214	32
VEU3 horizontal FIR filter coefficient Cb/B pixel setting 2	VEUAD3_FCOE_HCB2	R/W	H'FE92 C218	32
VEU3 horizontal FIR filter coefficient Cr/R pixel setting 0	VEUAD3_FCOE_HCR0	R/W	H'FE92 C220	32
VEU3 horizontal FIR filter coefficient Cr/R pixel setting 1	VEUAD3_FCOE_HCR1	R/W	H'FE92 C224	32
VEU3 horizontal FIR filter coefficient Cr/R pixel setting 2	VEUAD3_FCOE_HCR2	R/W	H'FE92 C228	32

Register Name	Abbreviation	R/W	Address	Access Size
VEU3 vertical FIR filter coefficient Y/G pixel setting 0	VEUAD3_FCOE_VY0	R/W	H'FE92 C230	32
VEU3 vertical FIR filter coefficient Y/G pixel setting 1	VEUAD3_FCOE_VY1	R/W	H'FE92 C234	32
VEU3 vertical FIR filter coefficient Y/G pixel setting 2	VEUAD3_FCOE_VY2	R/W	H'FE92 C238	32
VEU3 vertical FIR filter coefficient Cb/B pixel setting 0	VEUAD3_FCOE_VCB0	R/W	H'FE92 C240	32
VEU3 vertical FIR filter coefficient Cb/B pixel setting 1	VEUAD3_FCOE_VCB1	R/W	H'FE92 C244	32
VEU3 vertical FIR filter coefficient Cb/B pixel setting 2	VEUAD3_FCOE_VCB2	R/W	H'FE92 C248	32
VEU3 vertical FIR filter coefficient Cr/R pixel setting 0	VEUAD3_FCOE_VCR0	R/W	H'FE92 C250	32
VEU3 vertical FIR filter coefficient Cr/R pixel setting 1	VEUAD3_FCOE_VCR1	R/W	H'FE92 C254	32
VEU3 vertical FIR filter coefficient Cr/R pixel setting 2	VEUAD3_FCOE_VCR2	R/W	H'FE92 C258	32
VEU3 FIR filter calculation optional setting register	VEUAD3_FCOE_FSWT	R/W	H'FE92 C260	32
VEU3 alpha resize clip threshold setting register	VEUAD3_ALPTH	R/W	H'FE92 C300	32
VEU3 resize clip value setting register	VEUAD3_ALPVAL	R/W	H'FE92 C304	32

G.36 Register Configuration of BEU

Register Name	Abbreviation	R/W	Address (A side)	Address (B side)	Mirror Address	Access size
Start/stop register	BESTR	R/W	H'FE93_0000	—	—	32
Input 1 : source image memory width	BSMWR1	R/W	H'FE93_0010	H'FE93_1010	H'FE93_2010	32
Input 1 : source image size	BSSZR1	R/W	H'FE93_0014	H'FE93_1014	H'FE93_2014	32
Input 1 : source image Y/RGB start address	BSAYR1	R/W	H'FE93_0018	H'FE93_1018	H'FE93_2018	32
Input 1 : source image Cb/Cr start address	BSACR1	R/W	H'FE93_001C	H'FE93_101C	H'FE93_201C	32
Input 1 : source image α start address	BSAAR1	R/W	H'FE93_0020	H'FE93_1020	H'FE93_2020	32
Input 1 : source image format	BSIFR1	R/W	H'FE93_0024	H'FE93_1024	H'FE93_2024	32
Input 2 : source image memory width	BSMWR2	R/W	H'FE93_0028	H'FE93_1028	H'FE93_2028	32

Register Name	Abbreviation	R/W	Address (A side)	Address (B side)	Mirror Address	Access size
Input 2 : source image size	BSSZR2	R/W	H'FE93_002C	H'FE93_102C	H'FE93_202C	32
Input 2 : source image Y/RGB start address	BSAYR2	R/W	H'FE93_0030	H'FE93_1030	H'FE93_2030	32
Input 2 : source image Cb/Cr start address	BSACR2	R/W	H'FE93_0034	H'FE93_1034	H'FE93_2034	32
Input 2 : source image α start address	BSAAR2	R/W	H'FE93_0038	H'FE93_1038	H'FE93_2038	32
Input 2 : source image format	BSIFR2	R/W	H'FE93_003C	H'FE93_103C	H'FE93_203C	32
Input 3 : source image memory width	BSMWR3	R/W	H'FE93_0040	H'FE93_1040	H'FE93_2040	32
Input 3 : source image size	BSSZR3	R/W	H'FE93_0044	H'FE93_1044	H'FE93_2044	32
Input 3 : source image Y/RGB start address	BSAYR3	R/W	H'FE93_0048	H'FE93_1048	H'FE93_2048	32
Input 3 : source image Cb/Cr start address	BSACR3	R/W	H'FE93_004C	H'FE93_104C	H'FE93_204C	32
Input 3 : source image α start address	BSAAR3	R/W	H'FE93_0050	H'FE93_1050	H'FE93_2050	32
Input 3 : source image format	BSIFR3	R/W	H'FE93_0054	H'FE93_1054	H'FE93_2054	32
Tile pattern output size	BTPSR	R/W	H'FE93_0058	H'FE93_1058	H'FE93_2058	32
Blend control	BBLCR1	R/W	H'FE93_0104	—	—	32
Input 1 : blend location	BLOCR1	R/W	H'FE93_0114	H'FE93_1114	H'FE93_2114	32
Input 2 : blend location	BLOCR2	R/W	H'FE93_0118	H'FE93_1118	H'FE93_2118	32
Input 3 : blend location	BLOCR3	R/W	H'FE93_011C	H'FE93_111C	H'FE93_211C	32
BEU output format	BPKFR	R/W	H'FE93_0140	H'FE93_1140	H'FE93_2140	32
Transparency color control	BPCCR0	R/W	H'FE93_0144	H'FE93_1144	H'FE93_2144	32
Input 1 : transparency color control register 1	BPCCR11	R/W	H'FE93_0148	H'FE93_1148	H'FE93_2148	32
Input 1 : transparency color control register 2	BPCCR12	R/W	H'FE93_014C	H'FE93_114C	H'FE93_214C	32

Register Name	Abbreviation	R/W	Address (A side)	Address (B side)	Mirror Address	Access size
Input 2 : transparency color control register 1	BPCCR21	R/W	H'FE93_0150	H'FE93_1150	H'FE93_2150	32
Input 2 : transparency color control register 2	BPCCR22	R/W	H'FE93_0154	H'FE93_1154	H'FE93_2154	32
Input 3 : transparency color control register 1	BPCCR31	R/W	H'FE93_0158	H'FE93_1158	H'FE93_2158	32
Input 3 : transparency color control register 2	BPCCR32	R/W	H'FE93_015C	H'FE93_115C	H'FE93_215C	32
Destination memory width	BDMWR	R/W	H'FE93_0160	H'FE93_1160	H'FE93_2160	32
Destination image Y/RGB start address	BDAYR	R/W	H'FE93_0164	H'FE93_1164	H'FE93_2164	32
Destination image Cb/Cr start address	BDACR	R/W	H'FE93_0168	H'FE93_1168	H'FE93_2168	32
Destination image format	BDPFR	R/W	H'FE93_016C	H'FE93_116C	H'FE93_216C	32
Address fixed	BAFXR	R/W	H'FE93_0180	H'FE93_1180	H'FE93_2180	32
Data swapping control	BSWPR	R/W	H'FE93_0184	H'FE93_1184	H'FE93_2184	32
Event interrupt control	BEIER	R/W	H'FE93_0188	—	—	32
Event flag and clear	BEVTR	R/W	H'FE93_018C	—	—	32
Register side control	BRCNTR	R/W	H'FE93_0194	—	—	32
Status register	BSTAR	R/W	H'FE93_0198	—	—	32
Module reset register	BBRSTR	R/W	H'FE93_019C	—	—	32
Register side forcible setting	BRCHR	R/W	H'FE93_01A0	—	—	32
Input 1 : source image α control	BSASR1	R/W	H'FE93_0224	H'FE93_1224	H'FE93_2224	32
Input 1 : source image α value set	BSAVR1	R/W	H'FE93_0228	H'FE93_1228	H'FE93_2228	32
Input 2 : source image α control	BSASR2	R/W	H'FE93_0264	H'FE93_1264	H'FE93_2264	32
input2 : source image α value set	BSAVR2	R/W	H'FE93_0268	H'FE93_1268	H'FE93_2268	32
Input 3 : source image α control	BSASR3	R/W	H'FE93_02A4	H'FE93_12A4	H'FE93_22A4	32

Register Name	Abbreviation	R/W	Address (A side)	Address (B side)	Mirror Address	Access size
Input 3 : source image α value set	BSAVR3	R/W	H'FE93_02A8	H'FE93_12A8	H'FE93_22A8	32
Blend Unit-A : ROP control	BRCAR	R/W	H'FE93_0350	H'FE93_1350	H'FE93_2350	32
Blend Unit-A : Blend control	BBCAR	R/W	H'FE93_0354	H'FE93_1354	H'FE93_2354	32
Blend Unit-C : ROP control	BRCCR	R/W	H'FE93_0370	H'FE93_1370	H'FE93_2370	32
Blend Unit-C : Blend control	BBCCR	R/W	H'FE93_0374	H'FE93_1374	H'FE93_2374	32
The CLUT area is used on OSD	CLUT	R/W	H'FE93_3000 to H'FE93_33FF	—	—	32

G.37 Register Configuration of VPU5HG

Register Name	Abbreviation	R/W	Address	Access Size
VPU5HG version control register H	VP5_VCRH	R	H'FE90 0000	32
VPU5HG version control register L	VP5_VCRL	R	H'FE90 0004	32
VPU5HG command register	VP5_CMD	R/W	H'FE90 0008	32
VPU5HG overall control register	VP5_CTRL	R/W	H'FE90 000C	32
VPU5HG interrupt control register	VP5_IRQ_ENB	R/W	H'FE90 0010	32
VPU5HG interrupt status register	VP5_IRQ_STA	R/W	H'FE90 0014	32
VPU5HG clock supply control register	VP5_CLK_STOP	R/W	H'FE90 001C	32
VPU5HG status register	VP5_STATUS	R	H'FE90 0020	32
Motion vector count register	VP5_CE_MV_NUM	R	H'FE90 0050	32
Forward reference horizontal motion vector sum register	VP5_CE_MVH_REF0	R	H'FE90 0054	32
Forward reference vertical motion vector sum register	VP5_CE_MVV_REF0	R	H'FE90 0058	32
Backward reference horizontal motion vector sum register	VP5_CE_MVH_REF1	R	H'FE90 005C	32
Backward reference vertical motion vector sum register	VP5_CE_MVV_REF1	R	H'FE90 0060	32
CE microcode base address register	VP5_CE_MBA	R/W	H'FE90 0080	32
CE parameter base address register 0	VP5_CE_PBA0	R/W	H'FE90 0084	32

Register Name	Abbreviation	R/W	Address	Access Size
CE parameter base address register 1	VP5_CE_PBA1	R/W	H'FE90 0088	32
CE error code register	VP5_CE_ERR	R	H'FE90 00C0	32
Intermediate stream bit count register 0	VP5_CE_INT_TB0	R	H'FE90 00C8	32
Intermediate stream bit count register 1	VP5_CE_INT_TB1	R	H'FE90 00CC	32
Macroblock attribute register	VP5_CE_MB_ATTR	R	H'FE90 00D0	32
Macroblock intra-SAD register	VP5_CE_MB_SADA	R	H'FE90 00D4	32
Macroblcok inter-SAD register	VP5_CE_MB_SADR	R	H'FE90 00D8	32
Macroblcok used-SAD register	VP5_CE_MB_USAD	R	H'FE90 00DC	32
Activity total value register	VP5_CE_ASUM	R	H'FE90 00E0	32
Activity register	VP5_CE_ACT	R	H'FE90 00E4	32
Quantization coefficient total value register	VP5_CE_QSUM	R	H'FE90 00E8	32
Virtual buffer register	VP5_CE_DJS	R	H'FE90 00EC	32
MB average luminance total value register	VP5_CE_YSUM	R	H'FE90 00F0	32
VLCS microcode base address register	VP5_VLC_MBA	R/W	H'FE90 0100	32
VLCS parameter base address register 0	VP5_VLC_PBA0	R/W	H'FE90 0104	32
VLCS parameter base address register 1	VP5_VLC_PBA1	R/W	H'FE90 0108	32
Picture byte count register	VP5_VLC_TB	R	H'FE90 0144	32
VLCS status register H	VP5_VLC_ERRH	R	H'FE90 0148	32
VLCS status register L	VP5_VLC_ERRL	R	H'FE90 014C	32
Intermediate stream bit count register 0	VP5_VLC_INT_TB0	R	H'FE90 0150	32
Intermediate stream bit count register 1	VP5_VLC_INT_TB1	R	H'FE90 0154	32

G.37.1 VPU5HG Internal Registers (Set with Initial Routine DMAC Channel 0)

Register Name	Abbreviation	VPU Address	Remarks
Base address array register 0	VP5_BAAR0	H'0014 4000	Refer to table 27.20 for details.
Decode luminance picture DMA channel register 0	VP5_CE_DCHR_DECY0	H'0014 0040	
Decode chrominance picture DMA channel register 0	VP5_CE_DCHR_DECC0	H'0014 0048	
Filter luminance picture DMA channel register 0	VP5_CE_DCHR_DISPY0	H'0014 0050	

Register Name	Abbreviation	VPU Address	Remarks
Filter chrominance picture DMA channel register 0	VP5_CE_DCHR_DISPC0	H'0014 0058	
Reference picture DMA channel register	VP5_CE_DCHR_REF	H'0014 0060	
Encode picture DMA channel register 0	VP5_CE_DCHR_TMP0	H'0014 0068	Set only for encoding which involves one CE
MV information output DMA channel register 0	VP5_CE_DCHR_MVINFO0	H'0014 0090	
Odd MB line MV information output DMA channel register 0	VP5_CE_DCHR_MVINFOB0	H'0014 0098	
Anchor picture MV information DMA channel register 0	VP5_CE_DCHR_MVR0	H'0014 00A0	
Anchor picture odd MB line MV information DMA channel register 0	VP5_CE_DCHR_MVRB0	H'0014 00A8	
CE intermediate stream DMA channel register 0	VP5_CE_DCHR_CEIS0	H'0014 00B0	
CE intermediate control stream DMA channel register 0	VP5_CE_DCHR_CEIC0	H'0014 00B8	
Stream A DMA channel register	VP5_VLC_DCHR_STRA	H'0014 00C0	
Stream B DMA channel register	VP5_VLC_DCHR_STRB	H'0014 00C8	
Command stream DMA channel register	VP5_VLC_DCHR_CMDS	H'0014 00D0	
VLCS data partition DMA channel register	VP5_VLC_DCHR_BPDP	H'0014 00D8	
VLCS intermediate stream DMA channel register 0	VP5_VLC_DCHR_VLIS0	H'0014 00E0	
VLCS intermediate control stream DMA channel register 0	VP5_VLC_DCHR_VLIC0	H'0014 00E8	
VLCS co-location not coded DMA channel register	VP5_VLC_DCHR_CLNC	H'0014 00F0	
VLCS data partition write DMA channel register	VP5_VLC_DCHR_DPW	H'0014 00F8	
GDMAC operation control register	VP5_GDMAC_ARDPRI	H'0014 1008	
GDMAC SHwy arbitration control register	VP5_GDMAC_SHWARBT	H'0014 1038	
CE sequence level control register	VP5_CE_SPAR	H'0000 0000	
CE picture level control register	VP5_CE_PPAR	H'0000 0010	
Reserved register	VP5_CE_ENC_WPRED	H'0000 0050	
Encode control register	VP5_CE_ENC_CTRL	H'0000 0058	
Activity control register	VP5_CE_ACQ_CTRL	H'0000 0060	

Register Name	Abbreviation	VPU Address	Remarks
Intermode judgement control register	VP5_CE_ME_COST	H'0000 0068	
VLCF control register	VP5_CE_VLCF	H'0000 00A0	
Slice size register	VP5_CE_SLC_SIZE	H'0000 00A8	
Target bit rate control register	VP5_CE_TBIT	H'0000 00B0	
Virtual buffer control register	VP5_CE_RCDJ	H'0000 00B8	
Intra refresh control register	VP5_CE_MBRF	H'0000 00C8	
Reverse quantization matrix	VP5_CE_IQMAT	H'003D 0600	EMASK = H'10
Quantization matrix	VP5_CE_QMAT	H'003D 0840	EMASK = H'10
CE intermediate stream 0 buffer size register	VP5_CE_IS_BS0	H'0012 0440	
FME0QNC0 control register	VP5_CE_FME0_QNC0	H'000B 00F0	Set only for encoing which involves one CE
FME0QNC1 control register	VP5_CE_FME0_QNC1	H'000B 80F0	Set only for encoing which involves one CE
TRF0QNC0 control register	VP5_CE_TRF0_QNC0	H'000F 00F0	Set only for encoing which involves one CE
TRF0QNC1 control register	VP5_CE_TRF0_QNC1	H'000F 80F0	Set only for encoing which involves one CE
VLCS sequence level control register	VP5_VLC_SPAR	H'0002 0000	
VLCS slice header register	VP5_VLC_SH	H'0002 8000	
VLCS mode register	VP5_VLC_MODE	H'0002 0F50	
Stream A buffer size register	VP5_VLC_STRA_BS	H'0002 0F80	
Stream B buffer size register	VP5_VLC_STRB_BS	H'0002 0F88	
VLCS intermediate stream 0 buffer size register	VP5_VLC_IS_BS0	H'0002 0FA0	
VLCS intermediate stream 1 buffer size register	VP5_VLC_IS_BS1	H'0002 0FB0	

G.37.2 VPU5HG Internal Registers (Set with Initialization Routine DMAC Channel 1)

Register Name	Abbreviation	VPU Address	Remarks
Base address array register	VP5_BAAR1	H'0034 4000	Refer to table 27.25 for details.
Decode luminance picture DMA channel register 1	VP5_CE_DCHR_DECY1	H'0034 0040	
Decode chrominance picture DMA channel register 1	VP5_CE_DCHR_DECC1	H'0034 0048	
Filter luminance picture DMA channel register 1	VP5_CE_DCHR_DISPY1	H’0034 0050	

Register Name	Abbreviation	VPU Address	Remarks
Filter chrominance picture DMA channel register 1	VP5_CE_DCHR_DISPC1	H'0034 0058	
Encode picture DMA channel register	VP5_CE_DCHR_TMP1	H'0034 0068	
MV information output DMA channel register 1	VP5_CE_DCHR_MVINFO1	H'0034 0090	
Odd MB line MV information output DMA channel register 1	VP5_CE_DCHR_MVINFOB1	H'0034 0098	
Anchor picture MV information DMA channel register 1	VP5_CE_DCHR_MVR1	H'0034 00A0	
Anchor picture odd MB line MV information DMA channel register 1	VP5_CE_DCHR_MVRB1	H'0034 00A8	
CE intermediate stream DMA channel register 1	VP5_CE_DCHR_CEIS1	H'0034 00B0	
CE intermediate control stream DMA channel register 1	VP5_CE_DCHR_CEIC1	H'0034 00B8	
CE intermediate stream 1 buffer size register	VP5_CE_IS_BS1	H'0032 0440	
DEB1LMDMA synchronous register	VP5_CE_DEB_LMDMASR1	H'0030 0050	
VLCS intermediate stream DMA channel register 1	VP5_VLC_DCHR_VLIS1	H'0034 00E0	
VLC intermediate control stream DMA channel register 1	VP5_VLC_DCHR_VLIC1	H'0034 00E8	

G.38 Register Configuration of 2D-DMAC

Register Name	Abbreviation	R/W	Address	Access Size
Interrupt status clear register	CHSTCLR	R/W	H'FEA0 0010	32
CH0 control register	CH0CTRL	R/W	H'FEA0 0020	32
CH1 control register	CH1CTRL	R/W	H'FEA0 0024	32
CH2 control register	CH2CTRL	R/W	H'FEA0 0028	32
CH3 control register	CH3CTRL	R/W	H'FEA0 002C	32
CH4 control register	CH4CTRL	R/W	H'FEA0 0120	32
CH5 control register	CH5CTRL	R/W	H'FEA0 0124	32
CH6 control register	CH6CTRL	R/W	H'FEA0 0128	32
CH7 control register	CH7CTRL	R/W	H'FEA0 012C	32
CH0 input swap register	CH0SWAP	R/W	H'FEA0 0030	32
CH1 input swap register	CH1SWAP	R/W	H'FEA0 0034	32
CH2 input swap register	CH2SWAP	R/W	H'FEA0 0038	32
CH3 input swap register	CH3SWAP	R/W	H'FEA0 003C	32
CH4 input swap register	CH4SWAP	R/W	H'FEA0 0130	32
CH5 input swap register	CH5SWAP	R/W	H'FEA0 0134	32

Register Name	Abbreviation	R/W	Address	Access Size
CH6 input swap register	CH6SWAP	R/W	H'FEA0 0138	32
CH7 input swap register	CH7SWAP	R/W	H'FEA0 013C	32
CH0 source address register	CH0SAR	R/W	H'FEA0 0080	32
CH0 destination address register	CH0DAR	R/W	H'FEA0 0084	32
CH0 destination pixel register	CH0DPXL	R/W	H'FEA0 0088	32
CH0 source format register	CH0SFMT	R/W	H'FEA0 008C	32
CH0 destination format register	CH0DFMT	R/W	H'FEA0 0090	32
CH0 source line address register	CH0SARE	R	H'FEA0 0094	32
CH0 destination line address register	CH0DARE	R	H'FEA0 0098	32
CH0 destination pixel processing register	CH0DPXLE	R	H'FEA0 009C	32
CH1****	CH1****	-	H'FEA0 00A0 to H'FEA0 00BC	32
CH2****	CH2****	-	H'FEA0 00C0 to H'FEA0 00DC	32
CH3****	CH3****	-	H'FEA0 00E0 to H'FEA0 00FC	32
CH4****	CH4****	-	H'FEA0 0180 to H'FEA0 019C	32
CH5****	CH5****	-	H'FEA0 01A0 to H'FEA0 01BC	32
CH6****	CH6****	-	H'FEA0 01C0 to H'FEA0 01DC	32
CH7****	CH7****	-	H'FEA0 01E0 to H'FEA0 01FC	32

G.39 Register Configuration of MERAM

Register Name	Abbreviation	R/W	Address	Access Size
ICB control register 0	MEVCR0	R/W	H'E550 0000	32
ICB control register 1	MEVCR1	R/W	H'E550 0004	32
ICB transfer end interrupt set register 0	METEIE0	R/W	H'E550 0008	32
ICB transaction error interrupt control register 0	MEILIE0	R/W	H'E550 000C	32
ICB active status register 0	MEACTST0	R/W	H'E550 0010	32
ICB transfer end status register 0	METEST0	R/W	H'E550 0014	32
ICB write transaction error status register	MEILWST	R/W	H'E550 0018	32
ICB read transaction error status register	MEILRST	R/W	H'E550 001C	32

Register Name	Abbreviation	R/W	Address	Access Size
ICB request queue priority select register 1	MEQSEL1	R/W	H'E550 0040	32
ICB request queue priority select register 2	MEQSEL2	R/W	H'E550 0044	32
Extended ICB active status register 1	MEACTST1	R/W	H'E550 0050	32
Extended ICB transaction error status register1	MEILST1	R/W	H'E550 0054	32
Extended ICB transfer end status register 1	METEST1	R/W	H'E550 0058	32
Extended ICB transfer end interrupt set register 1	METEIE1	R/W	H'E550 005C	32
Extended ICB active status register 2	MEACTST2	R/W	H'E550 0060	32
Extended ICB transaction error status register 2	MEILST2	R/W	H'E550 0064	32
Extended ICB transfer end status register 2	METEST2	R/W	H'E550 0068	32
Extended ICB transaction error interrupt set register 2	METEIE2	R/W	H'E550 006C	32
Extended ICB active status register 3	MEACTST3	R/W	H'E550 0070	32
Extended ICB transaction error status register 3	MEILST3	R/W	H'E550 0074	32
Extended ICB transfer end status register 3	METEST3	R/W	H'E550 0078	32
Extended ICB transaction error interrupt set register 3	METEIE3	R/W	H'E550 007C	32
ICB00 buffer control register	ME00CTRL	R/W	H'E550 0400	32
ICB00 frame size register	ME00BSIZE	R/W	H'E550 0404	32
ICB00 MERAM set register	ME00MCNF	R/W	H'E550 0408	32
ICB00 reserved	-	R	H'E550 040C	32
ICB00 external memory start address register A	ME00SSARA	R/W	H'E550 0410	32
ICB00 external memory start address register B	ME00SSARB	R/W	H'E550 0414	32
ICB00 external memory buffer size register	ME00SBSIZE	R/W	H'E550 0418	32
ICB00 reserved	-	R	H'E550 041C	32
ICBnn buffer control register (nn = 01 to 31)	MEnnCTRL	R/W	H'E550 0400 + H'0020 * nn	32
ICBnn frame size register (nn = 01 to 31)	MEnnBSIZE	R/W	H'E550 0404 + H'0020 * nn	32
ICBnn MERAM set register (nn = 01 to 31)	MEnnMCNF	R/W	H'E550 0408 + H'0020 * nn	32
ICBnn external memory start address register A (nn = 01 to 31)	MEnnSSARA	R/W	H'E550 0410 + H'0020 * nn	32

Register Name	Abbreviation	R/W	Address	Access Size
ICBnn external memory start address register B (nn = 01 to 31)	MEnnSSARB	R/W	H'E550 0414 + H'0020 * nn	32
ICBnn external memory buffer size register (nn = 01 to 31)	MEnnSBSIZE	R/W	H'E550 0418 + H'0020 * nn	32
Extended ICBnn buffer control register (nn = 32 to 127)	MEnnCTRL	R/W	H'E550 0400 + H'0020 * nn	32
Extended ICBnn frame size register (nn = 32 to 127)	MEnnBSIZE	R/W	H'E550 0404 + H'0020 * nn	32
Extended ICBnn MERAM set register (nn = 32 to 127)	MEnnMCNF	R/W	H'E550 0408 + H'0020 * nn	32
Extended ICBnn external memory start address register A (nn = 32 to 127)	MEnnSSARA	R/W	H'E550 0410 + H'0020 * nn	32
Extended ICBnn external memory start address register B (nn = 32 to 127)	MEnnSSARB	R/W	H'E550 0414 + H'0020 * nn	32
Extended ICBnn external memory buffer size register (nn = 32 to 127)	MEnnSBSIZE	R/W	H'E550 0418 + H'0020 *nn	32
MERAM direct access space	-	R/W	H'E558 0000 to H'E56F FFFF	8/16/32

Note: Any address from H'E800 0000 to H'E81F FFFF is also accessible as a mirror address. However, when making an access from the AP-Realtime (AP-RT) Core, only the mirror address range is accessible.

G.39.1 Register Configuration of LCD Refresh Controller

Register Name	Abbreviation	R/W	Address	Access Size
LCD refresh control register	LRCTRL	R/W	H'FE94 8000	32
LCD refresh interrupt enable register	LRIER	R/W	H'FE94 8004	32
LCD refresh interrupt source register	LRISR	R/W	H'FE94 8008	32
LCD refresh status register	LRSR	R/W	H'FE94 800C	32
MERAM operation mode set register	LRLPRSR	R/W	H'FE94 8014	32
LCD refresh interrupt address register 1	LRIAR1	R/W	H'FE94 8018	32
LCD refresh interrupt address register 2	LRIAR2	R/W	H'FE94 801C	32

Register Name	Abbreviation	R/W	Address	Access Size
LCD refresh extended address register 2	LRXAR2	R/W	H'FE94 8024	32
LCD refresh memory boundary address register 1	LRMAR1	R/W	H'FE94 8028	32
LCD refresh memory boundary address register 2	LRMAR2	R/W	H'FE94 802C	32
External access control register	LREBUFC	R/W	H'FE94 8030	32
External access read buffer allocation register	LREBUFP	R/W	H'FE94 8034	32
External access address map register 80	LREMAP80	R/W	H'FE94 8040	32
External access address map register 88	LREMAP88	R/W	H'FE94 8044	32
External access address map register 90	LREMAP90	R/W	H'FE94 8048	32
External access address map register 98	LREMAP98	R/W	H'FE94 804C	32
External access address map register A0	LREMAPA0	R/W	H'FE94 8050	32
External access address map register A8	LREMAPA8	R/W	H'FE94 8054	32
External access address map register B0	LREMAPB0	R/W	H'FE94 8058	32
External access address map register B8	LREMAPB8	R/W	H'FE94 805C	32
Virtual MERAM0A allocation register	LRPG0A	R/W	H'FE94 8080	32
Virtual MERAM0A external memory address register	LRSD0A	R/W	H'FE94 8084	32
Virtual MERAM0B allocation register	LRPG0B	R/W	H'FE94 8088	32
Virtual MERAM0B external memory address register	LRSD0B	R/W	H'FE94 808C	32
Virtual MERAM1A allocation register	LRPG1A	R/W	H'FE94 8090	32
Virtual MERAM1A external memory address register	LRSD1A	R/W	H'FE94 8094	32
Virtual MERAM1B allocation register	LRPG1B	R/W	H'FE94 8098	32
Virtual MERAM1B external memory address register	LRSD1B	R/W	H'FE94 809C	32
Virtual MERAM2A allocation register	LRPG2A	R/W	H'FE94 80A0	32
Virtual MERAM2A external memory address register	LRSD2A	R/W	H'FE94 80A4	32
Virtual MERAM2B allocation register	LRPG2B	R/W	H'FE94 80A8	32
Virtual MERAM2B external memory address register	LRSD2B	R/W	H'FE94 80AC	32
Virtual MERAM3A allocation register	LRPG3A	R/W	H'FE94 80B0	32
Virtual MERAM3A external memory address register	LRSD3A	R/W	H'FE94 80B4	32

Register Name	Abbreviation	R/W	Address	Access Size
Virtual MERAM3B allocation register	LRPG3B	R/W	H'FE94 80B8	32
Virtual MERAM3B external memory address register	LRSD3B	R/W	H'FE94 80BC	32

G.40 Register Configuration of LCDC

Register Name	Abbreviation	R/W	Address (Set A/current)	Address (Set B/program)	Mirror Address	Access Size
LCDC palette data registers 00 to FF	LDPR00 to LDPRFF	R/W	H'FE94 0000 to H'FE94 03FC	-	-	32
LCD dot clock pattern set register 1	MLDDCKPAT1R	R/W	H'FE94 0400	-	-	32
LCD dot clock pattern set register 2	MLDDCKPAT2R	R/W	H'FE94 0404	-	-	32
LCDC dot clock register	LDDCKR	R/W	H'FE94 0410	-	-	32
Dot clock stop register	LDDCKSTPR	R/W	H'FE94 0414	-	-	32
LCD module type register 1	MLDMT1R	R/W	H'FE94 0418	H'FE94 1418	H'FE94 2418	32
LCD module type register 2	MLDMT2R	R/W	H'FE94 041C	H'FE94 141C	H'FE94 241C	32
LCD module type register 3	MLDMT3R	R/W	H'FE94 0420	H'FE94 1420	H'FE94 2420	32
LCD data format register	MLDDFR	R/W	H'FE94 0424	H'FE94 1424	H'FE94 2424	32
LCD scan mode register 1	MLDSM1R	R/W	H'FE94 0428	H'FE94 1428	H'FE94 2428	32
LCD scan mode register 2	MLDSM2R	R/W	H'FE94 042C	-	-	32
LCD display data read start address register 1	MLDSA1R	R/W	H'FE94 0430	H'FE94 1430	H'FE94 2430	32
LCD display data read start address register 2	MLDSA2R	R/W	H'FE94 0434	H'FE94 1434	H'FE94 2434	32
LCD display data storing memory line size register	MLDMLSR	R/W	H'FE94 0438	H'FE94 1438	H'FE94 2438	32
LCD write-back data format register	MLDWBFR	R/W	H'FE94 043C	H'FE94 143C	H'FE94 243C	32

Register Name	Abbreviation	R/W	Address (Set A/current)	Address (Set B/program)	Mirror Address	Access Size
LCD write-back control register	MLDWBCNTR	R/W	H'FE94 0440	H'FE94 1440	H'FE94 2440	32
LCD write-back start address register	MLDWBAR	R/W	H'FE94 0444	H'FE94 1444	H'FE94 2444	32
LCD horizontal character number register	MLDHCNR	R/W	H'FE94 0448	H'FE94 1448	H'FE94 2448	32
LCD horizontal sync signal register	MLDHSYNR	R/W	H'FE94 044C	H'FE94 144C	H'FE94 244C	32
LCD vertical line number register	MLDVLNR	R/W	H'FE94 0450	H'FE94 1450	H'FE94 2450	32
LCD vertical sync signal register	MLDVSYNR	R/W	H'FE94 0454	H'FE94 1454	H'FE94 2454	32
LCD horizontal partial display register	MLDHPDR	R/W	H'FE94 0458	H'FE94 1458	H'FE94 2458	32
LCD vertical partial display register	MLDVPDR	R/W	H'FE94 045C	H'FE94 145C	H'FE94 245C	32
LCD power management register	MLDPMR	R/W	H'FE94 0460	-	-	32
LCDC palette control register	LDPALCR	R/W	H'FE94 0464	-	-	32
LCDC interrupt register	LDINTR	R/W	H'FE94 0468	-	-	32
LCDC status register	LDSR	R	H'FE94 046C	-	-	32
LCDC control register 1	LDCNT1R	R/W	H'FE94 0470	-	-	32
LCDC control register 2	LDCNT2R	R/W	H'FE94 0474	-	-	32
LCDC register set change control register	LDRCNTR	R/W	H'FE94 0478	-	-	32
LCDC input image data swap register	LDDDSR	R/W	H'FE94 047C	-	-	32
LCDC register set forcible select register	LDRCR	R/W	H'FE94 0484	-	-	32
Tabular mode register	LDDBSLMR	R/W	H’FE94_0490	-	-	32
Horizontal slide number register	LDSLHPNR	R/W	H’FE94_0494	-	-	32
Vertical slide number register	LDSLVLNR	R/W	H’FE94_0498	-	-	32

Register Name	Abbreviation	R/W	Address (Set A/current)	Address (Set B/program)	Mirror Address	Access Size
Slide data register	LDSLRGBR	R/W	H’FE94_049C	-	-	32
LCD horizontal sync signal adjust register	MLDHAJR	R/W	H’FE94 04A0	H'FE94 14A0	H’FE94 24A0	32
LCD vertical sync signal delay register	MLDIVSNR	R/W	H’FE94 04A4	-	-	32
LCDC driver write data register 0	LDDWD0R	R/W	H'FE94 0800	-	-	32
LCDC driver write data register 1	LDDWD1R	R/W	H'FE94 0804	-	-	32
LCDC driver write data register 2	LDDWD2R	R/W	H'FE94 0808	-	-	32
LCDC driver write data register 3	LDDWD3R	R/W	H'FE94 080C	-	-	32
LCDC driver write data register 4	LDDWD4R	R/W	H'FE94 0810	-	-	32
LCDC driver write data register 5	LDDWD5R	R/W	H'FE94 0814	-	-	32
LCDC driver write data register 6	LDDWD6R	R/W	H'FE94 0818	-	-	32
LCDC driver write data register 7	LDDWD7R	R/W	H'FE94 081C	-	-	32
LCDC driver write data register 8	LDDWD8R	R/W	H'FE94 0820	-	-	32
LCDC driver write data register 9	LDDWD9R	R/W	H'FE94 0824	-	-	32
LCDC driver write data register A	LDDWDAR	R/W	H'FE94 0828	-	-	32
LCDC driver write data register B	LDDWDBR	R/W	H'FE94 082C	-	-	32
LCDC driver write data register C	LDDWDCR	R/W	H'FE94 0830	-	-	32
LCDC driver write data register D	LDDWDDR	R/W	H'FE94 0834	-	-	32
LCDC driver write data register E	LDDWDER	R/W	H'FE94 0838	-	-	32
LCDC driver write data register F	LDDWDFR	R/W	H'FE94 083C	-	-	32
LCDC driver read data register	LDDRDR	R/W	H'FE94 0840	-	-	32
LCDC driver write access register	LDDWAR	R/W	H'FE94 0900	-	-	32
LCDC driver read access register	LDDRAR	R/W	H'FE94 0904	-	-	32

Register Name	Abbreviation	R/W	Address (Set A/current)	Address (Set B/program)	Mirror Address	Access Size
LCDC coefficient RGB register for color management matrix R	LDCMRKRGBR	R/W	H'FE94 0A00	H'FE94 1A00	H'FE94 2A00	32
LCDC coefficient CMY register for color management matrix R	LDCMRKCMYR	R/W	H'FE94 0A04	H'FE94 1A04	H'FE94 2A04	32
LCDC coefficient of hue circle register for color management matrix R	LDCMRK1R	R/W	H'FE94 0A08	H'FE94 1A08	H'FE94 2A08	32
LCDC coefficient of hue circle register for color management matrix R	LDCMRK2R	R/W	H'FE94 0A0C	H'FE94 1A0C	H'FE94 2A0C	32
LCDC coefficient RGB register for color management matrix G	LDCMGKRGBR	R/W	H'FE94 0A10	H'FE94 1A10	H'FE94 2A10	32
LCDC coefficient CMY register for color management matrix G	LDCMGKCMYR	R/W	H'FE94 0A14	H'FE94 1A14	H'FE94 2A14	32
LCDC coefficient of hue circle register 1 for color management matrix G	LDCMGK1R	R/W	H'FE94 0A18	H'FE94 1A18	H'FE94 2A18	32
LCDC coefficient of hue circle register 2 for color management matrix G	LDCMGK2R	R/W	H'FE94 0A1C	H'FE94 1A1C	H'FE94 2A1C	32
LCDC coefficient RGB register for color management matrix B	LDCMBKRGBR	R/W	H’FE94 0A20	H’FE94 1A20	H’FE94 2A20	32
LCDC coefficient CMY register for color management matrix B	LDCMBKCMYR	R/W	H’FE94 0A24	H’FE94 1A24	H’FE94 2A24	32

Register Name	Abbreviation	R/W	Address (Set A/current)	Address (Set B/program)	Mirror Address	Access Size
LCDC coefficient of hue circle register 1 for color management matrix B	LDCMBK1R	R/W	H'FE94 0A28	H'FE94 1A28	H'FE94 2A28	32
LCDC coefficient of hue circle register 2 for color management matrix B	LDCMBK2R	R/W	H'FE94 0A2C	H'FE94 1A2C	H'FE94 2A2C	32
LCDC peak correction coefficient of hue circle register 1 for color management	LDCMHKPR	R/W	H'FE94 0A30	H'FE94 1A30	H'FE94 2A30	32
LCDC peak correction coefficient of hue circle register 2 for color management	LDCMHKQR	R/W	H'FE94 0A34	H'FE94 1A34	H'FE94 2A34	32
LCDC multiplier coefficient select register for color management	LDCMSELR	R/W	H'FE94 0A38	H'FE94 1A38	H'FE94 2A38	32
LCDC color saturation improvement for color management	LDCMTVR	R/W	H'FE94 0A3C	H'FE94 1A3C	H'FE94 2A3C	32
LCDC color saturation improvement select for color management	LDCMTVSELR	R/W	H'FE94 0A40	H'FE94 1A40	H'FE94 2A40	32
LCDC coefficient dither register for color management	LDCMDTHR	R/W	H'FE94 0A44	H'FE94 1A44	H'FE94 2A44	32
LCDC control register for color management	LDCMCNTR	R/W	H'FE94 0A48	H'FE94 1A48	H'FE94 2A48	32
LCDC control register for color palette expander	LDPALECR	R/W	H'FE940A50	H'FE94 1A50	H'FE94 2A50	32

Register Name	Abbreviation	R/W	Address (Set A/current)	Address (Set B/program)	Mirror Address	Access Size
LCDC color palette data start address register	LDPALADD	R/W	H'FE940A54	H'FE94 1A54	H'FE94 2A54	32
blend control register	LDBCR	R/W	H'FE940B00	-	-	32
CH 1 source image format register	LDB1BSIFR	*1	H'FE94 0B20	H'FE94 1B20	H'FE94 2B20	32
CH 1 source size register	LDB1BSSZR	*1	H'FE94 0B24	H'FE94 1B24	H'FE94 2B24	32
CH 1 blend location register	LDB1BLOCR	*1	H'FE94 0B28	H'FE94 1B28	H'FE94 2B28	32
CH 1 source memory width register	LDB1BSMWR	*1	H'FE94 0B2C	H'FE94 1B2C	H'FE94 2B2C	32
CH 1 source address Y register	LDB1BSARY	*1	H'FE94 0B30	H'FE94 1B30	H'FE94 2B30	32
CH 1 source address C register	LDB1BSARC	*1	H'FE94 0B34	H'FE94 1B34	H'FE94 2B34	32
CH 1 source address α register	LDB1BSARA	*1	H'FE94 0B38	H'FE94 1B38	H'FE94 2B38	32
CH 1 penetration color control register	LDB1BPPCR	*1	H'FE94 0B3C	H'FE94 1B3C	H'FE94 2B3C	32
CH 1 back ground color register	LDB1BBGCL	*1	H'FE94 0B10	H'FE94 1B10	H'FE94 2B10	32
CH 2 source image format register	LDB2BSIFR	*1	H'FE94 0B40	H'FE94 1B40	H'FE94 2B40	32
CH 2 source size register	LDB2BSSZR	*1	H'FE94 0B44	H'FE94 1B44	H'FE94 2B44	32
CH 2 blend location register	LDB2BLOCR	*1	H'FE94 0B48	H'FE94 1B48	H'FE94 2B48	32
CH 2 source memory width register	LDB2BSMWR	*1	H'FE94 0B4C	H'FE94 1B4C	H'FE94 2B4C	32
CH 2 source address Y register	LDB2BSARY	*1	H'FE94 0B50	H'FE94 1B50	H'FE94 2B50	32
CH 2 source address C register	LDB2BSARC	*1	H'FE94 0B54	H'FE94 1B54	H'FE94 2B54	32
CH 2 source address α register	LDB2BSARA	*1	H'FE94 0B58	H'FE94 1B58	H'FE94 2B58	32
CH 2 penetration color control register	LDB2BPPCR	*1	H'FE94 0B5C	H'FE94 1B5C	H'FE94 2B5C	32
CH 2 back ground color register	LDB2BBGCL	*1	H'FE94 0B14	H'FE94 1B14	H'FE94 2B14	32
CH 3 source image format register	LDB3BSIFR	*1	H'FE94 0B60	H'FE94 1B60	H'FE94 2B60	32

Register Name	Abbreviation	R/W	Address (Set A/current)	Address (Set B/program)	Mirror Address	Access Size
CH 3 source size register	LDB3BSSZR	*1	H'FE94 0B64	H'FE94 1B64	H'FE94 2B64	32
CH 3 blend location register	LDB3BLOCR	*1	H'FE94 0B68	H'FE94 1B68	H'FE94 2B68	32
CH 3 source memory width register	LDB3BSMWR	*1	H'FE94 0B6C	H'FE94 1B6C	H'FE94 2B6C	32
CH 3 source address Y register	LDB3BSARY	*1	H'FE94 0B70	H'FE94 1B70	H'FE94 2B70	32
CH 3 source address C register	LDB3BSARC	*1	H'FE94 0B74	H'FE94 1B74	H'FE94 2B74	32
CH 3 source address α register	LDB3BSARA	*1	H'FE94 0B78	H'FE94 1B78	H'FE94 2B78	32
CH 3 penetration color control register	LDB3BPPCR	*1	H'FE94 0B7C	H'FE94 1B7C	H'FE94 2B7C	32
CH 3 back ground color register	LDB3BBGCL	*1	H'FE94 0B18	H'FE94 1B18	H'FE94 2B18	32
CH 4 source image format register	LDB4BSIFR	*1	H'FE94 0B80	H'FE94 1B80	H'FE94 2B80	32
CH 4 source size register	LDB4BSSZR	*1	H'FE94 0B84	H'FE94 1B84	H'FE94 2B84	32
CH 4 blend location register	LDB4BLOCR	*1	H'FE94 0B88	H'FE94 1B88	H'FE94 2B88	32
CH 4 source memory width register	LDB4BSMWR	*1	H'FE94 0B8C	H'FE94 1B8C	H'FE94 2B8C	32
CH 4 source address Y register	LDB4BSARY	*1	H'FE94 0B90	H'FE94 1B90	H'FE94 2B90	32
CH 4 source address C register	LDB4BSARC	*1	H'FE94 0B94	H'FE94 1B94	H'FE94 2B94	32
CH 4 source address α register	LDB4BSARA	*1	H'FE94 0B98	H'FE94 1B98	H'FE94 2B98	32
CH 4 penetration color control register	LDB4BPPCR	*1	H'FE94 0B9C	H'FE94 1B9C	H'FE94 2B9C	32
CH 4 back ground color register	LDB4BBGCL	*1	H'FE94 0B1C	H'FE94 1B1C	H'FE94 2B1C	32

*1 the program and mirror are R/W, the current is R/O

Note: The address of LCDC0 register : H'FE940000 - H'FE943FFF
The address of LCDC1 register : H'FE944000 - H'FE947FFF

G.41 Register Configuration of CSI2

G.41.1 Register Configuration of CSI2C

Register Name	Abbreviation	R/W	Address	Access Size
Control timing select register	CSI2_TREF	R/W	H'FFC9 0000	32
Software reset register	CSI2_SRST	R/W	H'FFC9 0004	32
PHY operation control register	CSI2_PHYCNT	R/W	H'FFC9 0008	32
Checksum control register	CSI2_CHKSUM	R/W	H'FFC9 000C	32
Channel data type select register	CSI2_VCDT	R/W	H'FFC9 0010	32
Embedded Data capture control register	CSI2_CAP	R/W	H'FFC9 0018	32
Field detect control register	CSI2_FLD	R/W	H'FFC9 001C	32
Monitor control register	CSI2_MONCNT	R/W	H'FFC9 0020	32
Output control register	CSI2_OUT	R/W	H'FFC9 0024	32
Long DataType setting register0	CSI2LNGDT0	R/W	H'FFC9 0028	32
Long DataType setting register1	CSI2LNGDT1	R/W	H'FFC9 002C	32
Interrupt enable register	CSI2_INTEN	R/W	H'FFC9 0030	32
Interrupt status monitor register	CSI2_INTSTATE	R/W	H'FFC9 0038	32
Short packet data register	CSI2SHPDAT	R	H'FFC9 0040	32
Short packet count register	CSI2SHPCNT	R	H'FFC9 0044	32
Direct dump control register 1	CSI2DDCNT1	R/W	H'FFC9 0050	32
Destination address register 1A	CSI2DESTADR1A	R/W	H'FFC9 0060	32
Destination address register 1B	CSI2DESTADR1B	R/W	H'FFC9 0064	32
Destination space width register 1	CSI2DESTWDT1	R/W	H'FFC9 0068	32
Direct dump reload register 1	CSI2DDRLD1	R/W	H'FFC9 006C	32
Embedded Data receive byte count register	CSI2_EBDBCUNT	R/W	H'FFC9 0154	32
Embedded Data monitor register	CSI2_EBDMON0 to 2047	R	H'FFC9 2000 to H'FFC9 3FFC	32

G.41.2 Register Configuration of CSI2I

Register Name	Abbreviation	R/W	Address	Access Size
Control timing select register	CSI2I_TREF	R/W	H'FE8F 7000	32
Software reset register	CSI2I_SRST	R/W	H'FE8F 7004	32
PHY operation control register1	CSI2I_PHYCNT1	R/W	H'FE8F 7008	32
Control register1	CSI2I_CNT1	R/W	H'FE8F 7020	32
Pixel size register	CSI2I_SIZE	R/W	H'FE8F 7024	32
Control register2	CSI2I_CNT2	R/W	H'FE8F 7060	32
Field detect control register	CSI2I_FLD	R/W	H'FE8F 7064	32
Interrupt clear register	CSI2I_INTCLR	R/W	H'FE8F 7070	32
Interrupt enable register	CSI2I_INTEN	R/W	H'FE8F 7074	32

Register Name	Abbreviation	R/W	Address	Access Size
Interrupt monitor register	CSI2I_INTMON	R/W	H'FE8F 707C	32

G.42 Register Configuration of DSI

Register name	Abbreviation	R/W	Address	Access Size
System Control Register	SYSCTRL	R/W	H'FFC60000	32
System Configuration Register	SYSCONF	R/W	H'FFC60004	32
Transition Timing Parameter Setting Register	TIMSET	R/W	H'FFC60008	32
Transmission Packet Type Setting Register 0	PTYPESET0	R/W	H'FFC60010	32
Transmission Packet Type Setting Register 1	PTYPESET1	R/W	H'FFC60014	32
Response Request Setting Register 0	RESREQSET0	R/W	H'FFC60018	32
Response Request Setting Register 1	RESREQSET1	R/W	H'FFC6001C	32
HS Transmission Time-out Setting Register	HSTTOVSET	R/W	H'FFC60020	32
LP Reception Time-out Setting Register	LPRTOVSET	R/W	H'FFC60024	32
Turn Around Time-out Setting Register	TATOVSET	R/W	H'FFC60028	32
Peripheral Reset Time-out Value Setting Register	PRTOVSET	R/W	H'FFC6002C	32
DSI-LINK Control Register	DSICTRL	R/W	H'FFC60030	32
Reception Packet Type Setting Register 0	RPTYPESET0	R/W	H'FFC60038	32
Reception Packet Type Setting Register 1	RPTYPESET1	R/W	H'FFC6003C	32
DSI-LINK Status Register	DSIS	R	H'FFC60040	32
DSI-LINK Interrupt Status Register	DSIINT	R/W	H'FFC60050	32
DSI-LINK Interrupt Enable Register	DSIINTE	R/W	H'FFC60060	32
PHY Control Register	PHYCTRL	R/W	H'FFC60070	32
DSI-L-Bridge Control Register	DTCTR	R/W	H'FFC68000	32
DSI-L-Bridge Status Register	DTST	R	H'FFC68004	32
DSI-L-Bridge Status Clear Register	DTSTCL	R/W	H'FFC68008	32
DSI-L-Bridge Interrupt Enable Register	DTIRQEN	R/W	H'FFC6800C	32
Video Mode Control Register 1	VMCTR1	R/W	H'FFC68020	32
Video Mode Control Register 2	VMCTR2	R/W	H'FFC68024	32
Video Mode Data Length Register 1	VMLEN1	R/W	H'FFC68028	32
Video Mode Data Length Register 2	VMLEN2	R/W	H'FFC6802C	32

Register name	Abbreviation	R/W	Address	Access Size
Video Mode Data Length Register 3	VMLEN3	R/W	H'FFC68030	32
Video Mode Data Length Register 4	VMLEN4	R/W	H'FFC68034	32
Video Mode Short Packet Data Register 1	VMSDAT1	R/W	H'FFC68038	32
Video Mode Short Packet Data Register 2	VMSDAT2	R/W	H'FFC6803C	32
Command Mode Reception Control Register	CMRCTR	R/W	H'FFC68040	32
Command Mode Reception Data Register	CMRDAT	R	H'FFC68044	32
Command Mode Reception Header Register	CMRHEAD	R	H'FFC68048	32
Tearing Effect Request Register	CMRTEREQ	R/W	H'FFC6804C	32
Command Mode Transmission Long Packet Request CH0 Register	CMTLNGREQ0	R/W	H'FFC68060	32
Command Mode Transmission Long Packet Request CH1 Register	CMTLNGREQ1	R/W	H'FFC68064	32
Command Mode Transmission Long Packet Request CH2 Register	CMTLNGREQ2	R/W	H'FFC68068	32
Command Mode Transmission Long Packet Request CH3 Register	CMTLNGREQ3	R/W	H'FFC6806C	32
Command Mode Transmission Short Packet Request Register	CMTSRTREQ	R/W	H'FFC68070	32
Command Mode Transmission Initiator Address CH0 Register	CMTIADR0	R/W	H'FFC68080	32
Command Mode Transmission Initiator Address CH1 Register	CMTIADR1	R/W	H'FFC68084	32
Command Mode Transmission Initiator Address CH2 Register	CMTIADR2	R/W	H'FFC68088	32
Command Mode Transmission Initiator Address CH3 Register	CMTIADR3	R/W	H'FFC6808C	32
Command Mode Transmission Initiator Total Data CH0 Register	CMTITTL0	R/W	H'FFC68090	32
Command Mode Transmission Initiator Total Data CH1 Register	CMTITTL1	R/W	H'FFC68094	32
Command Mode Transmission Initiator Total Data CH2 Register	CMTITTL2	R/W	H'FFC68098	32
Command Mode Transmission Initiator Total Data CH3 Register	CMTITTL3	R/W	H'FFC6809C	32
Command Mode Transmission Initiator Address Increment CH0 Register	CMTIADRI0	R/W	H'FFC680A0	32
Command Mode Transmission Initiator Address Increment CH1 Register	CMTIADRI1	R/W	H'FFC680A4	32

Register name	Abbreviation	R/W	Address	Access Size
Command Mode Transmission Initiator Address Increment CH2 Register	CMTIADRI2	R/W	H'FFC680A8	32
Command Mode Transmission Initiator Address Increment CH3 Register	CMTIADRI3	R/W	H'FFC680AC	32
Command Mode Transmission Initiator Repeat Number CH0 Register	CMTIRN0	R/W	H'FFC680B0	32
Command Mode Transmission Initiator Repeat Number CH1Register	CMTIRN1	R/W	H'FFC680B4	32
Command Mode Transmission Initiator Repeat Number CH2 Register	CMTIRN2	R/W	H'FFC680B8	32
Command Mode Transmission Initiator Repeat Number CH3 Register	CMTIRN3	R/W	H'FFC680BC	32
Command Mode Transmission Long Packet Control CH0 Register	CMTLNGCTR0	R/W	H'FFC680C0	32
Command Mode Transmission Long Packet Control CH1 Register	CMTLNGCTR1	R/W	H'FFC680C4	32
Command Mode Transmission Long Packet Control CH2 Register	CMTLNGCTR2	R/W	H'FFC680C8	32
Command Mode Transmission Long Packet Control CH3 Register	CMTLNGCTR3	R/W	H'FFC680CC	32
Command Mode Transmission Short Packet Control Register	CMTSRTCTR	R/W	H'FFC680D0	32
Command Mode Transmission Long Packet Data Type CH0 Register	CMTLNGDT0	R/W	H'FFC680E0	32
Command Mode Transmission Long Packet Data Type CH1 Register	CMTLNGDT1	R/W	H'FFC680E4	32
Command Mode Transmission Long Packet Data Type CH2 Register	CMTLNGDT2	R/W	H'FFC680E8	32
Command Mode Transmission Long Packet Data Type CH3 Register	CMTLNGDT3	R/W	H'FFC680EC	32

G.43 Register Configuration of JPU

Register Name	Abbreviation	R/W	Address	Access Size
JPEG code mode register	JCMOD	R/W	H'FE98 0000	32
JPEG code command register	JCCMD	R/W	H'FE98 0004	32
JPEG code status register	JCSTS	R	H'FE98 0008	32

Register Name	Abbreviation	R/W	Address	Access Size
JPEG code quantization table number register	JCQTN	R/W	H'FE98 000C	32
JPEG code Huffman table number register	JCHTN	R/W	H'FE98 0010	32
JPEG code DRI upper register	JCDRIU	R/W	H'FE98 0014	32
JPEG code DRI lower register	JCDRID	R/W	H'FE98 0018	32
JPEG code vertical size upper register	JCVSZU	R/W	H'FE98 001C	32
JPEG code vertical size lower register	JCVSZD	R/W	H'FE98 0020	32
JPEG code horizontal size upper register	JCHSZU	R/W	H'FE98 0024	32
JPEG code horizontal size lower register	JCHSZD	R/W	H'FE98 0028	32
JPEG code data count upper register	JCDTCU	R	H'FE98 002C	32
JPEG code data count middle register	JCDTCM	R	H'FE98 0030	32
JPEG code data count lower register	JCDTCD	R	H'FE98 0034	32
JPEG interrupt enable register	JINTE	R/W	H'FE98 0038	32
JPEG interrupt status register	JINTS	R/W	H'FE98 003C	32
JPEG code decode error register	JCDERR	R/W	H'FE98 0040	32
JPEG code reset register	JCRST	R	H'FE98 0044	32
JPEG interface encoding control register	JIFECNT	R/W	H'FE98 0070	32
JPEG interface encode source Y address register 1	JIFESYA1	R/W	H'FE98 0074	32
JPEG interface encode source C address register 1	JIFESCA1	R/W	H'FE98 0078	32
JPEG interface encode source Y address register 2	JIFESYA2	R/W	H'FE98 007C	32
JPEG interface encode source C address register 2	JIFESCA2	R/W	H'FE98 0080	32
JPEG interface encode source memory width register	JIFESMW	R/W	H'FE98 0084	32
JPEG interface encode source vertical size register	JIFESVSZ	R/W	H'FE98 0088	32
JPEG interface encode source horizontal size register	JIFESHSZ	R/W	H'FE98 008C	32
JPEG interface encode destination address register 1	JIFEDA1	R/W	H'FE98 0090	32
JPEG interface encode destination address register 2	JIFEDA2	R/W	H'FE98 0094	32
JPEG interface encode data reload size register	JIFEDRSZ	R/W	H'FE98 0098	32
JPEG interface decoding control register	JIFDCNT	R/W	H'FE98 00A0	32

Register Name	Abbreviation	R/W	Address	Access Size
JPEG interface decode source address register 1	JIFDSA1	R/W	H'FE98 00A4	32
JPEG interface decode source address register 2	JIFDSA2	R/W	H'FE98 00A8	32
JPEG interface decode data reload size register	JIFDDRSZ	R/W	H'FE98 00AC	32
JPEG interface decode destination memory width register	JIFDDMW	R/W	H'FE98 00B0	32
JPEG interface decode destination vertical size register	JIFDDVSZ	R	H'FE98 00B4	32
JPEG interface decode destination horizontal size register	JIFDDHSZ	R	H'FE98 00B8	32
JPEG interface decode destination Y address register 1	JIFDDYA1	R/W	H'FE98 00BC	32
JPEG interface decode destination C address register 1	JIFDDCA1	R/W	H'FE98 00C0	32
JPEG interface decode destination Y address register 2	JIFDDYA2	R/W	H'FE98 00C4	32
JPEG interface decode destination C address register 2	JIFDDCA2	R/W	H'FE98 00C8	32
JPEG code quantization table 0 register	JCQTBL0	R/W	H'FE99 0000 to H'FE99 003C	32
JPEG code quantization table 1 register	JCQTBL1	R/W	H'FE99 0040 to H'FE99 007C	32
JPEG code quantization table 2 register	JCQTBL2	R/W	H'FE99 0080 to H'FE99 00BC	32
JPEG code quantization table 3 register	JCQTBL3	R/W	H'FE99 00C0 to H'FE99 00FC	32
JPEG code Huffman table DC0 register	JCHTBD0	R/W	H'FE99 0100 to H'FE99 010C	32
JPEG code Huffman table DC0 register	JCHTBD0	R/W	H'FE99 0110 to H'FE99 0118	32
JPEG code Huffman table AC0 register	JCHTBA0	R/W	H'FE99 0120 to H'FE99 012C	32
JPEG code Huffman table AC0 register	JCHTBA0	R/W	H'FE99 0130 to H'FE99 01D0	32
JPEG code Huffman table DC1 register	JCHTBD1	R/W	H'FE99 0200 to H'FE99 020C	32
JPEG code Huffman table DC1 register	JCHTBD1	R/W	H'FE99 0210 to H'FE99 0218	32
JPEG code Huffman table AC1 register	JCHTBA1	R/W	H'FE99 0220 to H'FE99 022C	32
JPEG code Huffman table AC1 register	JCHTBA1	R/W	H'FE99 0230 to H'FE99 02D0	32

Note: For the settings of the JPEG code quantization table and JPEG code Huffman table, see section 43.3.1 (6), Table Setting.

G.44 Register Configuration of TSIF

Register Name	Abbreviation	R/W	Address	Access Size
TSIF0 control register	TS0CTLR	R/W	H'FFE8 0000	32
TSIF0 PID data register	TS0PIDR	R/W	H'FFE8 0004	32
TSIF0 command register	TS0CMDR	R/W	H'FFE8 0008	32
TSIF0 interrupt status register	TS0STR	R/W	H'FFE8 000C	32
TSIF0 TS data register	TS0TSDR	R	H'FFE8 0010	32
TSIF0 buffer clear register	TS0BUFCLRR	R/W	H'FFE8 0014	32
TSIF0 interrupt enable register	TS0INTER	R/W	H'FFE8 0018	32
TSIF0 PSCALE register	TS0PSCALER	R/W	H'FFE8 0020	32
TSIF0 PSCALE_R register	TS0PSCALERR	R/W	H'FFE8 0024	32
TSIF0 PCRADCMODE register	TS0PCRADCMDR	R/W	H'FFE8 0028	32
TSIF0 PCRADC register	TS0PCRADCR	R	H'FFE8 002C	32
TSIF0 TR_PCRADC register	TS0TRPCRADCR	R	H'FFE8 0030	32
TSIF0 D_PCRADC register	TS0DPCRADCR	R	H'FFE8 0034	32
TSIF0 free run counter L	TS0FRCL	R/W	H'FFE8 0040	32
TSIF0 free run counter H	TS0FRCH	R/W	H'FFE8 0044	32
TSIF0 FSCALE register	TS0FSCALER	R/W	H'FFE8 0048	32
TSIF0 FSCALE R register	TS0FSCALERR	R/W	H'FFE8 004C	32
TSIF0 compare match ctrl register	TS0CMCTLR	R/W	H'FFE8 0050	32
TSIF0 compare match counter 0	TS0CMCNT0	R/W	H'FFE8 0054	32
TSIF0 compare match counter 1	TS0CMCNT1	R/W	H'FFE8 005C	32
TSIF0 compare match constant reg 0	TS0CMCOR0	R/W	H'FFE8 0064	32
TSIF0 compare match constant reg 1	TS0CMCOR1	R/W	H'FFE8 006C	32
TSIF0 packet counter	TS0PCNT	R/W	H'FFE8 0074	32
TSIF0 packet counter keep register	TS0PCNTKP	R/W	H'FFE8 0078	32
TSIF0 packet counter push register	TS0PCNTPSH	R/W	H'FFE8 007C	32
TSIF1 control register	TS1CTLR	R/W	H'FFE9 0000	32
TSIF1 PID data register	TS1PIDR	R/W	H'FFE9 0004	32
TSIF1 command register	TS1CMDR	R/W	H'FFE9 0008	32
TSIF1 interrupt status register	TS1STR	R/W	H'FFE9 000C	32
TSIF1 TS data register	TS1TSDR	R	H'FFE9 0010	32
TSIF1 buffer clear register	TS1BUFCLRR	R/W	H'FFE9 0014	32
TSIF1 interrupt enable register	TS1INTER	R/W	H'FFE9 0018	32
TSIF1 PSCALE register	TS1PSCALER	R/W	H'FFE9 0020	32
TSIF1 PSCALE_R register	TS1PSCALERR	R/W	H'FFE9 0024	32
TSIF1 PCRADCMODE register	TS1PCRADCMDR	R/W	H'FFE9 0028	32
TSIF1 PCRADC register	TS1PCRADCR	R	H'FFE9 002C	32
TSIF1 TR_PCRADC register	TS1TRPCRADCR	R	H'FFE9 0030	32
TSIF1 D_PCRADC register	TS1DPCRADCR	R	H'FFE9 0034	32
TSIF1 free run counter L	TS1FRCL	R/W	H'FFE9 0040	32
TSIF1 free run counter H	TS1FRCH	R/W	H'FFE9 0044	32

Register Name	Abbreviation	R/W	Address	Access Size
TSIF1 FSCALE register	TS1FSCALER	R/W	H'FFE9 0048	32
TSIF1 FSCALE R register	TS1FSCALERR	R/W	H'FFE9 004C	32
TSIF1 compare match ctrl register	TS1CMCTLR	R/W	H'FFE9 0050	32
TSIF1 compare match counter 0	TS1CMCNT0	R/W	H'FFE9 0054	32
TSIF1 compare match counter 1	TS1CMCNT1	R/W	H'FFE9 005C	32
TSIF1 compare match constant reg 0	TS1CMCOR0	R/W	H'FFE9 0064	32
TSIF1 compare match constant reg 1	TS1CMCOR1	R/W	H'FFE9 006C	32
TSIF1 packet counter	TS1PCNT	R/W	H'FFE9 0074	32
TSIF1 packet counter keep register	TS1PCNTKP	R/W	H'FFE9 0078	32
TSIF1 packet counter push register	TS1PCNTPSH	R/W	H'FFE9 007C	32

G.45 Register Configuration of CEC

Register	Abbreviation	R/W	Address	Access Size
CEC function control register 1	CECC1	R/W	H'E6BF 0000	8
CEC function control register 2	CECC2	R/W	H'E6BF 0001	8
CEC function control register 3	CECC3	R/W	H'E6BF 0002	8
CEC function control register 4	CECC4	R/W	H'E6BF 0003	8
CEC flag register	CECFLG	R/W	H'E6BF 0004	8
CEC interrupt factor select register	CISEL	R/W	H'E6BF 0005	8
CEC transmission buffer register 1	CCTB1	R/W	H'E6BF 0006	8
CEC transmission buffer register 2	CCTB2	R/W	H'E6BF 0007	8
CEC reception buffer register 1	CCRB1	R/W	H'E6BF 0008	8
CEC reception buffer register 2	CCRB2	R/W	H'E6BF 0009	8
CEC reception follower address register 1	CRADR1	R/W	H'E6BF 000A	8
CEC reception follower address register 2	CRADR2	R/W	H'E6BF 000B	8
CEC interrupt flag register	CINTR	R/W	H'E6BF 001C	8
CEC interrupt flag clear register	CINTCLR	R/W	H'E6BF 001D	8
CEC interrupt mode select register	CINTSEL	R/W	H'E6BF 001E	8

G.46 Register Configuration of SPU2

Register Name	Abbreviation	R/W		Access Size (Bit)		Physical Address	DSP Address
		CPU	DSP	CPU	DSP		
PRAM bank control register 0	PBANKC0	R/W	R	32	24	H'FE2F FC00	H'FF00
PRAM bank control register 1	PBANKC1	R/W	R	32	24	H'FE2F FC04	H'FF01

Register Name	Abbreviation	R/W		Access Size (Bit)		Physical Address	DSP Address
		CPU	DSP	CPU	DSP		
XRAM bank control register 0	XBANKC0	R/W	R/W	32	24	H'FE2F FC10	H'FF04
XRAM bank control register 1	XBANKC1	R/W	R/W	32	24	H'FE2F FC14	H'FF05
SPU software reset register	SPUSRST	R/W	R	32	24	H'FE2F FC24	H'FF09
SPU address register	SPUADR	R	R	32	24	H'FE2F FC28	H'FF0A
SHwy endian register	ENDIAN	R	R	32	24	H'FE2F FC2C	H'FF0B
Global common register 0	GCOM0	R/W	R/W	32	24	H'FE2F FC40	H'FF10
Global common register 1	GCOM1	R/W	R/W	32	24	H'FE2F FC44	H'FF11
Global common register 2	GCOM2	R/W	R/W	32	24	H'FE2F FC48	H'FF12
Global common register 3	GCOM3	R/W	R/W	32	24	H'FE2F FC4C	H'FF13
Global common register 4	GCOM4	R/W	R/W	32	24	H'FE2F FC50	H'FF14
Global common register 5	GCOM5	R/W	R/W	32	24	H'FE2F FC54	H'FF15
Global common register 6	GCOM6	R/W	R/W	32	24	H'FE2F FC58	H'FF16
Global common register 7	GCOM7	R/W	R/W	32	24	H'FE2F FC5C	H'FF17
Inter-DSP communication buffer register 0	DMABUF0	R	R	32	24	H'FE2F FC80	H'FF20
Inter-DSP communication buffer register 1	DMABUF1	R	R	32	24	H'FE2F FC84	H'FF21
Inter-DSP communication buffer register 2	DMABUF2	R	R	32	24	H'FE2F FC88	H'FF22
Inter-DSP communication buffer register 3	DMABUF3	R	R	32	24	H'FE2F FC8C	H'FF23
DSP0 registers							
DSP full reset register	DSPRST	R/W	R	32	24	H'FE2F FD00	H'FF40
DSP core reset register	DSPCORERST	R/W	R	32	24	H'FE2F FD04	H'FF41
DSP hold register	DSPHOLD	R	R	32	24	H'FE2F FD08	H'FF42
DSP restart register	DSPRESTART	R/W	R	32	24	H'FE2F FD0C	H'FF43
CPU interrupt source mask register	IEMASKC	R/W	-	32	24	H'FE2F FD18	H'FF46

Register Name	Abbreviation	R/W		Access Size (Bit)		Physical Address	DSP Address
		CPU	DSP	CPU	DSP		
CPU interrupt signal mask register	IMASKC	R/W	-	32	24	H'FE2F FD1C	H'FF47
CPU interrupt source register	IEVENTC	R/W	-	32	24	H'FE2F FD20	H'FF48
DSP interrupt source mask register	IEMASKD	-	R/W	32	24	H'FE2F FD24	H'FF49
DSP interrupt signal mask register	IMASKD	-	R/W	32	24	H'FE2F FD28	H'FF4A
DSP interrupt set register	IESETD	R/W	R/W	32	24	H'FE2F FD2C	H'FF4B
DSP interrupt clear register	IECLRD	-	R/W	32	24	H'FE2F FD30	H'FF4C
DMAC operation register	OR	R/W	R/W	32	24	H'FE2F FD34	H'FF4D
CPU-DSP communication register 0	COM0	R/W	R/W	32	24	H'FE2F FD38	H'FF4E
CPU-DSP communication register 1	COM1	R/W	R/W	32	24	H'FE2F FD3C	H'FF4F
CPU-DSP communication register 2	COM2	R/W	R/W	32	24	H'FE2F FD40	H'FF50
CPU-DSP communication register 3	COM3	R/W	R/W	32	24	H'FE2F FD44	H'FF51
CPU-DSP communication register 4	COM4	R/W	R/W	32	24	H'FE2F FD48	H'FF52
CPU-DSP communication register 5	COM5	R/W	R/W	32	24	H'FE2F FD4C	H'FF53
CPU-DSP communication register 6	COM6	R/W	R/W	32	24	H'FE2F FD50	H'FF54
CPU-DSP communication register 7	COM7	R/W	R/W	32	24	H'FE2F FD54	H'FF55
Bus-through address high register	BTADRU	R/W	R/W	32	24	H'FE2F FD58	H'FF56
Bus-through address low register	BTADRL	R/W	R/W	32	24	H'FE2F FD5C	H'FF57
Bus-through write data high register	WDATU	R/W	R/W	32	24	H'FE2F FD60	H'FF58

Register Name	Abbreviation	R/W		Access Size (Bit)		Physical Address	DSP Address
		CPU	DSP	CPU	DSP		
Bus-through write data low register	WDATL	R/W	R/W	32	24	H'FE2F FD64	H'FF59
Bus-through read data high register	RDATU	R	R	32	24	H'FE2F FD68	H'FF5A
Bus-through read data low register	RDATL	R	R	32	24	H'FE2F FD6C	H'FF5B
Bus-through mode control register	BTCTRL	R	R/W	32	24	H'FE2F FD70	H'FF5C
SPU status register	SPUSTS	R	R	32	24	H'FE2F FD74	H'FF5D
Source base address register 0	SBAR0	R/W	R/W	32	24	H'FE2F FE00	H'FF80
Source address register 0	SAR0	R/W	R/W	32	24	H'FE2F FE04	H'FF81
Destination base address register 0	DBAR0	R/W	R/W	32	24	H'FE2F FE08	H'FF82
Destination address register 0	DAR0	R/W	R/W	32	24	H'FE2F FE0C	H'FF83
Transfer count register 0	TCR0	R/W	R/W	32	24	H'FE2F FE10	H'FF84
SHwy priority register 0	SHPRI0	R/W	R/W	32	24	H'FE2F FE14	H'FF85
Channel control register 0	CHCR0	R/W	R/W	32	24	H'FE2F FE18	H'FF86
Source base address register 1	SBAR1	R/W	R/W	32	24	H'FE2F FE20	H'FF88
Source address register 1	SAR1	R/W	R/W	32	24		H'FF89
Destination base address register 1	DBAR1	R/W	R/W	32	24	H'FE2F FE28	H'FF8A
Destination address register 1	DAR1	R/W	R/W	32	24	H'FE2F FE2C	H'FF8B
Transfer count register 1	TCR1	R/W	R/W	32	24	H'FE2F FE30	H'FF8C
SHwy priority register 1	SHPRI1	R/W	R/W	32	24	H'FE2F FE34	H'FF8D
Channel control register 1	CHCR1	R/W	R/W	32	24	H'FE2F FE38	H'FF8E
Source base address register 2	SBAR2	R/W	R/W	32	24	H'FE2F FE40	H'FF90
Source address register 2	SAR2	R/W	R/W	32	24	H'FE2F FE44	H'FF91
Destination base address register 2	DBAR2	R/W	R/W	32	24	H'FE2F FE48	H'FF92
Destination address register 2	DAR2	R/W	R/W	32	24	H'FE2F FE4C	H'FF93

Register Name	Abbreviation	R/W		Access Size (Bit)		Physical Address	DSP Address
		CPU	DSP	CPU	DSP		
Transfer count register 2	TCR2	R/W	R/W	32	24	H'FE2F FE50	H'FF94
SHwy priority register 2	SHPRI2	R/W	R/W	32	24	H'FE2F FE54	H'FF95
Channel control register 2	CHCR2	R/W	R/W	32	24	H'FE2F FE58	H'FF96
Loop start address register 0	LSA0	R/W	R/W	32	24	H'FE2F FE80	H'FFA0
Loop end address register 0	LEA0	R/W	R/W	32	24	H'FE2F FE84	H'FFA1
Loop start address register 1	LSA1	R/W	R/W	32	24	H'FE2F FE90	H'FFA4
Loop end address register 1	LEA1	R/W	R/W	32	24	H'FE2F FE94	H'FFA5
Loop start address register 2	LSA2	R/W	R/W	32	24	H'FE2F FEA0	H'FFA8
Loop end address register 2	LEA2	R/W	R/W	32	24	H'FE2F FEA4	H'FFA9
DSP1 registers							
DSP full reset register	DSPRST	R/W	R	32	24	H'FE3F FD00	H'FF40
DSP core reset register	DSPCORERST	R/W	R	32	24	H'FE3F FD04	H'FF41
DSP hold register	DSPHOLD	R	R	32	24	H'FE3F FD08	H'FF42
DSP restart register	DSPRESTART	R/W	R	32	24	H'FE3F FD0C	H'FF43
CPU interrupt source mask register	IEMASKC	R/W	-	32	24	H'FE3F FD18	H'FF46
CPU interrupt signal mask register	IMASKC	R/W	-	32	24	H'FE3F FD1C	H'FF47
CPU interrupt source register	IEVENTC	R/W	-	32	24	H'FE3F FD20	H'FF48
DSP interrupt source mask register	IEMASKD	-	R/W	32	24	H'FE3F FD24	H'FF49
DSP interrupt signal mask register	IMASKD	-	R/W	32	24	H'FE3F FD28	H'FF4A
DSP interrupt set register	IESETD	R/W	R/W	32	24	H'FE3F FD2C	H'FF4B
DSP interrupt clear register	IECLRD	-	R/W	32	24	H'FE3F FD30	H'FF4C
DMAC operation register	OR	R/W	R/W	32	24	H'FE3F FD34	H'FF4D
CPU-DSP communication register 0	COM0	R/W	R/W	32	24	H'FE3F FD38	H'FF4E

Register Name	Abbreviation	R/W		Access Size (Bit)		Physical Address	DSP Address
		CPU	DSP	CPU	DSP		
CPU-DSP communication register 1	COM1	R/W	R/W	32	24	H'FE3F FD3C	H'FF4F
CPU-DSP communication register 2	COM2	R/W	R/W	32	24	H'FE3F FD40	H'FF50
CPU-DSP communication register 3	COM3	R/W	R/W	32	24	H'FE3F FD44	H'FF51
CPU-DSP communication register 4	COM4	R/W	R/W	32	24	H'FE3F FD48	H'FF52
CPU-DSP communication register 5	COM5	R/W	R/W	32	24	H'FE3F FD4C	H'FF53
CPU-DSP communication register 6	COM6	R/W	R/W	32	24	H'FE3F FD50	H'FF54
CPU-DSP communication register 7	COM7	R/W	R/W	32	24	H'FE3F FD54	H'FF55
Bus-through address high register	BTADRU	R/W	R/W	32	24	H'FE3F FD58	H'FF56
Bus-through address low register	BTADRL	R/W	R/W	32	24	H'FE3F FD5C	H'FF57
Bus-through write data high register	WDATU	R/W	R/W	32	24	H'FE3F FD60	H'FF58
Bus-through write data low register	WDATL	R/W	R/W	32	24	H'FE3F FD64	H'FF59
Bus-through read data high register	RDATU	R	R	32	24	H'FE3F FD68	H'FF5A
Bus-through read data low register	RDATL	R	R	32	24	H'FE3F FD6C	H'FF5B
Bus-through mode control register	BTCTRL	R	R/W	32	24	H'FE3F FD70	H'FF5C
SPU status register	SPUSTS	R	R	32	24	H'FE3F FD74	H'FF5D
Source base address register 0	SBAR0	R/W	R/W	32	24	H'FE3F FE00	H'FF80
Source address register 0	SAR0	R/W	R/W	32	24	H'FE3F FE04	H'FF81
Destination base address register 0	DBAR0	R/W	R/W	32	24	H'FE3F FE08	H'FF82
Destination address register 0	DAR0	R/W	R/W	32	24	H'FE3F FE0C	H'FF83

Register Name	Abbreviation	R/W		Access Size (Bit)		Physical Address	DSP Address
		CPU	DSP	CPU	DSP		
Transfer count register 0	TCR0	R/W	R/W	32	24	H'FE3F FE10	H'FF84
SHwy priority register 0	SHPRI0	R/W	R/W	32	24	H'FE3F FE14	H'FF85
Channel control register 0	CHCR0	R/W	R/W	32	24	H'FE3F FE18	H'FF86
Source base address register 1	SBAR1	R/W	R/W	32	24	H'FE3F FE20	H'FF88
Source address register 1	SAR1	R/W	R/W	32	24	H'FE3F FE24	H'FF89
Destination base address register 1	DBAR1	R/W	R/W	32	24	H'FE3F FE28	H'FF8A
Destination address register 1	DAR1	R/W	R/W	32	24	H'FE3F FE2C	H'FF8B
Transfer count register 1	TCR1	R/W	R/W	32	24	H'FE3F FE30	H'FF8C
SHwy priority register 1	SHPRI1	R/W	R/W	32	24	H'FE3F FE34	H'FF8D
Channel control register 1	CHCR1	R/W	R/W	32	24	H'FE3F FE38	H'FF8E
Source base address register 2	SBAR2	R/W	R/W	32	24	H'FE3F FE40	H'FF90
Source address register 2	SAR2	R/W	R/W	32	24	H'FE3F FE44	H'FF91
Destination base address register 2	DBAR2	R/W	R/W	32	24	H'FE3F FE48	H'FF92
Destination address register 2	DAR2	R/W	R/W	32	24	H'FE3F FE4C	H'FF93
Transfer count register 2	TCR2	R/W	R/W	32	24	H'FE3F FE50	H'FF94
SHwy priority register 2	SHPRI2	R/W	R/W	32	24	H'FE3F FE54	H'FF95
Channel control register 2	CHCR2	R/W	R/W	32	24	H'FE3F FE58	H'FF96
Loop start address register 0	LSA0	R/W	R/W	32	24	H'FE3F FE80	H'FFA0
Loop end address register 0	LEA0	R/W	R/W	32	24	H'FE3F FE84	H'FFA1
Loop start address register 1	LSA1	R/W	R/W	32	24	H'FE3F FE90	H'FFA4
Loop end address register 1	LEA1	R/W	R/W	32	24	H'FE3F FE94	H'FFA5
Loop start address register 2	LSA2	R/W	R/W	32	24	H'FE3F FEA0	H'FFA8

Register Name	Abbreviation	R/W		Access Size (Bit)		Physical Address	DSP Address
		CPU	DSP	CPU	DSP		
Loop end address register 2	LEA2	R/W	R/W	32	24	H'FE3F FEA4	H'FFA9

G.47 Register Configuration of FSI2

Type	Register Name	Abbreviation	R/W (Common to CPU/DSP)	Access Size		Physical Address	DSP Address
				CPU	DSP		
Port A	Port A output serial format register	A_DO_FMT	R/W	32	24	H'FE3C0000	H'0000
	Port A output FIFO control register	A_DOFF_CTL	R/W	32	24	H'FE3C0004	H'0001
	Port A output FIFO status register	A_DOFF_ST	R/W	32	24	H'FE3C0008	H'0002
	Port A input serial format register	A_DI_FMT	R/W	32	24	H'FE3C000C	H'0003
	Port A input FIFO control register	A_DIFF_CTL	R/W	32	24	H'FE3C0010	H'0004
	Port A input FIFO status register	A_DIFF_ST	R/W	32	24	H'FE3C0014	H'0005
	Port A Audio clock control register	A_ACK_MD	R/W	32	24	H'FE3C0018	H’0006
	Port A clock invert control register	A_ACK_RV	R/W	32	24	H'FE3C001C	H’0007
	Port A read data register	A_DIDT	R	32	24	H'FE3C0020	H'0008
	Port A write data register	A_DODT	W	32	24	H'FE3C0024	H'0009
	Port A MUTE state register	A_MUTE_ST	R	32	24	H'FE3C0028	H'000A
	Port A DMA control register(Output)	A_OUT_DMAC	R/W	32	24	H'FE3C002C	H’000B
	Port A output control register	A_OUT_SEL	R/W	32	24	H'FE3C0030	H’000C
	Port A output SPDIF state register	A_OUT_SPST	R/W	32	24	H'FE3C0034	H’000D

Type	Register Name	Abbreviation	R/W (Common to CPU/DSP)	Access Size CPU	Access Size DSP	Physical Address	DSP Address
	Port A DMA control register(Input)	A_IN_DMAC	R/W	32	24	H'FE3C0038	H’000E
	Port A input control register	A_IN_SEL	R/W	32	24	H'FE3C003C	H’000F
Port B	Port B output serial format register	B_DO_FMT	R/W	32	24	H'FE3C0040	H’0010
	Port B output FIFO control register	B_DOFF_CTL	R/W	32	24	H'FE3C0044	H’0011
	Port B output FIFO status register	B_DOFF_ST	R/W	32	24	H'FE3C0048	H’0012
	Port B Audio clock control register	B_ACK_MD	R/W	32	24	H'FE3C0058	H’0016
	Port B clock invert control register	B_ACK_RV	R/W	32	24	H'FE3C005C	H’0017
	Port B write data register	B_DODT	W	32	24	H'FE3C0064	H’0019
	Port B MUTE state register	B_MUTE_ST	R	32	24	H'FE3C0068	H’001A
	Port B DMA control register(Output)	B_OUT_DMAC	R/W	32	24	H'FE3C006C	H’001B
	Port B output control register	B_OUT_SEL	R/W	32	24	H'FE3C0070	H’001C
	Port B output SPDIF state register	B_OUT_SPST	R/W	32	24	H'FE3C0074	H’001D
Port A/B	Port A master clock control register	A_MST_CTLR	R/W	32	24	H'FE3C0180	H’0060
	Port B master clock control register	B_MST_CTLR	R/W	32	24	H'FE3C01A0	H’0068
Timer	Timer set register	TMR_CTL	R/W	32	24	H'FE3C01D8	H’0076
	Timer clear register	TMR_CLR	R/W	32	24	H'FE3C01DC	H’0077
Interrupt	Interrupt clear register	INT_CLR	R/W	32	24	H'FE3C01F0	H'007C

Type	Register Name	Abbreviation	R/W (Common to CPU/DSP)	Access Size CPU	Access Size DSP	Physical Address	DSP Address
	CPU interrupt state register	CPU_INT_ST	R/W	32	24	H'FE3C01F4	H'007D
	CPU interrupt source mask register	CPU_IEMSK	R/W	32	24	H'FE3C01F8	H'007E
	CPU interrupt signal mask register	CPU_IMSK	R/W	32	24	H'FE3C01FC	H'007F
	DSP interrupt state register	DSP_INT_ST	R/W	32	24	H'FE3C0200	H'0080
	DSP interrupt source mask register	DSP_IEMSK	R/W	32	24	H'FE3C0204	H'0081
	DSP interrupt signal mask register	DSP_IMSK	R/W	32	24	H'FE3C0208	H'0082
MUTE	MUTE set register	MUTE	R/W	32	24	H'FE3C020C	H'0083
Reset	Clock reset register	ACK_RST	R/W	32	24	H'FE3C0210	H'0084
	Software reset register	SOFT_RST	R/W	32	24	H'FE3C0214	H'0085
FIFO	FIFO size register	FIFO_SZ	R	32	24	H'FE3C0218	H'0086
Peripheral	Clock select register	CLK_SEL	R/W	32	-	H'FE3C0220	-
Bus	SWAP select register	SWAP_SEL	R/W	32	-	H'FE3C0228	-
	HPB software reset register	HPB_SRST	R/W	32	-	H'FE3C022C	-
Port A Param	SPDIF(60958) Port A channel state register	A_SP_CHST00 A_SP_CHST01	R/W	32	24	H'FE3C0240 H'FE3C0244	H'0090 H'0091
	SPDIF(60958) Port A user data register	A_SP_USDT00 … A_SP_USDT23	R/W	32	24	H'FE3C02A0 … H'FE3C02FC	H'00A8 … H'00BF
	SPDIF(61937) Port A preamble pa register	A_SP_PA	R/W	32	24	H'FE3C0300	H'00C0
	SPDIF(61937) Port A preamble pb register	A_SP_PB	R/W	32	24	H'FE3C0304	H'00C1
	SPDIF(61937)	A_SP_PC	R/W	32	24	H'FE3C0308	H'00C2

Type	Register Name	Abbreviation	R/W (Common to CPU/DSP)	Access Size CPU	Access Size DSP	Physical Address	DSP Address
	Port A preamble pc register						
	SPDIF(61937) Port A preamble pd register	A_SP_PD	R/W	32	24	H'FE3C030C	H’00C3
	Port A Pause cycle register	A_SP_PS	R/W	32	24	H'FE3C0314	H’00C5
	Port A Pause length register	A_SP_PL	R/W	32	24	H'FE3C0318	H’00C6
	Port A Frame size register	A_SP_FS	R/W	32	24	H'FE3C031C	H’00C7
Port B Param	SPDIF(60958) Port B channel state register	B_SP_CHST00 B_SP_CHST01	R/W	32	24	H'FE3C0320 H'FE3C0324	H’00C8 H’00C9
	SPDIF(60958) Port B user data register	B_SP_USDT00 … B_SP_USDT23	R/W	32	24	H'FE3C0380 … H'FE3C03DC	H’00E0 … H’00F7
	SPDIF(61937) Port B preamble pa register	B_SP_PA	R/W	32	24	H'FE3C03E0	H’00F8
	SPDIF(61937) Port B preamble pb register	B_SP_PB	R/W	32	24	H'FE3C03E4	H’00F9
	SPDIF(61937) Port B preamble pc register	B_SP_PC	R/W	32	24	H'FE3C03E8	H’00FA
	SPDIF(61937) Port B preamble pd register	B_SP_PD	R/W	32	24	H'FE3C03EC	H’00FB
	Port B Pause cycle register	B_SP_PS	R/W	32	24	H'FE3C03F4	H’00FD
	Port B Pause length register	B_SP_PL	R/W	32	24	H'FE3C03F8	H’00FE
	Port B Frame size register	B_SP_FS	R/W	32	24	H'FE3C03FC	H’00FF
common	Interrupt SEL register	INT_SEL	R/W	32	24	H'FE3FF808	H’FE02

Note: The port A and port B registers have the same functions and settings.

G.48 Register Configuration of FMSI

Register Name	Abbreviation	R/W	Physical Address	DSP Address	Access Size		Dynamic/ Static
					CPU	DSP	
Serial output format register	S_DO_FMT	R/W	H'FE3C 0400	H'0100	32	24	S
Serial output FIFO control register	S_DOFF_CTL	R/W	H'FE3C 0404	H'0101	32	24	S/D*
Serial output FIFO status register	S_DOFF_ST	R/W	H'FE3C 0408	H'0102	32	24	D
Serial input format register	S_DI_FMT	R/W	H'FE3C 040C	H'0103	32	24	S
Serial input FIFO control register	S_DIFF_CTL	R/W	H'FE3C 0410	H'0104	32	24	S/D*
Serial input FIFO status register	S_DIFF_ST	R/W	H'FE3C 0414	H'0105	32	24	D
Serial input FIFO read register	S_DIDT	R	H'FE3C 0420	H'0108	32	24	D
Serial output FIFO write register	S_DODT	W	H'FE3C 0424	H'0109	32	24	D
Serial MUTE state register	S_MUTE_ST	R	H'FE3C 0428	H'010A	32	24	D
Parallel input format register	P_DI_FMT	R/W	H'FE3C 044C	H'0113	32	24	S
Parallel input FIFO control register	P_DIFF_CTL	R/W	H'FE3C 0450	H'0114	32	24	S/D*
Parallel input FIFO status register	P_DIFF_ST	R/W	H'FE3C 0454	H'0115	32	24	D
Parallel input FIFO read register	P_DIDT	R	H'FE3C 0460	H'0118	32	24	D
Parallel MUTE state register	P_MUTE_ST	R	H'FE3C 0468	H'011A	32	24	D
SO-IF and MI-IF operating clock set register	SOMI_CKG_MD	R/W	H'FE3C 05C0	H'0170	32	24	S
SO-IF and MI-IF operating clock invert register	SOMI_CKG_RV	R/W	H'FE3C 05C4	H'0171	32	24	S
SI-IF and MSUO-IF operating clock set register	SIMO_CKG_MD	R/W	H'FE3C 05C8	H'0172	32	24	S
SI-IF and MSUO-IF operating clock invert register	SIMO_CKG_RV	R/W	H'FE3C 05CC	H'0173	32	24	S
Clock system set register	CKG_SMD	R/W	H'FE3C 05D0	H'0174	32	24	S
Timer count set register	TMR_CTL	R/W	H'FE3C 05D8	H'0176	32	24	D

Register Name	Abbreviation	R/W	Physical Address	DSP Address	Access Size		Dynamic/ Static
					CPU	DSP	
Timer count clear register	TMR_CLR	R/W	H'FE3C 05DC	H'0177	32	24	D
Direct serial transfer set register	DRCT_SRL	R/W	H'FE3C 05E0	H'0178	32	24	S
Interrupt state register	INT_ST	R/W	H'FE3C 0600	H'0180	32	24	D
Interrupt source mask register	IEMSK	R/W	H'FE3C 0605	H'0181	32	24	D
Interrupt signal mask register	IMSK	R/W	H'FE3C 0608	H'0182	32	24	D
MUTE set register	MUTE	R/W	H'FE3C 060C	H'0183	32	24	D
Clock reset register	CLK_RST	R/W	H'FE3C 0610	H'0184	32	24	S
Software reset register	SOFT_RST	R/W	H'FE3C 0614	H'0185	32	24	S
FIFO size register	FIFO_SZ	R	H'FE3C 0618	H'0186	32	24	S

Note: The (FIFO) CLR bit (bit 0) is a static bit; however, all the other bits in the register, that is, interrupt monitoring condition setting bits can be modified dynamically.

There are two types of registers, dynamic and static. Static registers should not be modified when the FSI is in operation (during continuous operation).

The CPU can write/read data to/from the lower bits (23 to 0) in registers. The upper bits are read as 0 and cannot be modified.

For setting the FMSI operation, also see a description of the register for selecting the FSI/FMSI interrupt acknowledge destination in section 52.4.19.

G.49 Register Configuration of FSIDIV

Register Name	Abbreviation	R/W	initial value	Access Size	Physical Address
Port A Divider control register	FSIDIVA	R/W	H'00000000	32	H'FE1F8000
Port B Divider control register	FSIDIVB	R/W	H'00000000	32	H'FE1F8008

G.50 Register Configuration of I2C

Register Name	Abbreviation	R/W	Address	Access Size
x is a channel identification character.	x is a channel identification character.		High order address	
I²C0:0	I²C0:0		I²C0:H'FFF2	
I²C1:1	I²C1:1		I²C1:H'E6C2	
I²C2:2	I²C2:2		I²C2:H'FFF3	

Register Name	Abbreviation	R/W	Address	Access Size
I²C3:3 I²C4:4	I²C3:3 I²C4:4		I²C3:H'E6D2 I²C4:H'E6D3	
I²C bus data register x	ICDRx	R/W	H'XXXX 0000	8
I²C birth control register x	ICCRx	R/W	H'XXXX 0004	8
I²C bus status register x	ICSRx	R/W	H'XXXX 0008	8
I²C interruption control register x	ICICx	R/W	H'XXXX 000C	8
I²C clock control register low x	ICCLx	R/W	H'XXXX 0010	8
I²C clock control register high x	ICCHx	R/W	H'XXXX 0014	8
I²C transformer register x	ICTRx	R	H'XXXX 0018	8
I²C receipt register x	ICRRx	R	H'XXXX 001C	8
I²C transformer monitor x	ICTAx	R	H'XXXX 0020	8
I²C transformer buffer monitor x	ICTBx	R	H'XXXX 0024	8
I²C transformer control register x	ICTCx	R/W	H'XXXX 0028	8
I²C transformer control status monitor x	ICTDx	R/W	H'XXXX 002C	8
I²C shift register x	ICSFx	R	H'XXXX 0030	8
I²C Hs Clock control register low x*1	ICHLx	R	H'XXXX 0034	8
I²C Hs Clock control register high x*1	ICHHx	R	H'XXXX 0038	8
I²C Hs master code x*1	ICHMCODx	R	H'XXXX 003C	8
I²C Option enabling register x*1	ICVCONx	R	H'XXXX 006C	8
I²C automatic transmission interruption mask register x*1	ICIMSKx	R/W	H'XXXX 0050	8
I²C automatic transmission interruption flag register x*1	ICINTx	R	H'XXXX 0054	8
I²C automatic transmission processing enabling register x*1	ICACEx	R/W	H'XXXX 0058	8
I²C automatic transmission timer control register 1x *1	ICTMC1x	R/W	H'XXXX 0060	8
I²C automatic transmission timer control register 2x *1	ICTMC2x	R/W	H'XXXX 0064	8
I²C automatic transmission wait control register x*1	ICTMCWx	R/W	H'XXXX 0068	8
I²C automatic transmission transformer start register x*1	ICASTARTx	R/W	H'XXXX 0070	8
I²C automatic transmission transformer control register x*1	ICATFRx	R/W	H'XXXX 0080	8
I²C automatic transmission transformer time register 1x *1	ICATSET1x	R/W	H'XXXX 0084	8
I²C automatic transmission transformer time register 2x *1	ICATSET2x	R/W	H'XXXX 0088	8
I²C automatic transmission receipt time register 1x *1	ICARSET1x	R/W	H'XXXX 008C	8
I²C automatic transmission receipt time register 2x *1	ICARSET2x	R/W	H'XXXX 0090	8

Register Name	Abbreviation	R/W	Address	Access Size
I²C automatic transmission transformer data 00x *1	ICATD00x	R/W	H'XXXX 0100	8
I²C automatic transmission transformer data 01x *1	ICATD01x	R/W	H'XXXX 0104	8
I²C automatic transmission transformer data 02x *1	ICATD02x	R/W	H'XXXX 0108	8
I²C automatic transmission transformer data 03x *1	ICATD03x	R/W	H'XXXX 010C	8
I²C automatic transmission transformer data 04x *1	ICATD04x	R/W	H'XXXX 0110	8
I²C automatic transmission transformer data 05x *1	ICATD05x	R/W	H'XXXX 0114	8
I²C automatic transmission transformer data 06x *1	ICATD06x	R/W	H'XXXX 0118	8
I²C automatic transmission transformer data 07x *1	ICATD07x	R/W	H'XXXX 011C	8
I²C automatic transmission transformer data 08x *1	ICATD08x	R/W	H'XXXX 0120	8
I²C automatic transmission transformer data 09x *1	ICATD09x	R/W	H'XXXX 0124	8
I²C automatic transmission transformer data 10x *1	ICATD10x	R/W	H'XXXX 0200	8
I²C automatic transmission transformer data 11x *1	ICATD11x	R/W	H'XXXX 0204	8
I²C automatic transmission transformer data 12x *1	ICATD12x	R/W	H'XXXX 0208	8
I²C automatic transmission transformer data 13x *1	ICATD13x	R/W	H'XXXX 020C	8
I²C automatic transmission transformer data 14x *1	ICATD14x	R/W	H'XXXX 0210	8
I²C automatic transmission transformer data 15x *1	ICATD15x	R/W	H'XXXX 0214	8
I²C automatic transmission transformer data 16x *1	ICATD16x	R/W	H'XXXX 0218	8
I²C automatic transmission transformer data 17x *1	ICATD17x	R/W	H'XXXX 021C	8
I²C automatic transmission transformer data 18x *1	ICATD18x	R/W	H'XXXX 0220	8
I²C automatic transmission transformer data 19x *1	ICATD19x	R/W	H'XXXX 0224	8
I²C automatic transmission receipt data 00x *1	ICARD00x	R	H'XXXX 0300	8
I²C automatic transmission receipt data 01x *1	ICARD01x	R	H'XXXX 0304	8
I²C automatic transmission receipt data 02x *1	ICARD02x	R	H'XXXX 0308	8

Register Name	Abbreviation	R/W	Address	Access Size
I²C automatic transmission receipt data 03x *1	ICARD03x	R	H'XXXX 030C	8
I²C automatic transmission receipt data 04x *1	ICARD04x	R	H'XXXX 0310	8
I²C automatic transmission receipt data 05x *1	ICARD05x	R	H'XXXX 0314	8
I²C automatic transmission receipt data 06x *1	ICARD06x	R	H'XXXX 0318	8
I²C automatic transmission receipt data 07x *1	ICARD07x	R	H'XXXX 031C	8
I²C automatic transmission receipt data 08x *1	ICARD08x	R	H'XXXX 0320	8
I²C automatic transmission receipt data 09x *1	ICARD09x	R	H'XXXX 0324	8
I²C automatic transmission receipt data 10x *1	ICARD10x	R	H'XXXX 0400	8
I²C automatic transmission receipt data 11x *1	ICARD11x	R	H'XXXX 0404	8
I²C automatic transmission receipt data 12x *1	ICARD12x	R	H'XXXX 0408	8
I²C automatic transmission receipt data 13x *1	ICARD13x	R	H'XXXX 040C	8
I²C automatic transmission receipt data 14x *1	ICARD14x	R	H'XXXX 0410	8
I²C automatic transmission receipt data 15x *1	ICARD15x	R	H'XXXX 0414	8
I²C automatic transmission receipt data 16x *1	ICARD16x	R	H'XXXX 0418	8
I²C automatic transmission receipt data 17x *1	ICARD17x	R	H'XXXX 041C	8
I²C automatic transmission receipt data 18x *1	ICARD18x	R	H'XXXX 0420	8
I²C automatic transmission receipt data 19x *1	ICARD19x	R	H'XXXX 0424	8

*1 Only I²C2 and I²C3 and I²C4 are effective. Please do not access in I²C0 and I²C1.

The automatic transmission assumes the end of communication by interruption, and error detection, please do not perform principle polling during automatic transmission.

G.51 Register Configuration of KEYSC

Register Name	Abbreviation	R/W	Address*	Access Size

Register Name	Abbreviation	R/W	Address*	Access Size
Manual key scan control register 1	M_KYCR1	R/W	H'E61B 0000 H'E71B 0000	16
Manual key scan control register 2	M_KYCR2	R/W	H'E61B 0004 H'E71B 0004	16
Manual key scan-in data register	M_KYINDR	R	H'E61B 0008 H'E71B 0008	16
Manual key scan-out data register	M_KYOUTDR	R/W	H'E61B 000C H'E71B 000C	16
Auto key scan control register 1	A_KYCR1	R/W	H’E61B0010 H’E71B0010	16
Auto key scan control register 2	A_KYCR2	R/W	H’E61B0014 H’E71B0014	16
Auto key scan control register 4	A_KYCR4	R/W	H’E61B001C H’E71B001C	16
Auto key scan control register 6	A_KYCR6	R/W	H’E61B0024 H’E71B0024	16
Auto key scan interrupt control register	A_KYIR	R/W	H’E61B0030 H’E71B0030	32
Auto key scan status register	A_KYSR	R/W	H’E61B0034 H’E71B0034	32
Auto key scan-in data register	A_KYINDR	R	H’E61B0038 H’E71B0038	16
Auto key scan-out data register	A_KYOUTDR	R/W	H’E61B003C H’E71B003C	16
Auto key scan data register L	A_KYSCDRL	R	H’E61B0040 H’E71B0040	32
Auto key scan data register H	A_KYSCDRH	R	H’E61B0044 H’E71B0044	32
Auto key scan data-touch register L	A_KYSCDTRL	R	H’E61B0048 H’E61B0048	32
Auto key scan data-touch register H	A_KYSCDTRH	R	H’E61B004C H’E71B004C	32
Auto key scan data-release register L	A_KYSCDRRL	R	H’E61B0050 H’E71B0050	32
Auto key scan data-release register H	A_KYSCDRRH	R	H’E61B0054 H’E71B0054	32
Auto key scan data-count register	A_KYSCDNUM	R/W	H’E61B0060 H’E71B0060	32

* These registers can be accessed from both HPBC area (H'E6xx xxxx) and HPBD area (H'E7xx xxxx).

G.52 Register Configuration of IrDA

Register	Abbreviation	R/W	Address	Access Size
Transfer mode register	IRTMR	R/W	H'E6D0 1F00	8/16
Configuration register	IRCFR	R/W	H'E6D0 1F02	8/16
IR control register	IRCTR	R/W	H'E6D0 1F04	8/16
Transmit frame length register	IRTFLR	R/W	H'E6D0 1F20	8/16
Transmit control register	IRTCTR	R/W	H'E6D0 1F22	8/16
Receive frame length register	IRRFLR	R	H'E6D0 1F40	8/16
Receive control register	IRRCTR	R/W	H'E6D0 1F42	8/16
SIR-UART mode interrupt source register	SIRISR	R	H'E6D0 1F60	8/16
SIR-UART mode interrupt mask register	SIRIMR	W	H'E6D0 1F62	8/16
SIR-UART mode interrupt clear register	SIRICR	W	H'E6D0 1F64	8/16
SIR-UART mode baud rate count register	SIRBCR	R/W	H'E6D0 1F68	8/16
MIR/FIR mode interrupt source register	MFIRISR	R	H'E6D0 1F70	8/16
MIR/FIR mode interrupt mask register	MFIRIMR	W	H'E6D0 1F72	8/16
MIR/FIR mode interrupt clear register	MFIRICR	W	H'E6D0 1F74	8/16
CRC engine control register	CRCCTR	R/W	H'E6D0 1F80	8/16
CRC engine input data register	CRCIR	W	H'E6D0 1F86	8/16
CRC engine calculation register	CRCCR	W	H'E6D0 1F8A	16
CRC engine output data register	CRCOR	R	H'E6D0 1F8E	8/16
FIFO current pointer	FIFOCP	R/W	H'E6D0 1FC0	16
FIFO follow pointer	FIFOFP	R/W	H'E6D0 1FC2	16
FIFO receive status mask	FIFORSMSK	R/W	H'E6D0 1FC4	16
FIFO receive status OR	FIFORSOR	R	H'E6D0 1FC6	16
FIFO select	FIFOSEL	R/W	H'E6D0 1FC8	16
FIFO receive status	FIFORS	R/W	H'E6D0 1FCA	16
FIFO receive frame length	FIFORFL	R/W	H'E6D0 1FCC	16
FIFO RAM current pointer	FIFORAMCP	R/W	H'E6D0 1FCE	16
FIFO RAM follow pointer	FIFORAMFP	R/W	H'E6D0 1FD0	16
BUS interface control	BIFCTL	R/W	H'E6D0 1FD2	16
IrDA buffer RAM	IRDARAM	R/W	H'E6D0 0000 to H'E6D0 1039	8/16/32 (read-only for 32)

G.53 Register Configuration of GPIO

Side	Register Name	Abbreviation	R/W	Address	Initial value	Access Size
D	PORT0 Port control register	PORT0CR	R/W	H'E6051000	H'A0	8,32
D	PORT1 Port control register	PORT1CR	R/W	H'E6051001	H'A0	8,32
D	PORT2 Port control register	PORT2CR	R/W	H'E6051002	H'10	8,32
D	PORT3 Port control register	PORT3CR	R/W	H'E6051003	H'A0	8,32
D	PORT4 Port control register	PORT4CR	R/W	H'E6051004	H'A0	8,32
D	PORT5 Port control register	PORT5CR	R/W	H'E6051005	H'A0	8,32
D	PORT6 Port control register	PORT6CR	R/W	H'E6051006	H'A0	8,32
D	PORT7 Port control register	PORT7CR	R/W	H'E6051007	H'A0	8,32
D	PORT8 Port control register	PORT8CR	R/W	H'E6051008	H'A0	8,32
D	PORT9 Port control register	PORT9CR	R/W	H'E6051009	H'10	8,32
D	PORT10 Port control register	PORT10CR	R/W	H'E605100A	H'10	8,32
D	PORT11 Port control register	PORT11CR	R/W	H'E605100B	H'10	8,32
D	PORT12 Port control register	PORT12CR	R/W	H'E605100C	H'A0	8,32
D	PORT13 Port control register	PORT13CR	R/W	H'E605100D	H'A0	8,32
D	PORT14 Port control register	PORT14CR	R/W	H'E605100E	H'A0	8,32
D	PORT15 Port control register	PORT15CR	R/W	H'E605100F	H'10	8,32
D	PORT16 Port control register	PORT16CR	R/W	H'E6051010	H'A0	8,32
D	PORT17 Port control register	PORT17CR	R/W	H'E6051011	H'A0	8,32
D	PORT18 Port control register	PORT18CR	R/W	H'E6051012	H'A0	8,32
D	PORT19 Port control register	PORT19CR	R/W	H'E6051013	H'12	8,32
D	PORT20 Port control register	PORT20CR	R/W	H'E6051014	H'11	8,32
D	PORT21 Port control register	PORT21CR	R/W	H'E6051015	H'11	8,32

Side	Register Name	Abbreviation	R/W	Address	Initial value	Access Size
D	PORT22 Port control register	PORT22CR	R/W	H'E6051016	H'11	8,32
D	PORT23 Port control register	PORT23CR	R/W	H'E6051017	H'11	8,32
D	PORT24 Port control register	PORT24CR	R/W	H'E6051018	H'11	8,32
D	PORT25 Port control register	PORT25CR	R/W	H'E6051019	H'11	8,32
D	PORT26 Port control register	PORT26CR	R/W	H'E605101A	H'11	8,32
D	PORT27 Port control register	PORT27CR	R/W	H'E605101B	H'11	8,32
D	PORT28 Port control register	PORT28CR	R/W	H'E605101C	H'11	8,32
D	PORT29 Port control register	PORT29CR	R/W	H'E605101D	H'11	8,32
D	PORT30 Port control register	PORT30CR	R/W	H'E605101E	H'11	8,32
D	PORT31 Port control register	PORT31CR	R/W	H'E605101F	H'11	8,32
D	PORT32 Port control register	PORT32CR	R/W	H'E6051020	H'11	8,32
D	PORT33 Port control register	PORT33CR	R/W	H'E6051021	H'11	8,32
D	PORT34 Port control register	PORT34CR	R/W	H'E6051022	H'11	8,32
D	PORT35 Port control register	PORT35CR	R/W	H'E6051023	H'11	8,32
D	PORT36 Port control register	PORT36CR	R/W	H'E6051024	H'11	8,32
D	PORT37 Port control register	PORT37CR	R/W	H'E6051025	H'11	8,32
D	PORT38 Port control register	PORT38CR	R/W	H'E6051026	H'11	8,32
D	PORT39 Port control register	PORT39CR	R/W	H'E6051027	H'11	8,32
D	PORT40 Port control register	PORT40CR	R/W	H'E6051028	H'11	8,32
D	PORT41 Port control register	PORT41CR	R/W	H'E6051029	H'11	8,32
D	PORT42 Port control register	PORT42CR	R/W	H'E605102A	H'11	8,32
D	PORT43 Port control register	PORT43CR	R/W	H'E605102B	H'11	8,32
D	PORT44 Port control register	PORT44CR	R/W	H'E605102C	H'11	8,32

Side	Register Name	Abbreviation	R/W	Address	Initial value	Access Size
D	PORT45 Port control register	PORT45CR	R/W	H'E605102D	H'11	8,32
R	PORT46 Port control register	PORT46CR	R/W	H'E605202E	H'C1	8,32
R	PORT47 Port control register	PORT47CR	R/W	H'E605202F	H'C1	8,32
R	PORT48 Port control register	PORT48CR	R/W	H'E6052030	H'C1	8,32
R	PORT49 Port control register	PORT49CR	R/W	H'E6052031	H'C1	8,32
R	PORT50 Port control register	PORT50CR	R/W	H'E6052032	H'C1	8,32
R	PORT51 Port control register	PORT51CR	R/W	H'E6052033	H'C1	8,32
R	PORT52 Port control register	PORT52CR	R/W	H'E6052034	H'C1	8,32
R	PORT53 Port control register	PORT53CR	R/W	H'E6052035	H'C1	8,32
R	PORT54 Port control register	PORT54CR	R/W	H'E6052036	H'C1	8,32
R	PORT55 Port control register	PORT55CR	R/W	H'E6052037	H'C1	8,32
R	PORT56 Port control register	PORT56CR	R/W	H'E6052038	H'C1	8,32
R	PORT57 Port control register	PORT57CR	R/W	H'E6052039	H'C1	8,32
R	PORT58 Port control register	PORT58CR	R/W	H'E605203A	H'C1	8,32
R	PORT59 Port control register	PORT59CR	R/W	H'E605203B	H'C1	8,32
R	PORT60 Port control register	PORT60CR	R/W	H'E605203C	H'C1	8,32
R	PORT61 Port control register	PORT61CR	R/W	H'E605203D	H'C1	8,32
R	PORT62 Port control register	PORT62CR	R/W	H'E605203E	H'11	8,32
R	PORT63 Port control register	PORT63CR	R/W	H'E605203F	H'11	8,32
R	PORT64 Port control register	PORT64CR	R/W	H'E6052040	H'11	8,32
R	PORT65 Port control register	PORT65CR	R/W	H'E6052041	H'E0	8,32
R	PORT66 Port control register	PORT66CR	R/W	H'E6052042	H'C0	8,32
R	PORT67 Port control register	PORT67CR	R/W	H'E6052043	H'E0	8,32

Side	Register Name	Abbreviation	R/W	Address	Initial value	Access Size
R	PORT68 Port control register	PORT68CR	R/W	H'E6052044	H'11	8,32
R	PORT69 Port control register	PORT69CR	R/W	H'E6052045	H'11	8,32
R	PORT70 Port control register	PORT70CR	R/W	H'E6052046	H'11	8,32
R	PORT71 Port control register	PORT71CR	R/W	H'E6052047	H'11	8,32
R	PORT72 Port control register	PORT72CR	R/W	H'E6052048	H'11	8,32
R	PORT73 Port control register	PORT73CR	R/W	H'E6052049	H'E1	8,32
R	PORT74 Port control register	PORT74CR	R/W	H'E605204A	H'E1	8,32
R	PORT75 Port control register	PORT75CR	R/W	H'E605204B	H'E0	8,32
L	PORT76 Port control register	PORT76CR	R/W	H'E605004C	H'80	8,32
L	PORT77 Port control register	PORT77CR	R/W	H'E605004D	H'80	8,32
L	PORT78 Port control register	PORT78CR	R/W	H'E605004E	H'80	8,32
L	PORT79 Port control register	PORT79CR	R/W	H'E605004F	H'80	8,32
L	PORT80 Port control register	PORT80CR	R/W	H'E6050050	H'80	8,32
L	PORT81 Port control register	PORT81CR	R/W	H'E6050051	H'80	8,32
L	PORT82 Port control register	PORT82CR	R/W	H'E6050052	H'80	8,32
L	PORT83 Port control register	PORT83CR	R/W	H'E6050053	H'80	8,32
L	PORT84 Port control register	PORT84CR	R/W	H'E6050054	H'C0	8,32
L	PORT85 Port control register	PORT85CR	R/W	H'E6050055	H'C0	8,32
L	PORT86 Port control register	PORT86CR	R/W	H'E6050056	H'C0	8,32
L	PORT87 Port control register	PORT87CR	R/W	H'E6050057	H'C0	8,32
L	PORT88 Port control register	PORT88CR	R/W	H'E6050058	H'C0	8,32
L	PORT89 Port control register	PORT89CR	R/W	H'E6050059	H'C0	8,32
L	PORT90 Port control register	PORT90CR	R/W	H'E605005A	H'C0	8,32

Side	Register Name	Abbreviation	R/W	Address	Initial value	Access Size
L	PORT91 Port control register	PORT91CR	R/W	H'E605005B	H'C0	8,32
L	PORT92 Port control register	PORT92CR	R/W	H'E605005C	H'E0	8,32
L	PORT93 Port control register	PORT93CR	R/W	H'E605005D	H'E0	8,32
L	PORT94 Port control register	PORT94CR	R/W	H'E605005E	H'E0	8,32
L	PORT95 Port control register	PORT95CR	R/W	H'E605005F	H'E0	8,32
L	PORT96 Port control register	PORT96CR	R/W	H'E6050060	H'C0	8,32
L	PORT97 Port control register	PORT97CR	R/W	H'E6050061	H'E0	8,32
L	PORT98 Port control register	PORT98CR	R/W	H'E6050062	H'E0	8,32
L	PORT99 Port control register	PORT99CR	R/W	H'E6050063	H'C0	8,32
U	PORT100 Port control register	PORT100CR	R/W	H'E6053064	H'A0	8,32
U	PORT101 Port control register	PORT101CR	R/W	H'E6053065	H'A0	8,32
U	PORT102 Port control register	PORT102CR	R/W	H'E6053066	H'A0	8,32
U	PORT103 Port control register	PORT103CR	R/W	H'E6053067	H'A0	8,32
U	PORT104 Port control register	PORT104CR	R/W	H'E6053068	H'A0	8,32
U	PORT105 Port control register	PORT105CR	R/W	H'E6053069	H'A0	8,32
U	PORT106 Port control register	PORT106CR	R/W	H'E605306A	H'E0	8,32
U	PORT107 Port control register	PORT107CR	R/W	H'E605306B	H'E0	8,32
U	PORT108 Port control register	PORT108CR	R/W	H'E605306C	H'E0	8,32
U	PORT109 Port control register	PORT109CR	R/W	H'E605306D	H'E0	8,32
U	PORT110 Port control register	PORT110CR	R/W	H'E605306E	H'E0	8,32
U	PORT111 Port control register	PORT111CR	R/W	H'E605306F	H'E0	8,32
U	PORT112 Port control register	PORT112CR	R/W	H'E6053070	H'A0	8,32
U	PORT113 Port control register	PORT113CR	R/W	H'E6053071	H'A0	8,32

Side	Register Name	Abbreviation	R/W	Address	Initial value	Access Size
U	PORT114 Port control register	PORT114CR	R/W	H'E6053072	H'E0	8,32
U	PORT115 Port control register	PORT115CR	R/W	H'E6053073	H'E0	8,32
U	PORT116 Port control register	PORT116CR	R/W	H'E6053074	H'E0	8,32
U	PORT117 Port control register	PORT117CR	R/W	H'E6053075	H'E0	8,32
U	PORT118 Port control register	PORT118CR	R/W	H'E6053076	H'E0	8,32
U	PORT119 Port control register	PORT119CR	R/W	H'E6053077	H'E0	8,32
U	PORT120 Port control register	PORT120CR	R/W	H'E6053078	H'E0	8,32
L	PORT121 Port control register	PORT121CR	R/W	H'E6050079	H'A0	8,32
L	PORT122 Port control register	PORT122CR	R/W	H'E605007A	H'A0	8,32
L	PORT123 Port control register	PORT123CR	R/W	H'E605007B	H'A0	8,32
L	PORT124 Port control register	PORT124CR	R/W	H'E605007C	H'A0	8,32
L	PORT125 Port control register	PORT125CR	R/W	H'E605007D	H'A0	8,32
L	PORT126 Port control register	PORT126CR	R/W	H'E605007E	H'A0	8,32
L	PORT127 Port control register	PORT127CR	R/W	H'E605007F	H'A0	8,32
L	PORT128 Port control register	PORT128CR	R/W	H'E6050080	H'A0	8,32
L	PORT129 Port control register	PORT129CR	R/W	H'E6050081	H'A0	8,32
L	PORT130 Port control register	PORT130CR	R/W	H'E6050082	H'A0	8,32
L	PORT131 Port control register	PORT131CR	R/W	H'E6050083	H'A0	8,32
L	PORT132 Port control register	PORT132CR	R/W	H'E6050084	H'A0	8,32
L	PORT133 Port control register	PORT133CR	R/W	H'E6050085	H'A0	8,32
L	PORT134 Port control register	PORT134CR	R/W	H'E6050086	H'A0	8,32
L	PORT135 Port control register	PORT135CR	R/W	H'E6050087	H'A0	8,32
L	PORT136 Port control register	PORT136CR	R/W	H'E6050088	H'A0	8,32

Side	Register Name	Abbreviation	R/W	Address	Initial value	Access Size
L	PORT137 Port control register	PORT137CR	R/W	H'E6050089	H'A0	8,32
L	PORT138 Port control register	PORT138CR	R/W	H'E605008A	H'A0	8,32
L	PORT139 Port control register	PORT139CR	R/W	H'E605008B	H'A0	8,32
L	PORT140 Port control register	PORT140CR	R/W	H'E605008C	H'A0	8,32
L	PORT141 Port control register	PORT141CR	R/W	H'E605008D	H'A0	8,32
L	PORT142 Port control register	PORT142CR	R/W	H'E605008E	H'A0	8,32
L	PORT143 Port control register	PORT143CR	R/W	H'E605008F	H'A0	8,32
L	PORT144 Port control register	PORT144CR	R/W	H'E6050090	H'A0	8,32
L	PORT145 Port control register	PORT145CR	R/W	H'E6050091	H'A0	8,32
L	PORT146 Port control register	PORT146CR	R/W	H'E6050092	H'A0	8,32
L	PORT147 Port control register	PORT147CR	R/W	H'E6050093	H'A0	8,32
L	PORT148 Port control register	PORT148CR	R/W	H'E6050094	H'A0	8,32
L	PORT149 Port control register	PORT149CR	R/W	H'E6050095	H'A0	8,32
L	PORT150 Port control register	PORT150CR	R/W	H'E6050096	H'A0	8,32
L	PORT151 Port control register	PORT151CR	R/W	H'E6050097	H'A0	8,32
U	PORT152 Port control register	PORT152CR	R/W	H'E6053098	H'A0	8,32
U	PORT153 Port control register	PORT153CR	R/W	H'E6053099	H'A0	8,32
U	PORT154 Port control register	PORT154CR	R/W	H'E605309A	H'A0	8,32
U	PORT155 Port control register	PORT155CR	R/W	H'E605309B	H'A0	8,32
L	PORT156 Port control register	PORT156CR	R/W	H'E605009C	H'A0	8,32
L	PORT157 Port control register	PORT157CR	R/W	H'E605009D	H'A0	8,32
L	PORT158 Port control register	PORT158CR	R/W	H'E605009E	H'A0	8,32
L	PORT159 Port control register	PORT159CR	R/W	H'E605009F	H'A0	8,32

Side	Register Name	Abbreviation	R/W	Address	Initial value	Access Size
L	PORT160 Port control register	PORT160CR	R/W	H'E60500A0	H'10	8,32
L	PORT161 Port control register	PORT161CR	R/W	H'E60500A1	H'A0	8,32
L	PORT162 Port control register	PORT162CR	R/W	H'E60500A2	H'A0	8,32
L	PORT163 Port control register	PORT163CR	R/W	H'E60500A3	H'A0	8,32
L	PORT164 Port control register	PORT164CR	R/W	H'E60500A4	H'A0	8,32
L	PORT165 Port control register	PORT165CR	R/W	H'E60500A5	H'A0	8,32
L	PORT166 Port control register	PORT166CR	R/W	H'E60500A6	H'A0	8,32
R	PORT167 Port control register	PORT167CR	R/W	H'E60520A7	H'A1	8,32
R	PORT168 Port control register	PORT168CR	R/W	H'E60520A8	H'A1	8,32
R	PORT169 Port control register	PORT169CR	R/W	H'E60520A9	H'A1	8,32
R	PORT170 Port control register	PORT170CR	R/W	H'E60520AA	H'A1	8,32
R	PORT171 Port control register	PORT171CR	R/W	H'E60520AB	H'11	8,32
R	PORT172 Port control register	PORT172CR	R/W	H'E60520AC	H'E1	8,32
R	PORT173 Port control register	PORT173CR	R/W	H'E60520AD	H'A0	8,32
R	PORT174 Port control register	PORT174CR	R/W	H'E60520AE	H'A0	8,32
R	PORT175 Port control register	PORT175CR	R/W	H'E60520AF	H'A0	8,32
R	PORT176 Port control register	PORT176CR	R/W	H'E60520B0	H'A0	8,32
R	PORT177 Port control register	PORT177CR	R/W	H'E60520B1	H'A0	8,32
R	PORT178 Port control register	PORT178CR	R/W	H'E60520B2	H'E1	8,32
R	PORT179 Port control register	PORT179CR	R/W	H'E60520B3	H'11	8,32
R	PORT180 Port control register	PORT180CR	R/W	H'E60520B4	H'A0	8,32
R	PORT181 Port control register	PORT181CR	R/W	H'E60520B5	H'A0	8,32
R	PORT182 Port control register	PORT182CR	R/W	H'E60520B6	H'A0	8,32

Side	Register Name	Abbreviation	R/W	Address	Initial value	Access Size
R	PORT183 Port control register	PORT183CR	R/W	H'E60520B7	H'A0	8,32
R	PORT184 Port control register	PORT184CR	R/W	H'E60520B8	H'A0	8,32
R	PORT185 Port control register	PORT185CR	R/W	H'E60520B9	H'11	8,32
R	PORT186 Port control register	PORT186CR	R/W	H'E60520BA	H'A0	8,32
R	PORT187 Port control register	PORT187CR	R/W	H'E60520BB	H'A0	8,32
R	PORT188 Port control register	PORT188CR	R/W	H'E60520BC	H'A0	8,32
R	PORT189 Port control register	PORT189CR	R/W	H'E60520BD	H'A0	8,32
R	PORT190 Port control register	PORT190CR	R/W	H'E60520BE	H'A0	8,32
L	PORTL095_064 Data register	PORTL095_064DR	R/W	H'E6054008	H'00000000*3	32
L	PORTL127_096 Data register	PORTL127_096DR	R/W	H'E605400C	H'00000000*3	32
L	PORTL159_128 Data register	PORTL159_128DR	R/W	H'E6054010	H'00000000*3	32
L	PORTL191_160 Data register	PORTL191_160DR	R/W	H'E6054014	H'00000000*3	32
D	PORTD031_000 Data register	PORTD031_000DR	R/W	H'E6055000	H'00000000*3	32
D	PORTD063_032 Data register	PORTD063_032DR	R/W	H'E6055004	H'00000000*3	32
R	PORTR063_032 Data register	PORTR063_032DR	R/W	H'E6056004	H'00000000*3	32
R	PORTR095_064 Data register	PORTR095_064DR	R/W	H'E6056008	H'00000000*3	32
R	PORTR191_160 Data register	PORTR191_160DR	R/W	H'E6056014	H'00000000*3	32
U	PORTU127_096 Data register	PORTU127_096DR	R/W	H'E605700C	H'00000000*3	32
U	PORTU159_128 Data register	PORTU159_128DR	R/W	H'E6057010	H'00000000*3	32
L	PORTL095_064 Data set register	PORTL095_064DSR	R/W	H'E6054108/ H'E6074108*2	H'00000000*3	32
L	PORTL127_096 Data set register	PORTL127_096DSR	R/W	H'E605410C/ H'E607410C*2	H'00000000*3	32
L	PORTL159_128 Data set register	PORTL159_128DSR	R/W	H'E6054110/ H'E6074110*2	H'00000000*3	32
L	PORTL191_160 Data set register	PORTL191_160DSR	R/W	H'E6054114/ H'E6074114*2	H'00000000*3	32

Side	Register Name	Abbreviation	R/W	Address	Initial value	Access Size
D	PORTD031_000 Data set register	PORTD031_000DSR	R/W	H'E6055100/ H'E6075100*2	H'00000000*3	32
D	PORTD063_032 Data set register	PORTD063_032DSR	R/W	H'E6055104/ H'E6075104*2	H'00000000*3	32
R	PORTR063_032 Data set register	PORTR063_032DSR	R/W	H'E6056104/ H'E6076104*2	H'00000000*3	32
R	PORTR095_064 Data set register	PORTR095_064DSR	R/W	H'E6056108/ H'E6076108*2	H'00000000*3	32
R	PORTR191_160 Data set register	PORTR191_160DSR	R/W	H'E6056114/ H'E6076114*2	H'00000000*3	32
U	PORTU127_096 Data set register	PORTU127_096DSR	R/W	H'E605710C/ H'E607710C*2	H'00000000*3	32
U	PORTU159_128 Data set register	PORTU159_128DSR	R/W	H'E6057110/ H'E6077110*2	H'00000000*3	32
L	PORTL095_064 Data clear register	PORTL095_064DCR	R/W	H'E6054208/ H'E6074208*2	H'00000000*3	32
L	PORTL127_096 Data clear register	PORTL127_096DCR	R/W	H'E605420C/ H'E607420C*2	H'00000000*3	32
L	PORTL159_128 Data clear register	PORTL159_128DCR	R/W	H'E6054210/ H'E6074210*2	H'00000000*3	32
L	PORTL191_160 Data clear register	PORTL191_160DCR	R/W	H'E6054214/ H'E6074214*2	H'00000000*3	32
D	PORTD031_000 Data clear register	PORTD031_000DCR	R/W	H'E6055200/ H'E6075200*2	H'00000000*3	32
D	PORTD063_032 Data clear register	PORTD063_032DCR	R/W	H'E6055204/ H'E6075204*2	H'00000000*3	32
R	PORTR063_032 Data clear register	PORTR063_032DCR	R/W	H'E6056204/ H'E6076204*2	H'00000000*3	32
R	PORTR095_064 Data clear register	PORTR095_064DCR	R/W	H'E6056208/ H'E6076208*2	H'00000000*3	32
R	PORTR191_160 Data clear register	PORTR191_160DCR	R/W	H'E6056214/ H'E6076214*2	H'00000000*3	32
U	PORTU127_096 Data clear register	PORTU127_096DCR	R/W	H'E605720C/ H'E607720C*2	H'00000000*3	32
U	PORTU159_128 Data clear register	PORTU159_128DCR	R/W	H'E6057210/ H'E6077210*2	H'00000000*3	32
	AP block LSI internal communication interrupt/power reset function register*1	CCOMIFAP	R/W	H'E6058000 H'E6078000*2	H'00000000	32
	AP block LSI internal communication interrupt/power reset source register*1	CCOMIEAP	R	H'E6058004 H'E6078004*2	H'00000000	32
	AP block LSI internal	CCOMICAP	W	H'E6058008	H'00000000	32

Side	Register Name	Abbreviation	R/W	Address	Initial value	Access Size
	communication interrupt/power reset source clear register*1			H'E6078008*2		
	RT ->SYS LSI Internal communication interrupt/power reset function register*1	CCOMIFR2S	R/W	H'E6058060 H'E6078060*2	H'00000000	32
	RT ->SYS LSI Internal communication interrupt/power reset source register*1	CCOMIER2S	R	H'E6058064 H'E6078064*2	H'00000000	32
	RT ->SYS LSI Internal communication interrupt/power reset source clear register*1	CCOMICR2S	W	H'E6058068 H'E6078068*2	H'00000000	32
	SYS ->RT LSI Internal communication interrupt/power reset function register*1	CCOMIFS2R	R/W	H'E6058070 H'E6078070*2	H'00000000	32
	SYS ->RT LSI Internal communication interrupt/power reset source register*1	CCOMIES2R	R	H'E6058074 H'E6078074*2	H'00000000	32
	SYS ->RT LSI Internal communication interrupt/power reset source clear register*1	CCOMICS2R	W	H'E6058078 H'E6078078*2	H'00000000	32
	Module function select register1	MSEL1CR	R/W	H'E605800C	H'00000000	32
	Module function select register3	MSEL3CR	R/W	H'E6058020	H'00000000	32
	Module function select register4	MSEL4CR	R/W	H'E6058024	H'00000000	32
	USB Control register2	USBCR2	R/W	H'E605810C	H'0A0A orH'0A8A	16
	USB Control register4	USBCR4	R/W	H'E6058130	H'0A0A orH'0A8A	16
	USC Control register1	USCCR1	R/W	H'E6058144	H'0000	16
	USC Control register2	USCCR2	R/W	H'E6058146	H'0000	16
	CKO Control register	CKOCR	R/W	H'E6058110	H'0003	16
	WE0 Control register	WE0CR	R/W	H'E6058112	H'0003	16
	WE1 Control register	WE1CR	R/W	H'E6058114	H'0003	16
	MMCCLK0 Control register	MMCCLK0CR	R/W	H'E6058118	H'0003	16
	MMCCLK1 Control register	MMCCLK1CR	R/W	H'E605811A	H'0003	16

Side	Register Name	Abbreviation	R/W	Address	Initial value	Access Size
	SDHICLK0 Control register	SDHICLK0CR	R/W	H'E6058122	H'0003	16
	SDHICLK1 Control register	SDHICLK1CR	R/W	H'E6058124	H'0003	16
	SDHICLK2 Control register	SDHICLK2CR	R/W	H'E6058120	H'0003	16
	VCCQ Domain set register	VCCQ18CR	R/W	H'E6058180	H'0003	16
	VCCQ Domain(BSC Pins) Set register	VCCQBSCCR	R/W	H'E6058182	H'0003	16
	VCCQ Domain(VIO Pins) Set register	VCCQVIOCR	R/W	H'E6058184	H'0003	16
	VCCQ Domain(LCD Pins) Set register	VCCQLCDCR	R/W	H'E6058186	H'0003	16
	VCCQ Domain(MFI Pins) Set register	VCCQMFICR	R/W	H'E6058188	H'0003	16
	VCCQ3 Domain set register	VCCQ3CR	R/W	H'E605818A	H'0003	16
	VCCQ_MC0 Domain set register	VCCQMC0CR	R/W	H'E605818C	H'0003	16
	VCCQ_MC1 Domain set register	VCCQMC1CR	R/W	H'E605818E	H'0003	16
	IIC Control register	IICCR	R/W	H'E60581A0	H'8003	16
	CPORT GPI Register	CGPI	R	H'E60581C4	-	16
	CPORT GPOSR/GPOR Register	CGPOSR/CGPOR	R/W	H'E60581C6 H'E60781C6*2	H'0000	16
	CPORT GPOR2SSR/GPOR2SR Register	CGPOR2SSR/ CGPOR2SR	R/W	H'E60581CC H'E60781CC*2	H'0000	16
	CPORT GPOS2RSR/GPOS2RR Register	CGPOS2RSR/ CGPOS2RR	R/W	H'E60581CE H'E60781CE*2	H'0000	16
	USB PHY0 Interruption control registerAP	USBPHY0INTAP	R/W	H'E60781E0*2	H'0000	16
	USB PHY1 Interruption control registerAP	USBPHY1INTAP	R/W	H'E60781E2*2	H'0000	16

*1 For details, see section 5.6, LSI Internal Communication Interrupt/Power Reset (Request to the AP Block) and section 5.7, LSI Internal Communication Interrupt/Power Reset (Request to SYS from RT), section 5.8, LSI Internal Communication Interrupt/Power Reset (Request to RT from SYS).

*2 Accessing Address H'E605XXXX, It is controlled by the GPIO semaphore of HPB.

Accessing Address H'E607XXXX, It is not controlled by the GPIO semaphore of HPB.

*3 When the IE bit of PORTnCR is set to 1, the level of the corresponding pin is read.

G.54 Register Configuration of H-UDI

Register Name	Abbreviation	CPU Side				
		R/W	Logical Address	Physical Address	Size	Initial Value*1
Instruction register	SDIR	R	H'FC11 0000	H'FC11 0000	16	H'0EFF
Data register H	SDDR/SDDRH	R/W	H'FC11 0008	H'FC11 0008	32/16	Undefined
Data register L	SDDRL	R/W	H'FC11 000A	H'FC11 000A	16	Undefined
Interrupt source register	SDINT	R/W	H'FC11 0018	H'FC11 0018	16	H'0000
Bypass register	SDBPR*2	-	-	-	-	Undefined

*1 The low level of the TRST_N pin or the Test-Logic-Reset state of the TAP controller initializes to these values.

*2 SDBPR cannot be accessed from the CPU.

Register Name	Abbreviation	H-UDI Side		
		R/W	Size	Initial Value*1
Instruction register	SDIR	R/W	32	H'FFFF FFFD (fixed value*2)
Data register H	SDDR/SDDRH*4	-	-	-
Data register L	SDDRL*4	-	-	-
Interrupt source register	SDINT	W*3	32	H'0000 0000
Bypass register	SDBPR	R/W	1	Undefined

*1 The low level of the TRST_N pin or the Test-Logic-Reset state of the TAP controller initializes to these values.

*2 When reading via the H-UDI, the value is always H'FFFF FFFD.

*3 Only 1 can be written to the LSB by the H-UDI interrupt command.

*4 SDDR(SDDRH, SDDRL) cannot be accessed via the H-UDI.

G.55 Register Configuration of UBC

Register Name	Abbreviation	R/W	P4 Address	Area 7 Address	Access Size
Match condition setting register 0	CBR0	R/W	H'FF20 0000	H'FF20 0000	32

Register Name	Abbreviation	R/W	P4 Address	Area 7 Address	Access Size
Match operation setting register 0	CRR0	R/W	H'FF20 0004	H'FF20 0004	32
Match address setting register 0	CAR0	R/W	H'FF20 0008	H'FF20 0008	32
Match address mask setting register 0	CAMR0	R/W	H'FF20 000C	H'FF20 000C	32
Match condition setting register 1	CBR1	R/W	H'FF20 0020	H'FF20 0020	32
Match operation setting register 1	CRR1	R/W	H'FF20 0024	H'FF20 0024	32
Match address setting register 1	CAR1	R/W	H'FF20 0028	H'FF20 0028	32
Match address mask setting register 1	CAMR1	R/W	H'FF20 002C	H'FF20 002C	32
Match data setting register 1	CDR1	R/W	H'FF20 0030	H'FF20 0030	32
Match data mask setting register 1	CDMR1	R/W	H'FF20 0034	H'FF20 0034	32
Execution count break register 1	CETR1	R/W	H'FF20 0038	H'FF20 0038	32
Channel match flag register	CCMFR	R/W	H'FF20 0600	H'FF20 0600	32
Break control register	CBCR	R/W	H'FF20 0620	H'FF20 0620	32

G.56 Register Configuration of DBG

Register Name	Abbreviation	R/W	CPU Address*4	R/W	JTAG Command	Access Size
Debugging function selection register*3	DBGREG1	R/W	H'E610_0020/ H'E610_8020	R/W	B'0011_1000	32
LSI control register	DBGREG2	R/W	H'E610_0024/ H'E610_8024	R/W	B'1011_1000	32
KEY register	DBGREG9	R/W	H'E610_0040/ H'E610_8040	R/W	B'0010_0100	32
Access priority control register*3	DBGREG10	-	-*1	R/W	B'1010_0100	32

*1 Accessible only from the JTAG.

*2 Accessible from the CPU only under software control.

*3 Not a target for diagnosis.

*4 Address H'E610_0XXX is a non semaphore-address of this register and accessing through this address is not controlled by HPB semaphore.
Address H'E610_8XXX is a semaphore-address of this register and accessing thorough this address is controlled by HPB semaphore.

G.57 Register Configuration of USBHS0-DMAC

Register Name	Abbreviation	R/W	Address	Access Size
VCR register	USBDMA_VCR	R/W	USBDMA_BASE+H'00	32
Software reset register	USBDMA_SWR	R/W	USBDMA_BASE+H'08	32
DMA interrupt source register	USBDMA_DMICR	R	USBDMA_BASE+H'10	32
DMA source address register_0	USBDMA_SAR_0	R/W	USBDMA_BASE+H'20	32
DMA destination address register_0	USBDMA_DAR_0	R/W	USBDMA_BASE+H'24	32
DMA transfer count register_0	USBDMA_TCR_0	R/W	USBDMA_BASE+H'28	32
DMA timeout count register_0	USBDMA_TOCNTR_0	R	USBDMA_BASE+H'2C	32
DMA timeout constant register_0	USBDMA_TOCSTR_0	R/W	USBDMA_BASE+H'30	32
DMA channel control register_0	USBDMA_CHCR_0	R/W	USBDMA_BASE+H'34	32
DMA final transaction valid data transfer enable register_0	USBDMA_TEND_0	R/W	USBDMA_BASE+H'38	32
DMA source address register_1	USBDMA_SAR_1	R/W	USBDMA_BASE+H'40	32
DMA destination address register_1	USBDMA_DAR_1	R/W	USBDMA_BASE+H'44	32
DMA transfer count register_1	USBDMA_TCR_1	R/W	USBDMA_BASE+H'48	32
DMA timeout count register_1	USBDMA_TOCNTR_1	R	USBDMA_BASE+H'4C	32
DMA timeout constant register_1	USBDMA_TOCSTR_1	R/W	USBDMA_BASE+H'50	32
DMA channel control register_1	USBDMA_CHCR_1	R/W	USBDMA_BASE+H'54	32
DMA final transaction valid data transfer enable register_1	USBDMA_TEND_1	R/W	USBDMA_BASE+H'58	32
DMA operation register	USBDMA_DMAOR	R/W	USBDMA_BASE+H'60	32

Note: USBDMA_BASE=H'E68A0000

G.58 Register Configuration of USBHS1-DMAC

Register Name	Abbreviation	R/W	Address	Access Size

Register Name	Abbreviation	R/W	Address	Access Size
VCR register	USBDMA_VCR	R/W	USBDMA_BASE+H'00	32
Software reset register	USBDMA_SWR	R/W	USBDMA_BASE+H'08	32
DMA interrupt source register	USBDMA_DMICR	R	USBDMA_BASE+H'10	32
DMA source address register_0	USBDMA_SAR_0	R/W	USBDMA_BASE+H'20	32
DMA destination address register_0	USBDMA_DAR_0	R/W	USBDMA_BASE+H'24	32
DMA transfer count register_0	USBDMA_TCR_0	R/W	USBDMA_BASE+H'28	32
DMA timeout count register_0	USBDMA_TOCNTR_0	R	USBDMA_BASE+H'2C	32
DMA timeout constant register_0	USBDMA_TOCSTR_0	R/W	USBDMA_BASE+H'30	32
DMA channel control register_0	USBDMA_CHCR_0	R/W	USBDMA_BASE+H'34	32
DMA final transaction valid data transfer enable register_0	USBDMA_TEND_0	R/W	USBDMA_BASE+H'38	32
DMA source address register_1	USBDMA_SAR_1	R/W	USBDMA_BASE+H'40	32
DMA destination address register_1	USBDMA_DAR_1	R/W	USBDMA_BASE+H'44	32
DMA transfer count register_1	USBDMA_TCR_1	R/W	USBDMA_BASE+H'48	32
DMA timeout count register_1	USBDMA_TOCNTR_1	R	USBDMA_BASE+H'4C	32
DMA timeout constant register_1	USBDMA_TOCSTR_1	R/W	USBDMA_BASE+H'50	32
DMA channel control register_1	USBDMA_CHCR_1	R/W	USBDMA_BASE+H'54	32
DMA final transaction valid data transfer enable register_1	USBDMA_TEND_1	R/W	USBDMA_BASE+H'58	32
DMA operation register	USBDMA_DMAOR	R/W	USBDMA_BASE+H'60	32

Note: USBDMA_BASE=H'E68C0000

SH7372
User's Manual: Hardware

Publication Date: Rev. 0.54 Nov. 26, 2010
Published by: Renesas Electronics Corporation

© 2009, 2010. Renesas Electronics Corporation, All rights reserved.

SH7372
Hardware Manual

Renesas Electronics Corporation